Using the Synopsys TetraMAX Model with Artisan 130nm - 250nm ASL Memory Generators

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Revision History

Part Number	Release Number	Release Date	Comments
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Using the Synopsys TetraMAX Model

After generating the Synopsys TetraMAX model file, <*name*>.tv, check the models using the following steps. You can choose the instance name, <*name*>.

Generate the TetraMAX model, <*name*>.tv, with top module <*name*>.

Generate the Verilog model, <*name*>.v, with top module <*name*>.

Generate a TetraMAX script file, tmax.scr, with the following contents:

```
set netlist
read netlist <name>.tv
report violation -all
run build_model <name>
add clocks 0 CLK
run drc
set atpg -capture_cycles 6
remove faults -all
add fault -all
run atpg fast_sequential_only
report_faults - all
write patterns <name>.tb.v -format verilog_single -Replace
quit
```

In adding clocks to the script above (i.e., `add clocks 0 CLK`), list all possible clocks. For example, if you have dual-port SRAM or two-port register file memories, use `CLKA` and `CLKB` instead of `CLK`.

This script contains commands that run Automatic Test Pattern Generation (ATPG) on one instance of memory and generate test vectors in Verilog format. Verilog simulations can be run using the test vector file and the Verilog model of memories using any supported Verilog simulator.

The following example demonstrates a TetraMAX simulation using VCS.

To run TetraMAX in batch mode, enter:

```
tmax -shell tmax.scr > & tmax.log
```

To run a Verilog simulation using VCS, enter:

```
vcs <name>_tb.v <name>.v > vcs.log
./simv >> ! vcs.log
```

The log generated by TetraMAX, tmax.log, should not include any error messages. However, there may be some warning messages. These can be ignored since they have been verified with the tool vendor. You must test the vcs.log file to verify that the VCS simulation passed without any mismatch.