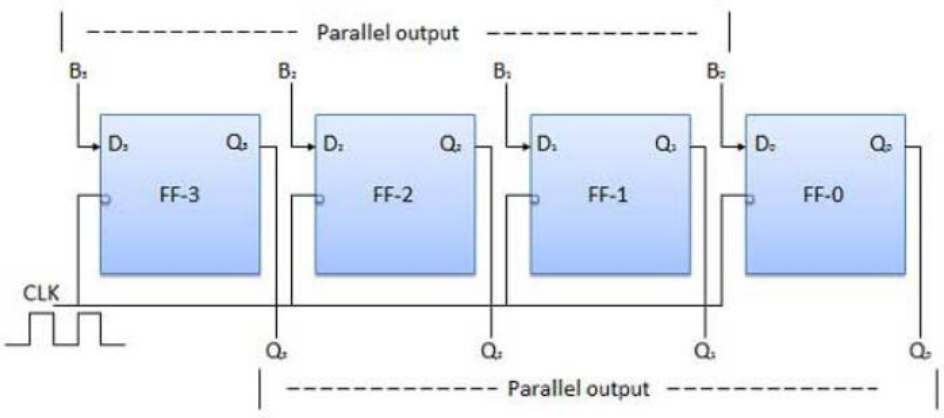
https://esim.fossee.in/circuit-simulation-project

Name of the participant : Dynaneshwari S Jangale

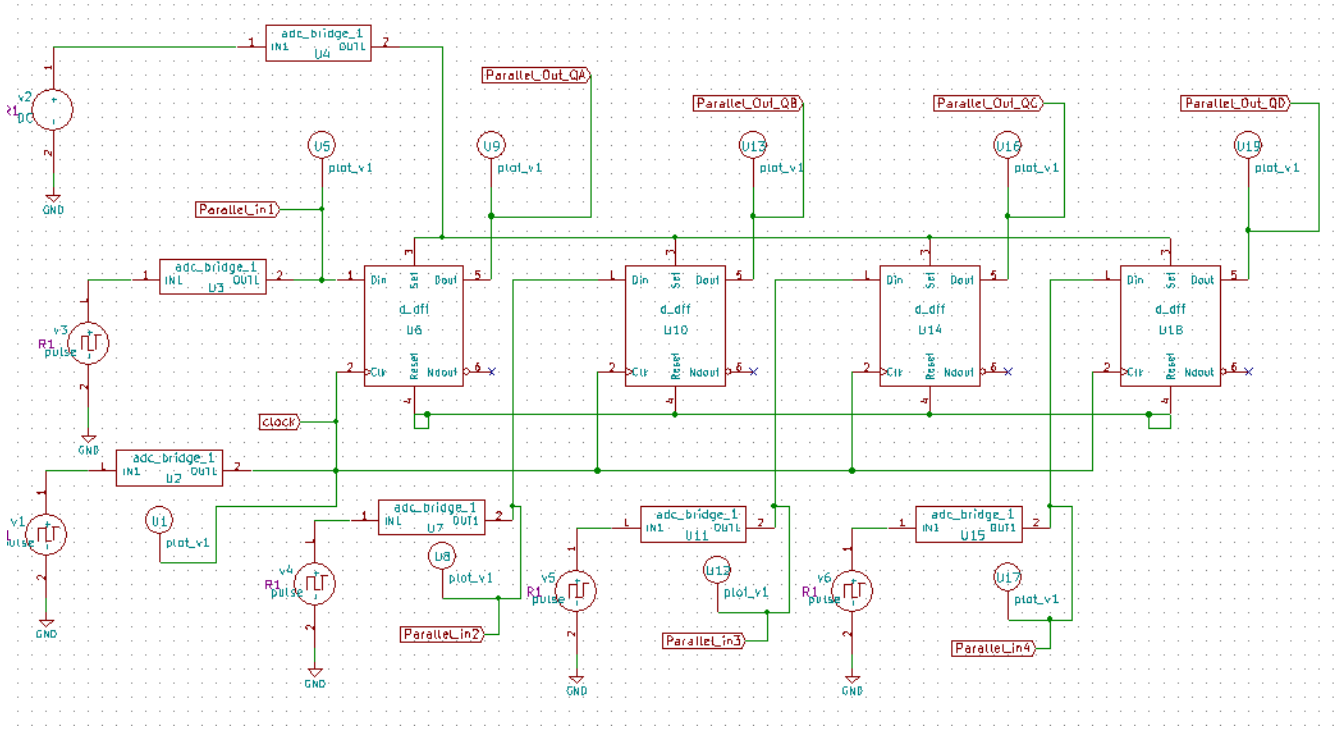
Title of the circuit : Parallel in Parallel out shift register

Theory/Description :

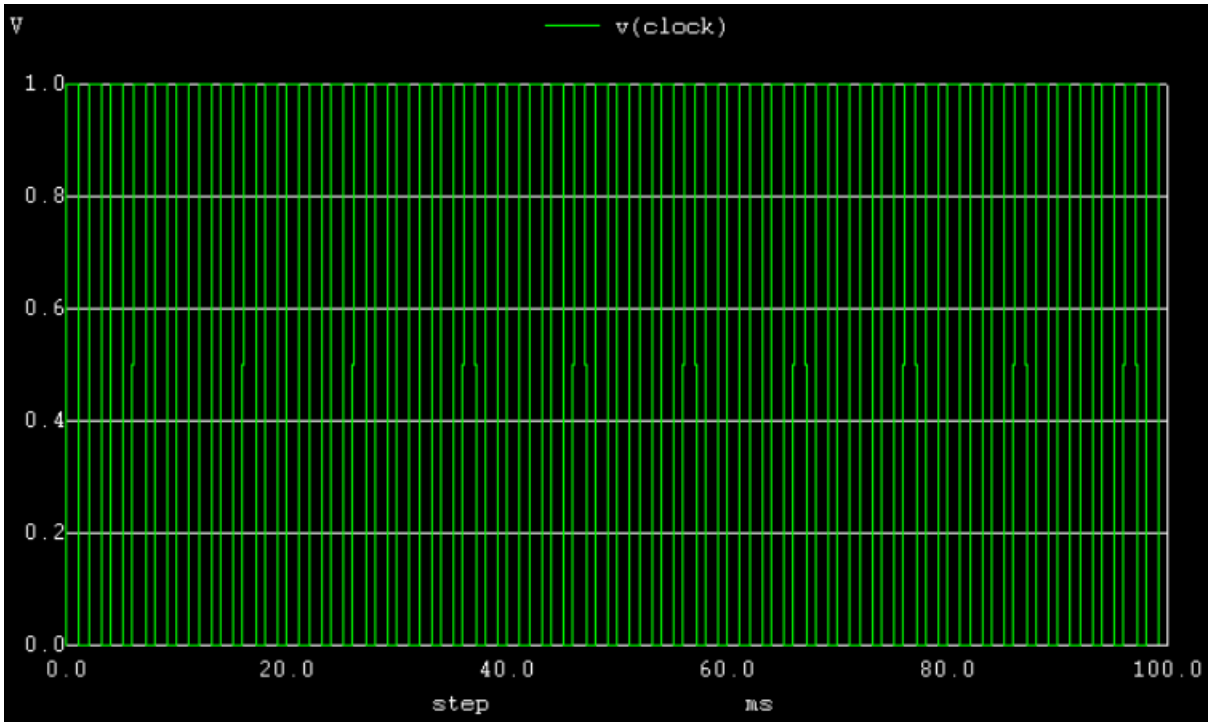
In this mode, the 4 bit binary input B0, B1, B2, B3 is applied to the data inputs D0, D1, D2, D3 respectively of the four flip-flops. As soon as a negative clock edge is applied, the input binary bits will be loaded into the flip-flops simultaneously. The loaded bits will appear simultaneously to the output side. Only clock pulse is essential to load all the bits.

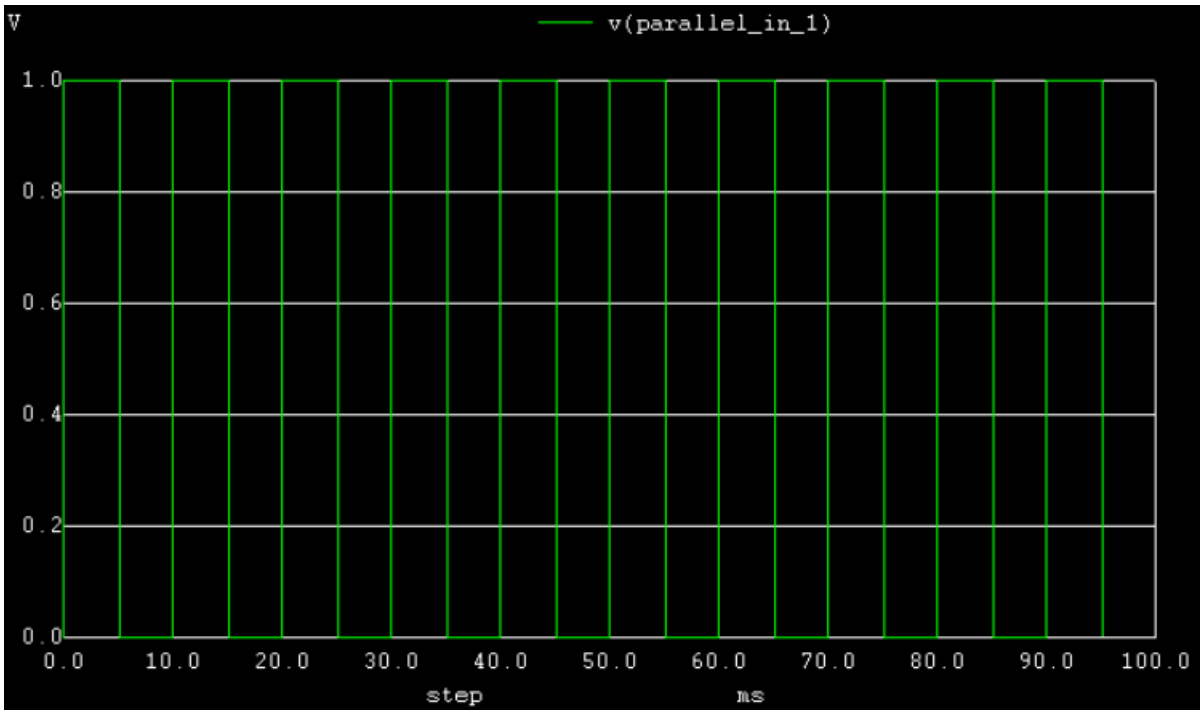


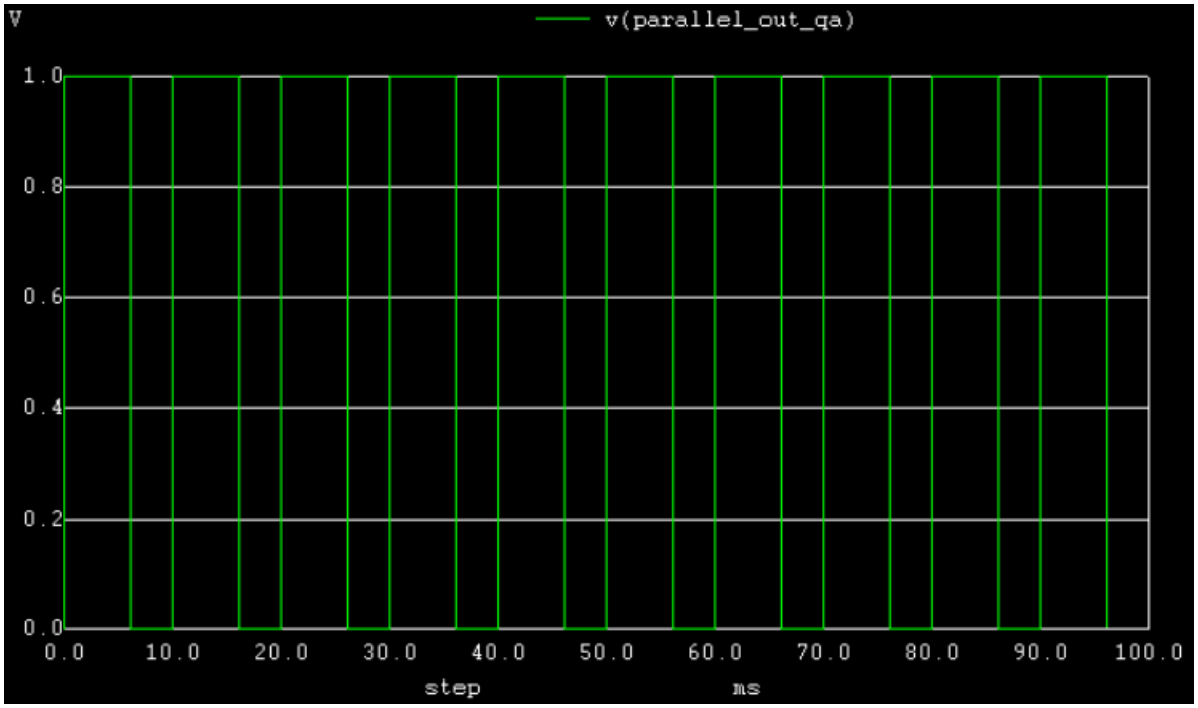
Circuit Diagram(s) :

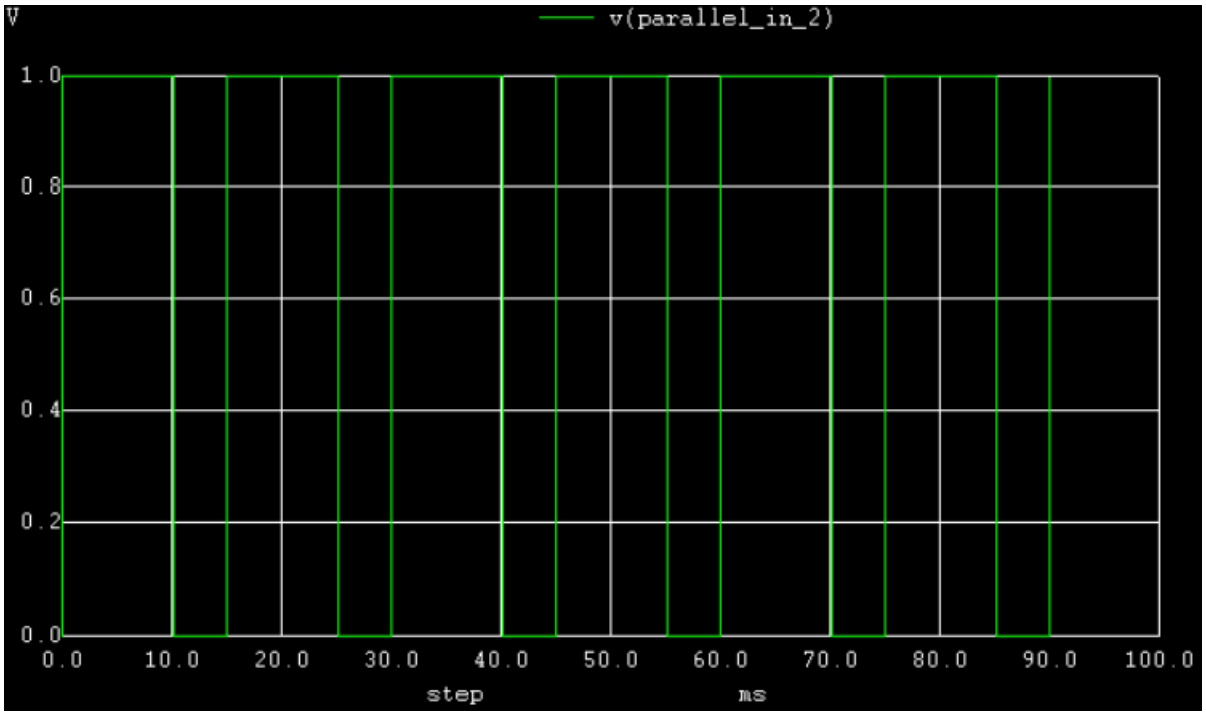


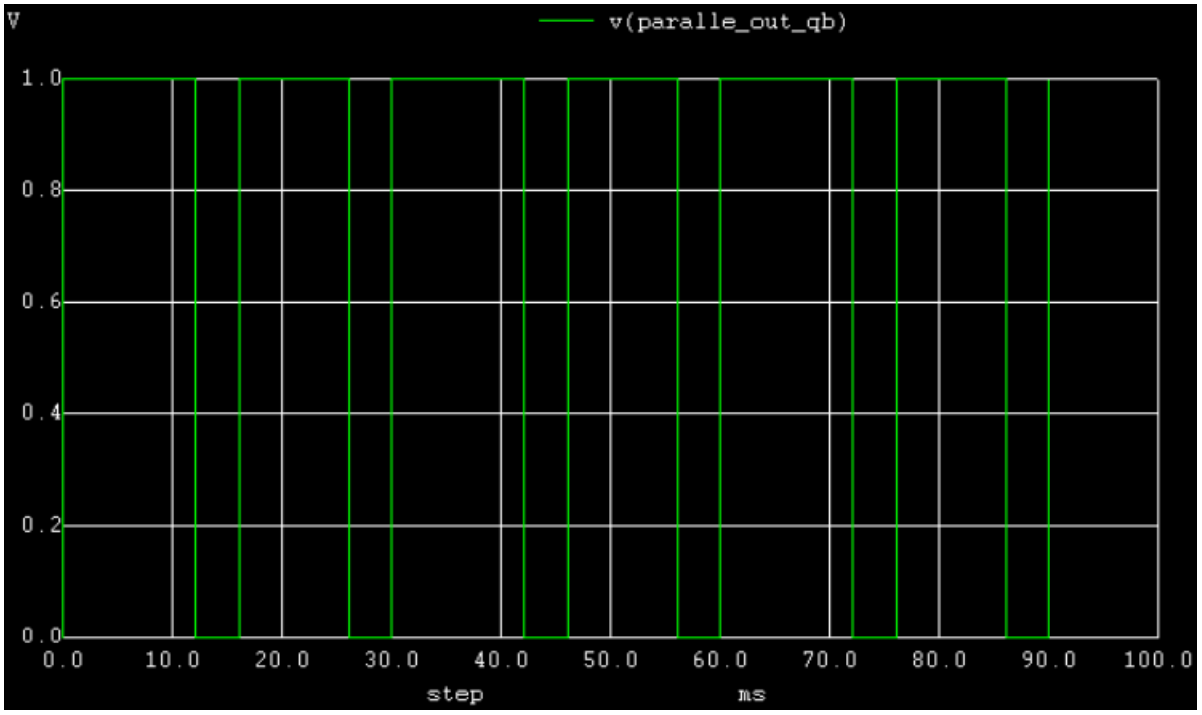
Results (Input, Output waveforms and/or Multimeter readings) :

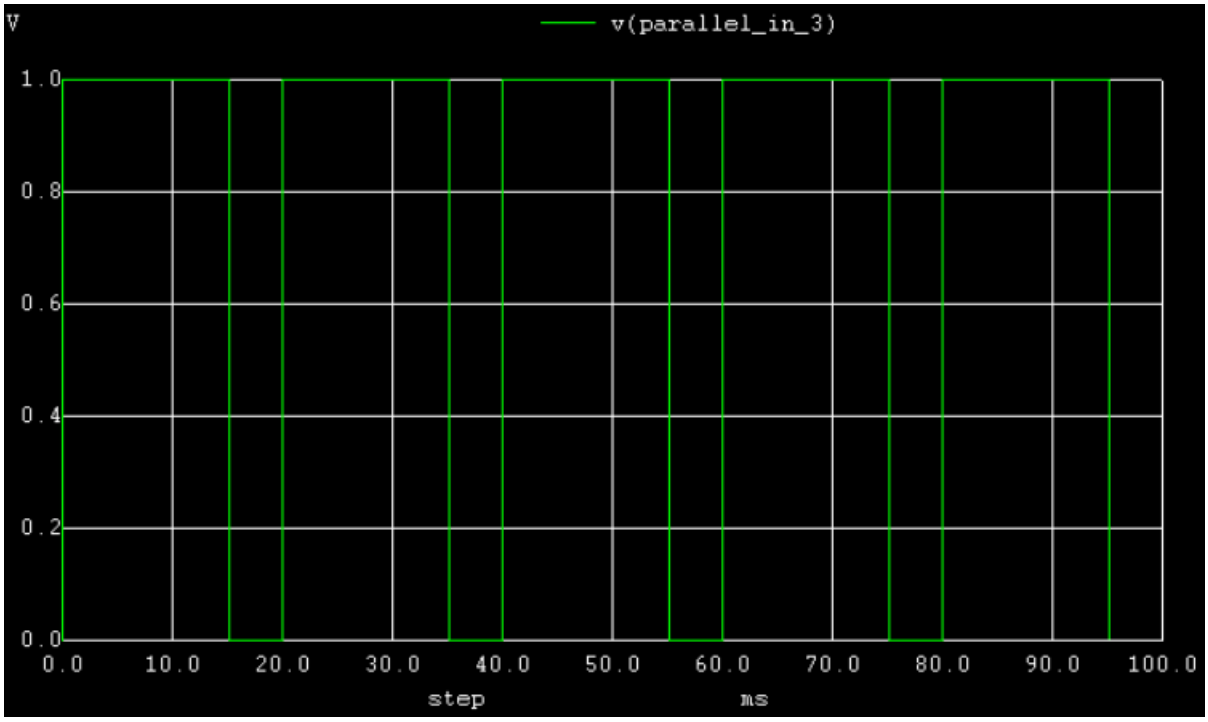


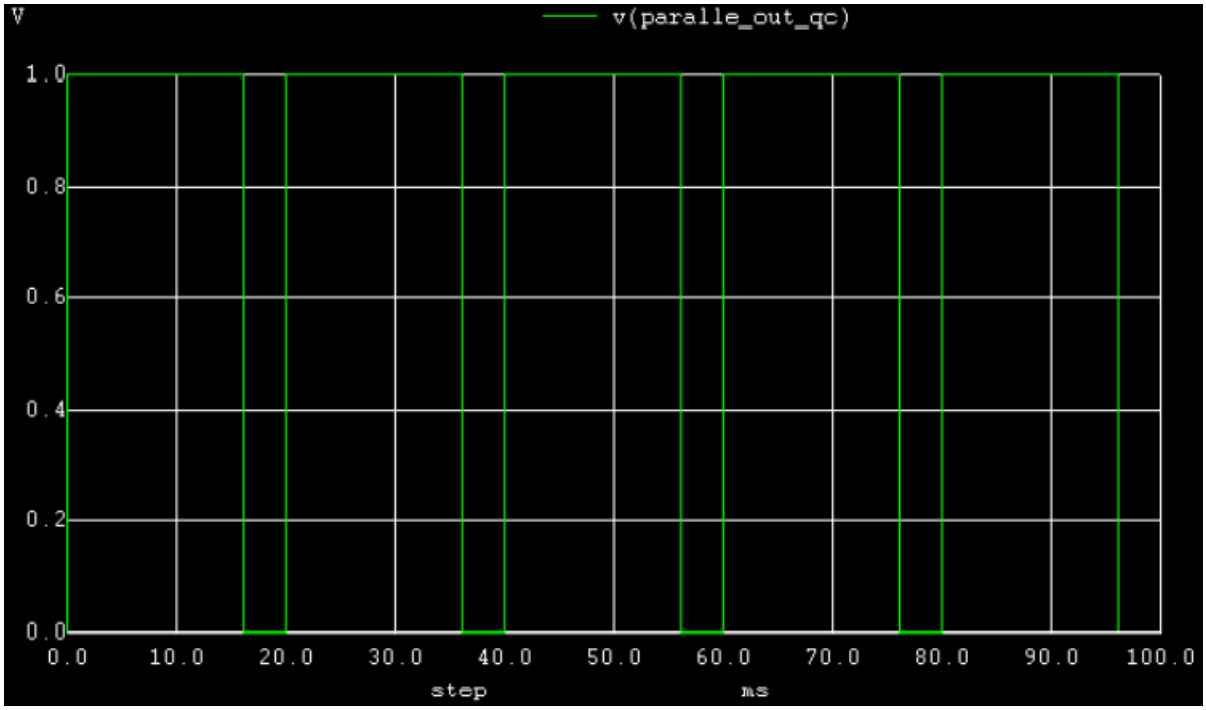


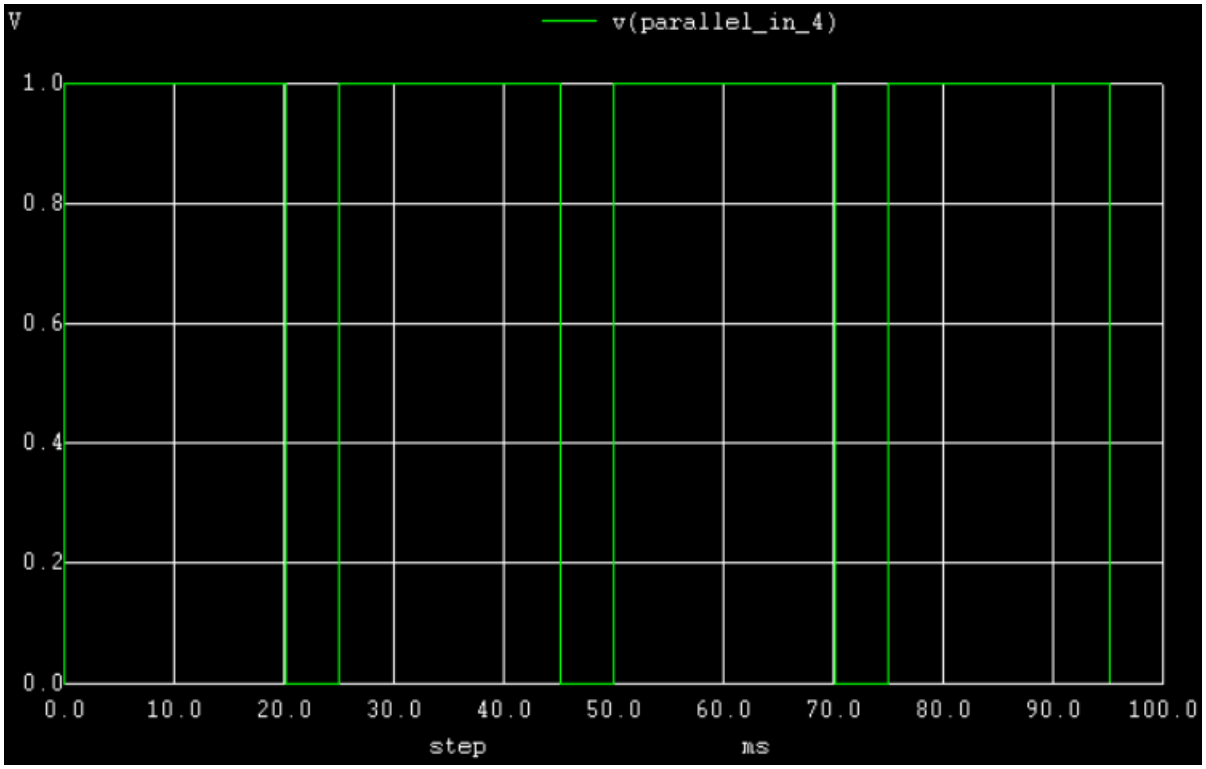

V
v(parallel_out_qa)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms

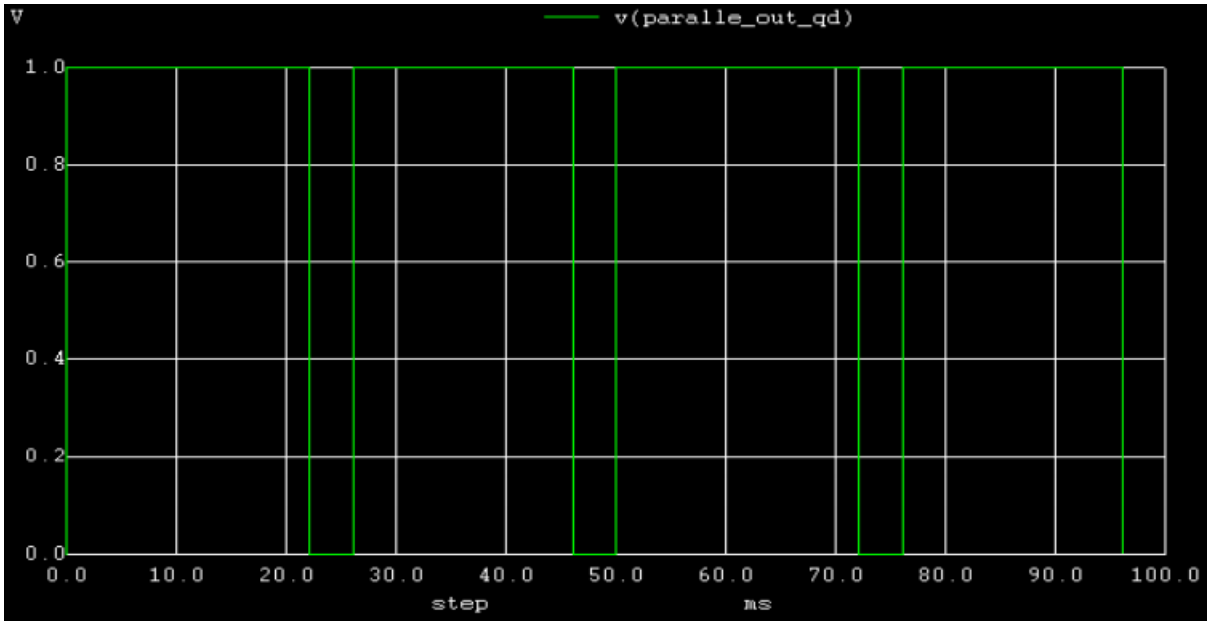

V
v(parallel_in_2)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms


V
v(paralle_out_qb)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms


V
v(parallel_in_3)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms


V
v(paralle_out_qc)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms


V
v(parallel_in_4)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms



Source/Reference(s) :

https://www.tutorialspoint.com/computer_logical_organization/digital_registers.htm