**Computer Organization 2018**

**HOMEWORK 0 Traffic\_light**

**Due date:**

**Overview**

這次作業的主要目的為複習verilog語言和熟悉開發環境，請實作出紅綠燈的簡單verilog

模組，運用有限狀態機的設計方式來設計本作業。

**General rules for deliverables**

* You need to complete this homework INDIVIDUALLY. You can discuss the homework with other students, but you need to do the homework by yourself. You should not copy anything from someone else, and you should not distribute your homework to someone else. If you violate any of these rules, you will get NEGATIVE scores, or even fail this course directly
* When submitting your homework, compress all files into a single zip file, and upload the compressed file to Moodle.
  + Please follow the file hierarchy shown in Figure 1.

**F740XXXXX (your id )(folder)**

**SRC ( folder) \* Store your source code**

**F740XXXXX\_Report.docx (Project Report. The report template is already included. Follow the template to complete the report.)**

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| Figure 1. File hierarchy for homework submission |

* **Important!** DO NOT submit your homework in the last minute. Late submission is not accepted.
* You should finish all the requirements (shown below) in this homework and Project report.

**Homework Description**

紅綠燈控制模組的示意圖如下：

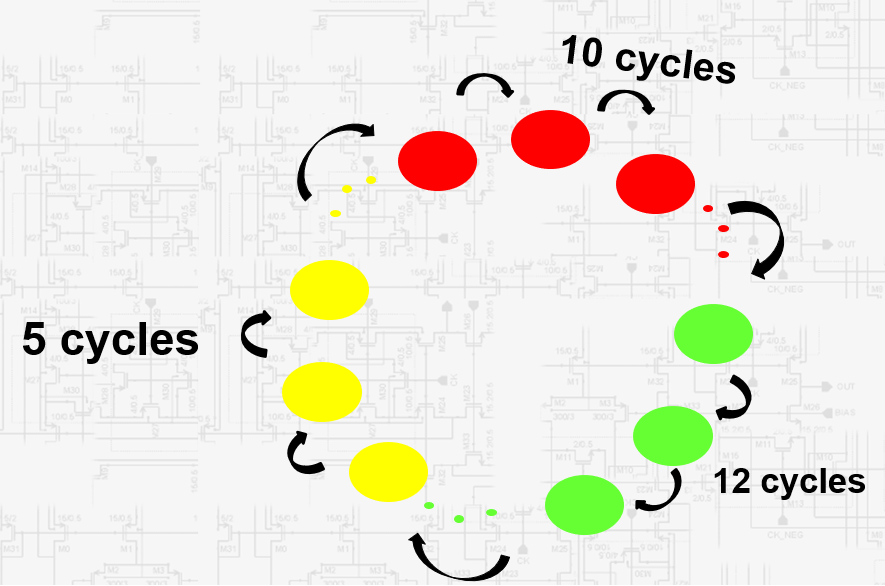


Figure 2. 紅綠燈狀態圖

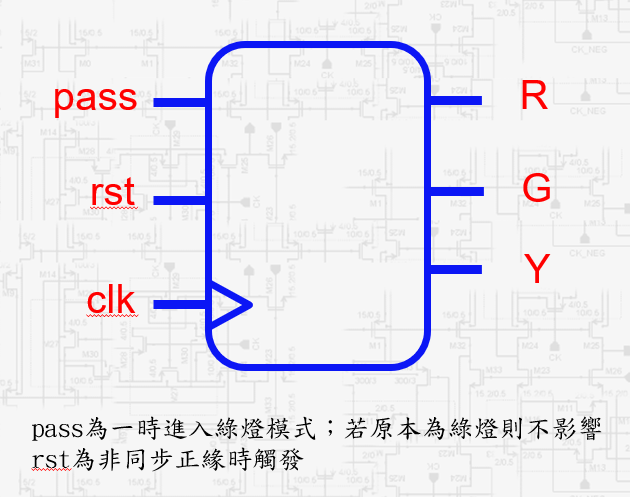


Figure 3. 紅綠燈控制模組的示意圖

作業規則如下：

1. 紅綠燈每27個cycles一個循環，綠燈維持12個cycles，切換成黃燈維持5個cycles，再切換成紅燈維持10個cycles，電路為clock**正緣觸發**。
2. 輸入訊號：
   1. pass：1bit訊號，當pass為1時，若當前狀態非綠燈，強制切換成綠燈第一個cycle，若原本為綠燈則不改變燈號和cycle。當pass為0則沒有任何動作。
   2. rst：1bit訊號，非同步正緣時觸發，將燈號狀態設成紅燈第1個cycle。
   3. clk：1bit clock訊號。
3. 輸出訊號：
   1. R：1bit訊號，代表紅燈的輸出訊號。
   2. G：1bit訊號，代表綠燈的輸出訊號。
   3. Y：1bit訊號，代表黃燈的輸出訊號。

三個輸出訊號同時間只有一個訊號為1。

**Homework Requirements**

1. 完成traffic\_light.v的設計。
2. 用modelsim教學中的步驟，將traffic\_light.v和traffic\_light\_tb.v放入modelsim專案中執行模擬。
3. 根據報告格式完成report.docx，記得更改檔名。

判斷nextstate 是啥 將nextstate放到state 判斷output

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