Our project aims to develop automatic clock gating for registers to reduce dynamic power consumption. We used yosys to get the gate level netlist in Verilog and we plan to replace its input multiplexor by a clock gating cell. To do that we wrote the RTL code for register and clock gating cell then generated the gate level netlist using yosys tool to get familiar with their gate level netlist design. Then we looked for a tool to help us parse and edit Verilog code “pyverilog tool”. We used the tool to lookup for sky130A pdk flip flops and we managed to reach a way to implement this function using python. We appended to the gate level netlist of “spm.v” and generated “spm.gl\_new.v” with the new cells of gating clock we want to replace them with, but we still working in how to replace them with each other. At this stage we are still working on our script and we are seeking more knowledge about python functions and power reduction evaluation methods.

To run the sample script we made on spm.gl.v 🡪 python3 main.py