Detailed Block Diagram Friday, April 24, 2020 1:50 AM DROUT PC out SPOUT Components: In /out signals 1. Constrol Signalo: 1 MOX I (85't mux) 2 MAR (FF) 1 PCOUT (8) 2 DROUT (8) 3 SPOUT (8) (0 to 1) MUX1_sel MARIOGA MEMWE (1) 3 MEM (RAM) M0×1 MUX2 sel DRIOAD (0 to 0) 4 MUX2 5 DR(ff) (1) PC (counter) IR (Pf) PCclr (1) Jump (1) Acout MARin DR-~ PC inc (1) MUX3 (1) IRload MUX3_sel ALV2 (24) 2A 01 (1) ACLBAD 11 MUX4 MUX4_sel (0 to 0) 12 MUX5 SPin 13 R (9F) SPdir (1) Spload Vres 14 ALUI (1) 15 3P (counter) Spent (1) DRout & MAROUT -LUI-op Rload 16 Z (16.4 PF) (1) 17 OR8 17 PCload ONA PI MUX5_sel Address (1) 19 OR 2 10ad MEM cond Memout Acout MUXZ result DR'm DR load - penable 8 8 DROUT DROUTER 8 ALUZOUT SPort DROUT PCCIT _ SCIT data data ALU 2 7R-99 PC_count MUX3 IR load MUX3-3el result result 8 8 PCout ALUZOUT Acin DROUT 18 data Ac lead MUX4 AC_ FF enable Vres AC out result Acout 8/ POR 8 Acout SPin R load enable MUXS R . ff ALU1 MUX5-341 ALUI-OP FJ 0297 result 8 ALUS out 8 R out 2000t 2 2 Z load enable Jump AND PCload ACE DR: ACLORD = 1 MUX3501=0 ACK AC+R: Acload=1 MUX3sel= 1 ALU100=0 AC + AC @ R: AC load = 1 MUx35e(= 1 ALUI Op= 1 DR & AC : DR load = 1 MUx2 sel= 1 DR & MEM[MAR] = DRIOAd=1 MUX 2 sel= 0 IR - DR: IRload MAR - PC: MARISad=1 MUX1 Sel = 00 MAR - DR: MARIOAS=1 MUX1 sel = 01 MAR + Sp: MARIOad=1 MUx 1 sel= 10 MEM[MAR] & DR: MEMWe = 1 PC & O: PC load = 0 PCclr = 1 PC CPC+1: PC load=0 Pc mc = 1 PC - DR : PCload=1 R + AC: Rload = 1 SPE-SP+1: SPload=0 SPdir=1 SPant = 1 SP - SP-1: SPload=0 SP div = 0 SPcn+=1 SPE DR: 5Pload=1 MUX4sel=0 SPESP+DR: SPload=1 MUX4 sel = 1 2 € V : 2 load = 1 MUX5 sel= 1

Z > NOT V: Zload = 1

MUX5501= 0