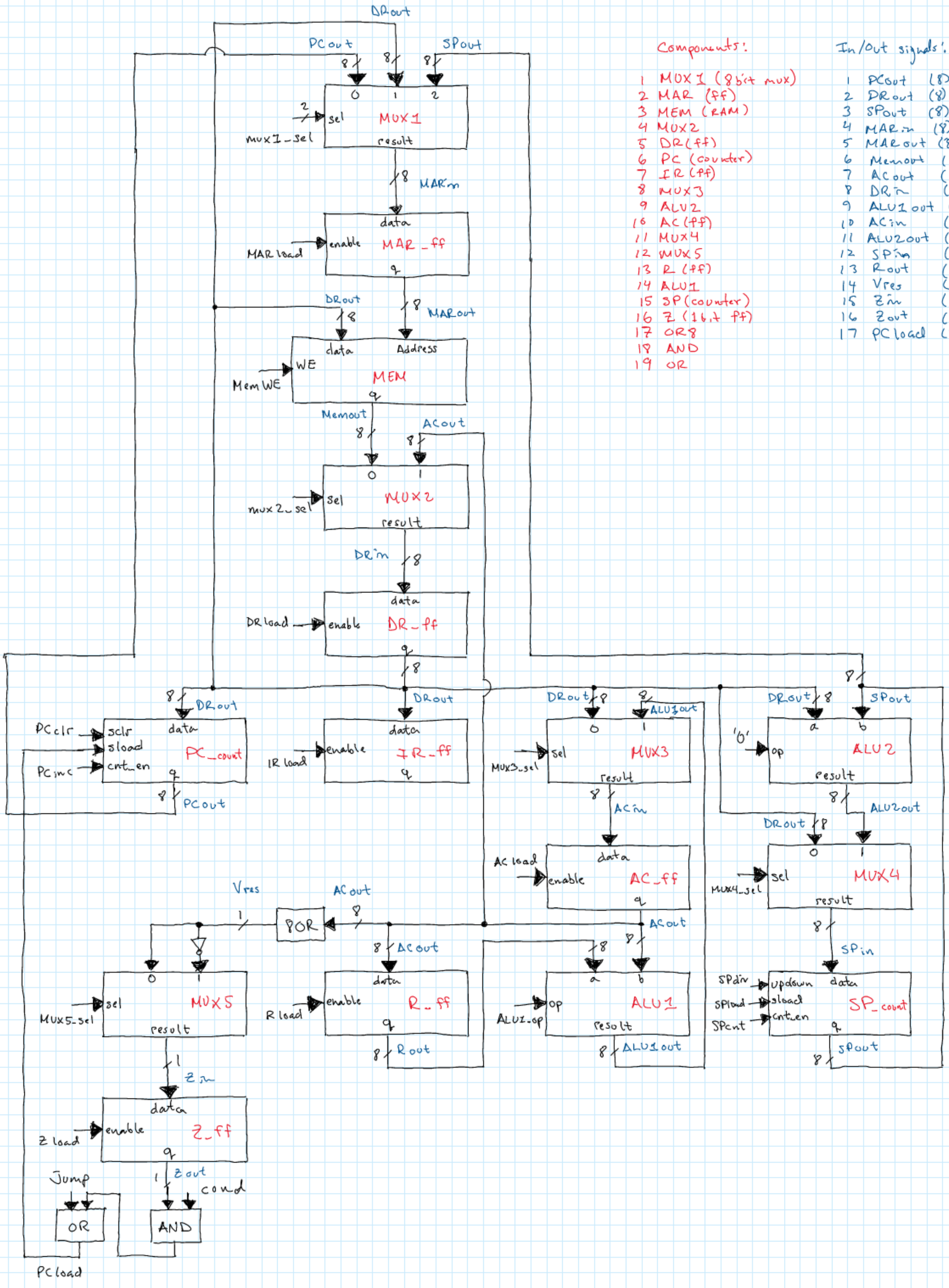
Detailed Block Diagram

Friday, April 24, 2020 1:50 AM



Components:	
1	MUX 1 (8 bit mux)
2	MAR (ff)
3	MEM (RAM)
4	MUX2
5	DR (ff)
6	PC (counter)
7	IR (ff)
8	MUX3
9	ALU2
10	AC (ff)
11	MUX4
12	MUX5
13	R (ff)
14	ALU1
15	SP (counter)
16	Z (1 bit ff)
17	OR8
18	AND
19	OR

In/Out signals:		
1	PCout	(8)
2	DRout	(8)
3	SPout	(8)
4	MARin	(8)
5	MARout	(8)
6	Memout	(8)
7	ACout	(8)
8	DRin	(8)
9	ALU1out	(8)
10	ACin	(8)
11	ALU2out	(8)
12	SPin	(8)
13	Rout	(8)
14	Vres	(1)
15	Zin	(1)
16	Zout	(1)
17	PCload	(1)

Control Signals:		
1	MUX1_sel	(0 to 1)
2	MARload	(1)
3	MEMWE	(1)
4	MUX2_sel	(0 to 0)
5	DRload	(1)
6	PCclr	(1)
7	Jump	(1)
8	PCinc	(1)
9	IRload	(1)
10	MUX3_sel	(0 to 0)
11	ACload	(1)
12	MUX4_sel	(0 to 0)
13	SPdir	(1)
14	SPload	(1)
15	SPcnt	(1)
16	ALU1_op	(1)
17	Rload	(1)
18	MUX5_sel	(0 to 0)
19	Zload	(1)
20	cond	(1)

AC ← DR : ACload = 1
MUX3sel = 0

AC ← AC + R : ACload = 1
MUX3sel = 1
ALU1op = 0

AC ← AC ⊕ R : ACload = 1
MUX3sel = 1
ALU1op = 1

DR ← AC : DRload = 1
MUX2sel = 1

DR ← MEM[MAR] : DRload = 1
MUX2sel = 0

IR ← DR : IRload

MAR ← PC : MARload = 1
MUX1sel = 00

MAR ← DR : MARload = 1
MUX1sel = 01

MAR ← SP : MARload = 1
MUX1sel = 10

MEM[MAR] ← DR : MEMwe = 1

PC ← 0 : PCload = 0
PCclr = 1

PC ← PC + 1 : PCload = 0
PCinc = 1

PC ← DR : PCload = 1

R ← AC : Rload = 1

SP ← SP + 1 : SPload = 0
SPdir = 1
SPcnt = 1

SP ← SP - 1 : SPload = 0
SPdir = 0
SPcnt = 1

SP ← DR : SPload = 1
MUX4sel = 0

SP ← SP + DR : SPload = 1
MUX4sel = 1

Z ← V : Zload = 1
MUX5sel = 1

Z ← NOT V : Zload = 1
MUX5sel = 0