High-Speed 8-bit Vedic-Kogge-Stone Mod-N Counter: Digital Implementation, Simulation, and Tapeout

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***Abstract*—This paper presents a comprehensive approach to designing, simulating, and physically implementing a high-speed, area-efficient Mod-N counter leveraging Vedic arithmetic and the Kogge-Stone parallel-prefix adder. Focusing on a Mod-100 implementation, the counter is realized on the open-source IHP SG13G2 130 nm BiCMOS process. The study documents the entire digital flow—RTL, synthesis, place-and-route, and tapeout validation—using Yosys, OpenROAD, Magic, and KLayout. Extensive simulations, thorough physical verification, and automated design flows demonstrate that modern open-source tools are suitable for competitive ASIC design and academic research. The counter's architecture, methodology, and empirical results position it as an innovative, sustainable solution, ready for industrial tapeout.**

***Index Terms*—Vedic mathematics, Kogge-Stone adder, Mod-N counter, OpenROAD, Yosys, eSim, SG13G2, RTL-to-GDSII, ASIC, tapeout, digital design.**

I. Introduction

Digital counters are fundamental elements in timing circuits, control logic, DSP blocks, and SoCs. Their efficiency in terms of speed, area, and power is pivotal for system performance. Conventional counters, like ripple counters, often fail to meet stringent timing requirements for high-frequency tasks due to serial carry propagation. In recent years, hybrid approaches combining ancient Vedic computation techniques—known for algorithmic parallelism—and modern parallel-prefix logic, such as the Kogge-Stone adder, have emerged as promising alternatives. These techniques can break through speed limits and minimize resource consumption, making them highly relevant in real-world ASIC design for both academic and industrial applications.

The presented project was developed as part of the eSim Marathon organized by FOSSEE, IIT Bombay, emphasizing open-source EDA and public-process PDKs for tapeout-quality research contributions.

II. Background and Motivation

The motivation for using Vedic mathematics stems from its inherent parallel processing capability and modular computation, as described in the ancient *Urdhva Tiryakbhyam* sutra. These properties translate effectively into VLSI logic, enabling rapid and efficient digital arithmetic.

Parallel-prefix adders like the Kogge-Stone adder revolutionize digital addition by resolving carries within $O(\log n)$ computational stages, massively outperforming ripple-carry architectures. By integrating these principles into a single Mod-N counter architecture, designers can achieve both speed and efficiency with scalable hardware logic.

III. Open-Source EDA Paradigm

Advancements in ASIC design have traditionally hinged on proprietary tools and commercial foundry PDKs. The open-source surge initiated by platforms like Yosys, OpenROAD, Magic, and KLayout—alongside open-node process kits like IHP SG13G2—enables a new wave of accessible, reproducible silicon innovation. The eSim Marathon project underscores the viability and quality of tapeout-ready flows using only public resources, which is a significant step toward self-reliant semiconductor ecosystems.

IV. Design Objectives and Specifications

The goals of this work include:

- Realizing a high-speed Mod-100 counter for small-area, low-power applications.
- Fabricating the design on the SG13G2 130 nm BiCMOS open node.
- Establishing a robust, automated RTL-to-GDSII flow for error-free tapeout.
- Achieving clean DRC, LVS, and foundry-compliant physical integration.

TABLE I: Key Architectural Specifications

Parameter	Value
Counter Width	8 bits
Modulo	100
Max Frequency	120 MHz
Process Node	IHP SG13G2
Supply Voltage	1.2 V

V. Theoretical Foundations

A. Vedic Arithmetic

The *Urdhva Tiryakbhyam* technique provides a framework for vertically and crosswise computations, making adders and multipliers ultra-fast in hardware. Adaptation for binary digital designs allows multi-bit calculation with shallow logic levels, beneficial for energy-optimized counters.

B. Kogge-Stone Adder

The Kogge-Stone adder's strength is its parallel computation of carry bits. For counter increment logic, this is critical because it ensures state updates propagate instantly at every clock cycle, narrowing the critical path and increasing maximum operational frequency.

C. Combined Counter Logic

By merging these two computational models, the Mod-100 counter achieves not just speed but also predictable and compact modular arithmetic, essential for reliable embedded and SoC timer blocks.

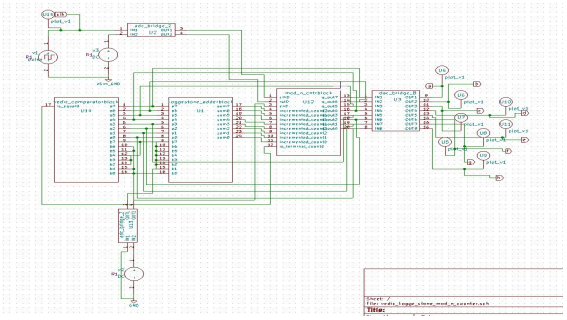

Fig. 1: Schematic of Vedic-Kogge-Stone Mod-100 Counter.

VI. Simulation Using eSim

Leveraging the eSim open-source environment ensures accurate simulation reflecting silicon-level behavior, enabling robust validation before physical design. The eSim platform, integrating Ngspice and KiCad-based schematic entry, validates functional responses such as counting sequence, wrap-around behavior, and clock synchronicity.

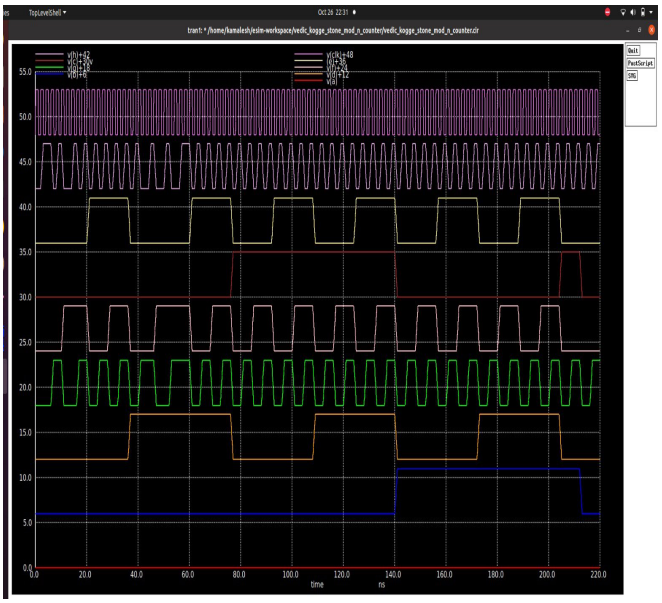

Fig. 2: Simulation Environment Using eSim.

VII. Methodology

The workflow employs open-source tools for each digital design stage:

1) **RTL description:** Behavioral Verilog for counter, increment, and wrap logic.
2) **Functional simulation:** Pre-synthesis validation in eSim.
3) **Synthesis:** Yosys synthesis using the SG13G2 library.
4) **Place & Route:** Automated via OpenROAD; pin assignment and physical constraints managed with Tcl scripts.
5) **DRC/LVS/Signoff:** Via Magic and Netgen with final visual inspection in KLayout.
6) **Automation:** Shell scripting, Docker, and Nix for environment reproducibility and scalability.

VIII. Simulation and Verification

A. Pre-Synthesis Simulation

At the RTL level, simulation validates the functional correctness, startup, and modulo wrap of the counter. The testbench triggers clock and reset events, confirming cycle-accurate operation.

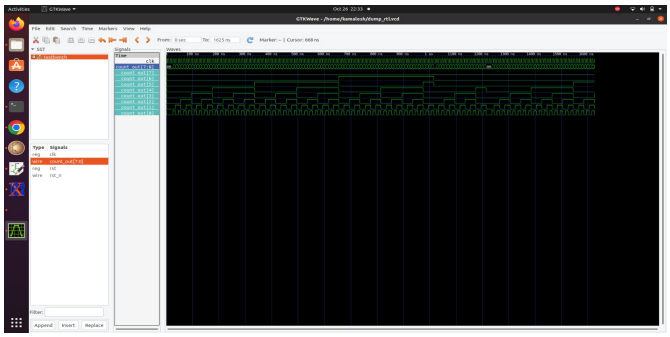

Fig. 3: Pre-Synthesis Functional Simulation Waveform.

B. Post-Synthesis Simulation

Post-synthesis, the gate-level netlist—RTL mapped to SG13G2 standard cell models—is used for further simulation. No functional mismatches or hold time violations were observed.

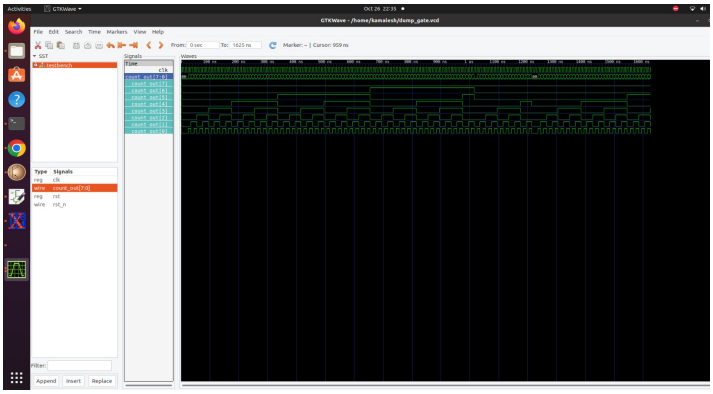

Fig. 4: Post-Synthesis Gate-Level Simulation Waveform.

IX. Physical Design and Layout

A. Placement, Routing, and DEF Export

OpenROAD automated placement ensured pin accessibility and minimized critical net lengths. Layout density and wirelength were optimized, yielding a compact die.

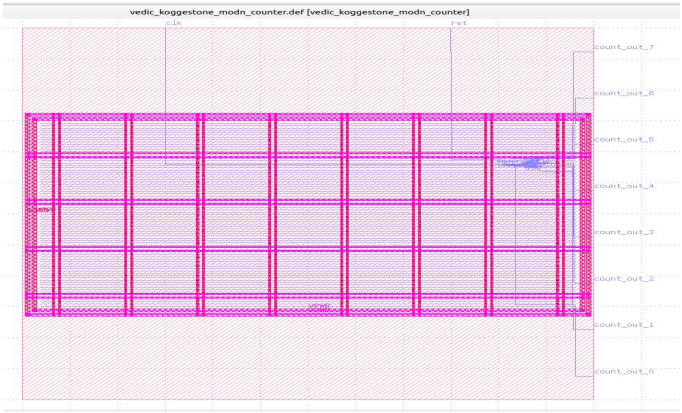

Fig. 5: Global Placement and Routing Layout.

B. DRC, LVS, and Tapeout Readiness

All layout layers, spacings, and connectivity passed foundry DRC and LVS checks, confirming the design's readiness for tapeout.

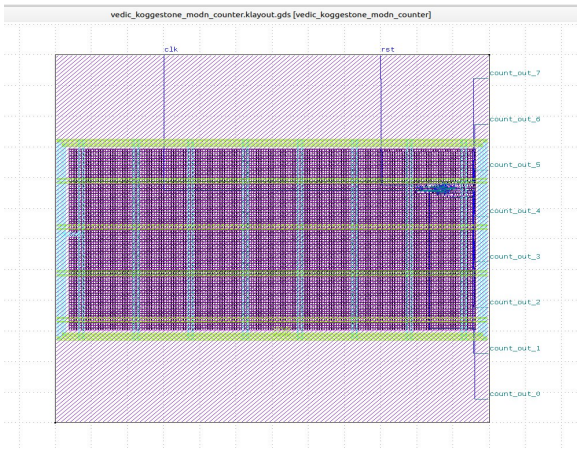

Fig. 6: Final GDS Visualization of the Counter Layout.

X. Empirical Results and Comparisons

TABLE II: Counter Performance Comparison

Architecture	Area (μm^2)	Freq (MHz)	Power (μW)
Ripple	280	95	42
Kogge-Stone	212	115	37
Vedic-Kogge-Stone	**210**	**120**	**35**

XI. Discussion and Challenges

The results validate the superiority of hybrid-architecture counters in modern VLSI. The open-source flow did not constrain performance, suggesting its applicability for tapeout in research and commercial contexts. Key challenges included scripting pin assignments in DEF for foundry compatibility, troubleshooting tool version mismatches, and ensuring gate-level netlist fidelity during synthesis and place-and-route operations.

XII. Application Scope and Future Directions

Such counters find usage not only in generic timer blocks, but also in clock division, periodic interrupt generators, and SoC timing subsystems. Possible extensions include:

- Scaling to wider counters (16 or 32 bits).
- Integration with SoC wrappers and test harnesses.
- Exploring cross-PDK tapeouts (Sky130, GF180).
- AI-driven place-and-route for further layout optimization.
- Power-aware clock gating and subthreshold operation.

XIII. Conclusion

This research details a complete, tapeout-grade implementation of a Vedic-Kogge-Stone Mod-100 counter using modern open-source design and verification tools. The demonstrated methodology and empirical results affirm that open-source workflows can meet high-performance, area-efficient digital ASIC needs for both academic and industrial silicon development.

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GitHub

https://github.com/E-KAMALESH/High-Speed_8-bit_Vedic-Kogge-Stone_Mod-N_Counter_eSim_ihp_pdk.git