Elisa Tsai (Wentao Cai)

elisa@mail.ustc.edu.cn | 187-5602-2840 | Github: github.com/E-Tsai

EDUCATION

University of Science and Technology of China (USTC)   Hefei, PRC
School of Computer Science and Technology   *Expected June 2020*

Relevant Coursework: Alogorithms (A), Operating Systems (A), Introduction to Computing Systems (A-),
Computer Networks (A), Graph Theory (A), Digital Logic Lab (A),
Introduction to Artificial Intelligence (A-).

RESEARCH INTERESTS

My research interests mainly lie in computer systems, security and architecture. I am also interested in music related programming.

RESEARCH EXPERIENCE

Research Assistant at EFES Lab   Ann Arbor, USA
Advised by Prof. Kasikci, University of Michigan Ann Arbor   *2019.7.1 - present*

- **Assembly/C Programming, Security**: Worked on defenses for speculative execution attacks: the DOLMA paper (in submission of ASPLOS 2020), providing mitigation for all known spectre-like attacks on hardware level.
  * Realized single micro-op version of spectre attack with D-cache and BTB as side channel, implemented on gem5.
  * Realized a spectre variant with BTB as side channel on real hardware (intel processors: i7 and Xeon), ruled out noises with statistic method.

INDUSTRY EXPERIENCE

An Intranet Distributed Version-Control System   Chengdu, PRC
Internship, Sinux Co.,Ltd.   *2017.8 - 2017.9*

- **Front-end**: Participated in developing an intranet distributed version-control web application, using java for back-end and vue as front-end framework.

REPRESENTING PROJECTS

Teaching Assistant for Operating Systems class, Spring 2019   Hefei, PRC
Worked with Prof. Xianglan Chen, University of Science and Technology of China   *2019.2 - 2019.7*

- **Teaching**: Worked as a Teaching Assistant for class of Operating System Principles And Implementation Spring 2019. Provided lectures for the course projects. I also worked as the grader for student projects and tests.
- **Assembly/C Programming**: Helped to redesign and made improvements for the course project: a simple operating system from bootstrap, which supports multi-processing and dynamic memory management, run on QEMU.
  * Started from boot loader written in x86 assembly, provided a walk through of a typical BIOS/MBR boot process.
  * Implemented several scheduling policies, including multilevel feedback queue, as well as dynamic memory management.
  * Provided improvements for the future projects: IPC, interruption handling, file systems, etc.
- **Documentation**: Writing a gitbook tutorial for the future course project.

International Genetically Engineered competition (Gold Medal)   Boston, USA
Member of USTC Software team   *2017.5 - 2017.11*

- **Frond-end and Python**: Built a web application for synthetic biology community, focusing on more efficient Biobricks information retrieval and convenient biological ideas sharing. It is constructed on the basis of iGEM's official database.
  * Website: Back-end written in python, front-end using vue as framework.
  * Search Engine: A powerful search engine against DNA sequences which conform to a restriction-enzyme assembly standard.
  * Plugin System: Allows users to develop new functions and integrated them into the platform.

Acked Patches For Linux Kernel
Open Source   *2019.1 - present*

- **C Programming**: Submitted patches of device drivers for Linux kernel.
  * Replaced deprecated APIs into more proper ones.
  * Fixed code style problems by using code style checker like checkpatch.pl and coccinelle.

An A Cappella generation framework   Hefei, PRC
Advised by Prof. Zengfu Wang, University of Science and Technology of China   *2018.6 - 2018.11*

- **ML, Speech Synthesis**: An Acappella generation framework based on machine learning and speech synthesis. I started this project since I like singing and want to shorten my song recording process.
  * Built a frame work for pitch recognition and recognizing chord progression.

* Extracted voice feature and speech synthesis (with provided project).

Personal Project: Elisa's Tech Blog

2017 - present

- **Blog**: Powered by Hexo and Github Pages, maintained since 2017 (blogs mainly written in Chinese).
  - Tech related: Translated and wrote blogs about systems (Linux kernel).

REPRESENTING COURSE PROJECTS

A JIT Compiler For C1 Language   USTC, PRC
Computer Architecture Class Project   _2018 Fall_

- **C++ Programming**: Implemented a compiler written with LLVM for C1 language, a subset of C.
  - Realized a C1 language recognizer library built with ANTLR v4, constructing an abstract syntax tree on given source input.
  - Generated assembly code from the given AST with LLVM IRBuilder, using CLI to transfer C1 code into LLVM IR.

A RISC-V 32I Pipeline Processor in Verilog   USTC, PRC
Compilers Class Project   _2019 Spring_

- **Verilog Programming**: Implemented a pipelined RISC-V 32I processor. The code is synthesizable and can be run on an FPGA.
  - ISA: Implemented all instructions in RISC-V 32I except FENCE, CSR, ECALL and EBREAK.
  - Out-of-order Execution: Implemented 5 stage pipeline, data forwarding, load/use stalling and hazard handling.
  - Branch Prediction Unit: Implemented a 2-bit predictor and BTB.
  - Cache Optimization: Experimented with associativity, size, blocksize, etc. to optimize performance.

Bank Management System with Web Control Interface   USTC, PRC
Database Class Project   _2019 Spring_

- **Database, Front-end, python**: Developed a web application for bank management. Using open source bootstrap framework for front-end, Flask framework for backend, and MySQL for database.

ENGLISH PROFICIENCY

- TOEFL: 113 (Speaking: 25).
- GRE: 321 (Verbal: 154; Quantity: 167) + Writing: 4.

AWARDS AND HONORS

- Outstanding Student Scholarship (2016) - First prize.
- Outstanding Student Scholarship (2017) - Third prize.

SKILLS

- **Software Programming**: x86 Assembly, C, C++, Bash, Python, Julia.
- **Web Development**: HTML, JavaScript, MySQL, Flask, Chrome DevTools.
- **Software Engineering**: Git Workflow, Software Testing and Debugging Tools.
- **Others**: Linux, Docker, Verilog (FPGA), LLVM.