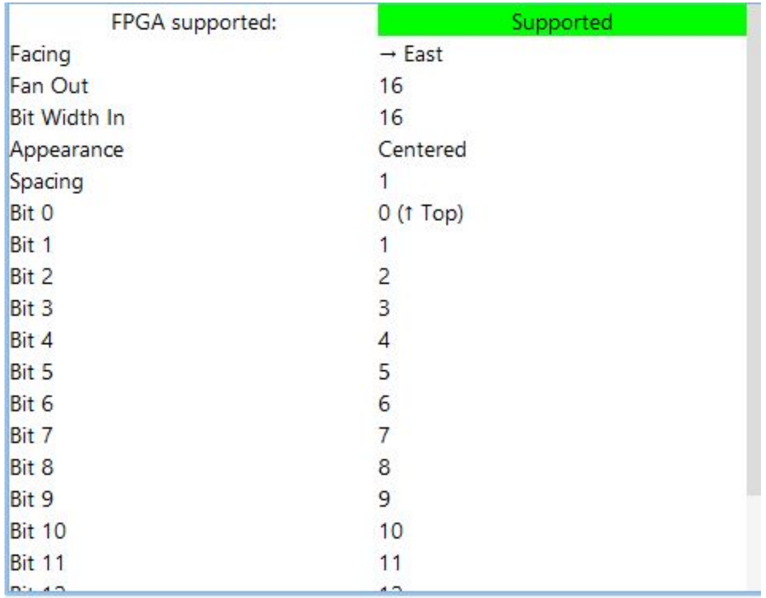
# Lab 6

61C Summer 2023

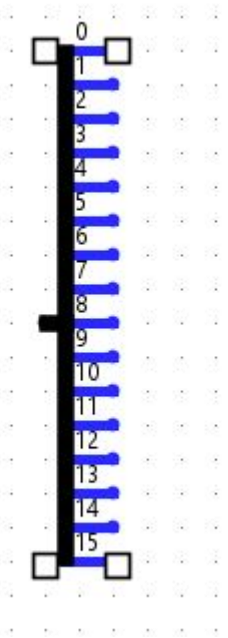
## Useful Logisim Components

## Splitters

- Split multibit inputs into individual bits or ranges of bits

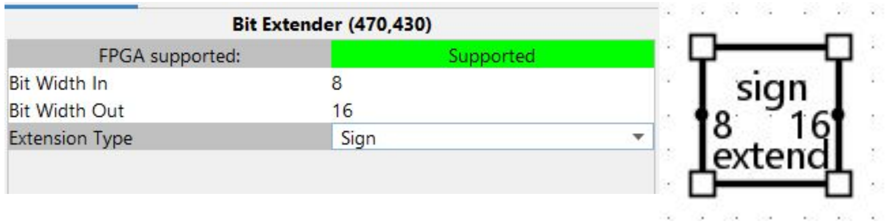


| | |
|---|---|
| FPGA supported: | Supported |
| Facing | → East |
| Fan Out | 16 |
| Bit Width In | 16 |
| Appearance | Centered |
| Spacing | 1 |
| Bit 0 | 0 (↑ Top) |
| Bit 1 | 1 |
| Bit 2 | 2 |
| Bit 3 | 3 |
| Bit 4 | 4 |
| Bit 5 | 5 |
| Bit 6 | 6 |
| Bit 7 | 7 |
| Bit 8 | 8 |
| Bit 9 | 9 |
| Bit 10 | 10 |
| Bit 11 | 11 |



## Bit Extenders

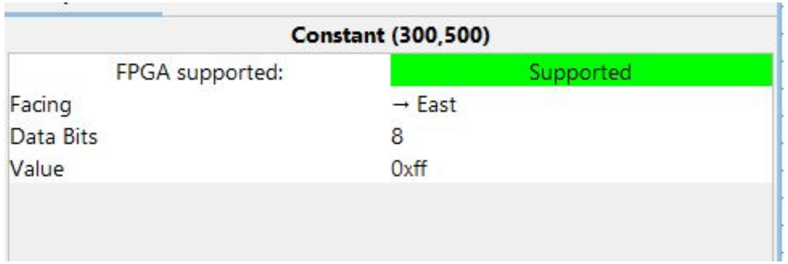
- Extends the input bit to chosen output bit width
- Choose extension types like signed or zero extended


Bit Extender (470,430)

| | |
|---|---|
| FPGA supported: | Supported |
| Bit Width In | 8 |
| Bit Width Out | 16 |
| Extension Type | Sign |

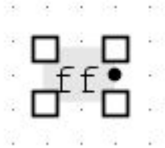
## Constants

- Constant values, useful for comparators



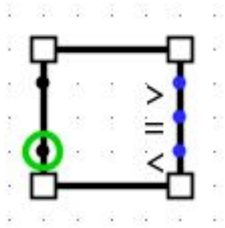
Constant (300,500)

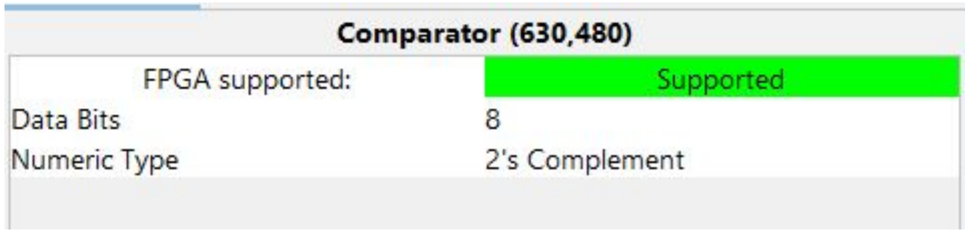
|  |  |
|---|---|
| FPGA supported: | Supported |
| Facing | → East |
| Data Bits | 8 |
| Value | 0xff |



# Comparators

- Compares two different values in either unsigned or two's complement



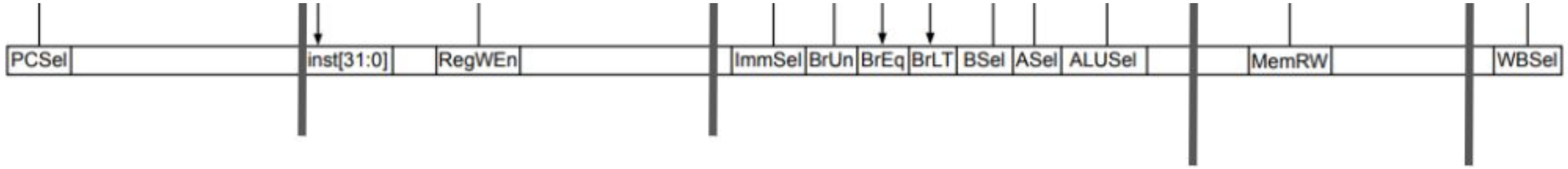


**Comparator (630,480)**

| | |
|---|---|
| FPGA supported: | Supported |
| Data Bits | 8 |
| Numeric Type | 2's Complement |

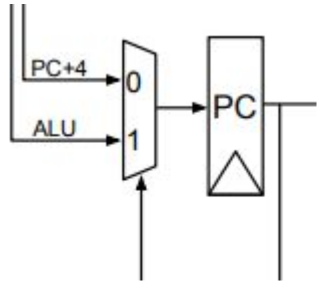
# Control Review

- The “brain” of the datapath
- Decodes the instruction and provides selectors(PCSel, ImmSel, BrUn) to the rest of the datapath elements



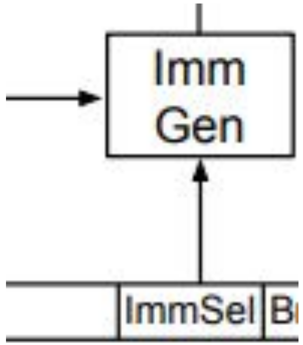
## 2.1 c)

- PCSel:
  - 0 corresponds with PC+4 (no branch)
  - 1 corresponds with ALU (PC + IMM)
  - For branching instructions, PCSel is known after EX



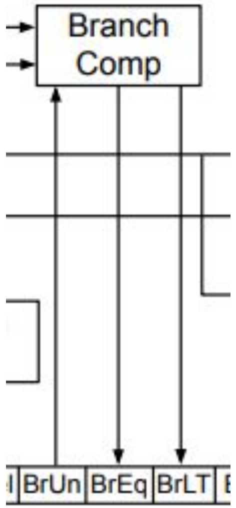
## 2.1 c)

- ImmSel:
  - ImmSel can be I, B, S, J, U



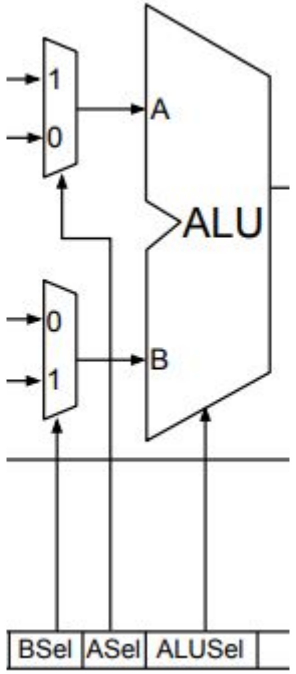
## 2.1 c)

- BrUn, BrEq, BrLt:
  - Control outputs BrUn to branch comp
  - Branch comp returns BrEq and BrLT according to BrUn
  - BrUn is only 1 for unsigned branch instructions



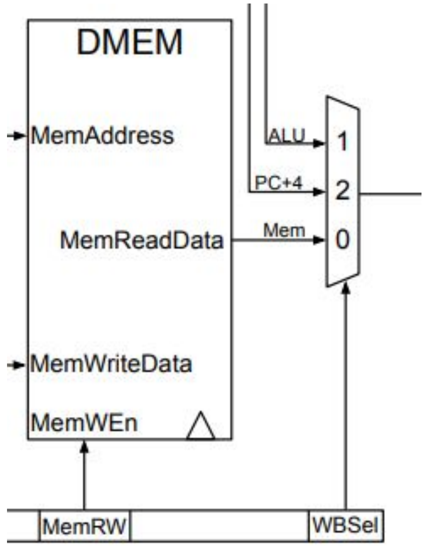
## 2.1 c)

- BSel, ASel:
  - 1 for ASel corresponds to PC, 0 corresponds to rs1
  - 1 for BSel corresponds to Imm, 0 corresponds to rs2
- ALUSel:
  - Chooses which operation
  - 16 different values, corresponding to operations like add, ori, etc.



## 2.1 c)

- MemRW:
    - Value of 1 allows for writes to memory, and vice versa for 0
- WBSel:
    - Chooses which value gets passed to regfile to be saved



## Timing Review

- We go from state element to state element (register to register)

$$t_{clk-to-q} + t_{logic,Max} + t_{setup} \le t_{clk-period}$$

$$t_{clk-to-q} + t_{logic,Min} \ge t_{hold}$$

## Pipelining

- Maximizes efficiency by allowing for higher clock frequency
- To pipeline, we put registers between stages to hold intermediate values
- To consider timing when it comes to pipelined circuits, consider the delay of each stage and clock period will be determined by the stage with max delay