Add two numbers

2002 (1) Accept 1st A ⇒ One single Instruction → (1) Fetch
(2) Decode
(3) Execute.

2003 (2) Accept 2nd B ⇒ "

2004 (3) Add A+B ⇒ C ⇒

2005 (4) Output C

PC → Addr. of next Instruction
CIR → 2002
MAR → Memory Add. Reg.
AC → Accumulator.
MDR → Memory data Reg ⇒

Address bus → A_0 – A_7

Unidirectional

Data bus → D_0 – D_7

Bidirectional

Control bus →

$\overline{RD}$, $\overline{WR}$

$\overline{MEMR}$; $\overline{IOR}$

MEMW ; $\overline{IOW}$

1 - Bit

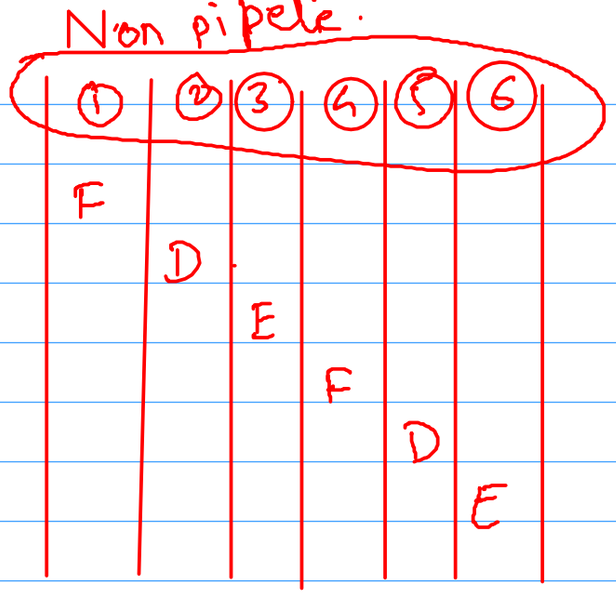
2 - Bit

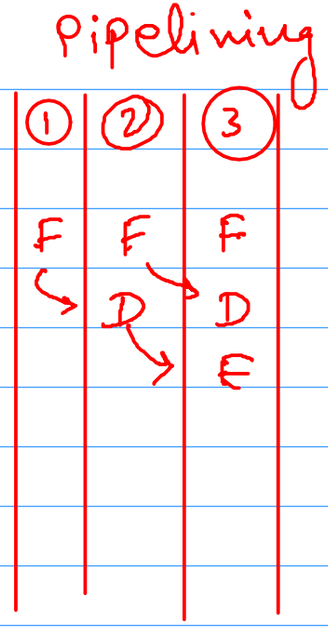
4 - Bit → nibble

8 - Bit → 1 byte

16 - Bit → 2 bytes → 1 word

32 - Bit → 4 bytes → 2 words





Q → 8 instructions
5 stage.

⇒ non-pipelining.
= K×N
= 8×5
= 40 cycle

⇒ pipelining
= K + (N-1)
= 5 + (8-1)
= 5+7 = 12 cycle.

Data bus → 8 bit → $2^8 = 256 =$ 11111111

D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7

lower dat bus — Higher data bus

Address bust

16 bit → $2^{16} = 65536 = 64$ KB

A_0 A_1 ----- A_7 A_8 A_9 ------ A_{15}

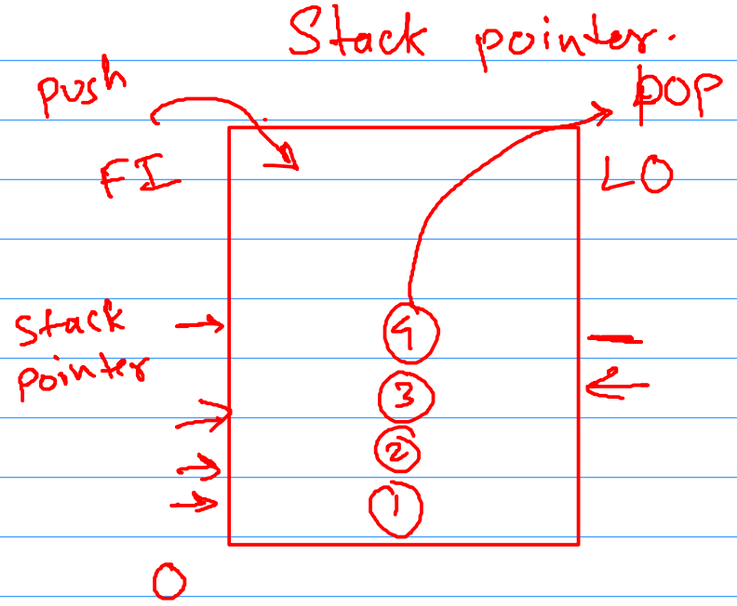
lower order — Higher order.

Small Endian

lower - high

Big Endian

high - lower


Stack pointer.
push
pop
FI
LO
stack pointer
4
3
2
1
0