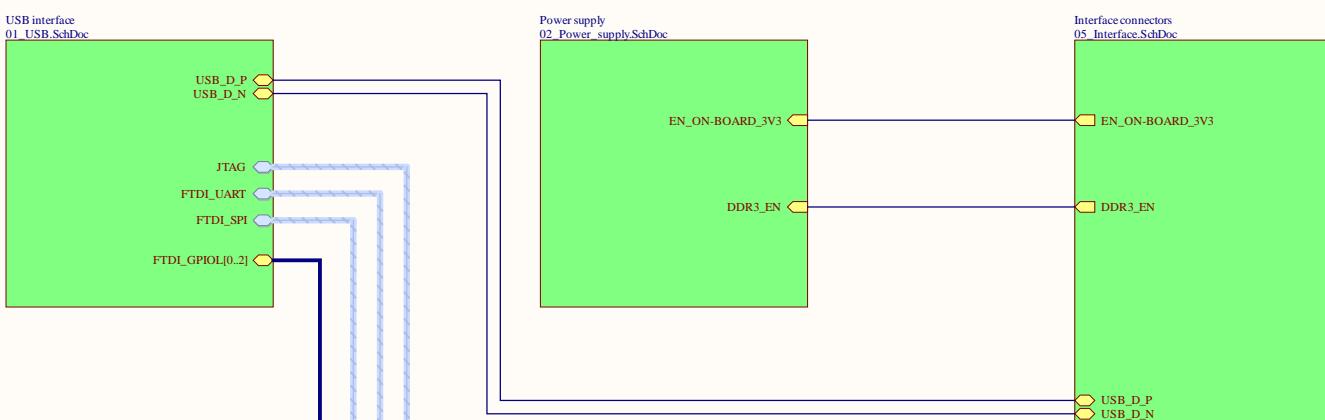
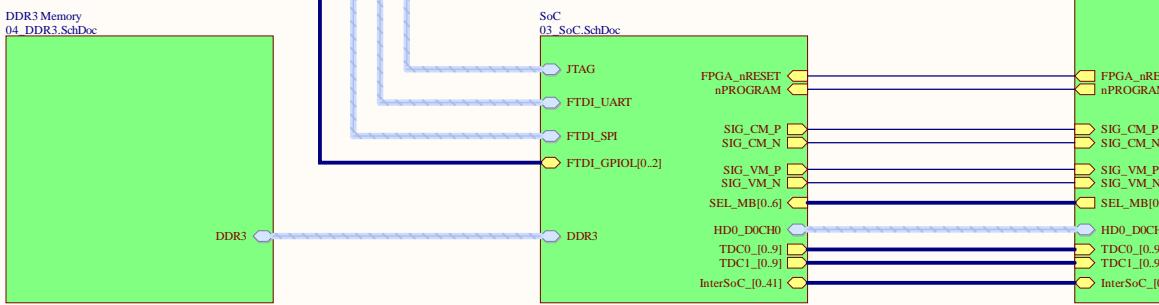


A



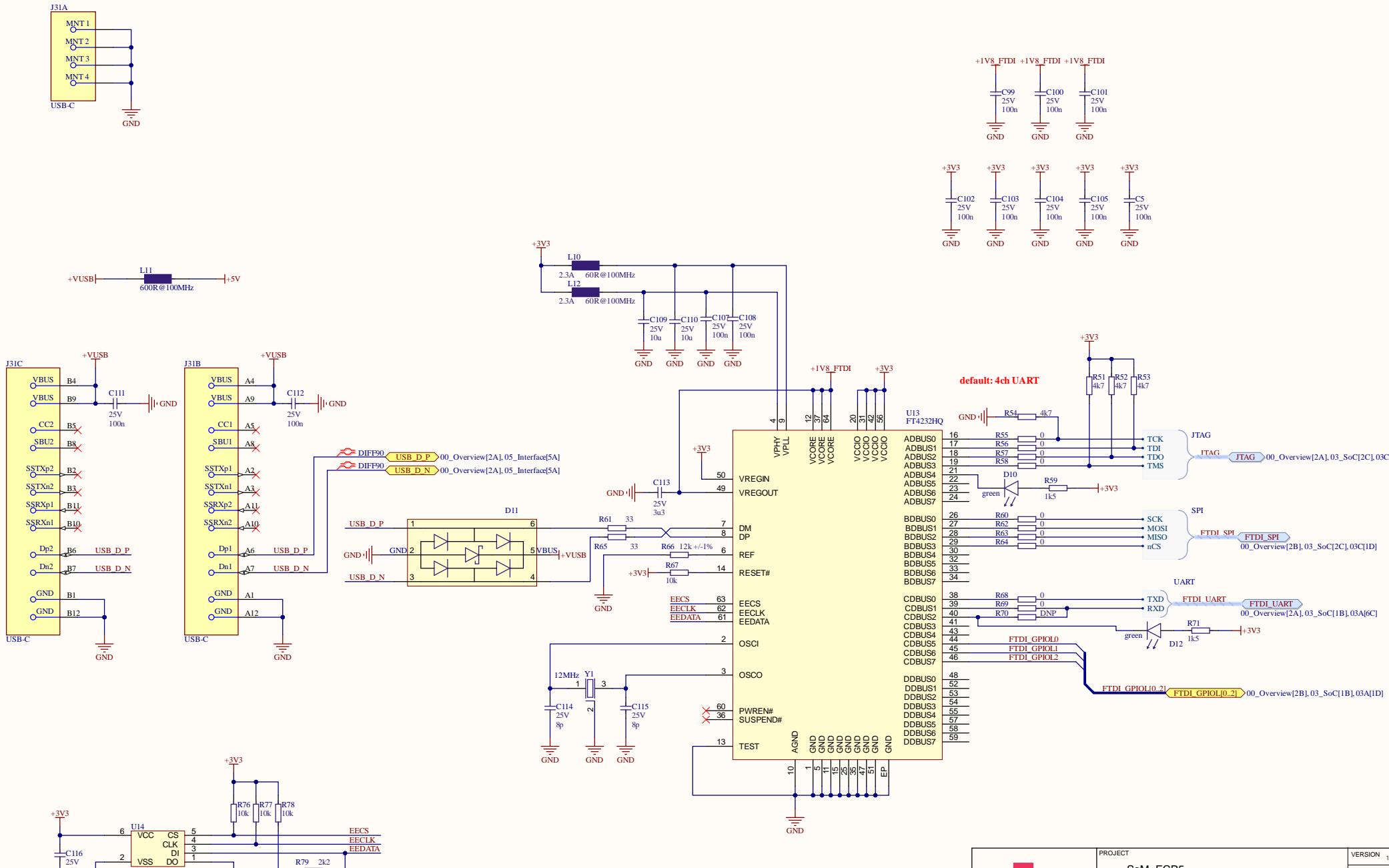
B



C

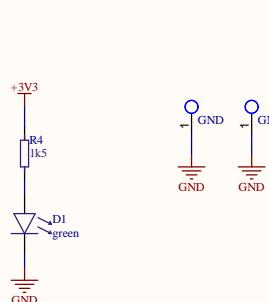
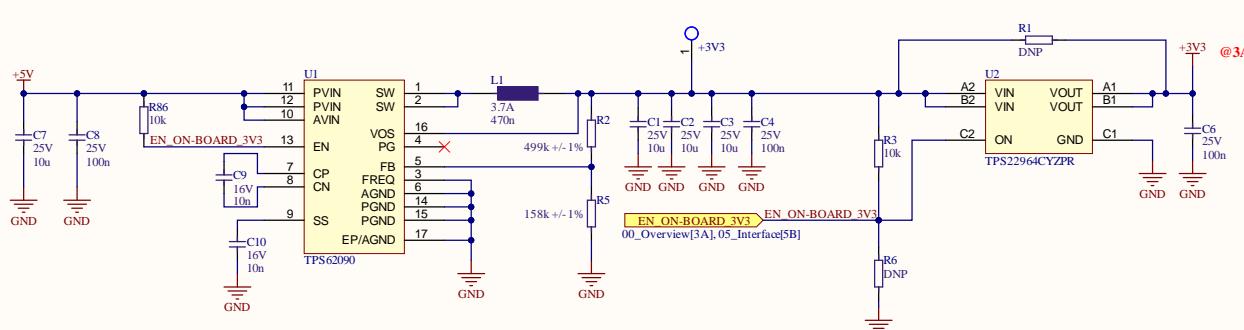
D

	PROJECT SoM_ECP5	VERSION 1.0
		DATE 15/04/2024
TITLE 00_Overview.SchDoc		
REFERENCE DOCUMENTS	Graz University of Technology Institute of Technical Informatics Infeldgasse 16/IV 8010 Graz, Austria	WORKING GROUP Embedded Architectures & Systems (EAS)
BOM:		SIZE A3
ASSY DWG:		
FAB DWG:		
PCB DWG:	URL https://www.tugraz.at/eas	DRAWN BY K. Kainic
FILE NAME	00_Overview.SchDoc	SHEET 1 OF 10

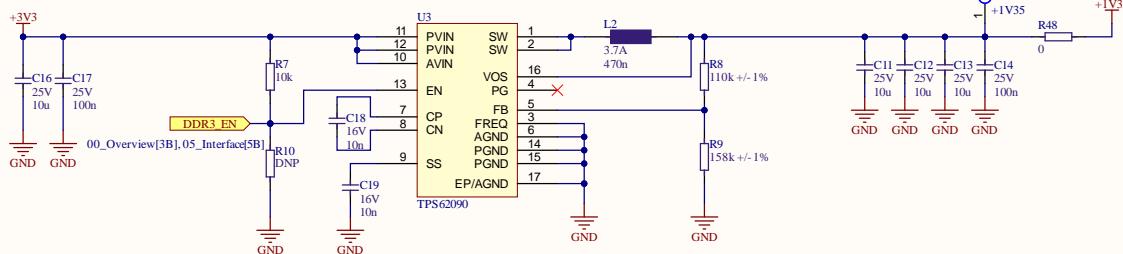


PROJECT		VERSION 1.0
SoM_ECP5		DATE 18/04/2024
TITLE 01_USB.SchDoc		
REFERENCE DOCUMENTS		
Graz University of Technology Institute of Technical Informatics Infeldgasse 16/3 8010 Graz, Austria		
ASSY DWG:	WORKING GROUP Embedded Architectures & Systems (EAS)	SIZE A3
FAB DWG:	URL https://www.tugraz.at/eas	DRAWN BY K. Kanics
PCB DWG:	FILE NAME 01_USB.SchDoc	SHEET 2 OF 10

A

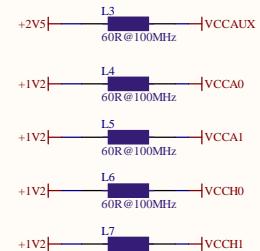
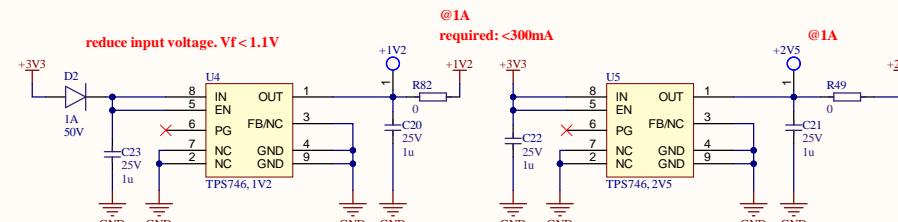


B



* populate only if LDO is too weak to power the FPGA
 * remove R82
 * change R8 and R9 accordingly! SMPS output must be 1V2

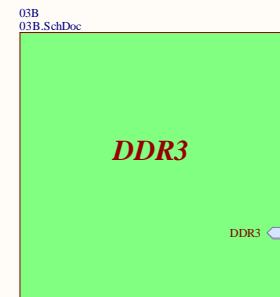
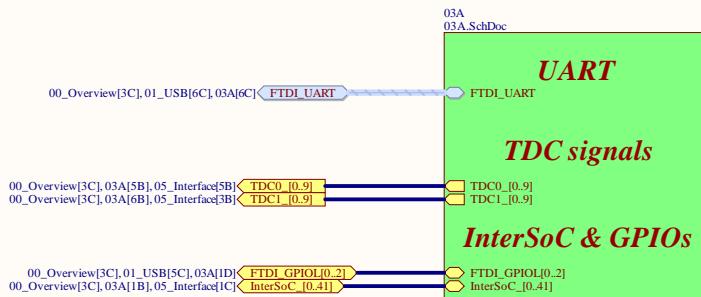
C



D

PROJECT		VERSION 1.0
SoM_ECP5		DATE 18/04/2024
REFERENCE DOCUMENTS		
BOM:	Graz University of Technology	SIZE A3
ASSY DWG:	Institute of Technical Informatics	
FAB DWG:	Infeldgasse 16/18 8010 Graz Austria	
PCB DWG:	URL https://www.tugraz.at/soem/	DRAWN BY K. Kanics
	FILE NAME 02_Power_supply.SchDoc	SHEET 3 OF 10

A

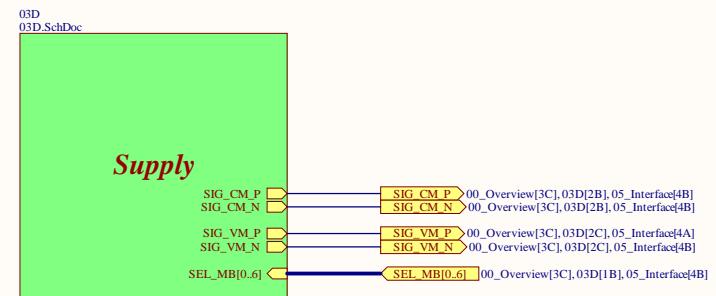
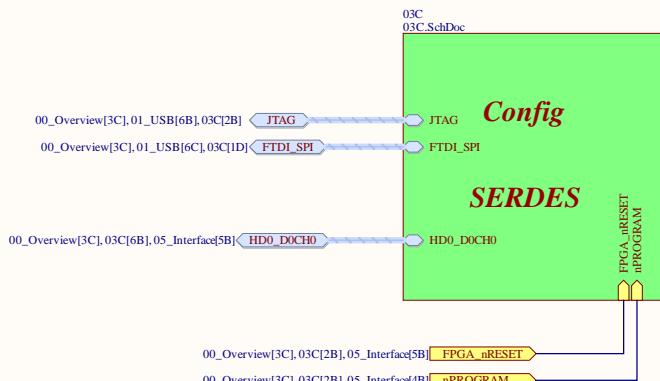


High-speed/LVDS capable banks on the left (Bank 6 & 7) and right (Bank 2 & 3)

A/B: diff. input/output
C/D: diff. input

A

B



SEL_MB[0..6]: !C_EN / C_Ch / V_EN / V_Ch

- I xxx 0 xx - VM, CM off
- x xxx 1 00 - VMB1 active
- x xxx 1 01 - VMB2 active
- x xxx 1 10 - VMB3 active
- x xxx 1 11 - VMB4 active
- 0 00x x xx - CMB1 active
- 0 0Ix x xx - CMB2 active
- 0 1x0 x xx - CMB3 active
- 0 1x1 x xx - CMB4 active

VM and CM channels can be combined

B

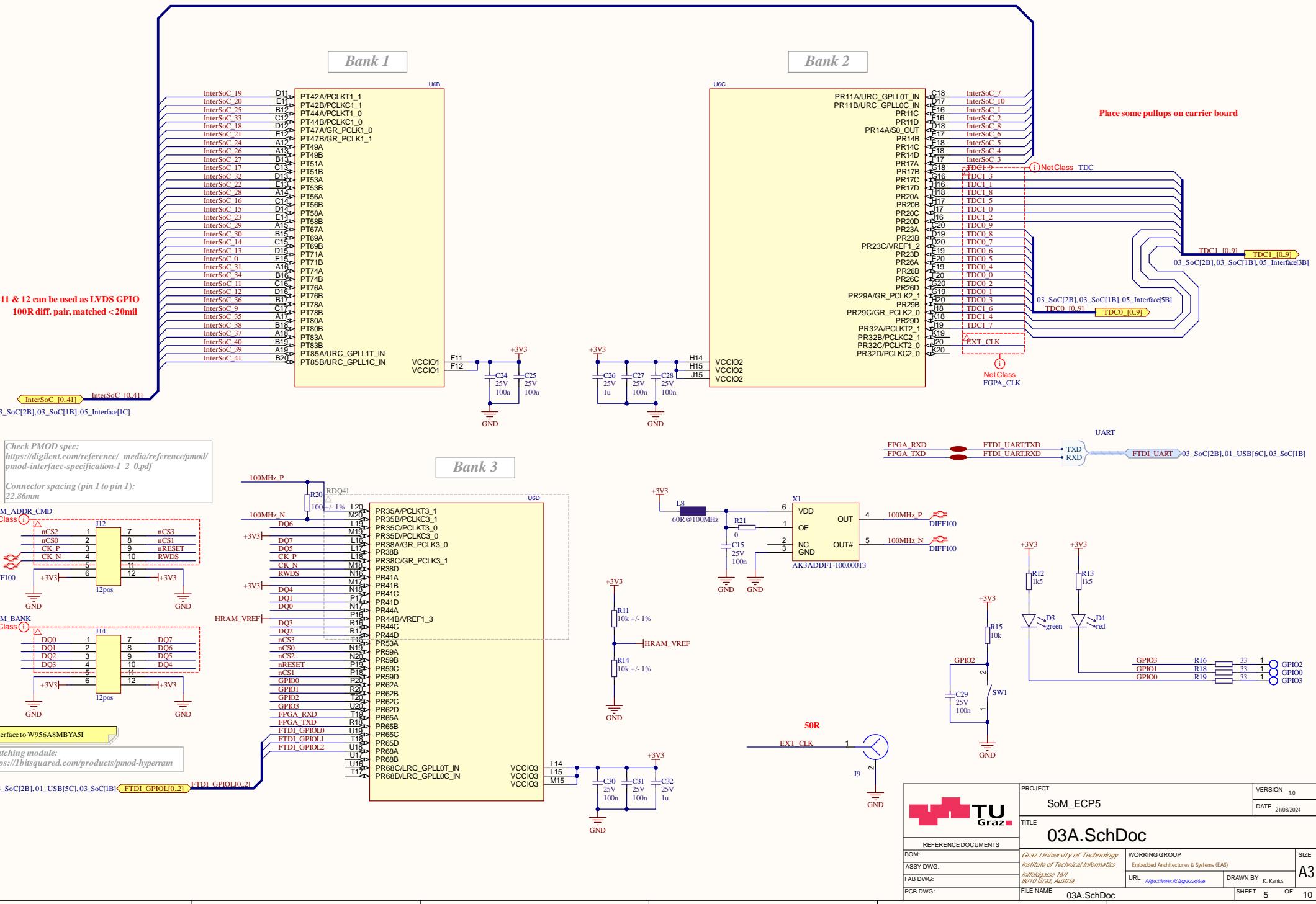
C

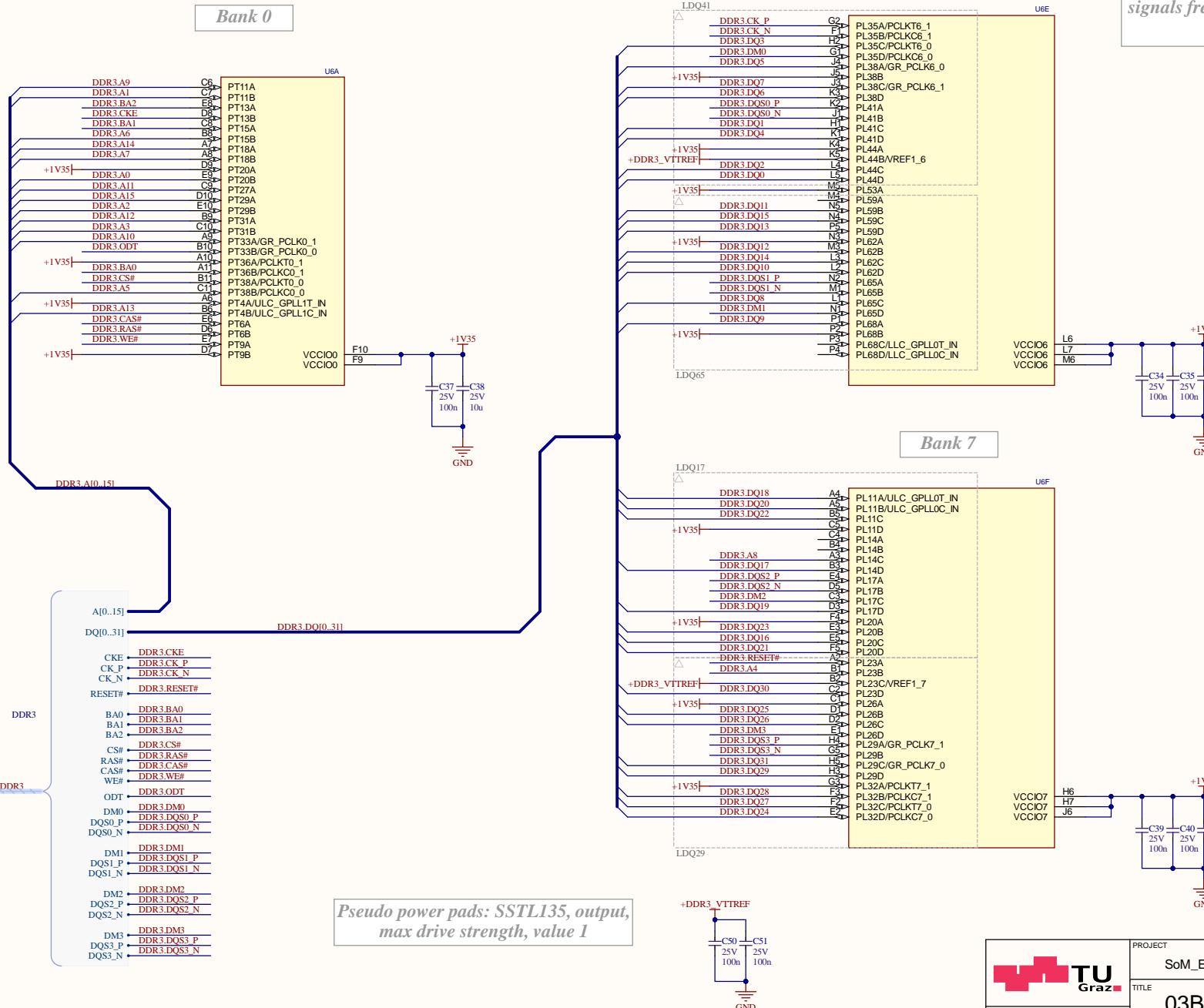
C

D

D

	PROJECT SoM_ECP5	VERSION 1.0
		DATE 19/04/2024
REFERENCE DOCUMENTS	WORKING GROUP	SIZE
BOIM:	Graz University of Technology Institute of Technical Informatics Infeldgasse 16/18 8010 Graz Austria	A3
ASSY DWG:		
FAB DWG:		
PCB DWG:	URL https://www.tugraz.at/eas	DRAWN BY K. Kanics
FILE NAME	03_SoC.SchDoc	SHEET 4 OF 10



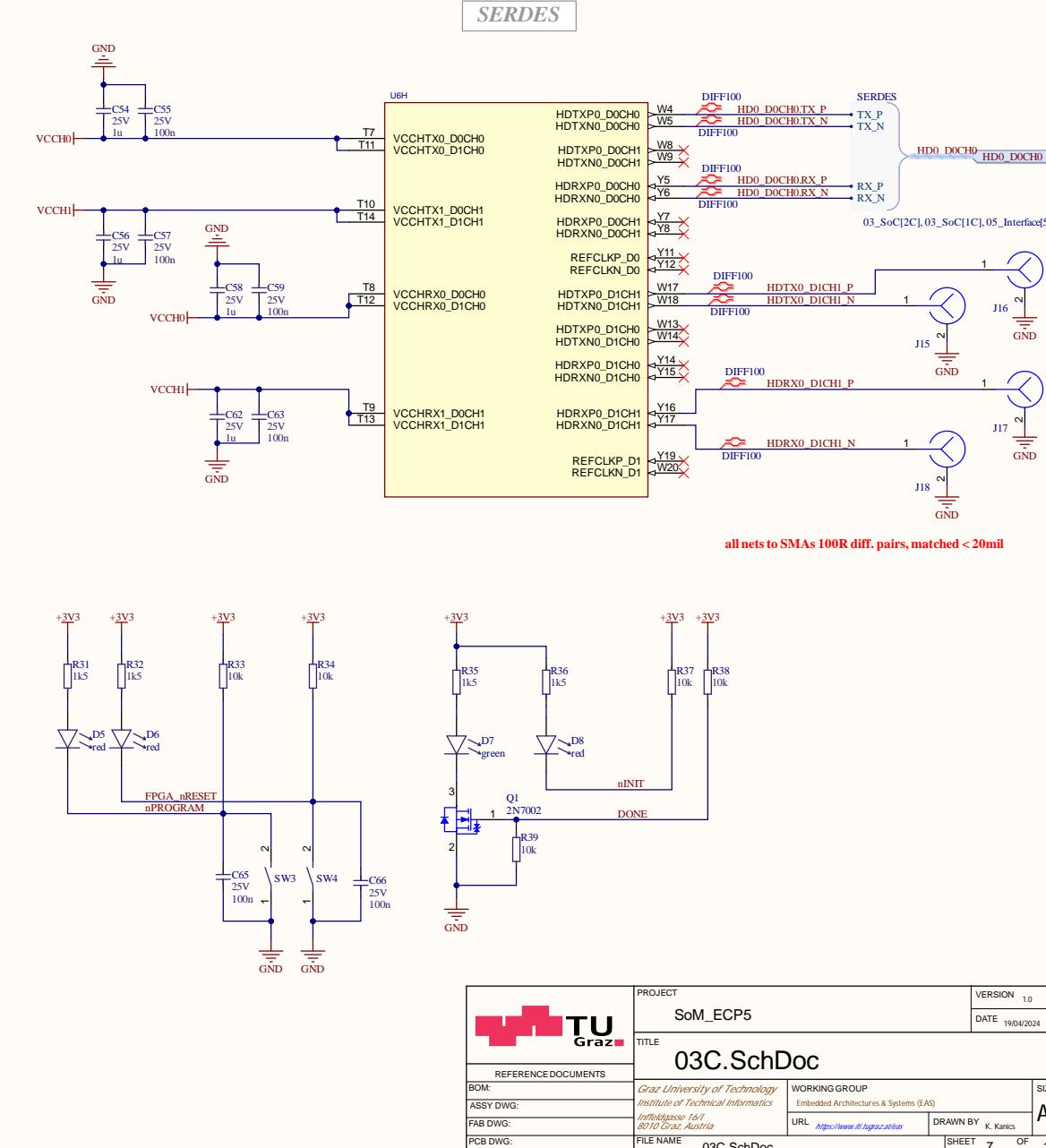
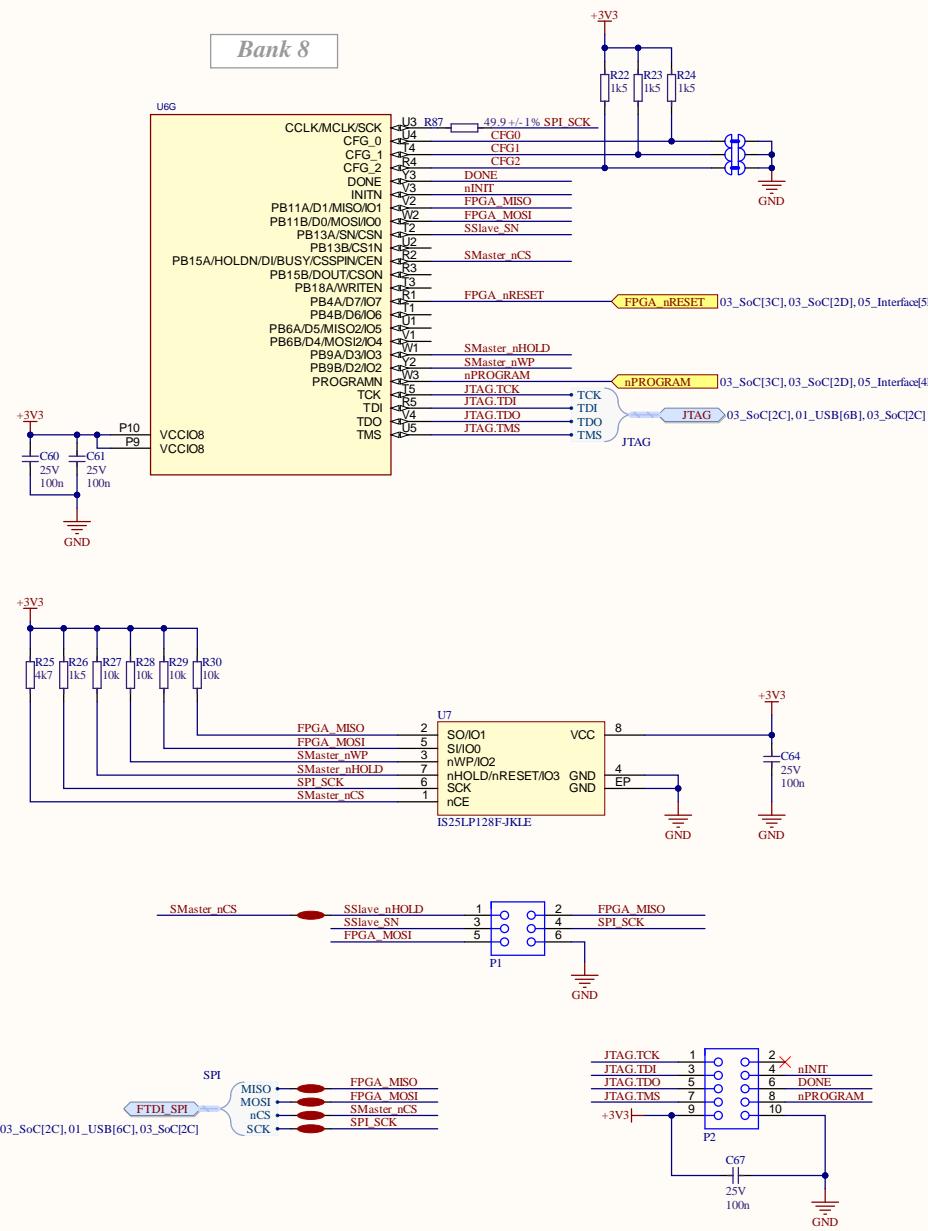
DDR3

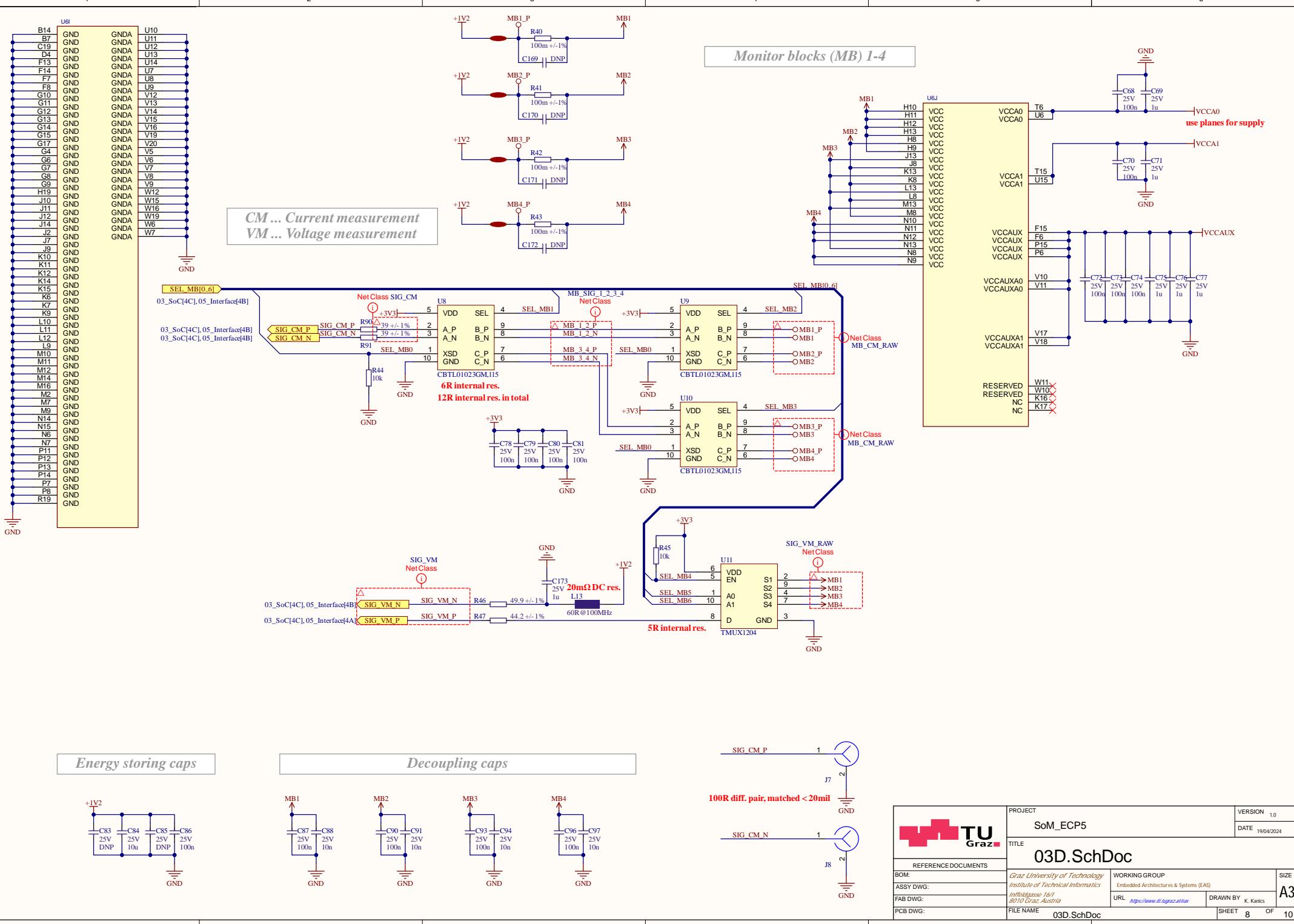
DQS, DQS# signals are fixed, all others signals free to choose as long as they are in the correct group

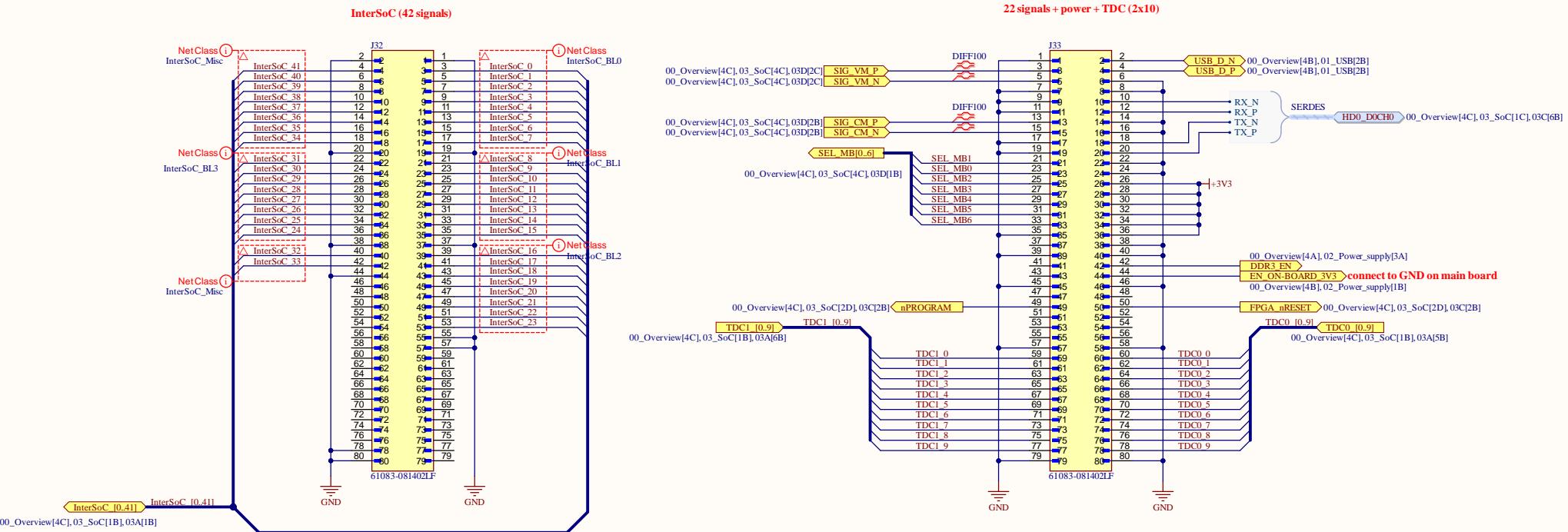
PROJECT		VERSION 1.0
SoM_ECP5		DATE 17/04/2024
REFERENCE DOCUMENTS		
BOM:	Graz University of Technology Institute of Technical Informatics	SIZE A3
ASSY DWG:	Infeldgasse 16/ 8010 Graz, Austria	
FAB DWG:	URL https://www.tugraz.at/eas	DRAWN BY K. Kanics
PCB DWG:	FILE NAME 03B.SchDoc	SHEET 6 OF 10

Config modes CFG[2:0]:

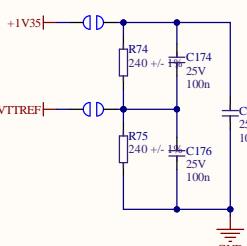
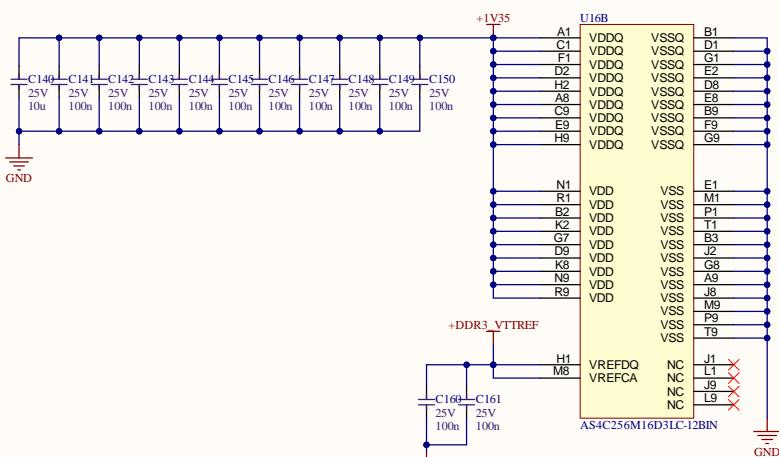
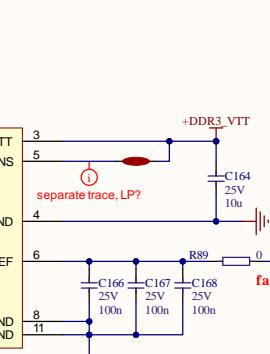
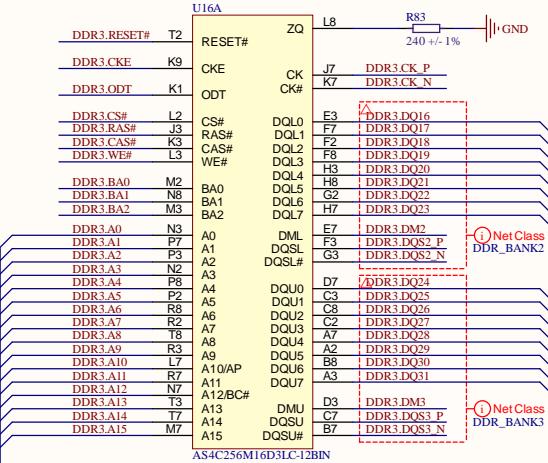
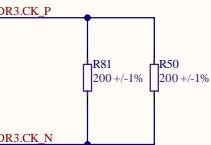
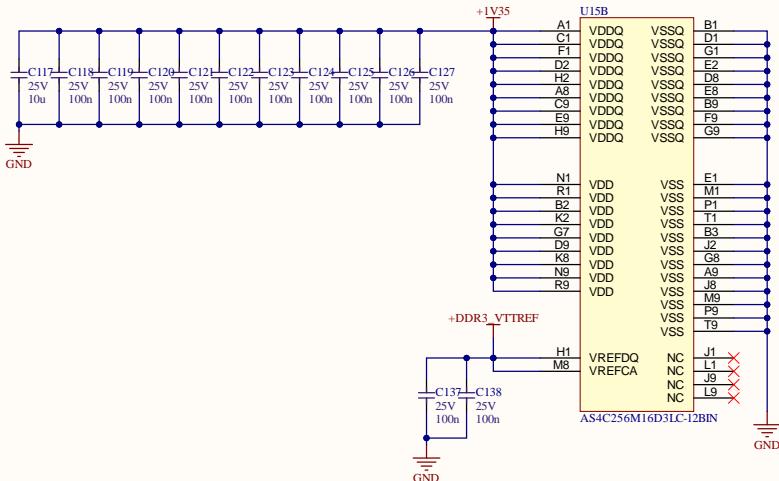
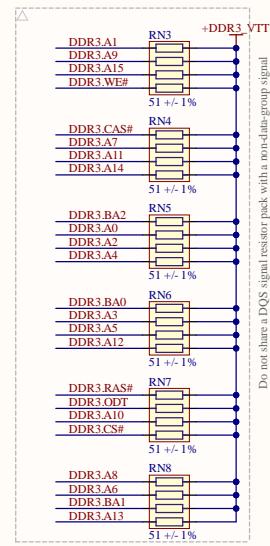
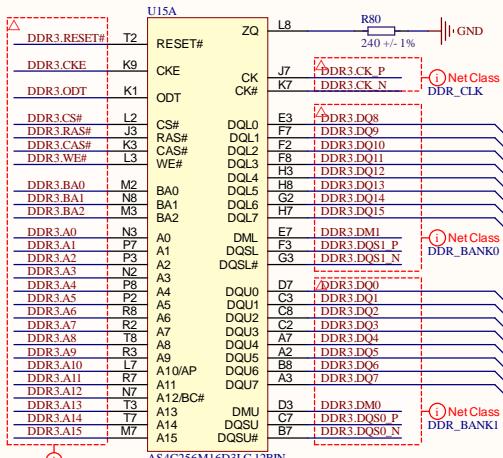
JTAG mode: Flash SPI memory via JTAG, Master SPI config needed
[010]: *Master SPI: FPGA reads flash config at startup from ext. memory*
[001]: *Slave SPI: FPGA is flashed via external SPI master - supported only via programming connector*
 [101] Slave serial- not supported
 [111] Slave parallel - not supported







AS4C256M16D3LC-12BIN
pincompatible with
IS43TR16xxxBL,
AS4C512M16D3LC,
AS4C256M16D3LC



far away from VTT_islands on different layers when possible



PROJECT		VERSION 1.0
SoM_ECP5		DATE 19/04/2024
REFERENCE DOCUMENTS		
BOM:	Graz University of Technology	SIZE
ASSY DWG:	Institute of Technical Informatics	
FAB DWG:	Infeldgasse 16/3	
PCB DWG:	8010 Graz, Austria	
FILE NAME	04_DDR3.SchDoc	DRAWN BY K. Kanics
SHEET 10 OF 10		A3

DDR3	CKE	DDR3.CKE	DIFF100
	CK_P	DDR3.CK_P	DIFF100
	CK_N	DDR3.CK_N	DIFF100
	RESET#	DDR3.RESET#	
	BA0	DDR3.BA0	
	BA1	DDR3.BA1	
	BA2	DDR3.BA2	
	CS#	DDR3.CS#	
	RAS#	DDR3.RAS#	
	CAS#	DDR3.CAS#	
	WE#	DDR3.WE#	
	ODT	DDR3.ODT	
	DM0	DDR3.DM0	
	DQ0_P	DDR3.DQ0_P	DIFF100
	DQ0_N	DDR3.DQ0_N	DIFF100
	DM1	DDR3.DM1	
	DQ1_P	DDR3.DQ1_P	DIFF100
	DQ1_N	DDR3.DQ1_N	DIFF100
	DM2	DDR3.DM2	
	DQ2_P	DDR3.DQ2_P	DIFF100
	DQ2_N	DDR3.DQ2_N	DIFF100
	DM3	DDR3.DM3	
	DQ3_P	DDR3.DQ3_P	DIFF100
	DQ3_N	DDR3.DQ3_N	DIFF100