

# EE\_HW2

● Graded

**Student**

苏慧哲

**Total Points**

100 / 100 pts

## Question 1

(no title)	30 / 30 pts
1.1 (no title)	10 / 10 pts
<input checked="" type="checkbox"/> - 0 pts Correct	
<ul style="list-style-type: none"><li>- 3 pts no logic circuit design</li><li>- 3 pts no Truth table</li><li>- 2 pts truth table wrong</li><li>- 2 pts The logic circuit needs to be drawn</li><li>- 2 pts truth table wrong</li><li>- 2 pts logic circuit wrong</li><li>- 1 pt better to draw the logic circuit</li><li>- 2 pts use xor to build xor circuit</li><li>- 2 pts logic circuit is incomplete</li><li>- 3 pts Connection error in PMOS substrates</li></ul>	
1.2 (no title)	15 / 15 pts
<input checked="" type="checkbox"/> - 0 pts Correct	
<ul style="list-style-type: none"><li>- 15 pts no CMOS-level implementation</li><li>- 5 pts It is not a xor logic circuit</li><li>- 3 pts Lack of elements such as input voltage &amp; supply voltage</li><li>- 12 pts wrong circuit</li><li>- 8 pts wrong circuit</li><li>- 10 pts not a CMOS-level implementation</li><li>- 3 pts Some pins are not properly connected</li></ul>	

1.3 L (no title)

Resolved 5 / 5 pts

✓ - 0 pts Correct

- 2 pts Not a good measurement result
- 2 pts No CMOS-level measurement result
- 2 pts It is not a xor logic circuit
- 5 pts no measurement result
- 5 pts wrong
- 2 pts wrong

C Regrade Request

Submitted on: Dec 03

我把两个的measurement放一起了，最后那三张是CMOS-level的测试。 (CMOS-level的是没有毛刺的那几张)

已更正，measurement中的图线分开，这样看不清楚结果

Reviewed on: Dec 03

## Question 2

(no title)	30 / 30 pts
2.1 (no title)	10 / 10 pts
<div style="border: 1px solid #ccc; padding: 5px;"><p>✓ - 0 pts correct</p></div>	
<ul style="list-style-type: none"><li>- 2 pts e not SOP</li><li>- 10 pts <math>A'B' \neq (AB)'</math></li><li>- 8 pts Click here to replace this description.</li><li>- 8 pts <math>A'B' \neq (AB)'</math></li></ul>	
2.2 (no title)	10 / 10 pts
<div style="border: 1px solid #ccc; padding: 5px;"><p>✓ - 0 pts Correct</p></div>	
<ul style="list-style-type: none"><li>- 8 pts <math>A'B' \neq (AB)'</math></li><li>- 10 pts no result</li><li>- 5 pts Kmap wrong</li><li>- 6 pts no result</li><li>- 8 pts no result</li><li>- 4 pts no simplified result</li></ul>	
2.3 (no title)	10 / 10 pts
<div style="border: 1px solid #ccc; padding: 5px;"><p>✓ - 0 pts Correct</p></div>	
<ul style="list-style-type: none"><li>- 2 pts (e) wrong</li><li>- 5 pts test wrong</li><li>- 5 pts no circuit</li><li>- 1 pt (e) test wrong</li><li>- 1 pt (d) test wrong</li><li>- 1 pt (e) no test</li><li>- 1 pt (d) no circuit</li><li>- 6 pts not complete</li><li>- 4 pts circuit not complete</li><li>- 2 pts test not good</li><li>- 4 pts Input pattern uncovered</li></ul>	

### Question 3

(no title) 20 / 20 pts

3.1 (no title) 15 / 15 pts

- 0 pts Correct

- 8 pts Procedure Missing

- 3 pts Procedure not Clear. Truth-table, K-map or final equation missing.

- 7 pts No Circuit

- 3 pts Final Circuit Missing

- 5 pts Two Displays

- 15 pts No Submission

- 9 pts Principle Error

- 5 pts No Display

3.2 (no title) 5 / 5 pts

- 0 pts Correct

- 5 pts Simulation Result Missing

- 2 pts Result ambiguous

#### Question 4

(no title)

20 / 20 pts

4.1 (no title)

10 / 10 pts

✓ - 0 pts Correct

- 3 pts The condition when S=R=1 is incorrect.

- 3 pts Circuit is missing.

- 5 pts Q is incorrect

- 3 pts Q is incorrect in the second half

- 4 pts Tool dependent

- 2 pts Input pattern incorrect

- 1 pt At S=R=1, the output is strong 0.

- 1 pt Q' is incorrect when S=R=1

- 10 pts No submission

- 3 pts The order of Q and Q' is wrong

💬 + 3 pts Extra pts for simulation

4.2 (no title)

10 / 10 pts

✓ - 0 pts Correct

- 10 pts wrong

Questions assigned to the following page: [1.1](#) and [1.2](#)

## Problem Set #2, EE part

Issue date: Nov. 14, 2020; Deadline: 23:59, Nov. 22, 2020

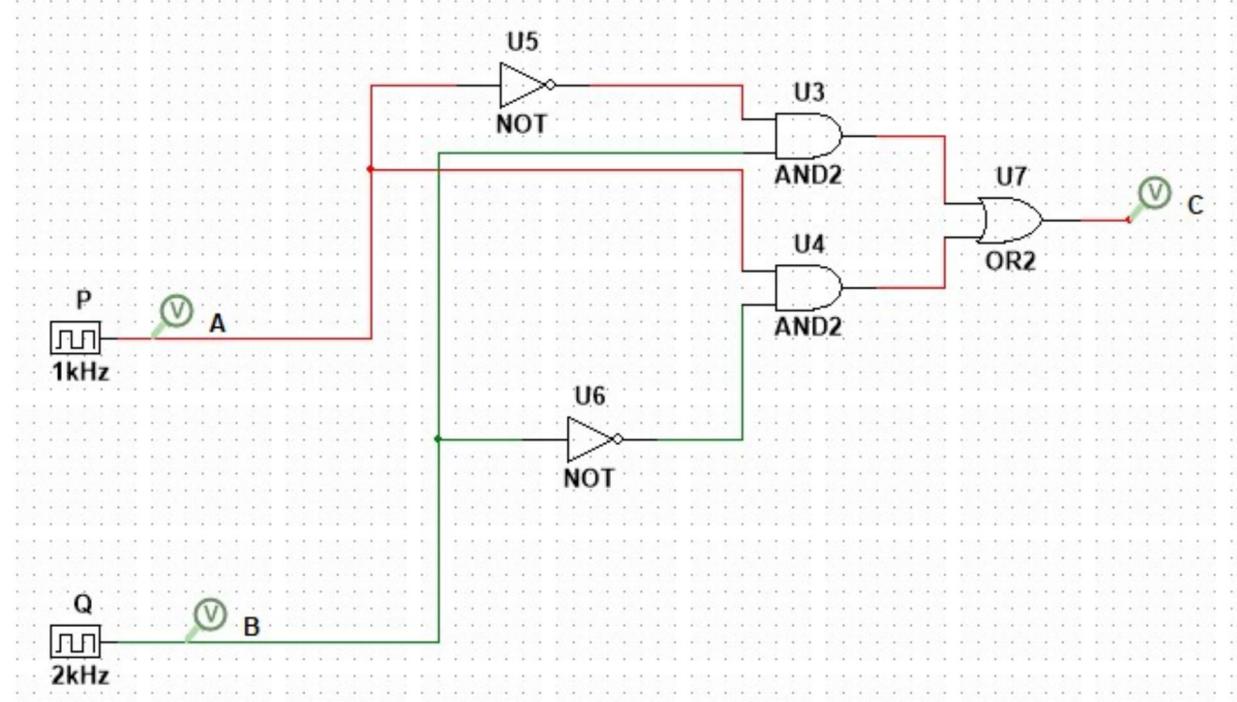
Student Name: \_\_\_\_\_ 苏慧哲 \_\_\_\_\_ Student No.: \_\_\_\_\_ 2020533009 \_\_\_\_\_

### 1. CMOS logic gate

Use the fundamental CMOS logic circuit units, such as NOT, AND, OR, to build a XOR gate –

Truth table and logic circuit (gate level) design. (10')

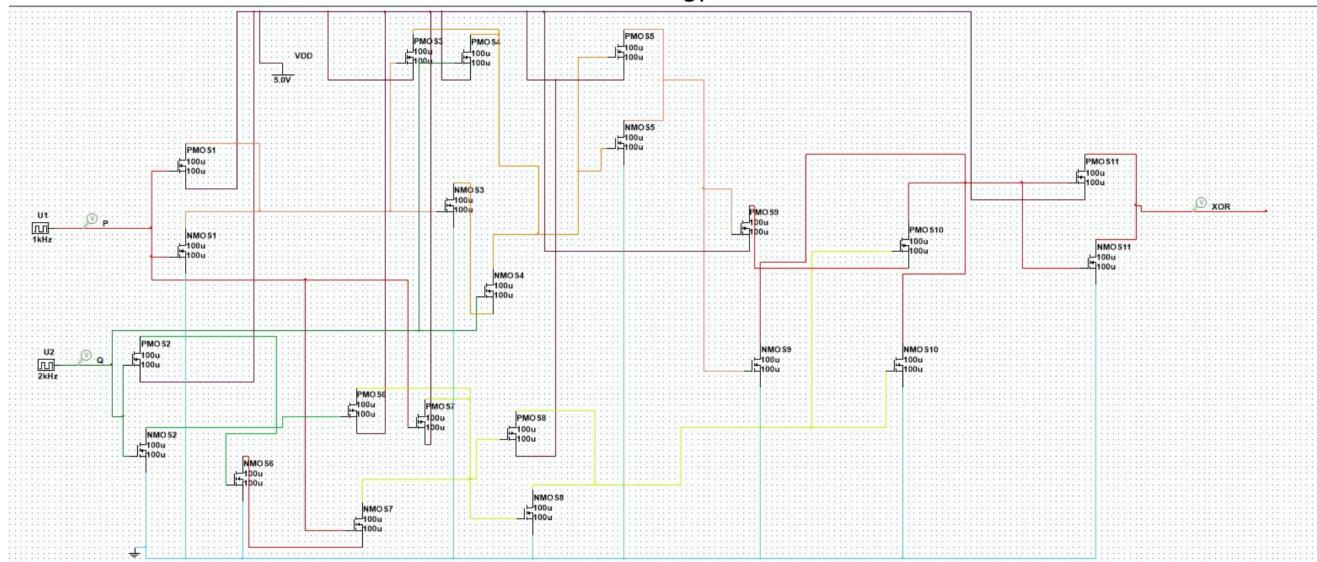
P	Q	P XOR Q
0	0	0
0	1	1
1	0	1
1	1	0



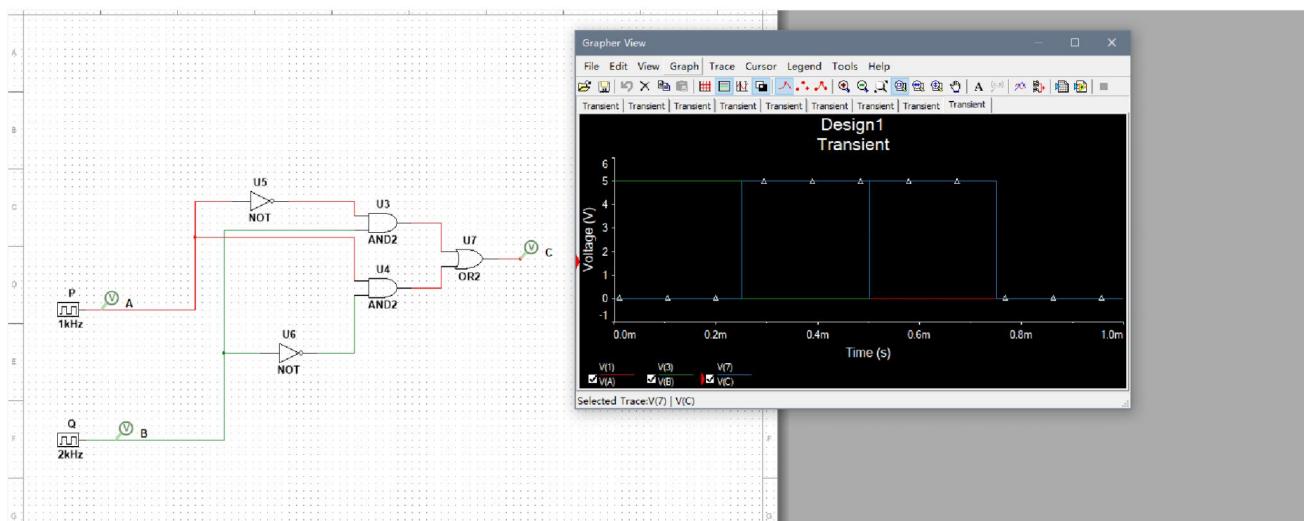
- CMOS-level implementation (15')



Questions assigned to the following page: [1.2](#) and [1.3](#)



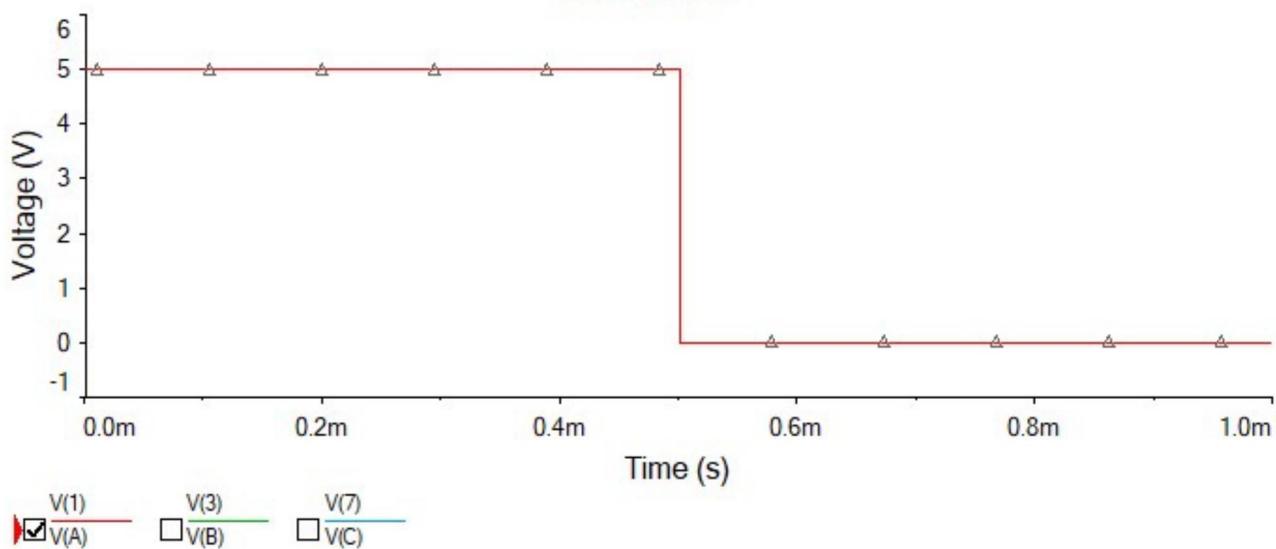
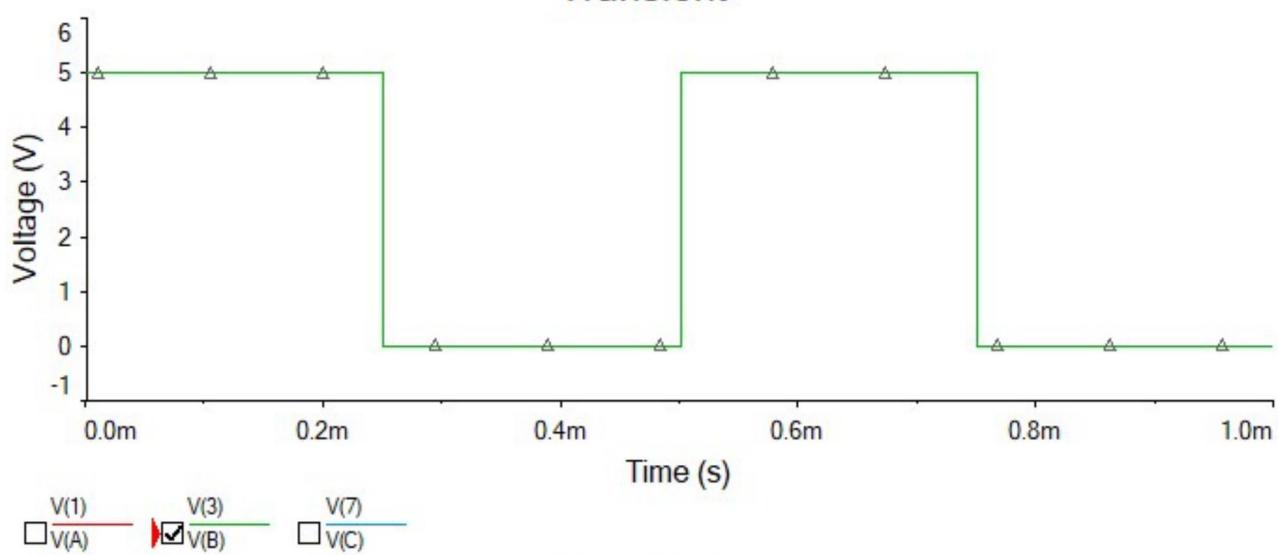
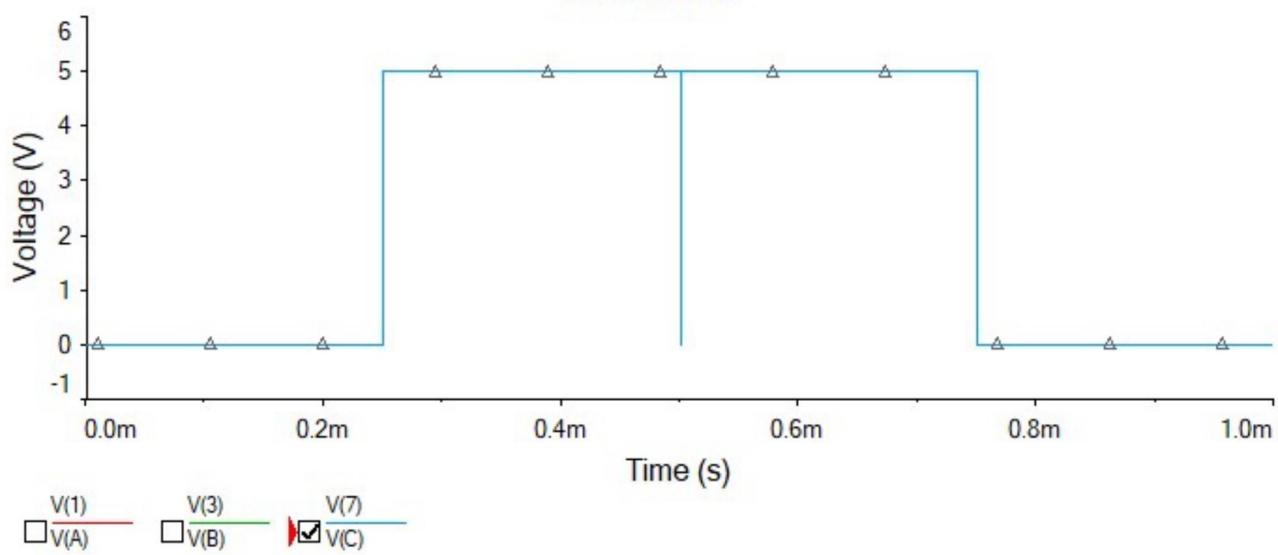
- #### - Measurement results (5')



First circuit:



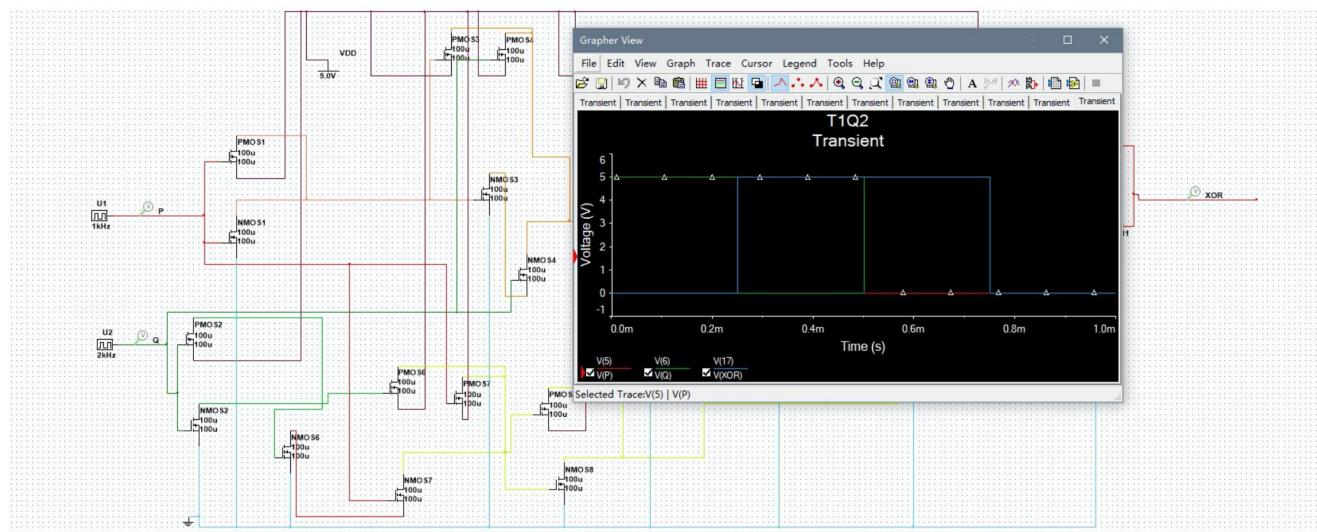
Question assigned to the following page: [1.3](#)

**Transient****Transient****Transient**



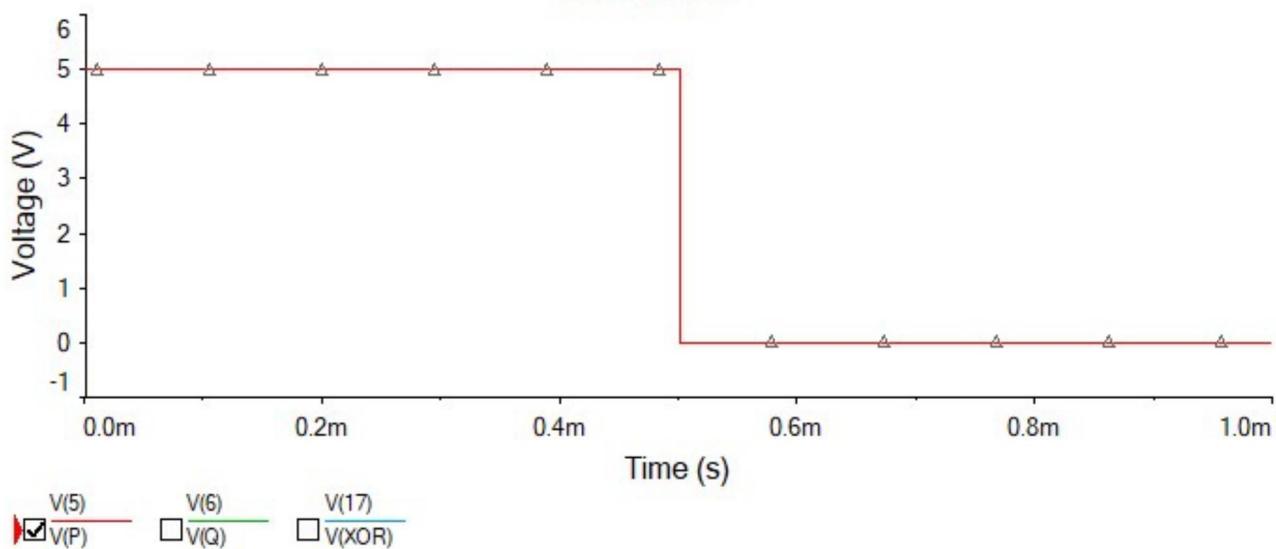
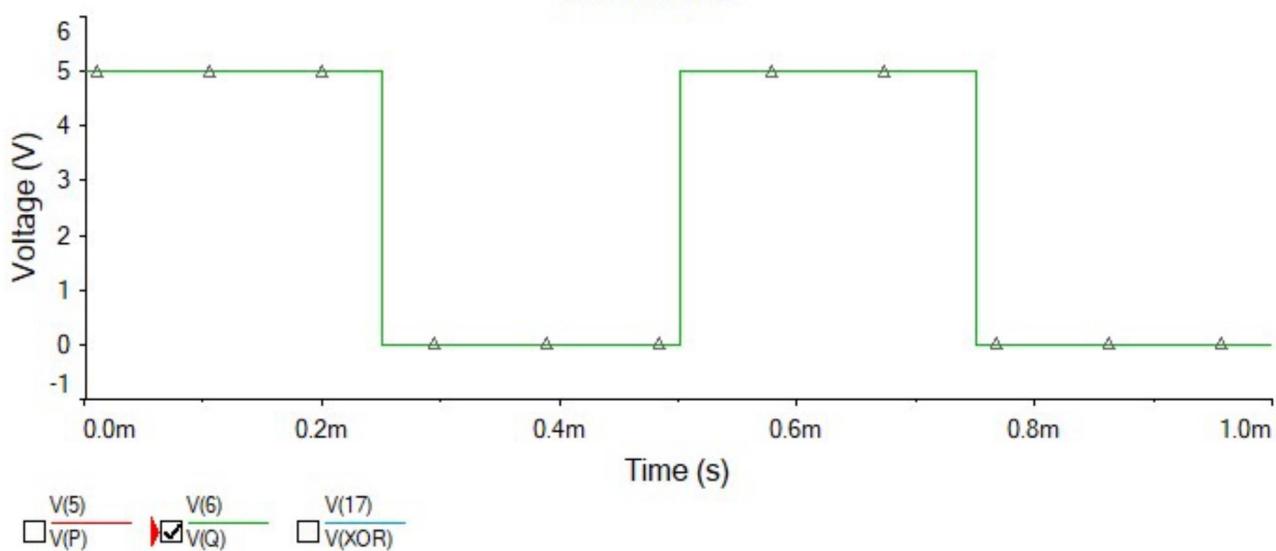
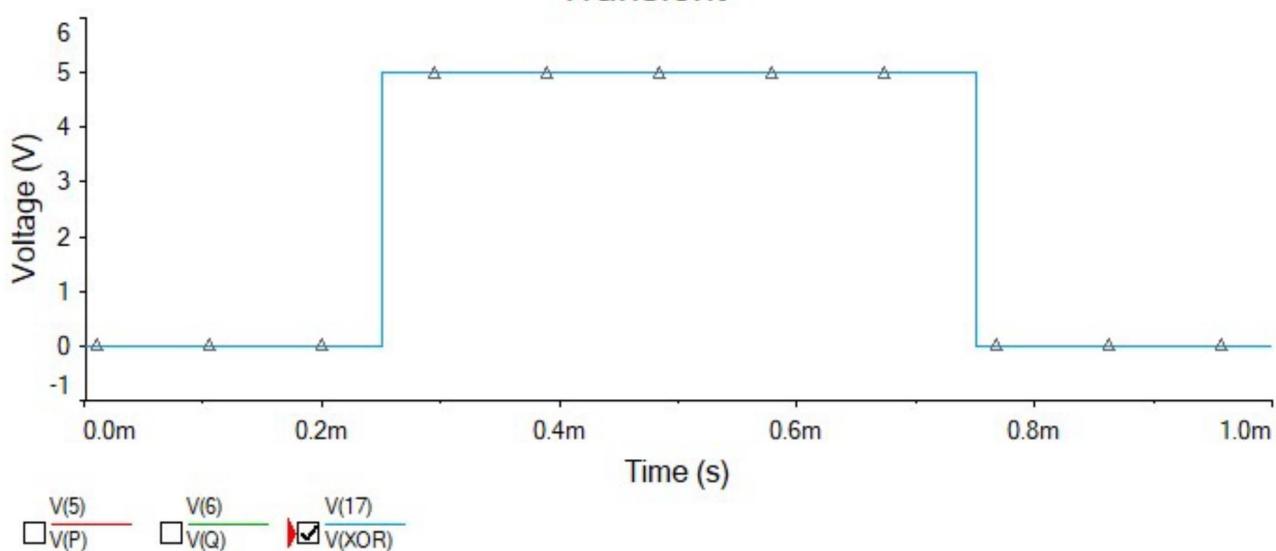
Question assigned to the following page: [1.3](#)

Second circuit:





Question assigned to the following page: [1.3](#)

**Transient****Transient****Transient**



Questions assigned to the following page: [2.1](#) and [2.2](#)

## 2. Combinational logic circuit exercises

- Write the Boolean equations in sum-of-products canonical form for each of the truth tables (2' \* 5)

(a)

$$Y = \bar{A}\bar{B} + A\bar{B} + AB$$

(b)

$$Y = \bar{A}\bar{B}\bar{C} + ABC$$

(c)

$$\bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + A\bar{B}C + ABC$$

(d)

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \cancel{\bar{A}B\bar{C}D} + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$$

(e)

$$\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \cancel{\bar{A}B\bar{C}D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + ABCD$$

- Simplify the logic using the K-map (2' \* 5)



Questions assigned to the following page: [2.2](#) and [2.3](#)

(a)  $Y = A + \bar{B}$

	A	B	Y
0	0	0	0
1	1	0	1

(b)

	A	B	C	Y
0	0	0	0	0
1	0	0	0	1
2	1	0	0	1
3	1	0	1	1

$Y = \bar{A}\bar{B}\bar{C} + ABC$

(c)

	A	B	C	Y
0	0	0	0	0
1	0	0	1	1
2	1	0	0	0
3	1	0	1	1

$\bar{B}\bar{C}$  ~~AP~~ AC.

~~AC + \bar{B}\bar{C} + \bar{A}\bar{C}~~

(d)

	A	B	C	D	Y
00	0	0	0	0	0
01	0	0	0	1	0
10	1	0	0	0	1
11	1	0	1	0	1

$\bar{AB} + \bar{ABC} + AB$

$\bar{ACD}$

$\bar{ABD}$

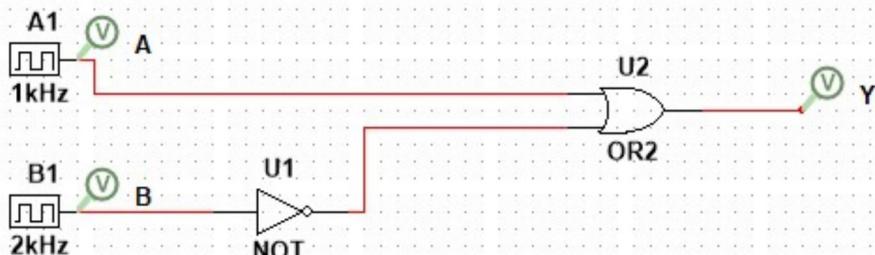
$Y = \bar{AB} + A\bar{C} + \bar{ABD}$

(e)

	A	B	C	D	Y
00	0	0	0	0	0
01	0	0	0	1	0
10	1	0	0	0	1
11	1	0	1	0	1

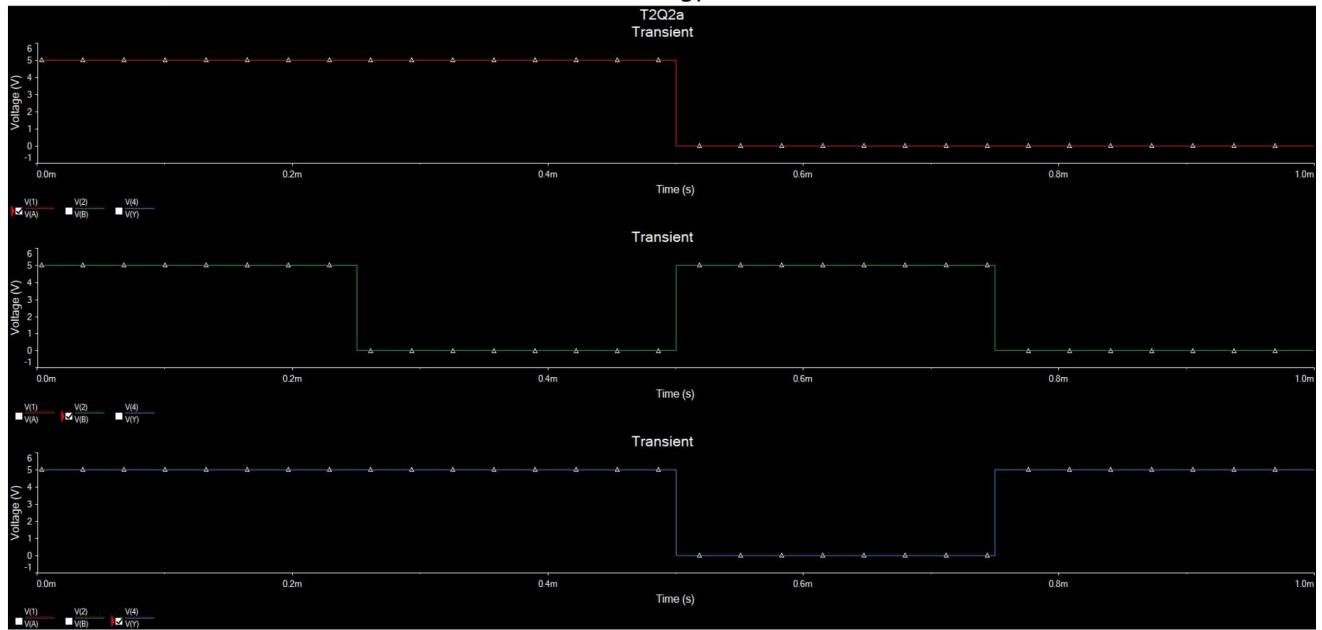
$Y = \bar{AB}\bar{CD} + \bar{ABC}D + \bar{ABC}\bar{D} + AB\bar{C}\bar{D} + ABCD + A\bar{B}\bar{C}D + A\bar{B}C\bar{D}$

- Implement the circuits in Multisim and test their performance (2' \* 5) (a)

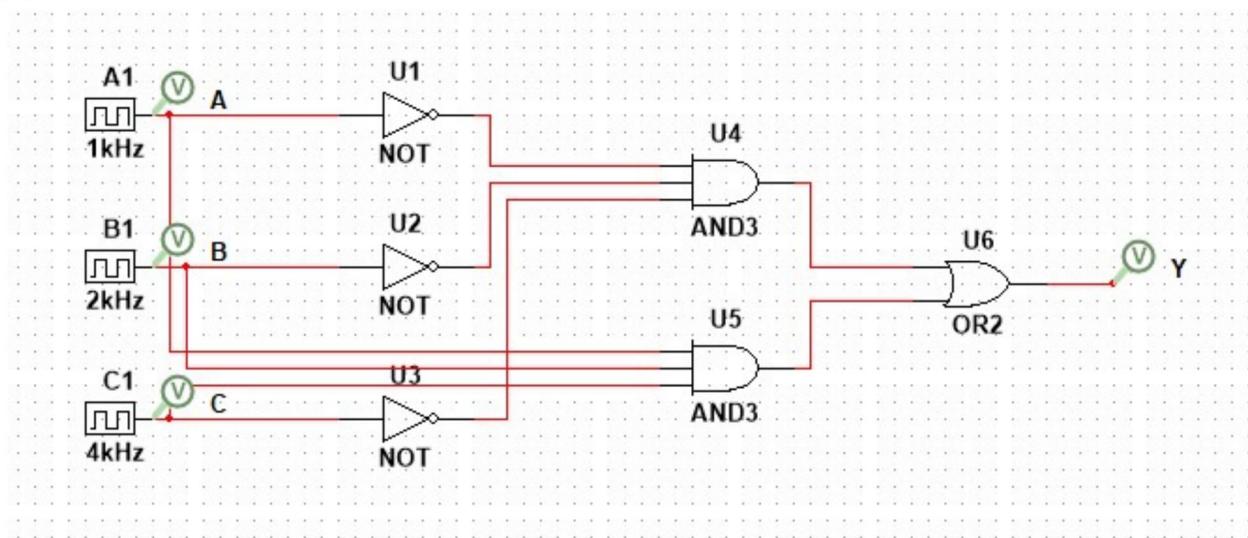




Question assigned to the following page: [2.3](#)

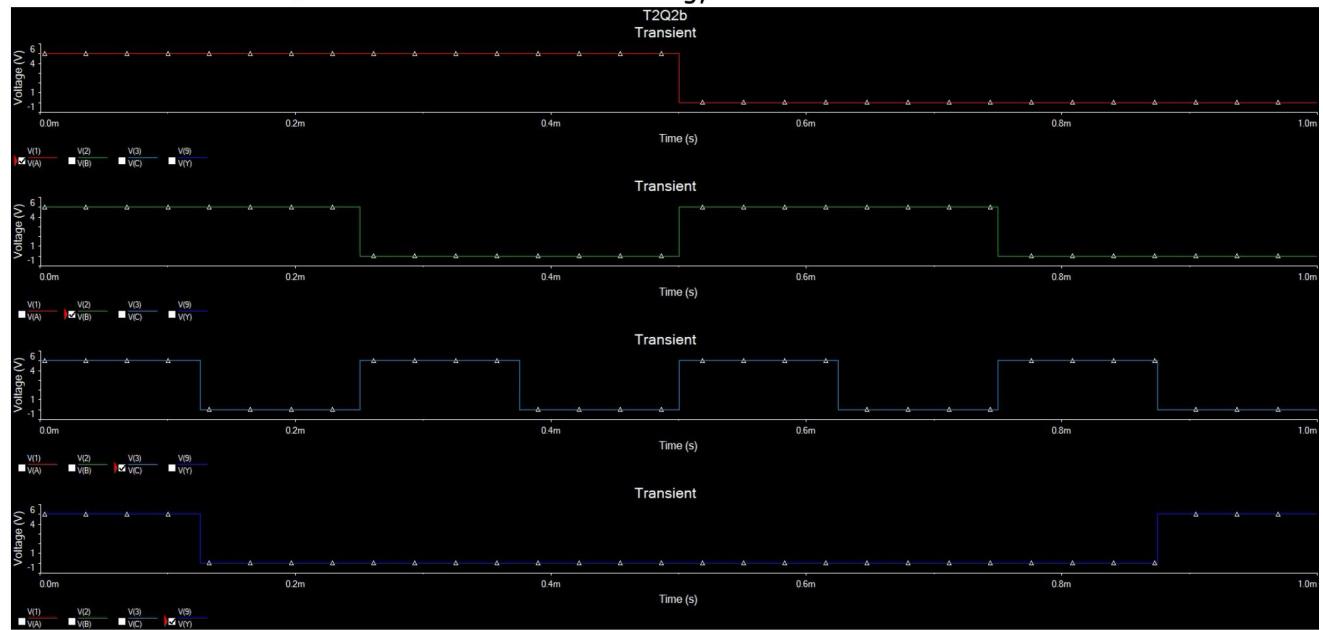


(b)

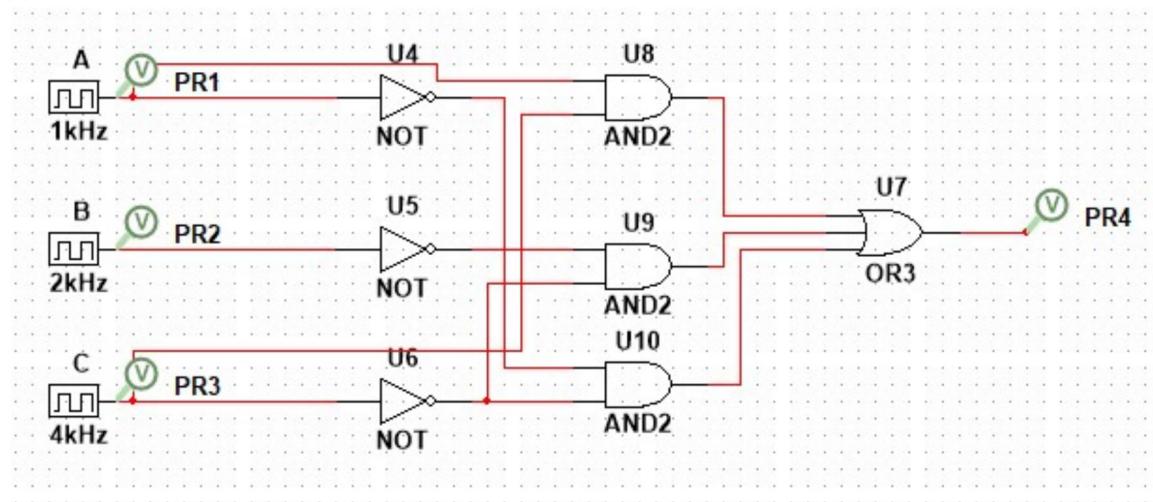




Question assigned to the following page: [2.3](#)

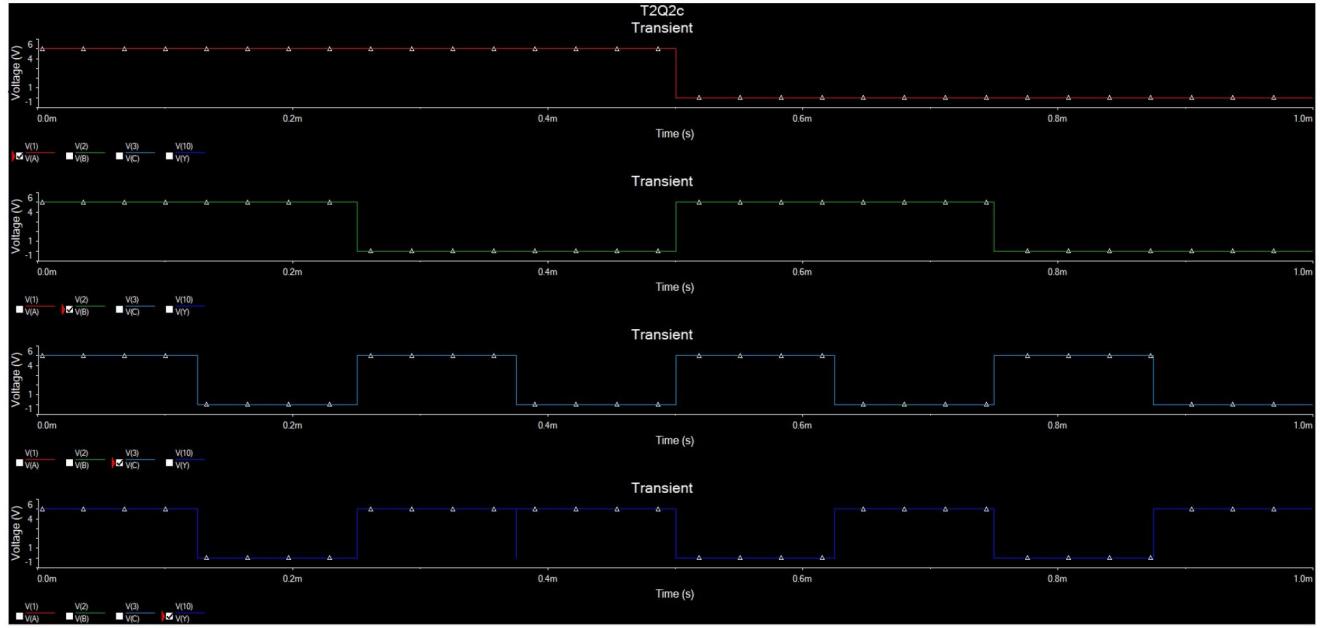


(c)

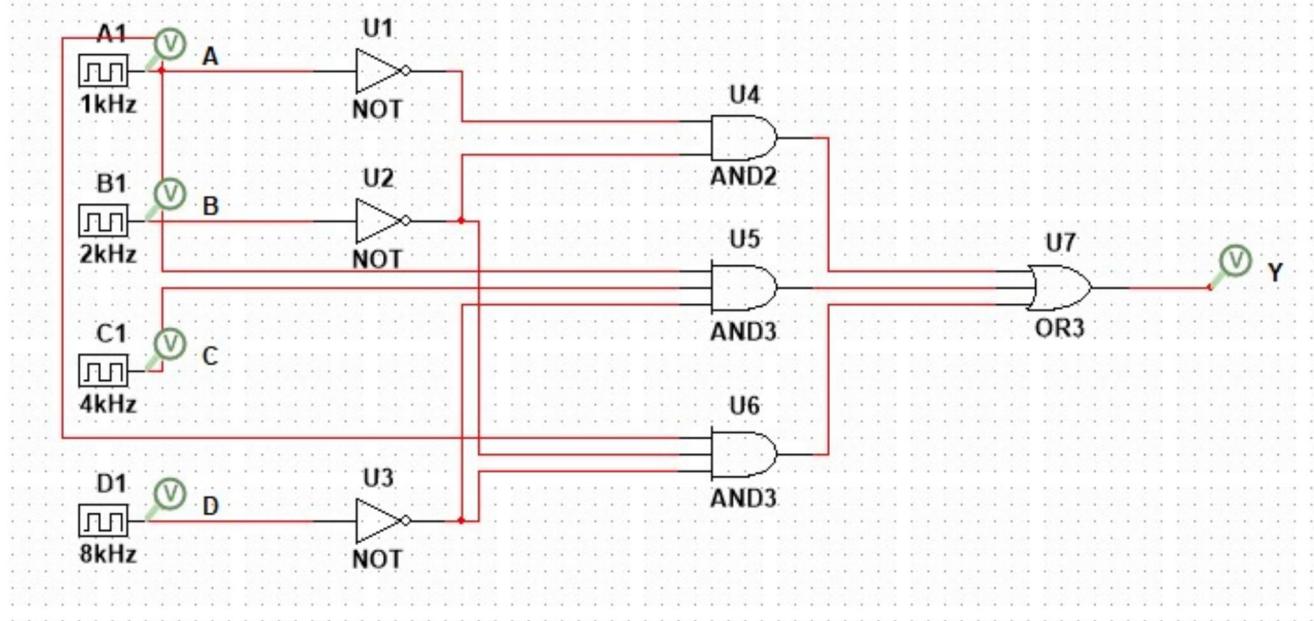




Question assigned to the following page: [2.3](#)

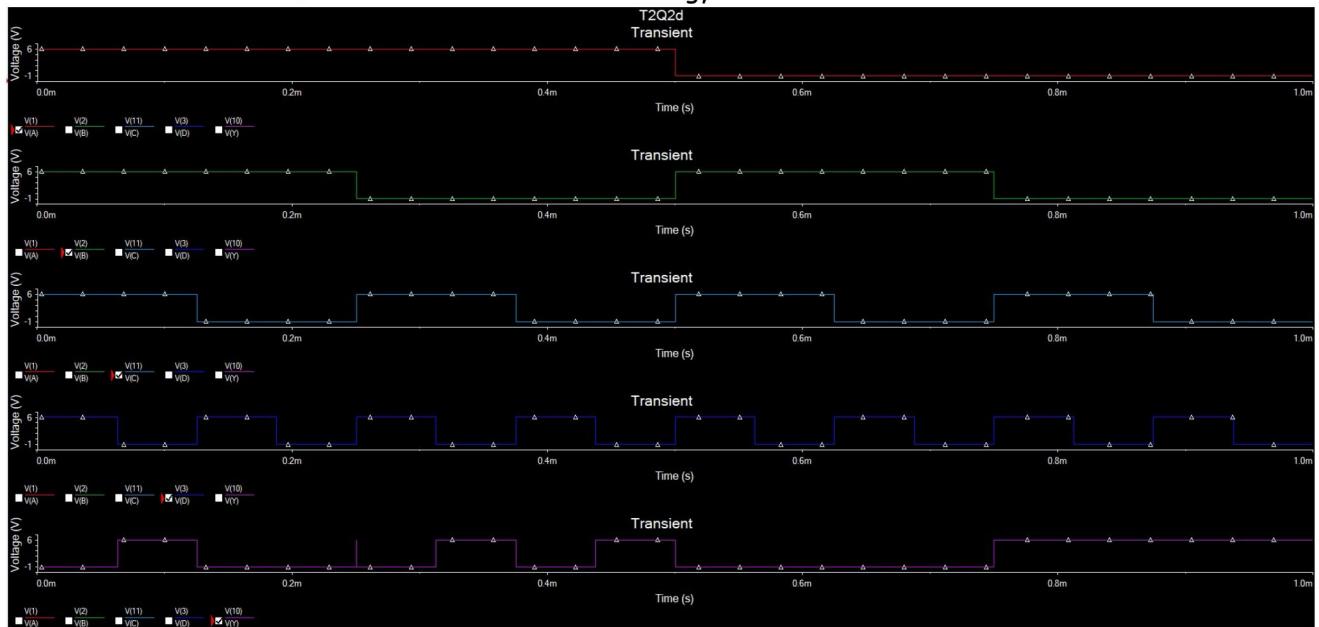


(d)

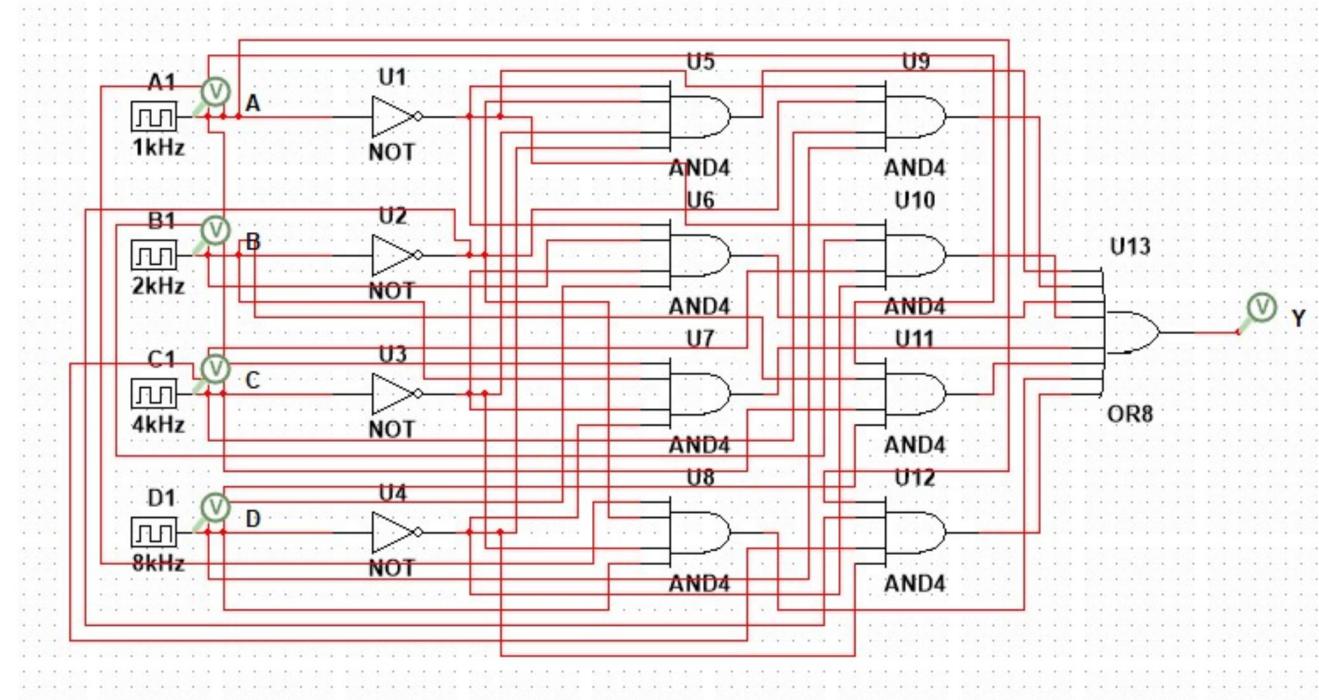




Question assigned to the following page: [2.3](#)

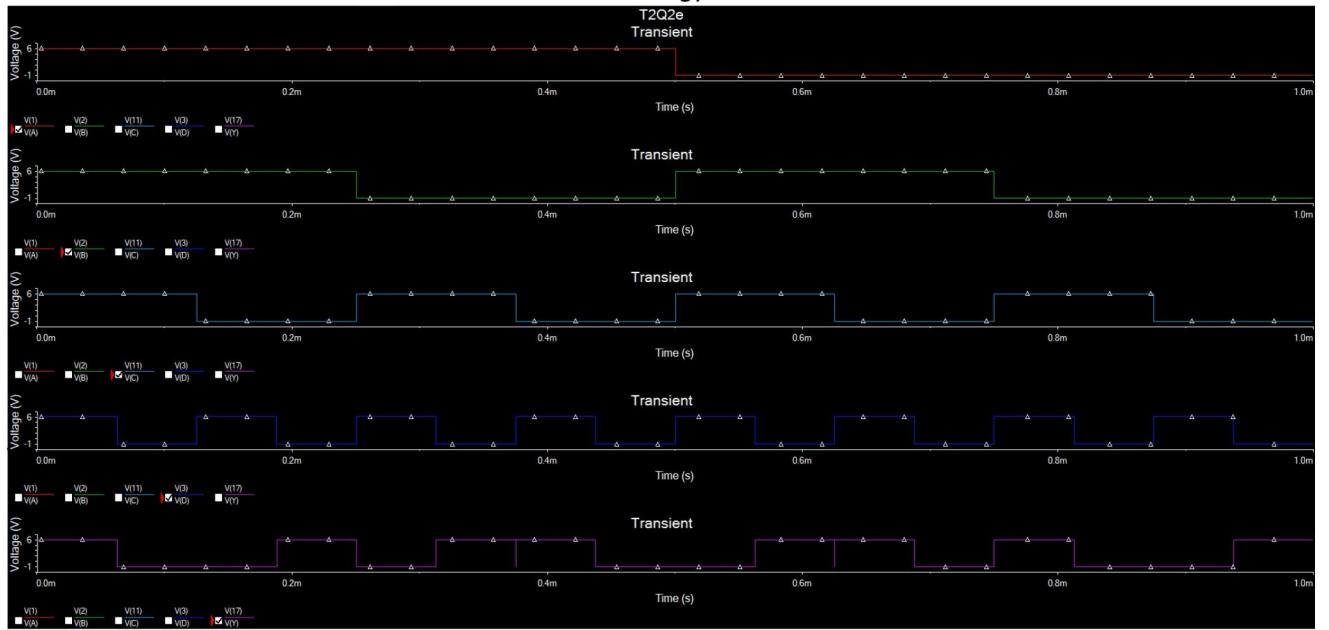


(e)





Questions assigned to the following page: [3.1](#) and [2.3](#)



(a)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

(b)

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(c)

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

(d)

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(e)

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

### 3. Majority voting and 14-segment alphabet display

Refering to the majority voting system introduced in the lecture, design a logic circuit with Multisim and show the voting result with a 14-segment display as follows (T for Trump and B for Biden).

- Show the design procedures and final circuit schematic. (15')



Questions assigned to the following page: [3.1](#) and [3.2](#)

- Let the Trump be 0, Biden be 1.

Truth table.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

K-map:

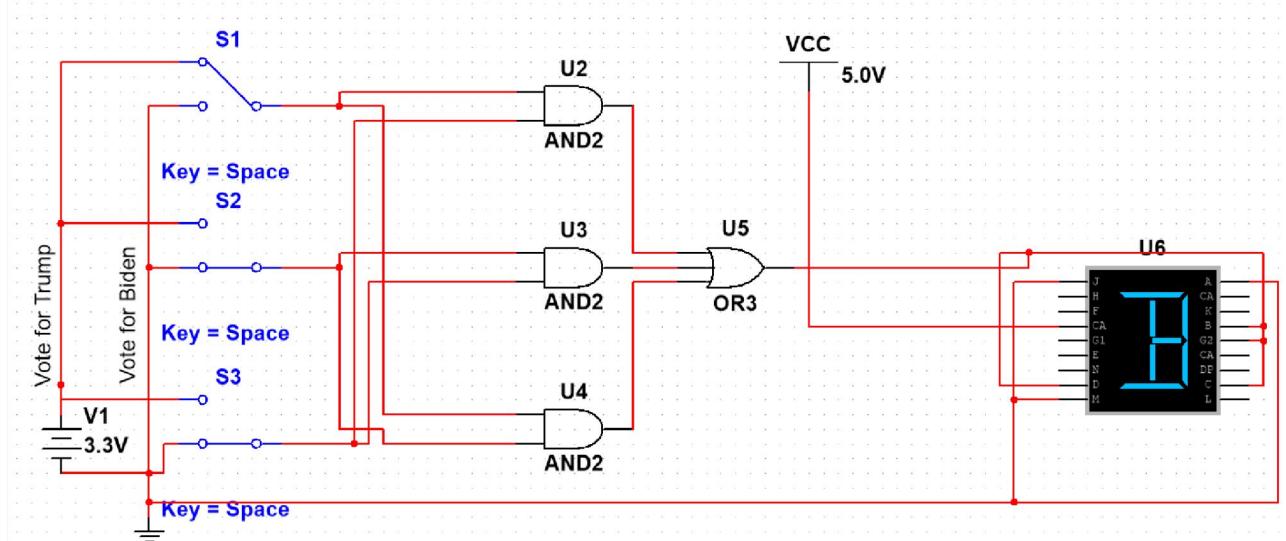
A\BC	00	01	10	11
0	0	0	1	0
1	0	1	1	1

$$Y = AC + BC + AB.$$

Truth table for display

	J	H	F	G1	E	N	D	M	A	K	B	G2	D2	C	L
Y=0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Y=1	1	0	0	0	0	0	0	0	1	1	1	0	1	1	0

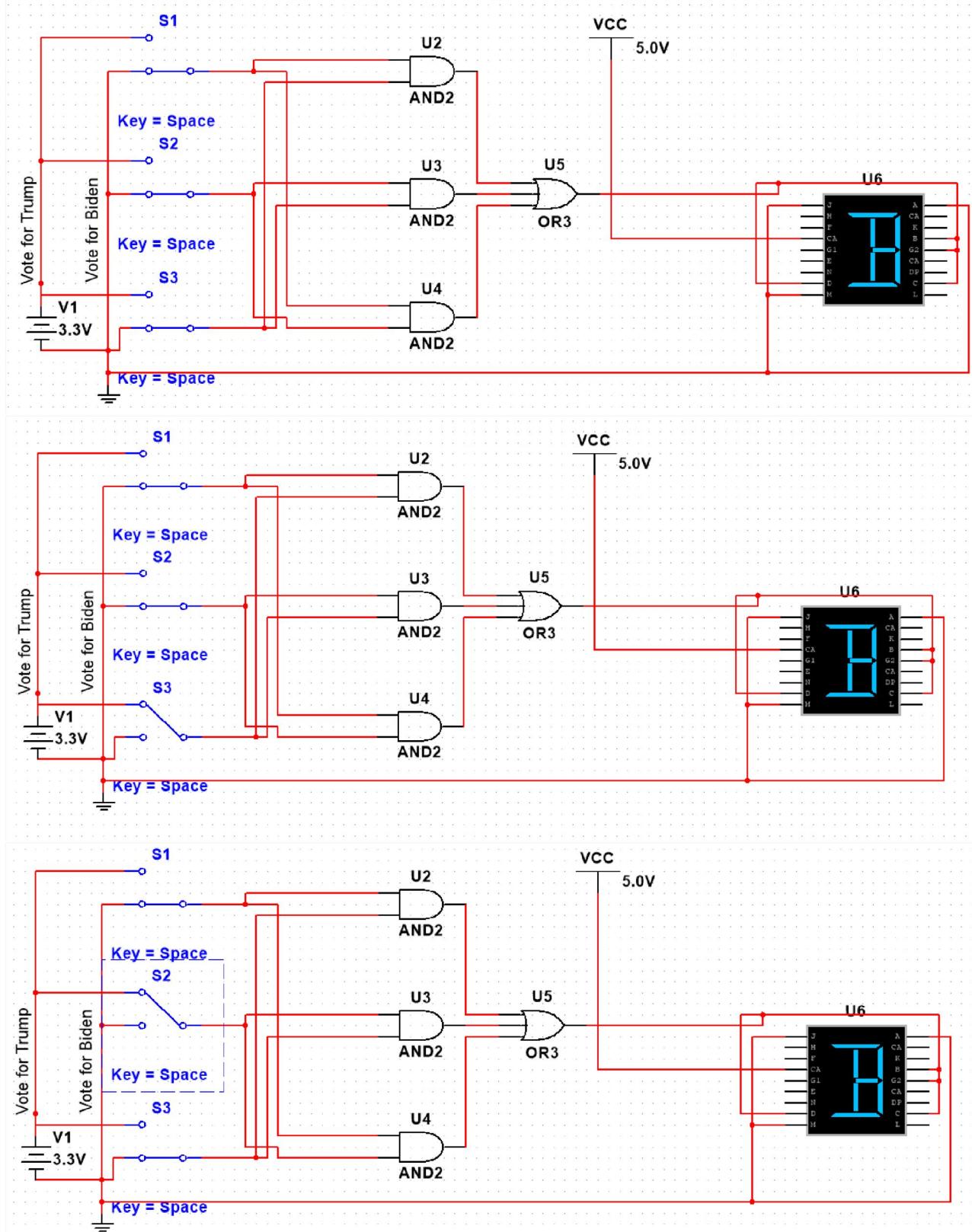
J, M, A are always 1, B, D, B, G2 change with Y, others remain 0.



- Show the result pictures of six input conditions. (5')

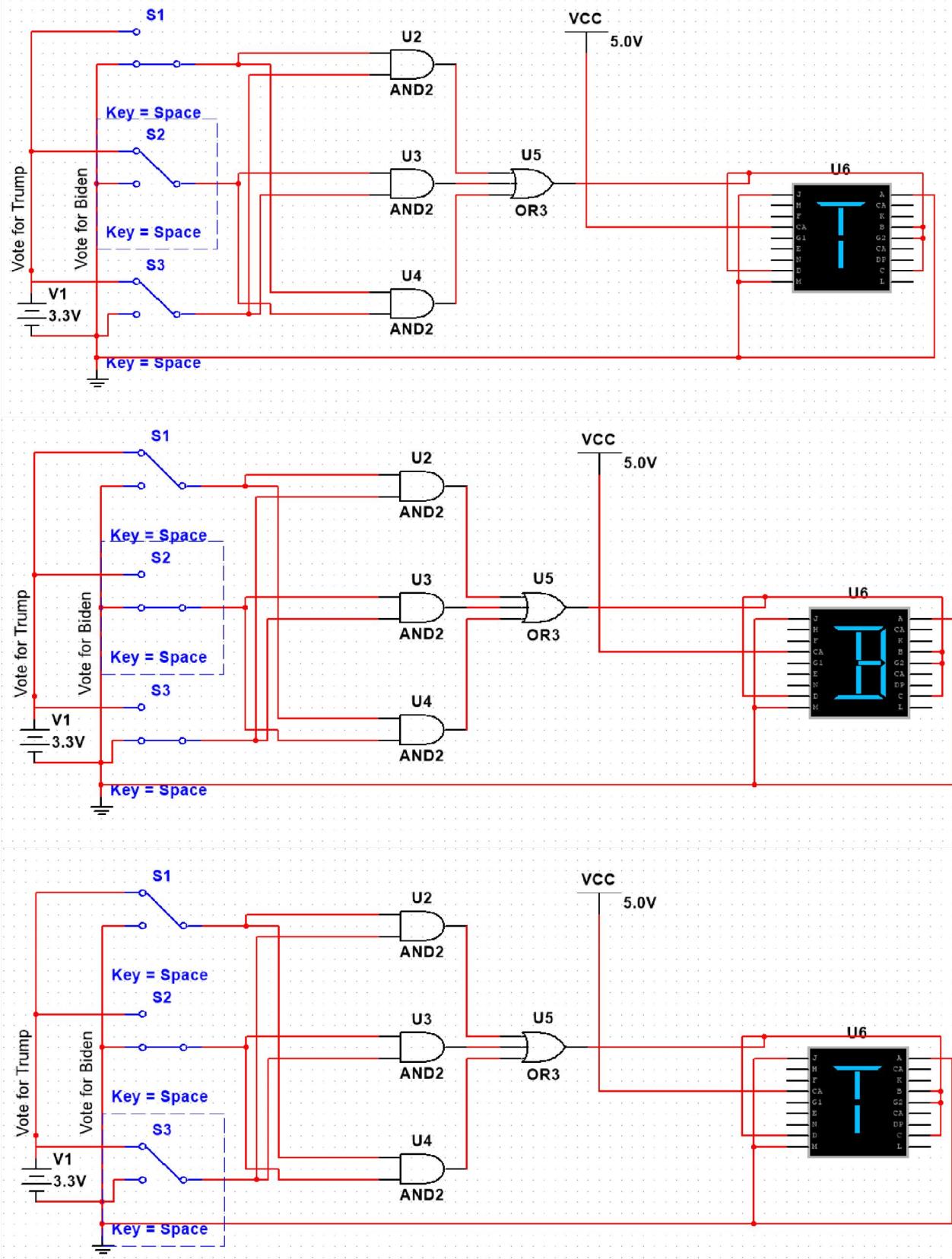


Question assigned to the following page: [3.2](#)



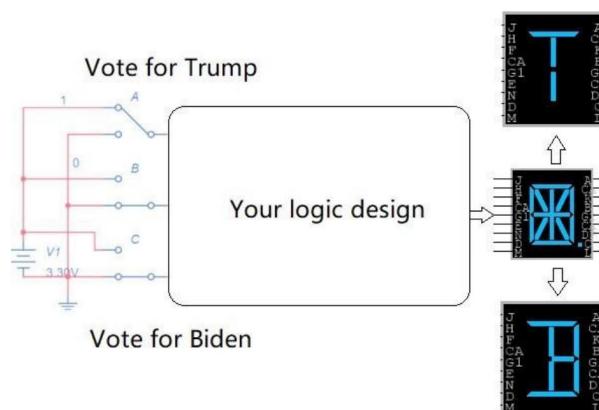
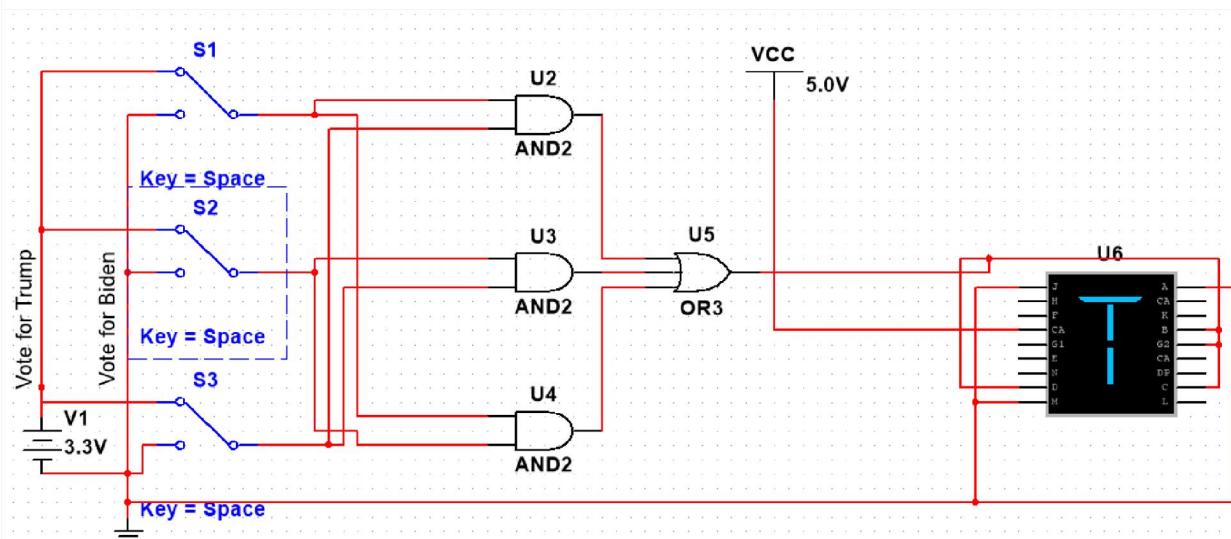
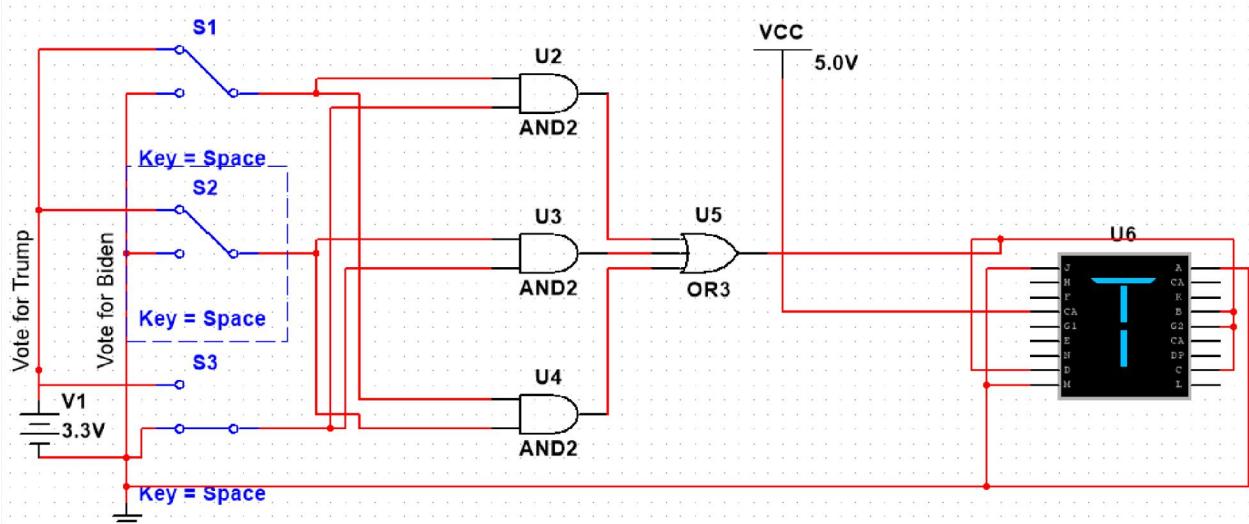


Question assigned to the following page: [3.2](#)





Question assigned to the following page: [3.2](#)

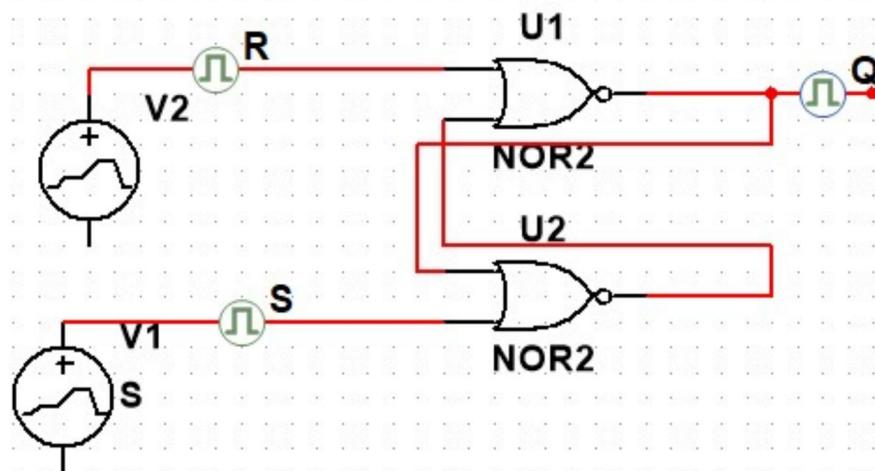
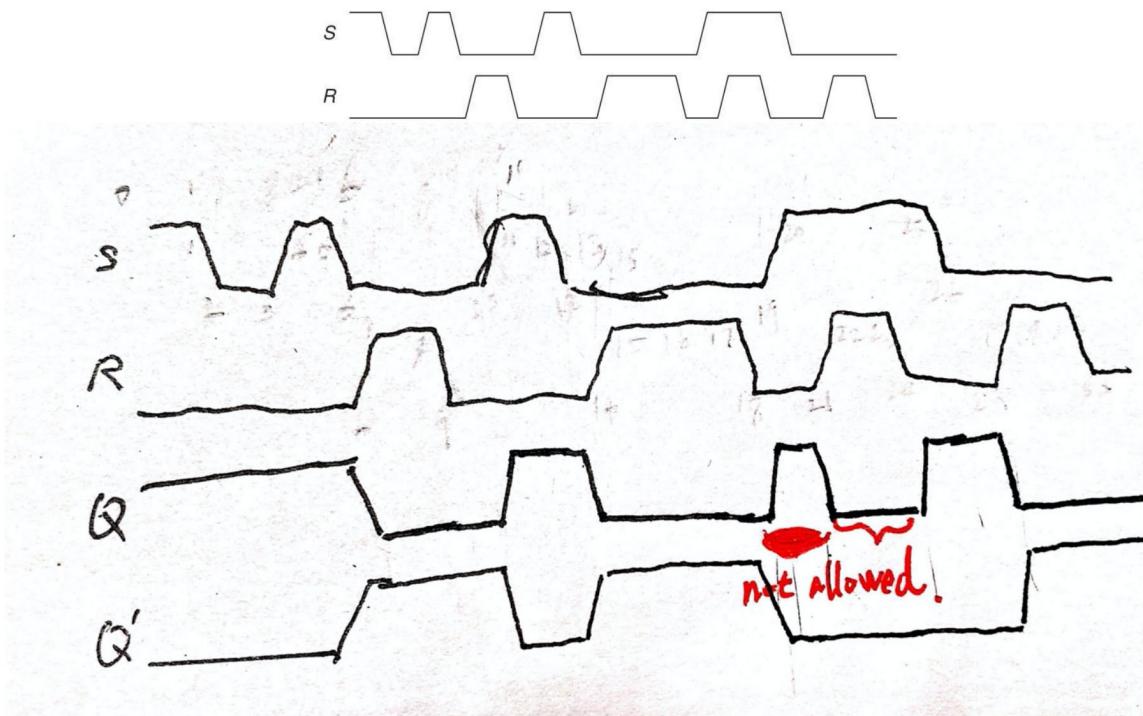




Question assigned to the following page: [4.1](#)

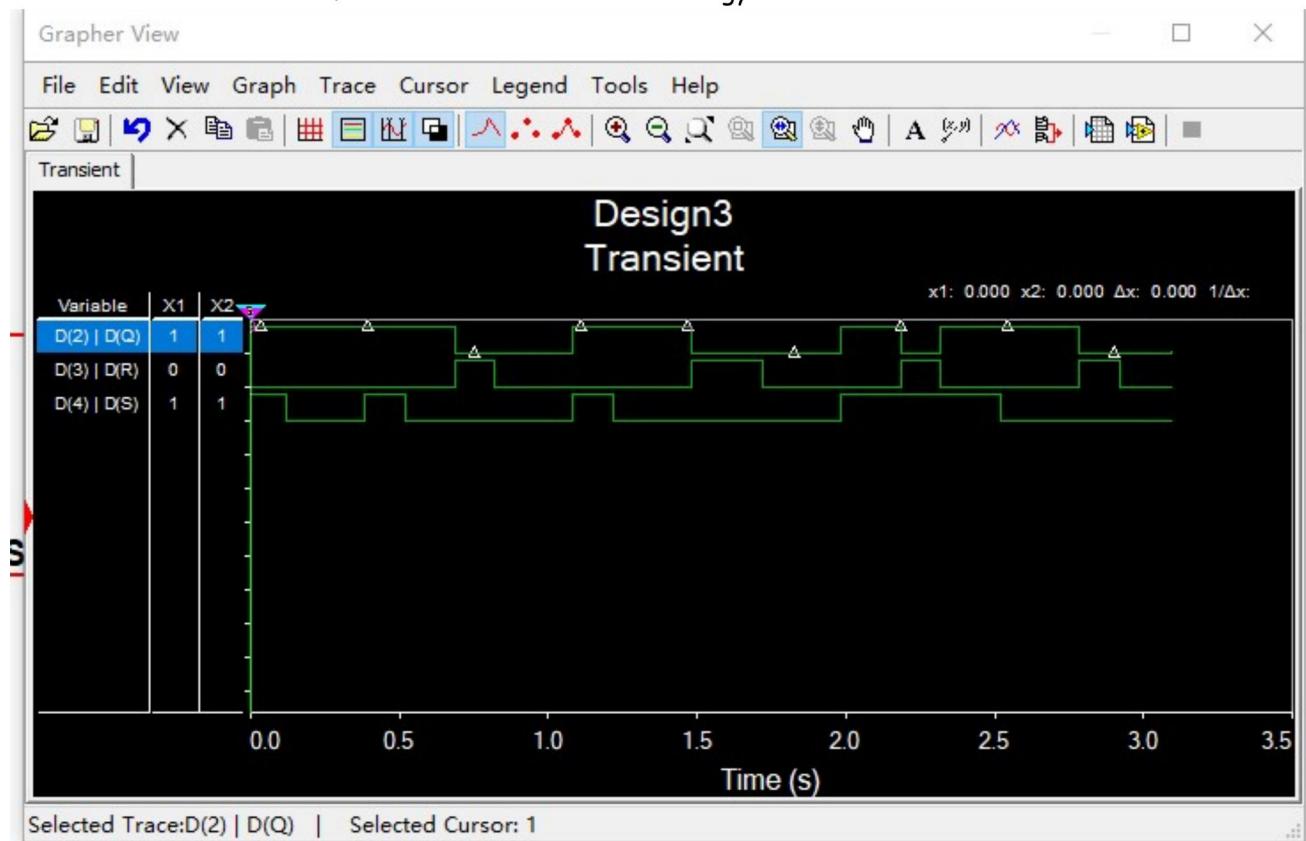
## 4. Sequential logic circuit exercises

- Given the input waveforms shown in the following figure, sketch the output, Q, of an SR latch. Check it out with Multisim and show the schematic and simulation result. (10')





Questions assigned to the following page: [4.1](#) and [4.2](#)

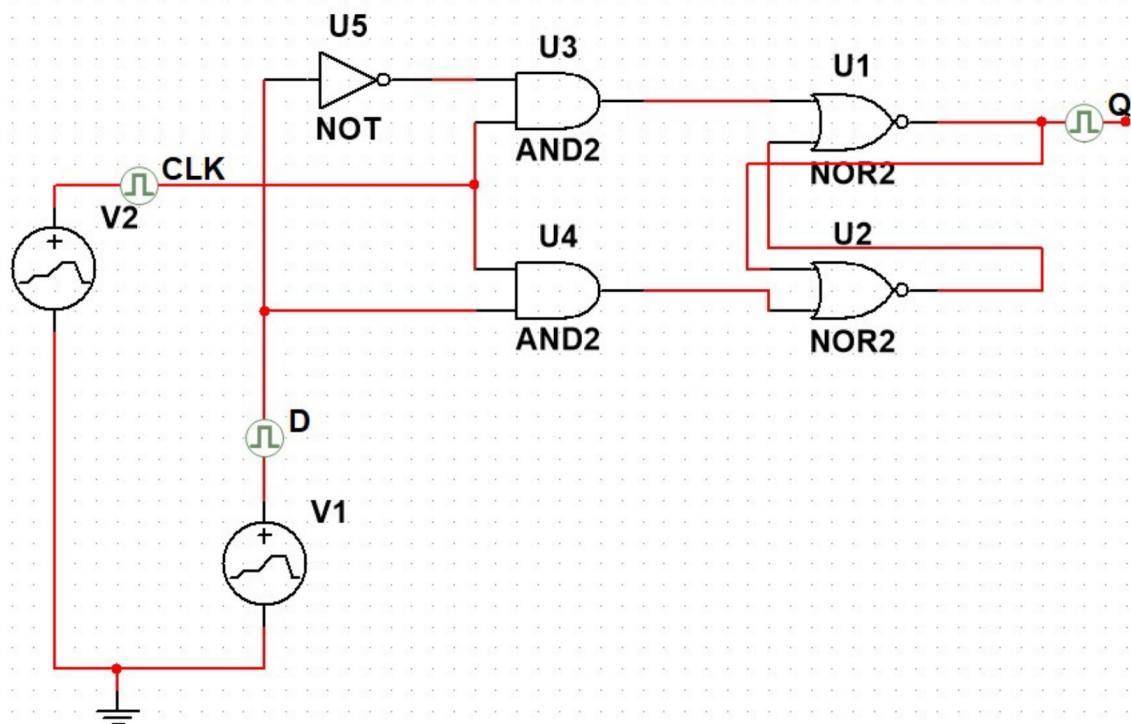
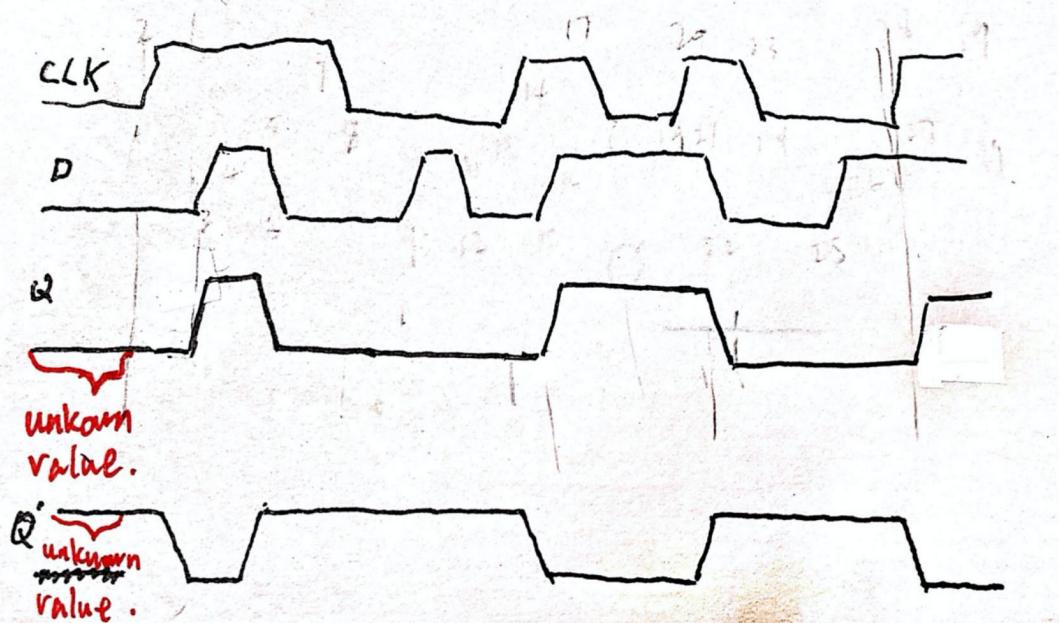


- Given the input waveforms shown in the following figure, sketch the output, Q, of a D latch. Check it out with Multisim and show the schematic and simulation result. (10')



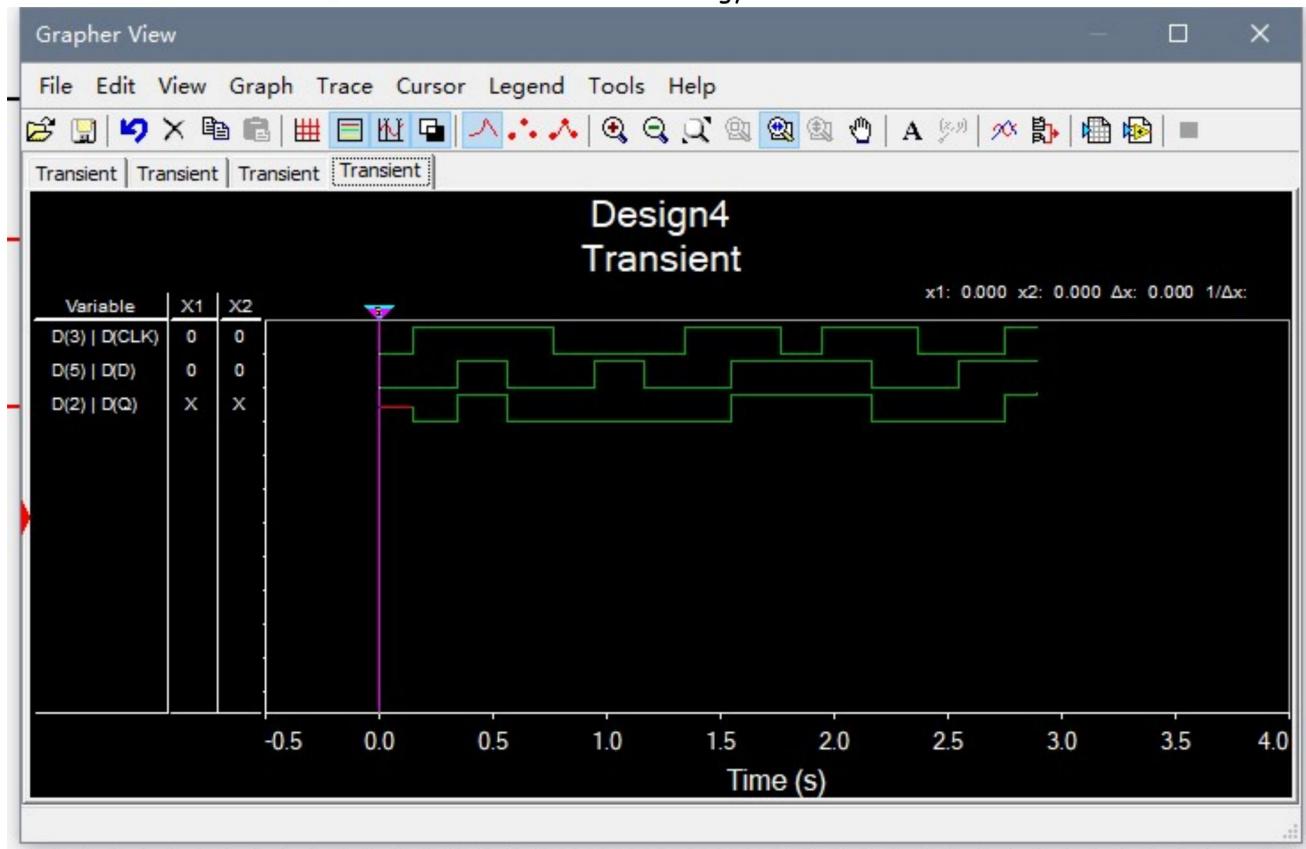


Question assigned to the following page: [4.2](#)





Question assigned to the following page: [4.2](#)



\* Please submit the softcopy of your solutions to the problems on gradescope.

\* All flow charts and codes should be enclosed in your solutions.

\* Discussion on methodology is allowed, yet, the assignment should be done individually. Plagiarism, once found, grades zero for the whole homework assignment!!

