2_3_Pipeline Model

1. Pipeline Timing Analysis

Two Core Cases

Normal Model

Enforcing au = p imes h

More Pipeline Case

Discussion: Intuition of Calculating h

2. Controller Design

Basic Model

Augmented Model

Summary

1. Pipeline Timing Analysis

For pipelined model, we will still use the example IBC system used in last part. But now, we assume we may use multiple core or we can build an pipeline structure.

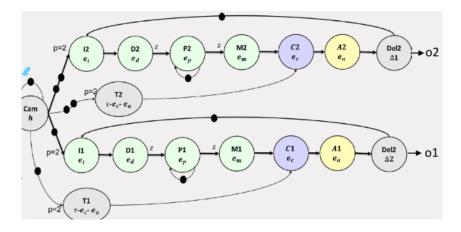
- Long sensor-to-actuator delay can degrade the control performance (e.g., longer settling time) if the controller is implemented sequentially
- Pipelining the sensing operation is a way tackle this design issue

Two Core Cases

- If frames can be processed independently, we can increase the rate of sensor-data processing by processing frames in parallel on multiple cores
- Pipelining reduces the sampling period
- Another requirement is: we need to guarantee the output interval are the same

Normal Model

For two pipeline case, based on the last above requirement, we can first draw the SDF model:



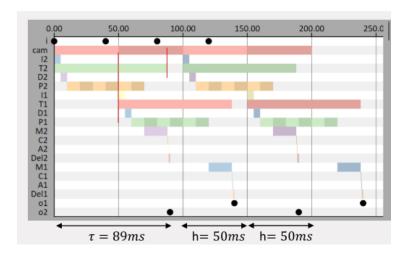
and we can calculate:

2_3_Pipeline Model 1

• sampling period $h = \lceil rac{ au}{p*f_h}
ceil f_h = 50$ ms

•
$$\Delta_1 = \Delta_2 = p \cdot h - au = 11 ext{ ms}$$

The execution schedule is shown in the following Figure



Enforcing au = p imes h

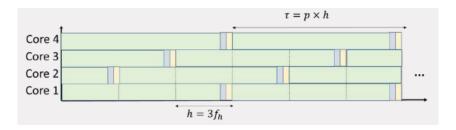
Because the analysis of controller design is quite complex (not in logic, but in augmented state dimension), we can enforce $\tau=p\times h$ to simplify the problem. Which means, the sensor-actuator delay is multiply of sampling time, so in a given timestep of sampling time, the input u will keep the same

ullet We can change the value of T_1 and T_2 to enforce au=p imes h

$$T_1 = T_2 = p \times h - e_a - e_c = (100 - 0.5 - 0.5)ms = 99ms$$

More Pipeline Case

- Three pipeline is almost the same
- For the 4 pipeline case, we will find that the Core 4 **does not help**. It repeats the activities in Core 1.



Discussion: Intuition of Calculating h

 τ/p means if we want to arrange p execution (average time so we use divide), how long is the interval between two execution. And then the intuition is the same as sequential model.

2. Controller Design

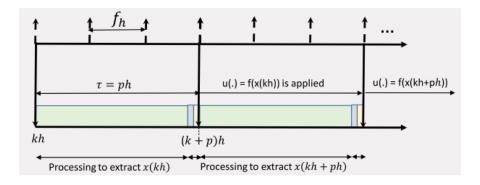
Here, we consider the model with enforcing au=p imes h

2_3_Pipeline Model 2

- sampling time $h = \lceil rac{ au}{p*f_h}
 ceil f_h$
- $au_{eff} = h \cdot p$

Basic Model

Because we use enforcing model, hen the input-sensing relation is shown in the graph



That means we have

- Continuous-Time model: $\dot{x} = Ax(t) + Bu(t au_{eff})$
- Discrete-Time model: $x(kh+h)=\phi x(kh)+\Gamma u(kh-ph)$, where:

$$\phi=e^{Ah} \ \Gamma=\int_0^h e^{As} B ds$$

Augmented Model

In order to solve the control problem and use control theory, we need to transform the delayed model into non-delayed model. We define augmented state z:

$$z(kh) = \left[egin{array}{c} x(kh) \ u(kh-ph) \ u(kh-ph+h) \ u(kh-ph+2h) \ & \cdots \ u(kh-h) \end{array}
ight]$$

Then we will have:

$$z(kh+h) = \left[egin{array}{c} x(kh+h) \ u(kh-ph+h) \ u(kh-ph+2h) \ u(kh-ph+3h) \ \dots \ u(kh) \end{array}
ight] = \left[egin{array}{c} \phi x(kh) + \Gamma u(kh-ph) \ u(kh-ph+h) \ u(kh-ph+2h) \ u(kh-ph+3h) \ \dots \ u(kh) \end{array}
ight] = \left[egin{array}{c} \phi & \Gamma & \mathbf{0} \ \mathbf{0} & \mathbf{0} & I \ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{array}
ight] z(kh) + \left[egin{array}{c} \mathbf{0} \ \mathbf{0} \end{array}
ight] u(kh)$$

Summary

- Can use pipeline to **pipelining the whole task:**
 - always used when the details of **processing step is not known**, that is we cannot divide the task into several steps
 - $\circ \ au > h$, for augmented state model, we need more previous input
 - marginal effect: after arriving at a given number of pipeline, more processor will have no improvements

2_3_Pipeline Model 4