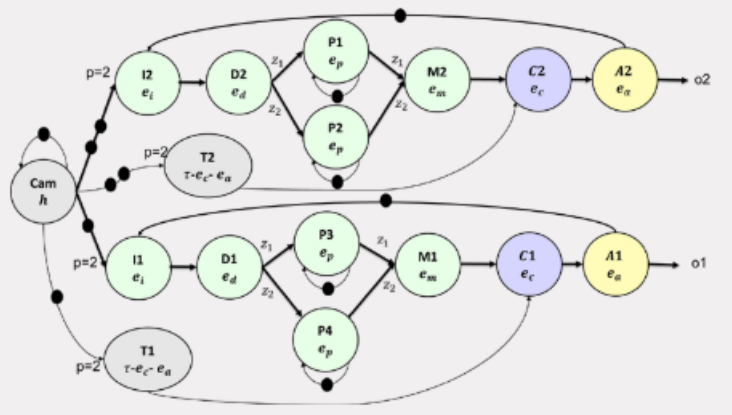
2_5_Parallel-Pipeline Mix Model

For parallel + pipeline model, we will still use the example IBC system used in last part. But now, we assume we may use parallel structure and pipeline structure

1. Timing Analysis

Compared to standard configuration, we assume we have 4 available cores and 2 pipes.

A example parallel-pipeline structure is shown in the following figure



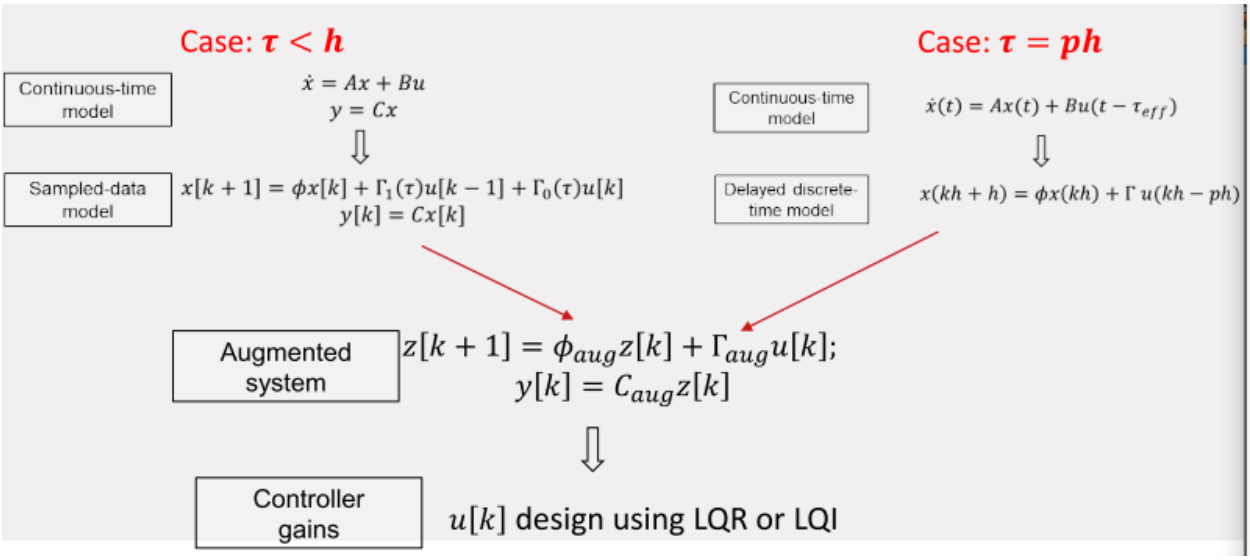
- First we calculate the sensor-to-actuator delay: $\tau = 59ms$
- Then we can calculating sampling period $h = \lceil \frac{\tau}{p \times f_h} \rceil f_h = 30ms$
- Then for simplifying, we can calculate $T_1 = T_2 = p \times h - e_c - e_a = 59ms$

Design Space

	No. of cores n_{avl}	Degree of parallelism $n_c^{\|\|}$	Pipeline depth p	(h, τ)
Sequential	1	1	1	h=90ms, τ=89ms
Parallel	2	2 (equal load sharing)	1	h=60ms, τ=59ms
Pipelined	2	1	2	h=50ms, τ=89ms
Pipelined + Parallel	4	2 (equal load sharing)	2	h=30ms, τ=59ms
Parallel	4	4	1	h=50ms, τ=49ms
Pipelined	4	1	4	h=30ms, τ=89ms

2. Controller Design

After decide h and τ, we need to design the controller



Summary

- We can mix parallel processing and pipeline