ECE 2140 System on a Chip

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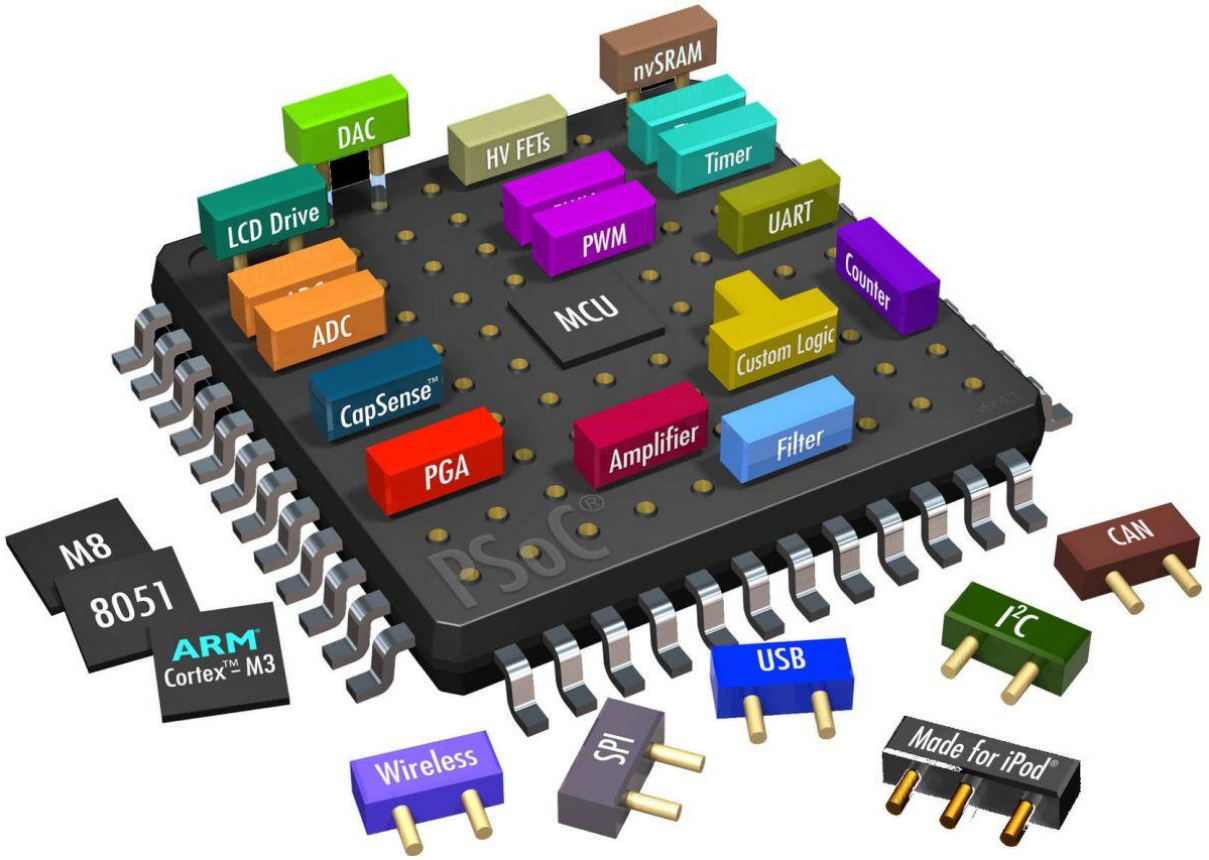


Overview

Description

- Transistor density doubles every 18 months which enables more and more features to be placed into a single VLSI chip. System-on-a-Chip refers to VLSI chips that contain both logic and CPUs that work together to implement a single system. Designing these devices involves both hardware and software design and presents numerous design tradeoffs. What should be in logic and what should be kept in software? How do these difference components talk to each other? Most of these tradeoffs are application-specific and as such, this course will be entirely project-based.

Instructor:

- Dr. Ray Hoare rayhoare@concurrenteda.com

- No on-campus office, so office hours will be held after class as needed and if requested.

Topics

The following topics will be covered in class and through team projects:

- SOC Overview
- Xilinx Zynq FPGAs
- Performance Analysis
- Hardware/Software Partitioning
- Test Planning and Test Benches
- Integration and Testing

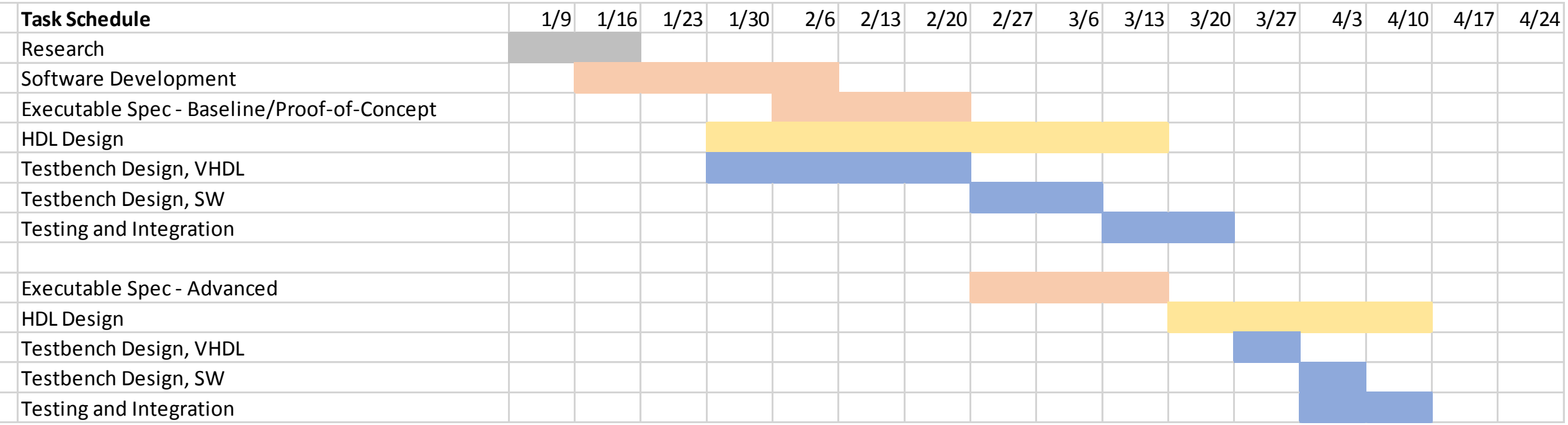
Prerequisite

- Computer Engineering background
- ECE 2120 Hardware Design Methodologies
- VHDL design experience
- Personal laptop with Vivado Webpack Installed (www.xilinx.com)

Schedule

	Class Schedule	1/9	1/16	1/23	1/30	2/6	2/13	2/20	2/27	3/6	3/13	3/20	3/27	4/3	4/10	4/17	4/24
Prof	SOC Overview, Project Presentation Req																
	No Class (MLK)																
Prof	VHDL Cram Course																
Team PPT	Project Presentations: Overview																
Prof	Zynq and AXI Interconnect (JumpStart), Project Mtg																
Prof	VHDL Cram Course, SW Demo Req																
Prof/ Mtg	Performance Analysis and HW/ SW Partitioning, Test Plan Req																
Team PPT	Project Presentations: SW Demo																
	Spring Break																
Prof/ Mtg	VHDL Cram Course: Test Benches, Baseline Demo Req																
Team PPT	Project Presentations: HW/SW Parition and Test Plan																
Mtg	Project Mtgs																
Team PPT	Project Presentations: Baseline Demo																
Open	Open																
Team PPT	Final Presentations & Demo																

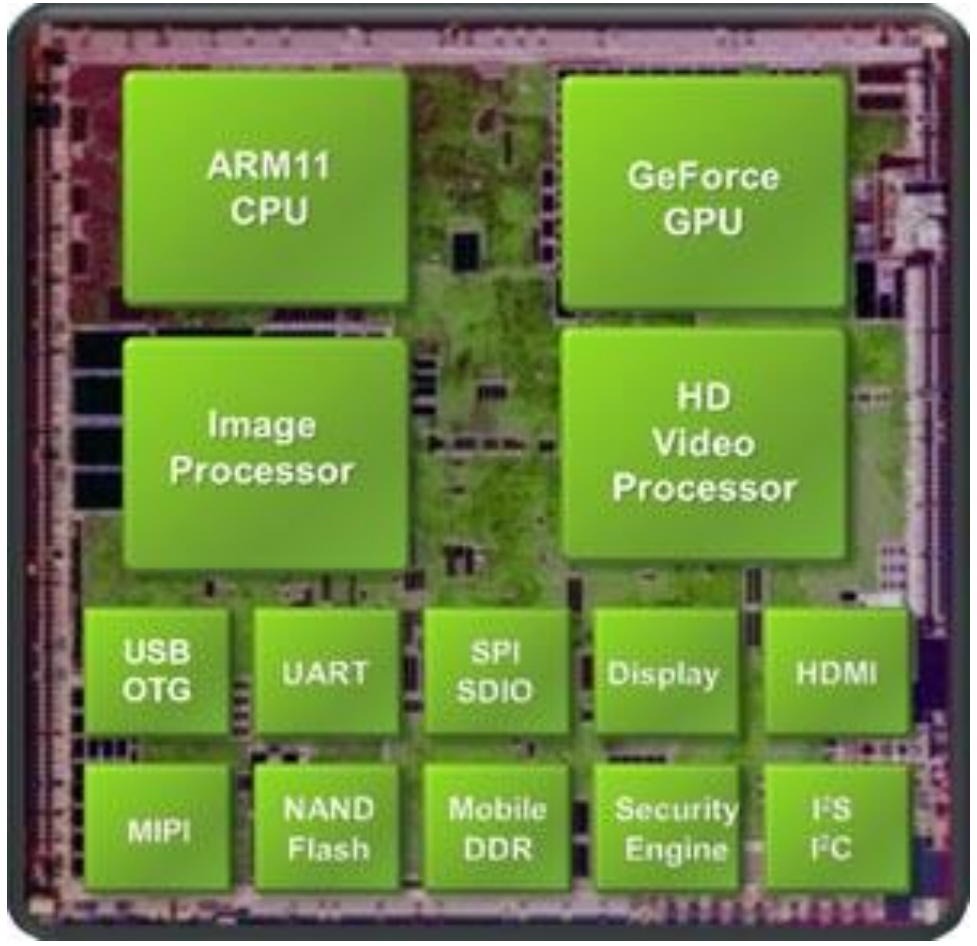
Work/Task Schedule



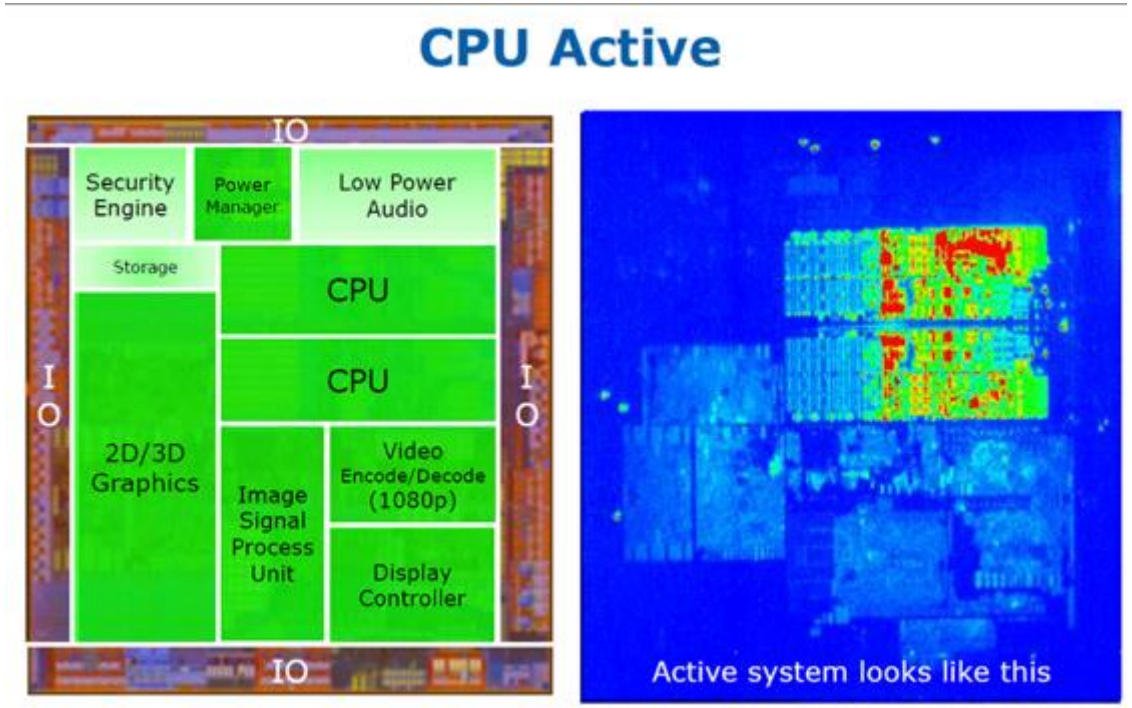
Grading

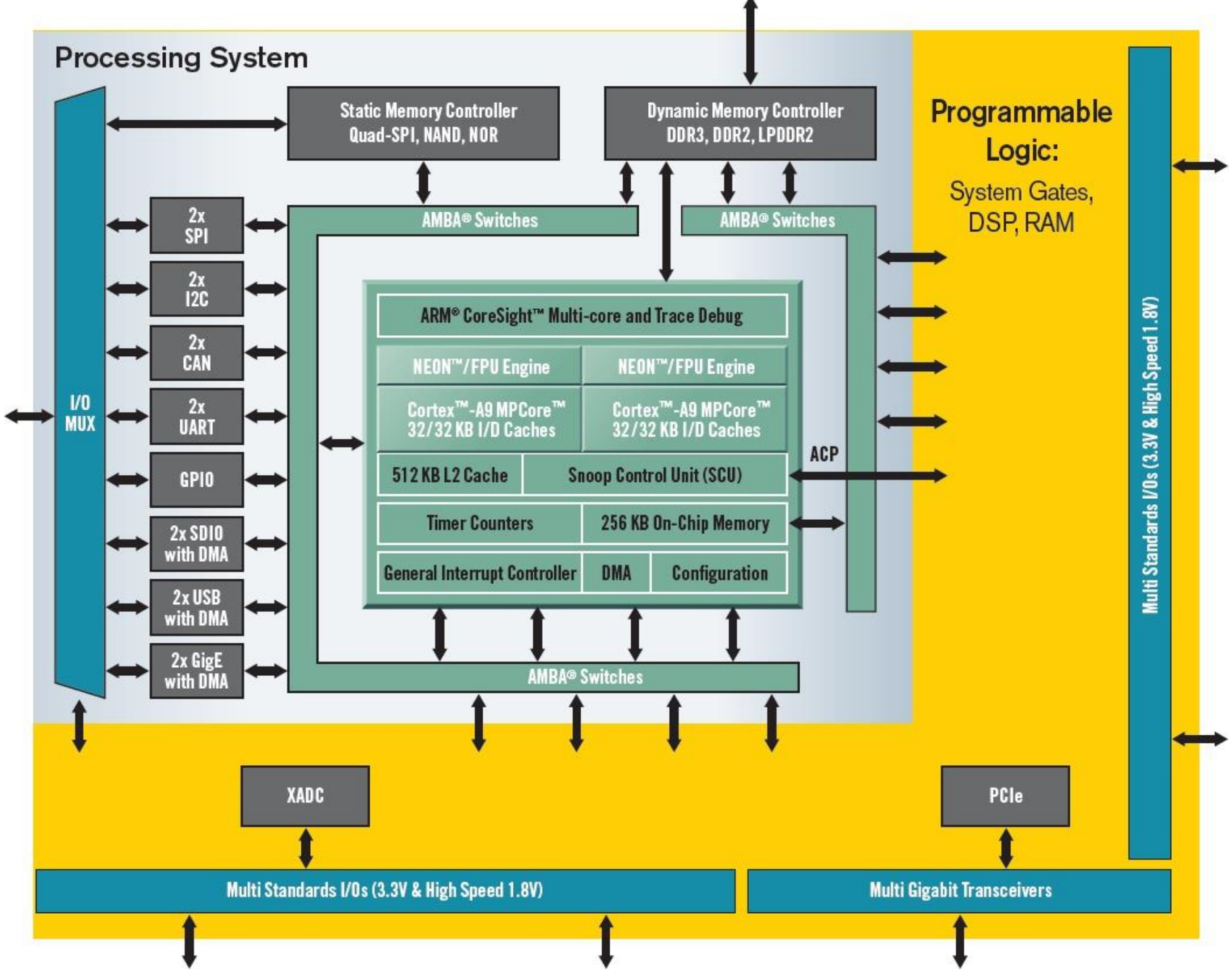
Presentations	25
Software Demonstration	15
Test Bench Design	10
HW/SW Test Bench + HDL Framework	10
HDL Functionality and Performance	20
Integrated Solution	15
On Schedule	5
Advanced Features	5 Point Bonus

NVIDIA TEGRA SOC



Intel Clover Trail

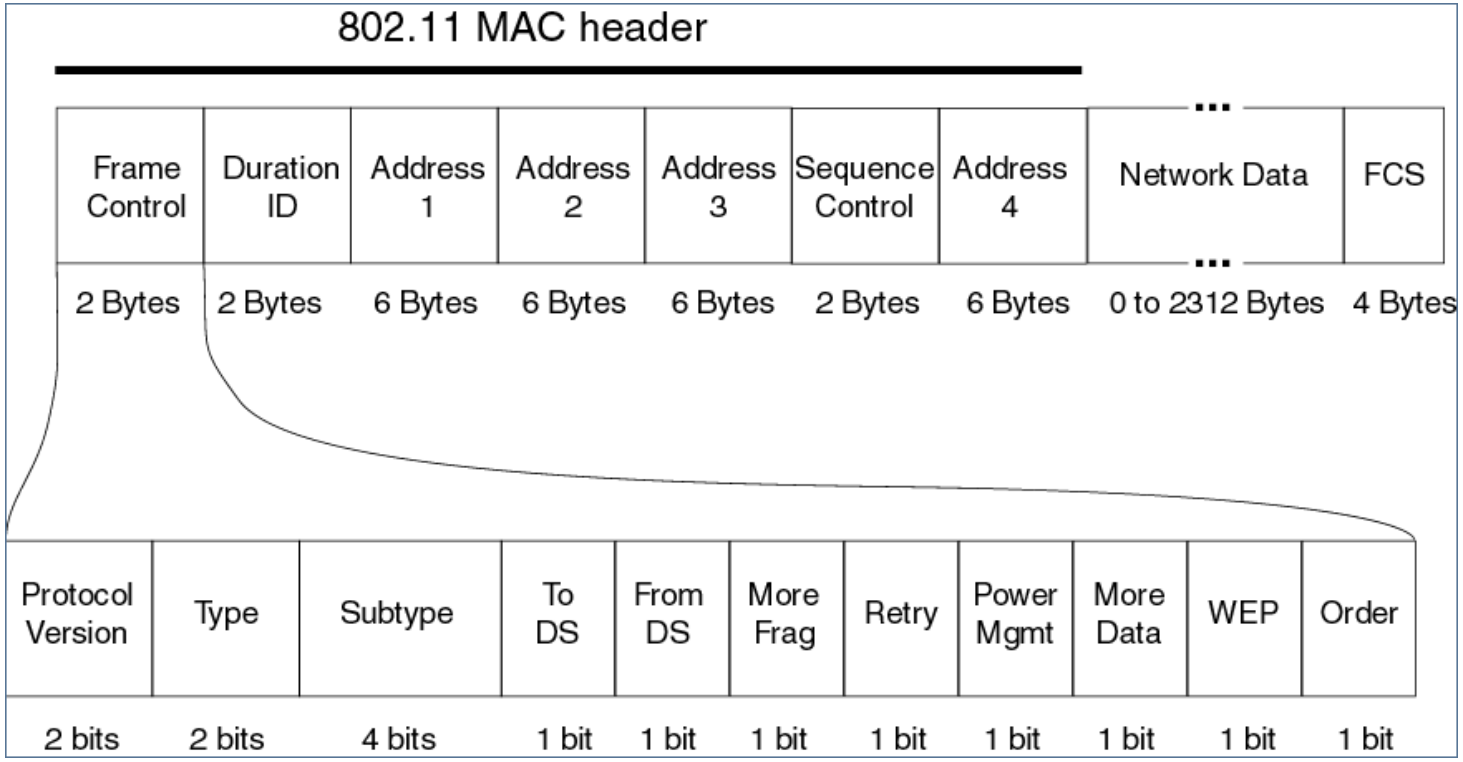



Processing System
Static Memory Controller
Quad-SPI, NAND, NOR
Dynamic Memory Controller
DDR3, DDR2, LPDDR2
Programmable
Logic:
System Gates,
DSP, RAM
I/O
MUX
2x
SPI
2x
I2C
2x
CAN
2x
UART
GPIO
2x SDIO
with DMA
2x USB
with DMA
2x GigE
with DMA
AMBA® Switches
AMBA® Switches
ARM® CoreSight™ Multi-core and Trace Debug
NEON™/FPU Engine
NEON™/FPU Engine
Cortex™-A9 MPCore™
32/32 KB I/D Caches
Cortex™-A9 MPCore™
32/32 KB I/D Caches
ACP
512 KB L2 Cache
Snoop Control Unit (SCU)
Timer Counters
256 KB On-Chip Memory
General Interrupt Controller
DMA
Configuration
AMBA® Switches
Multi Standards I/Os (3.3V & High Speed 1.8V)
XADC
PCIe
Multi Standards I/Os (3.3V & High Speed 1.8V)
Multi Gigabit Transceivers

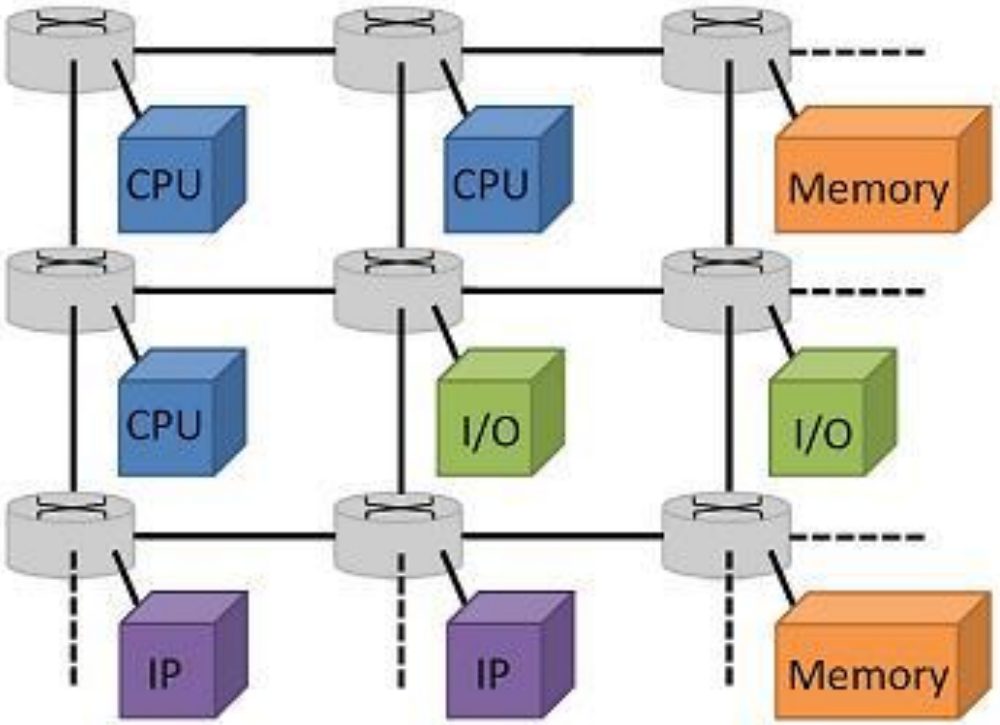
Projects

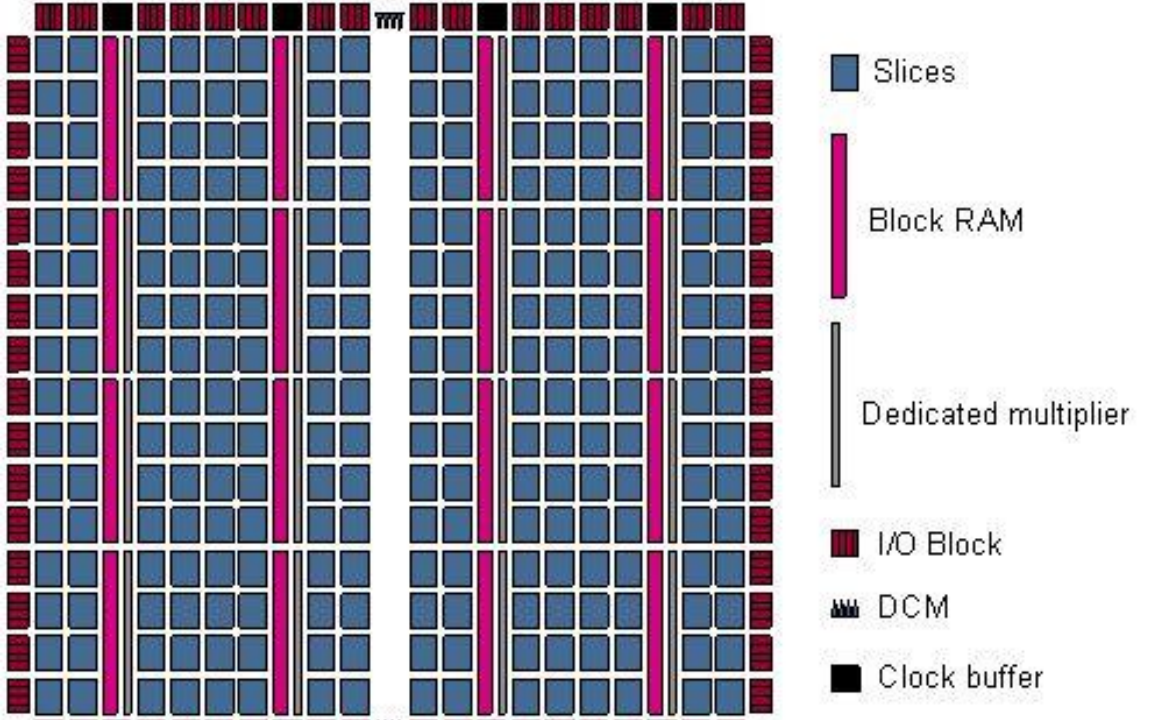
- 4 People per team.
  - Software
  - VHDL
  - Testing and Integration
- Projects
  - 10/40 Gb/s Ethernet MAC
  - Network on a Chip
  - Data Compression / Decompression
  - DSP CPU – Implement basics of MIPS using a DSP Slice
  - UDP/ TCP Offload Engine
  - Convolutional Neural Networks

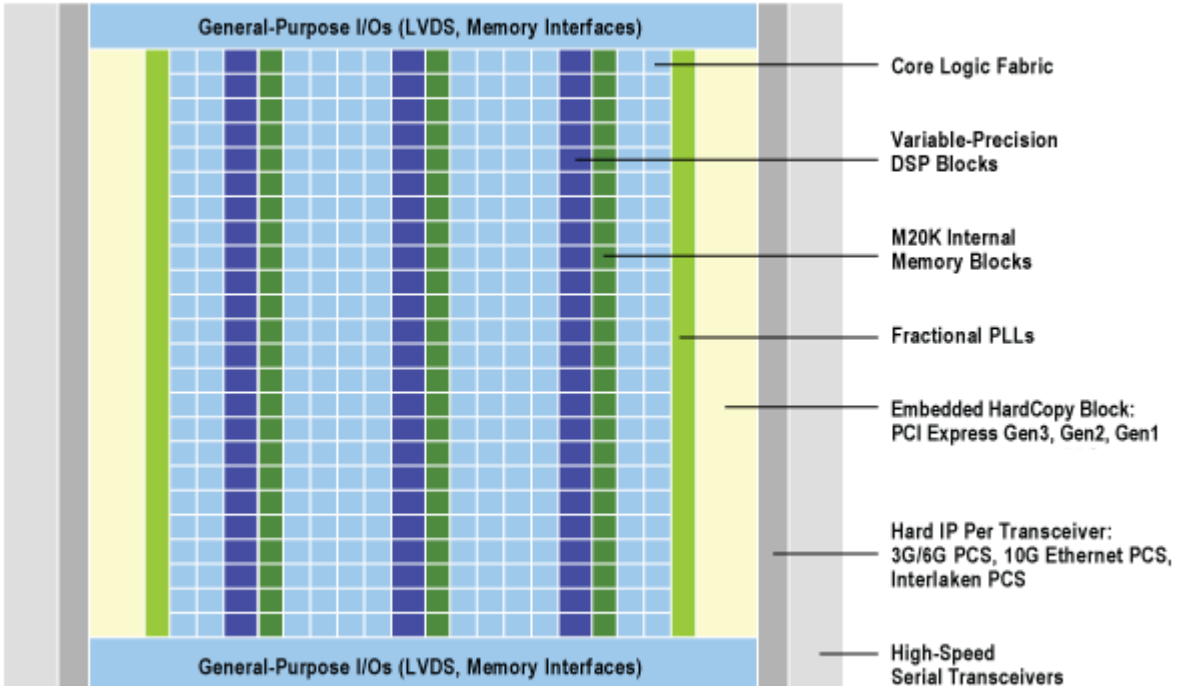
Ethernet MAC



Network on a Chip

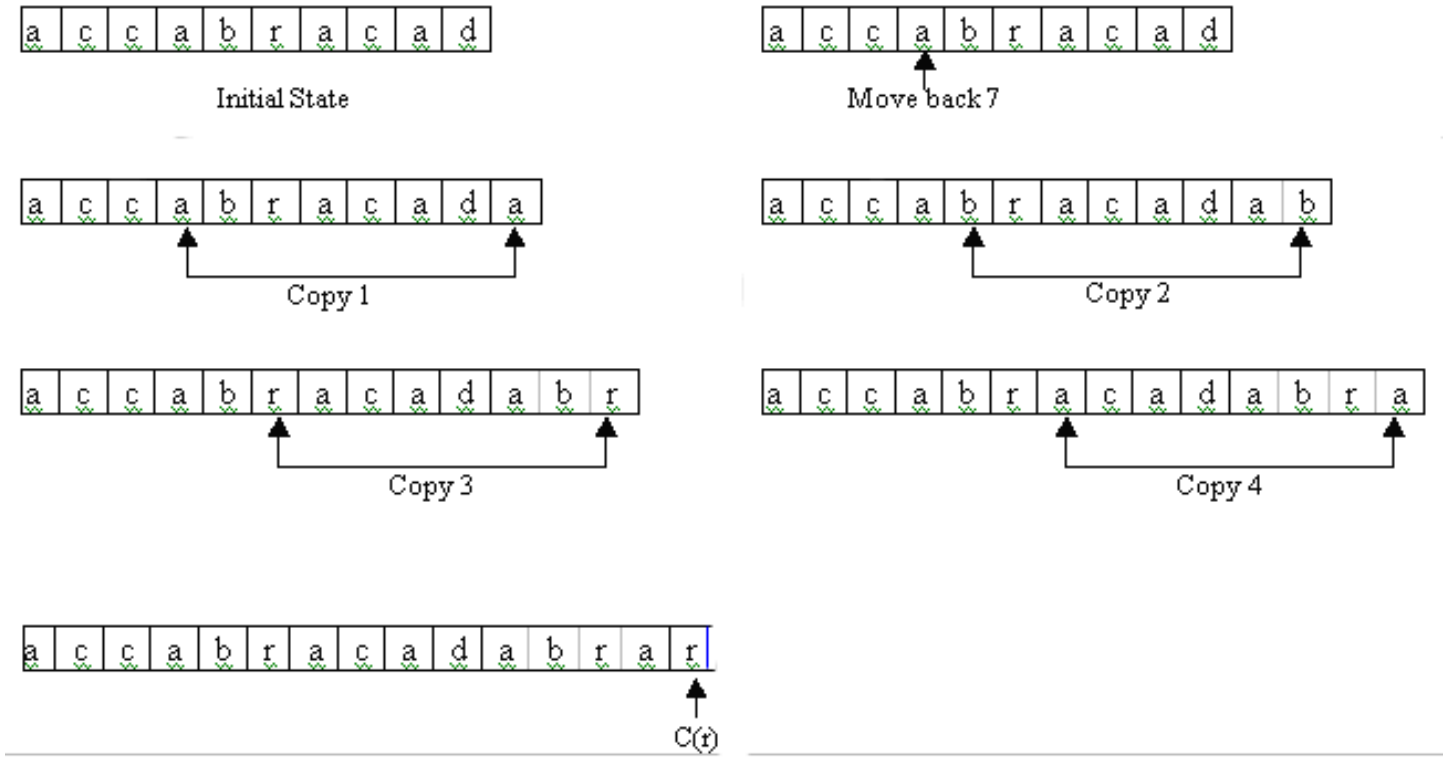






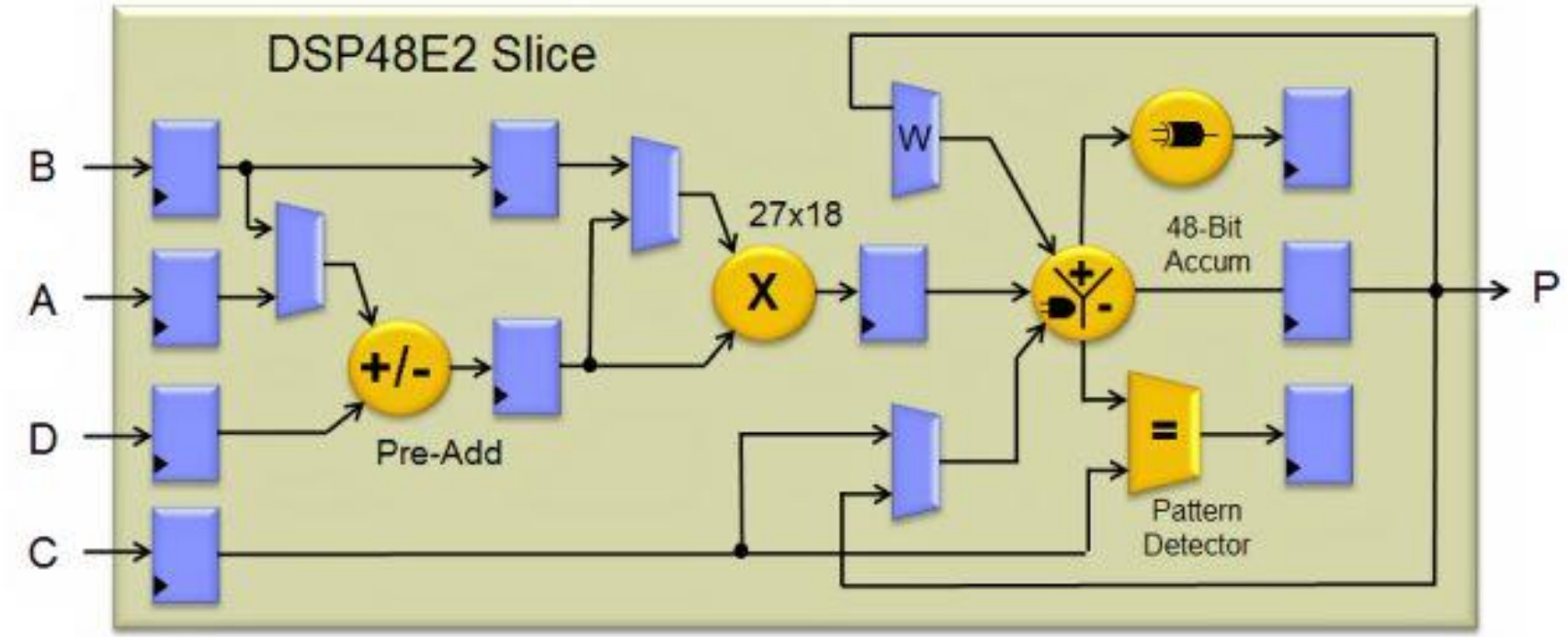
Data Compression

- https://sourceforge.net/projects/liblzw/?source=typ_redirect

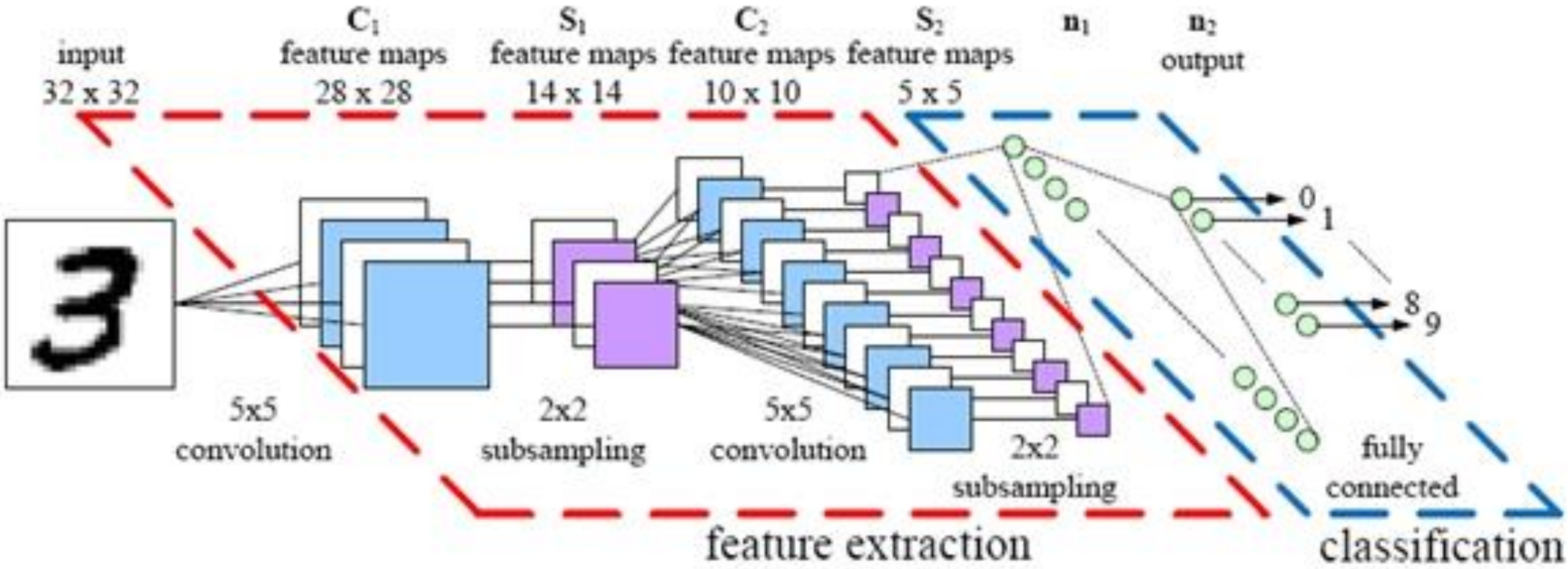


DSP CPU

http://www.mrc.uidaho.edu/mrc/people/jff/digital/MIPSir.html



AlexNet (CNN)


input
32 x 32
C1
feature maps
28 x 28
S1
feature maps
14 x 14
C2
feature maps
10 x 10
S2
feature maps
5 x 5
n1
n2
output
0
1
8
9
5x5
convolution
2x2
subsampling
5x5
convolution
2x2
subsampling
fully
connected
feature extraction
classification