# Lab Report #2

# Name: \_\_\_\_\_\_\_\_\_\_ Netid: \_\_\_\_\_\_\_\_\_\_\_

**Note: for this lab, you need to submit your corrected "max3sint16b.v" file and this report. Zip them together and name the zip folder after your netid.**

1. (10 pts) What is the third error identified in the video? What is the first test vector that fails because of this error (warning: the test vectors that you have are different from what is in the video. Capture a screen shot of the simulation showing the vectors the fail and explain why it fails. The vectors need to be formatted as signed decimal as shown in the video. Arrange the signals in the waveform viewer from top to bottom in the following order: a, b, u1\_lt, max\_ab, c, u2\_lt, y . The screenshot MUST have the yellow cursor over the failing vector.
   1. The third error was max\_ab was not defined as a 16 bit ( [15:0]), which let the result of the first test to be false when running the simulation.

A screenshot of a computer

Description automatically generated

1. (10 pts) What is the fourth error identified in the video? What is the first test vector that fails because of this error (warning: the test vectors that you have are different from what is in the video. Capture a screen shot of the simulation showing the vectors the fail and explain why it fails. The screenshot MUST have the yellow cursor over the failing vector.
   1. The first test to fail was test 3 at 250000s. It failed due to the second signed operator not being properly set up. It was initially c < max\_ab but needs to be max\_ab < c

A screenshot of a computer

Description automatically generated

1. (10 pts) What is the fifth error identified in the video? What is the first test vector that fails because of this error (warning: the test vectors that you have are different from what is in the video. Capture a screen shot of the simulation showing the vectors the fail and explain why it fails. The screenshot MUST have the yellow cursor over the failing vector.
   1. The fifth error was due to max\_ab not being declared as signed.

A screenshot of a computer

Description automatically generated

1. (5 pts) After correcting all errors, capture a screenshot showing the last vector that causes the message ‘All vectors passed’ to be printed (can capture this message in the screenshot as well).

A close up of numbers

Description automatically generated

1. (5pts) Run the implementation, then run the ‘Post Implementation Timing Simulation’. Capture a screenshot showing the message ‘All vectors passed’. In the screenshot, have the ‘uut’ selected in the ‘Scope’ tab, and have the screenshot include some of the signals from the ‘uut’ (there will be some signals named ‘…OBUF’ in here in addition to other signals).

A screenshot of a computer

Description automatically generated

1. (10 pts) What is the difference between declaring a signed versus an unsigned wire?
   1. The difference between declaring a wire signed or unsigned is that is that signed wires are in 2’s complement
2. (10 pts) What type does Verilog assume if a wire isn’t declared? How can this cause a problem for a multi-bit signal?
   1. Verilog assumes that it is an unsigned wire, this can cause major problems in multi-bit signals due key operations that are being done. For instance in this lab because we did not have the max\_ab variable set as signed. When we went to debug it we could not tell what the initial problem was until we had look at the errors and problems we were getting from a 2’complement point of view.
3. (10 pts) Why use behavioral simulation instead of other simulations when debugging Verilog?
   1. You run behavioral simulation instead of other simulation, so that when you are debugging you can correlate what you see in the simulator with the RTL statements in your Verilog.
4. (10 pts) After you run behavioral simulation, what should you do next to find useful waveform that helps you debug? If there is no waveform presents in your simulation, how to do? How do you know the total time that you should run to pass all your test vectors when you execute “run” command in TCL?
   1. You should delete all the waveforms that are in the behavior simulation “name” column and replace them with the signals in the uut tap under scopes.
   2. If there are no waveform present you can go to the TCL at the bottom of the screen and use the command “run 1 us””, which stands for run simulation for 1 micro-seconds
   3. You look at the test bench and see that there is a initial delay of 100 us and then another for 50 us. If the first first vector comes in at 150 us. then say (n – 1 \* 50 us) + 150 us = total time needed for all test cases to be run.
5. (20 pts) Based your understanding of the video, how should we do hardware debugging? Make a clear summary.
   1. Based on what I have observed through this last the way we should do hardware debugging is to first check the type of variables and bit sizes for each variable. Make sure they match after each operation and reassignment. Next make sure that the output is also properly mentioned in your code and not accidently renamed something else. Once these boxes are check we can go and run our synthesis tool to check for an errors. If none how then we can run a behavioral simulation to check the different waveforms and how they are acting based on the inputs and outputs. If there are any problems that arise here make sure to go back and check your operation to make sure they are setup up properly to ensure the correct output.
   2. Hardware debugging should be done at the lowest level first to make sure the proper signed or unsigned variables are set as well as their big sizes. Once done the other tools give can help catch the not so obvious errors like miss ordered operation blocks.