ECE260B Lab1

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Assignment1:

Increase the load from four INVX4 inverters to six INVX4 inverters. Report the rise and fall delays, What changes can be made to reduce these delays:

From the above form, we can know the rise and fall delay is 2.426e-11 and 1.290e-11

The way to reduce these delays is increase inverter width until the width reach invx32.

 (1) Plot rise and fall delays (y-axis) vs. different sizes of inverters (x-axis).

Invx2: rise delay: 1.651e-11 fall delay 9.659e-12

Invx4 Rise delay: 2.426e-11   fall_delay: 1.290e-11

Invx8: Rise delay: 1.352e-11   fall_delay: 8.101e-12
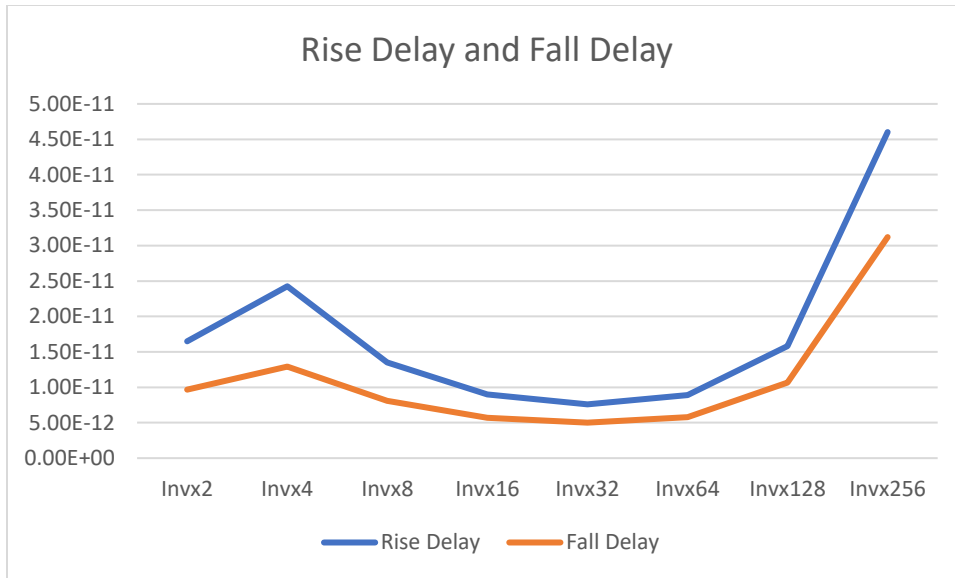
Invx16: Rise delay: 8.994e-12   fall_delay: 5.715e-12

Invx32: Rise delay: 7.590e-12   fall_delay: 5.010e-12

Invx64: Rise delay: 8.905e-12   fall_delay: 5.785e-12

Invx128: Rise delay:1.581e-11   fall_delay: 1.067e-11

Invx256: Rise delay: 4.602e-11   fall_delay: 3.120e-11

	Invx2	Invx4	Invx8	Invx16	Invx32	Invx64	Invx128	Invx256
Rise Delay	1.65E-11	2.426E-11	1.352E-11	8.994E-12	7.590E-12	8.905E-12	1.581E-11	4.602E-11
Fall Delay	9.659e-12	1.290e-11	8.101e-12	5.715e-12	5.010e-12	5.785e-12	1.067e-11	3.120e-11

Rise Delay and Fall Delay

(2) Plot rise and fall slews (at the output pin of inverter) vs. different sizes of inverters.

The inverter rise slew and fall slew shows as this:

	Invx2	Invx4	Invx8	Invx16	Invx32	Invx64	Invx128	Invx256
Rise slew	5.326e-11	2.809e-11	1.491e-11	7.302e-12	4.505e-12	4.289e-12	6.454e-12	1.593e-11
Fall slew	2.765e-11	1.194e-11	5.827e-12	3.436e-12	2.583e-12	2.623e-12	5.035e-12	1.726e-11

Rising and Falling slew
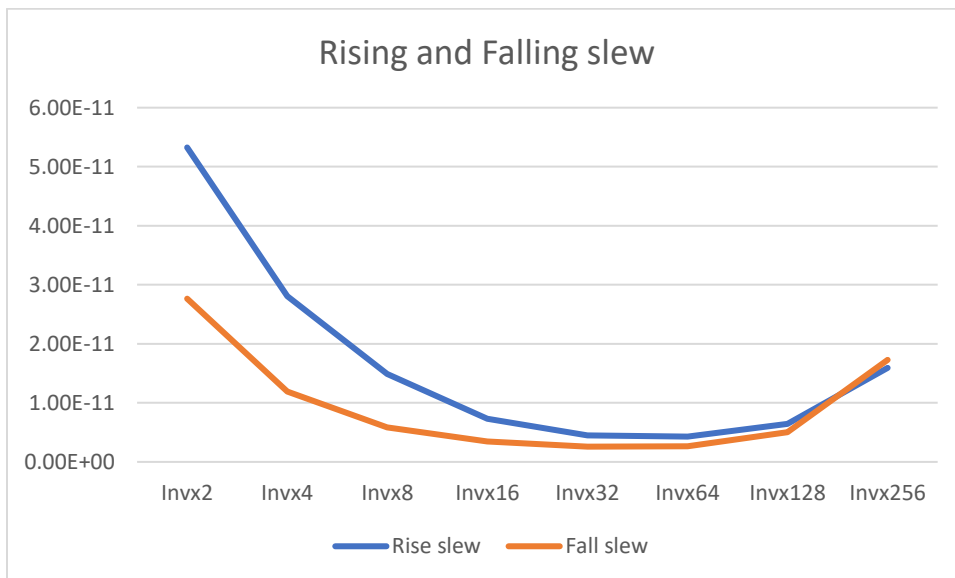
(3) Report the inverter size that achieves the minimum rise and fall delays.
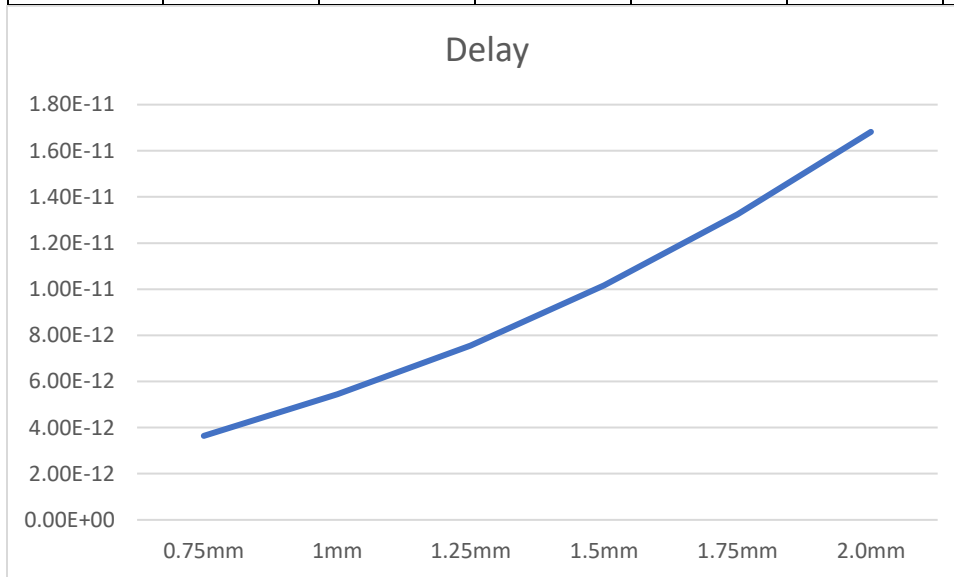
From the form above, we can know 32 width inverter achieves the minimum rise and fall delays

Assignment 2:

(1) Repeat the experiment from interconnect lengths of 1.25mm, 1.5mm, 1.75mm and 2.0mm. Plot delay (Y-axis) vs. interconnect length (X-axis) in your report.

The delay change as the length increase like this:

Length	0.75mm	1mm	1.25mm	1.5mm	1.75mm	2.0mm
Delay	3.642e-12	5.441e-12	7.553e-12	1.016e-11	1.324e-11	1.682e-11

Delay

Y-axis values
1.80E-11
1.60E-11
1.40E-11
1.20E-11
1.00E-11
8.00E-12
6.00E-12
4.00E-12
2.00E-12
0.00E+00

X-axis: 0.75mm 1mm 1.25mm 1.5mm 1.75mm 2.0mm

(2) Repeat the experiment by assuming a 250um interconnect segment to have resistance of 2.0 ohms and capacitance of 61.5 femto farads (fF) with interconnect length of 1mm. Report the wire delay.

After we change the resistance, with the interconnect length of 1mm, the wire delay is 1.321e-12

Assignment3:

How many inverters, and of what sizes (from X4, X8, X16, X32) are required to achieve the required delay with minimum power?

Based on the experiment, we found we need to insert two inverter to achieve the required delay, and the position of inverter have some matter. So we test 7 data to find the minimum power.
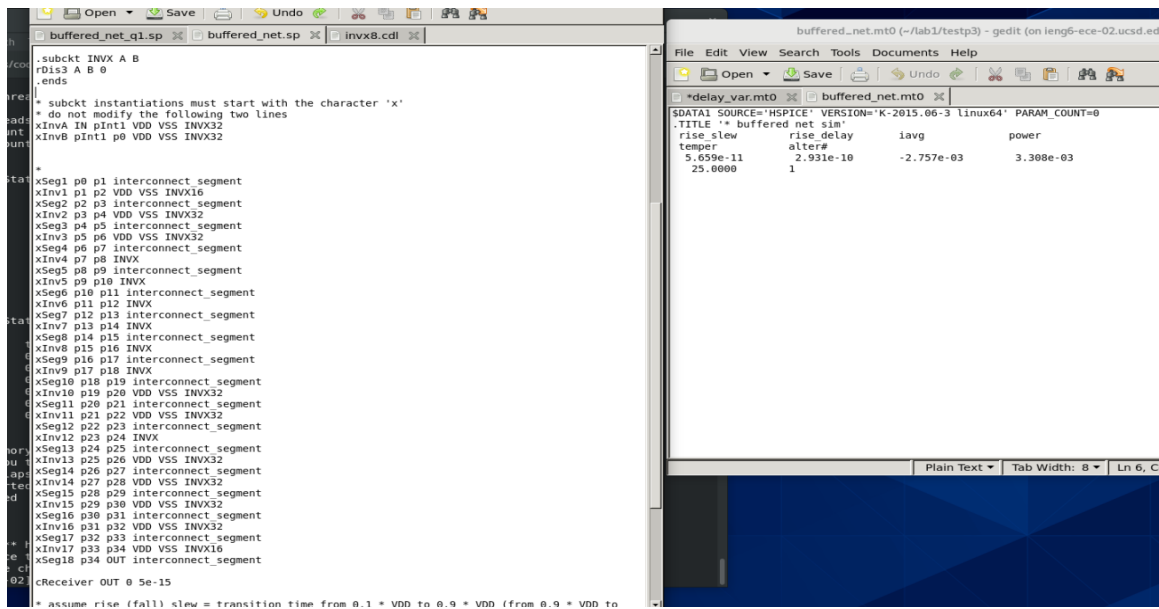
	Delete inv1 and inv2	Delete inv1 and inv3	Delete inv1 and inv4	Delete inv2 and inv3	Delete inv2 and inv4	Delete inv3 and inv4	Delete inv1 and inv4 and change the width of inverter from 32 to 16
Rise slew	2.672e-11	2.885e-11	4.244e-11	3.227e-11	4.5e-11	6.172e-11	4.469e-11
Rise Delay	5.057e-11	5.037e-11	4.936e-11	5.244e-11	5.5157e-11	5.128e-11	5.720e-11
power	3.754e-03	3.064e-03	3.686e-03	2.407e-03	3.004e-03	3.587e-03	2.180e-03

From the above form, we can find when delete inv1 and inv4 and change the width of inverter from 32 to 16, the power is minimum and meet the demand.

Repeat the experiment with interconnect length of 9mm and the required delay of **350ps**, and with the same slew time constraints as above. This time, assume that a 250um interconnect segment is used instead of 500um, and each has resistance of 2.0 ohms and capacitance of 61.5 femto farads (fF).

We try many design, and finally find insert 10 inverter which consist of 2 inv16 and 8 inv32 which can get the minimum power, and meet the demand;

The script shows as follow:

buffered_net_q1.sp ✕   **buffered_net.sp** ✕   **invx8.cdl** ✕

```
.subckt INVX A B
rDis3 A B 0
.ends

* subckt instantiations must start with the character 'x'
* do not modify the following two lines
xInvA IN pInt1 VDD VSS INVX32
xInvB pInt1 p0 VDD VSS INVX32

*
xSeg1 p0 p1 interconnect_segment
xInv1 p1 p2 VDD VSS INVX16
xSeg2 p2 p3 interconnect_segment
xInv2 p3 p4 VDD VSS INVX32
xSeg3 p4 p5 interconnect_segment
xInv3 p5 p6 VDD VSS INVX32
xSeg4 p6 p7 interconnect_segment
xInv4 p7 p8 INVX
xSeg5 p8 p9 interconnect_segment
xInv5 p9 p10 INVX
xSeg6 p10 p11 interconnect_segment
xInv6 p11 p12 INVX
xSeg7 p12 p13 interconnect_segment
xInv7 p13 p14 INVX
xSeg8 p14 p15 interconnect_segment
xInv8 p15 p16 INVX
xSeg9 p16 p17 interconnect_segment
xInv9 p17 p18 INVX
xSeg10 p18 p19 interconnect_segment
xInv10 p19 p20 VDD VSS INVX32
xSeg11 p20 p21 interconnect_segment
xInv11 p21 p22 VDD VSS INVX32
xSeg12 p22 p23 interconnect_segment
xInv12 p23 p24 INVX
xSeg13 p24 p25 interconnect_segment
xInv13 p25 p26 VDD VSS INVX32
xSeg14 p26 p27 interconnect_segment
xInv14 p27 p28 VDD VSS INVX32
xSeg15 p28 p29 interconnect_segment
xInv15 p29 p30 VDD VSS INVX32
xSeg16 p30 p31 interconnect_segment
xInv16 p31 p32 VDD VSS INVX32
xSeg17 p32 p33 interconnect_segment
xInv17 p33 p34 VDD VSS INVX16
xSeg18 p34 OUT interconnect_segment

cReceiver OUT 0 5e-15

* assume rise (fall) slew = transition time from 0.1 * VDD to 0.9 * VDD (from 0.9 * VDD to
```

*delay_var.mt0 ✕   **buffered_net.mt0** ✕

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-3 linux64' PARAM_COUNT=0
.TITLE '* buffered net sim'
rise_slew        rise_delay       iavg             power
temper           alter#
5.659e-11        2.931e-10        -2.757e-03       3.308e-03
 25.0000         1
```

From the picture, the minimum power is 3.308e-03;（the reason why we use the 18 interconnect segmentation is because we simplify the whole process. We don't insert the inverter inside it）

Assignment 4

Inverter	Parameter	Gate_delay	wire_delay	Gate_delay Scale factor	wire_delay Scale factor
inv4	slow corner: 0.8V, 125C	1.09E-10	6.50E-12		
inv4	fast corner: 1.4V, -30C	5.01E-11	6.20E-12	2.167832168	1.047580645
inv16	slow corner: 0.8V, 125C	2.85E-11	6.83E-12		
inv16	fast corner: 1.4V, -30C	1.14E-11	6.46E-12	2.493881119	1.057240099

1. Which of gate delay or wire delay, scales by a larger factor across corners?

- From the figure, we can see that **INVX16** of **gate delay and wire delay** scales by a larger factor across corners.

2. How does the variation of gate delay across corners change with the size of the inverter?

- The gate delay decreases with the size of the inverter increases.

3. Why is it required to use both corners for a design?

- Both corners can swap between different delays so that it can fit a better timing requirement or achieve a better working frequency.

Screenshots:

{slow corner: 0.8V, 125C} inv4


```
delay_var.sp        *delay_var.mt0        invx4.cdl        buffe

#0.8 125C INVX4

$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-3 linux64' PARAM_COUNT=0
.TITLE '* buffered net sim'
 gate_delay        wire_delay        temper        alter#
  1.085e-10         6.495e-12         125.0000      1
```

{fast corner: 1.4V, -30C} inv4

| delay_var.sp | *delay_var.mt0 | invx4.cdl | buffer |

```
#1.4V -30C INVX4


$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-3 linux64' PARAM_COUNT=0
.TITLE '* buffered net sim'
 gate_delay        wire_delay         temper             alter#
  5.005e-11         6.200e-12         -30.0000           1
```