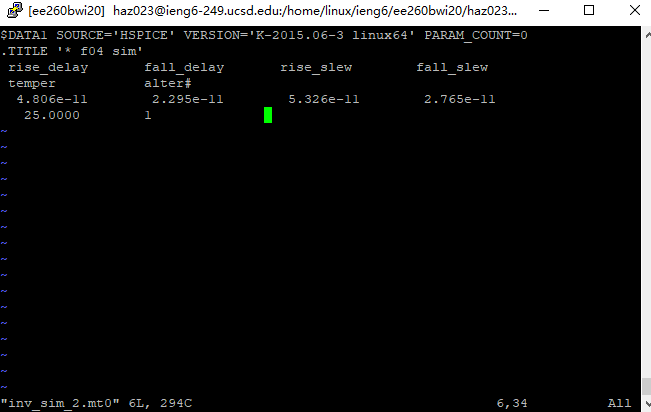
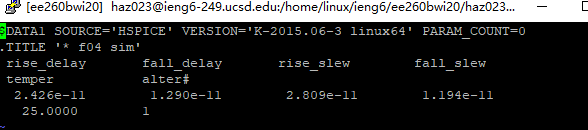
Assignment1:

1. Increase the load from four INVX4 inverters to six INVX4 inverters. Report the rise and fall delays:

Invx2: rise delay: 1.651e-11 fall delay 9.659e-12, rise\_slew: 5.326e-11, fall\_slew: 2.765e-11

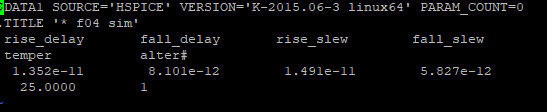


Invx4 Rise delay: 2.426e-11 fall\_delay: 1.290e-11 rise\_slew: 2.809e-11, fall\_slew: 1.194e-11

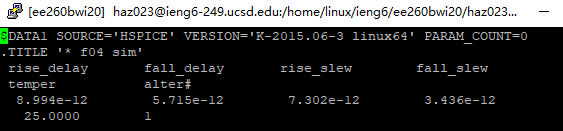


1. What changes can be made to reduce these delays:

Invx8: Rise delay: 1.352e-11 fall\_delay: 8.101e-12 rise\_slew: 1.491e-11 fall\_slew: 5.827e-12

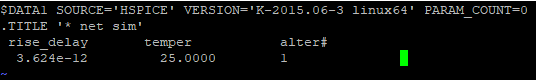


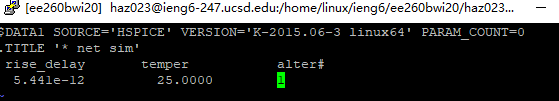
Invx16:

Invx16: Rise delay: 8.994e-12 fall\_delay: 5.715e-12, rise\_slew: 7.302e-12, fall\_slew: 3.436e-12

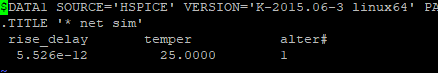
Assignment2:  
(1) Repeat the experiment from interconnect lengths of 1.25mm, 1.5mm, 1.75mm and 2.0mm. Plot delay (Y-axis) vs. interconnect length (X-axis) in your report.

0.75mm: rise\_delay: 3.642e-12 avg:1.21



1mm: rise\_delay: 5.441e-12 avg: 1.36

1.25mm: rise\_delay 5.526e-12 avg: 1.1

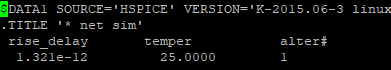


1.5mm:

1.75mm:

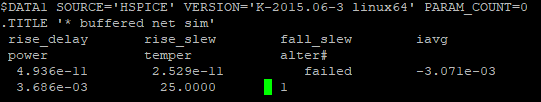
2.0mm:

 (2) Repeat the experiment by assuming a 250um interconnect segment to have resistance of 2.0 ohms and capacitance of 61.5 femto farads (fF) with interconnect length of 1mm.   Report the wire delay.



Assignment3:

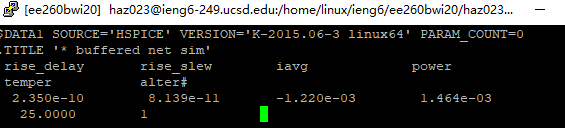
Cut off inv1 inv4, then change inv4 to inverter32:



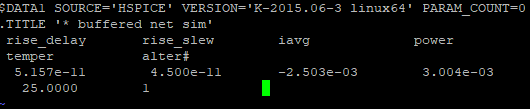
Cut off inv1

1. Requirement: Note that the delay of the buffered interconnect **must** be no larger than **60ps 6\*e-11**
2. you have limited inverter size options. You can freely choose from INVX4, INVX8, INVX16 or INVX32, (2) even number of inverters are inserted,
3. the slew time at input/output pins of each inverter (excluding drivers) as well as the slew time at the end of the interconnect **must** be no larger than **60ps**.

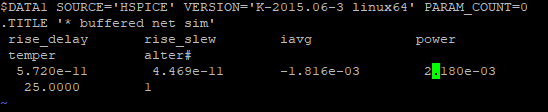
Original value:



Cut off inv2 inv4



Cut off inv2 inv3 and put the inv4 width from 32 to 16;



If the width increase, the power will increase and the delay will decrease before the width of 32

Repeat the experiment with interconnect length of 9mm and the required delay **of 350ps**, and with the same slew time constraints as above. This time, assume that a 250um interconnect segment is used instead of 500um, and each has resistance of **2.0 ohms and capacitance of 61.5 femto farads (fF).** Again, you can either insert an inverter between any two consecutive interconnect segments or not. Note that the window for power measurement should be changed from **150ps to 500ps** (use Line 50 instead of Line 48).

If plus the inverter, the delay increase, power decrease, and the slew decrease

Where there is a inverter If the width increase , the power increase, but the delay decrease

If the width decrease, the power decrease, the delay increase ,

Now the delay meet the demand, so we add more inverter32,

Assignment4:

The goal of this assignment is to study the **impact of voltage and temperature** variation on gate and wire delay for different inverter sizes. Please report the gate and wire delay at two extreme corners, i.e., {slow corner: 0.8V, 125C} and {fast corner: 1.4V, -30C} (You will need to change the temperature and voltage values in the spice file to define the corners). The length of wire shall stay fixed (i.e., 1mm). The delays should be reported for two different inverter sizes (i.e., INVX4 and INVX16). From the simulation results, answer the following.