### ECE260B Lab1

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# Assignment1:

Increase the load from four INVX4 inverters to six INVX4 inverters. Report the rise and fall delays, What changes can be made to reduce these delays:

From the above form, we can know the rise and fall delay is 2.426e-11  and 1.290e-11

The way to reduce these delays is increase inverter width until the width reach invx32.

1. Plot rise and fall delays (y-axis) vs. different sizes of inverters (x-axis).

Invx2: rise delay: 1.651e-11 fall delay 9.659e-12

Invx4 Rise delay: 2.426e-11   fall\_delay: 1.290e-11

Invx8: Rise delay: 1.352e-11   fall\_delay: 8.101e-12

Invx16: Rise delay: 8.994e-12   fall\_delay: 5.715e-12

Invx32: Rise delay: 7.590e-12   fall\_delay: 5.010e-12

Invx64: Rise delay: 8.905e-12   fall\_delay: 5.785e-12

Invx128: Rise delay:1.581e-11   fall\_delay: 1.067e-11

Invx256: Rise delay: 4.602e-11   fall\_delay: 3.120e-11

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Invx2 | Invx4 | Invx8 | Invx16 | Invx32 | Invx64 | Invx128 | Invx256 |
| Rise Delay | 1.65E-11 | 2.426E-11 | 1.352E-11 | 8.994E-12 | 7.590E-12 | 8.905E-12 | 1.581E-11 | 4.602E-11 |
| Fall Delay | 9.659e-12 | 1.290e-11 | 8.101e-12 | 5.715e-12 | 5.010e-12 | 5.785e-12 | 1.067e-11 | 3.120e-11 |

1. Plot rise and fall slews (at the output pin of inverter) vs. different sizes of inverters.

The inverter rise slew and fall slew shows as this:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Invx2 | Invx4 | Invx8 | Invx16 | Invx32 | Invx64 | Invx128 | Invx256 |
| Rise slew | 5.326e-11 | 2.809e-11 | 1.491e-11 | 7.302e-12 | 4.505e-12 | 4.289e-12 | 6.454e-12 | 1.593e-11 |
| Fall slew | 2.765e-11 | 1.194e-11 | 5.827e-12 | 3.436e-12 | 2.583e-12 | 2.623e-12 | 5.035e-12 | 1.726e-11 |

(3) Report the inverter size that achieves the minimum rise and fall delays.

From the form above, we can know 32 width inverter achieves the minimum rise and fall delays

# Assignment 2:

1. Repeat the experiment from interconnect lengths of 1.25mm, 1.5mm, 1.75mm and 2.0mm. Plot delay (Y-axis) vs. interconnect length (X-axis) in your report.

The delay change as the length increase like this:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Length | 0.75mm | 1mm | 1.25mm | 1.5mm | 1.75mm | 2.0mm |
| Delay | 3.642e-12 | 5.441e-12 | 7.553e-12 | 1.016e-11 | 1.324e-11 | 1.682e-11 |

1. Repeat the experiment by assuming a 250um interconnect segment to have resistance of 2.0 ohms and capacitance of 61.5 femto farads (fF) with interconnect length of 1mm. Report the wire delay.

After we change the resistance, with the interconnect length of 1mm, the wire delay is 1.321e-12

# Assignment3:

How many inverters, and of what sizes (from X4, X8, X16, X32) are required to achieve the required delay with minimum power?

Based on the experiment, we found we need to insert two inverter to achieve the required delay, and the position of inverter have some matter. So we test 7 data to find the minimum power.

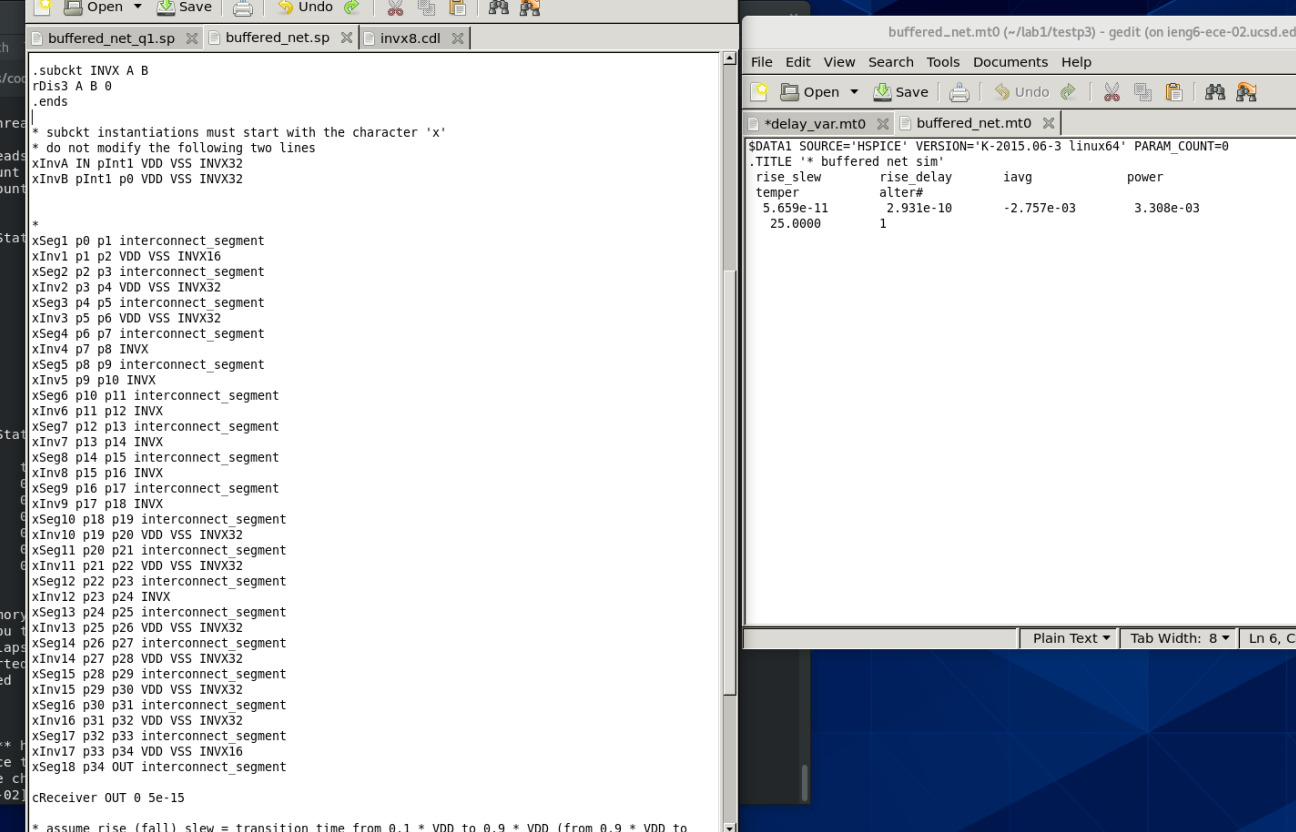
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | Delete inv1 and inv2 | Delete inv1 and inv3 | Delete inv1 and inv4 | Delete inv2 and inv3 | Delete inv2 and inv4 | Delete inv3 and inv4 | Delete inv1 and inv4 and change the width of inverter from 32 to 16 |
| Rise slew | 2.672e-11 | 2.885e-11 | 4.244e-11 | 3.227e-11 | 4.5e-11 | 6.172e-11 | 4.469e-11 |
| Rise Delay | 5.057e-11 | 5.037e-11 | 4.936e-11 | 5.244e-11 | 5.5157e-11 | 5.128e-11 | 5.720e-11 |
| power | 3.754e-03 | 3.064e-03 | 3.686e-03 | 2.407e-03 | 3.004e-03 | 3.587e-03 | 2.180e-03 |

From the above form, we can find when delete inv1 and inv4 and change the width of inverter from 32 to 16, the power is minimum and meet the demand.

Repeat the experiment with interconnect length of 9mm and the required delay of **350ps**, and with the same slew time constraints as above. This time, assume that a 250um interconnect segment is used instead of 500um, and each has resistance of 2.0 ohms and capacitance of 61.5 femto farads (fF).

We try many design, and finally find insert 10 inverter which consist of 2 inv16 and 8 inv32 which can get the minimum power, and meet the demand;

The script shows as follow:



From the picture, the minimum power is 3.308e-03;（the reason why we use the 18 interconnect segmentation is because we simplify the whole process. We don’t insert the inverter inside it）

# Assignment 4

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Inverter** | **Parameter** | **Gate\_delay** | **wire\_delay** | **Gate\_delay Scale factor** | **wire\_delay Scale factor** |
| inv4 | slow corner: 0.8V, 125C | 1.09E-10 | 6.50E-12 | 2.167832168 | 1.047580645 |
| inv4 | fast corner: 1.4V, -30C | 5.01E-11 | 6.20E-12 |
| inv16 | slow corner: 0.8V, 125C | 2.85E-11 | 6.83E-12 | 2.493881119 | 1.057240099 |
| inv16 | fast corner: 1.4V, -30C | 1.14E-11 | 6.46E-12 |

1. Which of gate delay or wire delay, scales by a larger factor across corners?

* From the figure, we can see that **INVX16** of **gate delay and wire delay** scales by a larger factor across corners.

2. How does the variation of gate delay across corners change with the size of the inverter?

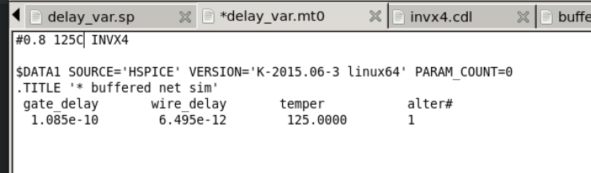
* The gate delay decreases with the size of the inverter increases.

3. Why is it required to use both corners for a design?

* Both corners can swap between different delays so that it can fit a better timing requirement or achieve a better working frequency.

Screenshots:

  {slow corner: 0.8V, 125C}  inv4



{fast corner: 1.4V, -30C}  inv4

