## Liberty Files

- Definition
- Format
- Header, Cell Level, Pin Level
- Cell Rise/Fall
- Rise/Fall Transition

### What are Liberty Files?

#### **Library Header**

```
* Generated by Liberty NCX vD-2010.06-SP2 on Tue Feb 11 15:51:07 2014
library ("scs8hd_ss_1.60v_-40C")
        define(switching_power_split_model,library,string);
       define(driver_model,library,string);
       define(leakage sim opt,library,string);
       define(default constraint arc mode, library, string);
       define(min pulse width mode, library, string);
       define(default arc mode, library, string);
       define(def_sim_opt,library,string);
       define(simulator, library, string);
       define(violation_delay_degrade_pct,timing,string);
        define(sim opt,timing,string);
        technology("cmos");
       delay model : "table lookup";
       bus naming style : "%s[%d]";
        in_place_swap_mode : "match_footprint";
        library features("report delay calculation");
        switching_power_split_model : "true";
        simulation : true;
        revision: "1.0000000";
        driver model : "ramp";
       leakage sim opt : "runlvl=5 accurate=1 method=bdf kcltest=1 gmin=1E-15
1 gmin=1E-15 runlvl=5 accurate=1 method=bdf kcltest=1 gmin=1E-15";
       input threshold pct rise : 50.000000;
       input_threshold_pct_fall : 50.000000;
       output threshold pct rise : 50.000000;
       output_threshold_pct_fall : 50.000000;
        slew lower threshold pct fall : 20.000000;
                                                          area: 3.753600;
        slew lower threshold pct rise : 20.000000;
        slew_upper_threshold_pct_fall : 80.000000;
        slew upper threshold pct rise : 80.000000;
        slew_derate_from_library : 1.000000;
```

time\_unit : "lns";
voltage\_unit : "1V";
current unit : "lmA";

"pf");

[iptguser@beazly PVT]\$

leakage\_power\_unit : "lnW";

pulling\_resistance\_unit : "lkohm";
capacitive load unit(1.000000, \

#### **Cell Level Data**

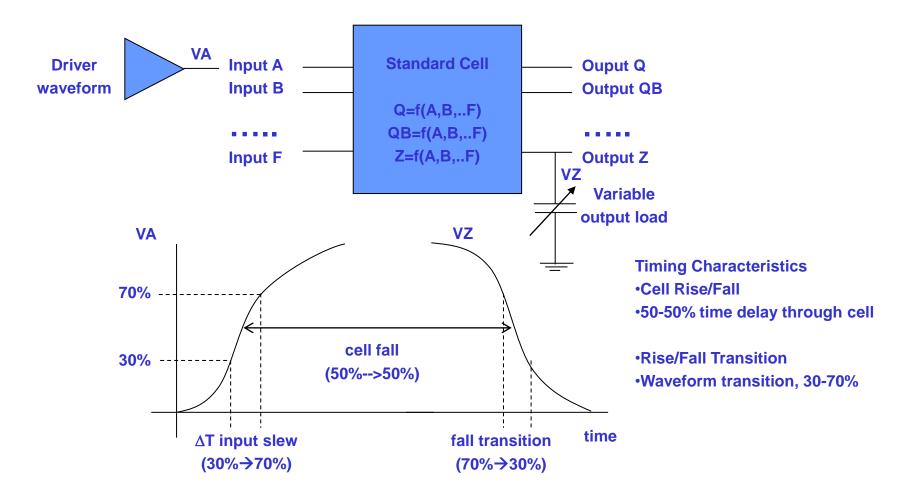
```
cell ("scs8hd inv 1") {
  cell footprint : "inv";
 cell_leakage_power : 2.706431e-04;
 driver waveform rise : "ramp";
  driver waveform fall : "ramp";
  pg pin (vpwr) {
     voltage_name : "vpwr";
    pg_type : "primary_power";
  pg_pin (vnb) {
    pg_type : "primary_ground";
    voltage name : "vnb";
  pg_pin (vpb) {
    pg_type : "primary_power";
    voltage name : "vpb";
 pg_pin (vgnd) {
  voltage_name : "vgnd";
    pg_type : "primary_ground";
  leakage_power () {
  value : "0.0005316";
  when : "A";
  leakage_power () {
  value : "9.6979784e-06";
  when : "!A";
```

#### **O** Definition

Liberty Files are a IEEE Standard for defining:

- PVT Characterization
- Relating Input and Output Characteristics
- Timing
- Power
- Noise

#### **Pin Level Data**



```
timing () {
                                        index_1: Input Waveform Rise Time (ns) (20-80%)
  related pin : "A";
                                        index 2: Output Load (pF)
  timing type : "combinational";
                                        cell rise values: delay 50%-50% (ns)
  timing sense : "negative unate";
  cell rise ("del 1 7 7") {
                                        rise transition values: Output Waveform Rise Time (ns) (20-80%)
    index 1("0.01, 0.0230506, 0.0531329, 0.122474, 0.282311, 0.650743, 1.5");
    index 2("0.0005, 0.0011915, 0.00283935, 0.00676619, 0.0161239, 0.0384232, 0.0915627");
    values("0.0393913, 0.0481351, 0.0682676, 0.1148176, 0.2261336, 0.4902760, 1.1271604", \
      "0.0455350, 0.0543177, 0.0745882, 0.1219566, 0.2321275, 0.4960252, 1.1251990", \setminus
      "0.0615748, 0.0702546, 0.0903614, 0.1380518, 0.2464881, 0.5123485, 1.1380734", \setminus
      "0.0999742, 0.1085959, 0.1287553, 0.1756036, 0.2859632, 0.5432616, 1.1732209", \
      "0.1745766, 0.1895887, 0.2170584, 0.2652452, 0.3755799, 0.6386030, 1.2626264", \setminus
      "0.3101955, 0.3368956, 0.3853594, 0.4625098, 0.5830301, 0.8453408, 1.4683126", \
      "0.5617597. 0.6087236. 0.6936649. 0.8289562. 1.0322970. 1.3284999. 1.9485167"):
  rise transition ("del 1 7 7") {
    index 1("0.01, 0.0230506, 0.0531329, 0.122474, 0.282311, 0.650743, 1.5");
    index 2("0.0005, 0.0011915, 0.00283935, 0.00676619, 0.0161239, 0.0384232, 0.0915627");
    values("0.0291454, 0.0406597, 0.0668243, 0.1304383, 0.2795841, 0.6384314, 1.5091380", \
      "0.0292797, 0.0406510, 0.0676452, 0.1294254, 0.2814416, 0.6369616, 1.4898204", \setminus
      "0.0293842, 0.0405772, 0.0673192, 0.1318008, 0.2833689, 0.6380833, 1.5070226", \setminus
      "0.0353473, 0.0441388, 0.0677661, 0.1305581, 0.2815879, 0.6418293, 1.5074368", \setminus
      "0.0603860, 0.0698299, 0.0871389, 0.1366998, 0.2825138, 0.6362187, 1.5013318", \setminus
      "0.1081614, 0.1228129, 0.1486038, 0.1952778, 0.3050307, 0.6431969, 1.4902587", \setminus
      "0.2026567, 0.2243255, 0.2683267, 0.3357463, 0.4515043, 0.6980425, 1.4977894");
```

# Liberty File Structure Library Header

- O Library name and delay models.
  - Table lookup is most predominate method. Hence massive number of matrices.
- Nom\_process FF, SS, FS, SF, TT
- Nom\_temperature Simulation Temperature
- O Nom\_voltage Simulation Voltage Reference
- Slew and Delay Threshold Points
  - Low Slew 10-20%
  - High Slew 80-90%
  - Threshold 50%
- O Sets Units (Voltage, Time, Current, Cap.)

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# Liberty File Structure Cell Header

- O Cell Name
- **O** Area
  - Cell Area without units
- Cell Leakage Power
- O Cell Footprint
  - Type of Cell (Shorthand)
    - Combinational (NAND, NOR, etc.)
    - Sequential (Flops)

# Liberty File Structure Pin Header

- O Direction Input, output, inout, internal
- O Clock Pin
- O Function
- O Max Capacitance Max output capacitance the output pin can drive.
- O Capacitance Input load capacitance
- Sequential Cells Flops
  - Clocked on
  - Next state
  - Clear
  - Preset

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# Liberty File Structure Pin Paramters

### O Internal Power

 Output pins in combinational cells define rise\_power and fall\_power to related input pin. Input and clock pins also define this in sequential cells.

## **O** Timing

- Output pins in combinational cells define: rise\_delay, fall\_delay, rise\_transition, and fall\_transition.
- Output pins in sequential cells define: rise\_constraint, fall\_constraint (Setup and Hold)

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