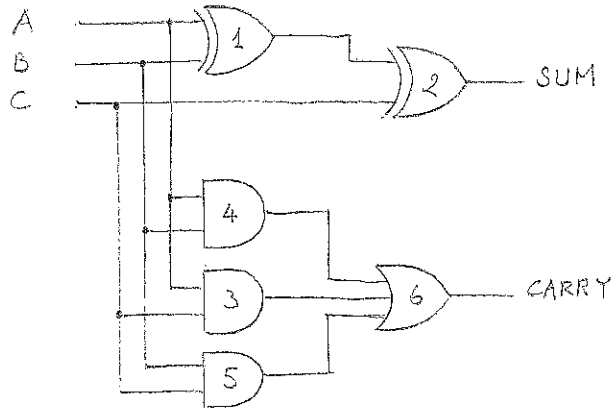
```
//*****************************************************************//
//      LCSIM.CPP                                                  //
//      Project #4  :   "Zero-Delay Combinational Logic Simulator" //
//      Student     :   Joseph D. Tran                             //
//      Class       :   ECE 299 - C++ for electrical engineers     //
//      Instructor  :   Dr. Chandra                                //
//      Date due    :   Dec 1, 1993                                //
//*****************************************************************//

/*     This logic simulator reads a combinational logic description file
   (LDF), lists the circuit in ascending gate number, and generates the
   truth table for user-selected outputs.  It has the following features:
   1.  The number of primary inputs is limited to 26
       (single character, usu. A to Z).
   2.  The number of user-selected outputs is limited to 26.
   3.  Fan-in for each gate is 8.
   4.  The following gate types are supported by LCSIM.CPP:
           { NOT,AND,OR,XOR,NAND,NOR,XNOR }
   5.  The gate count in each circuit is limited to 50.
   6.  Each line of the LDF should have the following format:
       <GATE_NUMBER> <NAME> <TYPE> <INP1> [<INP2> ... <INP8>] \n
   7.  The gate numbers should be contiguous, beginning with 1.
   8.  The simulator is invoked with command line argument(s):
       a) Output to the screen
          --------------------
          Usage:  lcsim <filename.in>
       b) Output to a disk file
          ---------------------
          Usage:  lcsim <filename.in> <filename.out>
       Note that the circuit listing is performed on the screen regardless
   of screen/disk operation, thus enabling the user to pick the outputs to
   be monitored.
*/

#include <iostream.h>
#include <fstream.h>
#include <string.h>
#include <ctype.h>
#include <stdlib.h>
#include <conio.h>
#include <math.h>

// Declaration of constants
const int MAXGATES = 50;                // max # of gates in a circuit
const int MAXPIO   = 26;                // max # of prime inputs or outputs
const int MAXNAME  = 12;                // max length for gate names
const int MAXTYPE  =  5;                // max length for gate types
const int MAXINP   =  8;                // fan-in for each gate
const int TRUE     =  1;
const int FALSE    =  0;

int cmpblock(const void *xptr, const void *yptr);

// Basic gate information
struct lgate {
  int block;
  char name[MAXNAME];
  char type[MAXTYPE];
  int ninp;
  int inp[MAXINP];
```

File Edit Search Options Help

FADDER1.IN

```
6       carry   OR      3       4       5
1       xor1    XOR     A       B
3       and2    AnD     A       C
4       AND1    AND     A       B
5       AND3    AND     B       C
2       sum     xor     1       c
```



MS-DOS Editor <F1=Help> Press ALT to activate menus | N 00001:025

Welcome to the Zero-delay Logic Simulator:

rcuit Listing

1	XOR1	XOR	A	B
2	SUM	XOR	1	C
3	AND2	AND	A	C
4	AND1	AND	A	B
5	AND3	AND	B	C
6	CARRY	OR	3	4 5

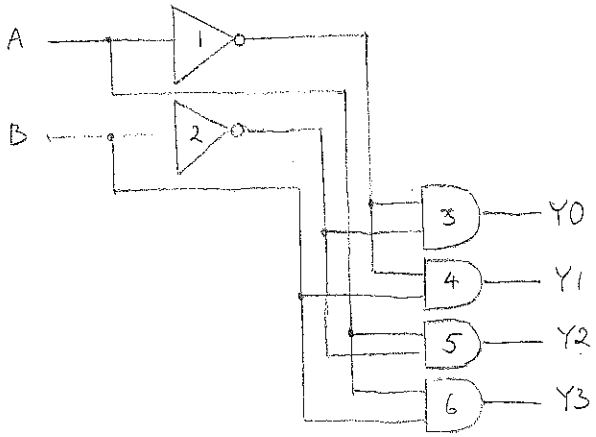
Truth Table for the Selected Outputs

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

File Edit Search Options Help

DEC2TO4.IN

```
3       Y0      and     1 2
4       Y1      and     1 b
5       Y2      and     2 a
6       Y3      and     A B
1       nota    not     A
2       notb    not     b
```



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File Edit Search Options Help

DEC2TO4.OUT

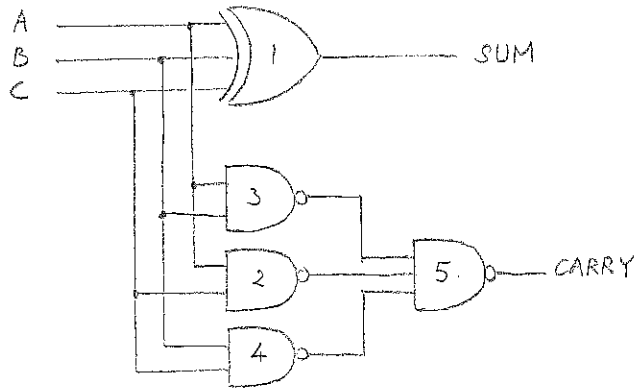
```
elcome to the Zero-delay Logic Simulator:
==========================================

Circuit Listing
---------------
1       NOTA    NOT     A
2       NOTB    NOT     B
3       Y0      AND     1 2
4       Y1      AND     1 B
5       Y2      AND     2 A
6       Y3      AND     A B

Truth Table for the Selected Outputs
------------------------------------
A       B       Y0      Y1      Y2      Y3

0       0       1       0       0       0
0       1       0       1       0       0
1       0       0       0       1       0
1       1       0       0       0       1
```

MS-DOS Editor <F1=Help> Press ALT to activate menus | N 00001:001

File Edit Search Options Help

FADDER2.IN

```
5       carry    nand    3 4 2
        sum      XOR     A B C
2       nand2    nAnD    A C
3       nAND1    nAND    A B
4       nAND3    nAND    B C
```



MS-DOS Editor <F1=Help> Press ALT to activate menus | N 00005:026

Welcome to the Zero-delay Logic Simulator:

rcuit Listing

1	SUM	XOR	A B C
2	NAND2	NAND	A C
3	NAND1	NAND	A B
4	NAND3	NAND	B C
5	CARRY	NAND	3 4 2

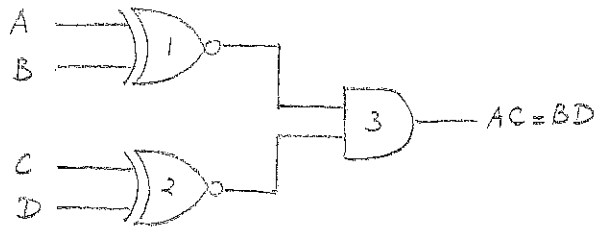
Truth Table for the Selected Outputs

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

File Edit Search Options Help

COMP2.IN

```
         xnor1    xnor     a        b
         xnor2    xnor     c        d
3        ac=bd    and      1        2
```



MS-DOS Editor <F1=Help> Press ALT to activate menus N 00001:001

Welcome to the Zero-delay Logic Simulator:

rcuit Listing

```
1        XNOR1    XNOR     A B
2        XNOR2    XNOR     C D
3        AC=BD    AND      1 2
```

Truth Table for the Selected Outputs

A	B	C	D	AC=BD
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

File Edit Search Options Help

MUX4TO1.IN

```
-        Y0      AND     C       1       2
         y1      and     d       1       b
5        y2      and     e       2       a
6        y3      and     a       b       f
1        nota    not     a
2        notb    NOT     B
7        MUX     OR      3       4       5       6
```

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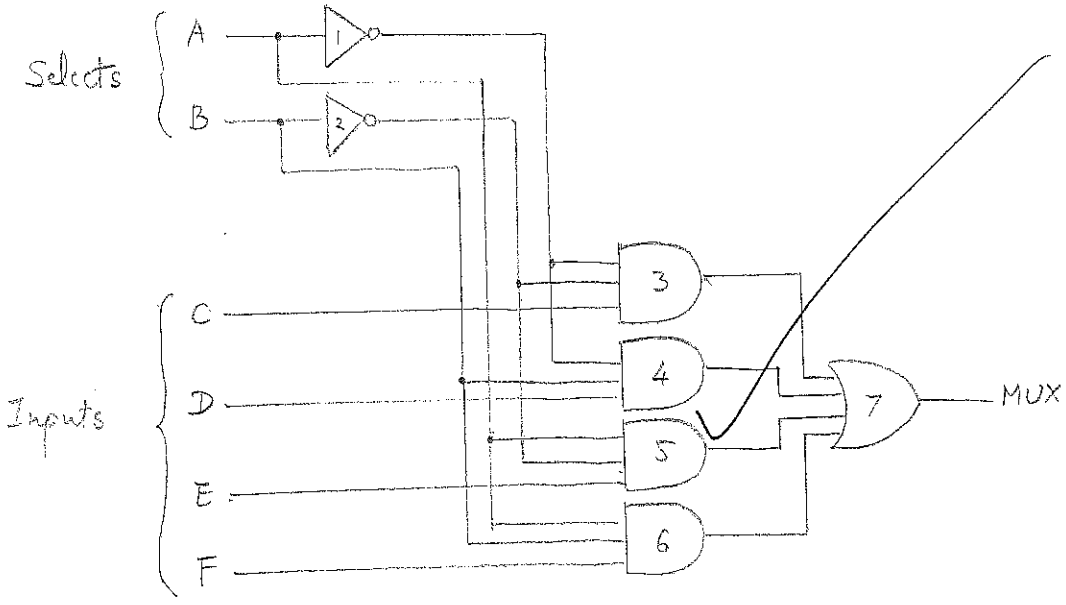

Welcome to the Zero-delay Logic Simulator:

Circuit Listing

1	NOTA	NOT	A
2	NOTB	NOT	B
3	Y0	AND	C 1 2
4	Y1	AND	D 1 B
5	Y2	AND	E 2 A
6	Y3	AND	A B F
7	MUX	OR	3 4 5 6

Truth Table for the Selected Outputs

A	B	C	D	E	F	MUX
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	0
0	0	1	0	0	0	1
0	0	1	0	0	1	1
0	0	1	0	1	0	1
0	0	1	0	1	1	1
	0	1	1	0	0	1
0	0	1	1	0	1	1
0	0	1	1	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	0
0	1	0	0	1	1	0
0	1	0	1	0	0	1
0	1	0	1	0	1	1
0	1	0	1	1	0	1
0	1	0	1	1	1	1
0	1	1	0	0	0	0
0	1	1	0	0	1	0
0	1	1	0	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	1
0	1	1	1	0	1	1
0	1	1	1	1	0	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	0	0	1	0
1	0	0	0	1	0	1
1	0	0	0	1	1	1
1	0	0	1	0	0	0
	0	0	1	0	1	0
	0	0	1	1	0	1
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	0	1	0	0	1	0
1	0	1	0	1	0	1