Test Outline

Hit/Miss Tests

- Read from address 0, result should be miss, bus op
- Read from address 1, result should be miss, bus op
- Read from address 0, result should be hit, no bus op
- Write to address 1, result should be hit, no bus op
- During the test, make sure to change the byte select bits to make sure that it doesn't affect the final results

LRU Tests

- Read from address 0-7, result should be all miss
- Read from address 8, result should be miss
- Read from address 9, result should be miss
- Use getLRU and check for LRU, should not be address 0

MESI/Snooping Tests

- First, invalidate all cache by setting to I
- Read from address 0, change I to either E or S
    - Using the byte select bits to determine snoop results from other caches
    - If no hit, then E
    - If hit/hitm, then S
- From E, S, or I to get to M
    - Write to address, hit, no bus op
    - M to I after a flush

Test Case Outlines

Miss Test 1 unoccupied

- Display cache set
- Read 4 addr to set,
- Display cache set, 4 cache lines should be occupied
- Read 4 addr to set, 8 cache lines should be occupied
- Check for correct Mesi, should only be e and s depending on byte offset
- 8 total cache reads
- 0 total cache writes
- 8 total cache miss
- 0 total cache hits
- 0/0 ratio

Miss Test 2 unoccupied

- Display cache set
- Write 4 addr to set,
- Display cache set, 4 cache lines should be occupied
- Write 4 addr to set, 8 cache lines should be occupied
- Check for Mesi, should only be M
- 0 total cache reads
- 8 total cache writes
- 8 total cache miss
- 0 total cache hits
- 0/0 ratio

Miss Test 3 read conflict/evict

- Display cache set
- Fill cache line
- Display cache set
- Read addr with different tag, should be miss
- Evict and change line , Mesi should be e or s
- 10 total cache reads
- 0 total cache writes
- 10 total cache miss
- 0 total cache hits
- 0/0 ratio

Miss Test 4 write conflict/evict

- Display cache set
- Fill cache line
- Display cache set
- Read addr with different tag, should be miss
- Evict and change line , Mesi should be M
- 0 total cache reads
- 10 total cache writes
- 10 total cache miss
- 0 total cache hits
- 0/0 ratio

Hit test 1 read

- Display cache set
- Read 4 addr to set
- Display cache set
- Read 2 of the same addr, hits
- Mesi to byteoff
- 6 total cache reads
- 0 total cache writes
- 2 total cache hits
- 4 total cache miss

Hit test 2 write

- Display cache set
- write 4 addr to set
- Display cache set
- write 2 of the same addr, hits
- MESI to M
- 0 total cache reads
- 6 total cache writes
- 2 total cache hits
- 4 total cache miss

LRU test 1 read

- Display cache set
- Fill cache set
- Access the first 2 lines
- Evict
- Should be the 4th way replaced

LRU test 2 write

- Display cache set
- Fill cache set
- Access the first 2 lines
- Evict
- Should be the 4th way replaced

Snoop invalid test

- Fill 3 lines
- One M, E and S
- Snoop each address
- Only S to I

Snoop read test

- Fill 3 lines
- One M, E and S
- Snoop each address
- Only M to S

Snoop write test

- Fill 3 lines
- One M, E and S
- Snoop each address
- All to I after hit
- No change if no hit

Snoop RWIM test

- Fill 3 lines
- One M, E and S
- Snoop each address
- All to I after hit
- No change if no hit