Power Consumption and Management for ECP5 and ECP5-5G Devices

Technical Note

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1. Introduction

A key requirement for many of today's high volume FPGA applications is low power consumption. The ECP5™ and ECP5-5G™ device provides many dynamic power-saving features for different blocks. This technical note provides users with detail for using the ECP5 and ECP5-5G device's low power architectural features including power supply considerations and power estimations provided by the Power Calculator tool.

2. Power Supply Sequencing and Hot Socketing

ECP5 and ECP5-5G devices have been designed to ensure predictable behavior during power-up and powerdown. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough (VCCMIN) to ensure reliable operation. In addition, leakage into I/O pins is controlled to within the limits specified in ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012), allowing for easy integration with the rest of the system.

These capabilities, along with lowest-power FPGA with SERDES, makes the ECP5 and ECP5-5G device the ideal choice for many low-power, high-speed SERDES, multiple power supply and hot-swap applications.

2.1. Recommended Power-up Sequence

Refer to the DC and Switching Characteristics section of ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012) for more information on any power-up sequence for ECP5 and ECP5-5G family.

3. Power Standby Mode

FPGA designers often minimize power consumption by turning off subsystems while configured and operational. Let us look at the different modes of operation for the device.

3.1. Normal Operation

Device is fully operational and all circuits are active and consuming highest power consumption.

3.2. Low Power Operation (Standby)

The ECP5 and ECP5-5G device have dynamic standby control for the components that are known to consume significant current consumption. The ECP device offers a flexible architecture that allows many on-chip components to be dynamically turned off during the low power operation modes.

Each of the block that has dynamic power control, is listed below, along with the signal that places it in standby mode.

Table 3.1. Power Save Features of ECP5 and ECP5-5G Devices

IP Block	Standby Control Signal
PLL	Through Standby Port.
DLL	Through freeze control. Internal oscillator will stop running to save power.
SERDES	Each RX and TX of each channel can be independently powered down through register bits or CIB signal controls.
IO	Through LVDS output buffer disable (per bank control) and INR disable (per bank control). Valid for Banks # 2, 3, 6, and 7.

The details of major power save features of the device are discussed in the sections that follow.

Dynamic Bank Controllers

The ECP5 and ECP5-5G device has Dynamic Bank Controllers that further help shut down power consuming sources in the IO blocks.

Referenced, differential and LVDS I/O standards consume more power than other I/O standards and are not always required to be active. The active high Bank Controller allows the designer to turn these I/Os off dynamically on a per bank selection. The Dynamic InRD (input referenced and differential I/Os) is used to turn off referenced and differential inputs. Dynamic LVDS control is used to turn off the LVDS output driver. The Bank Controller can be instantiated using the primitives shown (BCINRD for dynamic InRD, BCLVDSO for dynamic LVDS) are shown in the following sections.

In the ECP5 and ECP5-5G device, the Dynamic Bank Controller is used to power down banks InRD (Input Referenced and Differential), LVDS Outputs, PUSL (Pull up and Slew Rate) control.

INDENI (or Bank Controller for Input & Reference Differential)

This is used to disable the differential/reference receivers, vref generators and any bank controller reference circuits that consume DC power. It is to be noted that BCINRD can be enabled for all differential and referenced receivers - This applies to all rows of legal I/O combinations inputs except for the PCI, LVTTL or LVCMOS rows.

Here is the primitive for the BCINRD.

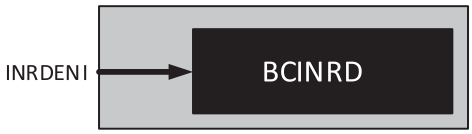

Figure 3.1. Input and Reference Differential Bank Controller

For a design that utilizes the power savings features of the devices, users can instantiate the INRDENI block in their design or in a soft power controller circuit that can turn off the Inputs and referenced differentials. It applies to the Banks # 2, 3, 6 and 7.

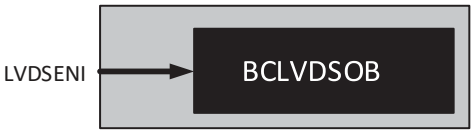

Figure 3.2. LVDS Output Buffers Bank Controller

For a design that utilizes the power savings features of the devices, users can instantiate the LVDSENI block in their design or in a soft power controller circuit that can turn off the Inputs and referenced differentials. It applies to the Banks # 2, 3, 6 and 7.

Generating the Dynamic Bank Controller

The Dynamic Bank Controller can be generated using Clarity Designer. From the Lattice Diamond environment, launch Clarity Designer and double-click **Dynamic Bank Controller** under Architecture Modules.

Select the options such as module name and HDL language, and then click **Customize**. The screen, shown in Figure 3.3, opens and allows you to generate a Dynamic Bank Controller module.

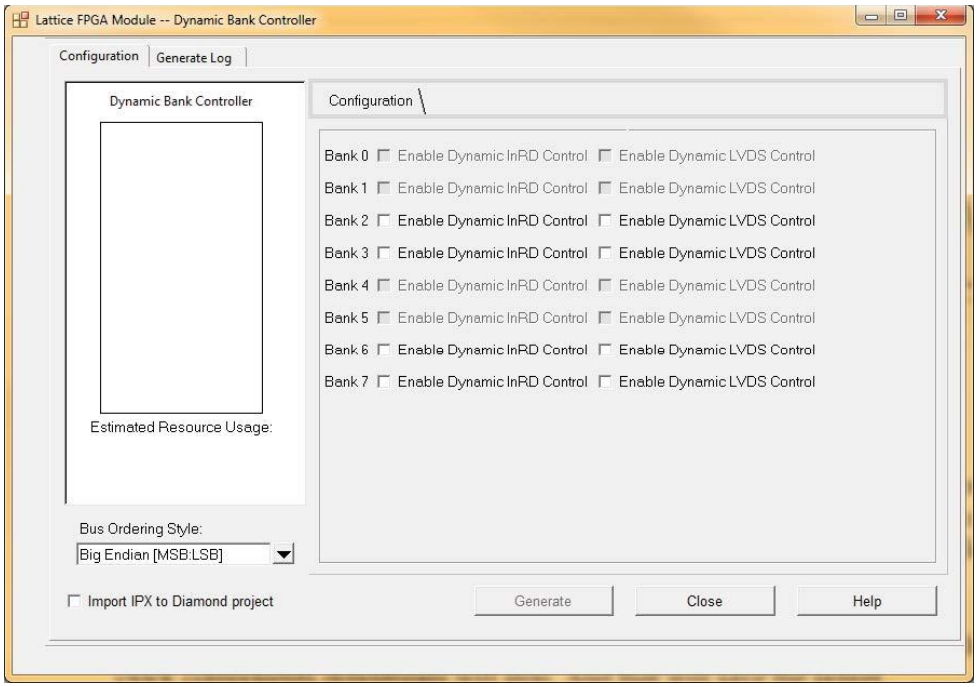

Figure 3.3. Generating Dynamic Bank Controller Using Clarity Designer

Soft Power Controller

All those standby operations can be access through fabric soft logic. The ECP5 and ECP5-5G device does not have a hard standby controller. All standby power management is done through soft logic.

Users can create their own logic that will control placing the components in the standby mode. The various controllers can be instantiated in the user code to place the components in standby mode.

A macro level block diagram for customer scenario is shown in Figure 3.4. This is for example purpose only.

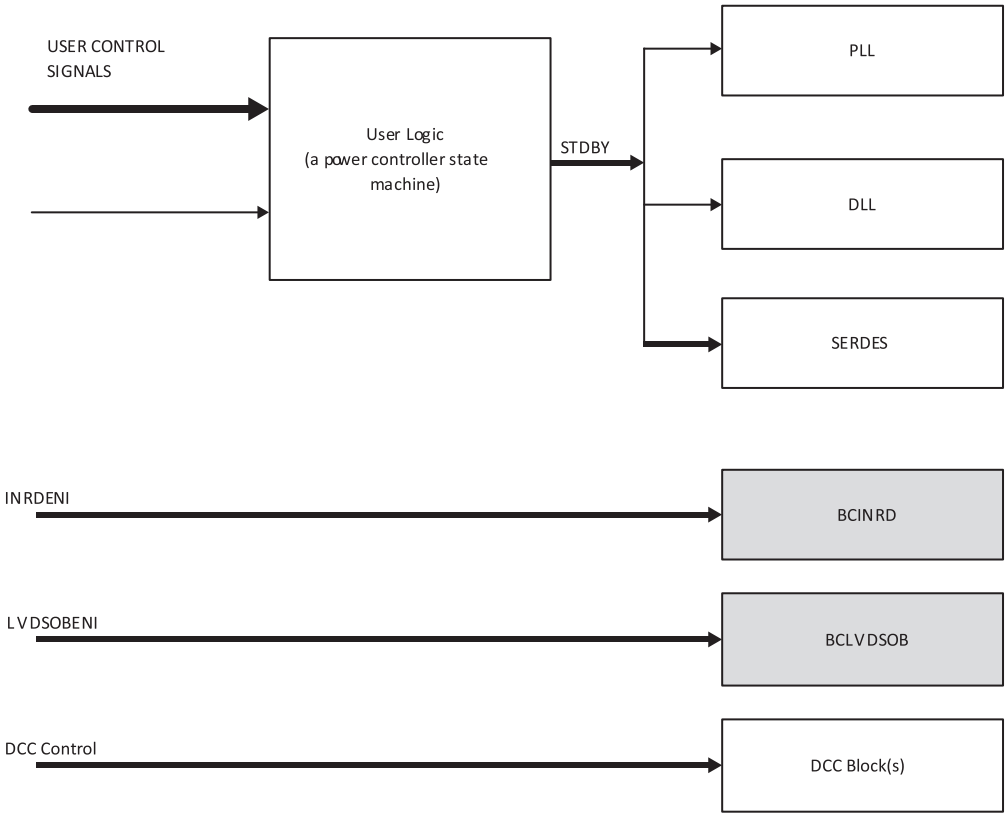

Figure 3.4. Macro Level Block Diagram for User Defined Power Controller

4. Digital Temperature Readout

ECP5 and ECP5-5G devices include a Digital Temperature Readout module. There is one DTR on the chip and users can use it to read the junction temperature at which the chip is operating.

Figure 4.1 provides the primitive that is required to be instantiated in the user design to be able to read the output of the DTR.

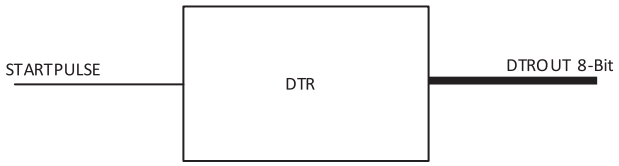

Figure 4.1. DTR Primitive

Table 4.1 provides the port definitions for the primitive and the logical capture port.

Table 4.1. Port Definitions for DTR

Port Name	Description	Logical Capture Port Name
STARTPULSE	Pulse to instruct DTR to start capturing temperature	cib_start_pulse
DTROUT	8-bit DTR output	tempcode<7:0>

The temperature codes for the ECP5 and ECP5-5G devices are defined for DTROUT(5:0). DTROUT(6) is reserved and DTROUT(7) is used as data valid bit.

4.1. DTR Timing

The default output for DTROUT in the functional and timing simulation corresponds to the code for 25 °C temperature. User can also override the value by providing a temperature code via a sim parameter. This is useful in simulation of using the right code in user logic when temperature reaches a particular value.

Table 4.2. DTR Simulation Parameters

Primitive Port	Parameter Name	Parameter Value	
START_PULSE			5ns wide start pulse to initiate DTR to measure temperature.
DTROUT(5:0)	DTR_TEMP	0 … 63 011001 (Default value, equivalent to 25°C)	DTR output that corresponds to the temperature (refer to DTR spec for binary values for different codes).
DTROUT(6)		0	DTROUT(6) is unused and reserved bit. The output value of this bit should match the HW and always set to 0 in simulation.
DTROUT(7)			DTROUT(7) bit is used for getting a data valid signal.

The timing waveform for the DTROUT is shown in Figure 4.2.

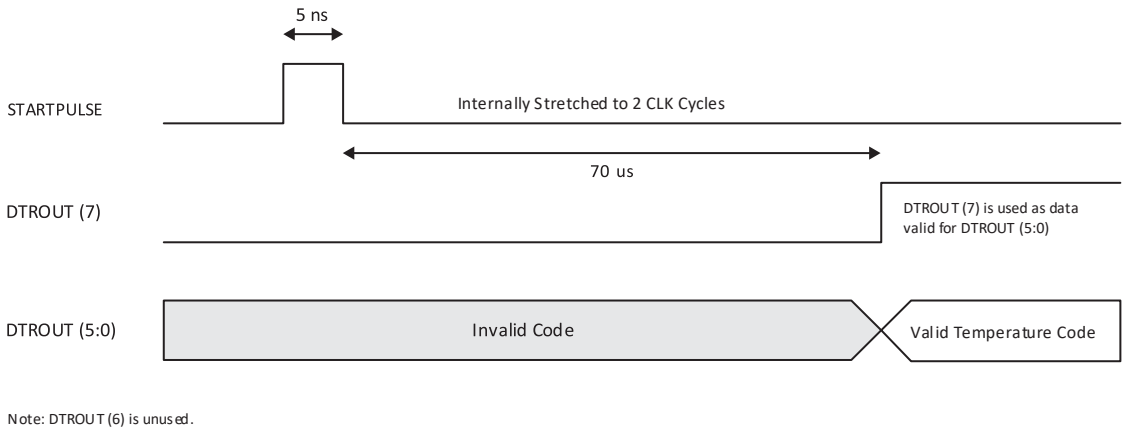

Figure 4.2. Timing Waveform for Valid Temperature with Respect to STARTPULSE

Figure 4.3 shows one of the scenarios where the DTR can be used. This is for example purposes only.

The User Logic block monitors the 8 bit DTROUT and can have fail safe control. When DTROUT shows that the temperature is high, user can get a visual indicator using Visual Display. Another way is to read DTROUT and then the USER LOGIC (user defined), can monitor the temperature. In case the temperature is high, this block can then generate a control signal for the design to shut down the clock.

Alternatively, the Control signal can also be used as an input to the user defined Power Controller and place the device in standby mode (for example).

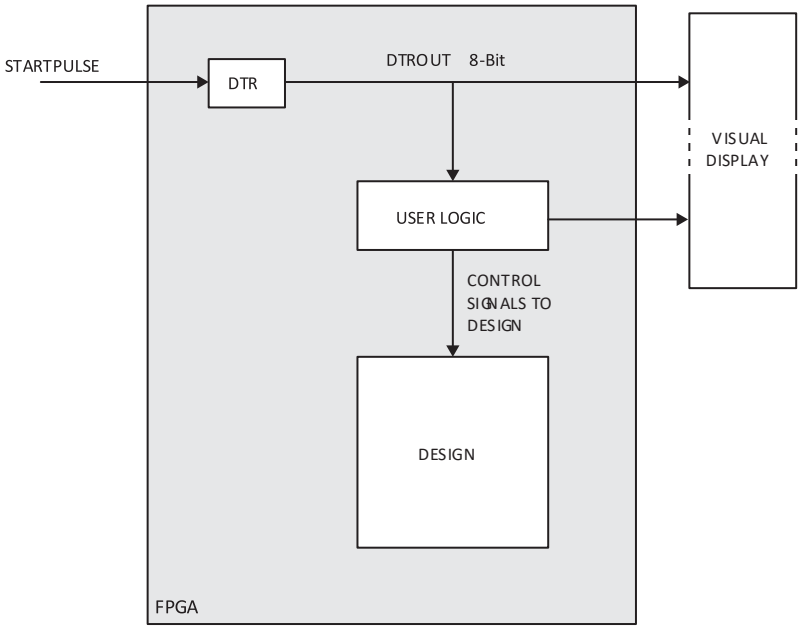

Figure 4.3. Using DTR Usage

4.2. Equivalent Junction Temperature for DTROUT values

Figure 4.3 provides the values of the corresponding Junction Temperature of the device. The table also includes the equivalent decimal values for ease of use.

Table 4.3. Valid DTROUT Values and Corresponding Junction Temperatures

Digital Temperature Readout						Decimal Equivalent	Junction Temperature
DTROUT (5)	DTROUT (4)	DTROUT (3)	DTROUT (2)	DTROUT (1)	DTROUT (0)		
0	0	0	0	0	0	0	–58
0	0	0	0	0	1	1	–56
0	0	0	0	1	0	2	–54
0	0	0	0	1	1	3	–52
0	0	0	1	0	0	4	–45
0	0	0	1	0	1	5	–44
0	0	0	1	1	0	6	–43
0	0	0	1	1	1	7	–42
0	0	1	0	0	0	8	–41
0	0	1	0	0	1	9	–40
0	0	1	0	1	0	10	–39
0	0	1	0	1	1	11	–38
0	0	1	1	0	0	12	–37
0	0	1	1	0	1	13	–36
0	0	1	1	1	0	14	–30
0	0	1	1	1	1	15	–20
0	1	0	0	0	0	16	–10
0	1	0	0	0	1	17	–4
0	1	0	0	1	0	18	0
0	1	0	0	1	1	19	4
0	1	0	1	0	0	20	10
0	1	0	1	0	1	21	21
0	1	0	1	1	0	22	22
0	1	0	1	1	1	23	23
0	1	1	0	0	0	24	24
0	1	1	0	0	1	25	25
0	1	1	0	1	0	26	26
0	1	1	0	1	1	27	27
0	1	1	1	0	0	28	28
0	1	1	1	0	1	29	29
0	1	1	1	1	0	30	40
0	1	1	1	1	1	31	50
1	0	0	0	0	0	32	60
1	0	0	0	0	1	33	70
1	0	0	0	1	0	34	76
1	0	0	0	1	1	35	80
1	0	0	1	0	0	36	81
1	0	0	1	0	1	37	82
1	0	0	1	1	0	38	83
1	0	0	1	1	1	39	84
1	0	1	0	0	0	40	85
1	0	1	0	0	1	41	86
1	0	1	0	1	0	42	87
1	0	1	0	1	1	43	88
1	0	1	1	0	0	44	89
1	0	1	1	0	1	45	95

Digital Temperature Readout						Decimal Equivalent	Junction Temperature
DTROUT (5)	DTROUT (4)	DTROUT (3)	DTROUT (2)	DTROUT (1)	DTROUT (0)		
1	0	1	1	1	0	46	96
1	0	1	1	1	1	47	97
1	1	0	0	0	0	48	98
1	1	0	0	0	1	49	99
1	1	0	0	1	0	50	100
1	1	0	0	1	1	51	101
1	1	0	1	0	0	52	102
1	1	0	1	0	1	53	103
1	1	0	1	1	0	54	104
1	1	0	1	1	1	55	105
1	1	1	0	0	0	56	106
1	1	1	0	0	1	57	107
1	1	1	0	1	0	58	108
1	1	1	0	1	1	59	116
1	1	1	1	0	0	60	120
1	1	1	1	0	1	61	124
1	1	1	1	1	0	62	128
1	1	1	1	1	1	63	132

5. Power Calculator

Power Calculator is the fastest power simulation tool available in the industry. The tool offers Estimation Mode for “what-if” analysis, and also allows designers to import NCD design files to accurately estimate power for their designs. The background engine performs each calculation quickly and accurately.

When running the Power Calculator tool in Estimation mode, designers provide estimates of the utilization of various components and the tool provides an estimate of the power consumption. This is a good start, especially for what-if analyses and device selection.

Calculation mode is a more accurate approach, where the designer imports the actual device utilization by importing the post place and route netlist design file (or NCD) file.

Users can also import a Trace Report (or TWR) file where the frequencies for various clocks are also imported. Note that the Trace Report only includes frequencies of the clocks nets that are constrained in the Preference file.

The default Activity Factor (AF%) for dynamic power calculation is set to 10% in the Power Calculator. Users can change the default AF for the entire project or for each clock net individually. Activity Factor is discussed in more detail later in this document.

5.1. Power Calculator and Power Equations

Please refer to the Diamond® Tutorial under Diamond Startup Page. Once you step through the procedure, you will see the Lattice Power Calculator main window as shown in Figure 5.1.

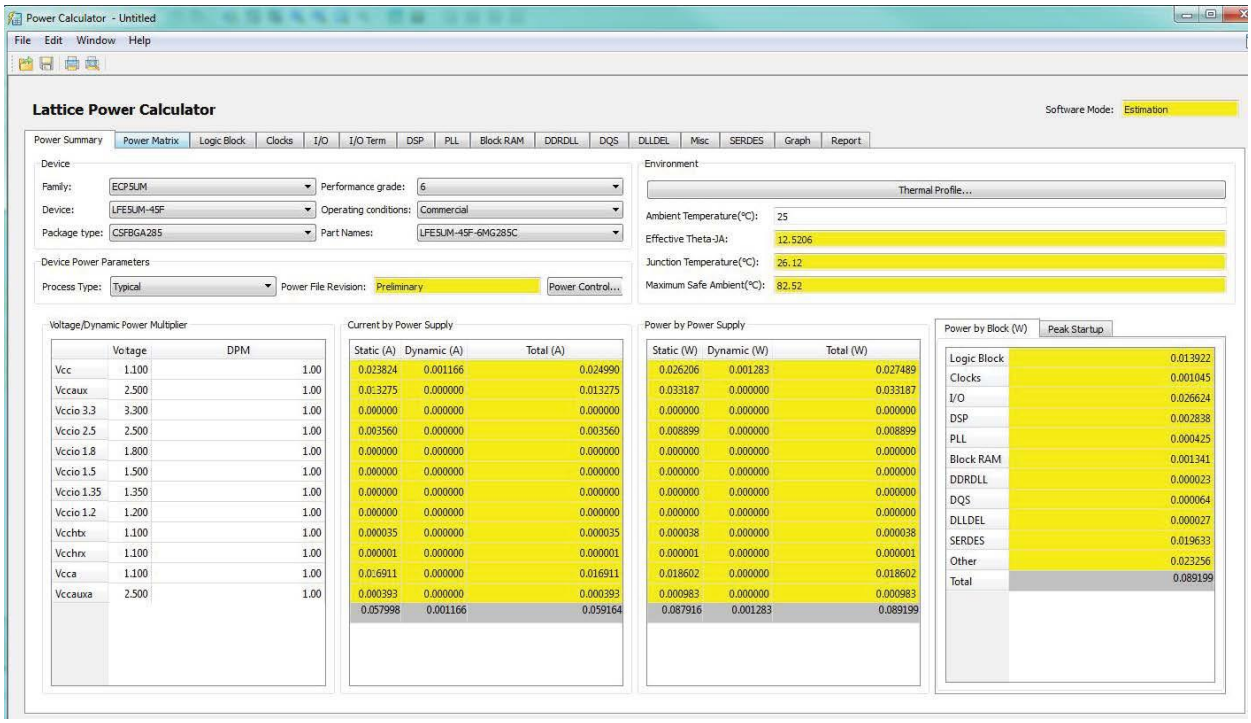

Figure 5.1. Power Calculator for ECP5 and ECP5-5G Devices

It is important to understand how the options available in Power Calculator affect the power. For example, if the ambient temperature is changed, the junction temperature is affected according to the following equation:

$$T_J = T_A + \Theta_{JA\_EFFECTIVE} * P \quad (1)$$

Where T_J and T_A are the junction and ambient temperatures, respectively, and P is the power.

$\Theta_{JA\_EFFECTIVE}$ is the effective thermal impedance between the die and its environment.

The junction temperature is directly dependent on the ambient temperature. An increase in T_A will increase T_J and result in an increase of the static leakage component.

Selecting the Process Type again affects the static leakage (or Static Power). For dynamic power, increasing the frequency of toggling will increase the dynamic component of power.

Typical and Worst Case Process Power/ICC

Another factor that affects DC power is process variation. This variation, in turn, causes variation in quiescent power.

Power Calculator takes these factors into account and allows designers to specify either a typical process or a worst case process.

Junction Temperature

Junction temperature is the temperature of the die during operation. It is one of the most important factors that affects the device power. For a fixed junction temperature, voltage and device package combination, quiescent power is fixed.

Ambient temperature affects the junction temperature as shown in Equation 1. Devices operating in a high-temperature environment have higher leakage since their junction temperature will be higher. Power Calculator models this ambient to junction temperature dependency. When the user provides an ambient temperature, it is rolled into an algorithm that calculates the junction temperature and power through an iterative process to find the thermal equilibrium of the system (device running with the design) with respect to its environment (T_A, airflow etc.).

Maximum Safe Ambient Temperature

Max. Safe Ambient Temperature is one of the most important numbers displayed in the Summary tab of the Power Calculator. This is the maximum ambient temperature at which the design can run without violating the junction temperature limits for commercial or industrial devices.

Power Calculator uses an algorithm to accurately predict this temperature. The algorithm adjusts itself as the user changes options such as voltage, process, frequency, AF% etc. (or any factor that may affect the power dissipation of the device).

Operating Temperature Range

When designing a system, engineers must make sure a device operates at specified temperatures within the system environment. This is particularly important to consider before a system is designed. With Power Calculator, users can predict device thermodynamics and estimate the dynamic power budget. The ability to estimate a device's operating temperature prior to board design also allows the designer to better plan for power budgeting and airflow.

Although total power, ambient temperature, thermal resistance and airflow all contribute to device thermodynamics, the junction temperature (as specified in ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012)) is the key to device operation. The allowed junction temperature range is 0 °C to 85 °C for commercial devices and –40 °C to 105 °C for industrial devices. If the junction temperature of the die is not within these temperature ranges, the performance and reliability of the device's functionality cannot be guaranteed.

Dynamic Power Multiplier (DPM)

It is difficult to estimate the temperature dependence of dynamic power due to various ways in which a design can be placed and routed. The user-defined frequency of operation makes this problem even more complex. To help resolve this issue, the Dynamic Power Multiplier provides some guard bands for system and board designers.

The Dynamic Power Multiplier is defaulted to "1" which means the dynamic power is what it is. If the user wishes to add 20% additional dynamic power, the DPM can be set to 1.2 (1 + 20%) and it can be placed against the appropriate power supply. This increases the dynamic power for that supply by 20% and provides users with some guard band (if needed).

Power Budgeting

Power Calculator provides the power dissipation of a design under a given set of conditions. It also predicts the junction temperature (T_J) for the design. Any time this junction temperature is outside the limits specified in ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012), the viability of operating the device at this junction temperature must be re-evaluated.

A commercial device is likely to show speed degradation with a junction temperature above 85 °C and an industrial device at a junction temperature will degrade above 100 °C. It is required that the die temperature be kept below these limits to achieve the guaranteed speed operation.

Operating a device at a higher temperature also means a higher SICC. The difference between the SICC and the total ICC (both Static ICC and Dynamic ICC) at a given temperature provides the dynamic budget available. If the device runs at a dynamic ICC higher than this budget, the total ICC is also higher. This causes the die temperature to rise above the specified operating conditions.

The four factors of power, ambient temperature, thermal resistance and airflow, can also be varied and controlled to reduce the junction temperature of the device. Power Calculator is a powerful tool to help system designers to properly budget the FPGA power that, in turn, helps improve overall system reliability.

Dynamic Power Savings

The Power Calculator dynamically estimates the power when the Bank Controller and other power save features are implemented in a design.

The ECP5 and ECP5-5G device has number of options to control the power, these can range from Bank Controllers to the disabling individual PLLs/ DLLs.

On the Summary tab of Power Calculator, there is a Power Controller button. Clicking the button will launch a window to perform what-if analysis to evaluate power consumption when different dynamic power options are used. The window looks like as shown below.

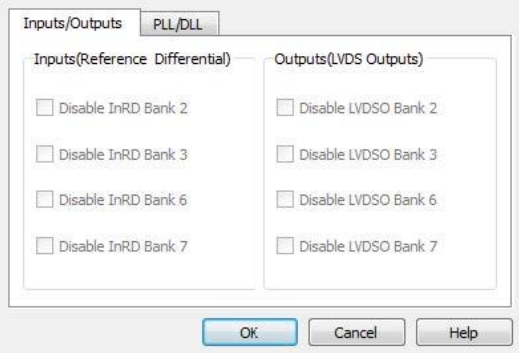

Figure 5.2. Dynamic Power Controller for ECP5 and ECP5-5G Devices

Activity Factor Calculation

The Activity Factor % (or AF%) is defined as the percentage of frequency (or time) that a signal is active or toggling the output. Most resources associated with a clock domain are running or toggling at some percentage of the frequency at which the clock is running. Users must provide this value as a percentage under the AF% column in the Power Calculator tool.

Another term for I/Os is the I/O Toggle Rate. The AF% is applicable to the PFU, Routing, and Memory Read Write Ports, etc. The activity of I/Os is determined by the signals provided by the user (in the case of inputs) or as an output of the design (in the case of outputs). The rates at which the I/Os toggle define their activity. The I/O Toggle Rate or the I/O Toggle Frequency is a better measure of their activity.

The Toggle Rate (or TR) in MHz of the output is defined in the following equation:

$$\text{Toggle Rate (MHz)} = 1/2 * f * AF\% \quad (5)$$

Users are required to provide the TR (MHz) value for the I/O instead of providing the frequency and AF% for other resources. AF can be calculated for each routing resource, output or PFU. However, this involves long calculations. The general recommendation for a design occupying roughly 30% to 70% of the device is an AF% between 15% and 25%. This is an average value. The accurate value of an AF depends upon clock frequency, stimulus to the design and the final output.

Power Calculator allows users to import a VCD file from their simulation to accurately assess the activity factor of their design (Edit > Open Simulation File). The VCD file is based on Post-P&R simulation and it is an ASCII file generated by the simulator. All major simulation tools allow that, please check simulation tool documentation on how to generate VCD file. It is to be noted that the AF calculated from the VCD file is based on how accurate the test-bench or stimulus is for the simulation.

6. Thermal Impedance and Airflow

A common method for characterizing a packaged device's thermal performance is with "Thermal Resistance", Θ. For a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are °C/W.

The most common examples are:

- Θ_{JA}, Thermal Resistance Junction-to-Ambient (in °C/W)
- Θ_{JC}, Thermal Resistance Junction-to-Case (also in °C/W)
- Θ_{JB}, Thermal Resistance Junction-to-Board (in °C/W)

Knowing the reference (i.e. ambient, case, or board) temperature, the power, and the relevant Θ value, the junction temperature can be calculated per following equations.

- $T_J = T_A + \Theta_{JA} * P$
- $T_J = T_C + \Theta_{JC} * P$
- $T_J = T_B + \Theta_{JB} * P$

Where T_J, T_A, T_C and T_B are the junction, ambient, case (or package) and board temperatures (in °C), respectively. P is the total power dissipation of the device.

Θ_{JA} is commonly used with natural and forced convection air-cooled systems. Θ_{JC} is useful when the package has a high conductivity case mounted directly to a PCB or heatsink. And Θ_{JB} applies when the board temperature adjacent to the package is known.

Power Calculator utilizes the ambient temperature (°C) to calculate the junction temperature (°C) based on the Θ_{JA} for the targeted device. Users can also provide the airflow values (in LFM) to obtain a more accurate junction temperature value.

To improve airflow effectiveness, it is important to maximize the amount of air that flows over the device or the surface area of the heat sink. The airflow around the device can be increased by providing an additional fan or increasing the output of the existing fan. If this is not possible, baffling the airflow to direct it across the device may help. This means the addition of sheet metal or objects to provide the mechanical airflow guides to guide air to the target device. Often the addition of simple baffles can eliminate the need for an extra fan. In addition, the order in which air passes over devices can impact the amount of heat dissipated.

6.1. DELPHI Models

DELPHI Models are thermo-mechanical models that can be used to simulate thermal behavior of the ECP5 and ECP5-5G device when used in a system.

DELPHI Models for the ECP5 and ECP5-5G device can be downloaded from the web and they are compatible with Flomerics' FloTHERM® and Mentor Graphics' Icepak tools.

7. Reducing Power Consumption

One of the most critical challenges for designers today is reducing the system power consumption. A low-order reduction in power consumption goes a long way, especially in modern hand-held devices and electronics. There are several design techniques that can be used to significantly reduce overall system power consumption. Some of these include:

- Using the ECP5 and ECP5-5G device power saving architecture features like Bank Controller and standby power controls.
- Reducing operating voltage while staying within data sheet limits.
- Operating within the specified package temperature limitations.
- Using optimum clock frequency reduces power consumption, as the dynamic power is directly proportional to the frequency of operation. Designers must determine if some portions of the design can be clocked at a lower rate that will reduce power.
- Reducing the span of the design across the device. A more closely-placed design uses fewer routing resources and therefore less power.
- Reducing the voltage swing of I/Os where possible.
- The unused IOs are powered by the VCCIO of a bank. Confining the unused IOs in a single bank and then lowering V_{CCIO} of the bank also helps reduce leakage of the unused IOs.
- Ensuring input logic levels are not left floating but pulled either up or down.
- Ensuring no I/O pull-up/down conflicts with other components on the board.
- Using optimum encoding for the Finite State Machines and counters, where possible. For example, a 16-bit binary counter has, on average, only 12% activity factor and a 7-bit binary counter has an average of 28% activity factor. On the other hand, a 7-bit LFSR counter will toggle at an activity factor of 50%, which causes higher power consumption. A gray code counter, where only one bit changes at each clock edge, will use the least amount of power, as the activity factor is less than 10%.
- Clock gating techniques can be used along with reducing the area of the spread of the design. When used together, these reduce the elements that are toggled by the clock, resulting in lower dynamic power. For details on Clock Gating, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (FPGA-TN-02200).
- Minimizing the operating temperature by the following methods:

    - Use packages that can better dissipate heat, such as ceramic packages.
    - Place heat sinks and thermal planes around the device on the PCB.
    - Use better airflow techniques, such as mechanical airflow guides and fans (both system fans and device mounted fans).
- To achieve the lowest standby power:
    - All clocks and combinatorial logic should be held at a steady state.
    - All inputs should be held at a rail.
    - All outputs should be tri-stated and the Bank Controller should turn off referenced and LVDS outputs.
    - PLLs should be turned off using the standby port.

8. Power Calculator Assumptions

The following are the assumptions made by the Power Calculator.

- The Power Calculator tool uses equations with constants based on a room temperature of 25°C. The default temperature of 25 °C can be changed.
- Users can define the ambient temperature (T_A) for device junction temperature (T_J) calculation based on the power estimation. T_J is calculated from the user-entered T_A and the power calculation of typical room temperature.
- I/O power consumption is based on an output loading of 5 pF. Designers have the ability to change this capacitive loading.
- Users can estimate power dissipation and current for each type of power supply (V_{CC} and V_{CCIO}).
- The nominal VCC is used by default to calculate power consumption. A lower or higher VCC can be chosen from a list of available values.
- Θ_{JA} can be changed to better estimate the operating system manually or by entering Airflow in Linear Feet per Minute (LFM) along with a Heat Sink options.
- The default value of the I/O types for ECP5 and ECP5-5G devices is LVCMOS25, 8 mA.
- The activity factor (AF) is defined as the toggle rate of the registered output. For example, assuming that the input of a flip-flop is changing at every clock cycle, 100% AF of a flip-flop running at 100 MHz is 50 MHz. The default activity factor for logic is 10%.
- Users can import the VCD file from their simulation to get activity factor based on the simulation. It is to be noted that the AF from VCD is as good as the coverage int he simulation.
- Unused IOs are configured as LVCMOS Inputs with weak internal pull ups. These are generally powered off the V_{CCIO} that is connected to the bank.
- Users have an option to import the Frequency from trace report (TWR) or preference file (LPF).
- The operating junction temperature range for commercial grade devices is 0 °C to 85 °C, Industrial is –40 °C to 100 °C and Automotive is –40 °C to 125 °C. For details, please refer to the DC Electrical Characteristics section in the data sheet.
- For thermal impedance, Power Calc default value is based on a medium size board (~6" x 6", with six to eight layers), with no heatsink and 200 LFM airflow. This can be changed as needed under Thermal Profile section in the tool.
- All virtual devices current and power consumption is calculated for the larger device on which the virtual device is based on.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.2, January 2022

Section	Change Summary
All	• Changed document number from TN1266 to FPGA-TN-02210. • Updated document template.
Disclaimer	Added this section.
Digital Temperature Readout	Updated the number of DTR blocks in the ECP5 chip to 1.

Revision 1.1, November 2016

Section	Change Summary
All	• Added support for ECP5-5G. • Changed document title to Power Consumption and Management for ECP5 and ECP5-5G Devices
Power Calculator and Power Equations	Updated Power Calculator and Power Equations section. Replaced Figure 5.1, Power Calculator for ECP5 Devices.
Technical Support Assistance	Updated Technical Support Assistance section.

Revision 1.0, March 2014

Section	Change Summary
All	Initial release.

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