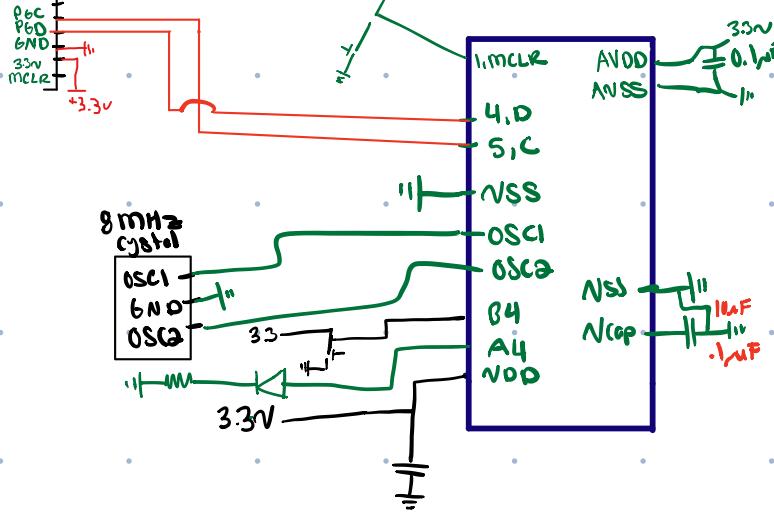


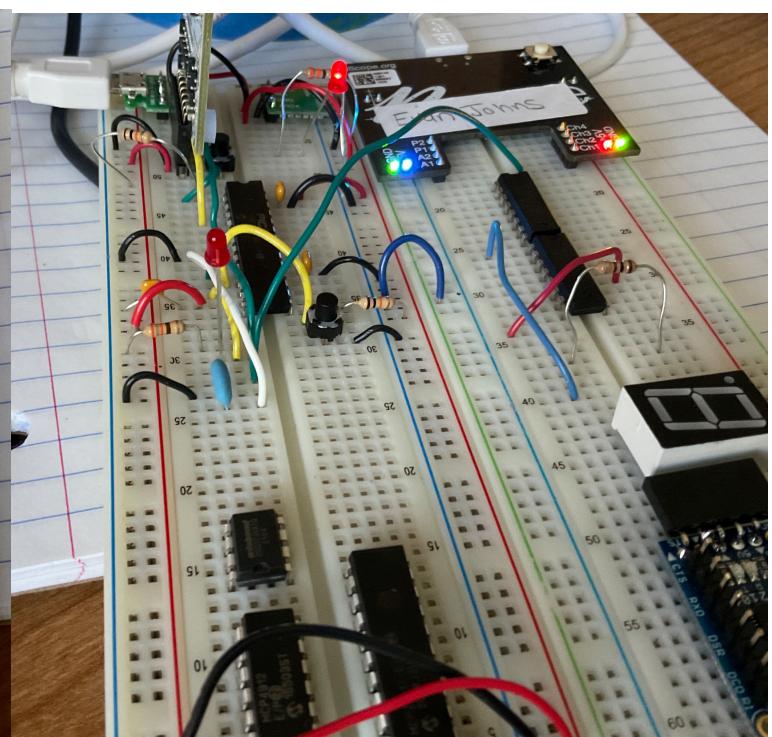
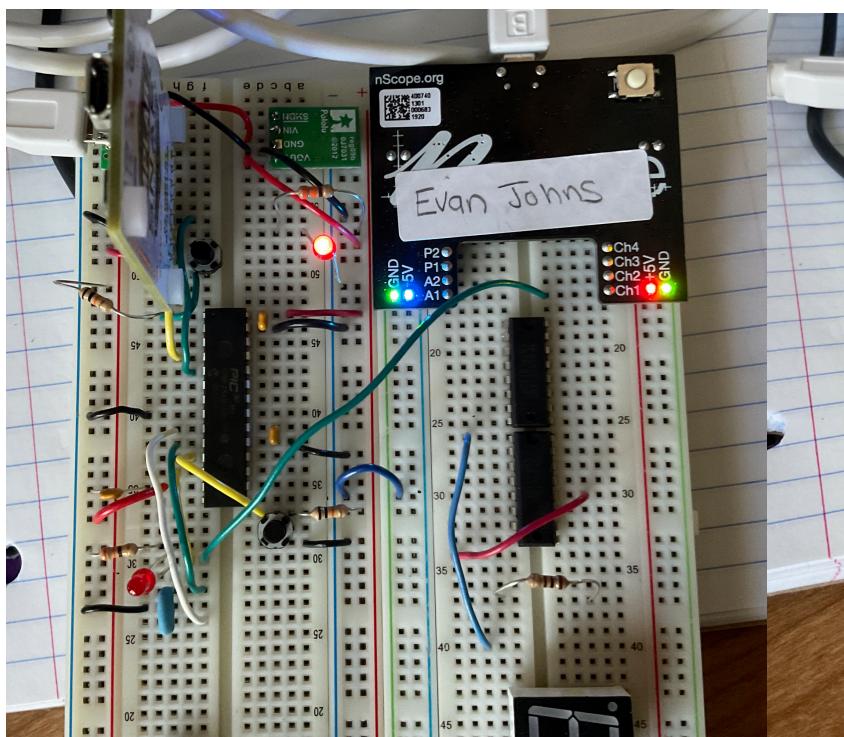
**SNAP**



**SNAP**

1. MCLR
2. 3.3V
3. -
4. P6D
5. P8C

Pin #	Full Pin Name	Pin #	Full Pin Name
1	MCLR	15	PGE3/RPB6/PMD6/RB6
2	VREF+/CVREF+/AN0/C3IN/C/PAA0/CTED1/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED1/AN2/C1ND/C2IN/B/C3ND/RPB0/RB0	18	TDI/RPB9/SDA1/CTED4/PMD3/RB9
5	PGE1/AN3/C1NC/C2NAR/RB1/CTED12/RB1	19	Vss
6	AN4/C1INB/C2ND/RPB2/SQ2A/CTED13/RB2	20	Vcap
7	AN5/C1NA/C2IN/RTCC/RPB3/SCL2/RB3	21	PGE2/TPB10/CTED11/PMD2/RB10
8	Vss	22	PGE2/TMS/TPB11/PMD1/RB11
9	OSC1/CLK1/RPA2/RA2	23	AN1/PMD0/RB12
10	OSC2/CLK2/RPA3/PMA0/RA3	24	AN1/TPB13/TPS/PMD/RB13
11	SOSC1/TPB4/RB4	25	CVREFOUT/AN10/C3IN/TPB14/SCK1/CTED5/PMWR/RB14
12	SOSC2/RPA4/T1CK/CTED9/PMA1/RA4	26	AN9/C3NA/TPB15/SCK2/CTED6/PMCS1/RB15
13	Vdd	27	AVss
14	PGED3/TPB7/PMD7/RB5	28	AVdd



```
#include<xc.h> // processor SFR definitions
#include<sys/attribute.h> // __ISR macro

// DEVCFG0
#pragma config DEBUG = OFF // disable debugging ICS_P6X1
#pragma config JTAGEN = OFF // disable jtag OFF
#pragma config ICESEL = X // use FQGDI and FQGCI OFF
#pragma config FWp = X // disable flash write protect OFF
#pragma config BWP = X // disable boot write protect OFF
#pragma config CP = X // disable code protect

// DEVCFG1
#pragma config FNOSC = X // use primary oscillator or crystal HS
#pragma config FOSCEN = X // enable secondary oscillator OFF
#pragma config IESO = X // disable switching clock OFF
#pragma config POSCMOD = X // high speed crystal mode
#pragma config OSCIOFNC = OFF // disable clock output
#pragma config FBDIV = X // divide by 1 for 8MHz system clock
#pragma config FCKSM = X // disable clock switch
#pragma config WDTPS = X // use 1ms for largest wdt
#pragma config WINDIS = X // use 1ms window at 256
#pragma config FWDTEN = X // wdt disabled
#pragma config FWDTWNSZ = X // use 1ms window at 256

// DEVCFG2 - get the system clock to be 8MHz
//          from the 32MHz crystal
#pragma config FPLLIDIV = X // divide input-clock to be in range 4-8MHz
#pragma config FPLLIMUL = X // multiply system clock by FPLLIDIV
#pragma config FPLLIDIV = X // divide clock FPLLIDIV to 8MHz
//          to get 4MHz
// DEVCFG3
#pragma config USERID = 0 // some 16bit user-id, doesn't matter what
#pragma config PMDLWAY = X // allow multiple reconfigurations
#pragma config IOLIWAY = X // allow multiple reconfigurations
```

PRIPLL

OFF

HS

OFF

OFF

OFF

HS

OFF

HS