FPGA LAB
Assignment 1

Yenigalla Samyuktha
EE20MTECH14019

Download all codes from

https://github.com/EE20MTECH14019/FPGA−14019/tree/main/Assignment_1

and latex-tikz codes from

https://github.com/EE20MTECH14019/FPGA−14019/tree/main/Assignment_1

1 Problem

(CBSE/CS/2015-1/6.c) Derive a Canonical POS expression for a Boolean function F, represented by the following truth table 0:

P	Q	R	$F(P,Q,R)$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

TABLE 0: Truth table for Function F

2 Solution

From the truth table 0, the function $F(P,Q,R)$ can be represented in the Canonical POS form as follows:
As F is logic 0 for four input combinations, the corresponding max terms are,

$$M_1 = (P + Q + \bar{R}) \tag{2.0.1}$$
$$M_2 = (P + \bar{Q} + R) \tag{2.0.2}$$
$$M_5 = (\bar{P} + Q + \bar{R}) \tag{2.0.3}$$
$$M_6 = (\bar{P} + \bar{Q} + R) \tag{2.0.4}$$

And the Canonical POS expression can be expressed using these max terms as.

$$F = M_1 \cdot M_2 \cdot M_5 \cdot M_6 \tag{2.0.5}$$
$$F = \prod M\,(1,2,5,6) \tag{2.0.6}$$
$$F = (P + Q + \bar{R}) \cdot (P + \bar{Q} + R) \cdot (\bar{P} + Q + \bar{R}) \cdot (\bar{P} + \bar{Q} + R) \tag{2.0.7}$$

Implementation using two input NAND gates

Minimizing the function (2.0.7) using K-maps,

P \ QR	00	01	11	10
0	1	0	1	0
1	1	0	1	0

From the K-Map, the minimized POS form is,

$$F = (Q + \bar{R}) \cdot (\bar{Q} + R) \tag{2.0.8}$$
$$F = \bar{Q} \cdot \bar{R} + Q \cdot R \tag{2.0.9}$$

Using Demorgan's law,

$$F = \overline{\overline{(\bar{Q} \cdot \bar{R})} \cdot \overline{(Q \cdot R)}} \tag{2.0.10}$$

Now, implementing the Boolean function F in (2.0.10) using two input NAND gates:

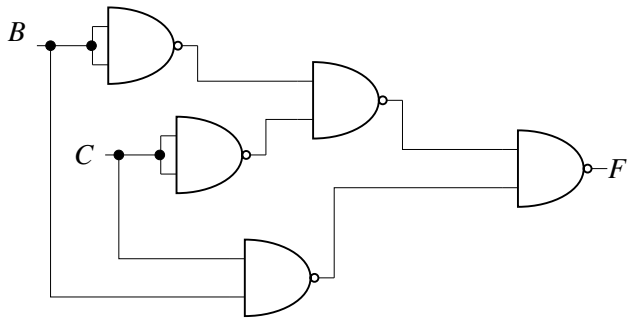

Fig. 0: Implementation using two input NAND gates