# Air-Core Coupled Inductor Based Modular Solid-State Circuit Breaker With Reduced Components for DC Buildings

Aditya Pogulaguntla, *Member, IEEE*, Daniel Dsa, *Student Member, IEEE*, Griddaluru Venkata Yagna, Satish Naik Banavath, *Senior Member, IEEE*, Edivan Laercio Carvalho, *Senior Member, IEEE*, Andrii Chub, *Senior Member, IEEE*, and Dmitri Vinnikov, *Fellow, IEEE*

***Abstract*—Traditional residential and commercial buildings can be decarbonized by adopting DC microgrids powered by renewable energy sources. With the challenges of DC systems and increasing power consumption, DC distribution systems of the buildings require modular and fast protective DC circuit breakers (DCCBs) against fault events. A few modular thyristor-based solid-state circuit breakers are presented in the literature for high-current applications. However, each proposed module requires a commutation circuit and a current sensor. This paper proposes a novel single-branch solid-state circuit breaker (SB-SSCB) that uses air-core coupled coils to commutate an SCR in the main conduction path. The modularity is achieved by extending the SB-SSCB to the two-branch solid-state circuit breaker (TB-SSCB) design to handle high currents. In this design, the two primary paths run parallel and share current, equipping three winding air-core coupled coils. The proposed TB-SSCB topology greatly reduces the component count because only one commutation circuit is required for fault current interruption in both branches. Air-core coils mitigate the necessity of over-dimensioning the core material to prevent saturation at higher current levels, hence decreasing the weight of the system. The proposed SB-SSCB and TB-SSCB are described in detail, including their operating modes. Then, a detailed approach for selecting and designing the components is provided. Later, the proposed topologies are compared to recent thyristor-based DCCBs. The proposed SB-SSCB and TB-SSCB are experimentally validated by developing a laboratory prototype for the standardized voltage level of 350 V DC given by the IEC 60364 and NPR 9090 for houses, offices, and commercial buildings, and at a nominal current rating of 10 A.**

***Index Terms*—Green buildings, DC distribution system, fault protection, DC circuit breaker (DCCB), solid-state circuit breaker (SSCB), high current applications, modularity, air core coupled coils.**

## I. Introduction

THE buildings account for almost 30% of total greenhouse gas emissions in the global energy sector, directly and indirectly [1]. Conventionally, buildings have relied on alternating current (AC) power supplied by the grid. However, to tackle environmental issues caused by carbon emissions, interest in direct current (DC) systems has grown over the past few decades due to the deployment of sustainable generation sources and advancements in end-use technologies [2]. The use of distributed energy resources (DERs) like solar photovoltaics, wind, fuel cells, and energy storage systems, combined with the widespread adoption of electronics, EVs, and LEDs, has led to a shift towards installing DC systems in buildings [3]–[5]. Green residential or commercial buildings utilizing DC power distribution provide various benefits over typical AC systems. These microgrids operate natively on DC power, eliminating the need for several power conversion stages required when integrating renewable sources, energy storage systems, and natively DC loads, increasing overall system efficiency and lowering energy losses. The DC systems improve reliability, increase configuration flexibility, and simplify the integration of DERs and loads [6]–[8].

Despite these various advantages, designing and implementing an appropriate protection system for DC microgrids remains a significant challenge. The difficulty stems from a rapid rise in DC fault current, which needs to be extinguished when there are no naturally occurring zero crossing points, possibly resulting in persistent arcs [9]–[12]. DCCBs are already very well studied and have emerged as a technology that enables the adaption of future DC systems in buildings. Because there is no natural zero current crossing in fault currents of DC systems, modified mechanical circuit breakers require extra arc extinguishing mechanisms to force the fault current to zero, resulting in a bulky and complicated design [13]. Taking advantage of power semiconductor device's quick and arc-less fault current turn-off performance, SSCBs are gaining appeal in different applications, including DC buildings [14]. As the adoption of DC residential microgrids continues to expand, the development and implementation of SSCBs will play a vital role in guaranteeing their safe and reliable functioning. By solving the unique protection requirements of DC power distribution, SSCBs open the way for the widespread integration of renewable energy sources and realize a sustainable, robust, and efficient energy future for buildings.

Semi-controlled switch-based SSCBs are gaining much rele-

This research is based upon work supported by the Science and Engineering Research Board (SERB), Department of Science and Technology (DST), India. File No: EEQ/2023/000017. The work of Estonian collaborators was supported in part by the Estonian Research Council under Grant PRG1086 and in part by the Estonian Centre of Excellence in Energy Efficiency, ENER (grant TK230), funded by the Estonian Ministry of Education and Research.

Aditya Pogulaguntla, Daniel Dsa, Griddaluru Venkata Yagna and Satish Naik Banavath are with the Department of Electrical, Electronics and Communication Engineering, Indian Institute of Technology Dharwad (IIT Dharwad), Dharwad, Karnataka 580007, India (e-mail:211021002@iitdh.ac.in; daniel.dsa@iitdh.ac.in; satish@iitdh.ac.in [corresponding author]).

Edivan Laercio Carvalho, Andrii Chub, and Dmitri Vinnikov are with the Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology Tallinn, Estonia, 19086, email: edivan.carvalho@taltech.ee; andrii.chub@taltech.ee; dmitri.vinnikov@taltech.ee.

vance due to their lower cost, easy market availability at higher voltage and current ratings, high short-circuit current withstand capability, and low conduction losses of the thyristors at high currents [15], [16]. Z-source circuit breakers (ZSCBs) [17], [18], which have been intensively investigated over the past decade, have gained a lot of attention for their automatic fault current interruption, eliminating sensing and trip electronics. The authors in [19] have proposed a modified z-source topology to mitigate undesired power flow and negative current flow in the load for a short period during commissioning and current stress through the SCR during reclosing. However, this modified topology cannot provide bidirectional protection, so the authors in [20], [21] introduced bidirectional ZSCB circuits. However, the proposed bidirectional ZSCB topologies incorporate many components. Several coupled inductor-based bidirectional ZSCBs [22]–[26] are also introduced to offer configurable fault current trip levels. However, the main drawback of ZSCBs is their inability to trip for large-impedance short-circuit faults and overload events. The authors in [16] have proposed a way to realize overload protection. However, this method uses extra power semiconductor devices, increasing control and design complexity. To address these drawbacks, a new class of thyristor-based SSCBs is proposed. The topologies proposed in [27]–[30] include a current sensor and use mutual coupling between the coupled inductors to achieve the commutation of the SCR.

The DC circuit breaker's rating must be significantly increased to accommodate the high current requirements of a DC residential or commercial microgrid with modern-day heavy loads such as EV chargers, HVAC systems, and LED lights. To deal with higher currents, the core material in the coupled inductor-based SSCBs needs to be oversized, leaving a margin to avoid saturation. This often increases the design cost and adds more weight to the system, which is undesirable in residential installations where space is limited. This paper introduces a new thyristor-based single-branch solid-state circuit breaker (SB-SSCB) topology incorporating air-core coupled coils for fault interruption. In [29], [31], the authors proposed a modular SSCB design for high-current applications and concluded that the respective designs could be more compact by connecting more modules. However, when considering two modules for operation, the proposed designs require a commutation circuit and a current sensor for each module. To address the issues, this paper proposes an extension to SB-SSCB, a two-branch SSCB (TB-SSCB) that uses air-core three-winding coupled coils, a single commutation circuit, and a current sensor, thereby greatly reducing the component count.

The main advantages or contributions of proposed circuit breaker are listed below.

1) The proposed circuit breaker utilizes air-core coupled coils, thus avoiding oversizing of the core in the design process for higher system currents.
2) It incorporates the feature of modularity which makes it more practical for high-power applications.
3) The two-branch design of the proposed breaker requires only one commutation circuit, whereas the existing modular topologies [29], [31] have been designed with separate commutation circuits for each module or branch. This feature greatly reduces the component count and cost and reduces the effort needed to maintain the circuit breaker.
4) Unless like the modular topologies presented in the literature, TB-SSCB contains only one current sensor for both branches. In case of failure of any branch, another parallel path may get overloaded and can interrupt the system falsely in [29], [31] and requires reconfiguration of each sensor preset fault current level. This arrangement reduces the sensor count and control complexity.

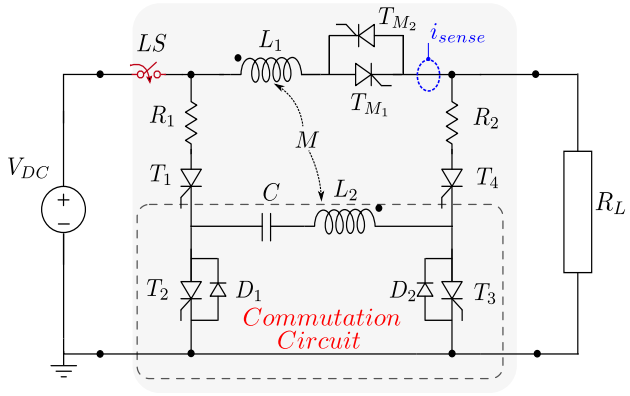



Fig. 1: Proposed SB-SSCB topology.

The paper is organized as follows. Section II describes the modes of operation of the proposed SB-SSCB and TB-SSCB in detail. Section III discusses the circuit analysis and design methodology of the proposed topologies. Hardware implementation details and results are provided in Section IV. Section V provides a detailed comparison of the proposed topologies with the recent thyristor-based SSCBs, highlighting the merits and drawbacks of the design. The conclusions are drawn in Section VI.

## II. PROPOSED BIDIRECTIONAL SB-SSCB AND TB-SSCB TOPOLOGIES

This section provides a detailed explanation of the operational modes of the proposed bidirectional SB-SSCB and TB-SSCB with a neat sketch of schematics. The single-branch topology, as shown in Fig. 1, consists of two main thyristors $T_{M_1}$ and $T_{M_2}$ connected in an anti-parallel fashion to facilitate bidirectional power flow. The proposed circuit breaker incorporates air-core coupled coils $L_1$ and $L_2$ wound on top of each other. The commutation circuit contains capacitor $C$, winding of the inductor $L_2$, thyristors $T_2$, $T_3$ and diodes $D_1$ and $D_2$. The thyristors $T_1$, $T_3$, and $T_2$, $T_4$ are mainly triggered to charge the capacitor. The resistors $R_1$ and $R_2$ are utilized to limit the peak capacitor charging current, and the low-speed switch $LS$ provides galvanic isolation between the DC bus and load.

### A. Operating Principle of SB-SSCB

Fig. 2 illustrates the operational modes of the proposed single-module SSCB. These modes are considered with the assumption that power flows from the right port to the left port since the proposed breaker is symmetrical. The proposed

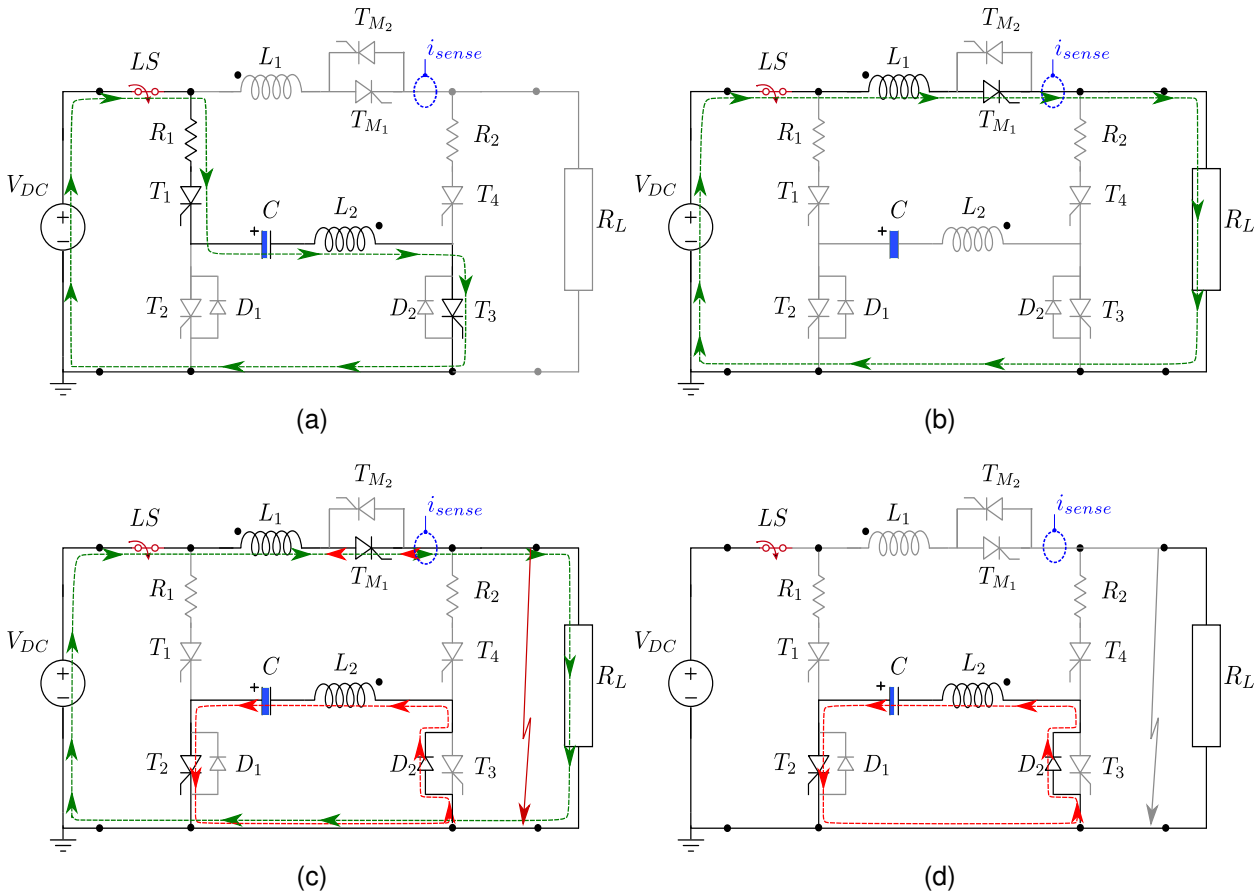



Fig. 2: Modes of operation for the proposed SB-SSCB: (a) Capacitor charging mode (*mode-1*), (b) Steady-state operation (*mode-2*), (c) Fault current interruption (*mode-3*), and (d) Resonance interval (*mode-4*).

breaker contains winding $L_1$ of the coupled inductor and SCR $T_{M_1}$ in the main conduction path. The conceptual waveforms about the modes of operation are illustrated in Fig. 3.

1) *Mode-1 ($t_1$ to $t_2$)*: The circuit schematic elucidating *mode-1* is shown in Fig. 2(a). In this mode, the switch $LS$ is closed and the thyristors $T_1$ and $T_3$ are triggered at the instant $t_1$ to charge the capacitor through a path $V_{DC} \rightarrow R_1 \rightarrow T_1 \rightarrow C \rightarrow L_2 \rightarrow T_3$ as indicated by green dotted line. To avoid resonance and prevent the capacitor from charging over the DC bus level, the behavior or response of the resonant circuit is intentionally overdamped by adding a resistor, $R_1$. This resistance also helps to limit the charging current. Once the capacitor is charged to the input DC voltage level, the charging current gradually falls below the holding current values of the thyristors $T_1$ and $T_3$, causing them to commutate automatically. Neglecting ESR and voltage drops of the thyristors, the governing capacitor voltage and current equations of this mode are given below.

$$V_C(t) = V_{DC} + A_1 V_{DC}\ e^{(-\alpha+\sqrt{\alpha^2-\omega_o^2})t} + A_2 V_{DC}\ e^{(-\alpha-\sqrt{\alpha^2-\omega_o^2})t} \tag{1}$$

$$i_C(t) = C\left(A_1 V_{DC}(-\alpha+\sqrt{\alpha^2-\omega_o^2})e^{(-\alpha+\sqrt{\alpha^2-\omega_o^2})t} + A_2 V_{DC}(-\alpha-\sqrt{\alpha^2-\omega_o^2})e^{(-\alpha-\sqrt{\alpha^2-\omega_o^2})t}\right) \tag{2}$$

where $A_1 = \dfrac{-\alpha-\sqrt{\alpha^2-\omega_o^2}}{2\sqrt{\alpha^2-\omega_o^2}}$, $A_2 = \dfrac{\alpha-\sqrt{\alpha^2-\omega_o^2}}{2\sqrt{\alpha^2-\omega_o^2}}$, $\alpha = \dfrac{R_1}{2L_2}, \omega_o = \dfrac{1}{\sqrt{L_2 C}}$

2) *Mode-2 ($t_2$ to $t_4$)*: In this mode, the main thyristor $T_{M_1}$ is triggered at the instant $t_2$ to allow the power flow from the source to load. After an initial transient period from $t_2$ to $t_3$, the system achieves a steady state with a voltage across the load equal to the DC bus voltage, ignoring voltage drop across the SCR and power loss in the winding $L_1$. The voltage across winding $L_2$ and current through SCR $T_{M_1}$ can be expressed as below

$$V_{L1}(t) = V_{DC}\ e^{\frac{-R_L}{L_1}t} \tag{3}$$

$$i_{T_{M_1}}(t) = \frac{V_{DC}}{R_L}\left(1 - e^{\frac{-R_L}{L_1}t}\right) \tag{4}$$

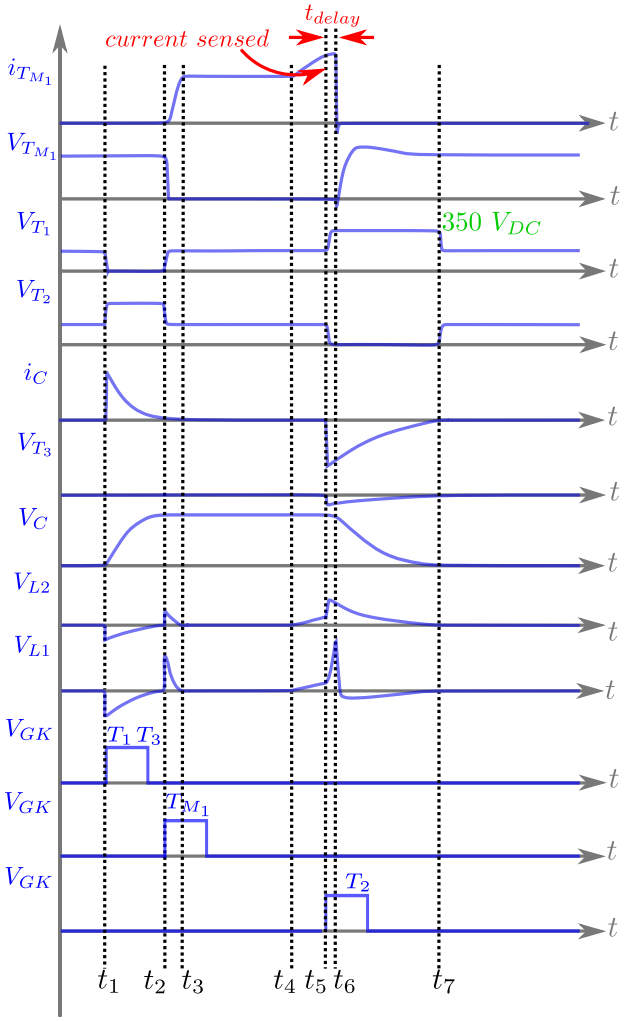



Fig. 3: Conceptual waveforms depicting modes of operation.

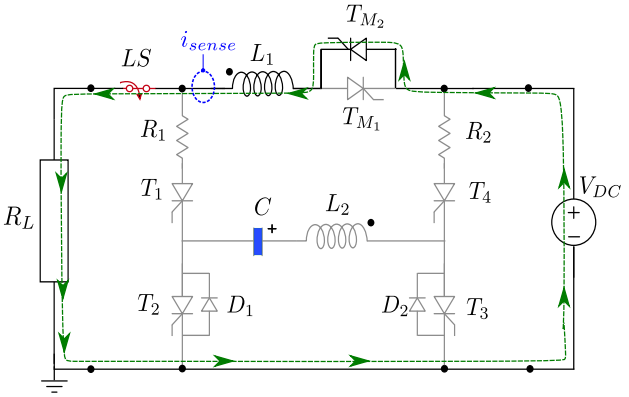



Fig. 4: Proposed SB-SSCB topology - reverse operation.

During this mode, the capacitor holds its energy as there is no path to discharge. The circuit diagram corresponding to this mode is shown in Fig. 2(b).

3) *Mode-3 ($t_4$ to $t_6$)*: The circuit schematic illustrating *Mode-3* is shown in Fig. 2(c). In this mode, a step change of load, short circuit fault, or an overcurrent event is created at the output port side of the circuit breaker at the instant $t_4$. The proposed topology incorporates a current sensor in the main conduction path. The current sensor continuously monitors the

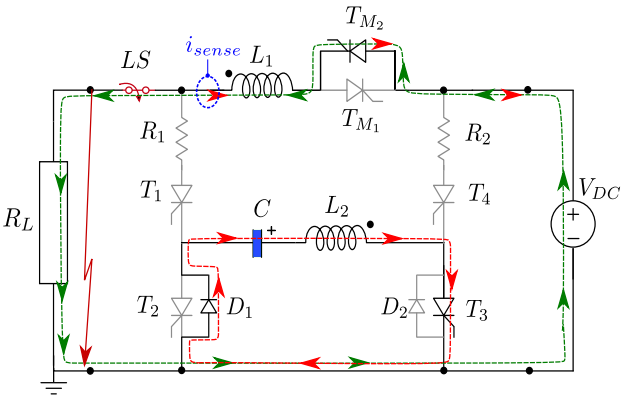



Fig. 5: Proposed SB-SSCB topology fault interruption - reverse operation.

main SCR $T_{M_1}$ current. When a fault occurs at the load side, the thyristor's current rises. When this current reaches the preset fault value (at the time instant $t_5$), a microcontroller unit generates the gate pulse for the thyristor $T_2$. After a short delay introduced by the sensor and trip electronics, the commutation thyristor $T_2$ is turned on at $t_6$. As a result, the capacitor discharges its energy through a path $C \rightarrow T_2 \rightarrow D_2 \rightarrow L_2$. The capacitor discharge current passes into the dot terminal of the winding $L_2$, changing the flux through the coil. As the windings $L_1$ and $L_2$ are wound on top of each other, the main winding $L_1$ also experiences the same rate of change of flux. This induces an EMF across the winding $L_1$ by the principle of electromagnetic induction. The induced EMF opposes the DC bus voltage and develops a counter transient current through the main thyristor $T_{M_1}$, which aids commutation by creating a natural current zero crossing point. After the short reverse recovery period, the main thyristor is turned off, and the current to the fault location and load is cut off.

3) *Mode-4 ($t_6$ to $t_7$)*: Following the fault interruption, the commutation circuit behaves as an LC resonance circuit. The capacitor discharges its remaining energy fully during the time interval between $t_6$ to $t_7$. Because of the resistance of the winding $L_2$ along with the ESR of the capacitor, the oscillations are damped. This mode of operation is described in Fig. 2(d).

Once the fault is fully cleared, the thyristors $T_1$ and $T_3$ are again triggered to charge the capacitor to the input voltage level. This ensures the circuit breaker's capacity to re-break in post-fault conditions. The proposed SSCB additionally allows for controlled power flow interruption in either direction by triggering the relevant commutation thyristors $T_2$ or $T_3$ to perform maintenance activities. Moreover, the capacitor $C$ could be charged repeatedly during continuous normal operation to compensate for self-discharge.

### *B. Realization of Fault Interruption in SB-SSCB for Reversed Current Flow*

This subsection briefly explains the operation of the proposed topology for bidirectional (reversed current flow) with SB-SSCB. Since the circuit in Fig. 1 is symmetric from both ports, the operating principle remains the same as explained

above. However, control gate trigger pulses are now given to the complimentary thyristors. The circuit schematic showing the reverse conduction of current is given in Fig. 4. To charge the capacitor, thyristors $T_4$ and $T_2$ are triggered simultaneously. Then, thyristor $T_{M_2}$ is triggered to instate the power flow in the reverse direction as shown in Fig. 4. For a fault on the load side, the current is sensed and if it hits the preset value, relevant thyristor $T_3$ is triggered. This helps the capacitor to discharge through winding $L_2$, SCR $T_3$, and diode $D_1$ as shown in Fig. 5. Due to the mutual coupling effect between $L_1$ and $L_2$, the fault is interrupted as described in the previous subsection.

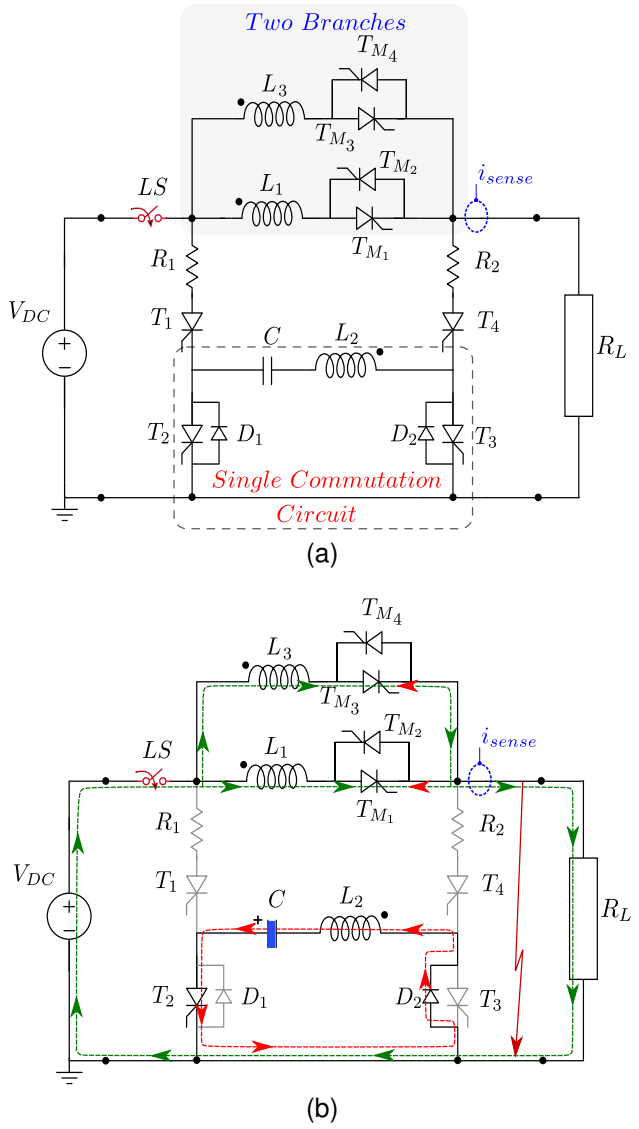



Fig. 6: (a) Proposed TB-SSCB and (b) TB-SSCB at the instant of fault interruption.

### C. Proposed Two-Branch Bidirectional SSCB (TB-SSCB) with Single Commutation Circuit for High Power Applications

The circuit schematic of the proposed design is shown in Fig. 6(a). The proposed two-branch DCCB functions in a manner identical to the single-branch topology as outlined in the previous sub-section. The fault interruption for the two-branch topology is illustrated in Fig. 6(b). The working operation is described briefly in the discussion below.

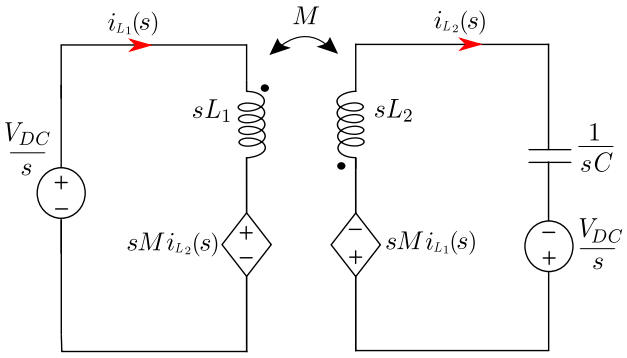



Fig. 7: Equivalent circuit of SB-SSCB during fault interruption.

The switch $LS$ is closed during the initial commissioning of the circuit breaker. Two gating pulses have to be sent to the thyristors $T_1$ and $T_3$ simultaneously to charge the capacitor $C$. Once the capacitor is fully charged, the main thyristors $T_{M_1}$ and $T_{M_3}$ in two parallel branches are triggered to allow power to the load. The short delay between the two gate pulses could cause the nominal load current to initially flow entirely through one branch until the next thyristor is activated. Nevertheless, afterward, the current will divide between the two branches based on their respective path resistances. A single current sensor is enough to monitor the overall load current. When the current reaches the preset level during a fault, a command is delivered to the gate driver, triggering the thyristor $T_2$. The capacitor discharges energy into the winding $L_2$, and according to the induction principle, an EMF developed across both the windings $L_1$ and $L_3$, aids in the commutation of the thyristors $T_{M_1}$ and $T_{M_3}$ and isolating the fault.

## III. Circuit Analysis and Component Selection

In this section, the equivalent circuit during the fault current interruption is modeled and the governing equations for choosing required inductance and capacitance are derived from the mathematical model. The guidelines for selecting the current limiting resistors are also provided. To simplify the analysis, the on-state voltage drops of the thyristors, winding resistance of the coils, and ESR of the capacitor are omitted.

### A. Short Circuit Modelling

The equivalent circuit during the thyristor commutation is shown in the Fig. 7. The set of s-domain equations of the system during this interval are given below.

$$\frac{V_{DC}}{s} = sL_1 i_{L_1}(s) + sMi_{L_2}(s) \tag{5}$$

$$\frac{V_{DC}}{s} = sMi_{L_1}(s) + \left[sL_2 + \frac{1}{sC}\right] i_{L_2}(s) \tag{6}$$

and

$$M = k\sqrt{L_1 L_2} \tag{7}$$

where $M$ is the mutual inductance between the coils and $k$ is the coupling coefficient, which is usually between $0 < k < 1$.

The analysis is performed assuming tight coupling between the coils. For the analysis, the $L_1$ and $L_2$ are considered as $L$ and $\frac{L}{n^2}$, respectively, where $n$ is the turns ratio of the coupled coils. The equation (8) provides a time-domain representation of the total current through the SCR $T_{M_1}$ during the turn-off period, taking into account the initial thyristor peak current ($I_{peak}$) before the fault trigger and the transient current during commutation by solving the equations (5) and (6).

$$\begin{aligned} i_{L_1}(t) &= i_{T_{M_1}}(t) \\ &= I_{peak} + \frac{V_{DC}}{L}t + (1-nk)\frac{V_{DC}}{n}\sqrt{\frac{C}{L(1-k^2)}}sin\omega t \\ &\quad - \frac{V_{DC}}{n}\sqrt{\frac{C(1-k^2)}{L}}sin\omega t \end{aligned} \tag{8}$$

where $\omega = \sqrt{\frac{n^2}{LC(1-k^2)}}$

Simplifying the equation (8) by applying the Taylor expansion yields the below expression for the SCR current.

$$i_{T_{M_1}}(t) = I_{peak} + (1-nk)\frac{V_{DC}}{L(1-k^2)}t \tag{9}$$

From (9), it is observed that the thyristor $T_{M_1}$ current drops to zero when

$$nk > 1 \tag{10}$$

By satisfying the above condition, the current through SCR reaches zero. After the SCR current drops to zero, the voltage across it also falls to a negative value to initiate the reverse recovery process. This helps in sweeping out the extra stored charge carriers in junctions and makes the thyristor turn off completely. The s-domain equation for commutation loop after the SCR turns off, is given below.

$$\frac{V_{DC}}{s} - nL_2I_{peak} - \left[sL_2 + \frac{1}{sC}]\right] i_{L_2}(s) = 0 \tag{11}$$

The time-domain expressions for voltage across the capacitor and current through the capacitor can be obtained by using equation (11) as provided below.

$$i_{L_2}(t) = i_C(t) = V_{DC}\sqrt{\frac{C}{L_2}}sin\frac{t}{\sqrt{L_2C}} + nI_{peak}cos\frac{t}{\sqrt{L_2C}} \tag{12}$$

$$V_C(t) = V_{DC}cos\frac{t}{\sqrt{L_2C}} - nI_{peak}\sqrt{\frac{L_2}{C}}sin\frac{t}{L_2C} \tag{13}$$

During the capacitor discharge interval, the voltage across the thyristor is given as,

$$V_{T_{M_1}} = V_{DC} - nkV_C \tag{14}$$

The voltage across the thyristor $T_{M_1}$ should remain negative for at least the device turn-off time ($t_q$) of the SCR. Substituting equation (13) in (14) and applying Taylor expansion yield the following condition for voltage across SCR for a duration of $t_q$.

$$V_{T_{M_1}}(t) \leq 0, t \geq t_q \tag{15}$$

$$\frac{nkV_{DC}}{2L_2C}{t_q}^2 + \frac{n^2kI_{peak}}{C}t_q + (1-nk)V_{DC} \leq 0 \tag{16}$$

The capacitor can be sized following the condition below.

$$C \geq \frac{nk}{2L_2(nk-1)}t_q^2 + \frac{n^2kI_{peak}}{(nk-1)V_{DC}}t_q \tag{17}$$

The value of $t_q$ can be selected from the datasheet of the chosen thyristor. By choosing a threshold current level ($I_{peak}$) and combining expressions (10) and (17), the sizing of $C$, $L_1$, $L_2$ can be done. A similar procedure can be followed to obtain the expressions for the design of coils and the capacitor of TB-SSCB topology.

### *B. Physical Design of Coupled Coils ($L_1$, $L_2$ and $L_3$)*

After obtaining the parameters required for the design of the coils, the cylindrical solenoid can be physically designed using a simple Wheeler's formula given below,

$$L = \frac{N^2r^2}{9r + 10l} \tag{18}$$

where N, r, and l are the number of turns, inner radius, and solenoid length in inches, respectively. The more detailed expression for inductance of the solenoid taking into the account wire diameter ($d_w$) and turn gap ($d_{tg}$) is reproduced from [32] below

$$L = \frac{\mu_o\pi N^2r^2}{Nd_w + (N-1)d_{tg} + 0.9r} \tag{19}$$

After choosing the required inductance and turns ratio, physical sizing of the inductor is made using the relation (18) or (19).

### *C. Selection of Current Limiting or Charging Resistors ($R_1$ and $R_2$)*

The resistors are chosen according to expressions given below to guarantee the peak current through thyristors, is limited to their maximum value ($i_{TSM}$, maximum peak non-repetitive surge current) and voltage response across the capacitor is overdamped to avoid charging it beyond the input DC level.

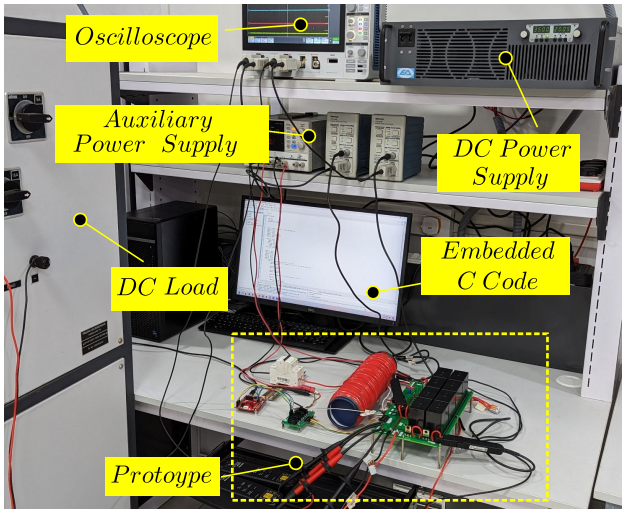
$$\frac{R_{1,2}}{2L_2} > \frac{1}{\sqrt{L_2C}} \tag{20}$$

$$\begin{aligned} i_{TSM} > C\Big(&A_1V_{DC}(-\alpha + \sqrt{\alpha^2 - \omega_o^2}) \\ &+ A_2V_{DC}(-\alpha - \sqrt{\alpha^2 - \omega_o^2})\Big) \end{aligned} \tag{21}$$

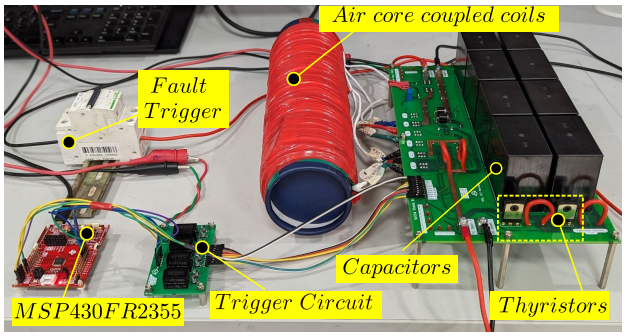
### *D. Selection of Diodes*

From Fig. 2(c) and Fig. 5, diodes $D_1$ and $D_2$ only conduct during fault interruption. Capacitor $C$ and inductor $L_2$ form a resonant loop where capacitor current flows through diodes for a short instant. Ideally neglecting ESR of the capacitor $C$, winding resistance of $L_2$, and path resistance, the maximum current flowing through diodes should be greater than the maximum value of current in equation (12) given below.

$$i_{D_{1,max}}, i_{D_{2,max}} > \sqrt{\frac{V_{DC}^2}{L_2} + n^2I_{peak}^2} \tag{22}$$




(a)




(b)

Fig. 8: (a) Experimental setup and (b) zoomed view of the designed laboratory prototype.

### *E. Selection of Thyristors*

Under a faulty scenario, the main path thyristors carry fault current, which can be expressed by equation (23).

$$i_f(t) = \frac{V_{DC}}{R_L} + \frac{V_{DC}}{L_{line} + L_1} t \tag{23}$$

With delays introduced by the current sensor and gate trigger circuit, the fault current increases linearly beyond the preset value since it is proportional to $t$. Thus care must be taken while selecting the current sensor and trigger circuits. Maximum current rating of SCR should be more than the preset fault current value. Assuming that the capacitor voltage from equation (13) swings to a negative DC bus at the end of resonance, the maximum blocking voltage of main path thyristors should be greater than two times the DC input voltage. However, thyristors employed in the commutation circuits can be of low-power rated devices since they do not conduct all the time. Considering the lab constraints, all the thyristors chosen for carrying out the experiment are of high-power-rated ones.

### *F. Implication of Line Inductance on Circuit Breaker Performance*

The line inductance in a practical system cannot be ignored while studying the behavior of the circuit breaker. Importantly,

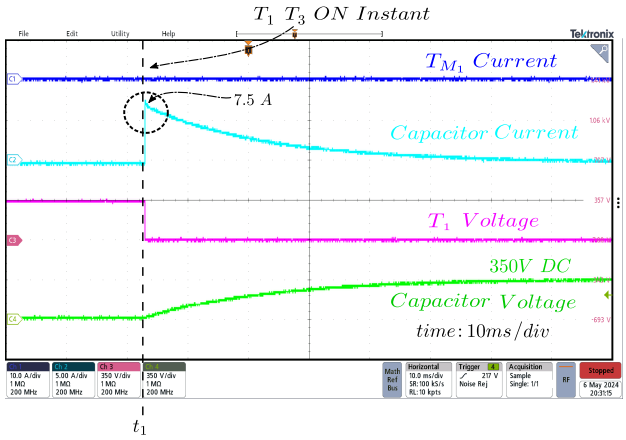



Fig. 9: Experimental result showing capacitor charging to the DC grid voltage.

line inductance slows down the commutation speed of thyristor which can lead to heavy stress on system components and circuit breaker failure. The dynamic value of thyristor current given in the equation (9) does not take line inductance into account. The modified thyristor current equation with inclusion of line inductance is provided in the equation (24).

$$i_{T_{M_1}}(t) = I_{peak} + (1 - nk)\frac{V_{DC}}{(L + L_{line})(1 - k^2)} t \tag{24}$$

For specific design parameters and satisfying the condition stated in (10), it is evident from equation (24) that with increasing $L_{line}$, the slope with which thyristor current falls reduces, leading to slow commutation response.

## IV. Experimental Validation

This section provides details of the hardware implementation and experimental validation and presents an elaborate discussion of the results. The experimental setup and the prototype developed in the laboratory are shown in Figs. 8(a) and 8(b), respectively. The proposed single- and two-branch circuit breaker topologies are validated for a DC power system with voltage and current ratings of 350 V and 10 A, respectively, which is relevant to the DC residential/commercial grid applications. The major components and pieces of equipment that have been used for the experimental validation are the 400 V/25 A DC power supply (from enArka Instruments), Vishay thyristors (SCR) 40TPS12A, Infineon's 1ED3123MU12H isolated driver IC, and RECOM R24P21509D DC/DC converter. These components are utilized for the design of gate trigger circuits implemented on PCB. An MSP430FR2355 microcontroller is used as a control and communication interface. A metalized polypropylene film capacitor (Panasonic EZPV60117MTC) is utilized to implement the required capacitance for the circuit breaker. A LEM LA 55-P current sensor is used to monitor the current through the main thyristor(s). The components and the equipment are summarized in the TABLE I.

### *A. Results and Discussion for SB-SSCB Topology*

This subsection presents the experimental results to validate the performance of the proposed single-branch topology shown

TABLE I: Components and Equipment.

| Components / Equipment | Value/Rating | Type/Part No |
|---|---|---|
| DC-link voltage ($V_{DC}$) | 350 V | eNarka 400 V / 25 A |
| Coupled coils($L_1$=$L_3$, and $L_2$) | 250 µH, 50 µH | Custom made |
| Capacitor ($C$) | 880 µF | EZPV60117MTC, Panasonic |
| Load resistance ($R_l$) | 35 Ω | Generic |
| Charging Resistors ($R_1$ & $R_2$) | 45 Ω | Generic |
| Thyristors ($T_{M_1}$, $T_{M_3}$, $T_1$, $T_2$, $T_3$ and $T_4$ ) | 1200 V, 40 A | 40TPS12A, Vishay |
| Diodes ($D_1$ & $D_2$) | 1000 V , 6 A | FR607, EiC Semi |

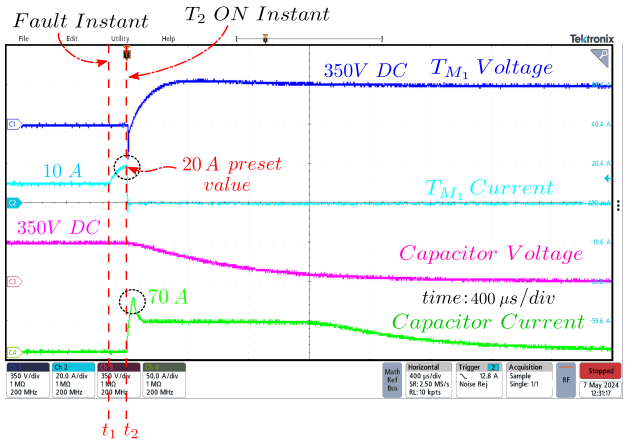



Fig. 10: Experimental result showing 20 A fault current interruption by SB-SSCB for 350 V, 10 A system.

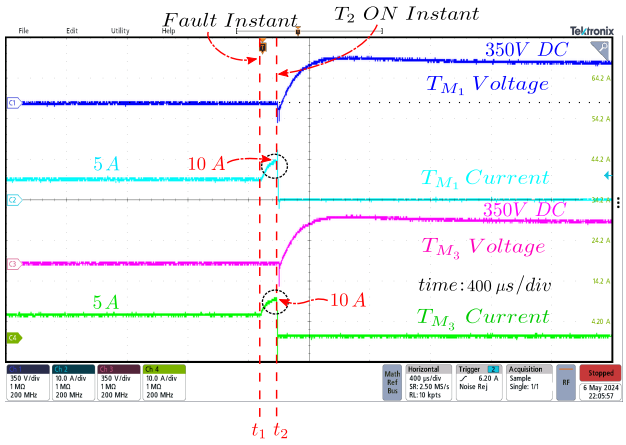



Fig. 11: Experimental result showing fault interruption by TB-SSCB for a system rating of 350 V , 10 A .

in Fig. 1. Initially, the switch $LS$ is closed. The thyristors $T_1$ and $T_3$ are triggered at the time instant $t_1$ as shown in the Fig. 9 to charge the capacitor to 350 $V$ DC. During this period, due to the presence of current limiting / charging resistance ($R_1$) of 45 Ω, ESR of the capacitor, and winding $L_2$ resistance, the observed peak charging current is close to 7.5 $A$ and the time taken by the capacitor to reach steady state voltage level is approximately 65 $ms$. After the capacitor charges to the DC grid voltage, the thyristors $T_1$ and $T_3$ are observed to be turned off automatically as the current through them falls below the holding threshold value. During the capacitor charging interval, the current through the main thyristor is observed to be zero since its gate pulse is kept low. Later, a gate trigger pulse is given to the main thyristor $T_{M_1}$ to establish the power flow to the load. Since the breaker is validated with a load resistance of 35 Ω, the current through the main thyristor settles closely to 10 $A$ after a short transient period. To check the circuit breaker response to the fault, a step change in load is initiated at the instant $t_1$ as shown in Fig. 10, so that the current through the system starts increasing gradually. This rate of the current change depends mostly on the inductor $L_1$. The preset fault current value is set as 20 $A$ for this validation study. When the main path current rises due to fault, the analog output from the current sensor gets compared with the equivalent reference set in the microcontroller ADC module. When the current goes beyond 20 $A$, the microcontroller takes the action to provide the trigger pulse to the gate of the commutation circuit thyristor $T_2$. After a short cumulative delay introduced by both sensor

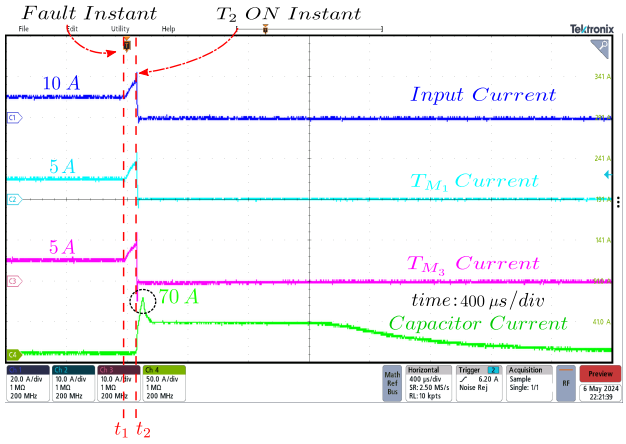



Fig. 12: Experimental result showing total input current, current sharing between two branches and capacitor discharge current during fault interruption by TB-SSCB.

and microcontroller, the SCR $T_2$ turns on at the instant $t_2$ as provided in Fig. 10. Then, the capacitor discharges the stored energy into the winding $L_2$. Due to the induction principle, an EMF produced on the winding $L_1$ opposes the bus voltage and aids in bringing the SCR current down to zero instantly. After a short reverse recovery process, the SCR begins to block the DC bus voltage, and the fault current is cut off. Meanwhile, the capacitor resonates with the winding $L_2$ while discharging, and the resistance of the path $C \rightarrow T_2 \rightarrow D_2 \rightarrow L_2$ prevents the capacitor from swinging down to the negative voltage as observed from the above result.

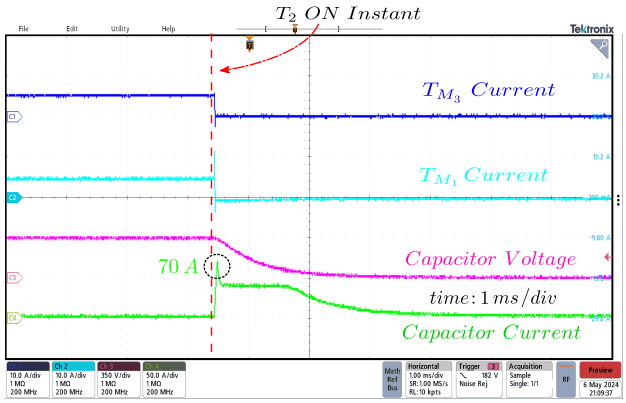



Fig. 13: Experimental result showing manual tripping of TB-SSCB by triggering $T_2$ from the steady-state operation for 350 V, 10 A system.

### B. Results and Discussion for TB-SSCB Topology

An additional branch was added in parallel to the main path as described in Fig. 6(a) to make the circuit breaker compatible with high-current applications. The inductor winding $L_3$ is designed with the same number of turns as the winding $L_1$ with almost the same diameter and length to obtain self-inductance of 250 $\mu$H. All three windings, $L_1$, $L_3$, and $L_2$, are distributed coaxially along the length of the solenoid cylinder on top of each other for the best mutual coupling. The performance of this topology is also validated for a total current of 10 $A$ shared between the two parallel branches. The proposed two-branch topology requires only one current sensor that senses the total current and the preset trigger value is set to 20 $A$. The capacitor is charged to 350 V DC with the same procedure followed in single-branch topology. Then two main thyristors $T_{M_1}$ and $T_{M_3}$ are triggered. It is observed from the experimental result shown in Fig. 11 that the total current 10 $A$ is shared, and each branch carries approximately 5 $A$. Then, the load current starts increasing gradually from the instant $t_1$, as shown in Fig. 11. It is observed that the current starts to increase in both branches with almost the same slope. When the total current reaches 20 $A$, as shown in Fig. 12, SCR $T_2$ is triggered to initiate the fault interruption process by the similar principle discussed in the previous subsection. After the recovery of the stored charge carriers of the two main thyristors, they start to block the input voltage as seen in Fig. 11. The system settles after approximately 700 $\mu$s. The steady-state operation of the breaker can be interrupted in both SB-SSCB and TB-SSCB for carrying out maintenance activities by just triggering the thyristor $T_2$. This feature is validated experimentally, as shown in Fig. 13.

### C. Power Loss and Efficiency Estimation of the Proposed Circuit Breakers

The major contributors into power loss in the proposed circuit breaker are thyristors and winding coils in the main current path as they continuously carry full load current. The power loss in auxiliary components used in the commutation circuit can be avoided since they come into action only during fault events, which occur for a short time interval. In SB-SSCB, only one thyristor $T_{M_1}$ and winding $L_1$ contribute to the power loss in steady state. In the prototype, a thyristor from Vishay with part number 40TPS12A is used for the experimental validation. It has a forward voltage drop of 0.9 V, and for a system current of 10 A, the conduction loss in SCR is estimated to be about 9 W. The power loss in winding $L_1$ due to its resistance dissipates as heat and affects efficiency of the circuit breaker. The total winding resistance from the designed coil is found to be 120 m$\Omega$, and the power loss calculated according to $i_{L_1}^2 * R_{L1}$ is 12 W. The total power loss incurred by SB-SSCB for a system rating of 350 V and 10 A is 21 W. Therefore, the efficiency of SB-SSCB is estimated at 99.4 %. Since TB-SSCB contains an additional branch (two branches and share an equal current of 10A), the total power loss and efficiency are found to be 42 W and 99.4 %, respectively for a system rating of 350 V and 20 A.

### D. Cost Analysis of Proposed Circuit Breakers

The main contributors to the cost of the proposed circuit breakers are thyristors ($T_{M_1}$, $T_{M_2}$, $T_1$, $T_2$, $T_3$ and $T_4$), Diodes ($D_1$ and $D_2$), capacitor, coupled inductor, current sensor, gate drivers for the thyristors, control and communication cards. The active components used in commutation circuits are selected in such a way that they have high surge current capability but a limited nominal current rating. When extending the topology to modularity, only power branch components increase, as a single commutation circuit is used for two branches. The cost of the components is listed in the Table. II. Although the cost of film capacitors used in the prototype is slightly higher than electrolytic capacitors, film capacitors life can reach 2 or 3 times that of aluminum electrolytic capacitors, providing a better and reliable performance.

TABLE II: Cost of the proposed SB-SSCB and TB-SSCB.

| Topology | SB-SSCB | TB-SSCB |
|---|---|---|
| SCRs | 40TPS12A<br>Total 6-$43.62 | 40TPS12A<br>Total 7-$50.89 |
| Diodes | FR607<br>Total 2, $1.08 | FR607<br>Total 2, $1.08 |
| Capacitor | EZPV60117MTC<br>Total 8, $181.44 | EZPV60117MTC<br>Total 8, $181.44 |
| Coupled Coils | custom made<br>$3 | custom made<br>$3.8 |
| Current Sensor | LA 55-P, $37.16 | LA 55-P, $37.16 |
| SCR Trigger Circuits | custom made, $20 | custom made, $25 |
| Controller | MSP430FR2355<br>$17.27 | MSP430FR2355<br>$17.27 |
| **Total Cost** | **$303.57** | **$316.64** |

## V. Comparative Study

The proposed SB-SSCB and TB-SSCB circuit breakers in this paper are compared with the recent bidirectional SCR-based SSCBs present in the literature. The comparison is based on the number of semiconductor and passive devices and commutation circuits required for each topology. Also, the comparison is extended to advantageous features such as protection from permanent faults, capability for rebreaking, conduction losses, controlled and automatic tripping, and provision for adjustable fault current trip level among different topologies. The merits and drawbacks of the proposed DCCBs are discussed in this section and are summarized in the TABLE. III.

TABLE III: Comparision of different bidirectional SCR-based DCCBs.

| **Topologies based on different Commutation Techniques** | **ZSCB** | | **Capacitor based** | | | | **Coupled Inductor based** | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | [33] | [34] | [35] | [36] | [37] | [31] | [30] | [28] | [29] | **SB-SSCB** | **TB-SSCB** |
| Number of switches (SCR, diode, IGBT, mechanical contactor) and energy absorbers | 6, 0 | 8, 0 | 6, 0 | 9, 2 | 6, 1 | 7, 0 | 8, 1 | 6, 0 | 3, 0 | 8, 0 | 10, 0 |
| Number of capacitors | 1 | 2 | 2 | 2 | 1 | 1 | 2 | 2 | 1 | 1 | 1 |
| Number of inductors(1) | 1 CI | 2 CI | 2 | 0 | 0 | 0 | 1 CI | 1 CI | 1 CI | 1 CI | 1 CI |
| Number of resistors | 1 | 4 | 2 | 3 | 2 | 1 | 1 | 2 | 0 | 2 | 2 |
| Modularity | No | No | No | No | No | Yes | No | No | Yes | No | Yes |
| Number of commutation circuits (for two modules) | - | - | - | - | - | 2 | - | - | 2 | - | 1 |
| Rebreaking | No | Yes | No | No | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Pre-commissioning faults protection | No | Yes | No | No | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Controlled tripping | No | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Automatic tripping | Yes | Yes | No | No | No | No | No | Yes | No | No | No |
| Adjustable fault current trip level | Yes | Yes | No | No | No | No | Yes | Yes | Yes | Yes | Yes |
| Efficiency(2) | ⋆ | ⋆⋆ | ⋆⋆ | ⋆⋆⋆ | ⋆⋆ | ⋆⋆⋆ | ⋆⋆⋆ | ⋆⋆ | ⋆ | ⋆⋆⋆ | ⋆⋆⋆ |

(1) CI: Coupled inductor, (2) Efficiency is estimated based on the number of semiconductor switches and coupled inductor windings in the main conduction path.

The SB-SSCB and TB-SSCB are first compared with the z-source circuit breakers (ZSCBs) proposed in [33], [34]. In [33], the z-source capacitor is charged after every fault interruption. Since there is no path to discharge, this topology does not provide a rebreaking facility and protection against permanent faults. During the commissioning of the breaker, the capacitor charging current flows through the load, which is undesirable. Whenever the main thyristor is triggered to power the load, the capacitor energy is dumped into the SCR, leading to high current stress and increasing the reliability concerns. Also, this topology lacks protection against large impedance faults. In [34], a fault protection strategy is incorporated into a new bidirectional ZSCB to protect against large impedance faults. However, this topology requires two coupled inductors and two capacitors. The bulky coupling inductors and their oversizing to compensate for saturation, along with the low reliability of capacitors, may not be practical for high-power applications in terms of both power density and reliability. In contrast, the proposed SB-SSCB and TB-SSCB overcome all the above-mentioned drawbacks of presented ZSCBs.

The topologies proposed in this paper are compared with capacitor commutation-based bidirectional DCCBs. In [35], [36], the proposed topologies provide a high-frequency path for the capacitor to discharge its energy and help in commutating the thyristor fastly. However, the fault level is not adjustable in these two topologies. This is because the initial voltage on the capacitors needs to be tuned for higher fault current interruptions, which is not possible in the provided configurations. Whereas in SB-SSCB and TB-SSCB, the turns ratio of the inductor can be configured to achieve an adjustable fault current tripping feature [38]. Also, both topologies in [35], [36] do not provide protection against permanent faults or pre-commissioned faults, which is improved in the SB-SSCB and TB-SSCB, where the capacitor can be precharged before triggering the main thyristor after commissioning. Moreover, it can be recharged regularly to compensate for self-discharge during long-term operation without faults. The topologies in [31], [36], [37], do not provide isolation of the source from the faulty section even after turning of the SCR, which can bring up safety concerns. However, the topologies proposed in this paper provide complete isolation of the source from the faulty section after interruption. In [31], the thyristor $T_3$ can be considered as a redundant device because the anti-parallel diodes of the IGBTs $Q_1$ and $Q_4$ provide a way for the capacitor to charge through the load even when the $T_3$ is switched off, which is undesirable during commissioning. In SB-SSCB and TB-SSCB, the capacitor charging is controlled by the thyristors $T_1$ and $T_4$ and has no additional unwanted paths to charge the capacitor.

In [29], the topology has no current limiting resistor during capacitor charging mode, which could damage diode and thyristor that come in the path. In contrast, the SB-SSCB and TB-SSCB have a current limiting resistance designed to ensure that the peak current is within the limits and below the peak current rating of SCRs. The circuit breakers proposed in [28], [30] do not provide fast load side interruption as the energy is still dissipated to the fault even after the turn-off of the main SCR. In [29], [31], authors proposed a modular design to handle high current applications. However, each module requires a commutation circuit and a current sensor to perform fault interruption. With the introduction of three winding air-core coupled inductors, the proposed TB-SSCB can perform modular operation with a single commutation circuit and current sensor, which results in a drastically reduced component count.

### *A. Potential Challenges and Drawbacks of the Proposed Topologies*

Since the coupled inductor used in the proposed circuit breaker is designed without a magnetic core, it exhibits a higher conduction loss as the length of the wire for a given inductor increases, thereby increasing resistance in the main path. On the other hand, the high AC resistance of coils helps to provide over damping during the capacitor discharge, ensuring its reliable operation. Moreover, air-core magnetics cannot saturate during fault conditions. The proposed topology also poses a space constraint due to the increased physical

dimensions of coupled coils. However, the concept of modularity reduces current per module and thus losses, as well as the size/weight of passive components per module.

## VI. Conclusion

This article introduces the new SB-SSCB and TB-SSCB topologies envisioned for DC buildings. The proposed topologies include air-core-coupled inductors to prevent saturation at high current levels while ensuring reliable current breaking during both short-circuit and large impedance faults. Moreover, the proposed DCCB concept enables modular implementation, making this technology easily scalable to different power levels. The TB-SSCB can interrupt the fault current in both parallel branches with a single commutation circuit, reducing the component count. This paper provides a comprehensive overview of the operational modes of the two topologies, an in-depth analysis, and a detailed circuit design. The proposed topologies are experimentally validated for a system voltage of 350 V DC and a current of 10 A (nominal current), with a fault current set at 20 A. A comprehensive review of existing competing solutions shows that the proposed breakers provide a unique set of features suitable for residential and commercial DC buildings. Some concerns about the size of air-core inductors could be raised, which require further optimization to improve power density.

## References


[1] IEA, "Technology and innovation pathways for zero-carbon-ready buildings by 2030, iea," IEA, Paris, 2022. [Online]. Available: https://www.iea.org/reports/technology-and-innovation-pathways-for-zero-carbon-ready-buildings-by-2030

[2] O. Abdel-Rahim, A. Chub, D. Vinnikov, and A. Blinov, "Dc integration of residential photovoltaic systems: A survey," *IEEE Access*, vol. 10, pp. 66 974–66 991, 2022.

[3] E. Rodriguez-Diaz, J. C. Vasquez, and J. M. Guerrero, "Intelligent dc homes in future sustainable energy systems: When efficiency and intelligence work together," *IEEE Consumer Electronics Magazine*, vol. 5, no. 1, pp. 74–80, 2016.

[4] H. Mehrjerdi, R. Hemmati, M. Shafie-khah, and J. P. S. Catalão, "Zero energy building by multicarrier energy systems including hydro, wind, solar, and hydrogen," *IEEE Transactions on Industrial Informatics*, vol. 17, no. 8, pp. 5474–5484, 2021.

[5] D. J. Becker and B. Sonnenberg, "Dc microgrids in buildings and data centers," in *2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC)*, 2011, pp. 1–7.

[6] D. Kumar, F. Zare, and A. Ghosh, "Dc microgrid technology: System architectures, ac grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects," *IEEE Access*, vol. 5, pp. 12 230–12 256, 2017.

[7] A. Sannino, G. Postiglione, and M. Bollen, "Feasibility of a dc network for commercial facilities," *IEEE Transactions on Industry Applications*, vol. 39, no. 5, pp. 1499–1507, 2003.

[8] T. R. de Oliveira, A. S. Bolzon, and P. F. Donoso-Garcia, "Grounding and safety considerations for residential dc microgrids," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 5526–5532.

[9] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "Dc microgrid protection: A comprehensive review," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2019.

[10] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "Dc microgrids—part ii: A review of power architectures, applications, and standardization issues," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3528–3549, 2016.

[11] A. Ray, K. Rajashekara, and S. N. Banavath, "Bidirectional coupled inductor based hybrid circuit breaker topologies for dc system protection," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 1138–1145.

[12] S. Zheng, R. Kheirollahi, J. Pan, L. Xue, J. Wang, and F. Lu, "Dc circuit breakers: A technology development status survey," *IEEE Transactions on Smart Grid*, vol. 13, no. 5, pp. 3915–3928, 2022.

[13] M. Saeedifard, M. Graovac, R. Dias, and R. Iravani, "Dc power systems: Challenges and opportunities," in *IEEE PES General Meeting*, 2010, pp. 1–7.

[14] T. Jalakas, S. N. Banavath, A. Chub, I. Roasto, and D. Vinnikov, "Performance analysis of protection methods in residential dc microgrids," in *2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2023, pp. 1–6.

[15] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 364–377, 2021.

[16] X. Song, P. Cairoli, Y. Du, and A. Antoniazzi, "A review of thyristor based dc solid-state circuit breakers," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 659–672, 2021.

[17] K. A. Corzine and R. W. Ashton, "A new z-source dc circuit breaker," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2796–2804, 2012.

[18] A. H. Chang, A.-T. Avestruz, S. B. Leeb, and J. L. Kirtley, "Design of dc system protection," in *2013 IEEE Electric Ship Technologies Symposium (ESTS)*, 2013, pp. 500–508.

[19] V. R. I, S. N. Banavath, and S. Thamballa, "Modified z-source dc circuit breaker with enhanced performance during commissioning and reclosing," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 910–919, 2022.

[20] D. J. Ryan, H. D. Torresan, and B. Bahrani, "A bidirectional series z-source circuit breaker," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7609–7621, 2018.

[21] A. Pogulaguntla, V. Raghavendra I, S. N. Banavath, A. Chub, T. Sreekanth, and H. S. Krishnamoorthy, "Bidirectional dc circuit breaker with improved performance during commissioning and reclosing," in *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, 2022, pp. 1–9.

[22] S. G. Savaliya and B. G. Fernandes, "Modified bi-directional z-source breaker with reclosing and rebreaking capabilities," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 3497–3504.

[23] L. Yi and J. Moon, "Bidirectional q-z-source dc circuit breaker," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9524–9538, 2022.

[24] Z. Zhou, J. Jiang, S. Ye, D. Yang, and J. Jiang, "Novel bidirectional o-z-source circuit breaker for dc microgrid protection," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1602–1613, 2021.

[25] Y. Yang and C. Huang, "A low-loss z-source circuit breaker for lvdc systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 3, pp. 2518–2528, 2021.

[26] Y. Wang, W. Li, X. Wu, and X. Wu, "A novel bidirectional solid-state circuit breaker for dc microgrid," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5707–5714, 2019.

[27] X. Xu, J. Ye, Y. Wang, X. Xu, Z. Lai, and X. Wei, "Design of a reliable bidirectional solid-state circuit breaker for dc microgrids," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 7200–7208, 2022.

[28] X. Diao, F. Liu, Y. Zhuang, S. Pan, and X. Zha, "A bidirectional efficient circuit breaker with automatic and controllable shutoff functions for dc distribution network," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 8, pp. 7988–7999, 2023.

[29] I. V. Raghavendra, S. N. Banavath, C. N. M. Ajmal, and A. Ray, "Modular bidirectional solid-state dc circuit breaker for next-generation electric aircrafts," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 5, pp. 5486–5497, 2022.

[30] Y. Wang, S. Wang, C. E. Ugalde-Loo, W. Ming, and W. Li, "Low-loss bidirectional solid-state circuit breakers with reliable breaking capability for protecting dc microgrids," *IEEE Transactions on Power Electronics*, vol. 38, no. 12, pp. 16 118–16 129, 2023.

[31] S. Nandakumar, I. V. Raghavendra, C. N. M. Ajmal, S. N. Banavath, and K. Rajashekara, "A modular bidirectional solid-state dc circuit breaker for lv and mvdc grid applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 7760–7771, 2022.

[32] Pratik, Ujjwal and Pantic, Zeljko, "Design of Variable Air-Core Coupled Co-axial Solenoidal Inductors," in 2022 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1–6, 2022.

[33] Z. Zhou, Y. Fei, Y. Li, Y. Wang, Y. Liu, and W. Li, "Circuit modeling and experimental validation of a bidirectional z-source circuit breaker based on coupled inductors," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 6, pp. 6242–6252, 2024.

[34] Y. Wang, Y. Tao, S. Wang, C. E. Ugalde-Loo, W. Ming, and W. Li, "A fault protection strategy based on z-source solid state circuit breaker for more electric aircraft," *IEEE Transactions on Transportation Electrification*, pp. 1–1, 2023.
[35] V. Raghavendra I, B. S. Naik, T. Sreekanth, and A. Chub, "Controlled bidirectional dc circuit breaker with zero negative current for high load shift applications," *IEEE Transactions on Industry Applications*, vol. 58, no. 6, pp. 6942–6951, 2022.
[36] R. Kheirollahi, S. Zhao, X. Zan, H. Zhang, X. Lu, J. Wang, A.-T. Avestruz, and F. Lu, "Fast y-type thyristor-based dc sscb using complementary commutation in a capacitor–capacitor pair structure," *IEEE Transactions on Power Electronics*, vol. 38, no. 1, pp. 1144–1154, 2023.
[37] M. Marwaha, K. Satpathi, M. H. M. Sathik, J. Pou, C. J. Gajanayake, A. K. Gupta, D. Molligoda, and R. K. Surapaneni, "Scr-based bidirectional circuit breaker for dc system protection with soft reclosing capability," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 5, pp. 4739–4750, 2023.
[38] K. A. Corzine, "A new-coupled-inductor circuit breaker for dc applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1411–1418, 2017.

**Aditya Pogulaguntla** (Member, IEEE) received the B.Tech. degree in electrical and electronics engineering from Velagapudi Ramakrishna Siddhartha Engineering College, India in 2021 and the M.S. degree in electrical engineering from Indian Institute of Technology Dharwad, India, in 2024. His current research interests include power electronic converters for transportation electrification systems and solid-state dc circuit breakers.

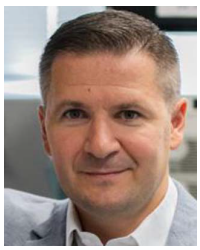
**Daniel Dsa** (Student Member, IEEE) received the M.E degree in electrical engineering from the University of Mumbai, India, in 2018. He is currently working toward the Ph.D. degree in electrical engineering with the Indian Institute of Technology Dharwad, Karnataka, India. His research interests include power electronics, solid-state dc circuit breakers, WBG-based modular power converters for transportation electrification, and software and hardware embedded systems.

**Venkata Yagna Griddaluru** received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Dharwad (IIT Dharwad), Karnataka, India, in 2024. He is currently pursuing the Ph.D. degree with the Holcombe Department of Electrical and Computer Engineering, Clemson University, Clemson, SC, USA. During his B.Tech. studies, he was with the Power Electronics Laboratory of Prof. Banavath. His interests are DC microgrids and Electric Vehicle Systems.

**Satish Naik Banavath** (Senior Member IEEE) received the B.Tech. degree in electrical and electronics engineering from Acharya Nagarjuna University, Guntur, India, in 2010. He received the M.E. and Ph.D. degrees in electrical engineering from the Indian Institute of Science, Bengaluru, India, in 2012 and 2018, respectively. From 2012 to 2014, he was with Defence Research and Development Organization (DRDO), Ministry of Defence, Government of India, Bengaluru, India. He was a Postdoctoral Fellow at the University of Houston, Houston, TX, USA, from September 2017 to May 2018. Later, he joined Mahindra Electric Mobility Limited, Bengaluru, where he served as a Research and Development Manager from July 2018 to January 2019. He is currently working as an Assistant Professor with the Department of Electrical Engineering at the Indian Institute of Technology (IIT) Dharwad, Dharwad, Karnataka where he joined in February 2019. His current research interests include multilevel power converters, power converters for renewable energy conversion, electric vehicles, and DC circuit breakers.

**Edivan Laercio Carvalho** (Senior Member IEEE) received the B.Sc. and M.Sc. degrees from the Federal University of Technology - Parana (UTFPR), Pato Branco, Brazil, in 2015, and 2018, respectively, and the Ph.D. degree from Federal University of Santa Maria (UFSM), Santa Maria, Brazil, in 2021, all in electrical engineering. He is currently a Researcher with the Power Electronics Group, Tallinn University of Technology, Tallinn, Estonia. His research interests include high-frequency power converter topologies, netzero energy buildings, and power management systems.

**Andrii Chub** (Senior Member IEEE) received the B.Sc. and M.Sc. degrees in electronic systems from Chernihiv State Technological University, Chernihiv, Ukraine, in 2008 and 2009, respectively, and the Ph.D. degree in electrical engineering from Tallinn University of Technology, Tallinn, Estonia, in 2016. He is currently a Senior Researcher with the Power Electronics Group, Tallinn University of Technology. His research interests include advanced dc–dc converters, energy-efficient buildings, reliability, and fault-tolerance of power electronic converters.



**Dmitri Vinnikov** (Fellow, IEEE) received the Dipl.Eng., M.Sc., and Dr.Sc.techn. degrees in electrical engineering from Tallinn University of Technology, Tallinn, Estonia, in 1999, 2001, and 2005, respectively. He is currently the Head of the Power Electronics Group, Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology. Moreover, he is one of the founders and leading researchers of ENER—Estonian Centre of Excellence in Energy Efficiency. He has authored or coauthored two books, five monographs, and one book chapter as well as more than 400 published articles on power converter design and development, and he is the holder of numerous patents and utility models in this field. His research interests include the applied design of power electronic converters and control systems, renewable energy conversion systems (photovoltaic and wind), impedance-source power converters, and the implementation of wide bandgap power semiconductors. Dr. Vinnikov is the Chair of the IEEE Estonia Section.