EE1200 - ELECTRIC CIRCUITS LAB

Experiment-9

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Contents

1 Aim

The objective of this experiment is to build a sequence detector, that detects the sequence of **11011** by using a **Moore machine** .

2 Apparatus Required

- 7474 D flip-flops
- 7432 2-input OR gates
- 7411 3-input AND gates
- LED
- Connecting wires
- Breadboard
- An Ardino UNO
- Resistor (220Ω)

3 Theory

A Moore machine is a finite-state machine where the output depends solely on the current state. Key characteristics include:

- **States**: A finite set of states.
- **Input Alphabet**: A set of input symbols.
- **Output Alphabet**: A set of output symbols.
- **State Transition Function**: Maps current state and input to the next state.
- **Output Function**: Maps current state to an output symbol.

Formally, a Moore machine is defined as:

$$M = (Q, \Sigma, \Lambda, \delta, \omega, q_0)$$

where Q is the set of states, Σ is the input alphabet, Λ is the output alphabet, δ is the state transition function, ω is the output function, and q_0 is the initial state.

Advantages:

- Simplicity and stability in output.
- Useful in digital circuit design and control systems.

Disadvantages:

- May require more states compared to Mealy machines.
- Output changes occur one clock cycle after state change.

4 State diagram

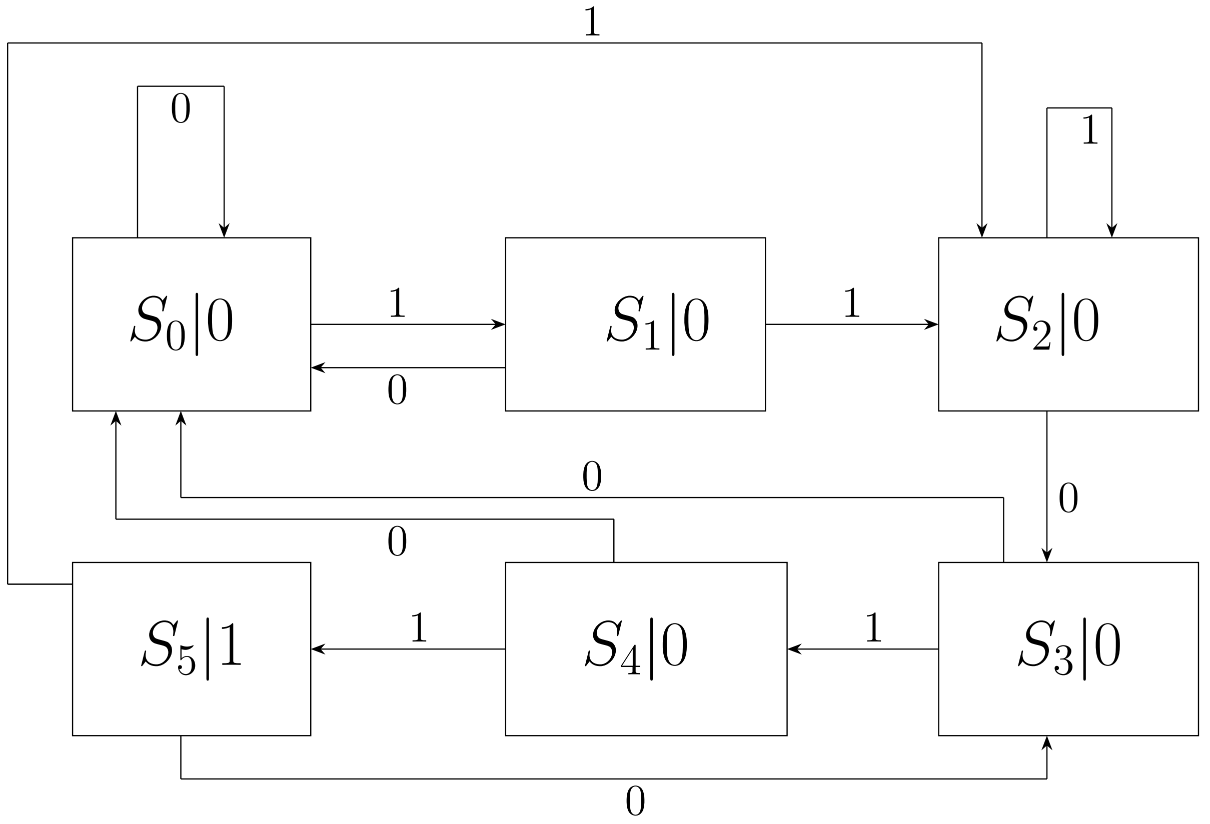

Figure 1: State Diagram

5 State transition table

- The given sequence, **11011** has 5 bits. Hence, the required number of states is 6 and the required number of flip-flops to implement this circuit is three.
- Let us assign the following binary values to each state -
- The state-transition table using T flip-flops is given below.
- The corresponding logic is given below -
- The state transition table using D flip-flops is given below -

State	**Binary value**
S_0	000
S_1	001
S_2	011
S_3	010
S_4	110
S_5	111

Table 1: State values

Input	P_2	P_1	P_0	T_2	T_1	T_0	N_2	N_1	N_0	**Output**
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	1	0
0	0	0	1	0	0	1	0	0	0	0
1	0	0	1	0	1	0	0	1	1	0
0	0	1	1	0	0	1	0	0	1	0
1	0	1	1	0	0	0	0	1	1	0
0	0	1	0	0	1	0	0	0	0	0
1	0	1	0	1	0	0	1	1	0	0
0	1	1	0	1	1	0	0	0	0	0
1	1	1	0	0	0	1	1	1	1	0
0	1	1	1	1	0	1	0	1	0	1
1	1	1	1	1	0	0	0	1	1	1
0	1	0	0	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X
0	1	0	1	X	X	X	X	X	X	X
0	1	0	1	X	X	X	X	X	X	X

Table 2: State transition table - T flip-flops

- The corresponding logic is given below -

- From 3 and 5, it can be seen that using a D flip-flop minimizes the circuit complexity, and hence we shall adopt that.

6 Circuit diagram

7 Procedure

- Connect the circuit according to the figure 2.
- When the circuit reaches the S_5, the LED glows.
- The number of times the sequence **11011** appears can be found out by noting the number of times the LED lights up.

State	**Logic**
T_2	$Q_2Q_0 + \overline{I}Q_2 + I\overline{Q_2}Q_1\overline{Q_0}$
T_1	$\overline{Q_1}Q_0I + Q_1\overline{Q_0}\,\overline{I}$
T_0	$Q_0\overline{I} + \overline{Q_1}\,\overline{Q_0}I + IQ_2\overline{Q_0}$
O	$Q_0Q_1Q_2$

Table 3: Logic - T flip-flops

Input	P_2	P_1	P_0	D_2	D_1	D_0	N_2	N_1	N_0	**Output**
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	1	0	1	1	0
0	0	1	1	0	0	1	0	0	1	0
1	0	1	1	0	1	1	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0
1	0	1	0	1	1	0	1	1	0	0
0	1	1	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1	0	1
1	1	1	1	0	1	1	0	1	1	1
0	1	0	0	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X
0	1	0	1	X	X	X	X	X	X	X
0	1	0	1	X	X	X	X	X	X	X

Table 4: State transition table - D flip-flops

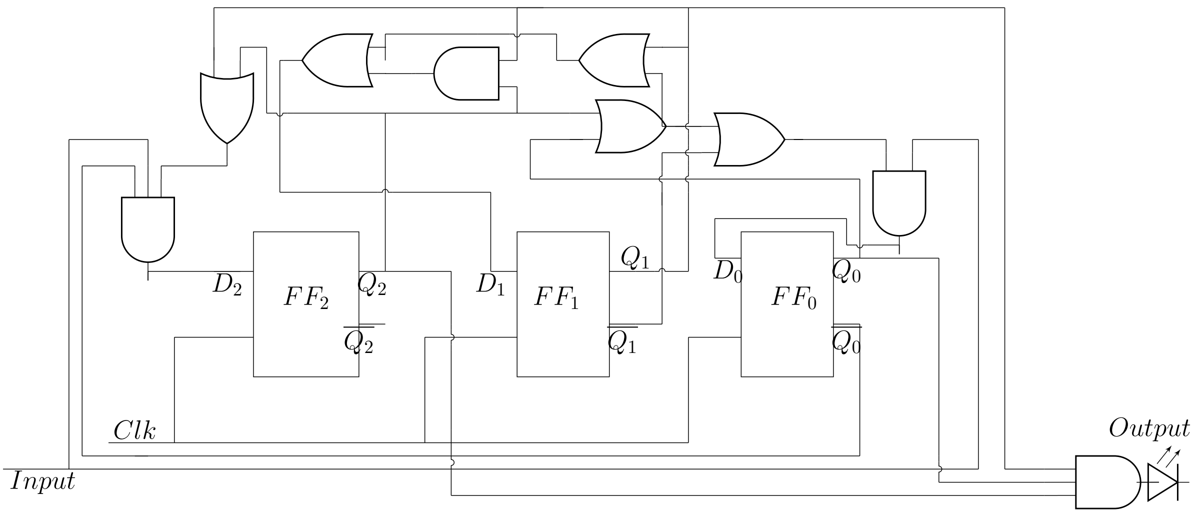

Figure 2: Circuit diagram

8 Observation

- The simulated diagram is attached herewith -

State	Logic
D_2	$D\overline{Q_0}(Q_1+Q_2)$
D_1	$D(Q_0+Q_1+Q_2)+Q_1Q_0$
D_0	$D(Q_0+Q_2+\overline{Q_1})$
O	$Q_0Q_1Q_2$

Table 5: Logic - D flip-flops

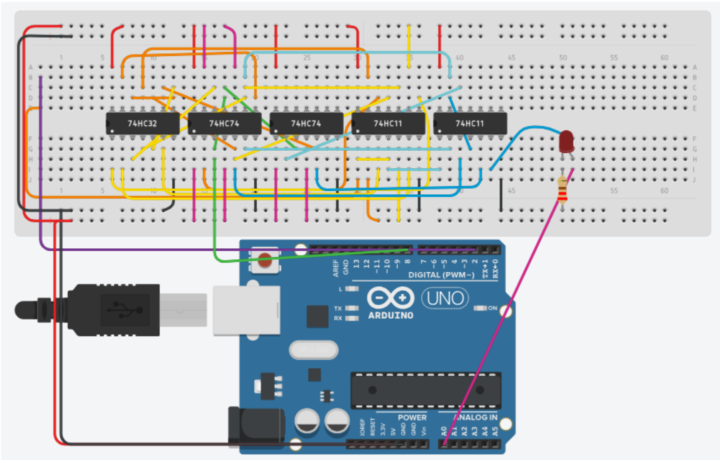

Figure 3: Simulated diagram

- It can be seen that the LED glows 4 times, in an interval of 3 seconds for the bit sequence **11011011011011011** and 5 seconds for the first time to glow, in one cycle.
- This can be explained by the nature of the functioning of the Moore machine. When the circuit reaches S_5, the LED lights up, which can be seen from the circuit diagram.

9 Result

Hence, the sequence detector circuit has been constructed using logic gates and D-flip-flops, by a finite state machine (FSM) .