EE1200 - ELECTRIC CIRCUITS LAB
Experiment-8

EE24BTECH11012 - Bhavanisankar G S
EE24BTECH11019 - Dwarak A

April 13, 2025

Contents

1 Objective

The objective of this project is to design and implement a digital counter that keeps track of the number of people in a mess facility. The counter increments when a person enters and decrements when a person exits. The circuit should be built using basic logic gate ICs and JK flip-flops in a synchronous configuration, ensuring accurate, reliable, and glitch-free operation.

2 Components Used

- AND, OR, NOT Gates (IC 7411, 7432, 7404)
- JK Flip-Flops (IC 7476)
- Seven Segment Display (Common Cathode)
- BCD to 7-Segment Decoder (IC 7447)
- Push Buttons (for simulating entry and exit)
- Resistors (1kΩ, 10kΩ)
- Breadboard, Connecting Wires
- 5V Power Supply (from Arduino UNO)

3 Theory

3.1 Synchronous Counters

Synchronous counters use a common clock signal for all flip-flops, resulting in more predictable and synchronized state transitions compared to asynchronous counters. Each flip-flop changes state based on the inputs and the common clock edge.

3.2 JK Flip-Flops

JK Flip-Flops are versatile and can function as T flip-flops or D flip-flops based on how inputs are connected. In counters, they toggle when both J and K are high. The toggling condition is crucial for building up/down counters.

3.3 Logic Gate ICs

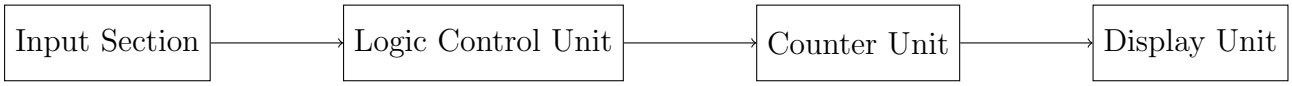
- **7411 (AND gate)** – Provides logical AND operations.
- **7432 (OR gate)** – Provides logical OR operations.
- **7404 (NOT gate)** – Provides logical inversion.

These gates are used to generate control signals for counting and ensure that entry and exit signals do not conflict.

3.4 Debouncing and Input Conditioning

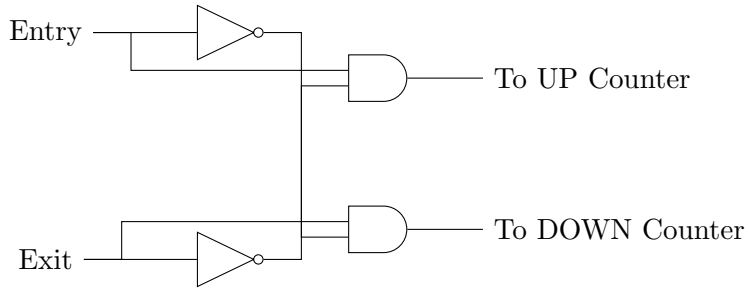
Mechanical buttons often produce bouncing effects, resulting in multiple transitions. This can be filtered using SR latches or simple RC debouncing circuits. For the purpose of this experiment, rapid pressing is avoided and basic logic gates are used to control invalid transitions.

3.5 Block Diagram



Functional Block Diagram of the Mess Counter

3.6 Logic Control Circuit



Logic Gate Circuit Ensuring Mutual Exclusion of Entry and Exit

3.7 Truth Table and Logic Expressions

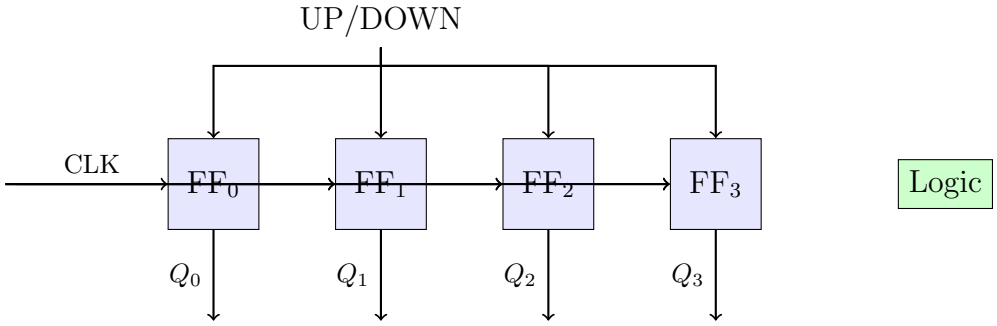
Entry (E)	Exit (X)	UP	DOWN
0	0	0	0
1	0	1	0
0	1	0	1
1	1	0	0

Table 1: Truth Table for Logic Control

Raw Logic Expressions:

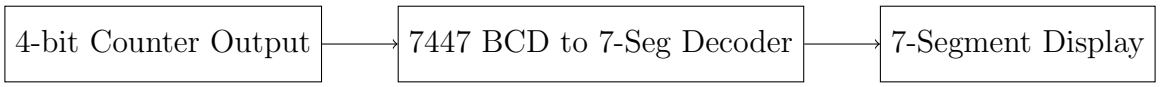
- UP = E $\cdot$ $\overline{X}$
- DOWN = X $\cdot$ $\overline{E}$

3.8 Counter Circuit



(Figure: Synchronous 4-bit Up/Down Counter using JK Flip-Flops)

3.9 Display Decoder Circuit



(Figure: Interfacing Counter Output with Display)

3.10 Circuit Description

The circuit is composed of the following major parts:

1. **Input Section:** Two push buttons are used—one for entry and one for exit. These generate control signals for counting.
2. **Logic Control Unit:** Logic gates ensure that only one action (increment or decrement) occurs at a time. If both buttons are pressed simultaneously, no change is registered.
3. **Counter Unit:** A 4-bit synchronous up-down counter is built using JK Flip-Flops. Entry signals cause an up count, and exit signals cause a down count.
4. **Display Unit:** The output of the counter is fed into a 7447 BCD to 7-segment decoder which drives a common cathode display.

4 Truth Table

Entry	Exit	Action	Count (Before)	Count (After)
0	0	No Change	N	N
1	0	Increment	N	N+1
0	1	Decrement	N	N-1
1	1	Invalid (No Change)	N	N

Table 2: Truth Table for Entry/Exit Logic

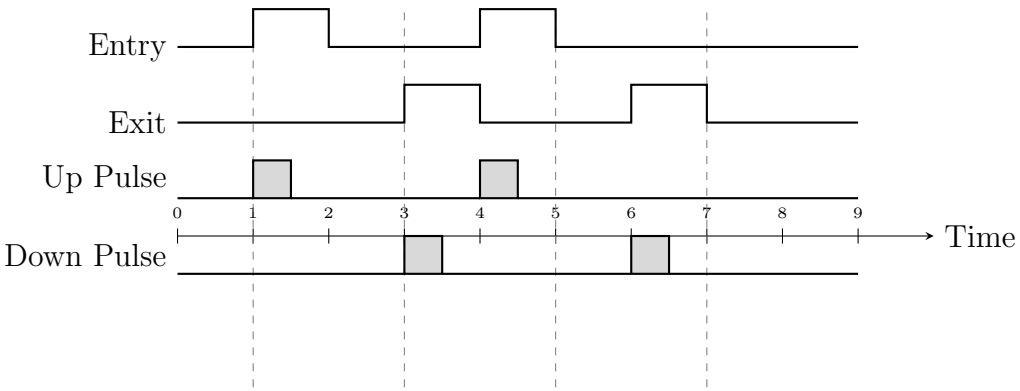


Figure 1: Timing diagram showing Entry, Exit, and corresponding counter pulses

4.1 Timing Diagram

4.2 Derivation of Logic

Below are the state tables and Karnaugh map derivations for both the up and down counter modes.

State Tables

Up Counter State Table:

Present State				T Flip-Flops				Next State			
Q_3	Q_2	Q_1	Q_0	T_3	T_2	T_1	T_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	1	0	0	1	0
0	0	1	0	0	0	0	1	0	0	1	1
0	0	1	1	0	1	1	1	0	1	0	0
0	1	0	0	0	0	0	1	0	1	0	1
0	1	0	1	0	0	1	1	0	1	1	0
0	1	1	0	0	0	0	1	0	1	1	1
0	1	1	1	1	1	1	1	1	0	0	0
1	0	0	0	0	0	0	1	1	0	0	1
1	0	0	1	1	0	0	1	0	0	0	0
1	0	1	0	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X

Table 3: State table for the single-digit BCD Up-counter. (X denotes don't-care conditions.)

Down Counter State Table:

Present State				T Flip-Flops				Next State			
Q_3	Q_2	Q_1	Q_0	T_3	T_2	T_1	T_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	1	0	0	1	1	0	0	1
0	0	0	1	0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	1	1	0	0	1	1
0	1	0	1	0	0	0	1	0	1	0	0
0	1	1	0	0	0	1	1	0	1	0	1
0	1	1	1	0	0	0	1	0	1	1	0
1	0	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	0	0	1	1	0	0	0
1	0	1	0	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X

Table 4: State table for the single-digit BCD Down-counter. (X denotes don't-care conditions.)

Karnaugh Maps for T Flip-Flops

Up Counter T Flip-Flops

For T_0:
Since $T_0 = 1$ for all cases, no Karnaugh map is required.

For T_1:

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	X	X	X	X
10	0	0	X	X

Thus,

$$T_1 = \overline{Q_3}\, Q_0.$$

For T_2:

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	X	X	X	X
10	0	0	X	X

Thus,

$$T_2 = Q_1\,Q_0.$$

For T_3:

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	0	1	X	X

Thus,

$$T_3 = Q_2\,Q_1\,Q_0 + Q_3\,Q_0.$$
$$T_3 = Q_2\,T_2 + Q_3\,Q_0$$

Down Counter T Flip-Flops

For T_0:
Again, $T_0 = 1$ for all cases.

For T_1:

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

Thus,

$$T_1 = Q_1\,\overline{Q_0} + Q_2\,\overline{Q_1}\,\overline{Q_0} + Q_3\,\overline{Q_1}\,\overline{Q_0}.$$
$$T_1 = Q_1\,\overline{Q_0} + T_2$$

For T_2:

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	X	X	X	X
10	1	0	X	X

Thus,

$$T_2 = Q_2\,\overline{Q_1}\,\overline{Q_0} + Q_3\,\overline{Q_1}\,\overline{Q_0}.$$

For T_3:

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	X	X	X	X
10	1	0	X	X

Thus,

$$T_3 = \overline{Q_2}\,\overline{Q_1}\,\overline{Q_0}.$$

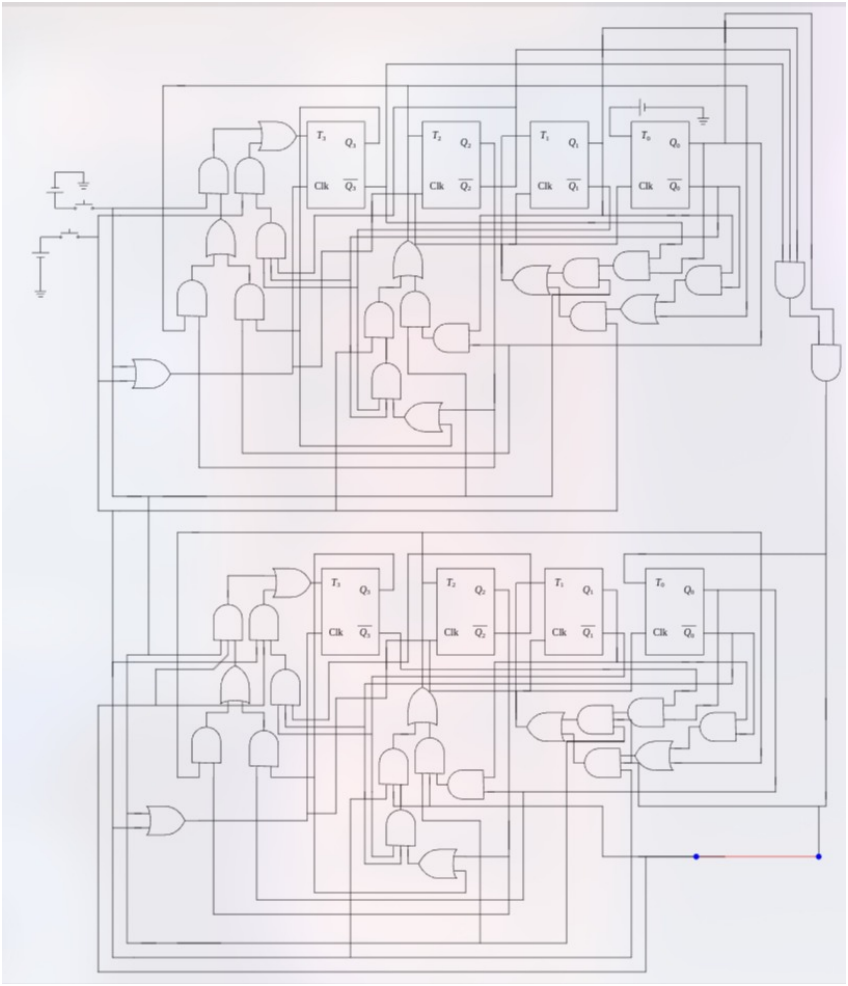


Figure 2: Complete circuit

5 Procedure

5.1 Circuit Connections

The detailed connections between components are as follows:

- **Input Circuit:**
  - Entry push button connected to +5V with a 10kΩ pull-down resistor
  - Exit push button connected to +5V with a 10kΩ pull-down resistor
- **Logic Control Unit:**
  - IC 7411 (AND gate):
    - Pin 1 & 2 (inputs) connected to Entry button and inverted Exit signal
    - Pin 3 (output) gives Up count signal
    - Pin 4 & 5 (inputs) connected to Exit button and inverted Entry signal
    - Pin 6 (output) gives Down count signal
    - The other input in both the cases is connected to V_{cc}
  - IC 7404 (NOT gate):
    - Pin 1 (input) connected to Exit button
    - Pin 2 (output) connected to AND gate for Up count
    - Pin 3 (input) connected to Entry button
    - Pin 4 (output) connected to AND gate for Down count
- **JK Flip-Flop Counter:**
  - For each 7476 JK Flip-Flop:
    - J and K inputs connected to control logic based on up/down counting
    - Clock inputs connected to common clock signal
    - Q outputs connected to next flip-flop's control logic
    - $\overline{Q}$ outputs used for control logic
  - For up counting: Each flip-flop toggles when all previous flip-flops are at logic 1
  - For down counting: Each flip-flop toggles when all previous flip-flops are at logic 0
- **Display Unit:**
  - IC 7447 BCD to 7-segment decoder:
    - Pins 7, 1, 2, 6 (A, B, C, D inputs) connected to Q0, Q1, Q2, Q3 of counter
    - Pins 13, 12, 11, 10, 9, 15, 14 (a-g outputs) connected to 7-segment display
  - 7-segment display:
    - Common cathode connected to ground through a 220Ω resistor
    - Segments connected to decoder outputs through 330Ω current-limiting resistors

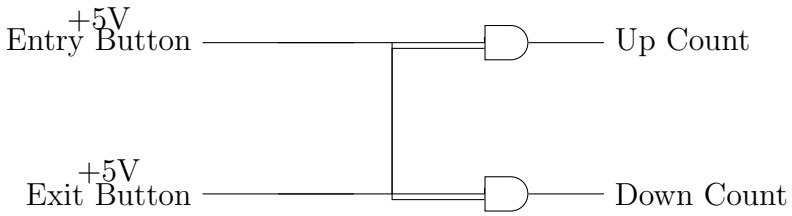


Figure 3: Detailed Logic Control Circuit Connections

6 Observations and Results

- Initial state is 0000 (0 count).
- Each press of the entry button increases count by 1.
- Each press of the exit button decreases count by 1.
- Simultaneous press of both buttons does not affect the count.
- Display reflects the correct count in real-time.
- It is observed that the counter resets the value to 0 and decrementing from 0 results in 99. This is a drawback to this connection.

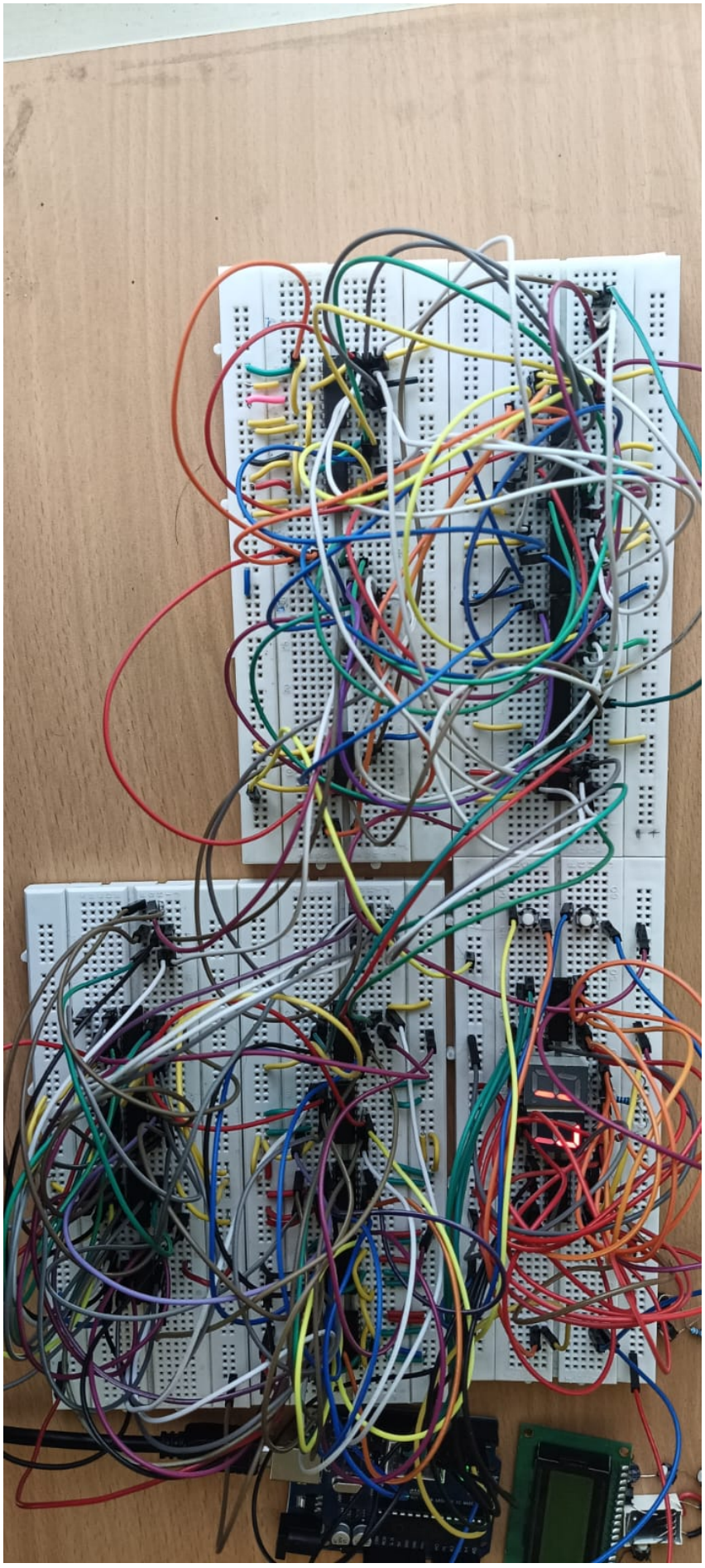


Figure 4: Figure