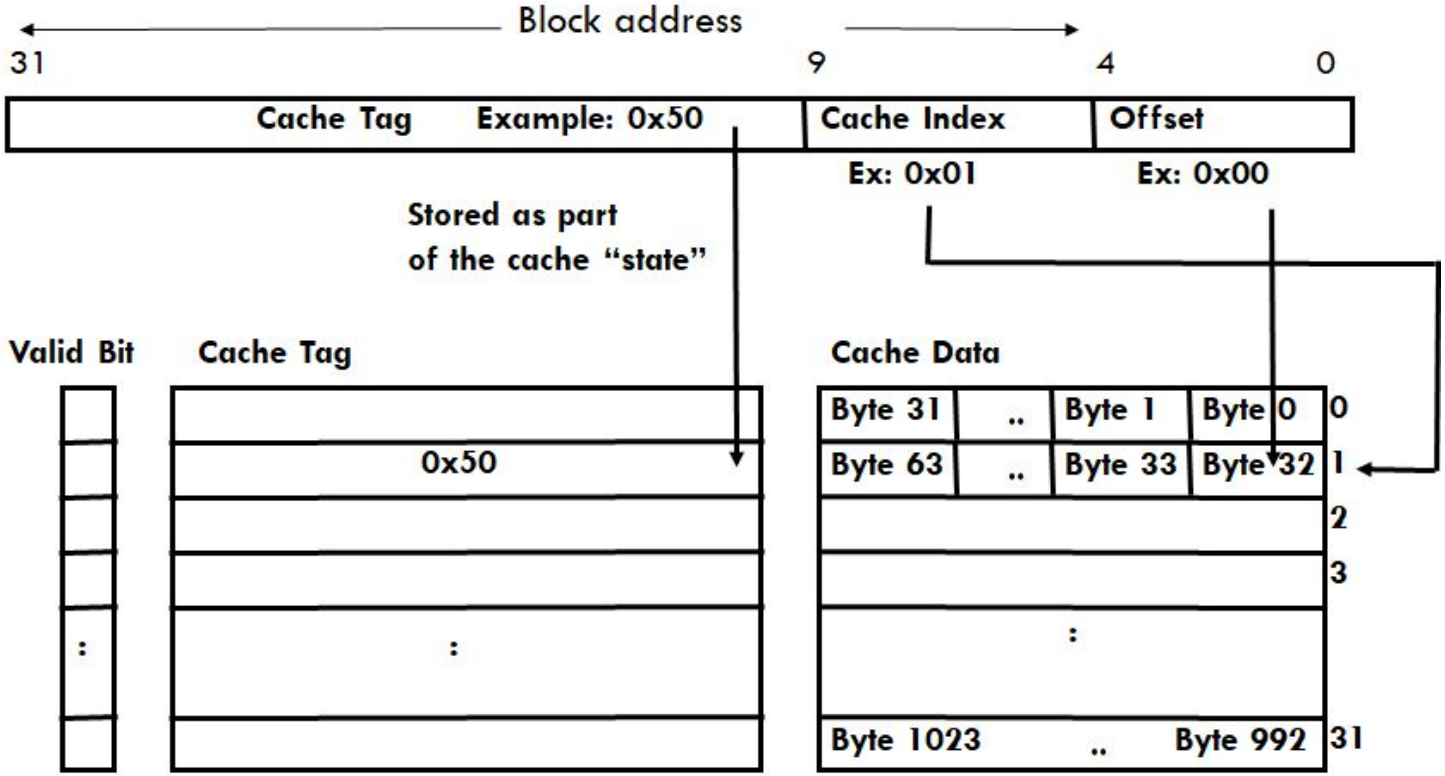
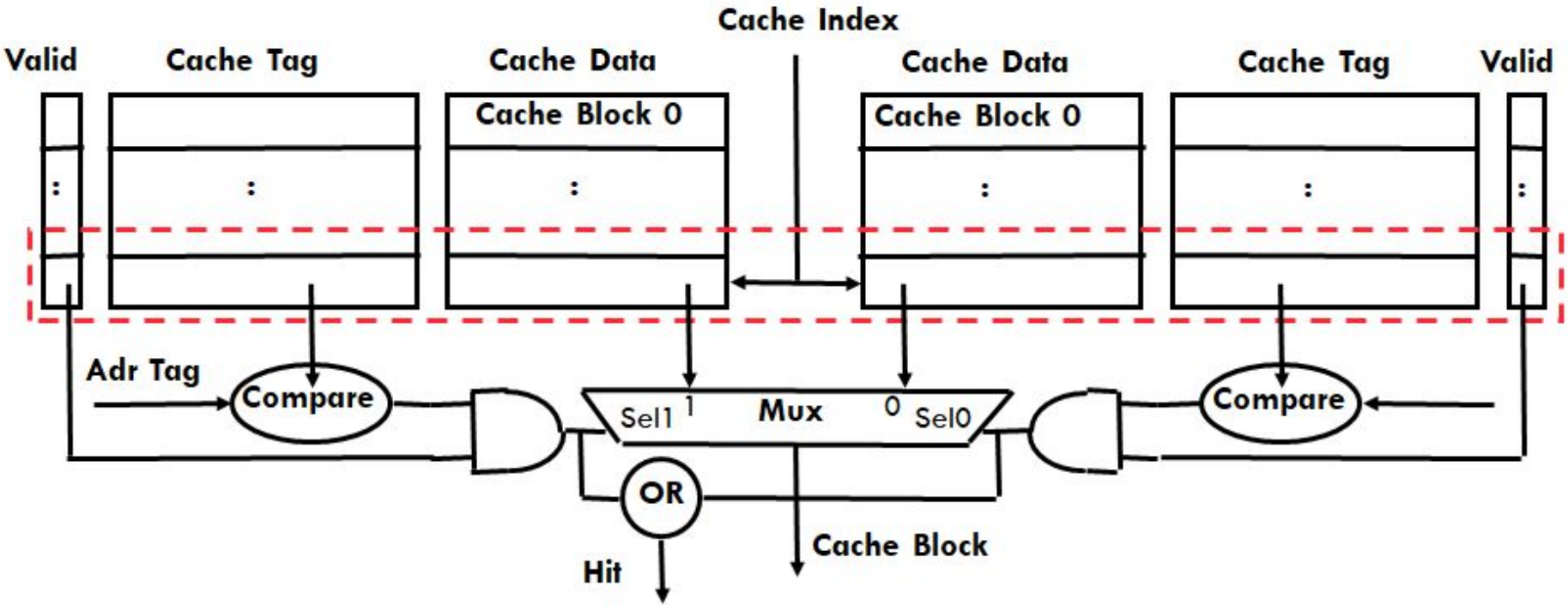
Discussion 14

Caches, FIFOs, DRAMs, Clocking, Parallelism, Pipelining

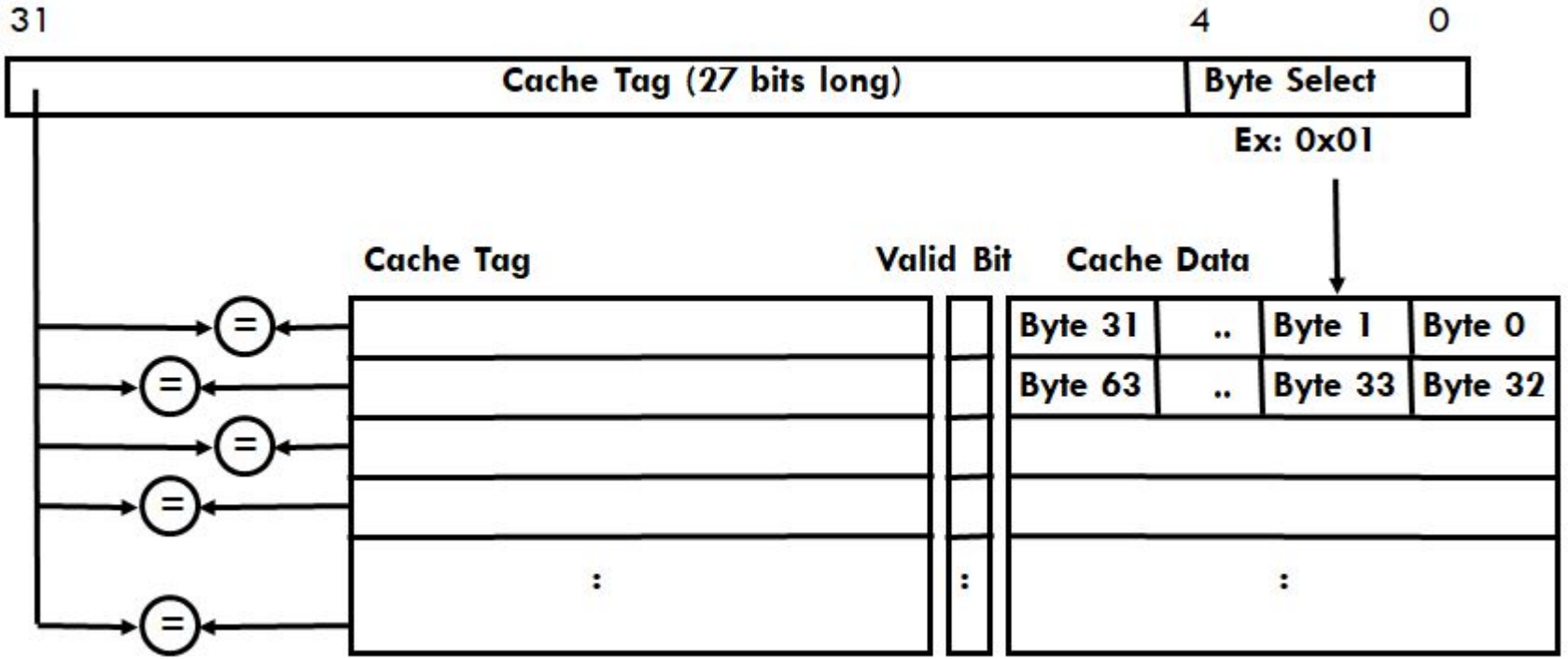
Caches - Direct Mapped



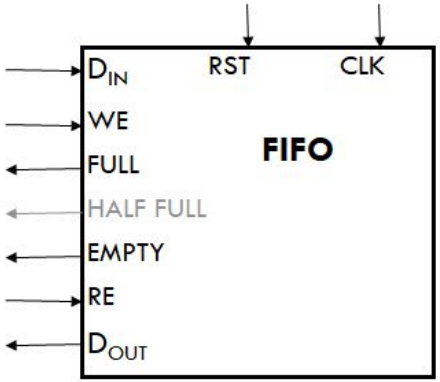
Caches - N-Way Set Associative



Caches - Fully Associative

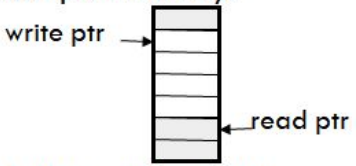


FIFO Interfaces

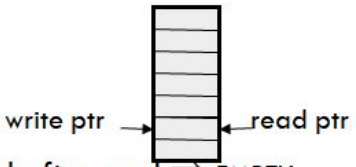


- After write or read operation, FULL and EMPTY indicate status of buffer.
- Used by external logic to control own reading from or writing to the buffer.
- FIFO resets to EMPTY state.
- HALF FULL (or other indicator of partial fullness) is optional.

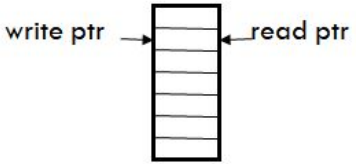
- Address pointers are used internally to keep next write position and next read position into a dual-port memory.



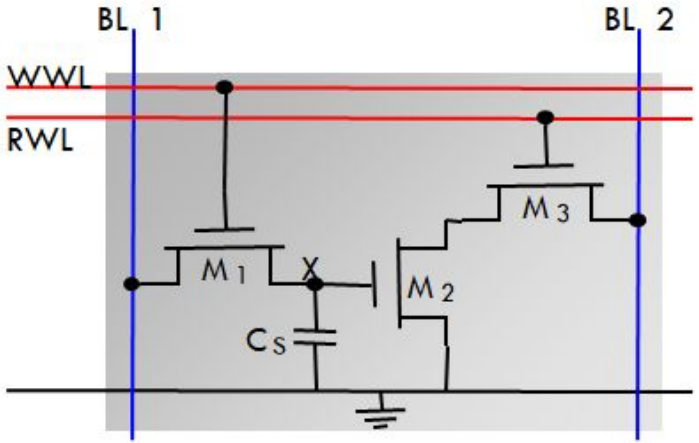
- If pointers equal after write $\Rightarrow$ FULL:

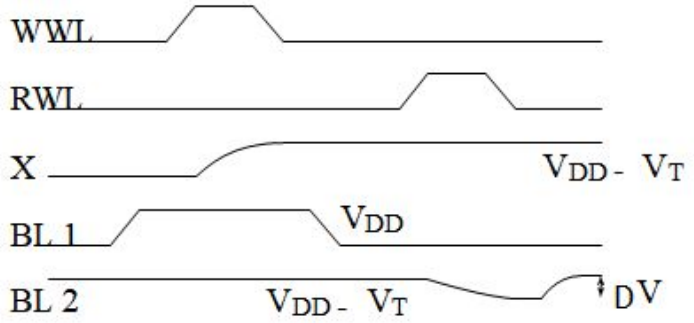


- If pointers equal after read $\Rightarrow$ EMPTY:



3T DRAM

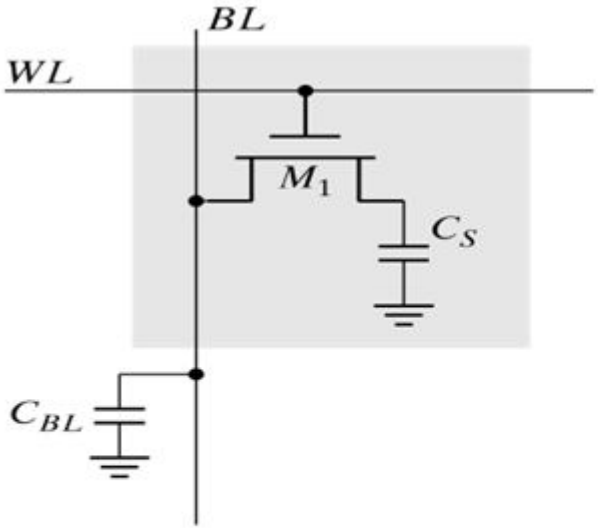


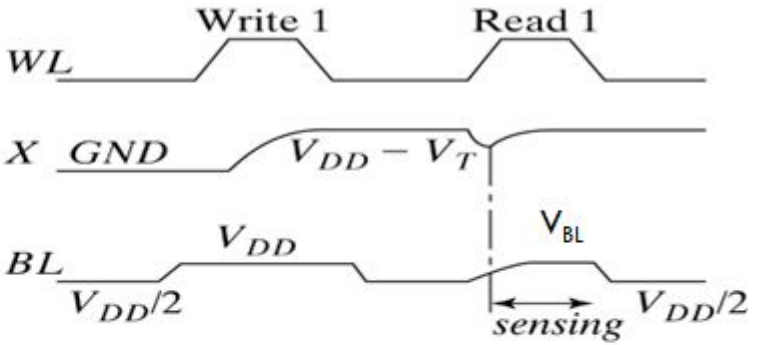


No constraints on device ratios
Reads are non-destructive
Value stored at node X when writing a "1" = $V_{WWL} - V_{Th}$

Can work with a logic IC process

1T DRAM



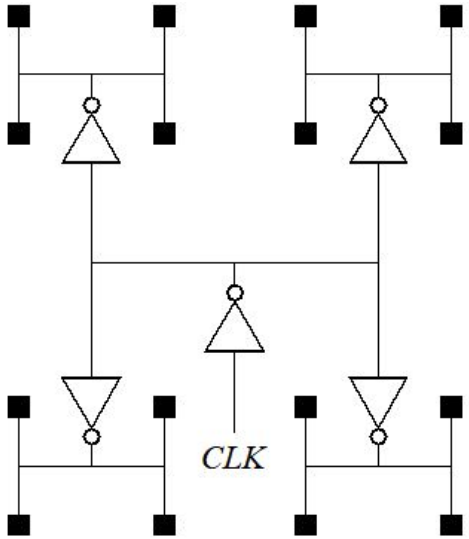


V_{BIT}= 0 or ($V_{DD} - V_T$)

Write: C S is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes places between bit line and storage capacitance

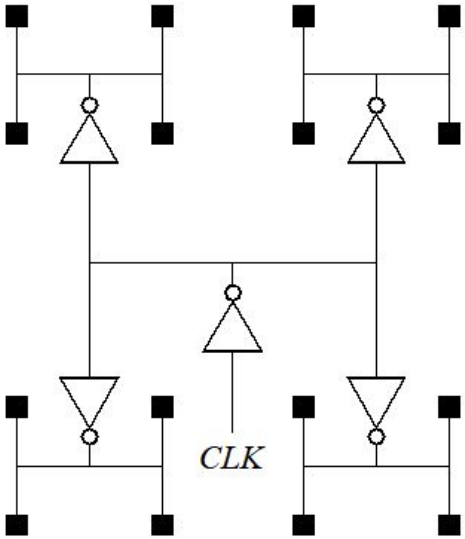
$C_S << C_{BL}$ Voltage swing is small; typically hundreds of mV.

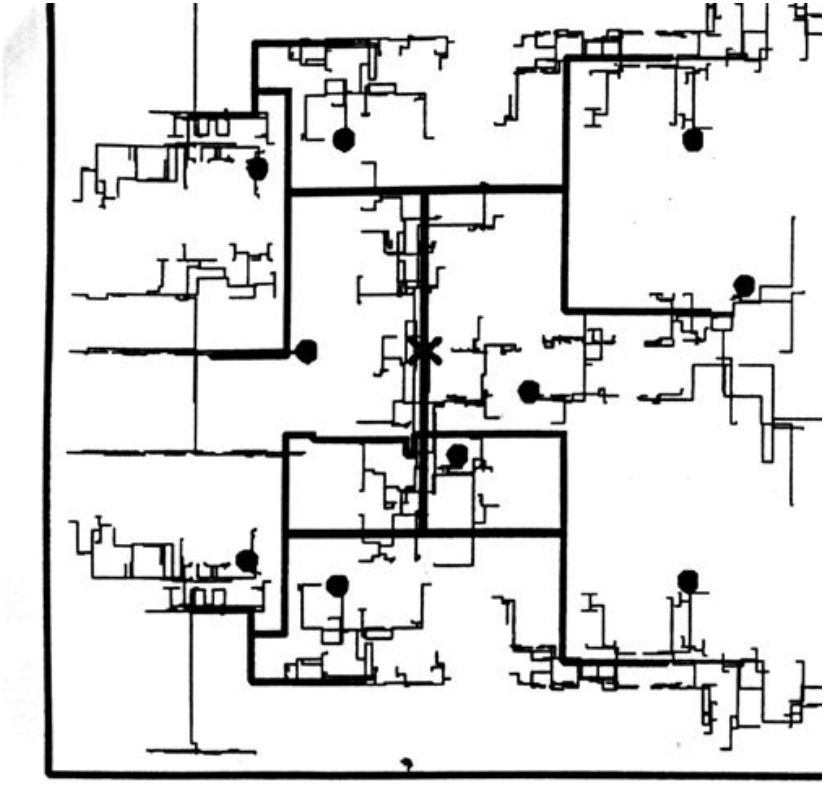
Clock Distribution



Clock is distributed in a tree-like fashion
Large chips (blocks) – many levels of buffers
Goal minimize skew, supply-induced jitter

Clock Distribution





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Parallelism

Pipelining