EECS 151/251A Homework 7

Due Monday, March 18th, 2024

Introduction

This homework is meant to test your understanding of the basic principles of transistor sizing, capacitive loads, and their impact on performance of digital circuit.

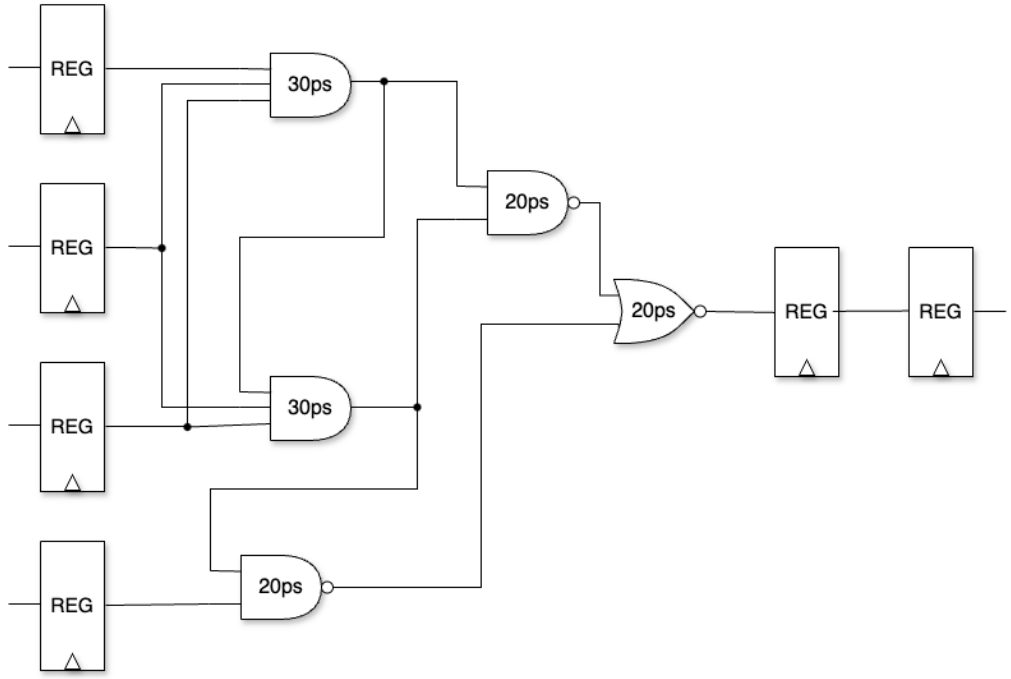
Problem 1: Transistor Sizing

Suppose you are given the layout information for some particular mobile integrated circuit (IC) developed with a planar process. A new technique you learned allows for you to change the size of all the transistors without making any other changes to the layout. Smaller transistors might mean less area consumed for your design, and therefore, less cost to manufacture the IC. However, the transistor sizing also impacts the performance of your circuit. Answer the following questions regardless the impact of transistor sizing on the performance:

1. Explain the impact of transistor sizing on the maximum clock frequency in general (i.e. how does the frequency change with larger transistors? how does the frequency change with smaller transistors?). Why does the clock frequency change due to transistor size?
2. Now assume you decide to "compact" the design to take advantage of the area savings from smaller transistors after decreasing the size of all the transistors. Explain now what would be the overall effect on frequency from the original design.
3. After shrinking the transistors, you realized one gate has a larger fanout (ex. an electrical fanout of 10, the output is connected to the input of 10 other gates). How could you compensate now that you have decreased the transistor size?

Problem 2: Retiming

Consider the circuit shown below. Assume all timing characteristics for the flip-flops are $10ps$ (i.e $t_{clk \to q}$, t_{setup}, and t_{hold} times). The delay for the gates are written within each gate symbol. *Ignore wire delay in this problem.*



(a) What is the maximum clock frequency (f_{max}) for this circuit?

(b) Without optimizing the logic, but only by retiming the circuit, now what is the new f_{max}? Draw your retimed circuit.

(c) The simplest form of retiming does not allow the addition of extra registers (i.e the latency does not increase). With pipelining you add registers to long delay paths to increase clock frequency, but also can increase latency. Take the pipelining approach. What would be the best f_{max} you can achieve by adding an arbitrary number of new registers?

Problem 3: CMOS Circuits Driving a Load

Consider a CMOS circuit in which a single NFET is used to pull the output capacitance from V_{DD} to 0 volts (as in an inverter). This circuit is driving a capacitive load. Sketch, on the same axis, the voltage on the output capacitence as a function of time assuming two different models for the transistor discussed in lecture: (1) transistor model as a simple resistor and (2) the non-linear model shown in the lecture notes.

Problem 4: Rise and Fall

Consider a NOR gate, NOR(a,b), designed for a planar CMOS process. For this problem, we will assume that all transistors in the gate (all PFETs and all NFETs) are designed to the same physical width. On a single set of axis, and with modeling the transistors as resistors, draw rough waveforms for output transitions based on the following input values. The table below shows the input values over time:

Time	a	b
0	1	1
1	0	0
2	0	1
3	0	0
4	1	1

Problem 5: Just in Time

Assume the critical path in our design is through the next state logic of a FSM. The registers we used have t_{clk-q} = t_{setup} = 280ps, and t_{hold} = 556ps. The delay through the combinational logic t_{CL} = 4ns. We set the clock period T = 5ns. Answer the questions below:

1. Will this circuit function correctly? If not, what can we change to correct it without a lose of performance? What the maximum frequency you can run the circuit at? Make sure to show your work.
2. A colleague points out another path between two registers (of the same type as in the critical path) except t_{CL} = 200ps. Why is this bad? What can you do to fix this issue?

Problem 6: Electrical Fanout

Suppose we have a unit sized inverter, with input capacitance of $10fF$ and an intrinsic delay of $2ps$, that needs to drive a large capacitance of $6pF$. Assume for this process, $\gamma = 1$.

(a) Calculate the delay of this single inverter driving the large capacitance.

(b) Using staged buffers, calculate the optimal number of stages, and the total delay. Show your work.

Problem 7: Delay through Chain of Inverters

Suppose we have three inverters daisy chained together. The wire between the first and second inverters is 100μm and the wire between the second and third inverters is 5μm. All inverters are of the same size and have input capacitance of 10 fF, internal capacitance of 10 fF, and effective pullup and pulldown resistance of 1kΩ. Both wires have a characteristic capacitance of 1 $fF/\mu m$ length and a characteristic resistance of 0.1 Ω/μ length.

(a) Calculate the delay from the first inverter turning on completely to when the input to the third inverter reaches $V_{DD}/2$.

(b) Without resizing transistors, what can you do to reduce this delay?

(c) Approximately, what improvement could you achieve?