EECS 151/251A Homework 10

Due Monday, April 27$^{\text{th}}$, 2021

For this Homework

Please include a short (1-2 sentence) explanation with your answer, unless otherwise noted.

Problem 1: Binary Incrementer

A straightforward way to implement a binary incrementer $(x+1)$ is to use an adder and a register. While this does achieve the result we desire, an adder is a very expensive circuit to implement for such a simple operation. Design an incrementer circuit that performs an N-bit binary increment combinationally.

Problem 2: Counters

Using binary counters with a count enable (`ce`) input and terminal count (`tc`) output, design an FSM controller for a 32-bit serial multiplier.

For this problem, turn in

- A state transition diagram

- A circuit diagram implementing the next state logic and multiplier. You may represent the counters as blocks.

- A short explanation of your design

Problem 3: Adders

Design a 16-bit Carry Look-Ahead adder using 4 4-bit ripple stages. Show a detailed circuit diagram.

Problem 4: More Adders

Write out the expression for the MSB of the sum of an 8-bit Brent-Kung adder, in terms of the sub-expressions of the other nodes in the adder.

Problem 5: Multipliers

For the following multiplier/muliplicand pairs, show the long-hand calculation for mulitplication using the method(s) indicated. All multiplications are 4-bit.

(a) Traditional long multiplication

- 5×3
- -3×6
- 5×-4
- -4×-2

(b) Booth Recoding

- 7×5

(c) Baugh-Wooley Method

- 5×3
- -3×6
- 5×-4
- -4×-2

You may explain your steps for the Booth and Baugh-Wooley calculations in place of the short explanation.

Problem 6: Constant Value Multiplication

Design a circuit using full adder cells for an unsigned multiplication that computes $Y = C \cdot X$, where $C = 2159$ and X is an input. Use a minimum number of only full adders, logical shifters, and inverters. (*Hint: Consider the CSD and KCM methods detailed in the lecture*)

Problem 7: Shifters

Design an 8-bit wide logarithmic shifter that performs an arithmetic shift left or right by 0-7 places. The circuit has a 4-bit input: 3 bits to specify the number of places to shift, and 1 bit to specify the direction. You are allowed to use multiplexers implemented using transmission gate logic to create the shifter. Provide a circuit diagram for the overall shifter, as well as a more detailed schematic of the multiplexers that you use. You may represent the multiplexers in your shifter diagram as symbols, but for each type of multiplexer you use, please show separately their implementation at the transistor level.