EECS 151/251A Homework 6

Due Monday, Feb 26th, 2024

Introduction

This homework is meant to exercise your understanding of CMOS circuits. For your submission, please make sure any circuits are drawn with a schematic maker or hand drawn cleanly (include drawings on tablet devices). Also, for clarity, please signify connections between two wires with solder joints (dots where wires are connected, are highly recommended).

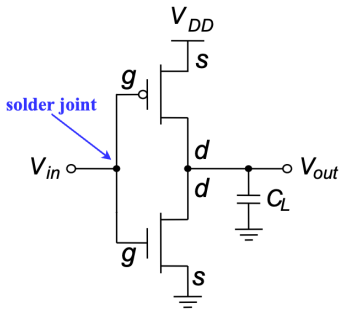
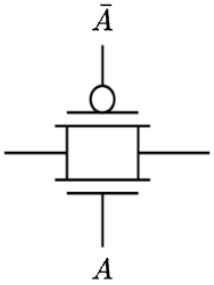


Figure 1: CMOS inverter schematic with solder joints

Problem 1: Static CMOS Circuit

A transmission gate is a simple structure composed of two transistors which operates like a switch. Answer the follow questions to understand their functionality and use.

1. What is the benefit of using a transmission gate compared to a single transistor?
2. Explain in words how a transmission gate functions when a single input and its complement are presented to the NMOS and PMOS gates respectively as shown below.



3. How can a transmission gate be used to tri-state the output of a gate? For example, as with a tri-state buffer?

Problem 2: Flip-Flop with Clock Enable

An implementation of a positive-edge triggered flip-flop using transmission gates was shown in lecture. Unlike many flip-flops used in real-world circuits, it does not have a clock enable. Modify the circuit from lecture to implement a flip-flop with a clock enable (*Hint: There are two ways to do this. Provide one of the two ways*).

Problem 3: Circuit-to-Boolean-to-Verilog

Below we display a schematic for a common function in digital circuits implemented in CMOS.

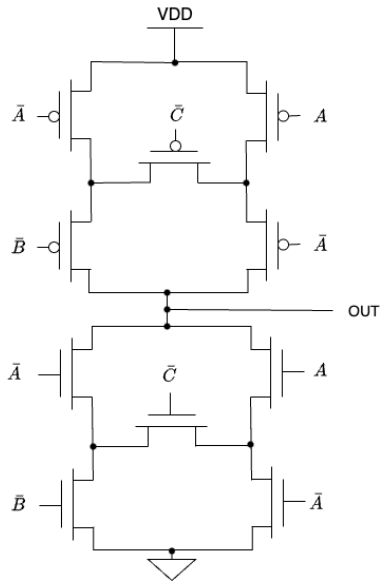


Figure 2: Schematic of CMOS

Complete the following for this circuit:

1. Write its Boolean expression
2. Explain in words what this circuit does
3. Provide a continuous assignment statement representing this circuit.

Problem 4: Layout Practice

Below we present a layout for a five input CMOS circuit. Complete the following:

1. A gate-level schematic of the circuit
2. The Boolean expression for the pull-down network.

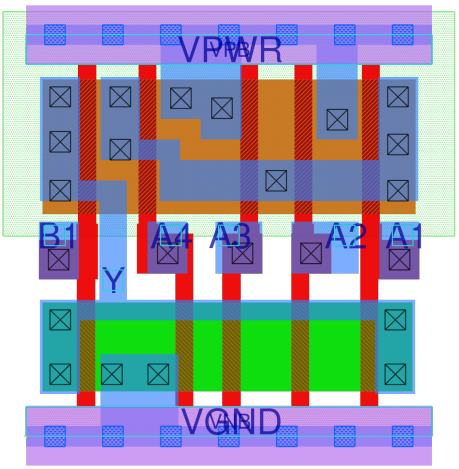


Figure 3: Layout of a unnamed circuit

Problem 5: 4-to-1 Multiplexor with Transmission Gates

Draw gate-level circuit diagram for a tri-state based 4-to-1 multiplexor using no more than four tri-state inverters, along with simple logic-gates, if needed.

Problem 6: Static Circuit

Draw a transistor-level schematic for the Boolean expression $(A + B)(C + D)$ in the "static CMOS style" (as presented in lecture) using the minimal number of transistors. You are not provided with complemented inputs (*Hint: You need to create the complements*).

Problem 7: Negative-Edge Trigged Flip-Flop

Draw the gate-level schematic for a negative-edge triggered flip-flop built using the "Tri-State-Inverter" style latch presented in lecture.