EECS 151/251A Homework 3

Due Monday, Feb 12th, 2024

Introduction

You will be asked to write several Verilog modules as part of this HW assignment. You will need to test your modules by running them through a simulator. We recommend the following free, online Verilog simulator: `https://www.edaplayground.com`.

Important: Use the register library in `EECS151.v` when sequential logic is needed for all of the HW problems.

Problem 1: Parallel to Serial Converter

In lecture, we introduced the parallel to serial converter. This module is defined with the following Verilog code:

Important: Use the register library in `EECS151.v`.

```
module ParToSer(ld, X, out, clk);
    input [3:0] X;
    input ld, clk;
    output out;
    wire [3:0] Q;
    wire [3:0] NS;
    assign NS =
    (ld) ? X : {Q[0], Q[3:1]};
    REGISTER state #(4)
    (.q(Q), .d(NS), .clk(clk));
    assign out = Q[0];
endmodule
```

1. Given the following waveforms for `X`,`ld`, and `clk`, please draw the corresponding waveform for `Q`, `NS`, and `out`.

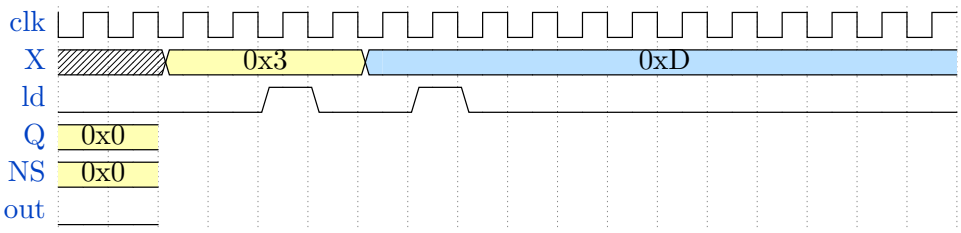

Figure 1: Serial to Parallel Waveform

2. Convert the above module to a generator that has takes as parameter `N` which represents the width of the `X` input.

Problem 2: Up/Down Counter with Powers of 2

We have already seen many examples of counters in lecture. Here we introduce the Up/Down counter, which takes an additional bit `sign`, that determines whether the module counts up (`sign` = 0) or down (`sign` = 1). In addition we introduce a second output `pow2` that outputs 2 raised to the power of the value in the counter. The full specification is defined as follows:

Specification:

- Input: `clk` (the clock signal), `rst` (reset), `en` (enable), and `sign` (up vs. down sign).
- Outputs: 4-bit count named `cnt`, and 16-bit value for the power of two named `pow2`.
- Counters hold the value of `cnt` constant when both `rst` and `en` are 0.
- Counters set `cnt` to 0 on a positive edge of `clk` if `rst` is 1.
- Counters change `cnt` by 1 at a positive edge of `clk` if `rst` is 0 and `en` is 1. If `sign` is 0, the counter will increase the value, if `sign` is 1, the counter will decrement the value.
- When `cnt` is the maximum possible value ($2^4 - 1$ for 4-bit counters), `cnt` will become 0 next time it is incremented. Similarly, when `cnt` is 0, it will become $2^4 - 1$ when next decremented.

1. Based on the specification above, write a Verilog module that behaves as required, but with only the use of one register.
2. Write a second Verilog module that uses 2 registers, one for the counter and a shift register for the power of 2.
3. Write a Verilog testbench that properly drives both modules. Ensure that the clock has a period of 10ns. Make sure to test:
   (a) Every combination of `rst` (reset), `en` (enable), and `sign`.
   (b) The counter going up and down for at least 5 clock periods with no changes to the input signals.
   (c) At 0, the counter should decrement to $2^4 - 1$, and at $2^4 - 1$ the counter should increment to 0.
   (d) On a reset, the counter should go to 0.
   (e) On `en` = 0, the counter value should not change.
   (f) Use the `$monitor` command to output the value of the input and output signals in a single repeating print statement (`$monitor` prints out a statement every time a given signal value changes, so you may find it useful for debugging your counter as well).

   Be sure to include all of the Verilog code you wrote, as well as the output of the `$monitor` command.

Important Note: There are several resources online to help write good test benches, but you can start with the Verilog Primer pdf on the class website. (Note that there is a Primer pdf and Primer slides. Both are helpful but the slides do not go as far into testbenches as you may need.)

Problem 3: Shift Register

A very common hardware structure is a shift register. They appear in many forms in hardware designs, and are an important precursor to pipelined processors.

1. Write a shift register generator with the following specifications:
   (a) 2 Parameters: `N` the bit length of each element (width), and `LEN` length of the shift register (depth)
   (b) Input: `clk`, `rst`, `en`, `ele_in` (a N-bit input to the shift register)
   (c) Output: `ele_out` (the N-bit value which was at the head of the shift register prior to `en` begin asserted)
   (d) Shift register elements are set to `'b0` if `rst` asserted
   (e) `ele_in` is shifted into shift register if `en` is asserted and `rst` is deasserted.
2. Write a Verilog module combining your shift register module with your counter module from Problem 2. Instantiate two shift registers: (1) with `N`=4 and `LEN`=5 and (2) `N`=1 and `LEN`=6. Connect the `cnt` output directly to the `ele_in` input of the first shift register. Write simple combinational logic which outputs '1' if an input is divisible by 4. Connect the `pow2` output to the input of this logic, and the output of the combinational logic to the `ele_in` input of the second shift register.
3. Extra Challenge: Write the above shift register with only a single register!

Problem 4: Combining LUTs

1. Suppose you are only given 4-LUTs (any number of them) and no other modules (this includes simple logic gates such as inverters, ANDs, ORs, etc.). Please draw a diagram showing how you would combine these LUTs to generate a 5-LUT. Remember than a 5-LUT should be able to implement any boolean function on 5 inputs. Provide some justification (truth table, formula, etc.) why your diagram is correct.
2. Extending this, explain how you would generate a (N+1) LUTs from any number of N-LUTs.

Problem 5: LUT Mapping

Given the following circuit (Figure 2) with 5 inputs and 2 outputs:

1. Please determine how many 3-LUTs are needed to fully represent this circuit (this means that the state in every register is equivalent between your LUT-based circuit and the original circuit).

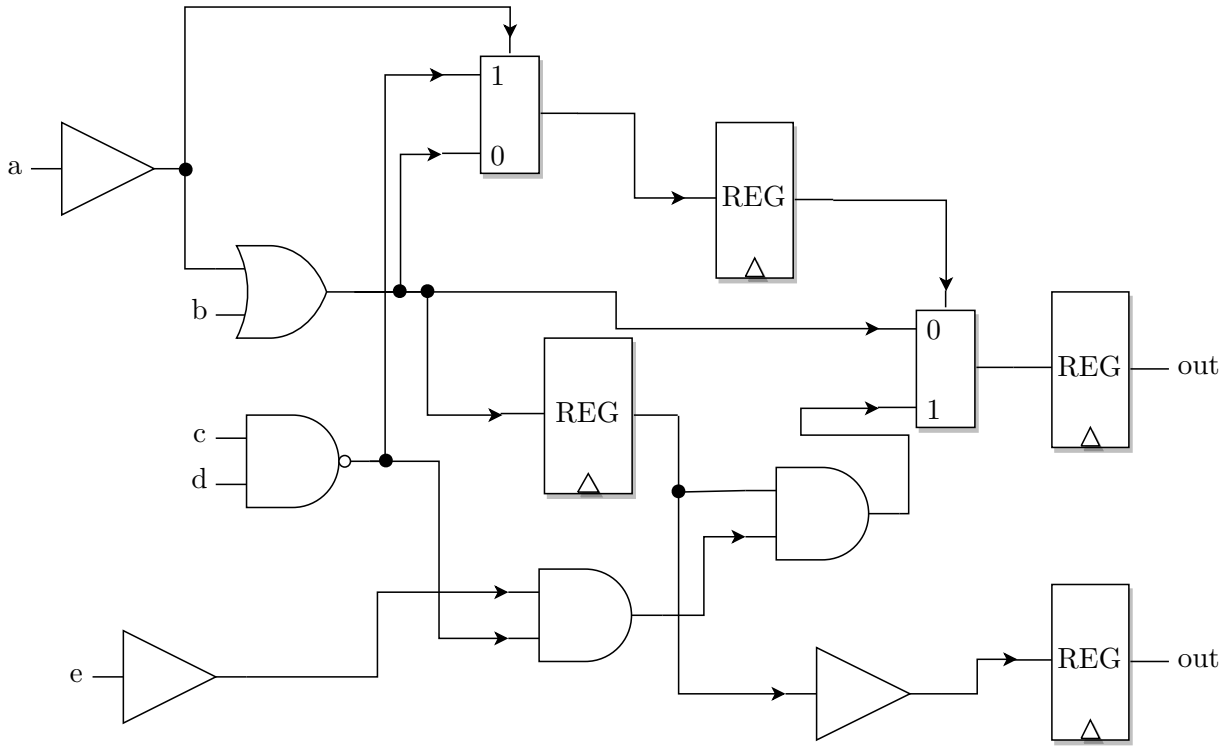

Figure 2: Problem 5 circuit

2. For each LUT, please give the truth table that represents the function the LUT encodes.