

EECS 151/251A FPGA Lab

Lab 3: Simulation, Connecting Modules, and Memories

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1 Before You Start This Lab

Before you proceed with the contents of this lab, we suggest that you look through these two documents that will help you better understand some Verilog constructs.

1. [fpga_labs_fa18/resources/Verilog/wire_vs_reg.pdf](#) - The differences between wire and reg nets and when to use each of them.
2. [fpga_labs_fa18/resources/Verilog/always_at_blocks.pdf](#) - Understanding the differences between the two types of always @ blocks and what they synthesize to.

The first couple sections of this lab focus on simulation and it would be valuable to read these documents before starting.

1.1 Helpful Hint: Synthesis Warnings and Errors

At various times in this lab, things will just not work on the FPGA or in simulation. To help with debugging, you can run the Synthesis step in your project from within Vivado. Have a look at the Synthesis messages that are generated as result. You can view them from the *Project Summary* window or from within the *Synthesized Design* window. Also remember that you can view all toolchain messages by selecting *Window* → *Messages*. Any synthesis warnings you see here could reveal a possible issue in your circuit. If you don't understand a warning, ask a TA.

2 Lab Overview

In this lab, we will begin by taking your configurable frequency `tone_generator` design from Lab 2 and simulating it in software. We will learn how to use ModelSim and/or Vivado to view waveforms and debug your circuits. You will then construct a module that can pull tones to play from a memory block and send them to your `tone_generator`.

3 Simulating the `tone_generator` from Lab 2

3.1 Copying Your Lab 2 Code

Run `git pull` in your git cloned `fpga_labs_fa18` directory to fetch the latest skeleton files.

Begin by copying your `tone_generator` implementation into the `lab3/lab3.srcs/sources_1/new/tone_generator.v` file.

Let's run some simulations on the `tone_generator` in software. To do this, we will need to use a Verilog testbench. A Verilog testbench is designed to test a Verilog module by supplying it with the inputs it needs (stimulus signals) and testing whether the outputs of the module match what we expect.

3.2 Overview of Testbench Skeleton

Check the provided testbench skeleton in `lab2/tone_generator_testbench.v` to see the test written for the `tone_generator`. Let's go through what every line of this testbench does.

```
`timescale 1ns/1ns
`timescale (simulation step time)/(simulation resolution)
```

The timescale declaration needs to be at the top of every testbench file. It provides information to the circuit simulator about the timing parameters of the simulation.

The first argument to the timescale declaration is the simulation step time. It defines the chunks of discrete time in which the simulation should proceed. In this case, we have defined the simulation step time to be one nanosecond. This means that we can advance the simulation time by as little as 1ns at a time.

The second argument to the timescale declaration is the simulation resolution. In our example it is also 1ns. The resolution allows the simulator to model transient behavior of your circuit in between simulation time steps. For this lab, we aren't modeling any gate delays, so the resolution can equal the step time.

```
`define SECOND 1000000000
`define MS 1000000
// The SAMPLE_PERIOD corresponds to a 44.1 kHz sampling rate
`define SAMPLE_PERIOD 22675.7
```

These are some macros defined for our testbench. They are constant values you can use when writing your testbench to simplify your code and make it obvious what certain numbers mean. For example, `SECOND` is defined as the number of nanoseconds in one second. The `SAMPLE_PERIOD` is the sampling period used to sample the square wave output of the `tone_generator` at a standard 44.1 kHz sample rate.

```
module tone_generator_testbench();
    // Testbench code goes here
endmodule
```

This module is a testbench module. It is not actually synthesized to be placed on an FPGA, but rather it is to be run by a circuit simulator. All your testbench code goes in this module. We will instantiate our DUT (device under test) in this module.

```
reg clock;
reg output_enable;
reg [23:0] tone_to_play;
wire sq_wave;
```

Here are the inputs and outputs of our `tone_generator`. You will notice that the inputs to the `tone_generator` are declared as `reg` type nets and the outputs are declared as `wire` type nets. This is because we will be driving the inputs in our testbench and we will be monitoring the output.

```
initial clock = 0;
always #4 clock <= ~clock;
```

This is clock signal generation code. The clock signal needs to be generated in our testbench so it can be fed to the DUT. The initial statement sets the value of the clock net to 0 at the very start of the simulation. The next line toggles the clock signal every 4ns, i.e. half period of 125 MHz clock.

```
tone_generator audio_controller (
    .clk(clock),
    .output_enable(output_enable),
    .tone_switch_period(tone_to_play),
    .square_wave_out(sq_wave)
);
```

Now we instantiate the DUT and connect its ports to the nets we have access to in our testbench.

```
initial begin
    output_enable <= 0;
    #(10 * `MS);
    output_enable <= 1;

    tone_to_play <= 24'd37500;
    #(200 * `MS);

    ...
    $finish();
end
```

Here is the body of our testbench. The `initial begin ... end` block specifies the ‘main()’ function for our testbench. It is the execution entry point for our simulator. In the `initial` block, we can set the inputs that flow into our DUT using non-blocking (`<=`) or blocking (`=`) assignments.

We can also order the simulator to advance simulation time using delay statements. A delay statement takes the form `#[delay in time steps];`. For instance the statement `#[100];` would run the simulation for 100ns.

In this case, we set `output_enable` to 0 at the start of the simulation, then we let the simulation run for 10ms, then we set `output_enable` to 1. We then change the `tone_to_play` several times, and give the `tone_generator` some time to produce the various tones. For now, the `tone_to_play` signal won’t affect your `tone_generator` which should only be playing a fixed 220 Hz tone.

The final statement is a system function: the `$finish()` function tells the simulator to halt the simulation.

```
integer file;
initial begin
```

```

    file = $fopen("output.txt", "w");
    forever begin
        $fwrite(file, "%h\n", sq_wave);
        #(`SAMPLE_PERIOD);
    end
end

```

This piece of code is written in a separate `initial begin ... end` block. The simulator treats both blocks as separate threads that both start execution at the beginning of the simulation and operate in parallel.

This block of code uses two system functions `$fopen()` and `$fwrite()`, that allow us to write to a file. The `forever begin` construct tells the simulator to run the chunk of code inside it continuously until the simulation ends.

In the `forever begin` block, we sample the `square_wave_out` output of the `tone_generator` and save it in a file. We sample this value every ``SAMPLE_PERIOD` nanoseconds which corresponds to a 44.1 kHz sampling rate. Your `tone_generator`'s output is stored as 1s and 0s in a text file that can be converted to an audio file to hear how your circuit will sound when deployed on the FPGA.

3.3 A Choice of Simulators

As you've realised, the steps in the design and synthesis toolchain are independent programs with agreed interfaces for data flow. When it comes to simulating an HDL description of some design, several commercially available simulation tools exist. In this lab we will consider two:

1. **Vivado Design Suite** has an integrated simulator, **xsim**, that can run your Verilog testbench directly. You will have seen in previous labs the *Simulation* category in *Flow Navigator* to the left of the Design Suite application window.
2. **ModelSim** is a third-party application by Mentor Graphics. It can also synthesise a simulation of a given Verilog testbench (and its dependent modules), but is a more powerful standalone product.

Both simulators have a lot in common. They both allow you to view the waveforms of various signals in your design as a simulation, which you control, progresses. They're both driven by Tcl scripts (below), though you can also use a GUI to tweak their behaviour. Their GUIs have similar elements.

To avoid using the Vivado ISE simulator past years' labs have relied on the external ModelSim application, which is also used by the ASIC labs. For our purposes, the newer Vivado Design Suite simulator is actually pretty good. It's also built-in to the free WebPACK version of Vivado, whereas ModelSim requires a second license - a pain if you want to run simulations locally, at home. We will still emphasise ModelSim, however to help give you experience in a sandbox environment. It'll be useful to get a feel for the Vivado integrated simulator too, as a back up should you ever need it. Understanding the features common to both or unique to one should make you more confident approaching unknown tools out in the wild.

We provide a `sim` directory in the `lab3` folder to run the ModelSim simulation from. (Vivado can also be configured to launch ModelSim directly - you can try and set that up if you want.) The next sections will introduce you to ModelSim before comparing it to the Vivado integrated option.

3.4 ModelSim

3.4.1 Using TCL scripts for ModelSim (.do files)

ModelSim takes commands from TCL scripts. Take a look at the `lab3/sim/tests/tone_generator_testbench.do` TCL script. Here is a quick description of what it instructs our simulator to do.

```
start tone_generator_testbench
add wave tone_generator_testbench/*
add wave tone_generator_testbench/audio_controller/*
run 10000ms
```

We begin by issuing the `start` command to the simulator. This instructs the simulator to scan a list of Verilog source files provided to it to find a module named `tone_generator_testbench`. This module name must exactly match the module name of your top-level testbench module. The simulator loads and elaborates this module so that it's ready to simulate/execute.

The two `add_wave` commands are important. By default, the simulator will not log the signals in our testbench or DUT as the simulation executes. The `add wave tone_generator_testbench/*` line tells the simulator to log all signals directly inside in the `tone_generator_testbench` module. The second line tells the simulator to log the signals in a submodule of the top-level testbench module. Observe that `audio_controller` is the instance name of the `tone_generator` instance in the testbench module.

Finally, the `run (time)` command tells the simulator to jump to the initial `begin` blocks in the testbench and actually run the simulation. The time value (in our case `10000ms = 10s`) gives the simulator an upper bound on the simulation time. The simulator will simulate for 10 seconds before timing out. If the simulator hits the `$finish()` function before the 10 second timeout is up, it will stop simulation instantly.

3.4.2 Running ModelSim

With all the details out of the way, let's actually run a simulation. Go to the `lab3/sim` directory and run `make CASES=tests/tone_generator_testbench.do`. After a minute or so, the simulation will finish.

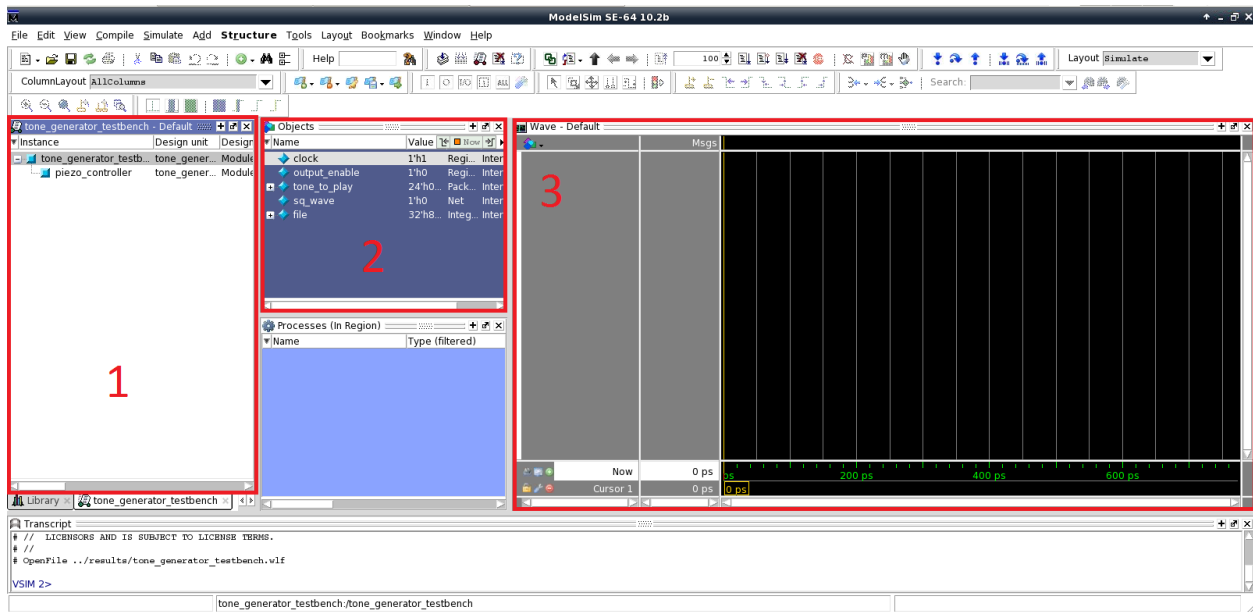
3.4.3 Viewing Waveforms

Let's take a look at the data that the simulator collected. Run the `viewwave` script like this:

```
./viewwave results/tone_generator_testbench.wlf &
```

The results of the simulation and the logged signals are stored in a `.wlf` file. This command should open that file in the ModelSim Wave Viewer.

You should see a window like this:



Let's go over the basics of ModelSim. The boxed screens are:

1. **Module Window** - List of the modules involved in the testbench. You can select one of these to have its signals show up in the object window.
2. **Object Window** - List of all the wires and regs in the selected module. You can add signals to the waveform view by selecting them, right-clicking, and doing **Add Wave**.
3. **Waveform Viewer** - The signals that you add from the object window show up here. You can navigate the waves by searching for specific values or going forward or backward one transition at a time. The x-axis represents time.

You may not see the **Waveform Viewer** when you first open ModelSim. To add signals to view, right click on the signal in the **Object Window**, and click on **Add Wave**. Add the `clock`, `output_enable`, and `sq_wave` signals to the waveform viewer.

Here are a few useful shortcuts:

- **Click on waveform:** Sets cursor position
- **O:** Zoom out of waveform
- **I:** Zoom into waveform
- **F:** Fit entire waveform into viewer (zoom full)
- **C:** Zoom in on cursor position

- **Middle Click + Drag Left/Right:** Zoom in on waveform section
- **Middle Click + Drag to Top Right:** Zoom out from current waveform section

You should play with these shortcuts for a few minutes. Now, zoom to fit the entire waveform in your viewer.

You should be able to see the clock oscillate at the frequency specified in the testbench. You should also see the `output_enable` signal start at 0 and then become 1 after 10 ms. However, you may see that the `sq_wave` signal is just a red line. What's going on?

3.4.4 Fixing the Undefined clock_counter

Blue lines in ModelSim indicate high-impedance (unconnected) signals. High-impedance is specified in Verilog as the letter `z`. We won't be using high-impedance signals in our designs, so blue lines in ModelSim indicate something in our testbench isn't wired up properly.

If you have a red line for your `clock_counter` at the start of your simulation, it may be because the initial value sitting inside the `clock_counter` register is unknown. It could be anything! Since we don't have an explicit reset signal for our circuit to bring the `clock_counter` to a defined value, it may be unknown for the entire simulation.

Let's fix this. In the future we will use a reset signal, but for now let's use a simpler technique. In `lab2/src/tone_generator.v` modify this line as such:

```
// Original code:
reg [x:0] clock_counter;

// Change to:
reg [x:0] clock_counter = 0;
```

This tells the simulator that the initial value for this register should be 0. For this lab, when you add new registers in your `tone_generator` or any other design module, you should instantiate them to their initial value in the same way. **Do not set an initial value for a 'wire' type net; it will cause issues with synthesis, and may cause X's in simulation.**

Now run the simulation again.

3.4.5 Helpful Tip: Reloading ModelSim .wlf

When you re-run your simulation and you want to plot the newly generated signals in ModelSim, you don't need to close and reopen ModelSim. Instead click on the 'Reload' button on the top toolbar which is to the right of the 'Save' button.

3.4.6 Listen to Your Square Wave Output

Take a look at the file written by the testbench located at `lab3/sim/build/output.txt`. It should be a sequence of 1s and 0s that represent the output of your `tone_generator` sampled at 44.1 kHz.

Use a Python script that can take this file and generate a `.wav` file that you can listen to.

Go to the `lab3/` directory and run the command:

```
python scripts/audio_from_sim.py sim/build/output.txt
```

This will generate a file called `output.wav`. Run this command to play it:

```
play output.wav
```

If `play` doesn't work, try running `aplay output.wav`.

You should hear 5 tones, played rapidly one after the other that have descending frequencies.

3.4.7 Playing with the Testbench

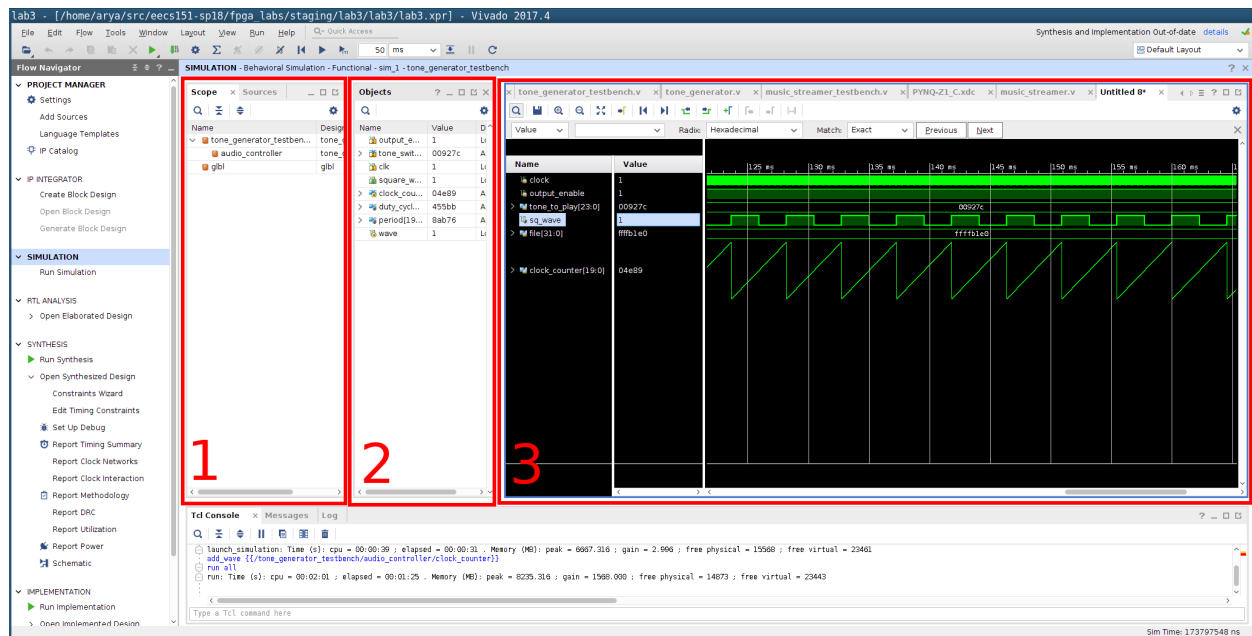
Play around with the testbench by altering the clock frequency, changing when you turn on `output_enable` and verifying that you get the audio you expect. For checkoff be able to answer the following questions and demonstrate understanding of simulation:

1. If you increase the clock frequency from 125 Mhz, would you expect the tone generated by your `tone_generator` to be of a higher or lower frequency than 220Hz? Why? Show audio evidence of this using simulation.
2. Prove that the `output_enable` input of your `tone_generator` actually works in simulation.
3. Create a testbench that plays some simple melody that you define and have its audio output file ready for checkoff.

3.5 Vivado's Integrated Simulator

Inside a Vivado project, expand the *Simulation Sources* category in your *Project Hierarchy* window (that's the one with all your files). At any given time only one Verilog module can be the simulation "Top", just as there can only be one synthesis "Top" for implementation. If it isn't already, right-click `tone_generator_testbench` and select *Set As Top*. Then in the *Flow Navigator* window, click *Run Simulation* in the *Simulation* category. You will get a context menu: select *Run Behavioural Simulation*.

Then you will be presented with the Vivado Simulation window:



This should be familiar to you: it looks and behaves like the ModelSim GUI you saw earlier.

1. is the **Scope Window**, which is like ModelSim's **Module Window**, and lets you select from among simulated modules;
2. is an **Object Window** just like ModelSim's, allowing you to select waveforms to view; and
3. is the **Waveform Viewer**.

Play around with it; does your intuition from ModelSim carry over?

Although the Vivado simulator can be controlled with a Tcl script like ModelSim, there is a GUI way to modify settings too. Click *Tools* menu → *Settings* to bring up the *Project Settings* dialog. Select the *Simulation* category in the left pane. (Notice that you can change the default simulator here from Vivado to, say, ModelSim.) The options defined in various tabs in the right hand pane allow you to select various simulation parameters, including initial duration.

A final note: when the *Simulation* window is open in Vivado, you can use the *Tcl Console* to execute simulation commands. (The *Tcl Console* appears just below boxes (1) - (3) in the figure above.) A lot of the commands you can use here will work like they do for ModelSim. The full list of commands is available in the user manual from Xilinx.

3.5.1 Where does Vivado put output.txt?

The Vivado simulator will also have produced an `output.txt` file with waveform samples. But where? In your project root directory, use `find` to *find* out:

```
lab3 $ find . -name "output.txt"
./lab3/lab3.sim/sim_1/behav/xsim/output.txt
```

3.6 Resetting Simulations

Running simulations, both for ModelSim and in Vivado, generates a lot of signal data for the waveforms viewers. You often don't need to keep this intermediary data (which is easily several gigabytes in this lab alone), and you may be running out of quota on the machine you're using. In order to clear intermediate state and reset the simulation, perform the following steps.

1. For **ModelSim**, navigate to the `sim` directory in which you executed `make CASES=`, e.g. `fpga_labs_fa18/lab3/sim`. There, execute `make clean`.
2. For **Vivado**, open the *Tcl Console*. It's usually available toward the bottom-left of the application window, but can also be opened from the menus. In the Tcl Console, execute `reset_simulation`.

4 Introduction to Inferred Asynchronous ROMs

An asynchronous memory is a memory block that isn't governed by a clock. In this lab, we will use a Python script to generate a ROM block in Verilog.

A ROM is a read-only memory. This data can be accessed by supplying an address to the ROM; after some time, the ROM will output the data stored at that address. A memory block in general can contain as many addresses in which to store data as you desire. Every address should contain the same amount of data (bits). The number of addresses is called the **depth** of the memory, while the number of bits stored per address is called the **width** of the memory.

The synthesizer takes the Verilog you write and converts it into a low-level netlist of the structures are actually used on the FPGA. Our Verilog **describes** the functionality of some digital circuit and the synthesizer **infers** what primitives implement the functional description. In this section, we will examine the Verilog that allows the synthesizer to infer a ROM. This is a minimal example of a ROM in Verilog: (depth of 8 entries/addresses, width of 12 bits)

```
module rom (input [2:0] address, output reg [11:0] data);
    always @(*) begin
        case(address)
            3'd0: data = 12'h000;
            3'd1: data = 12'hFFF;
            3'd2: data = 12'hACD;
            3'd3: data = 12'h122;
            3'd4: data = 12'h347;
            3'd5: data = 12'h93A;
            3'd6: data = 12'h0AF;
            3'd7: data = 12'hC2B;
        endcase
    end
endmodule
```

To power our `tone_generator`, we will be using a ROM that is X entries/addresses deep and 24 bits wide. The ROM will contain tones that the `tone_generator` will play. You can choose the depth of your ROM based on the length of the sequence of tones you want to play.

We've provided you with a few scripts that can generate a ROM from either a file with it's contents or even from sheet music. Run these commands from `lab3/`.

```
python scripts/musicxml_parser.py musicxml/Twinkle_Twinkle_Little_Star.xml music.txt
python scripts/rom_generator.py music.txt ../lab3.srcs/sources_1/new/rom.v 1024 24
```

The first script will parse a MusicXML file and turn it into a list of `tone_switch_periods` for each of the notes for a piece of sheet music. The second script will take that list and turn it into a ROM that's 1024 entries deep with a width of 24 bits.

Take a look at `music.txt` and `src/rom.v`. You can download your own music in MusicXML format from here (<https://musescore.org/>) and run it through the same parser; it should ideally only have one part to work properly. You can also directly edit the `music.txt` file to customize the contents of the ROM as you wish.

5 Design of the `music_streamer`

Open up the `music_streamer.v` file. This module will contain an instance of the ROM you created earlier and will address the ROM sequentially to play notes. The `music_streamer` will play each note in the ROM for a predefined amount of time by sending it to the `tone_generator`.

We will play each note for 1/25th of a second. Calculate what that is in terms of 125Mhz clock cycles.

Instantiate the `music_streamer` module in `z1top.v`. Use the instance name `streamer` to match the expected name in the `.do` file. Connect its `tone` output to the `tone_switch_period` input of the `tone_generator`. Connect its `clk` input to the global clock signal. Connect its `rom_address` output to the LEDs by routing the top 6 bits of address.

Now let's begin the design of the `music_streamer` itself. Instantiate your ROM in the `music_streamer` and connect the ROM's `address` and `data` ports to wire or reg nets that you create in your module (you can ignore the `last_address` port).

Next, write the RTL that will increment the address supplied to the ROM every **1/25th of a second**. The data coming out of the ROM should be fed to the `tone` output. The ROM's address input should go from 0 to the depth of the ROM and should then loop around back to 0. You don't have a reset signal, so define the initial state of any registers in your design for simulation purposes. Also hook up the `rom_address` output to the ROM address currently being accessed.

6 Simulating the `music_streamer`

To simulate your `music_streamer` open up the `lab3/src/music_streamer_testbench.v`. In contrast to the `tone_generator_testbench` where the `tone_generator` was instantiated in isolation,

in this testbench we are instantiating our entire top-level design, `z1top`. This testbench is referred to as a system-level testbench, which tests our entire design using top-level I/O, in contrast to the `tone_generator_testbench` which is a block-level testbench. This is similar to the difference between unit and integration tests in software development.

You can see that this testbench just runs a simulation for 2 seconds and then exits. You might have to modify the `music_streamer_testbench.do` file to match the name of your module instances in `z1top.v`.

To execute the testbench, run `make CASES=tests/music_streamer_testbench.do` in `lab3/sim`. This may take several minutes to complete. You may have to run `make clean` before running `make` if ModelSim has cached build artifacts.

Inspect your waveform to make sure you get what you expect. Verify that there are no undefined signals (red lines, x) Then run the Python script to generate a `.wav` file of your simulation results and listen to your `music_streamer`. It should sound like the first few seconds of the song that was loaded on the ROM.

7 Verify your Code Works For Rest Notes

In simulation, you can often catch bugs that would be difficult or impossible to catch by running your circuit on the FPGA. You should verify that if your ROM contains an entry that is zero (i.e. generate a 0Hz wave), that the `tone_generator` holds the `square_wave_out` output at either 1 or 0 with no oscillation. Verify this in simulation, and prove the correct functionality during checkoff.

8 Try it on the FPGA!

Now try your `music_streamer` on the FPGA. You should expect the output to be the same as in simulation. The `SWITCHES[1]` switch should still work to disable the output of the `tone_generator`. Show your final results, simulation, and the working design on the FPGA to the TA for checkoff.

9 Checkoff

1. Section 3 - Play an audio file that was generated using the `tone_generator_testbench` that plays some melody you define.
2. Section 7 - Prove that if the ROM contains an entry for a `tone_switch_period` of 0, that the square wave doesn't oscillate.
3. Section 8 - Show the working `music_streamer` on the FPGA.

10 Conclusion

You are done with lab 3! Please write down any and all feedback and criticism of this lab and share it with the TA.