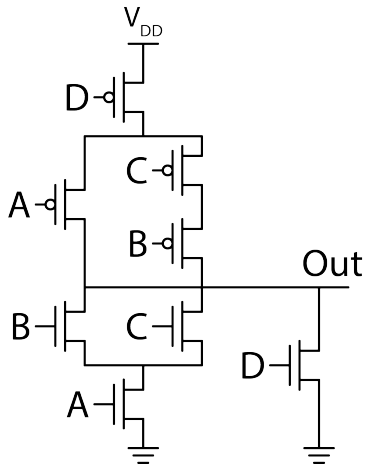
# EECS 151/251A Homework 6

Due Friday, November 4th, 2022 11:59PM

## Problem 1: CMOS Gates

(a) What is the boolean expression for the function described by the CMOS gate below?

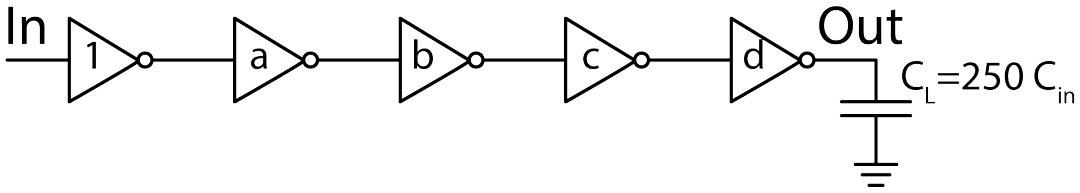



(b) Draw the static complementary CMOS circuit that implements the following logic function:

$$\overline{ABC + DE}$$

## Problem 2: Inverter Delay

We want to design a 5-stage inverter chain that can drive a load capacitance of $C_L = 250C_{in}$ with the smallest delay possible, where $C_{in}$ is the input capacitance of a minimum sized inverter. The first inverter is constrained to be minimum size ($W = 1$ as in shown in the figure). Assume that $\tau_{inv} = 10$ ps and $\gamma = 1$.




(a) How should the inverter chain be sized for minimum delay?

(b) What is the total delay through the inverter chain?

(c) Assume that the number of stages is not restricted to 5. How many stages should you use for minimum delay? What is the total delay?

## Problem 3: Logical Effort

In the lecture, we mentioned that inverters in today's FinFET technology nodes have equal NMOS and PMOS widths since the $R_{on,n} = R_{on,p}$. Here, we assume a different technology, where for a minimum size transistor ($W = 1$),

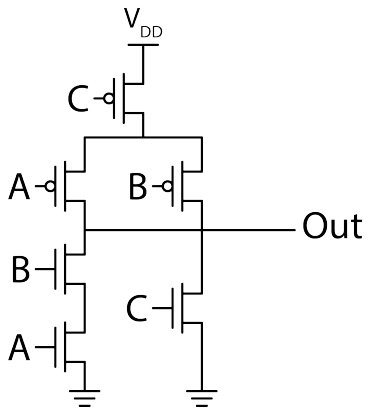
- NMOS on resistance $R_{on,n} = R$
- PMOS on resistance $R_{on,p} = 3R$
- Gate capacitance $C_g = C$ (same for both NMOS and PMOS)

Assume $\gamma = 1$.

(a) How should the minimum inverter be sized? Specify the NMOS width $W_n$ and PMOS width $W_p$.

(b) What is $R_{eq}$ and $C_{in}$ of the minimum size inverter?

(c) We want to design the following custom CMOS gate:




How should the custom gate be sized to have the same output current as the minimum size inverter?

(d) Compute the logical effort LE and (normalized) parasitic delay P of the custom gate.

*Note*: The logical effort should be calculated separately for each input.

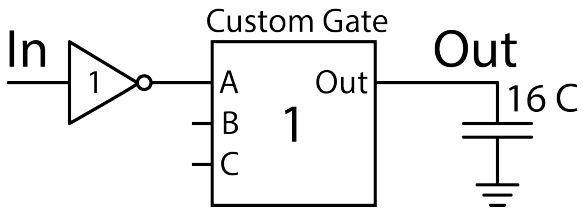
$LE_A =$

$LE_B =$

$LE_C =$

$P =$

(e) (251A Only) Suppose that we have the following data path:




An inverter drives the custom gate's input A, and the custom gate drives a load capacitance $C_L = 16C$. Both the inverter and custom gate are minimum size (as denoted by **"1"** in the figure). Assume that the custom gate's other inputs B and C are driven by other circuits not shown here.

What is the total delay from the input to the output? Express in terms of $R$ and $C$.