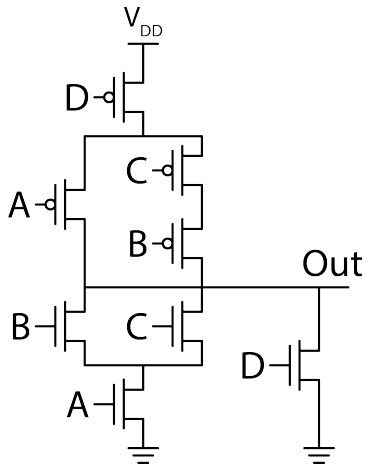
EECS 151/251A Homework 6

Due Friday, November 4th, 2022 11:59PM

Problem 1: CMOS Gates

(a) What is the boolean expression for the function described by the CMOS gate below?



Solution:

We can look at the PDN to observe the boolean expression, converting parallel branches to boolean ORs and series to boolean ANDs:

$$Out = \overline{A(B+C)+D} \tag{1}$$

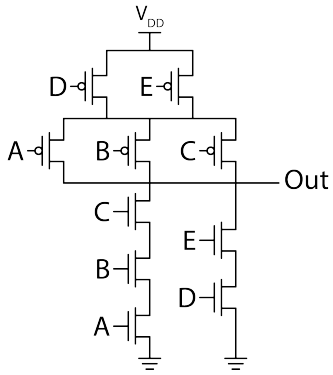
(b) Draw the static complementary CMOS circuit that implements the following logic function:

$$\overline{ABC + DE}$$

Solution:

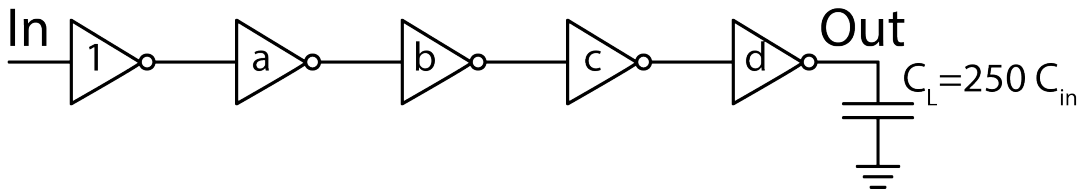
The output is 0 when $ABC+DE$ is true, so the PDN can directly map to this expression. Hence there are 2 parallel branches in the PDN, with A/B/C in series on one branch and D/E in series on the other branch.

The PUN can be derived by applying the duality of complementary CMOS gates. Series paths are converted to parallel, and parallel paths are converted to series. This results in 2 groups of transistors in series, with one group being A/B/C in parallel and the other being D/E in parallel.



Problem 2: Inverter Delay

We want to design a 5-stage inverter chain that can drive a load capacitance of $C_L = 250C_{in}$ with the smallest delay possible, where C_{in} is the input capacitance of a minimum sized inverter. The first inverter is constrained to be minimum size ($W = 1$ as in shown in the figure). Assume that $\tau_{inv} = 10$ ps and $\gamma = 1$.



(a) How should the inverter chain be sized for minimum delay?

Solution:

Delay is minimized when each stage has the same fanout. The total fanout is

$$F = \frac{C_L}{C_{in}} = \frac{250C_{in}}{C_{in}} = 250$$

The fanout per stage should then be

$$f = \sqrt[N]{F} = \sqrt[5]{250} \approx 3.02$$

We can then size the inverters from the back:

$$C_d = \frac{C_L}{f} = \frac{250C_{in}}{3.02} \approx 82.9C_{in} \Rightarrow d \approx 82.9$$
$$C_c = \frac{C_d}{f} = \frac{82.9C_{in}}{3.02} \approx 27.5C_{in} \Rightarrow c \approx 27.5$$
$$C_b = \frac{C_L}{f} = \frac{27.5C_{in}}{3.02} \approx 9.1C_{in} \Rightarrow b \approx 9.1$$
$$C_a = \frac{C_L}{f} = \frac{9.1C_{in}}{3.02} \approx 3.02C_{in} \Rightarrow a \approx 3.02$$

(b) What is the total delay through the inverter chain?

Solution:

$$t_{p,tot} = \tau_{inv} \cdot N(\gamma + f) = 10 \cdot 5(1 + 3.02) \approx 201\text{ps}$$

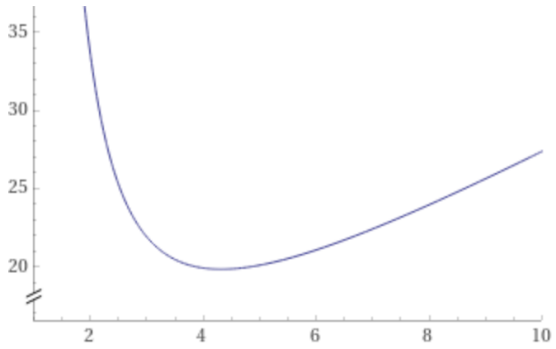
(c) Assume that the number of stages is not restricted to 5. How many stages should you use for minimum delay? What is the total delay?

Solution:

The total (normalized) delay through the inverter chain as a function of N (the number of stages), F (the total fanout), and γ is

$$D = N(\gamma + F^{1/N})$$

Using $F = 250$ and $\gamma = 1$, we can plot the delay curve:



The graph shows that the optimal number of stages is 4. Thus, the total delay is

$$t_{p,tot} = \tau_{inv} \cdot N(\gamma + F^{1/N}) = 10 \cdot 4(1 + 250^{1/4}) \approx 199\text{ps}$$

Problem 3: Logical Effort

In the lecture, we mentioned that inverters in today's FinFET technology nodes have equal NMOS and PMOS widths since the $R_{on,n} = R_{on,p}$. Here, we assume a different technology, where for a minimum size transistor ($W = 1$),

- NMOS on resistance $R_{on,n} = R$
- PMOS on resistance $R_{on,p} = 3R$
- Gate capacitance $C_g = C$ (same for both NMOS and PMOS)

Assume $\gamma = 1$.

(a) How should the minimum inverter be sized? Specify the NMOS width W_n and PMOS width W_p.

Solution:

$W_n = 1$, $W_p = 3$.

We want equal pull-down/pull-up strengths. $W_n = 1$ would result in a pull-down resistance of R, and $W_p = 3$ would result in a pull-up resistance of $3R/3 = R$.

(b) What is R_{eq} and C_{in} of the minimum size inverter?

Solution:

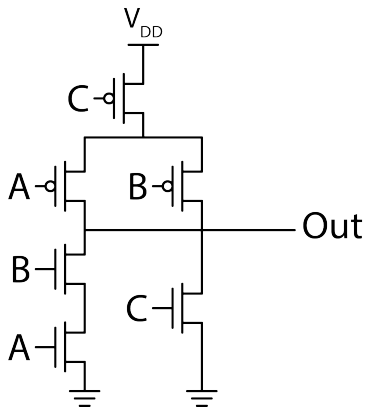
$R_{eq} = R$, $C_{in} = 4C$.

As mentioned in the solution to part (a), the minimum size inverter is sized to have a pull-up and pull-down resistance of R.

The total input capacitance is

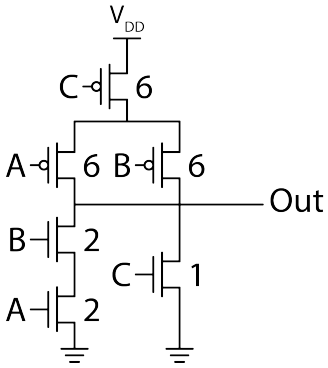
$$C_{g,n} + C_{g,p} = W_n C_g + W_p C_g = C + 3C = 4C$$

(c) We want to design the following custom CMOS gate:



How should the custom gate be sized to have the same output current as the minimum size inverter?

Solution:



We want to size each transistor such that in the worst case, the pull-up/pull-down resistance is equivalent to that of the minimum size inverter (i.e., R). For parallel branches, the worst case considers only one branch being on at a time.

First, consider the pull-down network. The NMOS with input C should be sized **1** to have a PD resistance of R. As for the NMOS with inputs A and B, both transistors must be on, resulting in 2x the resistance. Thus, each should be sized **2** such that the PD resistance in this case is $R/2 + R/2 = R$.

Next, consider the pull-up network. For the PUN to be turned on, all branches must require a stack of 2 PMOS devices to be on (either A & C or B & C). Thus, each PMOS must be sized 2x larger to account for the 2-stacked PMOS. In addition, PMOS must be 3x larger than the NMOS to account for the 3x larger on-resistance. Hence, setting the PMOS devices to have size **6** results in the PU resistances as

$$A, C : \frac{R_{on,p}}{W_A} + \frac{R_{on,p}}{W_C} = \frac{3R}{6} + \frac{3R}{6} = R$$
$$B, C : \frac{R_{on,p}}{W_B} + \frac{R_{on,p}}{W_C} = \frac{3R}{6} + \frac{3R}{6} = R$$

(d) Compute the logical effort LE and (normalized) parasitic delay P of the custom gate.
Note: The logical effort should be calculated separately for each input.

Solution:

The logical effort is computed as

$$LE = \frac{R_{eq,gate}C_{in,gate}}{R_{eq,inv}C_{in,inv}}$$

Because we sized the custom gate to have the same resistance as the inverter,

$$R_{eq,gate} = R_{eq,inv}$$

and the LE equation simplifies to the ratio of capacitances, or

$$LE = \frac{C_{in,gate}}{C_{in,inv}}$$

We can first compute the gate input capacitance for each input:

$$C_{in,A} = C_g(W_{n,A} + W_{p,A}) = C_g(2+6) = 8C$$
$$C_{in,B} = C_g(W_{n,B} + W_{p,B}) = C_g(2+6) = 8C$$
$$C_{in,C} = C_g(W_{n,C} + W_{p,C}) = C_g(1+6) = 7C$$

The logical effort for each input is then

$$LE_A = \frac{C_{in,A}}{C_{in,inv}} = \frac{8C}{4C} = 2$$
$$LE_B = \frac{C_{in,B}}{C_{in,inv}} = \frac{8C}{4C} = 2$$
$$LE_C = \frac{C_{in,C}}{C_{in,inv}} = \frac{7C}{4C} = 1.75$$

The (normalized) parasitic delay is computed as

$$P = \frac{R_{eq,gate}C_{p,gate}}{R_{eq,inv}C_{p,inv}}$$

As in the case with logical effort,

$$R_{eq,gate} = R_{eq,inv}$$

and the parasitic delay equation simplifies to the ratio of capacitances, or

$$P = \frac{C_{p,gate}}{C_{p,inv}}$$

There are 4 transistors whose drains are directly connected to the output: the NMOS with input B, NMOS with input C, PMOS with input A, and PMOS with input B. The parasitic output cap of the gate is thus

$$\gamma C_g(W_{n,B} + W_{n,C} + W_{p,A} + W_{p,B}) = 15\gamma C$$

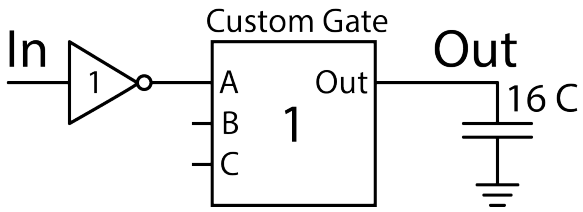
The parasitic output cap of the inverter is

$$\gamma C_g(W_n + W_p) = 4\gamma C$$

Thus, the parasitic delay is

$$P = \frac{15\gamma C}{4\gamma C} = \frac{15}{4} = 3.75$$

(e) (251A Only) Suppose that we have the following data path:



An inverter drives the custom gate's input A, and the custom gate drives a load capacitance $C_L = 16C$. Both the inverter and custom gate are minimum size (as denoted by **"1"** in the figure). Assume that the custom gate's inputs B and C are driven by other circuits not shown here.

What is the total delay from the input to the output? Express in terms of R and C.

Solution:

The total delay can be expressed in terms of parasitic delays, logical effort, and fanout:

$$\begin{aligned} t_{p,tot} &= t_{p,inv} + t_{p,gate} \\ &= \tau_{inv}(\gamma + f_{inv}) + \tau_{inv}(P_{gate} + LE_{gate,A} f_{gate}) \end{aligned}$$

The fanout of the inverter is

$$f_{inv} = \frac{C_{in,A}}{C_{in,inv}} = \frac{8C}{4C} = 2$$

The fanout of the custom gate is

$$f_{gate} = \frac{C_L}{C_{in,A}} = \frac{16C}{8C} = 2$$

Thus, the total delay is

$$\begin{aligned} t_{p,tot} &= \tau_{inv}[(\gamma + f_{inv}) + (\gamma \cdot P_{gate} + LE_{gate,A} f_{gate})] \\ &= \tau_{inv}[(1+2) + (1 \cdot 3.75 + 2 \times 2)] \\ &= 10.75\tau_{inv} \\ &= 10.75(4 \ln 2RC) \approx 29.8RC \end{aligned}$$