

EECS 151/251A Homework 1 Solutions

Problem 1: Dennard Scaling

Assuming perfect Dennard Scaling. Imagine a processor that runs at 5MHz & 1A and dissipates 5W.

- (a) What would the power and performance be in the next technology node if transistors are 1.25x smaller? Remember units!
- (b) How would power density change in the new technology node? Why?

Solution:

- (a) $\kappa = 1.25$

New power $\dot{P} = P \frac{1}{\kappa^2} = 5 \frac{1}{1.25^2} = 3.2 \text{ W}$

New capacitance $\dot{C} = C \frac{1}{\kappa}$ and new voltage $\dot{V} = V \frac{1}{\kappa}$

We know that $P = \frac{1}{2} CV^2 f$ and so:

$$\dot{P} = P \frac{1}{\kappa^2} = \frac{1}{2} C V \frac{1}{\kappa^2}$$

$$= \frac{1}{2} \kappa \dot{C} \kappa^2 \dot{V}^2 f \frac{1}{\kappa^2}$$

$$= \frac{1}{2} \dot{C} \dot{V}^2 (\kappa f)$$

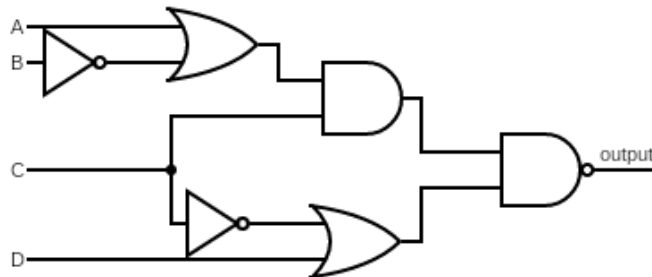
Thus new frequency $\dot{f} = \kappa f = 1.25 \cdot 5 = 6.25 = 6.25 \text{ MHz}$

- (b) Power density is $\frac{VI}{A}$

We know that new voltage $\dot{V} = V \frac{1}{\kappa}$, new current $\dot{I} = I \frac{1}{\kappa}$, new area $\dot{A} = \frac{A}{\kappa^2}$

New power density is $\frac{\dot{V}\dot{I}}{\dot{A}} = \frac{V \frac{1}{\kappa} I \frac{1}{\kappa}}{\frac{A}{\kappa^2}} = \frac{VI}{A}$

Problem 2: Simplifying Circuits



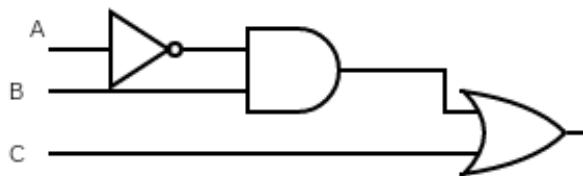
- (a) Write out the full truth table for the circuit above.
- (b) By inspecting the truth table drawn in part (a), draw a simplified circuit with a minimum number of logic gates

Solution:

(a) Truth Table

A	B	C	D	output
0	0	0	0	0
1	0	0	0	0
0	1	0	0	1
1	1	0	0	0
0	0	1	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	0	1
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

(b) Circuit



Problem 3: Verilog

For each example, identify the error in the Verilog code and suggest a fix. You don't have to rewrite the entire Verilog unless you think that's the most succinct & clear way to answer.

(a)

```
module example_one(
    input [1:0] a,
    input b, c,
    output x
```

```

);
    always @(*) begin
        case (a)
            2'b00 : x = b;
            2'b01 : x = c;
            2'b11 : x = b & c;
            2'b10 : x = b | c;
        endcase
    end
endmodule

```

Solution:

output x should be reg x. x is being assigned within an always block.

```

(b) module example_two(
    input a, b, c,
    output reg [1:0] x
);
    always @(*) begin
        if (a & b & c) begin
            x = 3;
        end
        else if (a & b) begin
            x = 2;
        end
        else if (c) begin
            x = 1;
        end
    end
endmodule

```

Solution:

Include an else case to catch all other cases or exhaust all 8 cases possible with a,b, and c. Don't want to accidentally create a latch.

```

(c) module example_three(
    input [1:0] a,
    input toggle, sel,
    output reg x
);
    always @(toggle) begin
        if (sel) begin
            x = a[1];
        end
        else if (!sel) begin
            x = a[0];
        end
    end
endmodule

```

```
        end  
    end  
endmodule
```

Solution:

always @(toggle) should be either always @(*) or always @(toggle, sel, a)