

EECS 151/251A Midterm 2

Review Session

Topics in Scope

- RISC-V ISA, pipelining, hazard resolution (data + control), pipeline diagrams, critical path analysis
- LUTs, how to use them to implement logic functions, how to combine them
- MOS switch model, sketching VTCs, find logical function from schematic
- MOS resistance/capacitance relationship with width
- Pass transistor gates, static CMOS gates (+ construction from logic formula), inverter VTC and switching threshold
- Inverter/Gate sizing, logical effort for minimum delay logic chain sizing
- RC delay, Elmore delay approximation
- Wire models
- Power/energy, energy on capacitor/drawn from supply, dynamic power
- Adders (ripple carry, carry bypass, carry select, CLA)

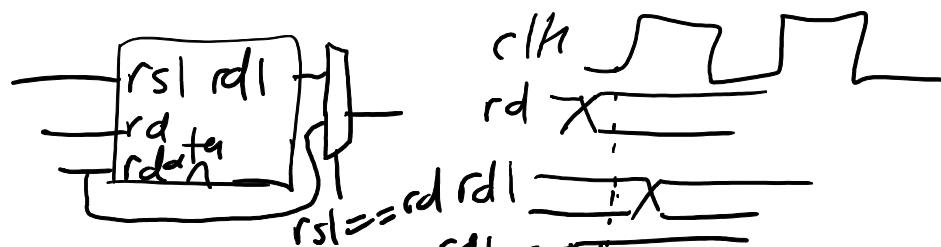
Topics NOT in Scope

- Multipliers
- Flip-flops/latches

RISC-V Datapath/Pipelining/Hazards

Fa15 MT2 #5

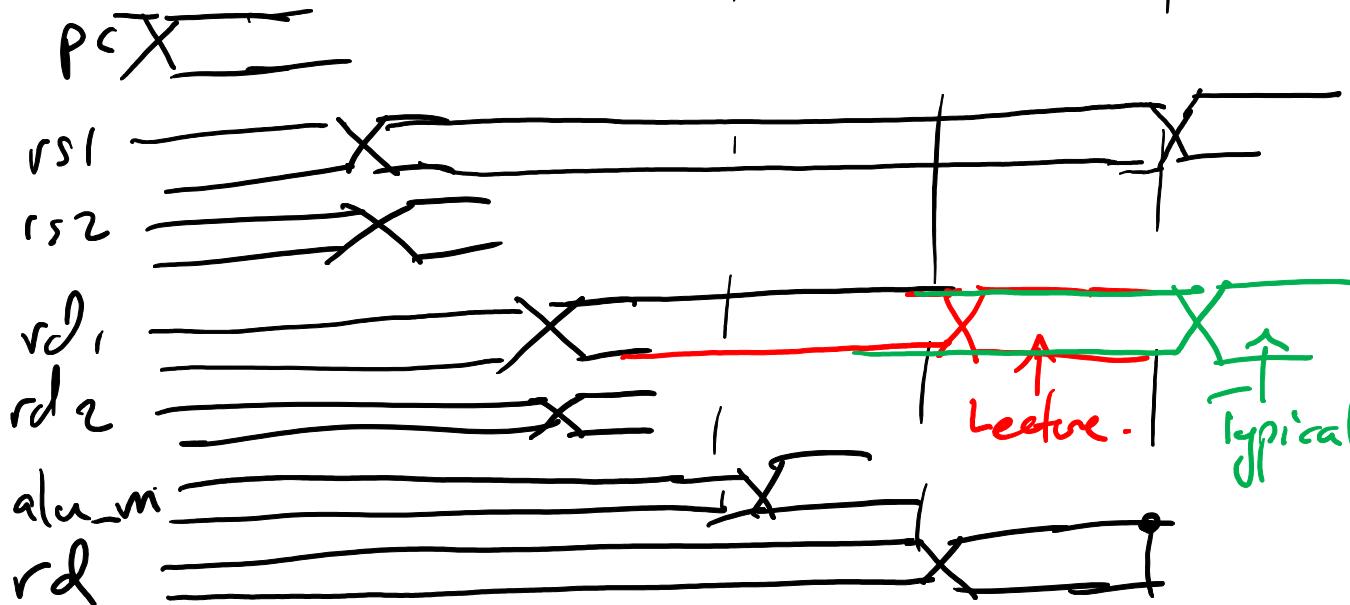
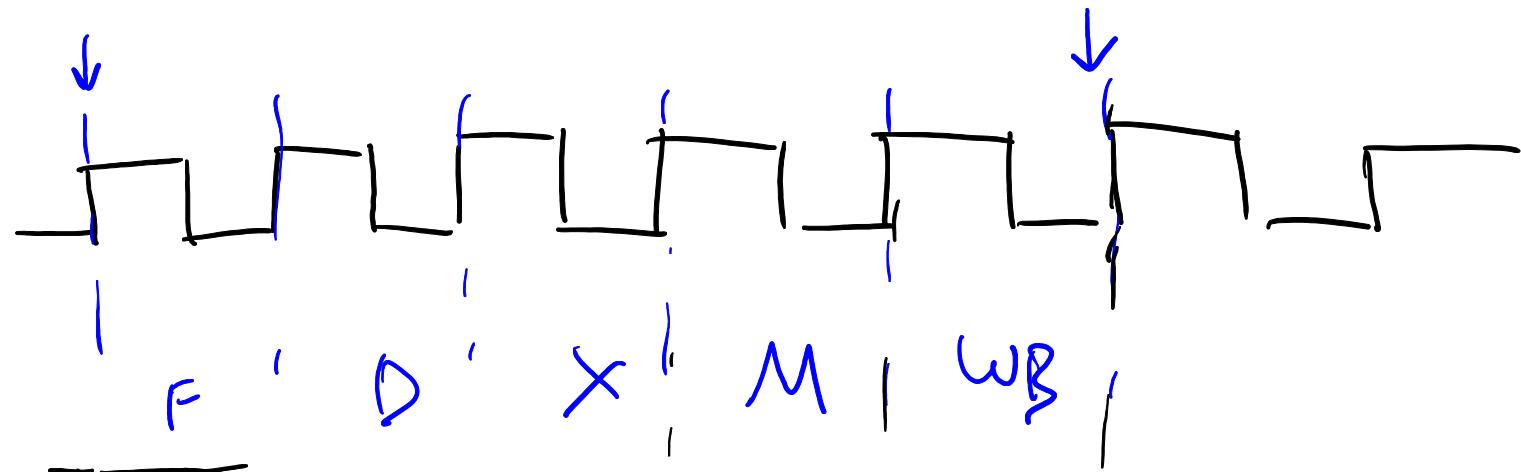
5. [12pts/12pts] MIPS microarchitecture.



Consider the design of the single-cycle MIPS processor, as we ~~were discussed in~~ class. Suppose you want to pipeline this design using *2 pipeline stages*. Functionality is divided into 2 pipeline stage as shown below:

stage 1	stage 2
instruction fetch/decode	ALU operation
regfile access	Dmem access WB

In the space below, explain what *hazards* will result from this pipelining (prior to any measures to remove the hazards). For each hazard, i) describe why it occurs, ii) write a short MIPS assembly language instruction sequence to demonstrate a case when the hazard would occur, and iii) describe what you can do to deal with the hazard. Write your answers in the space provided. (You might not need all answer spaces.)



Fa15 MT2 #5

(a) Hazard 1

- i. Control hazard occurs on every branch instruction because the branch comparison is done in stage 2 and the branch target address is needed in stage 1.
- ii. Any instruction sequence with a branch.
- iii. 1) Stall the pipeline to allow the branch instruction to complete, 2) implement branch prediction.

(b) Hazard 2

- i. Data hazard occurs on r-type instruction dependent on the immediately preceding instruction, because ALU output is available sometime in stage 2 but needed at the beginning of stage 2.

ii.

```
add $1, $2, $3  
add $4, $5, $1
```

- iii. 1) Stall the pipeline to allow r-type to store results back to register file, 2) Selectively feed output of ALU to ALU input register.

Fa15 MT2 #5

(c) Hazard 3

- i. Data hazard on load from memory when an instruction is dependent on load instruction immediately preceding. Result from memory load is available at end of stage 2 but needed at beginning of stage 2.

ii.

```
lw $1, 0($1)
add $4, $5, $1
```

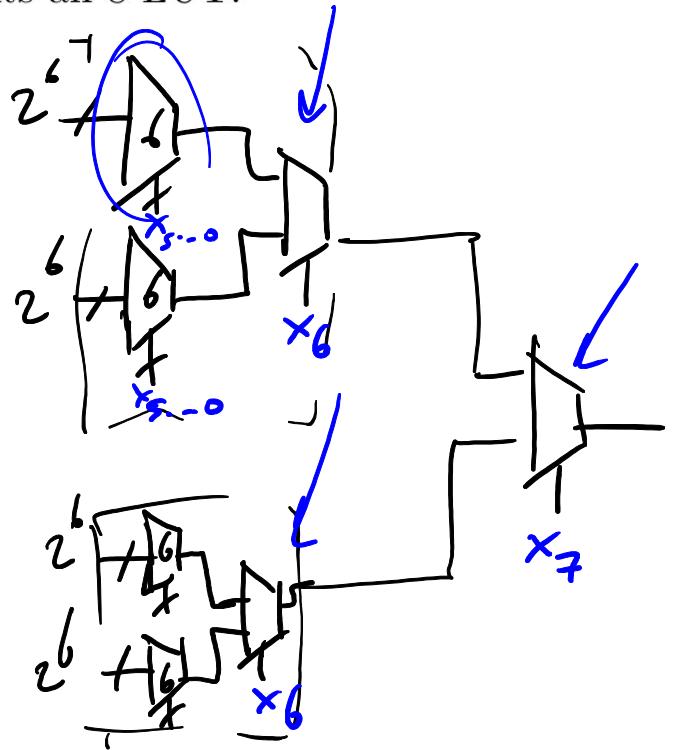
- iii. 1) Selectively direct output of memory to input register of ALU, 2) stall the load instruction.

FPGAs / LUTs

Sp13 Final



1. [4pts] Using 6-LUTs only (each with inputs x_0, x_1, \dots, x_5) and output y , draw a circuit that implements an 8-LUT.



CMOS Gates

Sp13 Final

9. [4pts] Draw a CMOS transistor-level circuit for a 2-input exclusive-or function (try to minimize the number of transistors).

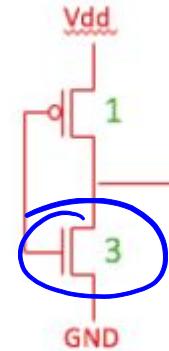
$$f = A \text{ xor } B = \overline{A}\overline{B} + \overline{A}B + A\overline{B}$$
$$\overline{\overline{f}} = f = \overline{A}\overline{B} + \overline{A}B + A\overline{B} = (\overline{A} + B) \cdot (A + \overline{B})$$

Fa 18 MT1

- c) Implement the logic function for C_0 as a complex static CMOS gate (3 Pts).

Reference inverter

$$C_0 = A_1B_1 + A_1A_0B_0 + A_0B_1B_0$$



Fa 18 MT1

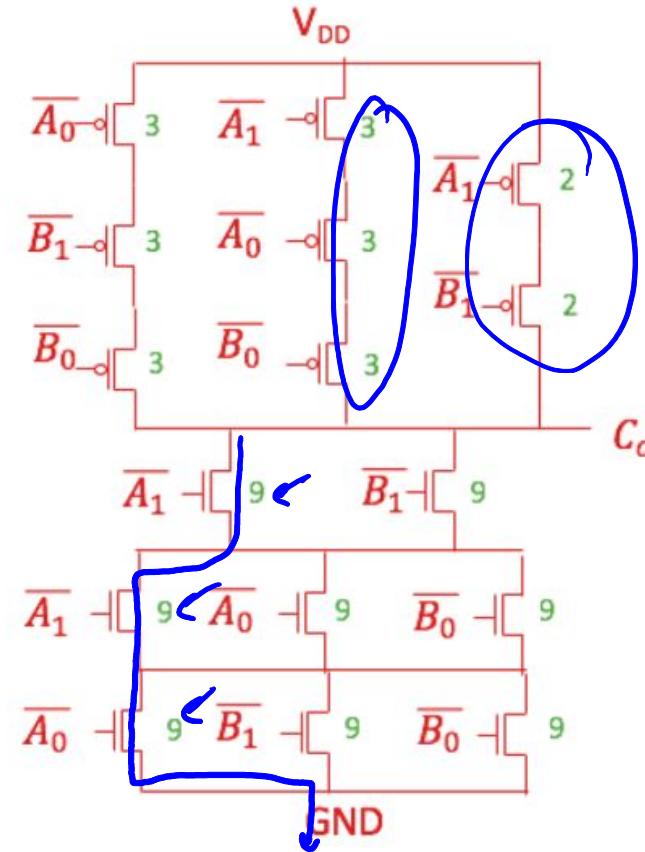
$$C_0 = A_1 B_1 + A_1 A_0 B_0 + A_0 B_1 B_0$$

$$\overline{C_0} = \overline{A_1 B_1 + A_1 A_0 B_0 + A_0 B_1 B_0}$$

$$\overline{C_0} = \overline{A_1} \overline{B_1} \cdot \overline{A_1} \overline{A_0} \overline{B_0} \cdot \overline{A_0} \overline{B_1} \overline{B_0}$$

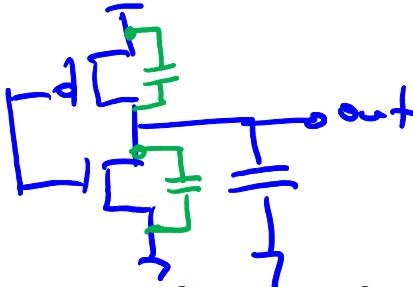
$$\overline{C_0} = (\overline{A_1} + \overline{B_1}) \cdot (\overline{A_1} + \overline{A_0} + \overline{B_0}) \cdot (\overline{A_0} + \overline{B_1} + \overline{B_0})$$

$$C_0 = \underbrace{(\overline{A_1} + \overline{B_1})}_{\text{green wavy line}} \cdot \underbrace{(\overline{A_1} + \overline{A_0} + \overline{B_0})}_{\text{green wavy line}} \cdot \underbrace{(\overline{A_0} + \overline{B_1} + \overline{B_0})}_{\text{green wavy line}}$$



Power / Energy

Sp12 Final



- (j) [1pt] The switching energy corresponding to a change in value on the output of a CMOS logic gate is given by $E = 1/2CV^2$. What does “C” represent in the actual circuit?

$$\underline{\underline{C}}$$

- (k) [1pt] Based on the equation above, if the gate is switching at a frequency of “f”, what is its average *power consumption*?

$$C \cdot \underline{\underline{V_{DD}^2}} \cdot f \cdot \underline{\underline{[x_{0 \rightarrow 1}]}}$$

Sp12 Final

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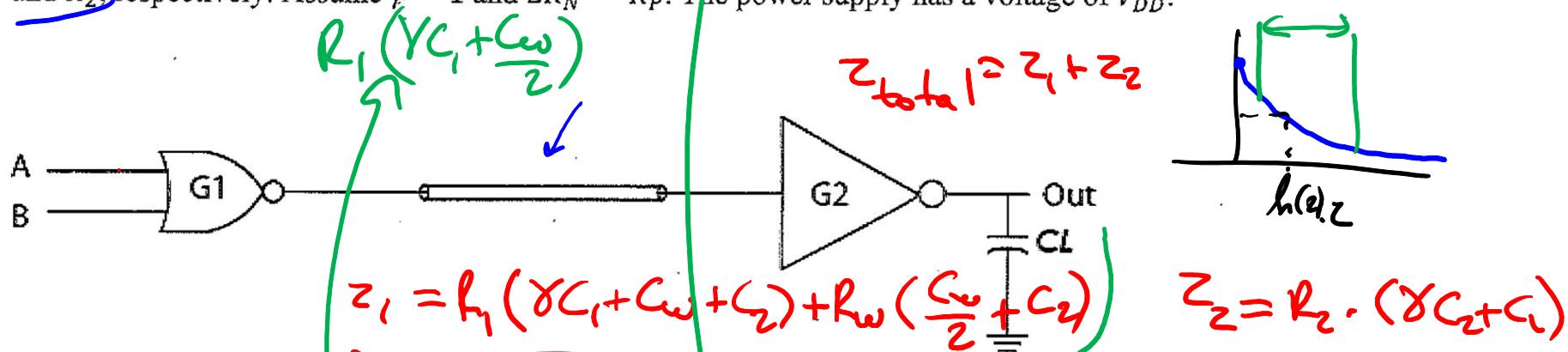
(k) [1pt] Based on the equation above, if the gate is switching at a frequency of “f”, what is its average *power consumption*?

- C = total parasitic capacitance of every gate (input and output)
- Power = [Energy/Time]
- $P_{\text{avg}} = C * V^2 * f$

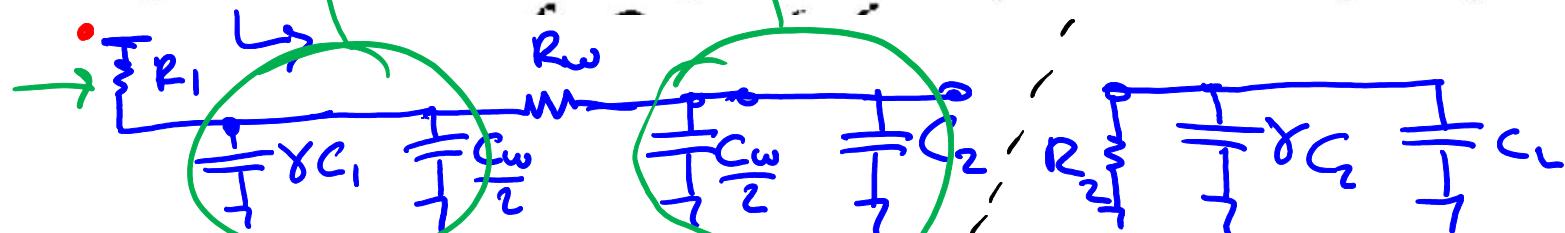
Sp16 Midterm 2

$$\rightarrow \left(\frac{C_w}{2} + C_2 \right) \cdot (R_w + R_1)$$

A NOR Gate (G1) with input capacitance C_1 is driving a wire with total resistance R_w and total capacitance C_w , and an inverter with input capacitance C_2 . Inverter G2 is driving an external load of C_L . The on-resistance of G1 and G2 are R_1 and R_2 , respectively. Assume $\gamma = 1$ and $2R_N = R_P$. The power supply has a voltage of V_{DD} .

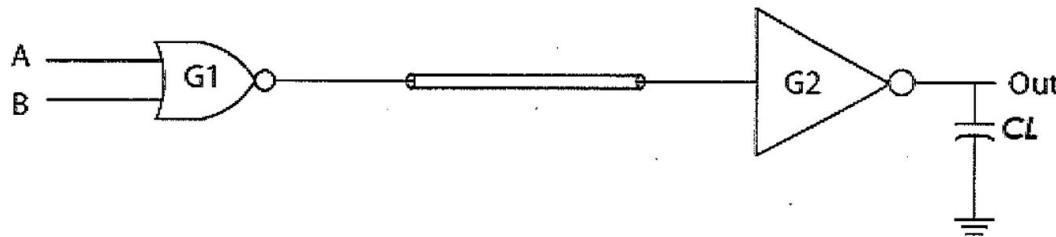


a) Determine the delay between input A to Out? (4 Pts)



Sp16 Midterm 2

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a) Determine the delay between input A to Out? (4 Pts)

$$t_1 = \ln 2 \left(R_1 \left(\frac{6}{5} C_1 + C_W + C_2 \right) \right) \quad t_2 = \ln 2 \left(R_2 (C_2 + C_L) \right)$$
$$t_{\text{total}} = t_1 + t_2$$

Fa16 Midterm 2

[PROBLEM 3] Energy (10 pts)

- a) (4 pts) How much energy is drawn from the 1V power supply in the circuit shown below in Fig 3a when I_{in} steps from 0V to 1V? How about when I_{in} steps from 1V to 0V? You can ignore all capacitors associated with the transistors inside of the inverter.

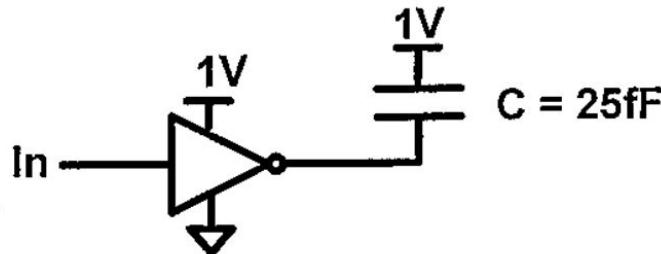


Figure 3a.

$$E = V_{DD} \cdot C [V_{DD} - 0] = CV_{DD}^2 = 25\text{fJ}$$

Fa16 Midterm 2

[PROBLEM 3] Energy (10 pts)

- a) (4 pts) How much energy is drawn from the 1V power supply in the circuit when V_c steps from 0V to 1V? How about when V_c steps from 1V to 0V? associated with the transistors inside of the inverter.

$0V \rightarrow 1V$

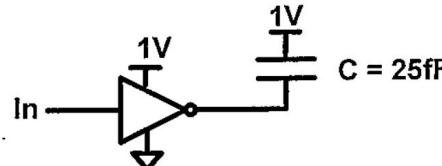
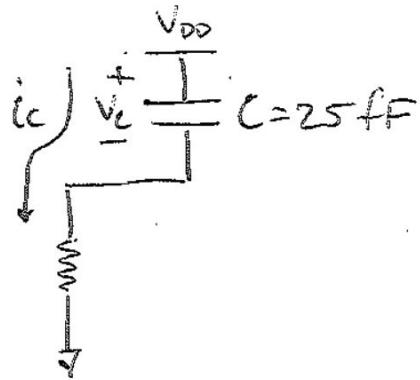


Figure 3a.

$$E = \int_{t=0}^{\infty} P dt = \int_{t=0}^{\infty} V_{DD} \cdot C \frac{dV_c}{dt} dt = \int_{t=0}^{\infty} V_{DD} \cdot C \cdot dV_c = V_{DD} \cdot C [V_c(\infty) - V_c(0)]$$

$$E = V_{DD} \cdot C [V_{DD} - 0] = CV_{DD}^2 = 25\text{fJ}$$

Fa16 Midterm 2

[PROBLEM 3] Energy (10 pts)

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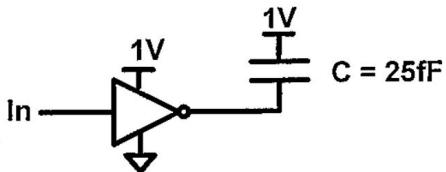
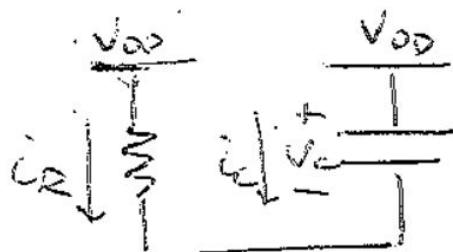


Figure 3a.

$V \rightarrow 0V$



$$i_R = -i_C$$

$$P = V_{DD} \cdot i_R + V_{DD} \cdot i_C = 0$$

$$\bar{E} = 0$$

Fa16 Midterm 2

- b) (6 pts) How much energy is pulled out of the 1V power supply in the circuit shown below when I_{in} steps from 1V to 0V? How about when I_{in} steps from 0V to 1V? You can ignore all capacitors associated with the transistors inside of the inverter.

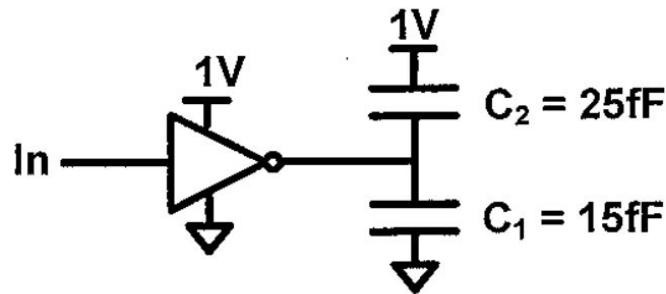


Figure 3b

Fa16 Midterm 2

- b) (6 pts) How much energy is pulled out of the 1V power supply in the circuit shown below when I_{in} steps from 1V to 0V? How about when I_{in} steps from 0V to 1V? You can ignore all capacitors associated with the transistors inside of the inverter.

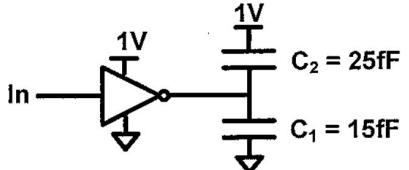
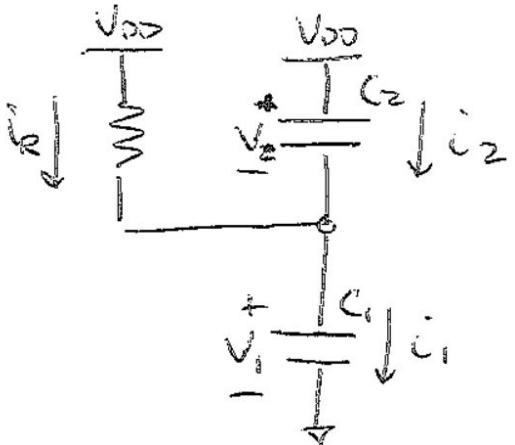


Figure 3b

$1V \rightarrow 0V$



$$i_2 + i_1 = i$$

$$P = V_{DD} \cdot i_2 + V_{DD} \cdot i_1 = V_{DD} \cdot i$$

$$i = C \frac{dV}{dt}$$

$$E = \int_{t=0}^{\infty} P dt = V_{DD} C_1 \cdot \int_{t=0}^{\infty} dV_1 = V_{DD} \cdot C_1 \left[V_1(\infty) - V_1(0) \right] = V_{DD}^2 \cdot C_1 = 15 fJ$$

Fa16 Midterm 2

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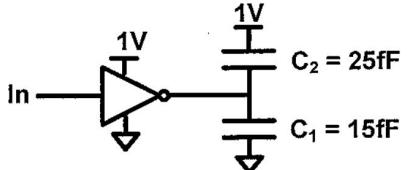
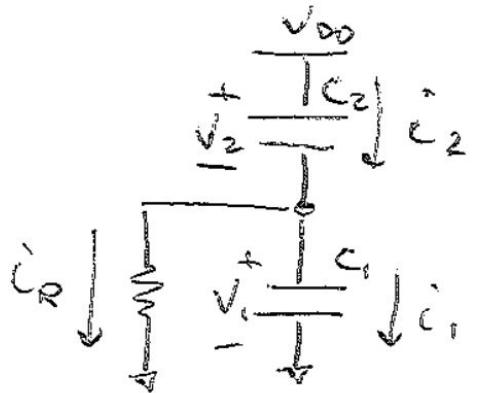


Figure 3b

$0V \rightarrow 1V$



$$P = V_{DD} \cdot i_2 \quad i_2 = C_2 \frac{dV_2}{dt}$$

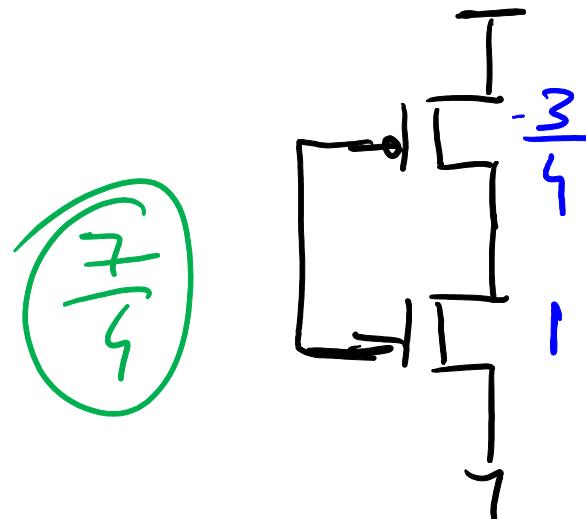
$$E = \int_{t=0}^{\infty} P dt = \int_{t=0}^{\infty} V_{DD} \cdot C_2 \cdot \frac{dV_2}{dt} dt$$

$$E = V_{DD} \cdot C_2 \cdot (V_2(\infty) - V_2(0)) = V_{DD}^2 \cdot C_2 = 25 \text{ fJ}$$

Logical Effort / RC Delay

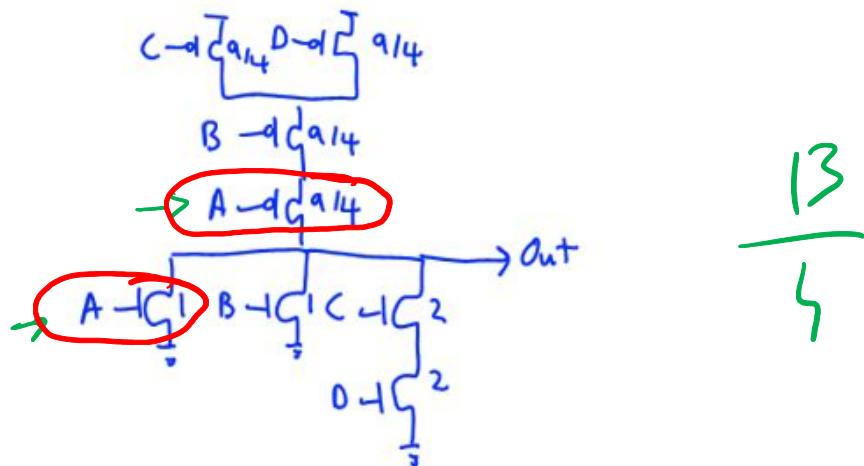
Sp17 Midterm 1

- a) (8 pts) Implement the function $F = \overline{A+B+C \cdot D}$ with a complex static CMOS gate. Assuming that for this process $R_P = 0.75 \cdot R_N$ (i.e., for the same width, a PMOS has 0.75 times the resistance of an NMOS), size your gate so that the worst-case pull up resistance is equal to the worst-case pull-down resistance.



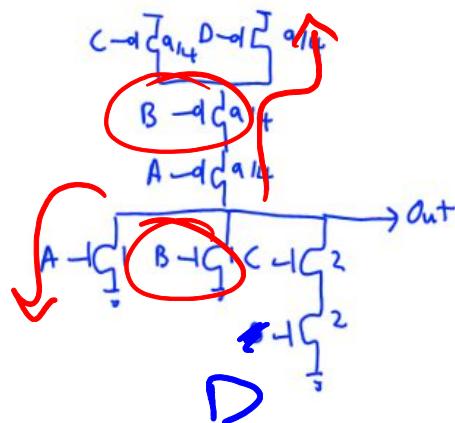
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Sp17 Midterm 1

- b) (8 pts) What is the logical effort of this gate from the A and C inputs?



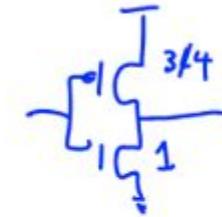
$$LE_A = \frac{R_{gate} \cdot C_{in, gate}}{R_{inv} \cdot C_{in, inv}} = \frac{\frac{13}{9}}{\frac{7}{9}} = \frac{17}{7}$$

$$LE_C = \frac{17}{7}$$

Sp17 Midterm 1

- b) (8 pts) What is the logical effort of this gate from the A and C inputs?

Reference inverter with same R as the gate:



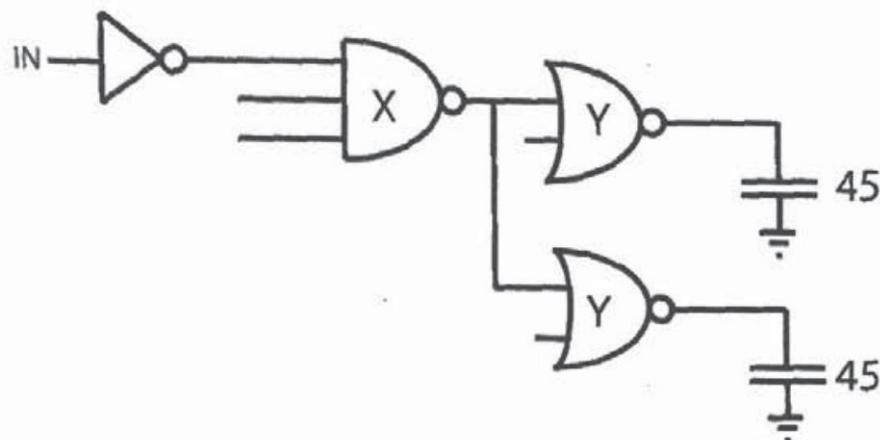
$$LE_A = \frac{13/4}{7/4} = \boxed{\frac{13}{7}}$$

$$LE_C = \frac{17/4}{7/4} = \boxed{\frac{17}{7}}$$

Sp16 Midterm 2

[PROBLEM 1] Logical Effort (15 pts)

Consider the following network of CMOS gates. Assume that the first inverter connected to IN is of size 1. Assume t_{p0} and γ equal to 1.

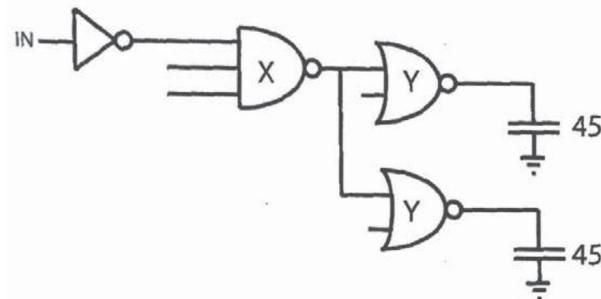


- a) Determine the Path Effort between IN and any of the two outputs OUT. (3 Pts)

Sp16 Midterm 2

[PROBLEM 1] Logical Effort (15 pts)

Consider the following network of CMOS gates. Assume that the first inverter connected to IN is of size 1. Assume t_{p0} and γ equal to 1.



- a) Determine the Path Effort between IN and any of the two outputs OUT. (3 Pts)

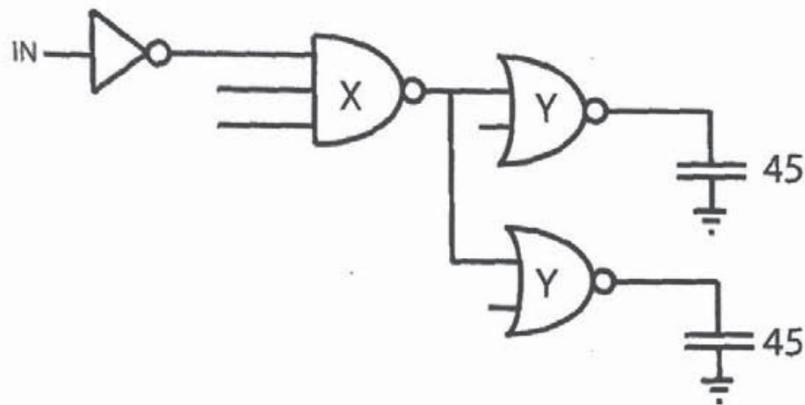
$$\text{Path Effort} = FGB$$

$$= (45) \left(\frac{5}{3}\right) \left(\frac{5}{3}\right) (2)$$

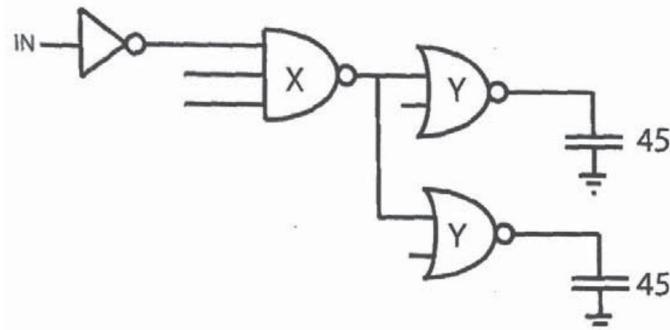
$$= \boxed{250}$$

Sp16 Midterm 2

b) Size X and Y to give the minimum delay and determine that minimum delay. (4 Pts)



Sp16 Midterm 2



$$f_1g_1 = f_2g_2 = f_3g_3 = \sqrt[3]{250} = 6.3$$

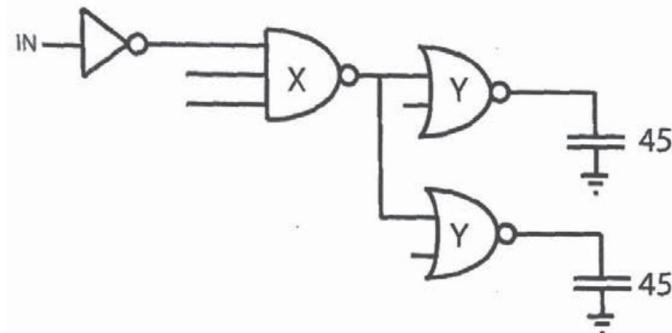
$$X = 6.3$$

$$f_2g_2 = 6.3 \rightarrow \frac{Y}{6.3} \cdot \left(\frac{5}{3}\right) = 6.3$$

$$Y_T = 23.8$$

$$Y = 11.9$$

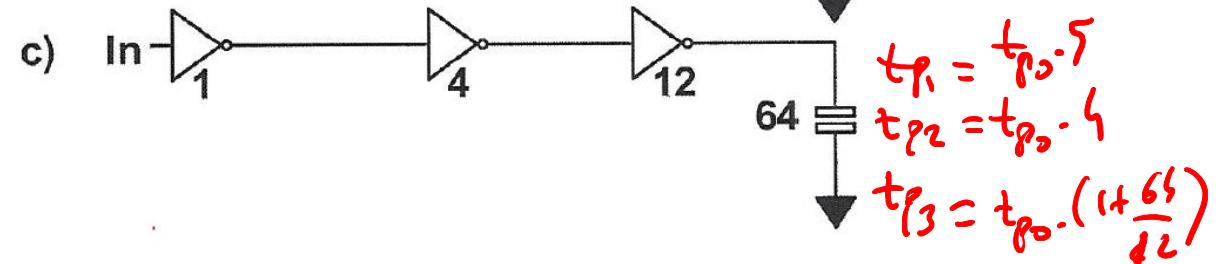
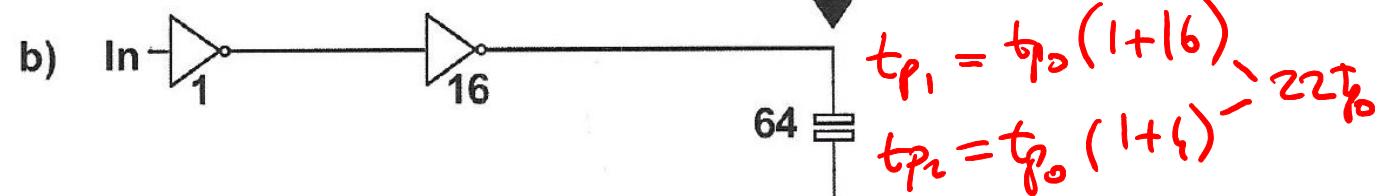
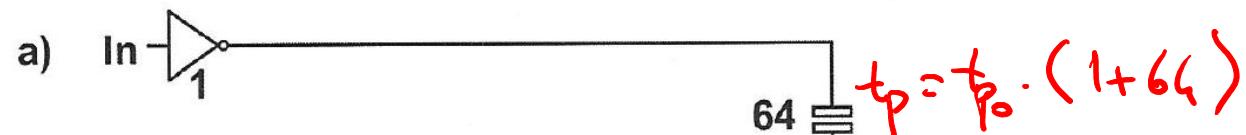
Sp16 Midterm 2



$$\begin{aligned} t_p &= t_{p0} \left[(\gamma + f_1) + (3\gamma + f_2) + \left(\frac{10}{3}\gamma + f_3 \right) \right] \\ &= t_{p0} \left[(1 + 6.3) + (2 + 6.3) + (3 + 6.5) \right] \\ &\approx \boxed{24.9 \text{ } t_{p0}} \end{aligned}$$

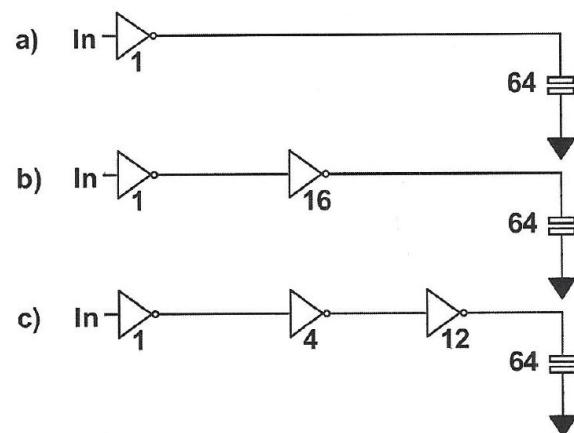
Sp16 Midterm 1

$$t_p = t_{p_0} (1 + f)$$



- a) Assume that the delay of a minimum size inverter is given by $t_p = 1 + f$ (that is $t_{p_0} = 1$ and $\gamma = 1$). f is the fanout. For each of the configurations shown, determine the delay between In and Out. (3 points)

Sp16 Midterm 1



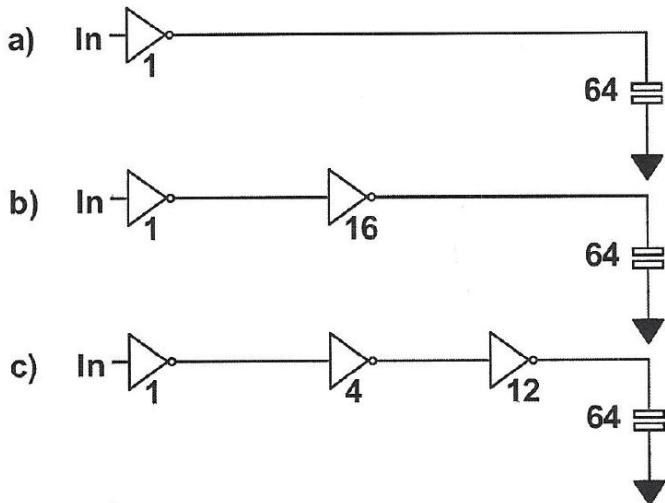
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$$(a) t_p = 1 + 63 = 65$$

$$(b) t_p = (1+16) + (1+5) = 22$$

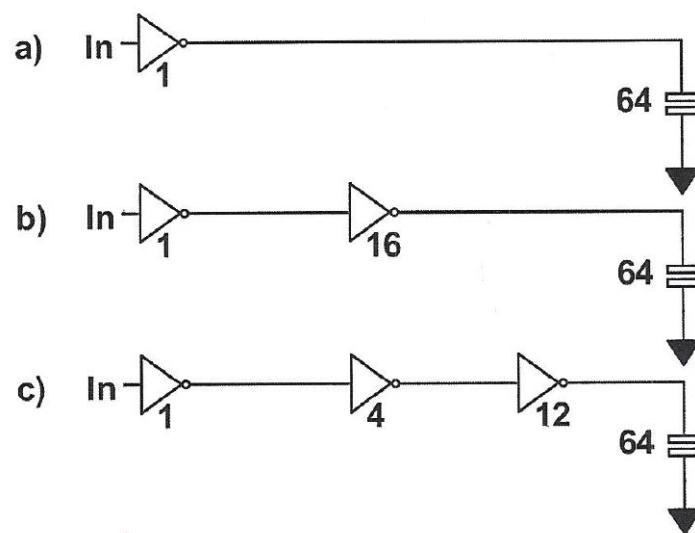
$$(c) t_p = (1+5) + (1+3) + \left(1 + \frac{16}{3}\right) = 15.33$$

Sp16 Midterm 1



- b) Assuming that the input inverter sizes are fixed to 1, size the other inverters so that the delay is minimized for each of the three configurations, and determine the corresponding delay. (4 points)

Sp16 Midterm 1



(a) same

(b)

$$f = \sqrt[2]{64} = 8 \Rightarrow t_p = (1+8)+(1+8) = 18$$

(c)

$$f = \sqrt[3]{64} = 4 \Rightarrow t_p = 15$$

Fa16 Midterm 2

[PROBLEM 2] Memory Decoders (12 pts)

Shown below is the critical path of a decoder for a 16x128 SRAM array. This decoder has been implemented by using a 2-4 predecoder, followed by a 4-16 final decoder. Both true and complementary addresses, A0-A3, are available, and the input capacitance per address bit is limited to $2C_{cell}$. $R_p = 2R_n$

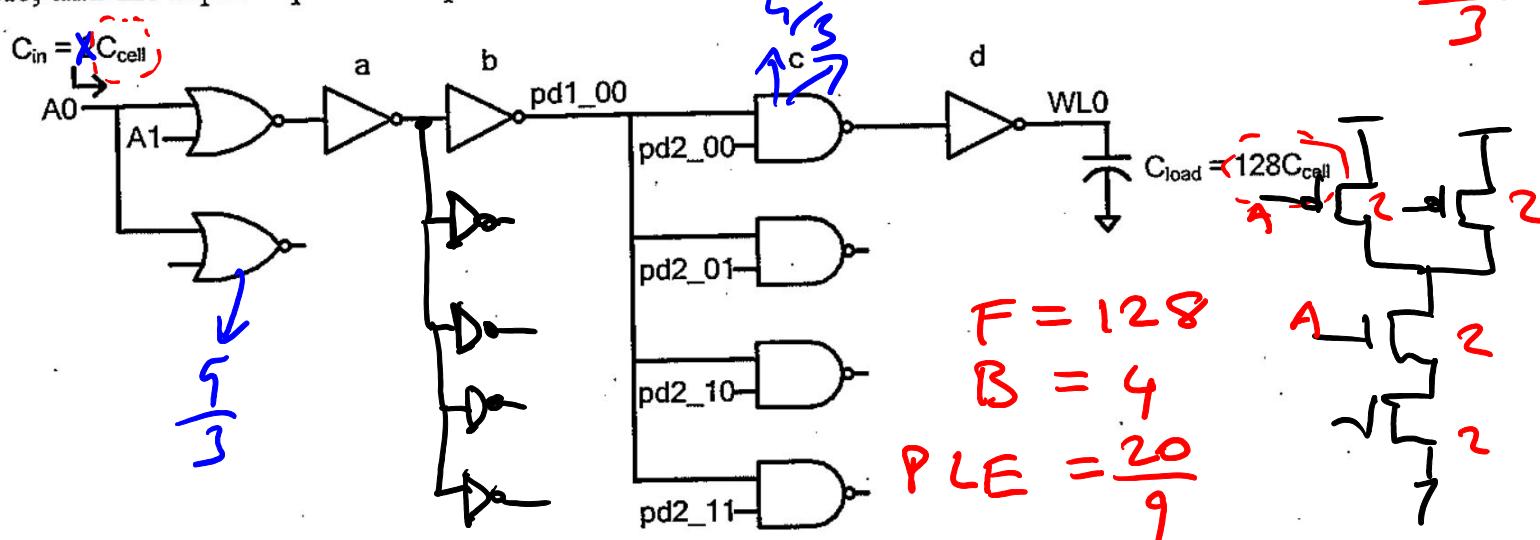


Figure2a

- a) (4 pts) What is the path effort from A0 to WL0?

Fa16 Midterm 2

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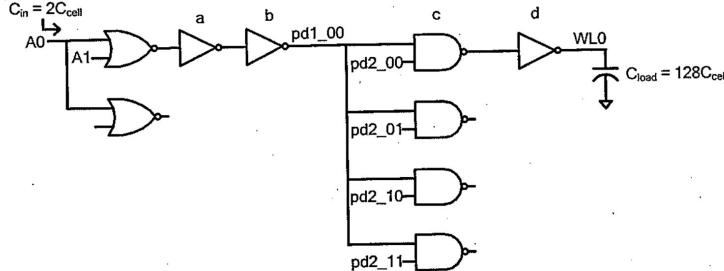


Figure2a

$$PE = H = FGB$$

$$F = \frac{128 C_{cell}}{2 C_{cell}} = 64$$

$$LE = G = \frac{5}{3} \cdot 1 \cdot 1 \cdot \frac{4}{3} \cdot 1 = \frac{20}{9}$$

$$B = 2 \cdot 1 \cdot 1 \cdot 4 \cdot 1 = 8$$

$$PE = H = 64 \cdot \frac{20}{9} \cdot 8 = \frac{10240}{9} \approx 1137.8$$

Fa16 Midterm 2

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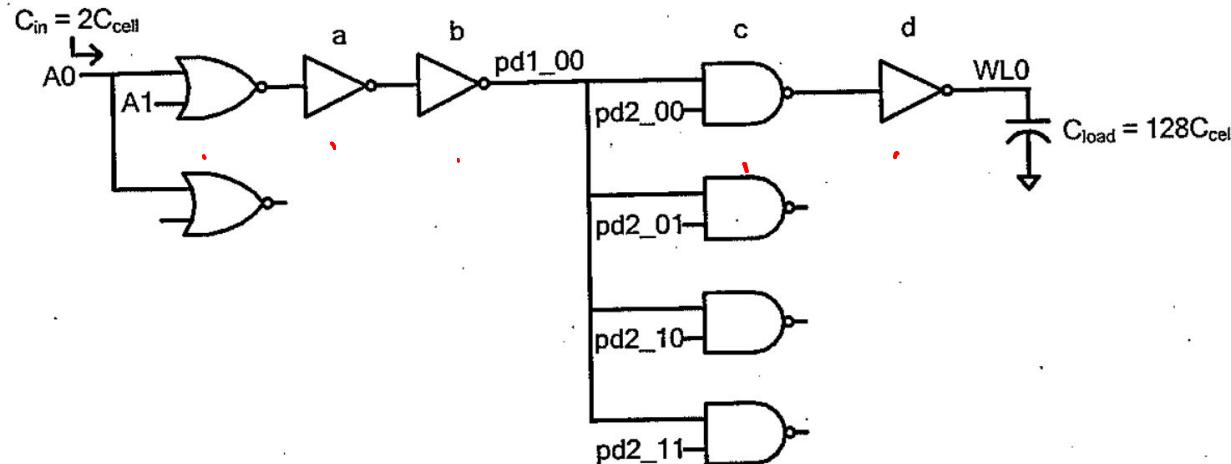


Figure2a

- b) (4 pts) What EF/stage minimizes the delay of this decoder?

Fa16 Midterm 2

[PROBLEM 2] Memory Decoders (12 pts)

Shown below is the critical path of a decoder for a 16x128 SRAM array. This decoder has been implemented by using a 2-4 predecoder, followed by a 4-16 final decoder. Both true and complementary addresses, A0-A3, are available, and the input capacitance per address bit is limited to $2C_{cell}$.

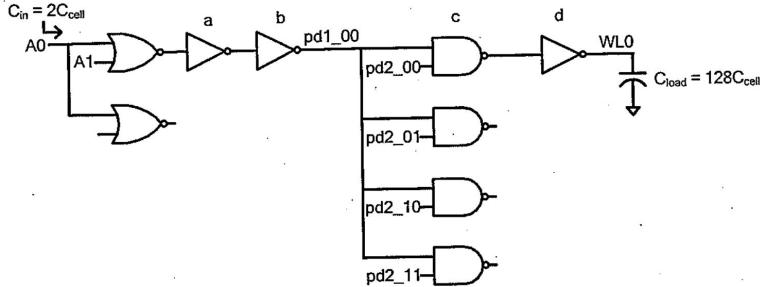


Figure2a

$$\frac{EF}{\text{stage}} = h = \sqrt[N]{H} \quad N=5$$

$$h = \sqrt[5]{1137.8} \approx 4$$

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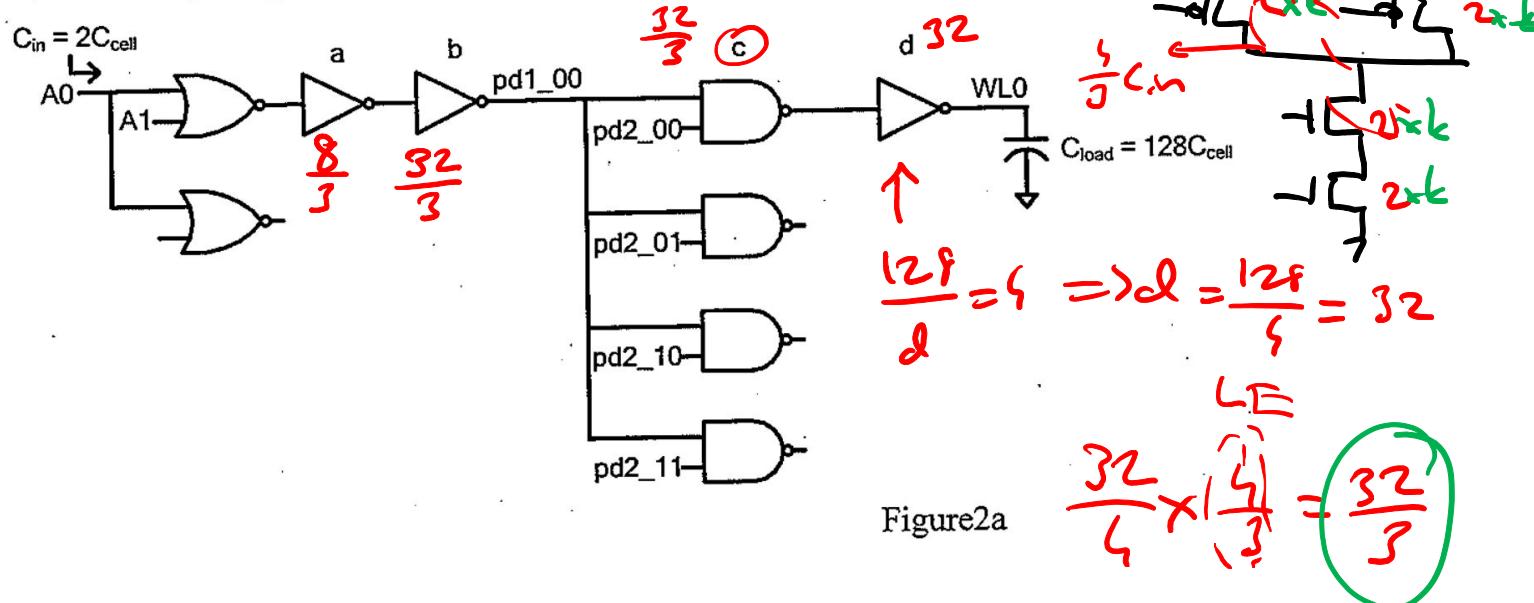


Figure2a

- c) (4 pts) Size the gates to minimize the delay from A0 to WL0.

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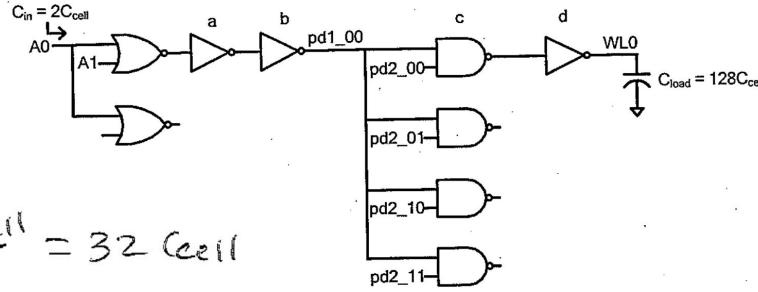


Figure2a

Size d:

$$f_d = \frac{n}{g_d} = \frac{4}{1} = 4$$

$$d = \frac{128 C_{cell}}{f_d} = \frac{128 C_{cell}}{4} = 32 C_{cell}$$

Size c:

$$f_c = \frac{n}{g_c} = \frac{4}{\left(\frac{4}{3}\right)} = 3$$

$$c = \frac{32 C_{cell}}{3} \approx 10.7 C_{cell}$$

Size b:

$$f_b = \frac{n}{g_b} = \frac{4}{1} = 4$$

$$b = \frac{4 \cdot \frac{32}{3} C_{cell}}{4} = \frac{32}{3} C_{cell} \approx 10.7 C_{cell}$$

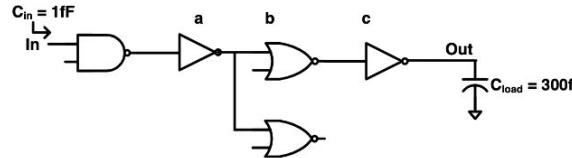
Size a:

$$f_a = \frac{n}{g_a} = \frac{4}{1} = 4$$

$$a = \frac{\frac{32}{3} C_{cell}}{4} = \frac{8}{3} C_{cell} \approx 2.7 C_{cell}$$

Sp17 Final

PROBLEM 1. Logical Effort and Gate Sizing (18 points + BONUS 6 pts)



a) (4 pts) What is the path effort from In to Out?

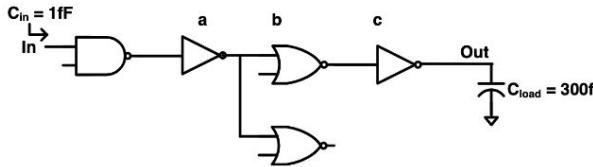
b) (2 pts) What EF/stage minimizes the delay of this chain of gates?

c) (6 pts) Size the gates to minimize the delay from In to Out.

Size	Value (fF)
a	
b	
c	

PROBLEM 1. Logical Effort and Gate Sizing (18 points + BONUS 6 pts)

Sp17 Final



- a) (4 pts) What is the path effort from In to Out?

$$PE = \pi LE \cdot \pi B \cdot F \\ = (s_3 \cdot 4s_3) \cdot 2 \cdot \frac{300ff}{1ff} = 1333.33$$

- b) (2 pts) What EF/stage minimizes the delay of this chain of gates?

$$EF_{\text{opt}} = (PE)^{1/4} \\ = 6.04$$

- c) (6 pts) Size the gates to minimize the delay from In to Out.

$$\frac{300ff}{c} = 6.04$$

$$\frac{c}{b} \cdot \frac{s}{3} = 6.04$$

$$\frac{2 \cdot b}{a} = 6.04$$

Size	Value (fF)
a	4.53
b	13.69
c	49.65

Fa16 Midterm 1

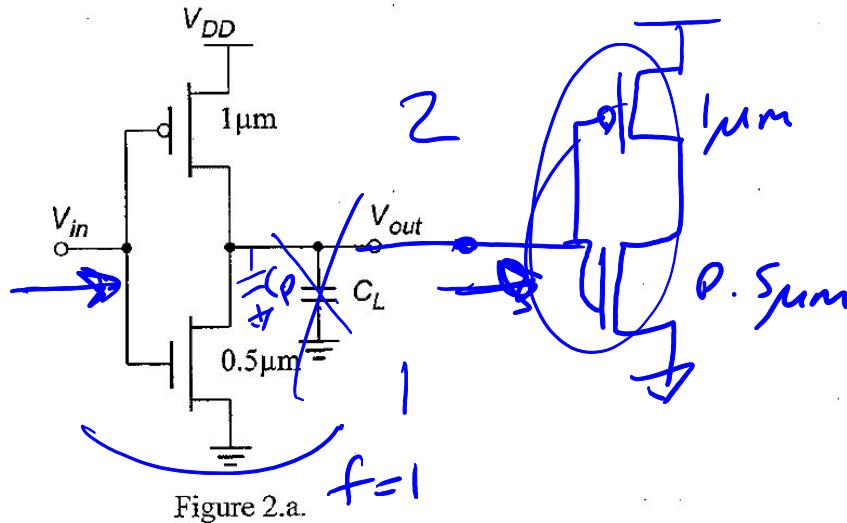
[PROBLEM 3] Inverter delay (16 pts)

Consider an inverter driving a capacitive load in $0.25\mu\text{m}$ CMOS technology, as shown in Figure 2.a.

$$t_{p,inv} = \tau_{inv}(1+f)$$

$$30\text{ps} = \tau_{inv}(1+1)$$

$$f = \frac{C_{in,inv}}{C_{in,inv}}$$



All transistors have minimum length and the inverter is symmetrically sized with $W_n = 0.5\mu\text{m}$ $W_p = 1\mu\text{m}$. In this technology, input (gate) capacitance and intrinsic (drain) capacitances are equal, $C_g = C_d = 2\text{fF}/\mu\text{m}$.

- a) (4pts) When this inverter drives another identical inverter of the same size, the delay is 30ps. What is the propagation delay for driving a 15fF load?

$\gamma = 1$

Fa16 Midterm 1

- a) (4pts) When this inverter drives another identical inverter of the same size, the delay is 30ps. What is the propagation delay for driving a 15fF load?

$$f = \frac{C_L}{C_g} = 1 \quad \underline{t_p = t_{po} \cdot \left(1 + \frac{f}{f}\right) = t_{po} \cdot \left(1 + \frac{1}{1}\right) = 30\text{ps}}$$

$$\boxed{t_{po} = 15\text{ ps}} \neq \tau_{inv}$$

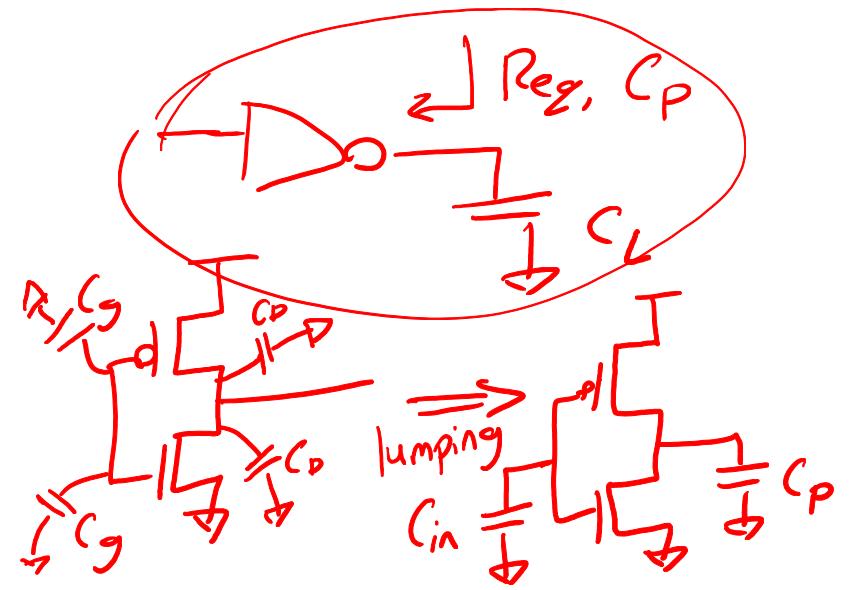
$$f = \frac{C_L}{C_g} = \frac{15\text{ fF}}{1.5\mu\text{m} \cdot 2\text{ fF}/\mu\text{m}} = 5$$

$$t_p = 15\text{ ps} \cdot \left(1 + \frac{5}{1}\right)$$
$$\boxed{t_p = 90\text{ ps}}$$

Adders

Sp13 Final

17. [4pts] Assume the delay through a full-adder cell (FA) is 1 from either input to either output, and the delay through a 2-input multiplexer (mux2) is 1 (from any input to output). What is the worse-case delay through an optimized 30-bit carry-select adder?



$$\left\{ \begin{array}{l} \text{Reg} \\ \overline{\text{Reg}} \end{array} \right\} \xrightarrow{\frac{1}{f}} C_p$$

$$t_{p,\text{inv}} = \text{Reg} (C_p + C_L)$$

$$= \text{Reg} C_p \left(1 + \frac{C_L}{C_p} \right)$$

$$= \text{Reg} C_p \left(1 + \frac{C_L}{C_{in} \cdot \delta} \right)$$

$$= \underbrace{\text{Reg} C_p}_{\text{intrinsic delay}} \left(1 + \frac{f}{\delta} \right)$$

$$= T_{inv} \left(1 + \frac{f}{\delta} \right), \quad \delta = 1$$

$$\frac{C_p}{C_{in}} = \delta$$

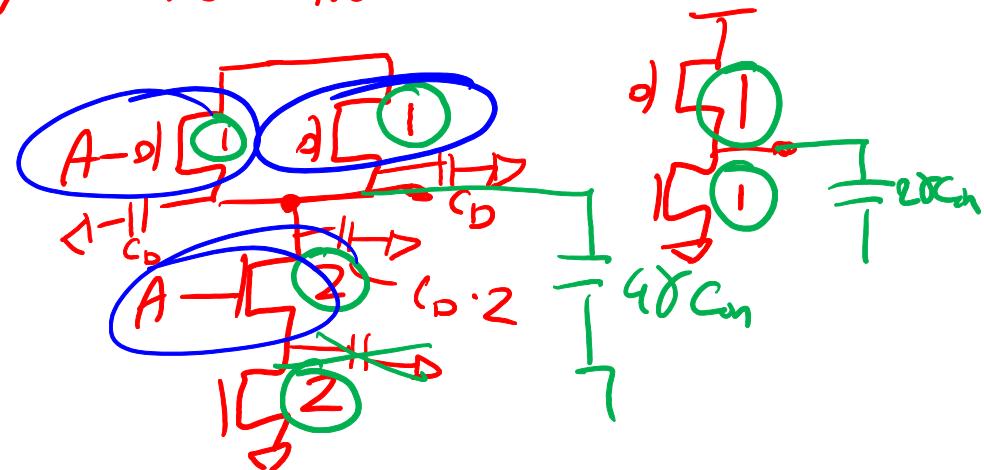
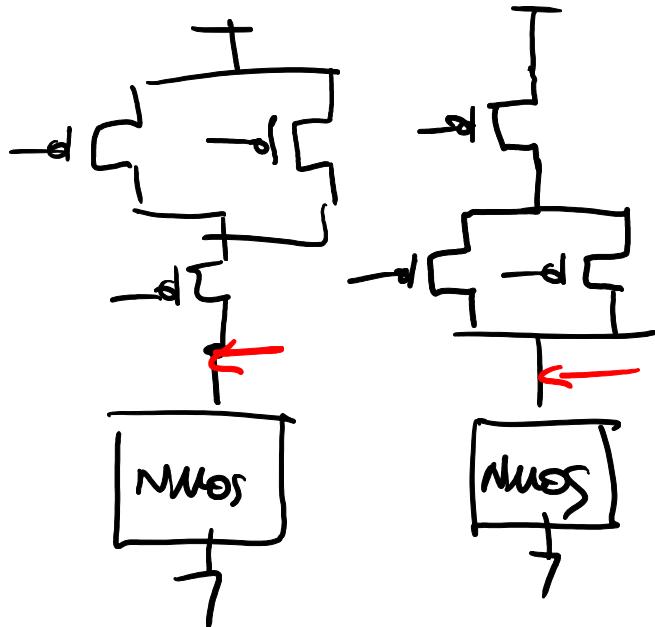
intrinsic delay

$$t_{p,\text{gate}} = T_{inv} (p + g_f) \xrightarrow{\text{LE}}$$

$$T_{inv} (1 + f) = T_{inv} \left(1 + \frac{f}{\delta} \right), \quad \delta = 1$$

- Size pullup / pulldown delays = ref inv

$$P = \frac{C_{out, gate}}{C_{out, inv}} = \frac{-}{C_P}$$



$$g = \frac{B}{2} \quad P = \frac{4\delta V_m}{2\delta V_m}$$

