EECS 151/251A Homework 6

Due Friday, October 25th, 2019

Problem 1: Riscy Hazards [5 pts]

Assume the datapath is pipelined as such:

1. It takes 15 cycles to finish 5 cycles and thus CPI = 3.

```
sub x3, x2, x4
add x1, x2, x3
add  x5, x4, x1
lw x1, 0(x2)
add x5, x4, x1
```

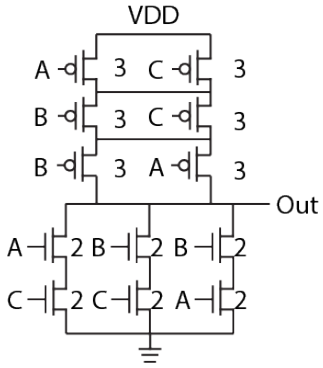
Cycle	F	D	X	M	W
1	sub (1)	-	-	-	-
2	add (1)	sub (1)	-	-	-
3	add (2)	add (1)	sub (1)	-	-
4	add (2)	add (1)	nop	sub (1)	-
5	add (2)	add (1)	nop	nop	sub (1)
6	lw (1)	add (2)	add (1)	nop	nop
7	lw (1)	add (2)	nop	add (1)	nop
8	lw (1)	add (2)	nop	nop	add (1)
9	add (3)	lw (1)	add (2)	nop	nop
10	-	add (3)	lw (1)	add (2)	nop
11	-	add (3)	nop	lw (1)	add (2)
12	-	add (3)	nop	nop	lw (1)
13	-	-	add (3)	nop	nop
14	-	-	-	add (3)	nop
15	-	-	-	-	add (3)

2. It should take 9 cycles for these 5 instructions. There will be increased delay which might actually become the critical path and seriously effect the clock period.

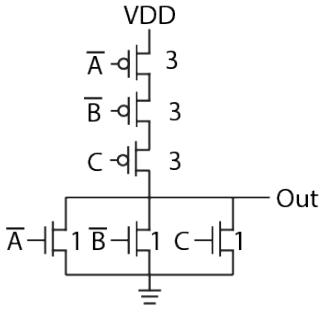
Cycle	F	D	X	M	W
1	sub (1)	-	-	-	-
2	add (1)	sub (1)	-	-	-
3	add (2)	add (1)	sub (1)	-	-
4	lw (1)	add (2)	add (1)	sub (1)	-
5	add (3)	lw (1)	add (2)	add (1)	sub (1)
6	-	add (3)	lw (1)	add (2)	add (1)
7	-	-	add (3)	lw (1)	add (2)
8	-	-	-	add (3)	lw (1)
9	-	-	-	-	add (3)

Problem 2: Complex CMOS gates [5 pts]

1. $Y = \overline{AB + AC + BC}$ Sizing done assuming 1:1 Nmos to PMOS ratio.



2. Function could be simplified! $Y = \overline{\overline{AB} + AC + BC} = \overline{\overline{A} + \overline{B} + C}$. It's a static gate and thus the voltage limits will actually always be VDD and GND!



Problem 3:Pass Gates and VTCs [5 pts]

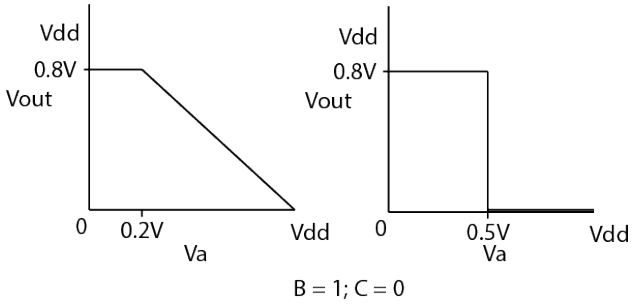
1. You should be able to read the minterms right off the bottom three branches. $Y = \overline{A}(\overline{B} + \overline{C})$

A	B	C	Out
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

2. Is this a static gate?? You could argue that if A and B are generated from ideal inverters then the output will always be connected to either VDD or GND. Remember since these are all nmos gates, the output can only go between $0V$ and $VDD - 2V_T$.

   Though, this is certainly not dynamic logic - there is no clock or multi-phase (pre-charge, etc..) operation. But, you could also argue that it's not quite static because the inputs might not be generated straight from VDD or GND. Credit should be given for any of these reasons, the point of the problem was for the students to pick a side and argue with a clear reasoning.

3. Remember that the output cannot go above $VDD - V_T$ because NMOS transistors can't pass strong 1s! Due to some issues from the clarifications there are actually two possible answers (either figure below is acceptable).



4. The circuit does not go rail to rail! It goes from GND to $VDD - V_T$ ($0Vto0.8V$). A Complementary CMOS version would solve this and allow the output to go rail to rail.