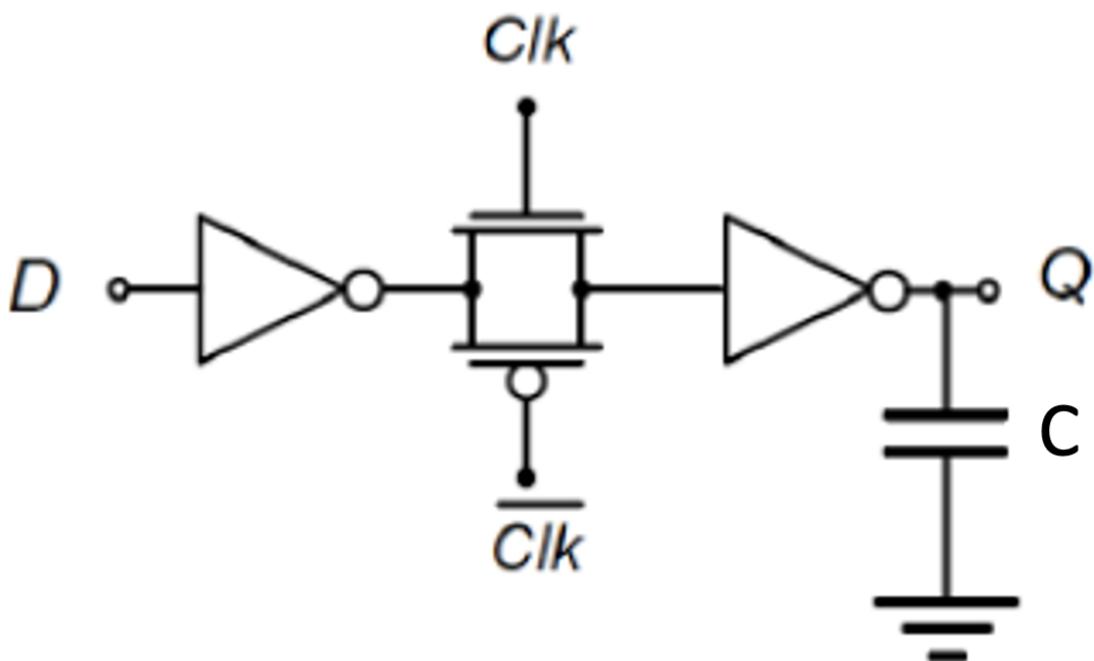


Homework 9

Due: 11/15/21 11:59pm

Problem 1: Latch Design

For this question, we will look into the latch design shown below. You may assume that the inverters are symmetrical with input capacitance C , self-loading capacitance also equal to C , and equivalent driving resistance R . Assume ideal VTCs for the inverters such that any tiny voltage above or below $VDD/2$ flips its output. The transmission gate is sized to have an equivalent resistance R and parasitic capacitance C on each side.



- a) Calculate the Clk-Q delay as a function of R and C of this latch. (hint: draw the equivalent RC circuit). If R is 10kohm and C is 10pF, what is the total clk-Q delay?

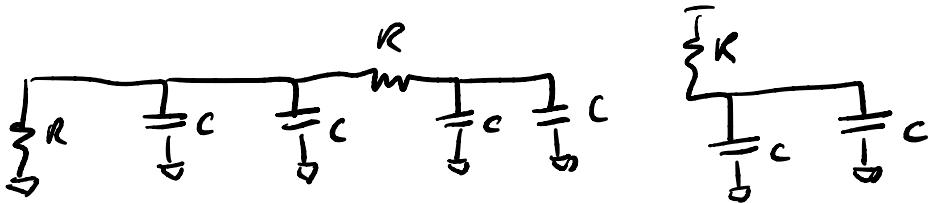
need path to VDD or $6N0$, but can assume output C already charged.

(dis) 0.4 μs (round to tenth).

$\text{delay} = \ln(2) [2RC + 2RC + 2RC]$

$$\begin{aligned}
 &= 6 \ln(2) RC \\
 &\approx 4.14 \times 10^{-7} \text{ s} \\
 &= 0.414 \text{ ps}
 \end{aligned}$$

- b) Calculate the D-Q delay as a function of R and C of this latch. (hint: draw the equivalent RC circuit). If R is 10kohm and C is 10pF, what is the total D-Q delay?



$$\begin{aligned} t_{D-Q} &= \ln(2) [4RC + 2RC + 2RC] = 8 \ln(2) RC \\ &= 5.52 \times 10^{-9} s \\ &= 0.552 \mu s \end{aligned}$$

0.6 μs (round to tenth).

- c) What is the approximate setup time for this latch given R is 10kohm and C is 10pF?

for latches, calculate setup time wrt closing edge of clk
want data to settle at input of second inverter by
the time clk goes low

$$\begin{aligned} t_{su} &= \ln(2) [4RC + 2RC] = 6 \ln(2) RC \\ &= 0.414 \mu s \end{aligned}$$

0.4 μs (round to tenth).

- d) What is the approximate hold time for this latch given R is 10kohm and C is 10pF?

assuming transmission gate immediately shuts off when the
clk goes low, need data at input of transmission gate to
have stayed steady so that new data doesn't propagate through.
Hold time is negative as the input data may change before
clk goes low, as long as it doesn't reach the input of the transmission
gate!

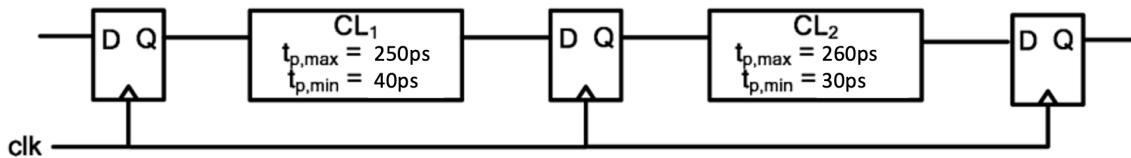
-0.1 μs (round to tenth).

$$t_h = -2 \ln(2) RC = 1.38 \times 10^{-9} s = 0.1 \mu s$$

would also accept explanation that data at output of transmission gate
remains steady, so $t_h = -6 \ln(2) RC = -0.4 \mu s$

Problem 2: Timing and clock distribution

In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: $t_{clk-q} = 40\text{ps}$, $t_{setup} = 35\text{ps}$, and $t_{hold} = 20\text{ps}$. You can assume that the clock has no jitter.



- a) What is the minimum clock cycle time for this pipeline?

largest delay is CL_2 , calculate t_{clk} from this:

$$t_{clk-q} + t_{p,max} \text{ } CL_2 + t_{setup} \leq t_{clk}$$

$$t_{clk} \geq 40\text{ps} + 260\text{ps} + 35\text{ps}$$

$$\underline{335} \text{ ps}$$

$$t_{clk} \geq 335\text{ps}$$

- b) Are there any minimum delay violations (yes/no)?

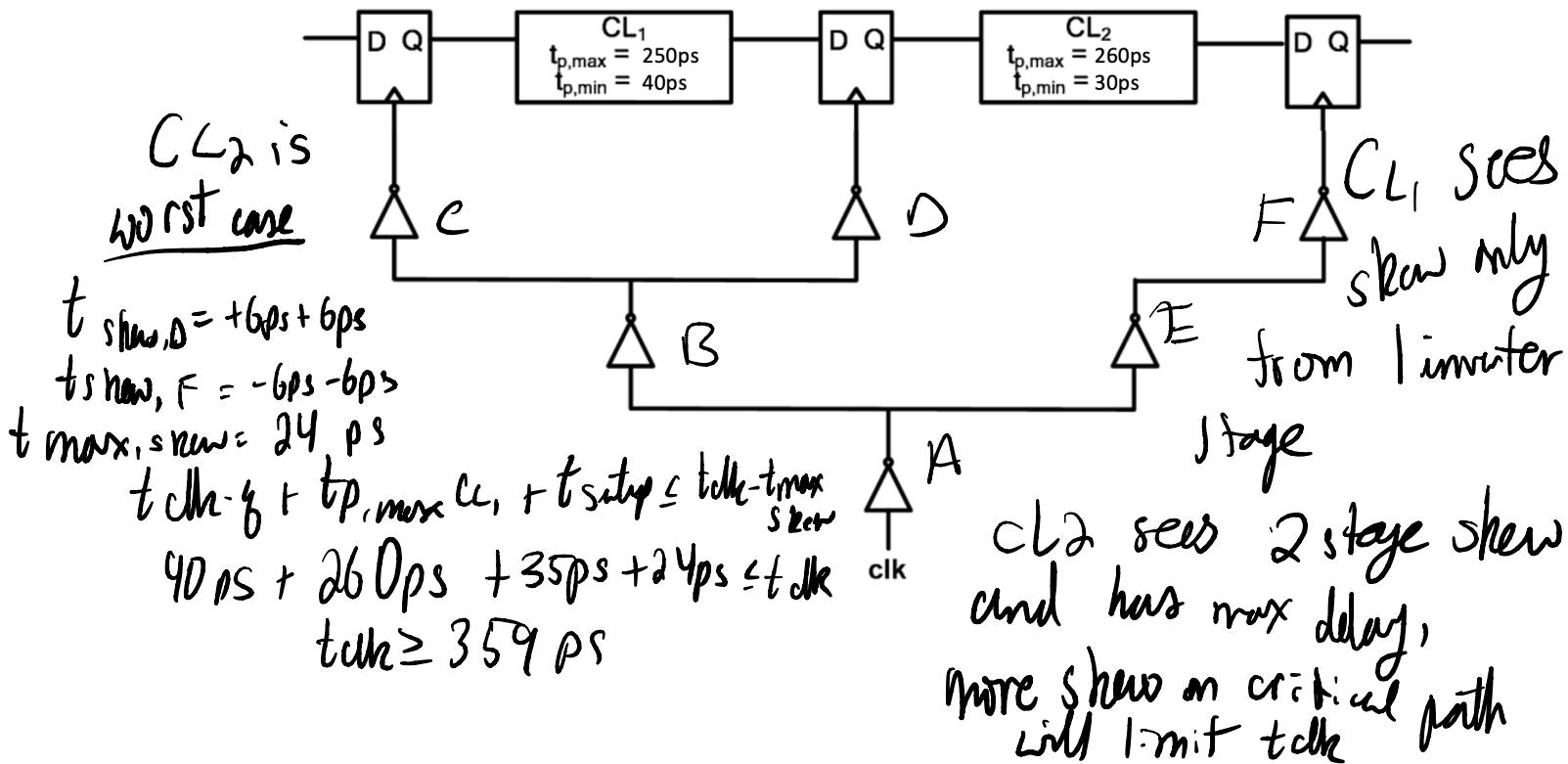
$$t_{clk-q} + t_{p,min} \text{ } CL_2 \geq t_{hold}$$

$$40\text{ps} + 30\text{ps} \geq 20\text{ps} \quad \checkmark$$

no

no violation

- c) Now we include the clock distribution network for this pipeline. Assuming that the delay of each inverter is nominally 40ps, but that each inverter's delay varies randomly by +/- 15%, now what is the minimum clock cycle time?



359 ps

- d) Under these same conditions (i.e., 40ps nominal inverter delay, +/-15% delay variation), can this pipeline fail any minimum delay constraints (yes/no)?

CL₂ sees 2-stage skew and has $t_{p,min}$, so it will be the critical case.

worst case skew for hold time means clock on F arrives late and clk on E arrives early, allowing data more time to race through. worst case still 24ps ($t_{skew,D} = -6ps - 6ps, t_{max,skew} = 6 + 6 = 12ps$)

$t_{dly-g} + t_{p,min} CL_2 \geq \text{hold} + t_{skew,max}$

$40ps + 30ps \geq 20ps + 24ps \quad \checkmark$

no violation