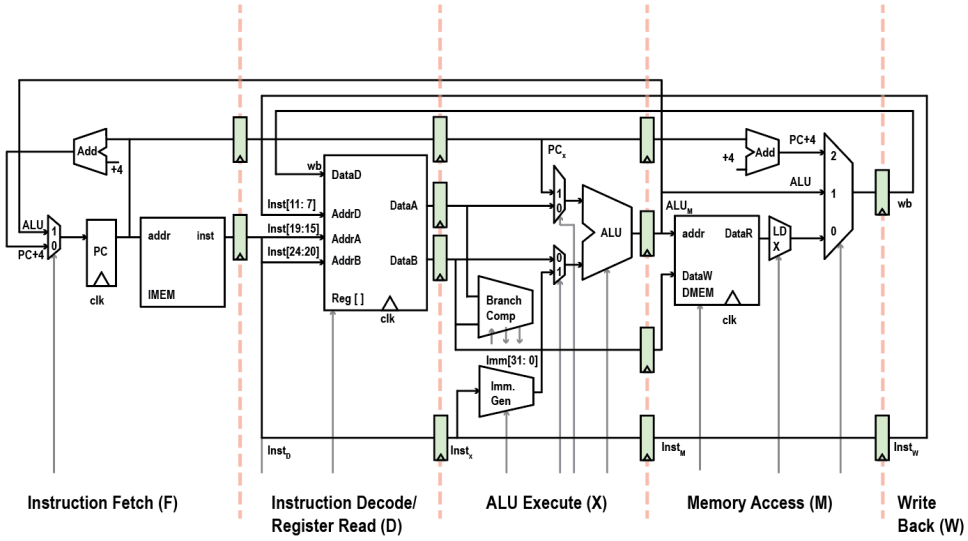
EECS 151/251A Homework 5

Due 11:59pm Friday, October 15th, 2021

1 Pipelines

Assuming a 5-stage RISC-V processor pipeline without any forwarding implemented (like below), draw a pipeline table for the following code snippet. How many cycles will the instructions take to execute? Note that the table is just an example and is not complete. Assume synchronous writes and asynchronous read, and the data in the write back stage can be read at the same cycle.




```
sub  x5, x2, x4
addi x2, x5, 16
lw   x1, 4(x2)
add  x3, x1, x4
```

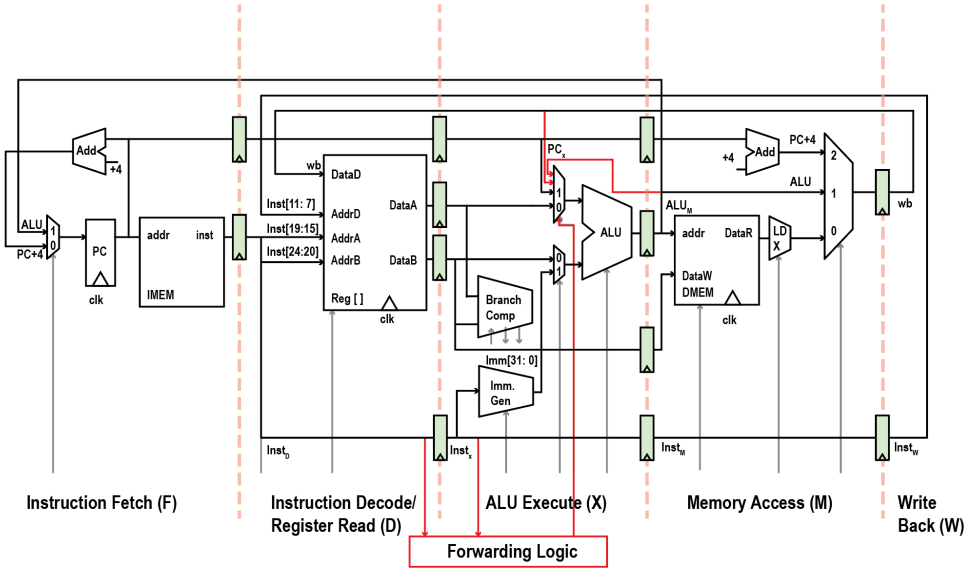
(a) It takes ____ cycles

Cycle	F	D	X	M	W
1	add	-	-	-	-
2	sub	add	-	-	-

(b) Fill in the instructions in each stage when Cycle = 7 in the blanks below. (Use `nop` if this stage need stall. Use `-`, if there is no more command or the first command has not reached this stage.)

F	D	X	M	W

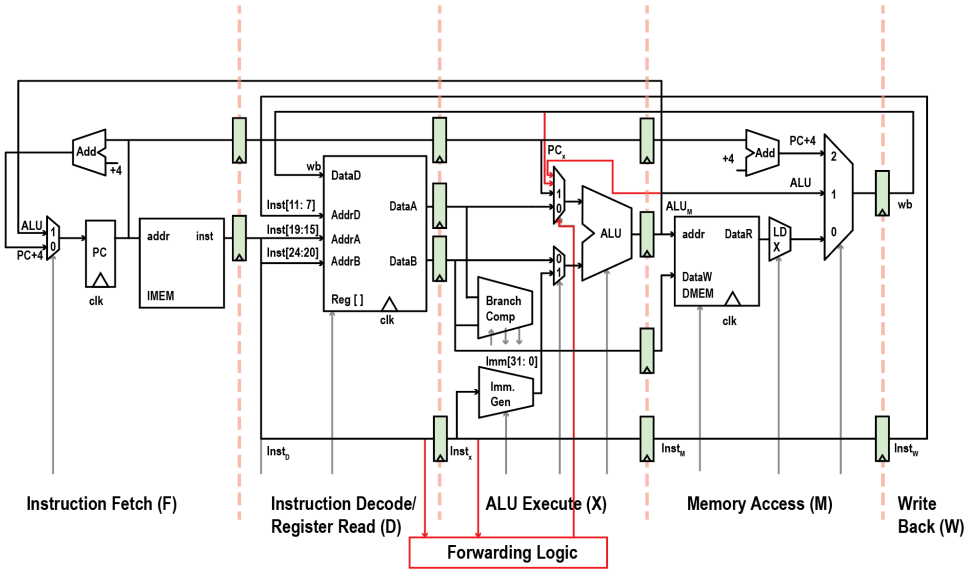
(c 251 Only) Now redraw the 5 stage pipeline with forwarding paths from the ALU output. How many cycles will the instructions take to execute?



It takes [ ] cycles

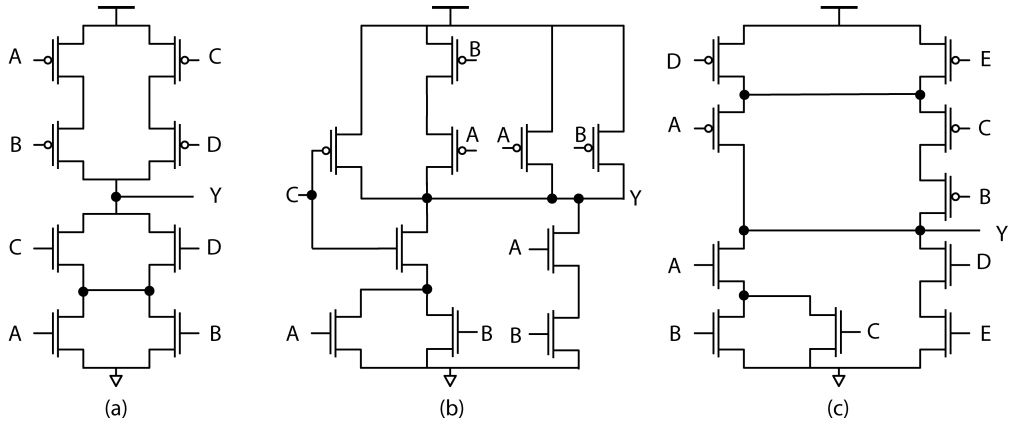
(d 251 Only) Fill in the command when Cycle = 5 in the blanks (Use `nop` if this stage need stall. Use `-` if there is no more command or the first command has not reach this stage.)

F	D	X	M	W



2 Complementary CMOS

Choose the simplified boolean expression for the function described by the CMOS circuit below.



(a)

A) $\overline{(A+B)(C+D)}$

B) $\overline{(AB+CD)}$

C) $\overline{(AC+DB)}$

D) $\overline{(A+C)(D+B)}$

(b)

A) $\overline{AB} + \overline{C}(\overline{A} + \overline{B})$

B) $\overline{AB + C(A + B)}$

C) $\overline{(A + B)(C + AB)}$

D) $(A + B)(C + AB)$

(c)

A) $\overline{A(B + C) + DE}$

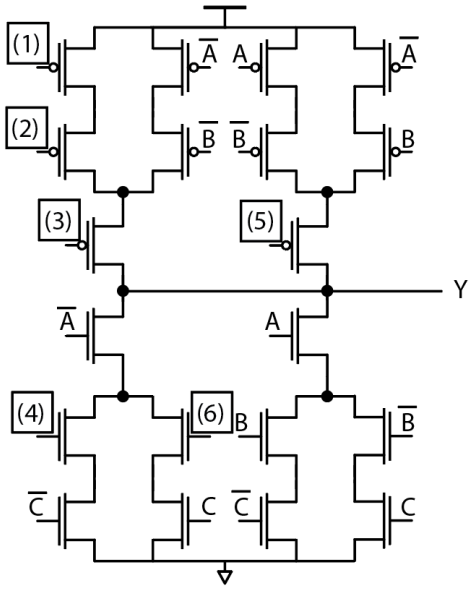
B) $(D + \overline{E})(\overline{A} + \overline{BC})$

C) $\overline{(D + E)(A + BC)}$

D) $(\overline{A}(\overline{B} + \overline{C}) + \overline{DE})$

3 XOR

(a) Below is a CMOS implementation of a 3-input XOR gate. Complete the circuit by filling in the signal name in the boxes.



1	2	3	4	5	6

A)

A	B	C	$\overline{B}$	$\overline{C}$	B

B)

A	B	$\overline{C}$	$\overline{B}$	C	B

C)

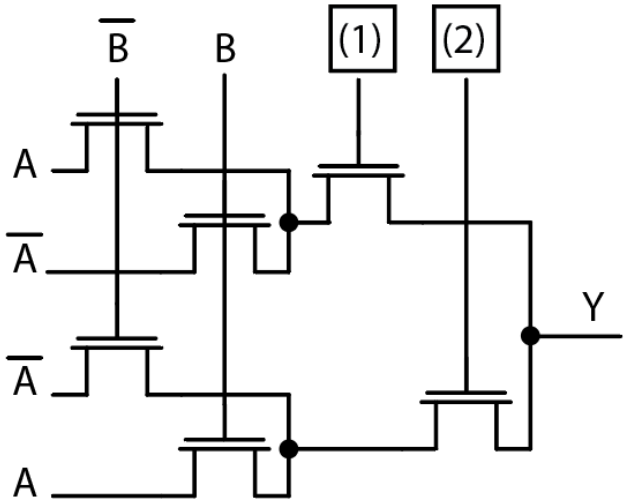
A	B	C	B	$\overline{C}$	$\overline{B}$

D)

A	B	$\overline{C}$	B	C	$\overline{B}$

(b) Is the gate shown above a complementary CMOS gate?

(c) Below is a passgate logic implementation of a 3 input XOR gate. Choose the signals that connect to the second stage NMOS gates.



1	2

A)

C	$\overline{C}$

B)

$\overline{C}$	C

C)

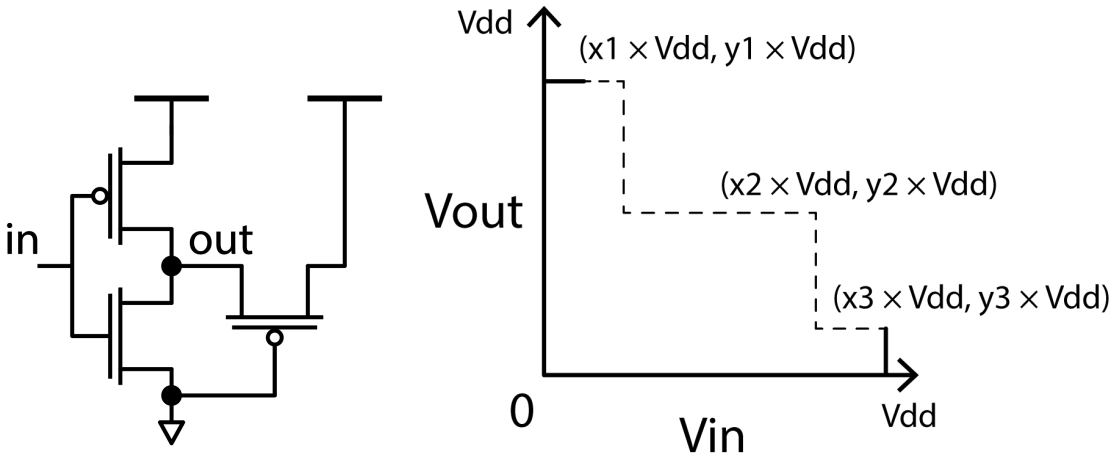
C	C

D)

$\overline{C}$	$\overline{C}$

4 Voltage Transfer Characteristic (VTC)

Using the transistor-as-a-switch model, write transition points in the voltage transfer characteristic for the circuit below. You will eventually recognize this as half of a 6T CMOS SRAM bit-cell. Assume that $|V_{th,p}| = V_{th,n} = V_{DD}/4$ and that $R_{on,p} = R_{on,n}$. For example, if the transition point is $(\frac{1}{2}V_{dd}, \frac{1}{3}V_{dd})$, write $\frac{1}{2}, \frac{1}{3}$ in the boxes. If there is only one or two transition points in the middle of the VTC, write $0, 0$ in the boxes.



(x1,y1)

(x2,y2)

(x3,y3)
