

# EECS 151/251A

## Discussion 7

Alisha Menon

10/12/21, 10/13/21, 10/18/21

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# Administrivia

- Slip week for labs – lab 5 due **10/15, 11:59pm**
- Homework 5 posted, due **10/15, 11:59pm**

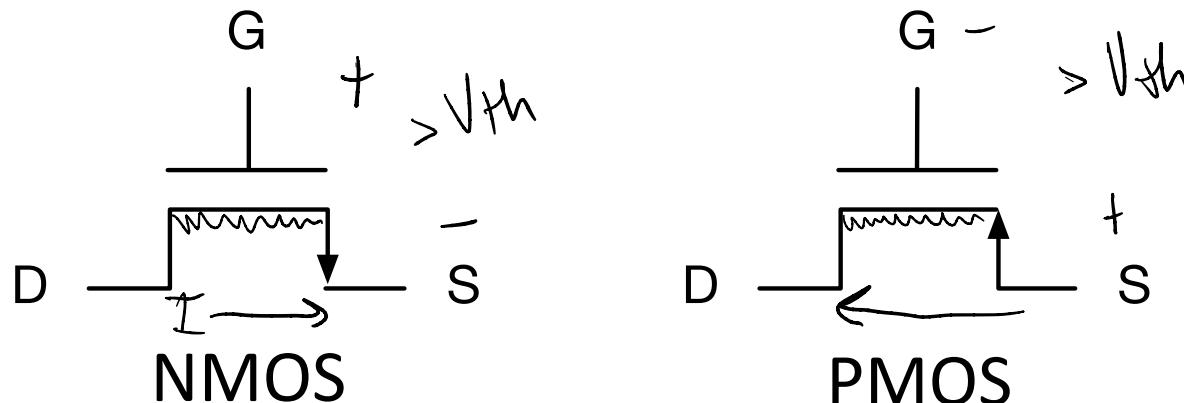
# Agenda

- Transistor as a switch model
- Inverter
- Complementary CMOS gates

# Transistor Models

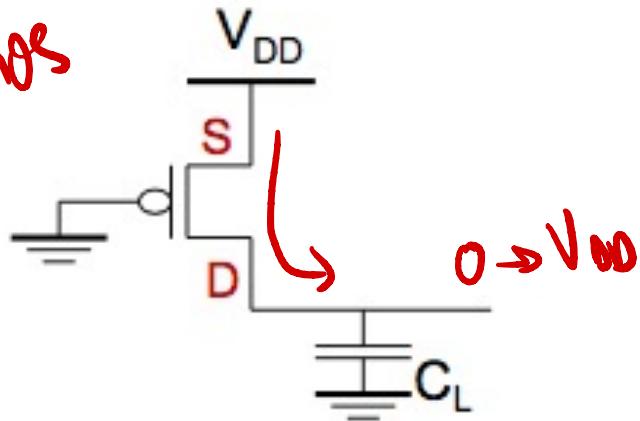
# Transistor review

- CMOS
  - Complementary Metal Oxide Semiconductor (FET)
- Transistor basics
  - N-type or P-type – based on carrier type
  - Potential between source and gate forms a “channel”
  - Channel connects source and drain
  - Defined by “threshold” voltage  $V_{th}$

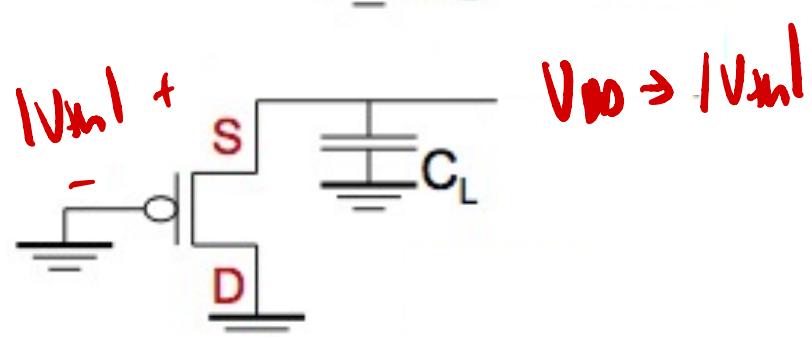
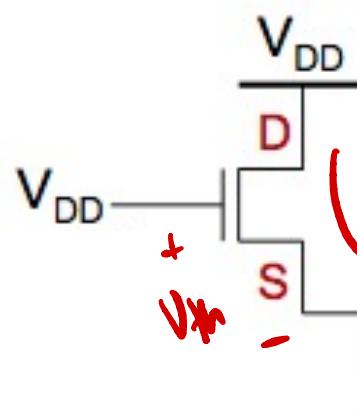
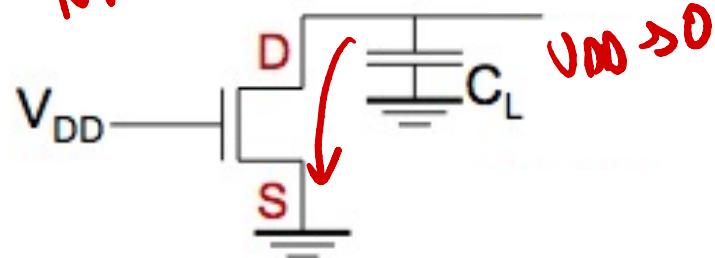


# Transistors connect outputs to supplies

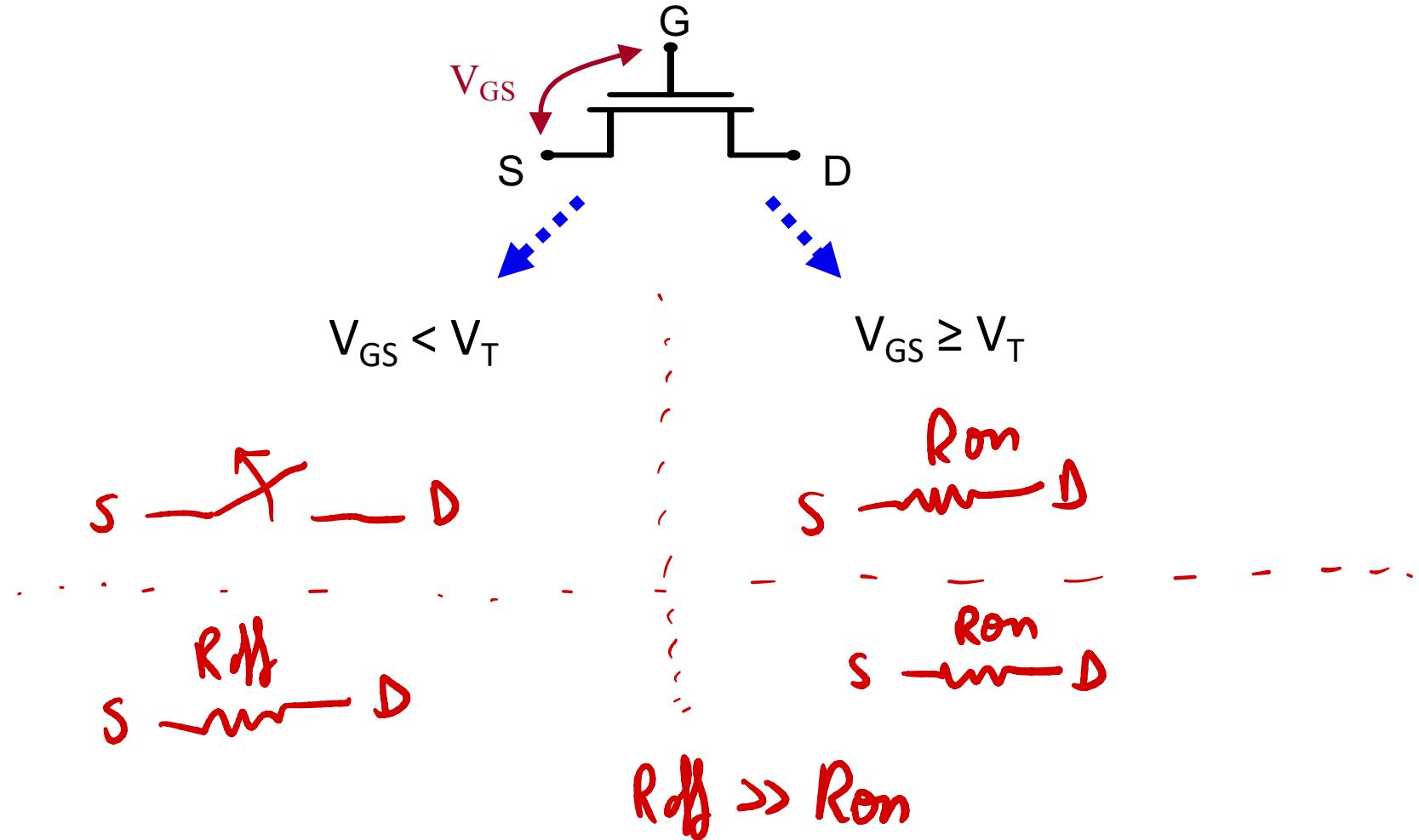
pmos



NMOS



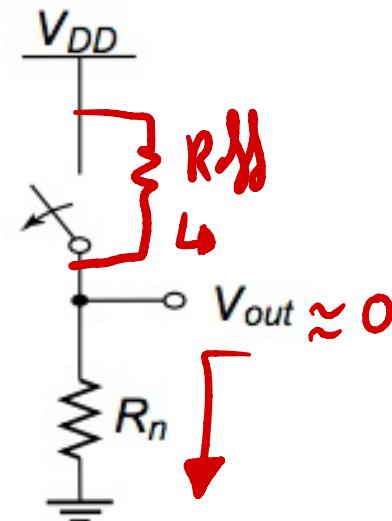
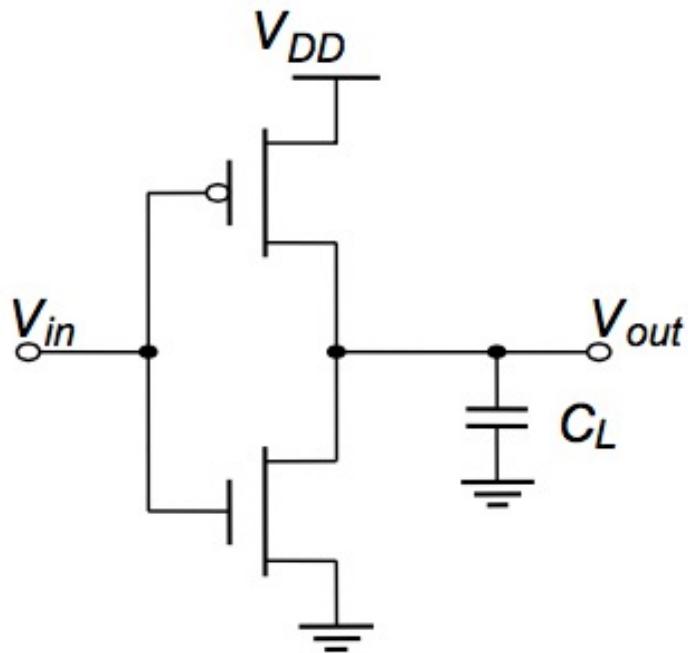
# Transistors as switches



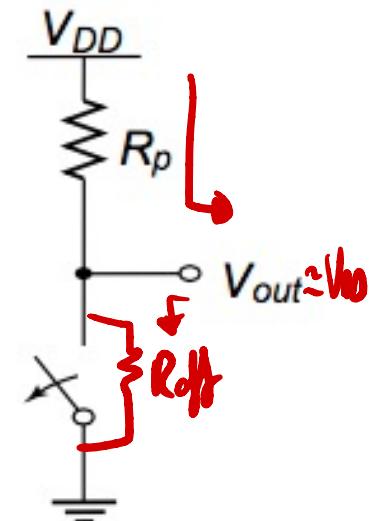
# Inverters

# CMOS inverter

Most basic CMOS logic gate



$$V_{in} = V_{DD}$$



$$V_{in} = 0$$

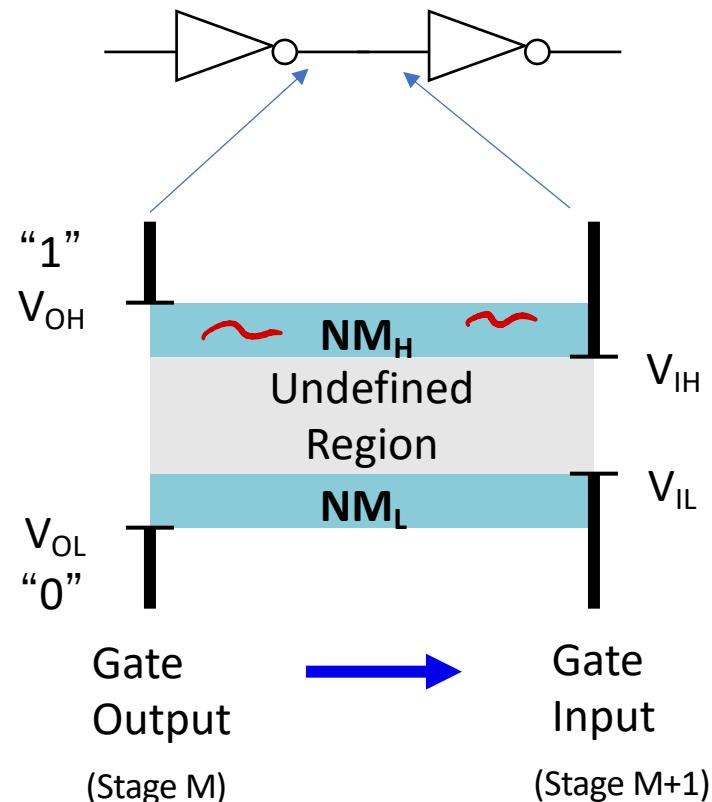
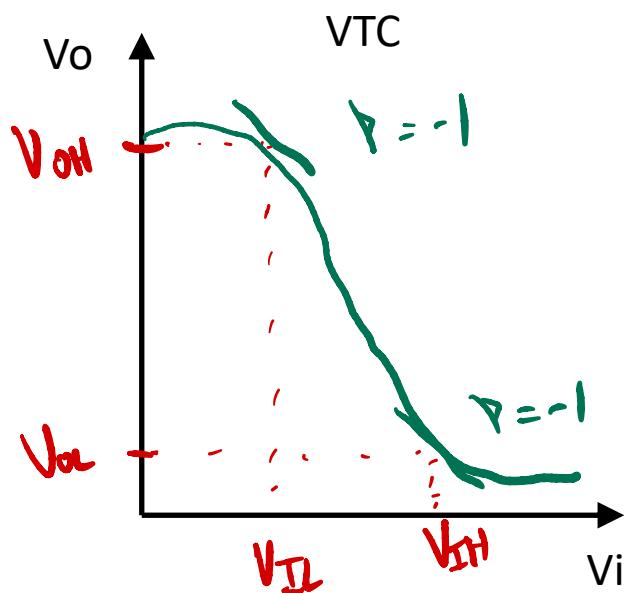
# Inverter noise margins

Noise margin high:

$$NM_H = V_{OH} - V_{IH}$$

Noise margin low:

$$NM_L = V_{IL} - V_{OL}$$

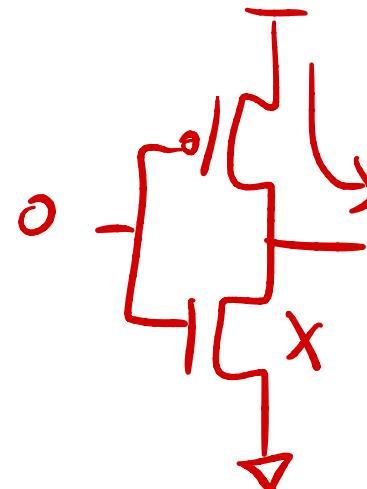
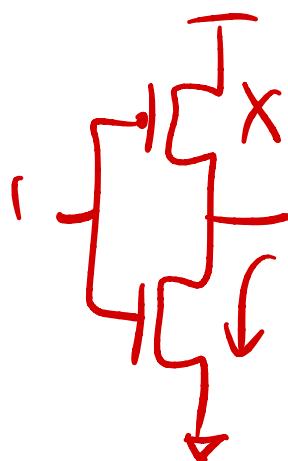
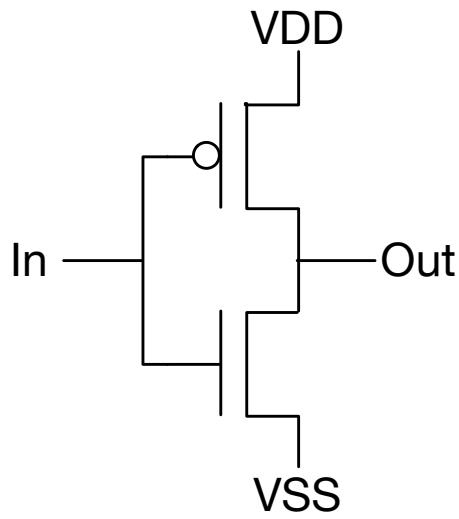


# Static complementary CMOS

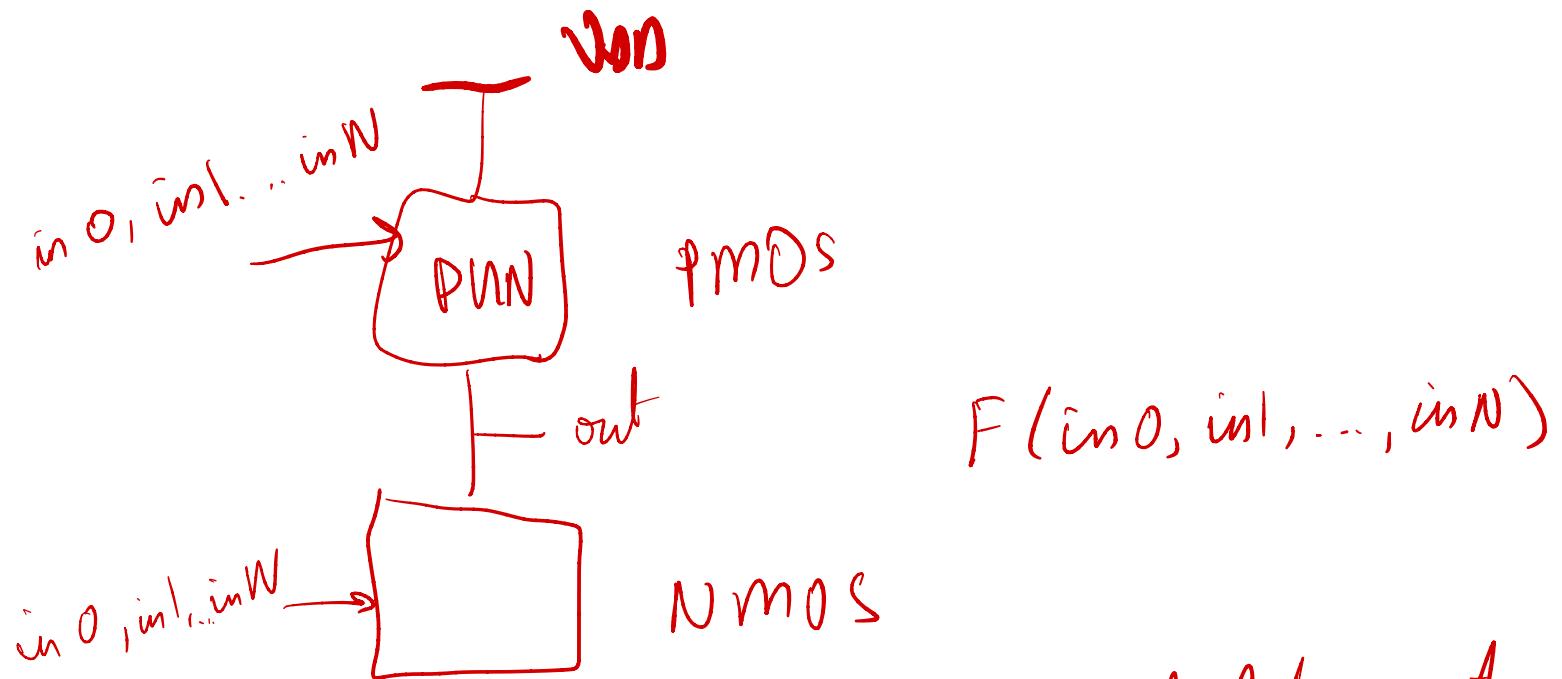
# Static gates

Static if :

- at every point in time (except switching) out is connected to either VDD or GND
- but not both!



# Static complementary CMOS



dual logic networks  
complementary -  
when PMW activated  
PDN is off

# NAND gate

$$\text{out} = \overline{A \cdot B}$$

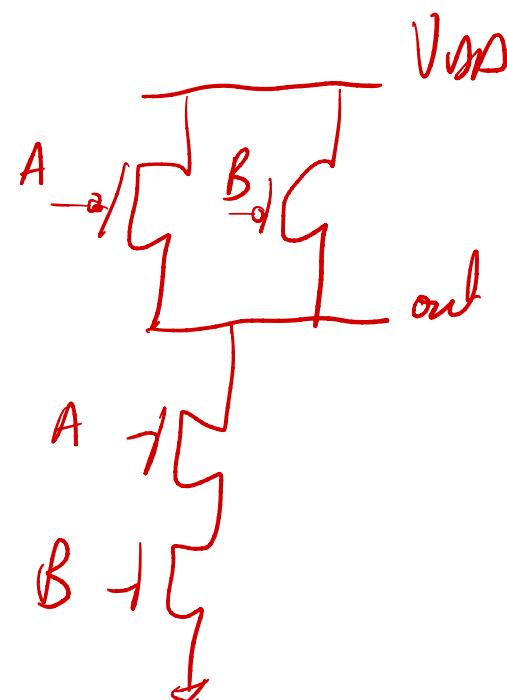
PDN:  $\text{out} = 0$  when  $A \cdot B$  is true

$\downarrow$   
series

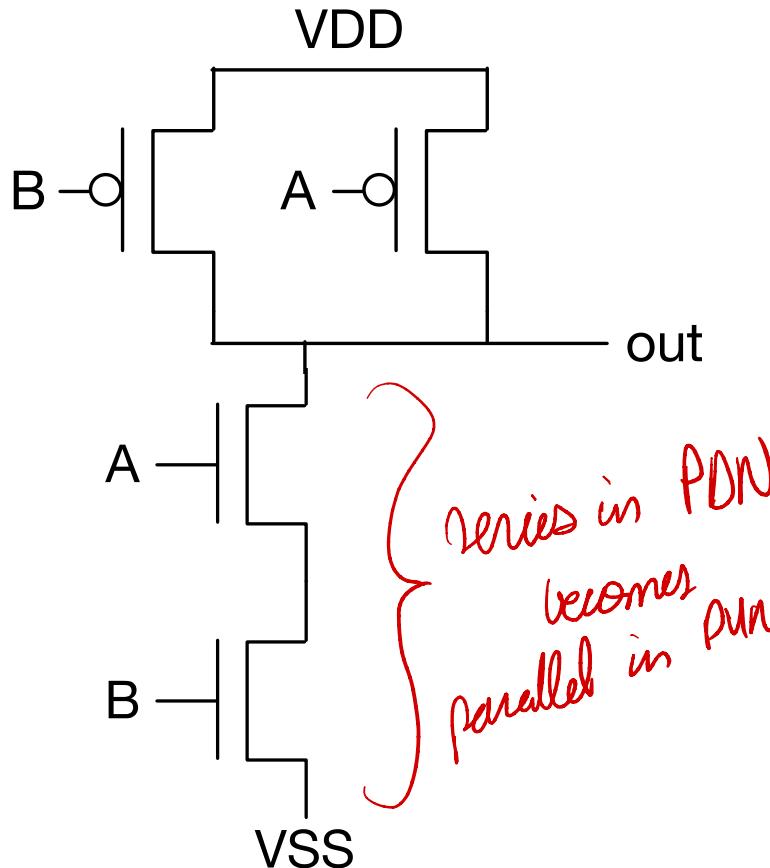
PUN:  $\text{out} = 1 = \overline{A \cdot B} = \bar{A} + \bar{B}$

PMOS conducts when output low  
 $\Rightarrow$  take complement

$$A + B$$



# NAND gate



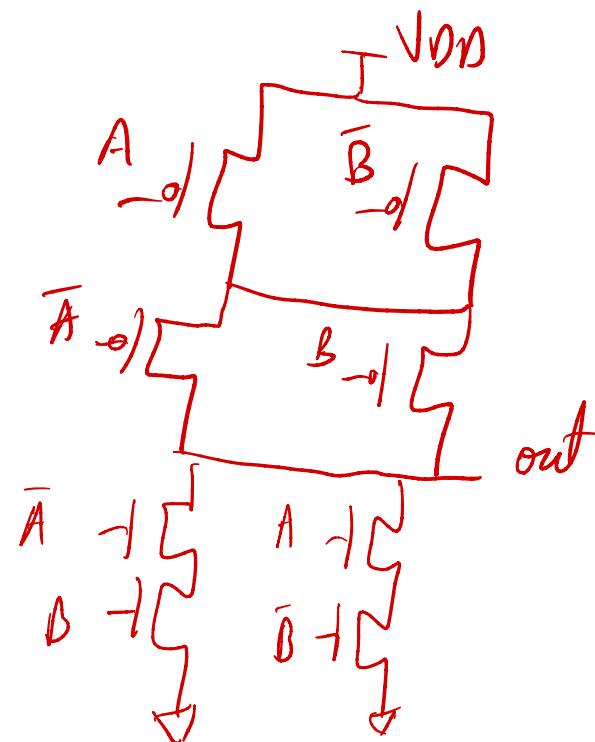
- Notice that the PUN and PDN are “opposite”
  - Meaning serial vs. parallel
  - This concept known as “duality”
- Also notice that the gate was inverting
  - How do we make an AND? (next slides)
- Easiest way to make a gate is to define the PDN first
  - Make the PUN by flipping the branches of the PDN

# XNOR gate

$$\text{out} = \overline{\bar{A}B + A\bar{B}}$$

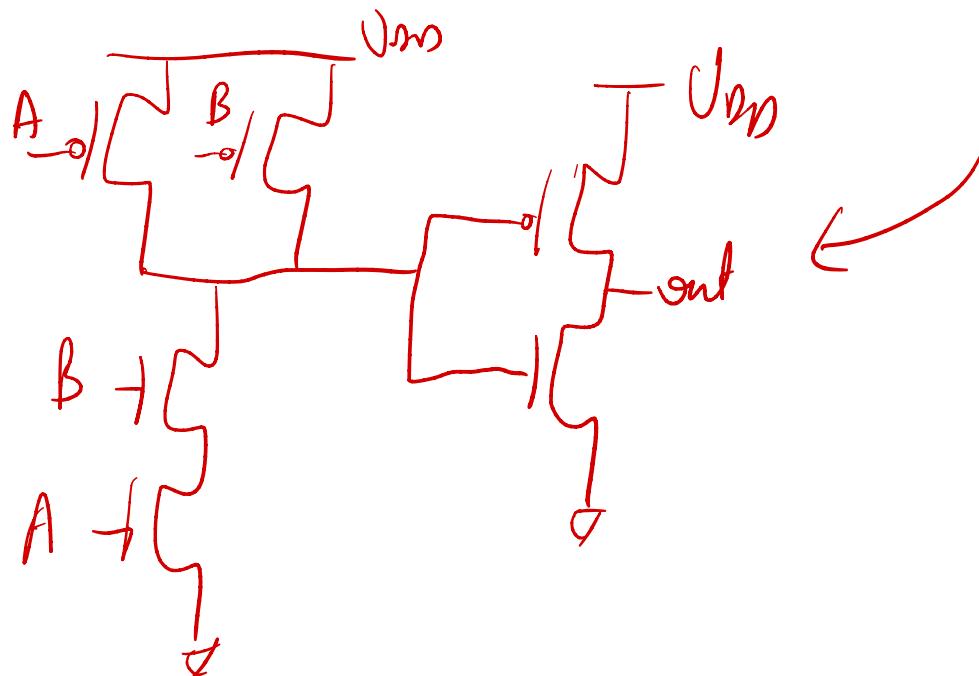
PDN:  $\text{out} = 0$  when  $\bar{A}B + A\bar{B}$

PUN: use duality



# AND gate

$$\text{AND 2} = AB = \overline{\overline{A}\overline{B}}$$



needs extra  
inversion!

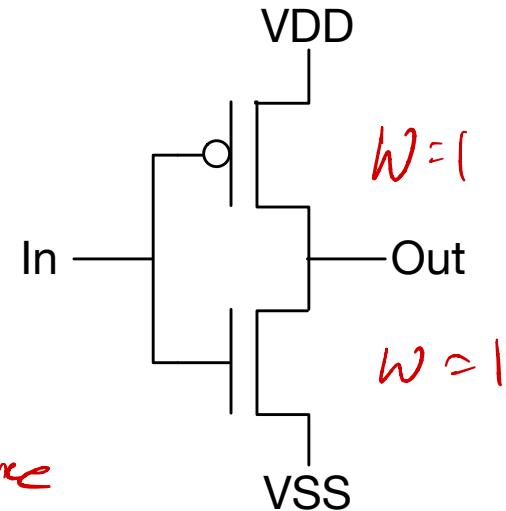
greater size  
and delay than NAND

# CMOS gate sizing

- Choosing the width of a transistor (typically use minimum length)
- Minimum sized inverter:

*Want equal pull up and pull down strength  
for modern technologies,  $R_{on,p} = R_{on,n}$   
for unit size*

$R \propto \frac{1}{w}$  so we need  $w_p \approx w_n$  for balance

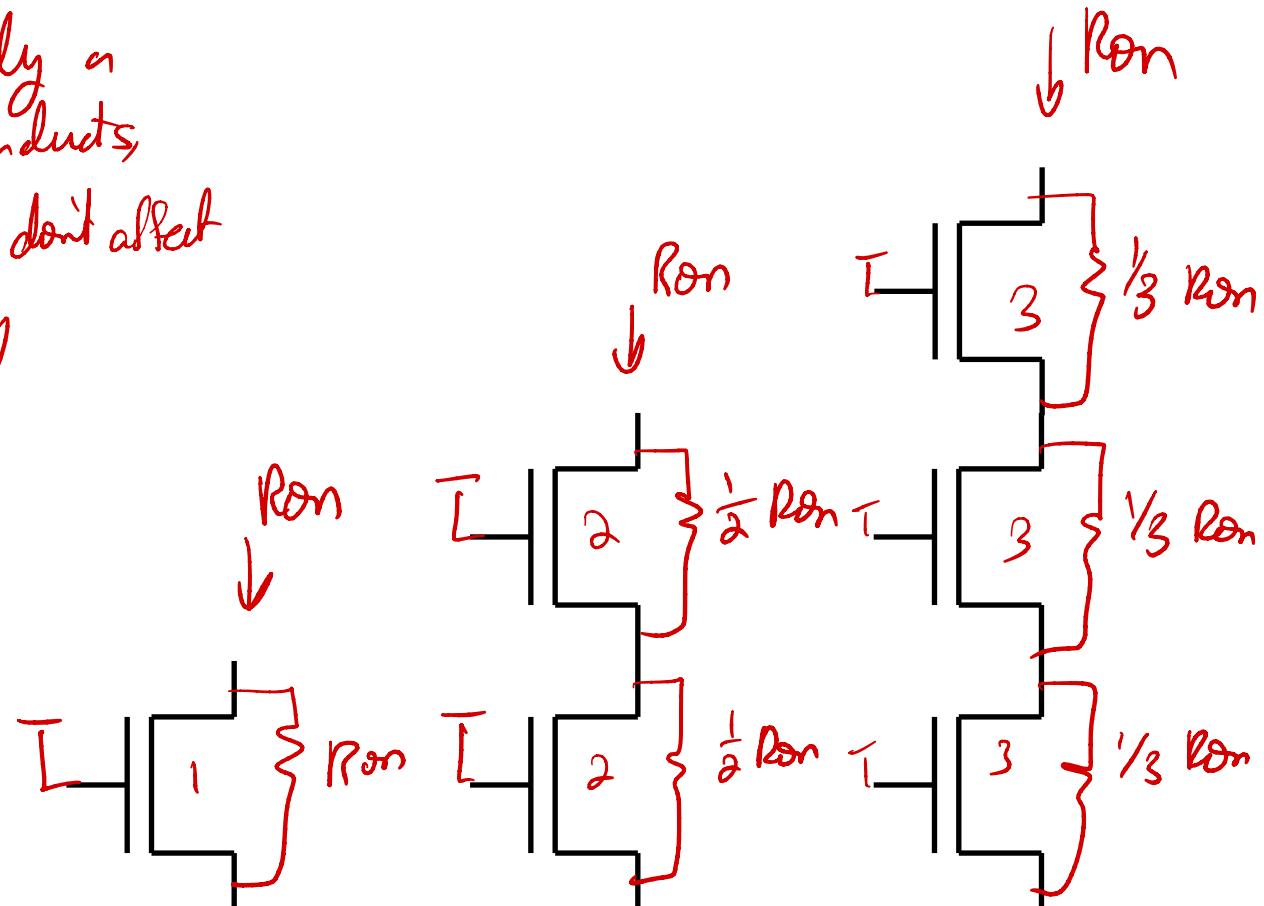


- Unless otherwise stated, complex gates should:
  - Have equal pull-up and pull-down resistances
  - Pull-up and pull-down resistances equivalent to minimum sized inverter *must be true in the worst case!*

# Transistor stacks – R vs. W

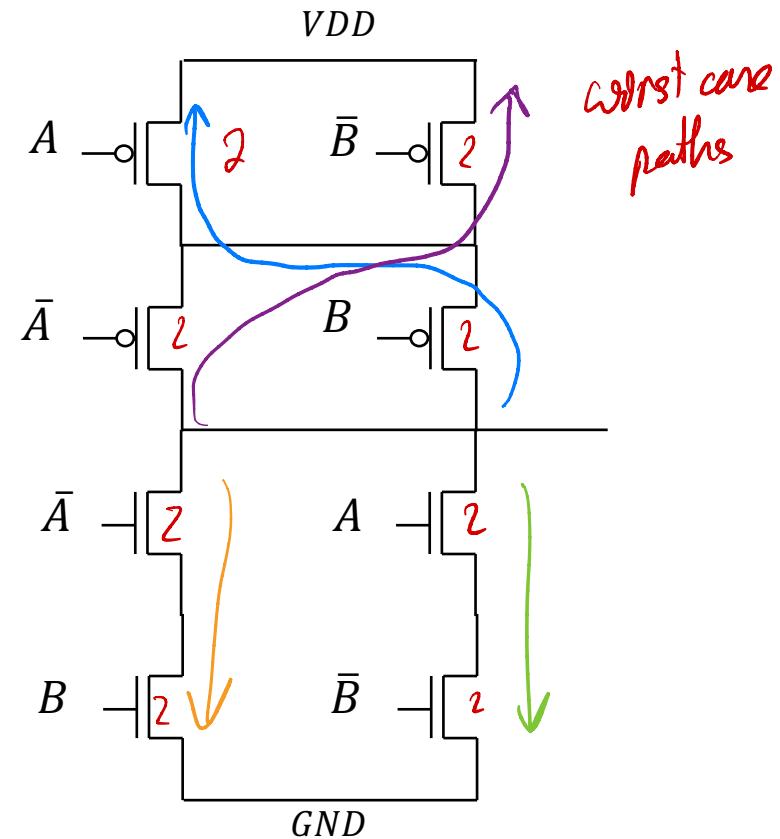
Note:

in worst case, only a single stack conducts  
parallel branches don't affect  
worst case sizing



# Gate sizing example – XNOR

min inverter :

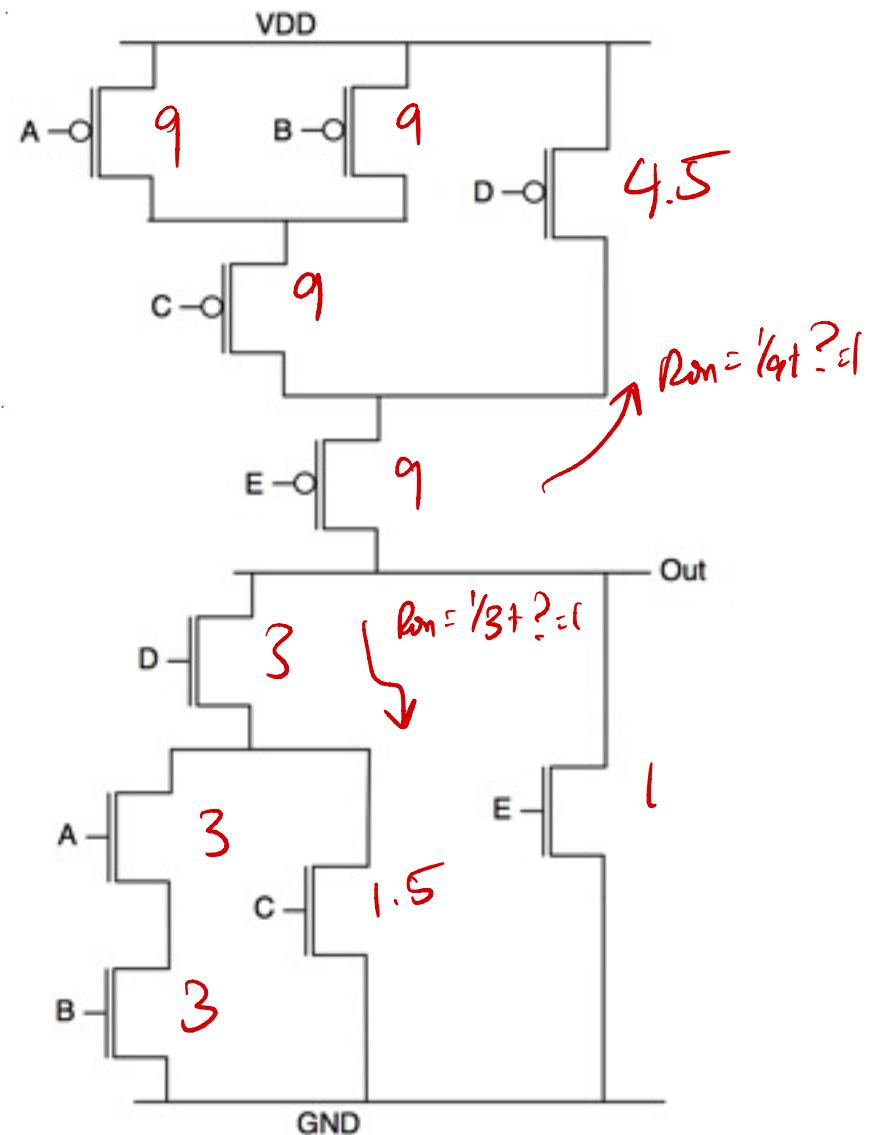


# Gate sizing example

$$R_{on,p} = 3 * R_{on,n}$$

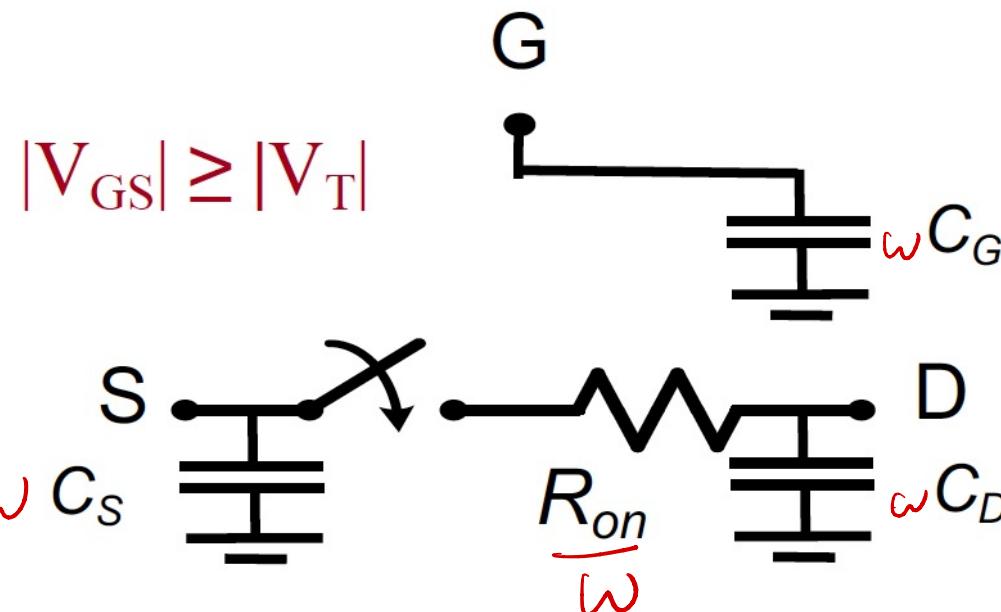
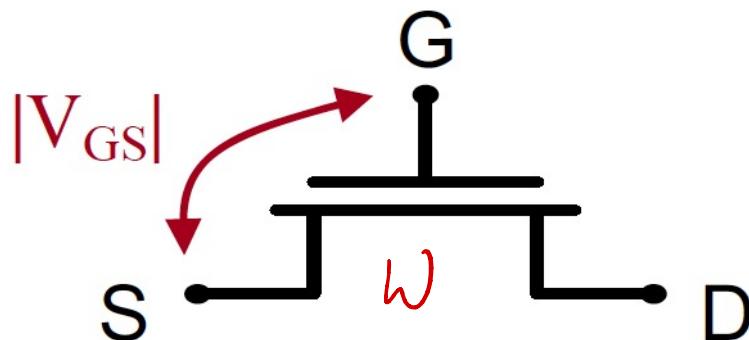
contrived, not true for modern technologies

min inverter:

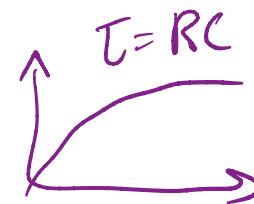
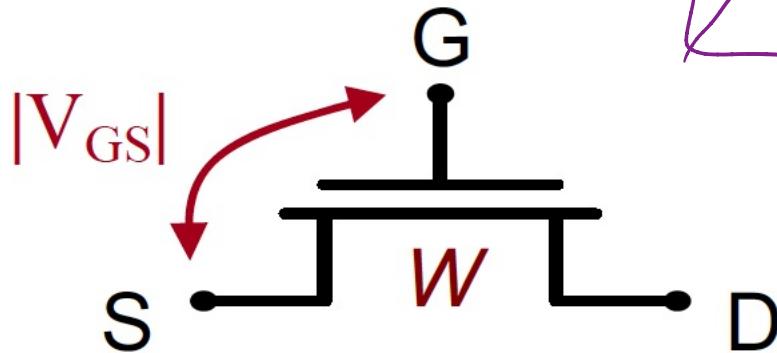


# Inverter delay

# Simple dynamic model



# Simple dynamic model



$$V_{out} = (1 - e^{-t/RC}) V_{in}$$

$$0.5 V_{in} = (1 - e^{-t/RC}) V_{in}$$

$$0.5 = 1 - e^{-t/RC}$$

$$e^{-t/RC} = 0.5$$

$$-t/RC = \ln(0.5)$$

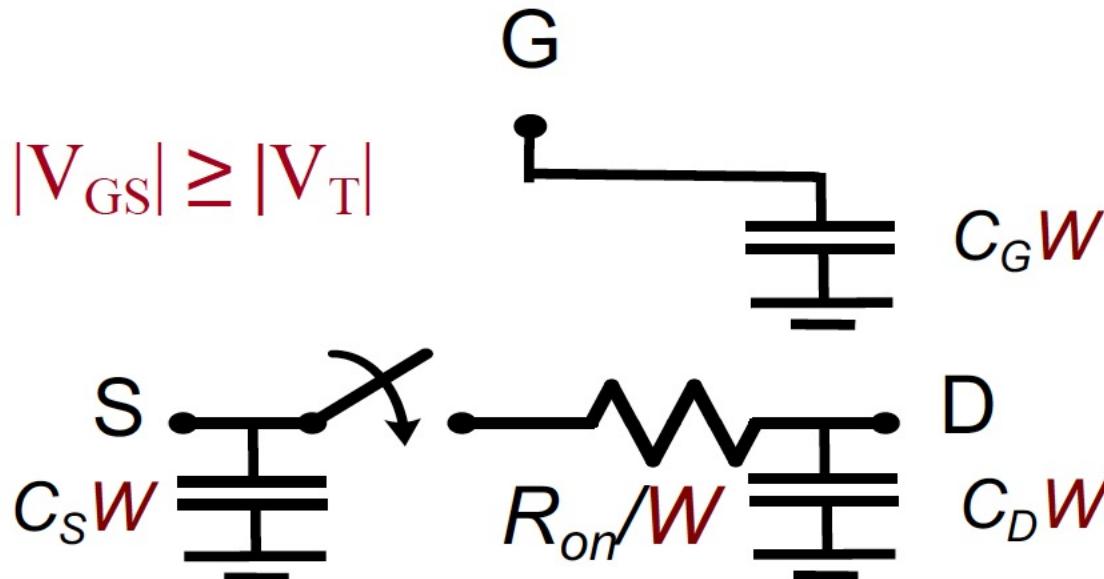
$$t = -\ln(0.5) \cdot RC$$

$$t = \ln(0.5^{-1}) \cdot RC$$

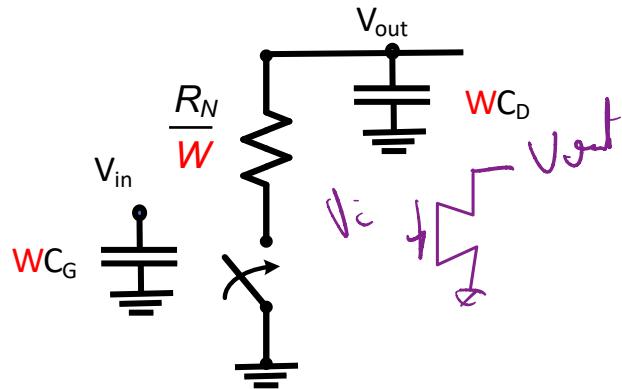
$$t = \ln(2) \cdot RC$$

$$= 0.69 \cdot RC$$

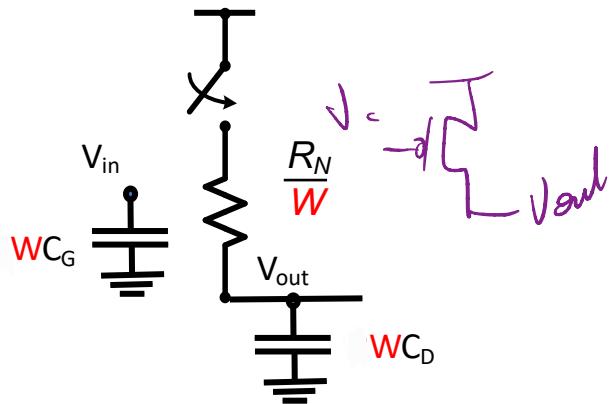
for 50%,  
coefficient is  $\ln(2)$



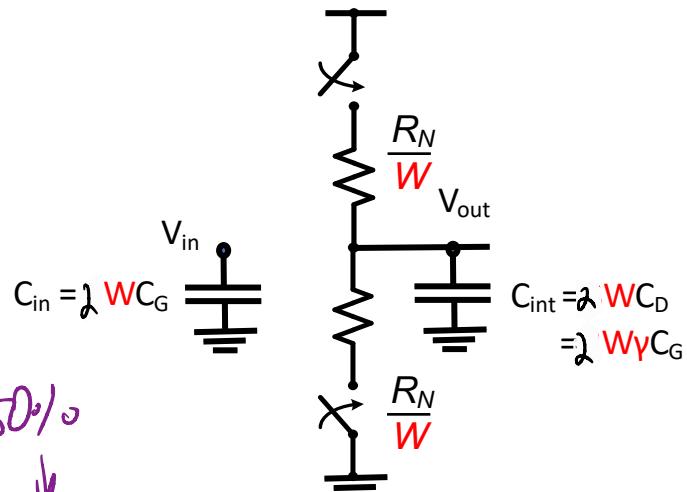
# Inverter delay



NMOS with size W



PMOS with same R as NMOS



for 50%

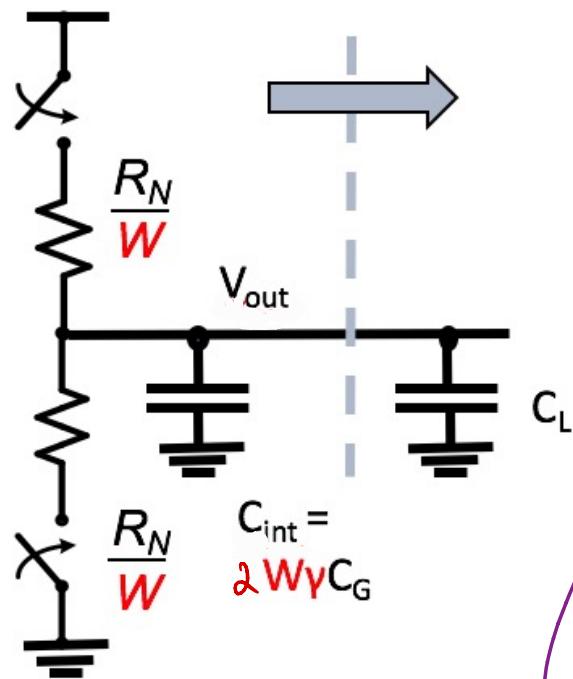
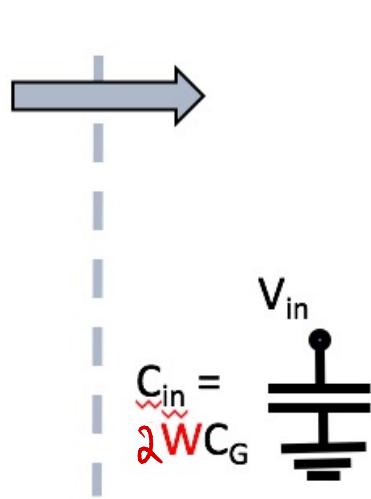
$$\tau_p = \ln(2) \frac{R_N}{\cancel{C_G}} 2 \cancel{W} \gamma C_G$$

$$= \ln(2) 2 \gamma R_N C_G$$

$$= \underbrace{\ln(2) 2 R_N C_G}_{t_{inv}} \gamma$$

*t<sub>inv</sub>*

# Inverter fanout



$$\begin{aligned}
 t_p &= \ln(2) \frac{R_N}{\lambda} (C_{in} + C_{int}) \\
 &= \ln(2) \frac{R_N}{\lambda} (2Wy C_G + C_L) \\
 &= \ln(2) 2 R_N C_G (\gamma + \frac{C_L}{C_G}) \\
 &= t_{inv} (\gamma + \frac{C_L}{C_{in}}) \\
 &\quad \text{↳ fanout}
 \end{aligned}$$

$$t_p = t_{inv} (\gamma + f)$$