

EECS151 : Introduction to Digital Design and ICs

Lecture 27 – Chips, Summary

Bora Nikolić



Lotfi Zadeh

Lotfi Aliasker Zadeh (February 1921 – 6 September 2017)^{[1][2]} was a mathematician, computer scientist, electrical engineer, artificial intelligence researcher, and professor^[7] of computer science at the University of California, Berkeley. Zadeh is best known for proposing fuzzy mathematics, consisting of several fuzzy-related concepts: fuzzy sets,^[8] fuzzy logic,^[9] fuzzy algorithms,^[10] fuzzy semantics,^[11] fuzzy languages,^[12] fuzzy control,^[13] fuzzy systems,^[14] fuzzy probabilities,^[15] fuzzy events,^[15] and fuzzy information.^[16] Zadeh was a founding member of the Eurasian Academy.^[17]

Wikipedia

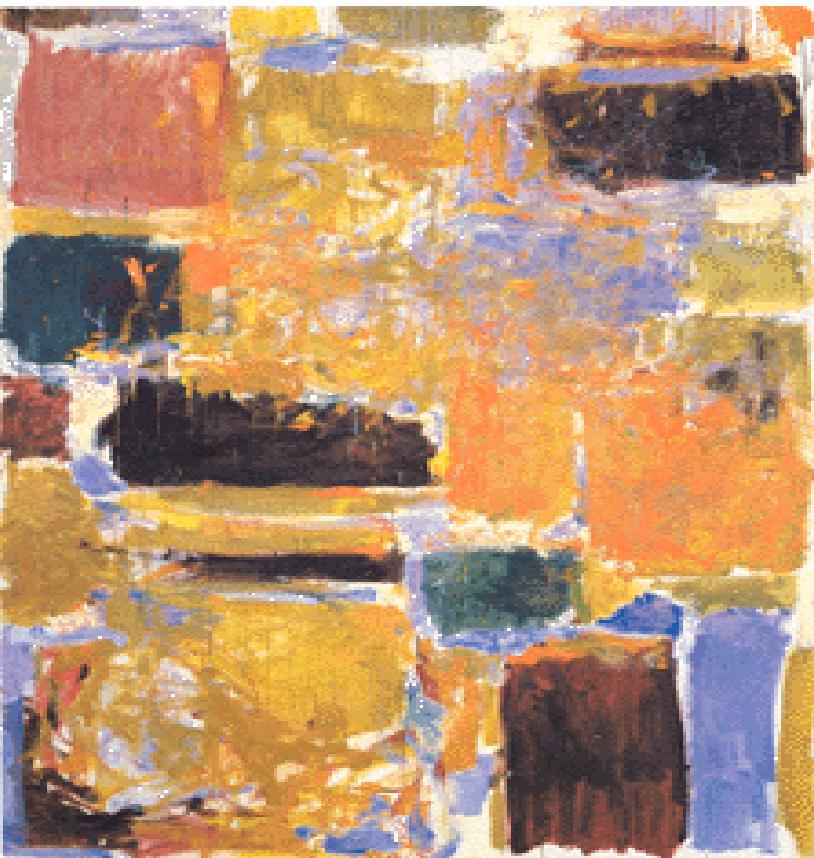
EECS151/251A L27 SUMMARY



Nikolić Fall 2021

Review

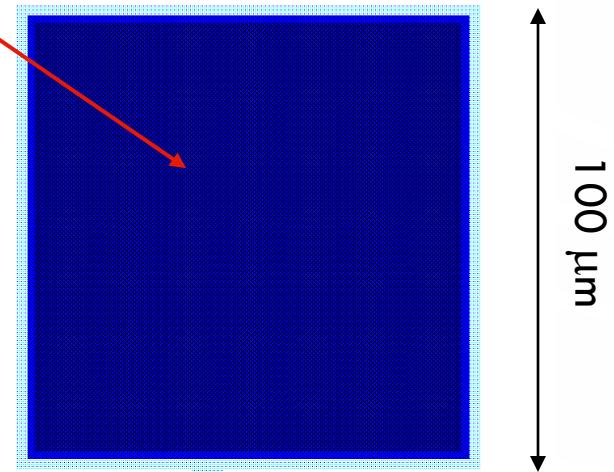
- Flash
 - Single-level vs multi-level
 - Read and Write Flash Cell
 - NAND vs NOR
- NVRAM
- CAM
- Parallelism for higher performance and lower power



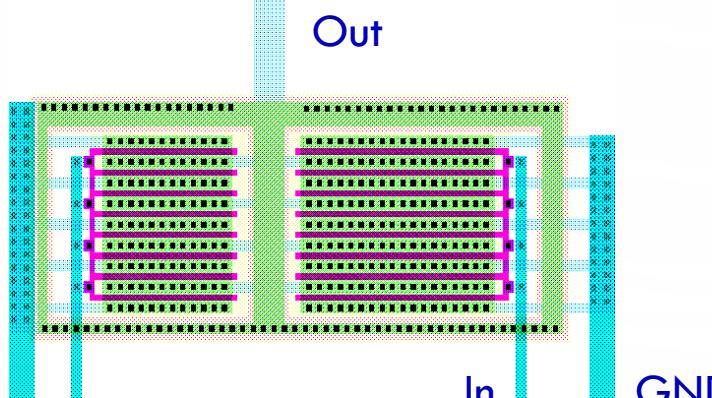
Chip Packaging, I/O

Bonding Pad Design

Bonding Pad



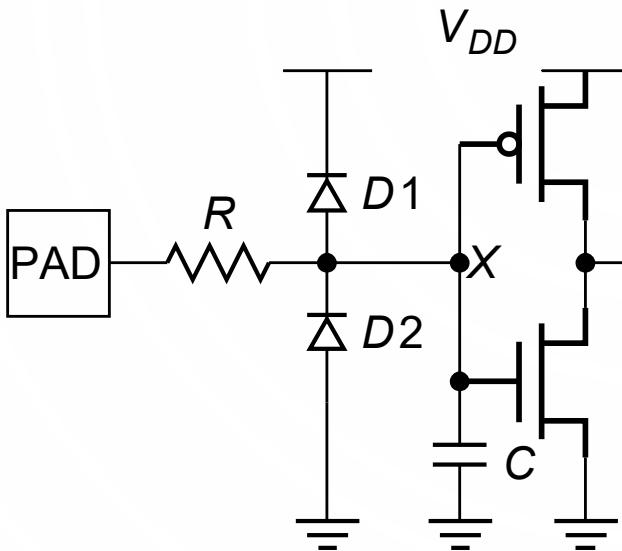
100 μm



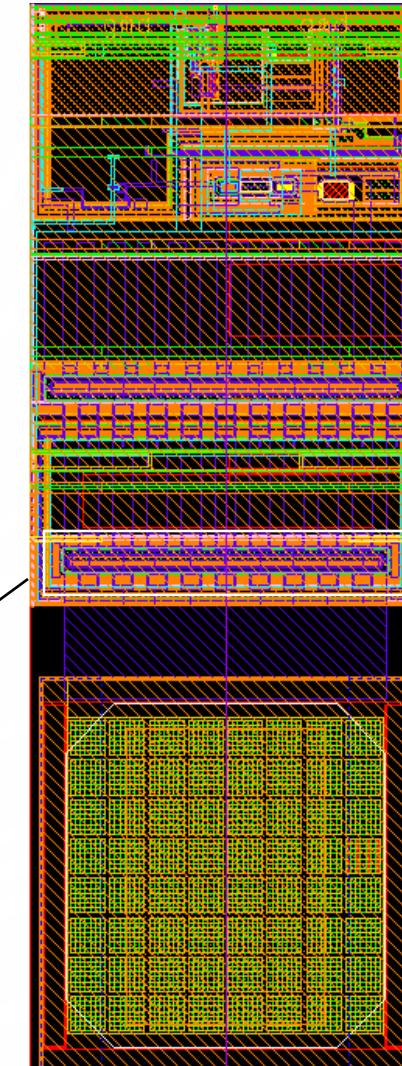
ESD Protection

- When a chip is being connected to a board, there is unknown (potentially large) static voltage difference
- Equalizing potentials requires (large) charge flow through the pads
- Diodes sink this charge into the substrate – need guard rings to pick it up.

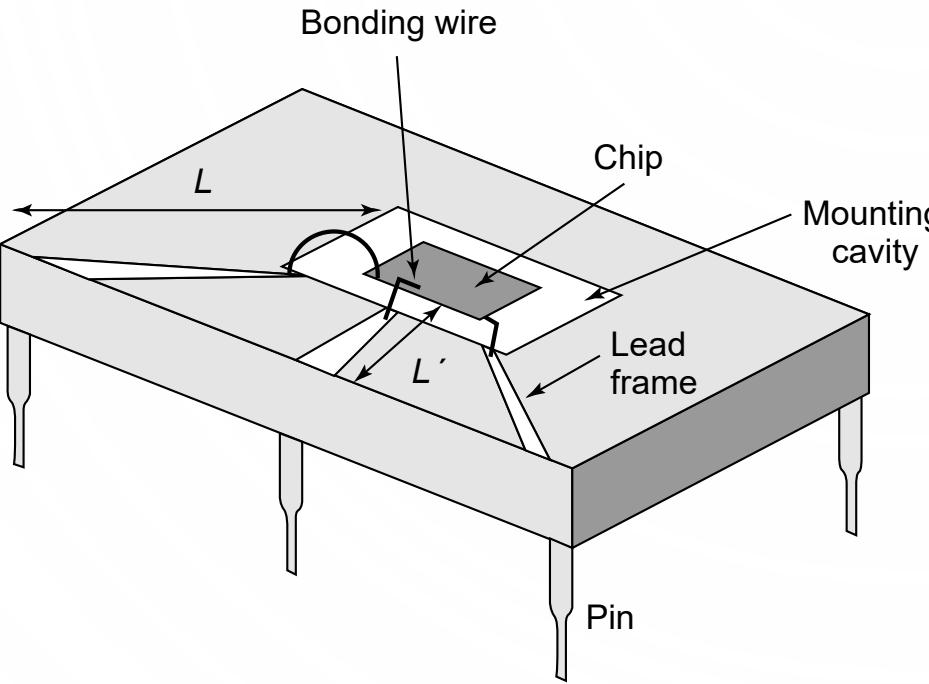
ESD Protection



Diode



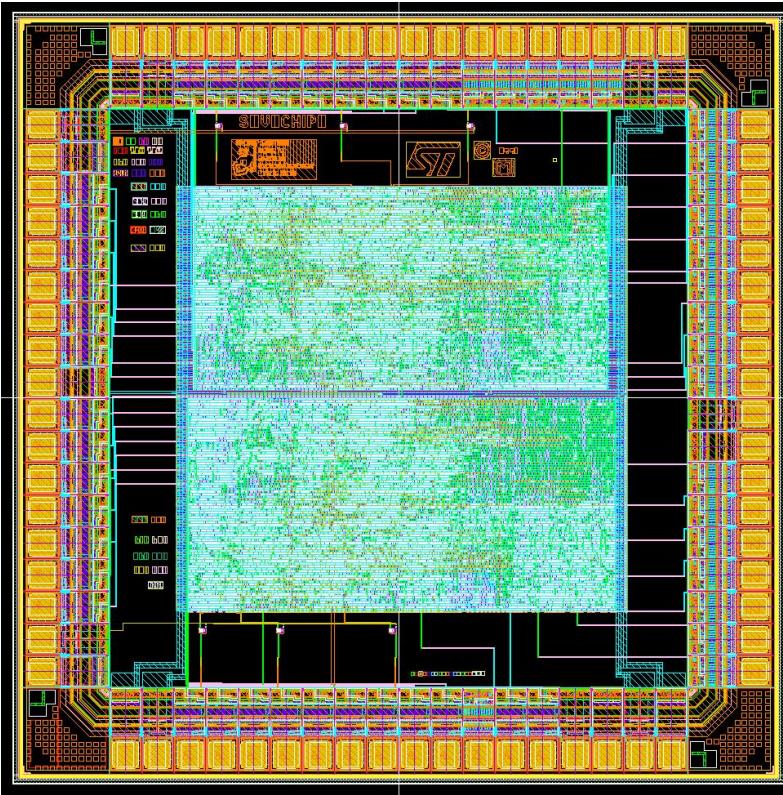
Chip Packaging



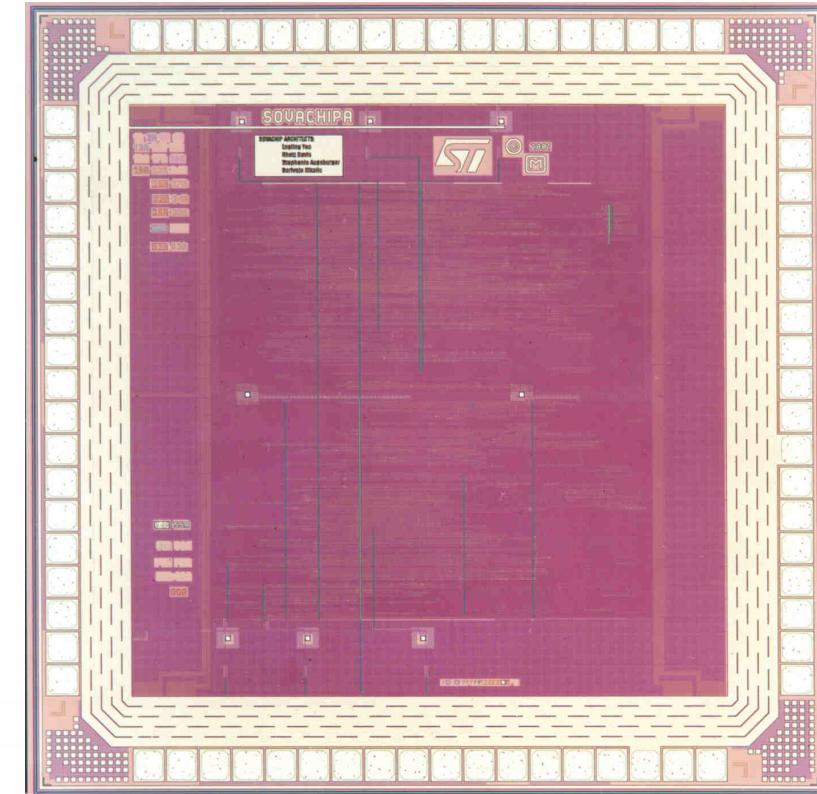
- Bond wires ($\sim 20\mu\text{m}$) are used to connect the package to the chip
- Pads are arranged in a frame around the chip
- Pads are relatively large
 $\sim 20\text{-}100\mu\text{m}$ ($40\text{-}200\mu\text{m}$ pitch)
- Many chips areas are 'pad limited'

Pad Frame

Layout

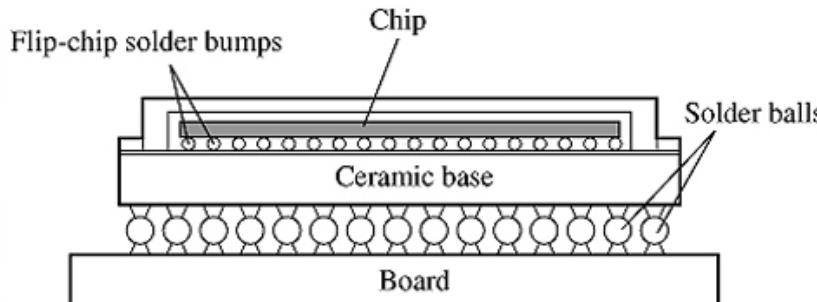


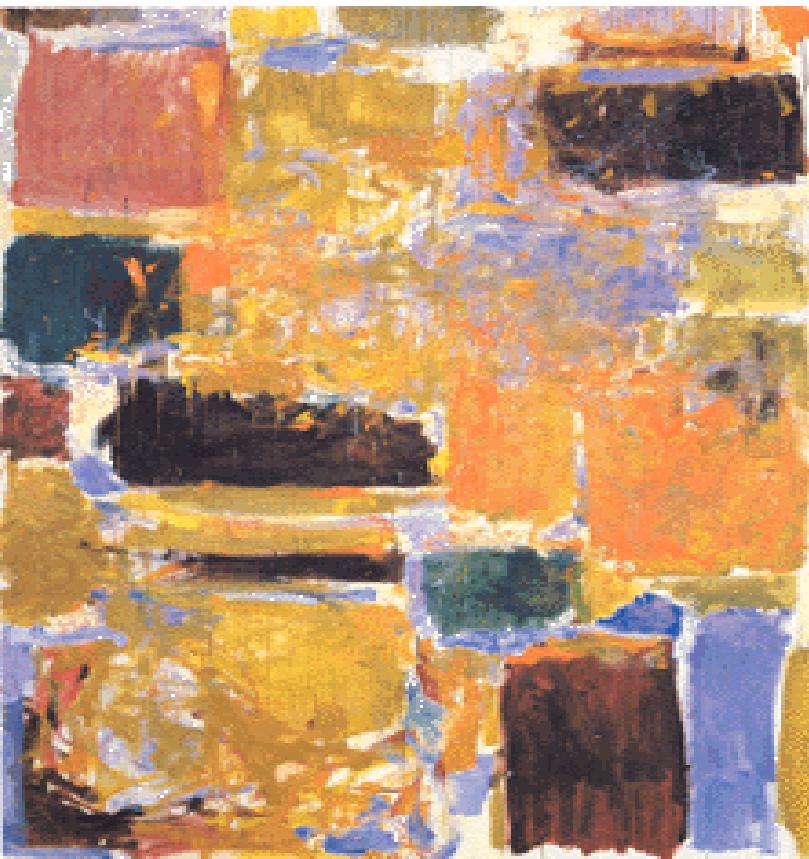
Die Photo



Chip Packaging

- Most modern chips are ‘flip-chip’ packaged
 - Pads are distributed around the chip
 - The soldering balls are placed on pads
 - The chip is ‘flipped’ onto the package
 - Can have many more pads





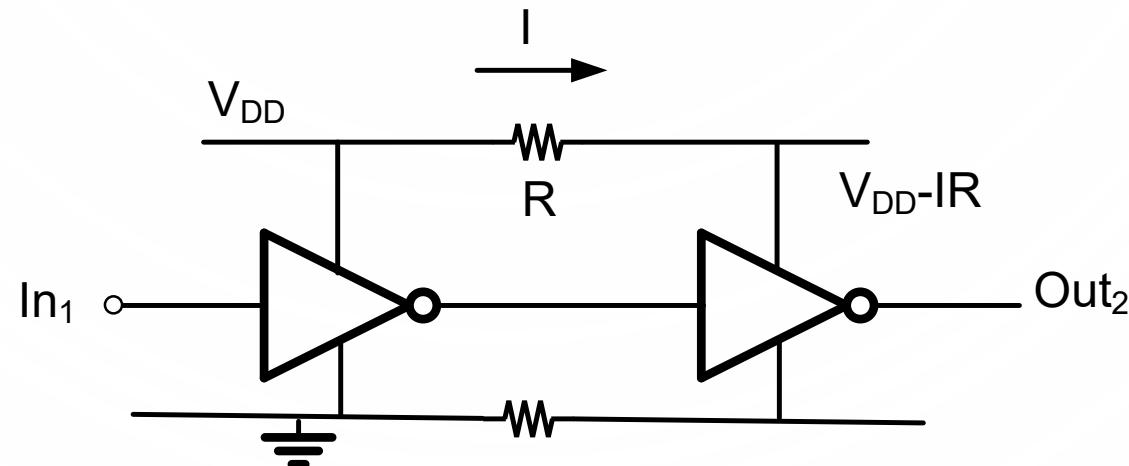
Supply Distribution

Impact of Resistance

- Impact of resistance is commonly seen in power supply distribution:
 - IR drop
 - Voltage variations
- Power supply is distributed to minimize the IR drop and compensate for the inductances

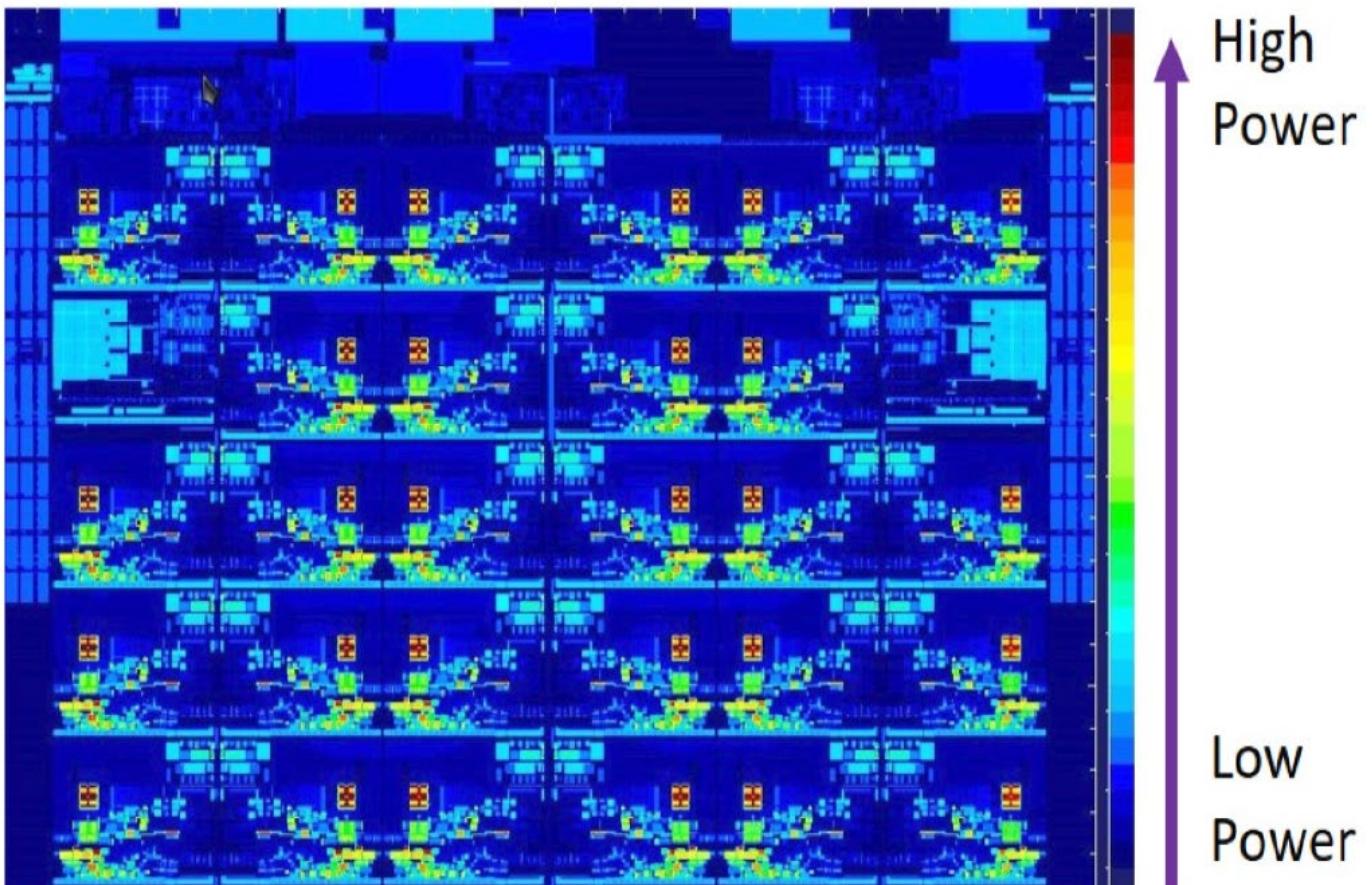
RI Introduced Voltage Drop and Noise

- Supply current:
 - Average
 - Time varying component, depends on activity



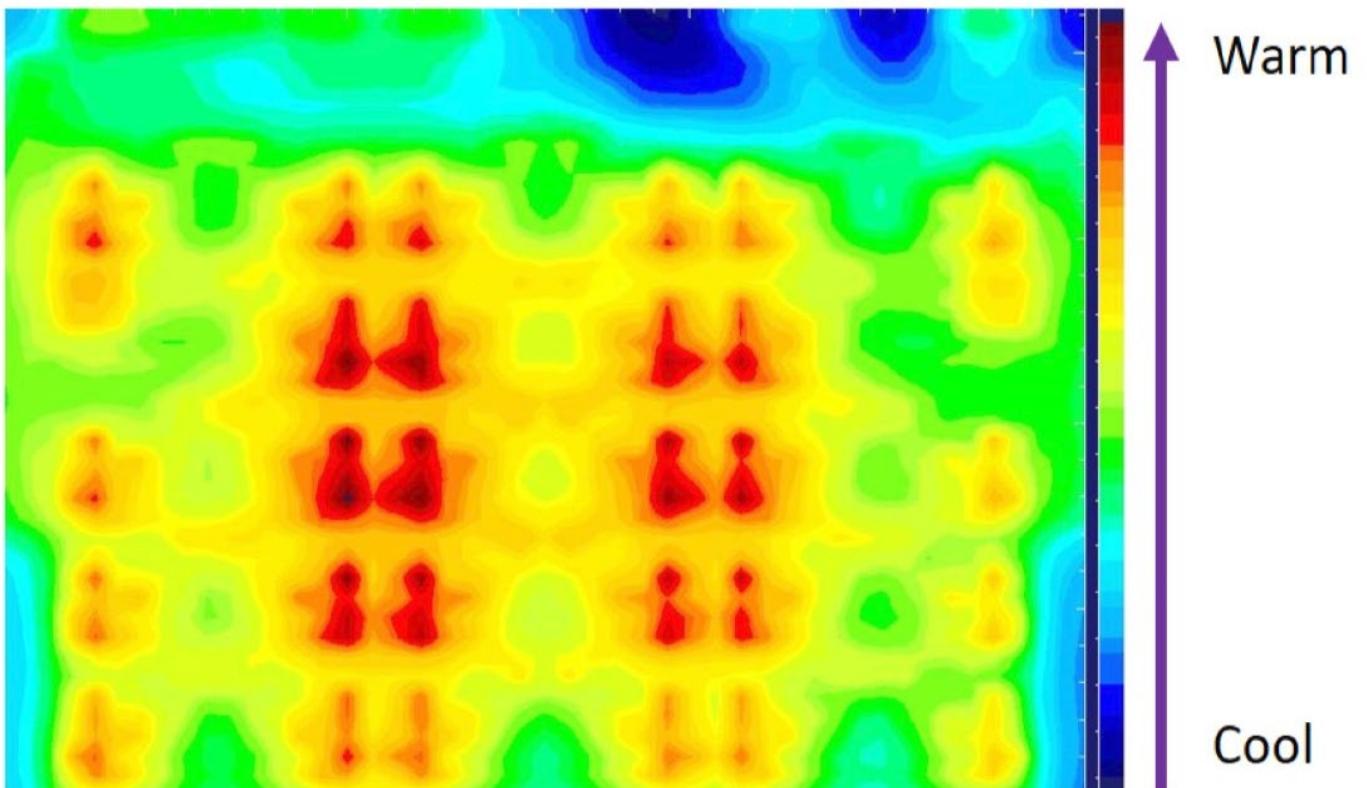
Resistance and the Power Distribution Problem

- Intel Skylake-SP power map
 - Power draw varies a lot across the die



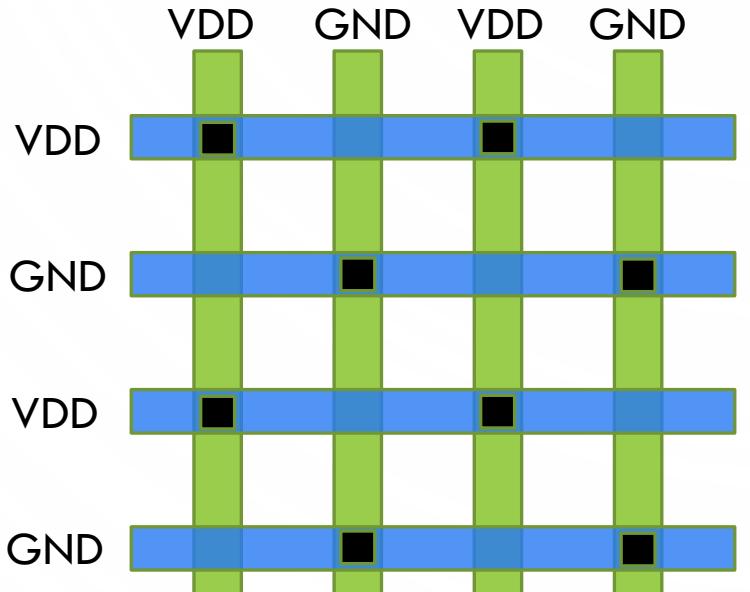
Power Converts to Heat

- Intel Skylake-SP thermal map
 - Temperature varies across the die
 - Leakage strongly depends on temperature



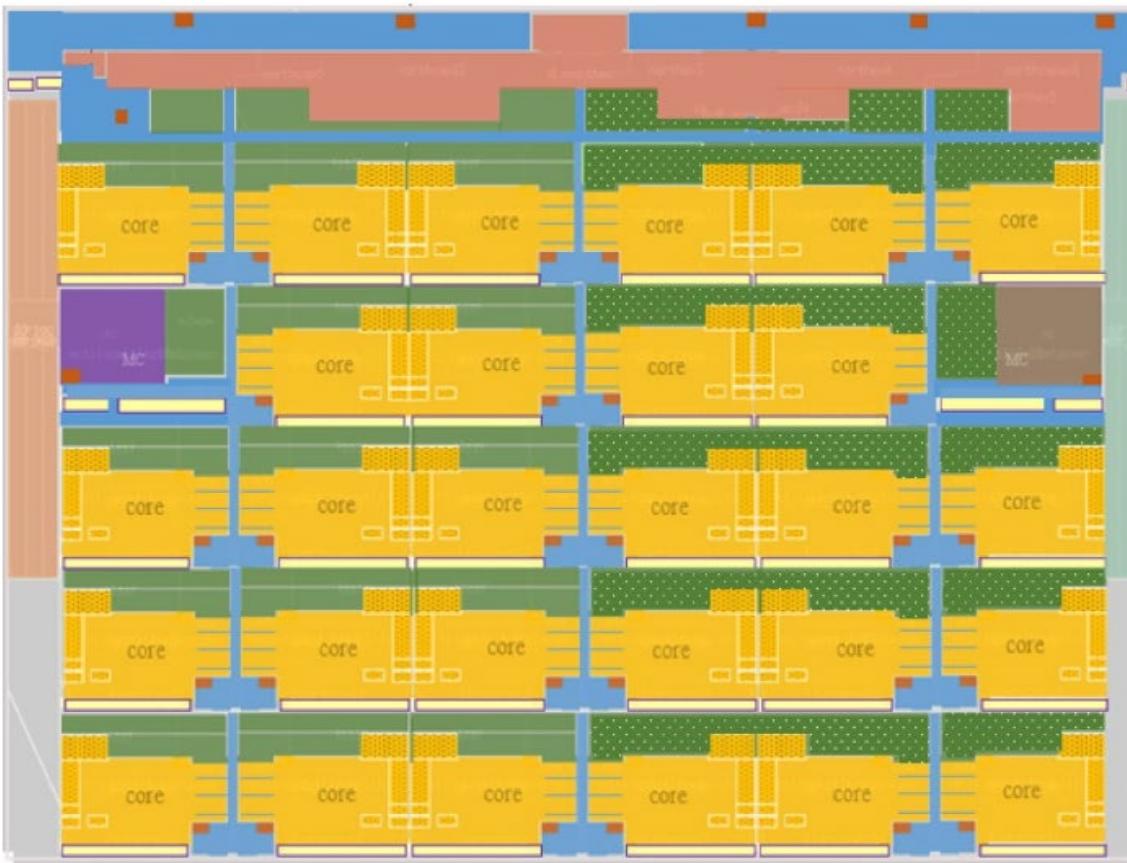
Power Distribution

- Low-level distribution is in Metal 1 / 2
- Power has to be ‘strapped’ in higher layers of metal.
- The spacing is set by IR drop, electromigration, inductive effects
- Always use multiple contacts on straps



Modern Example: Intel Skylake-SP

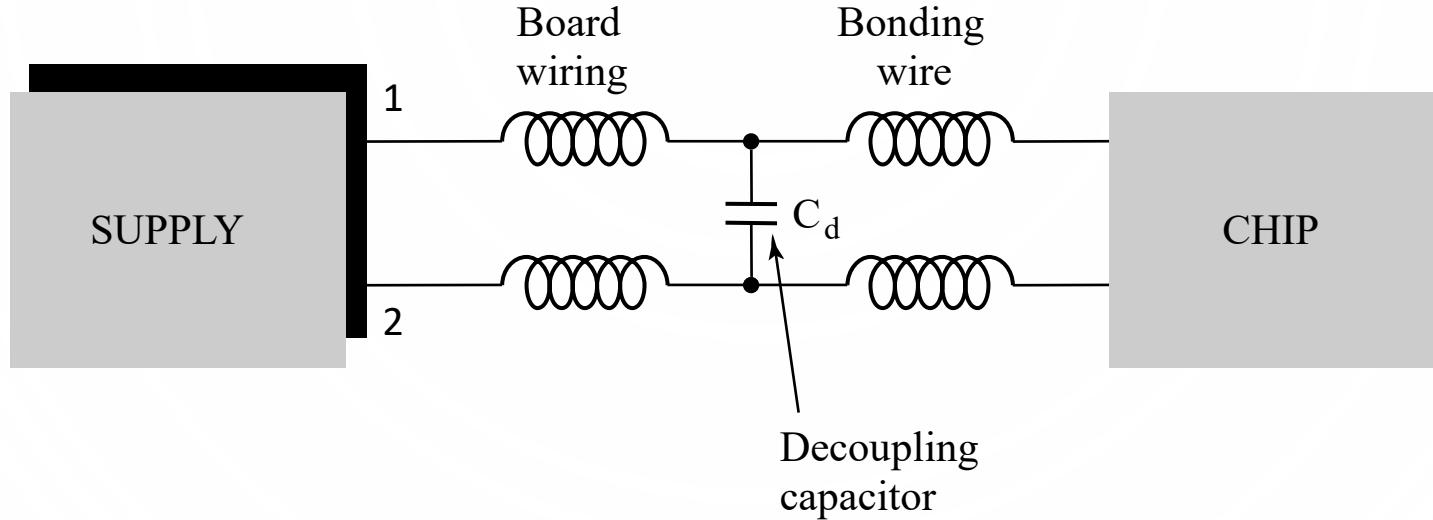
- Many power domains



- 9 primary VCC domains are partitioned into 35 VCC planes

- Vcc: core supply (per core)
- } Vccclm: Un-core supply
- Vccsa: System Agent supply
- Vccio: Infrastructure supply
- Vccsfr: PLL supply
- } Vccddrd: DDR logic supply
- } Vccddra: DDR I/O supply

Decoupling Capacitors



Decoupling capacitors are added:

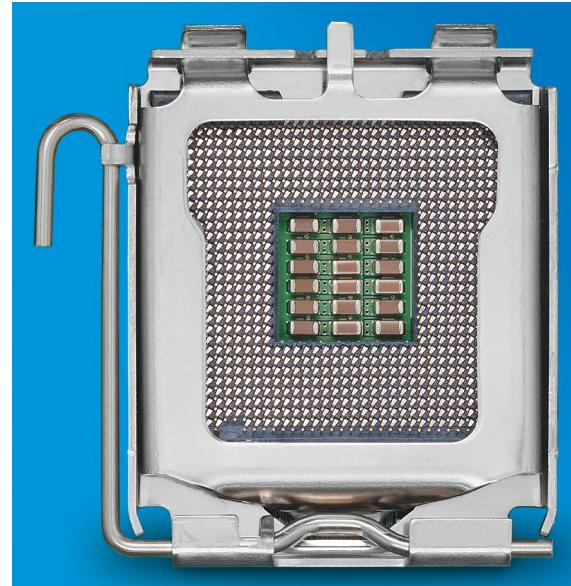
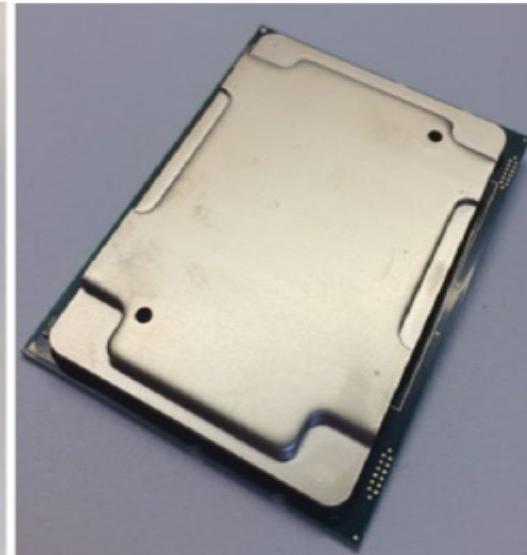
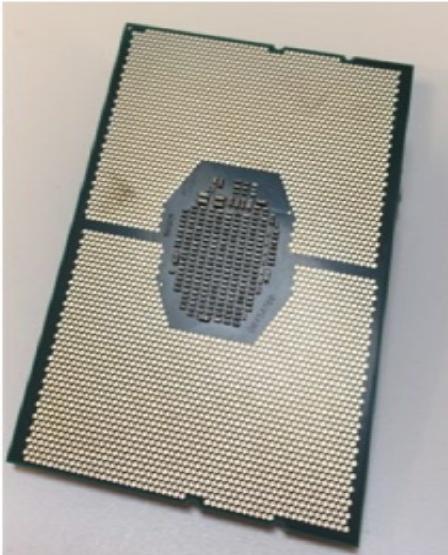
- On the board (right under the supply pins)
- On the chip (under the supply straps, near large buffers)

Decoupling Capacitors

- Under the die



- Intel Skylake-SP



- Intel Pentium 4 socket

Administrivia

- Special lecture on Monday, Dec 6. at 11:00am
 - FPGA prototyping
 - Not on final, but very useful
- Project, project, project !
 - Final checkoffs on Dec. 7
- Homework 11 due Dec 3.
- Final is on December 13, 11:30-2:30
 - Review session next Wednesday



This Class

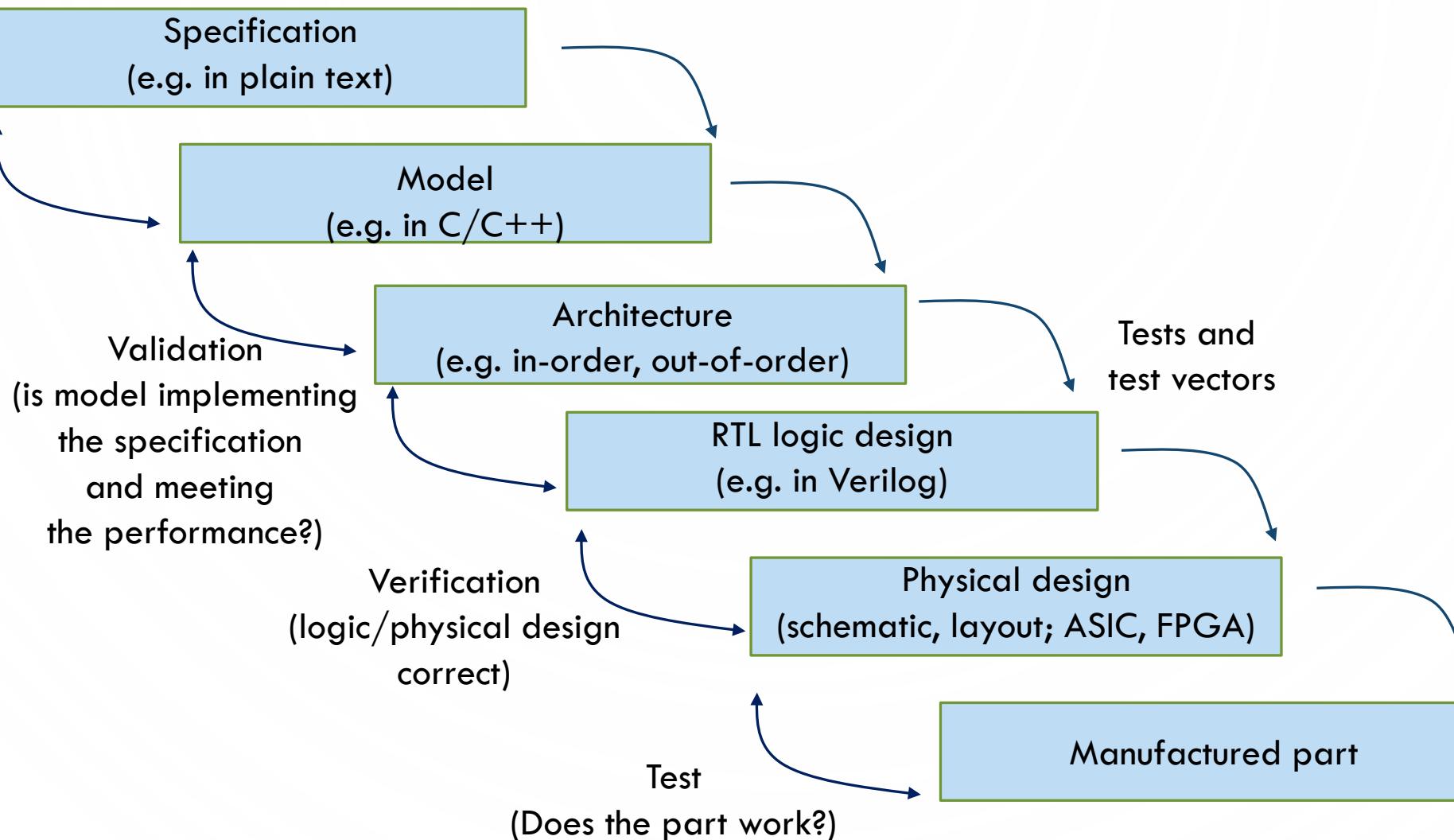
What This Class is All About?

- **Introduction to digital integrated circuit and system engineering**
 - Key concepts needed to be a good digital system designer
 - Discover your own creativity!
- **Learn models that allow reasoning about design behavior**
 - Manage design complexity through abstraction and understanding of tools
 - Allow analysis and optimization of the circuit's performance, power, cost, etc.
- **Learn how to make sure your circuit and system works**
 - *There are way more ways to mess up a chip than to get it right.*

Learn by doing!

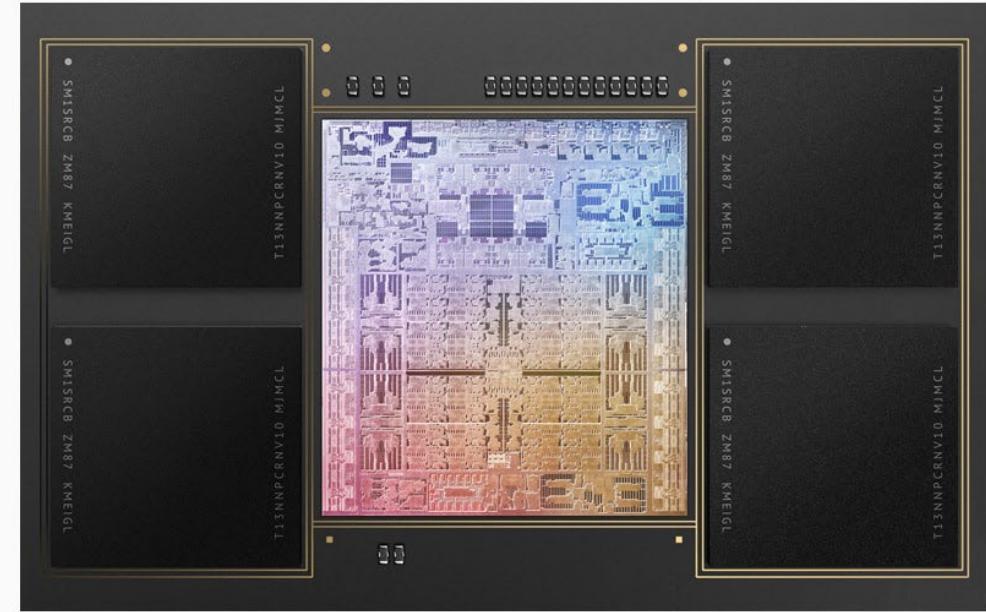
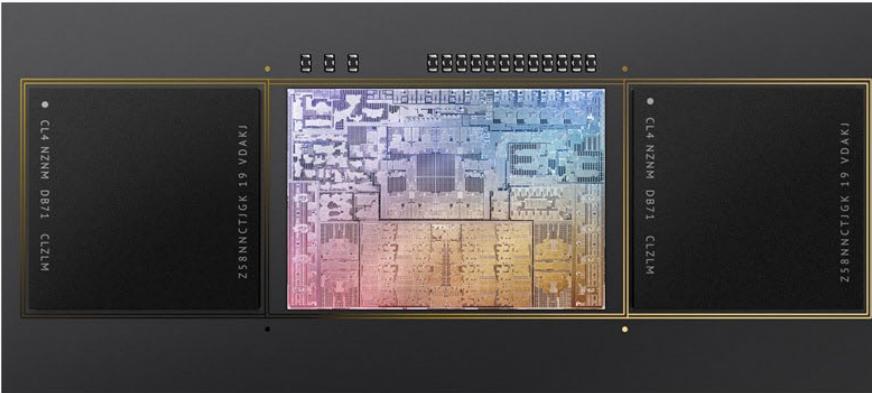
Design Process

- Design through layers of abstractions



Field Has Advanced

- Apple M1 Pro and M1 Max



<https://www.apple.com/newsroom/2021/10/introducing-m1-pro-l-chips-apple-has-ever-built/>

Field Has Advanced

- Intel's roadmap to 18A

Introducing Intel's new node naming

Node Name	Description	Previously Referred To As	Key Features
10nm SuperFin	In high-volume production	Previously referred to as Enhanced SuperFin	<ul style="list-style-type: none">10-15% perf/watt gainFinFET transistor optimizationsNow in volume production
Intel 7		Previously referred to as 7nm	<ul style="list-style-type: none">20% perf/watt gainFull use of EUV lithographyMeteor Lake for client tape in Q2 2021Granite Rapids compute tile for data center
Intel 4			<ul style="list-style-type: none">18% perf/watt gainDenser HP libraryIncreased intrinsic drive currentReduced via resistanceIncreased EUV useManufacturing products 2H 2023
Intel 3			
Intel 20A		The angstrom era of semiconductors	<ul style="list-style-type: none">Breakthrough innovations in 1H 2024RibbonFET – new transistor architecturePowerVia – interconnect innovation

intel accelerated



To Probe Further

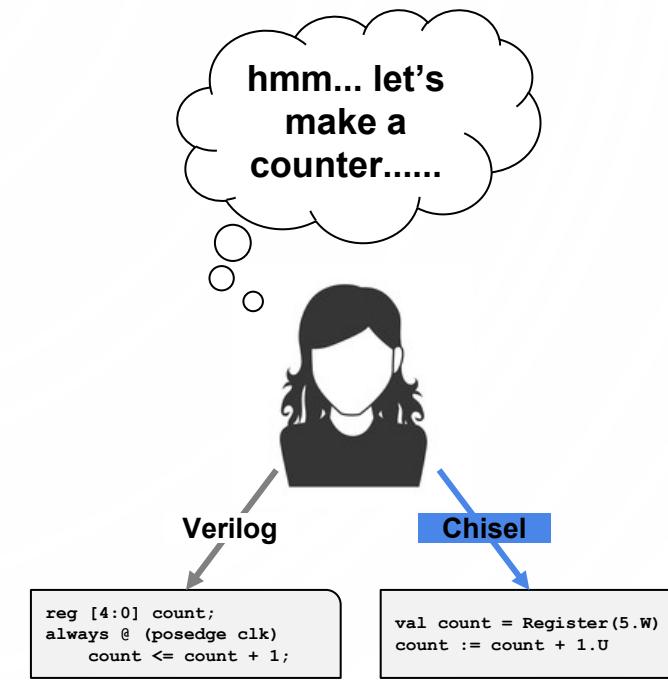
CS152/252 – Computer Architecture and Engineering

- Some have taken before EECS151
 - Taught only in Spring
- (More) advanced topics in computer architecture: Superscalar, out-of-order machines, vectors, GPUs, multithreading, memory hierarchy

Digital Systems/Computer Architecture Research

- Exploring new areas by using high productivity design

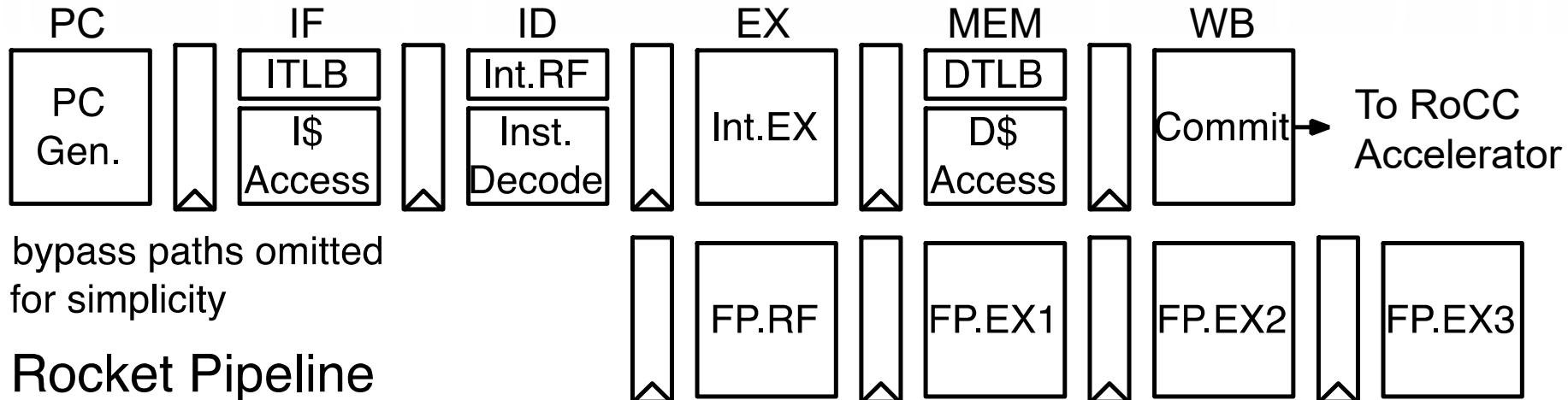
- Language: Chisel
- Same control over RTL as Verilog
- Higher software abstraction level
 - Powerful parameterization, functional and object-oriented programming, static typing
 - Huge base of existing software libraries



<https://www.chisel-lang.org/>

RISC-V Rocket and BOOM

- **Rocket core**

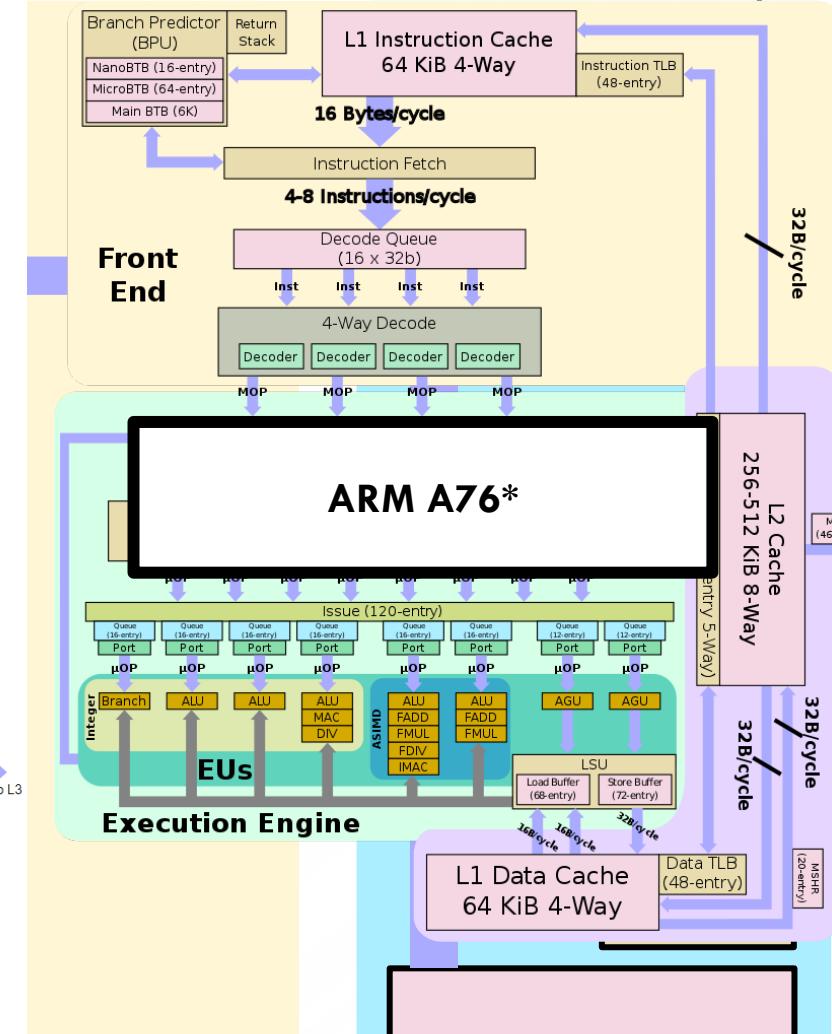
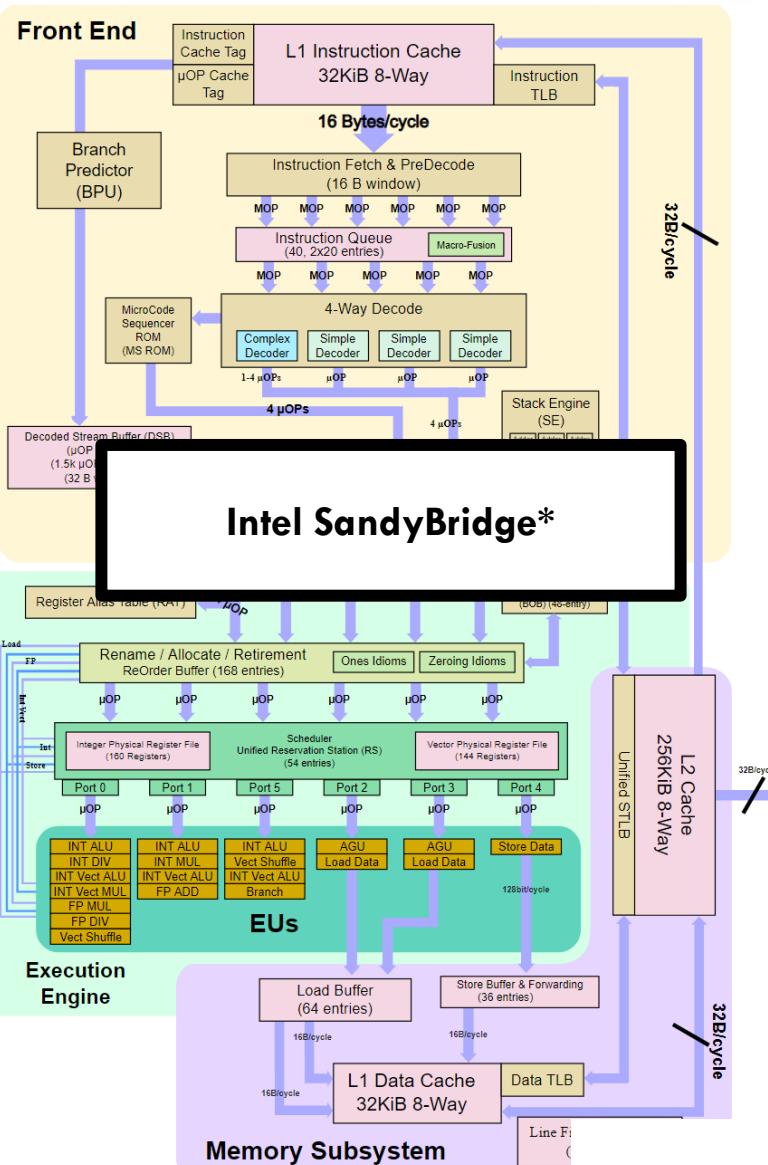
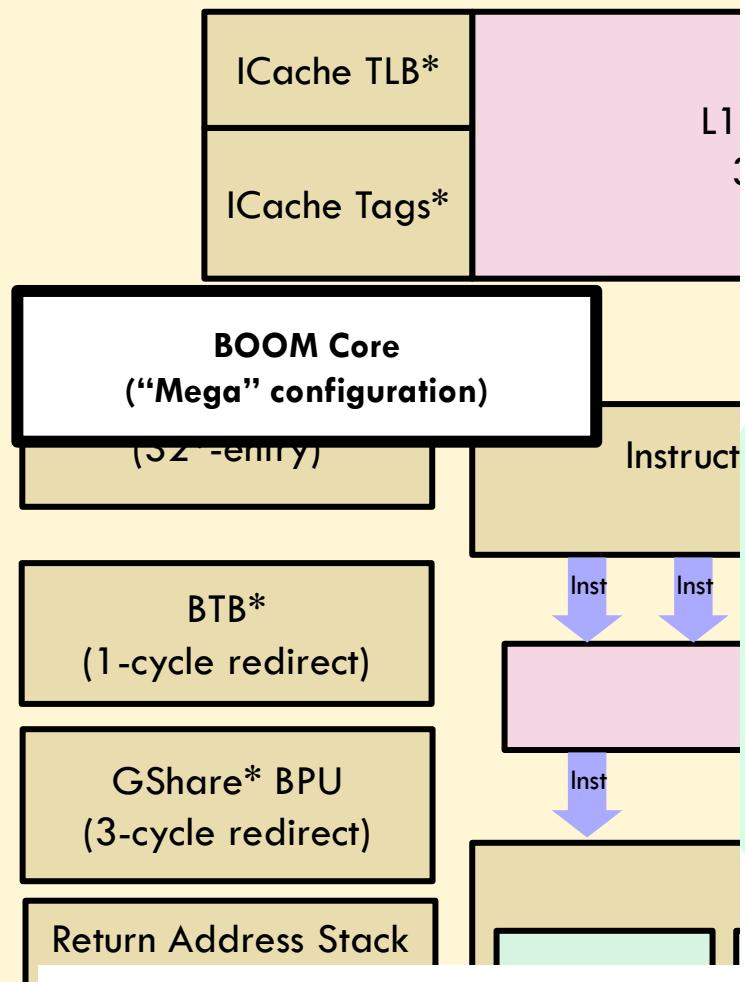


- 64-bit 5-stage single-issue in-order pipeline
- Design minimizes impact of long clock-to-output delays of compiler-generated RAMs
- 64-entry BTB, 256-entry BHT, 2-entry RAS (parameterized)
- MMU supports page-based virtual memory
- IEEE 754-2008-compliant FPU
 - Supports SP, DP FMA with hw support for subnormals

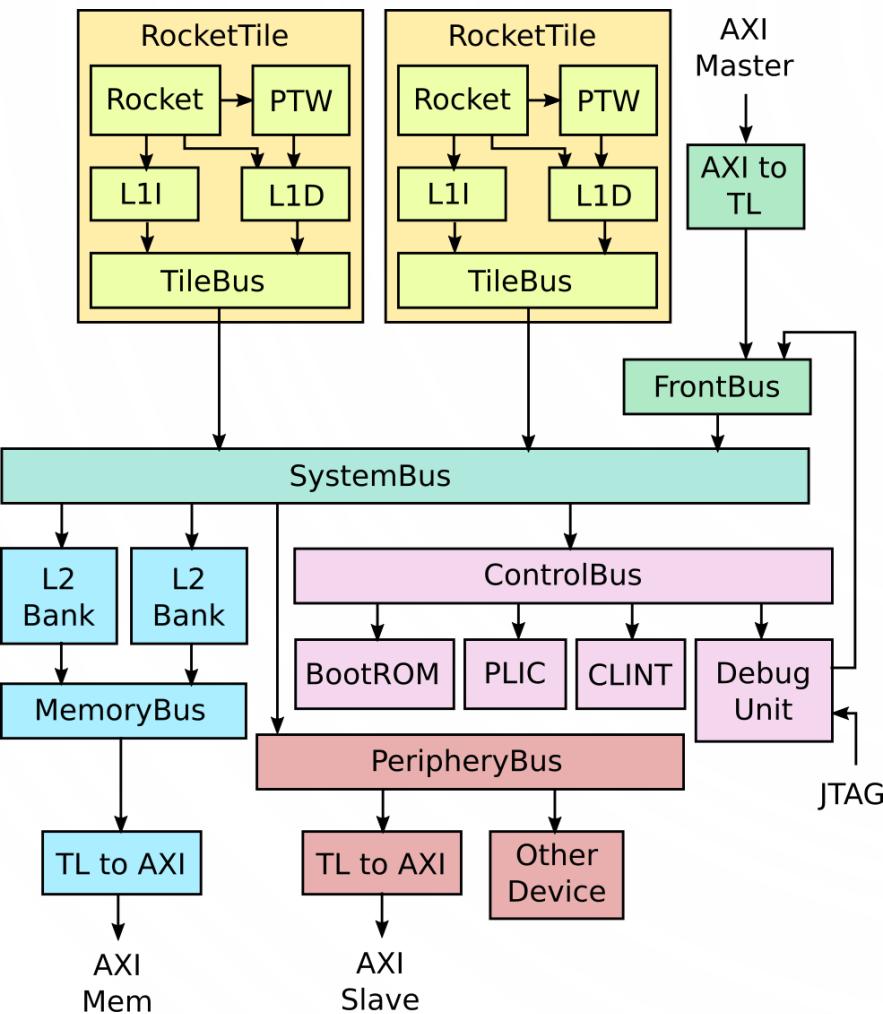
<https://github.com/chipsalliance/rocket-chip>

BOOM Microarchitecture

Front End



RocketChip Generator



Tiles: unit of replication for a core

- CPU
- L1 Caches
- Page-table walker

L2 banks:

- Receive memory requests

FrontBus:

- Connects to DMA devices

ControlBus:

- Connects to core-complex devices

PeripheryBus:

- Connects to other devices

SystemBus:

- Ties everything together

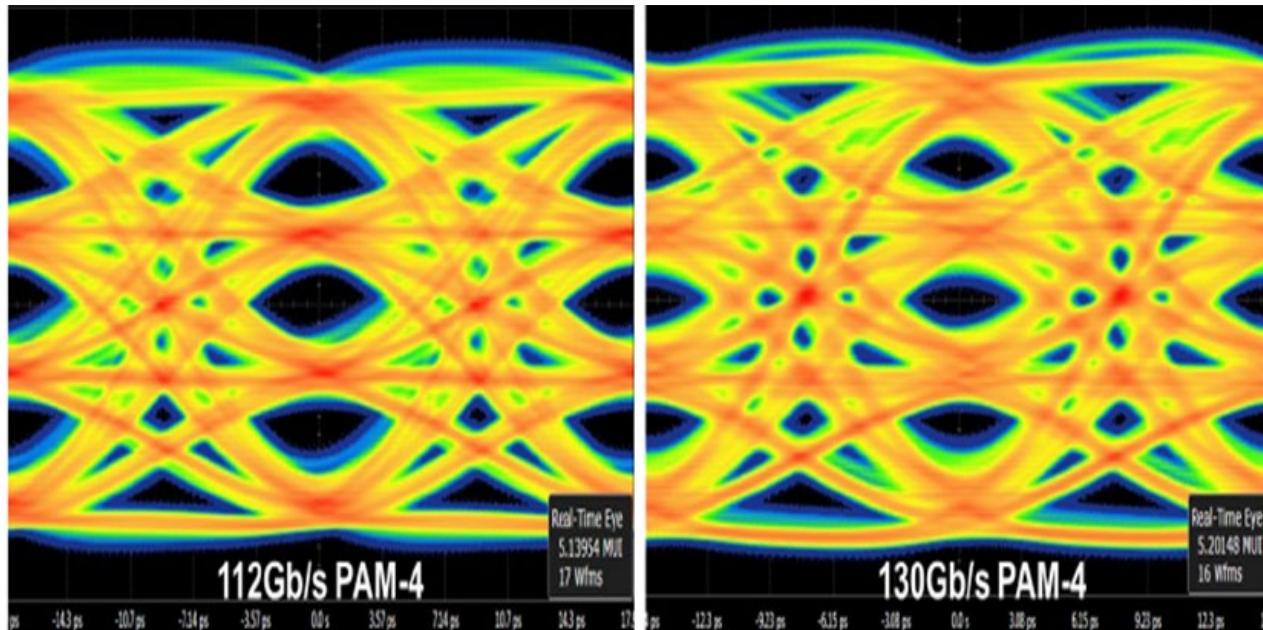
Building Complete SoCs

- Design and simulate complete prototype systems



High-Speed I/O

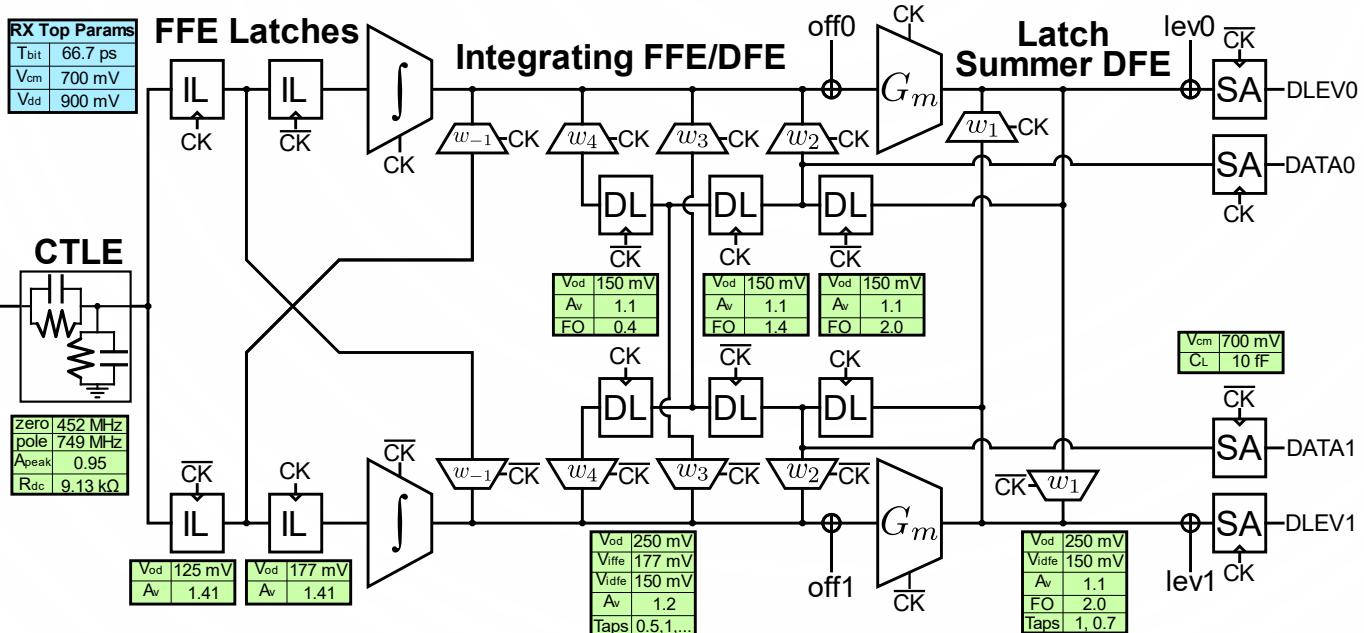
- $28\text{Gb/s} \rightarrow 56\text{Gb/s} \rightarrow 112\text{Gb/s} \rightarrow 224\text{Gb/s} \rightarrow \text{Optical ?}$



TSMC, IEDM'19

We Have a Generator For That, Too!

- But it is mostly analog
- Designed as a Berkeley Analog Generator (BAG)



- Deeper prerequisite chain
- EE105 → EE140/240A → EE240C or 290C (high-speed links)

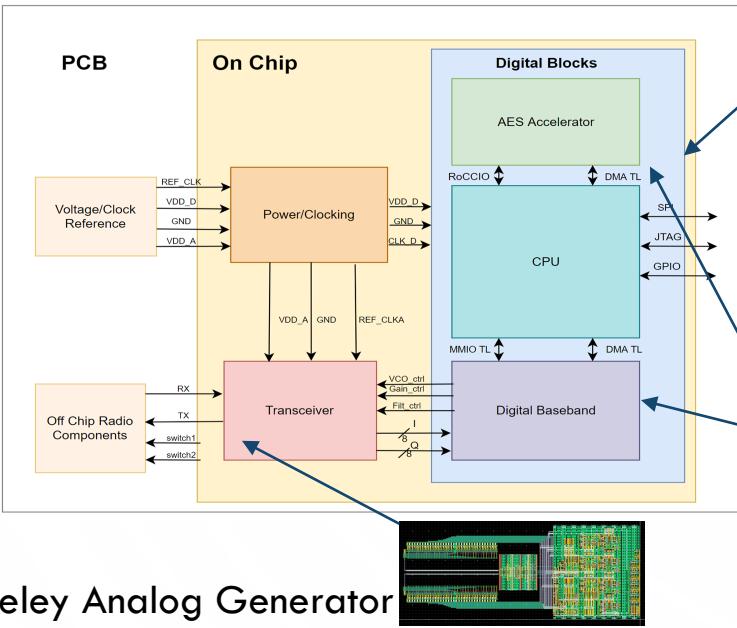
EE251B – Advanced Digital Circuits

- Starts with a deeper dive into technology, devices and models
- SoC architecture, interconnect
- Variability and a case study of large SRAM arrays
- Most of the class is low-power design and power management
- ASIC projects

- Pending campus approval

EE194/290 – Advanced Topics Classes

- Spring'22 Tapeout class (+ testing class, Fall'22)

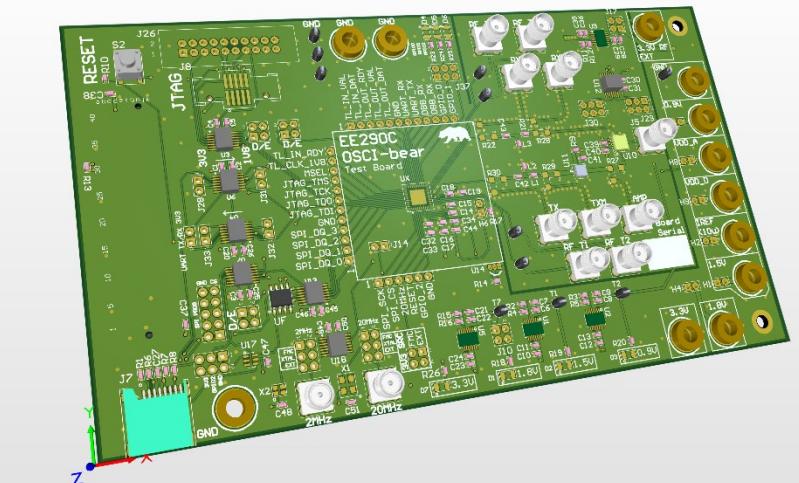
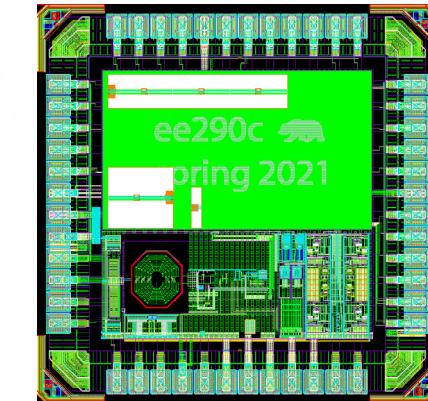


<https://github.com/ucb-bar/chipyard>
Processor core, interfaces
Software tools



<https://www.chisel-lang.org/>
Custom BLE digital baseband,
accelerator wrappers

1mm x 1mm in 28nm



- Spring'22 class will use Intel 16
 - Organizational meeting next Friday
 - Compute accounts, NDAs for technology access

Summary

- We accomplished a lot in this class
 - We hope changes we made were seamless
 - Worked nearly as hard as you did 😊
- We had a ton of fun
- And hope you had too!