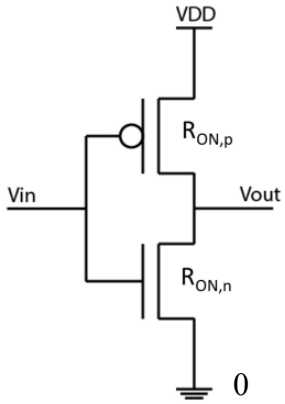
EECS 151/251A Homework 6

Due Friday, October 22th, 2021

Problem 1: Switch model

For the simple inverter shown below, the unrealistic PMOS and NMOS transistors made-up for this problem have on-resistances: $R_{ON,n} = R$, $R_{ON,p} = 3R$, and $V_{TH,n} = VTH$, $|V_{TH,p}| = 2VTH$. Sketch the voltage transfer characteristic for this gate. Assume the simple ON/OFF switch model for the transistors, and clearly annotate all the breakpoints in terms of VDD and VTH. Calculate the noise margins. Answer in terms of coefficients, VDD and VTH.



1. What is V_{OH}? _____
2. What is V_{OL}? _____
3. What is V_{IH}? _____
4. What is V_{IL}? _____
5. What is NMH? _____
6. What is NML? _____
7. What is Vout when Vin reaches VTH? _____

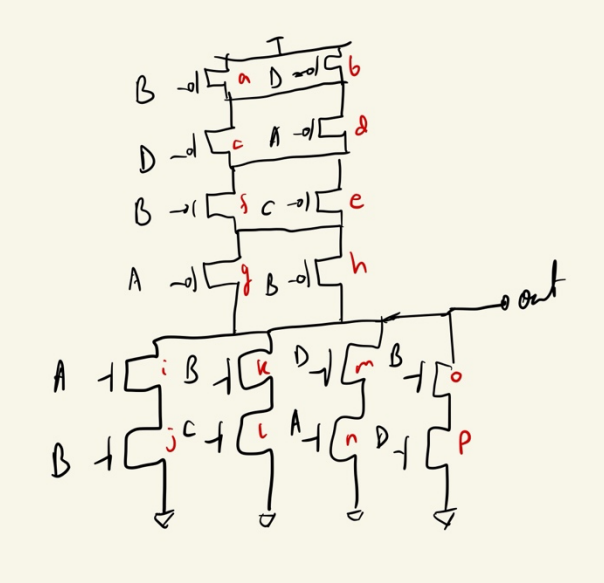
Now assume a more realistic switch model to repeat the same questions from part 1. Your more realistic model (with values unrealistically made-up for this problem) includes the R_{OFF} resistance. Let $R_{OFF,n}$ = 9R, ROFF,p = 5R. The rest of the parameters remain the same as before. Answer in terms of coefficients, VDD and VTH.

1. What is V_{OH}? _____
2. What is V_{OL}? _____
3. What is V_{IH}? _____
4. What is V_{IL}? _____
5. What is NMH? _____
6. What is NML? _____

Problem 2: Static Complementary CMOS

Implement the logic function OUT = (AB + BC + DA + BD)' using a complementary pull-up and pulldown network. Remember to properly size the gates for worst-case pull-up and pull-down delays equivalent to a minimum sized inverter. Our minimum sized inverter (made-up for the

purposes of this problem, in modern technology minimum size is approx. equal for PMOS and NMOS) has PMOS with width 3 and NMOS with width 1 ($R_{ON,pmos} = 3R_{ON,nmos}$).



1. What is the size of transistors marked by the following letters?

   a _____

   b _____

   c _____

   d _____

   e _____

   f _____

   g _____

   h _____

   i _____

   j _____

k _____

l _____

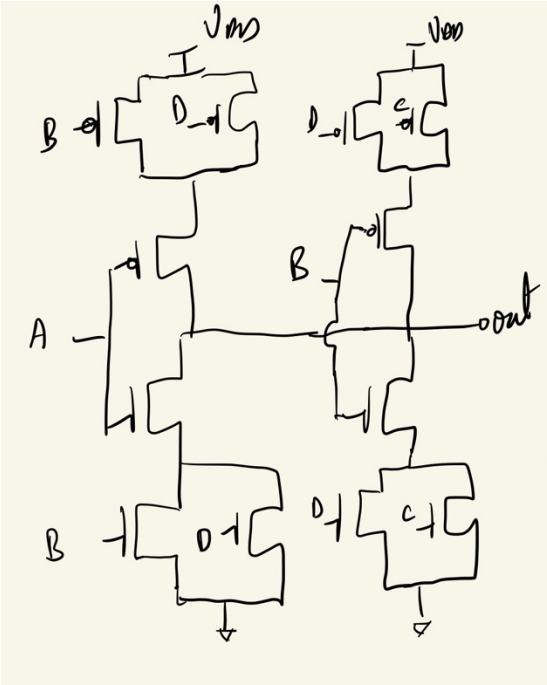
m _____

n _____

o _____

p _____

2. A friend proposes the following implementation of the function in subquestion (1).



Does this perform the same function as the gate from (1)? If it does, enter "-" into the

blank. If not, for which lines in the truth table is there discrepancy or uncertainty (enter as 1,2 if the first and second lines in the truth table are the answer)?

_____

3. Is the gate shown in (2) a static CMOS gate, (enter yes or no)?

_____

Problem 3: CMOS Gate Simplification

Design a complex CMOS logic gate that implements the function below, without simplifying the expression. You can assume you have access to both regular and inverted versions of your inputs. Remember to properly size the gates for worst-case pull-up and pull-down delays equivalent to a minimum sized inverter. Recall that our minimum sized inverter has PMOS with width 1 and NMOS with width 1 ($R_{ON,pmos} = R_{ON,nmos}$).

f(A, B, C) = (A'B'C + AB'C' + A'BC + A'B'C' + B'C')'

1. What is the area of the circuit (Note: Gate area can be estimated as the sum of all transistor widths): _____

2. Using boolean algebra rules, simplify the expression from (1) as far as possible. What is the resulting expression:

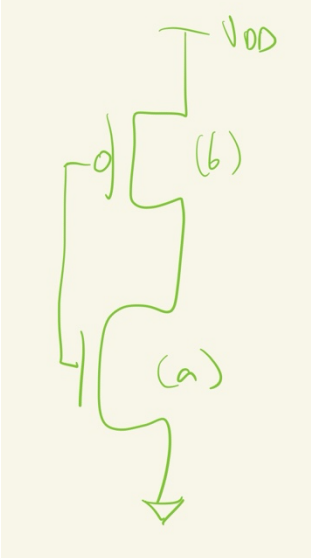
   (a) BC
   (b) A'C' + BC'
   (c) A'C + B'C'
   (d) A'B'C + B'C'

3. Design a CMOS logic gate to implement the reduced function from (2). Size the transistors as usual. What is the new area: _____

Problem 1: RC Delay and Logical Effort

For a CMOS inverter in a process where the PMOS effective on-resistance is J times that of the NMOS (i.e. $R_{on,p} = J \cdot R_{on,n}$) for minimum size transistors. $\gamma = C_d C_g$

1. What is the correct size of each FET for equal pull-up and pull-down strength. Assume the NMOS is of size '1', normalized to the minimum width of the process.



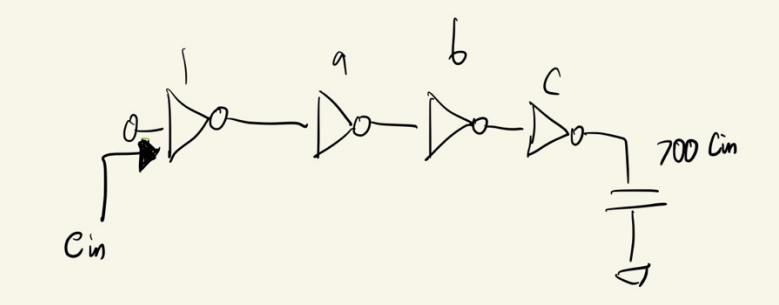
   (a) _____

   (b) _____

2. What is the delay of this inverter if it is unloaded, using RC time constants in terms of Rn, γ, and Cg, J, and ln(2). Call this delay tp. Assume input step transitions. Input answer with '*' between each value (for example: ln(2)*R*C)

   tp = _____

3. For an inverter chain with 4 stages that drives a load CL = 700 · Cin. Assume γ = 1.3 and tinv = 5 ps (the self-loaded intrinsic inverter delay). Size the chain for minimum delay. Give answers to the hundredths. (Note: Determining the total input capacitance for each inverter in terms of Cin is sufficient for sizing; you don't need to find the actual widths)



   Cin,a = _____*Cin
   Cin,b = _____*Cin
   Cin,c = _____*Cin

4. What is the total delay from input to output for part 3?

   _____ ps