

# EECS 151/251A

## Discussion 8

Daniel Grubb 10/19, 10/20, 10/25

# Administrivia

- Lab 6 due Friday 10/22 this
  - Cutoff for checkoffs and submissions is the end of ~~next~~ week's lab sessions
- ~~Project starts this week~~ checkoff #1 this week; piazza updates
  - Do your best to finish up labs and don't procrastinate! choose a lab section
- Homework ~~6~~<sup>7</sup> due Friday 10/~~22~~<sup>29</sup>
- Midterm 1 grades release
  - Regrades due ~~Friday 10/22~~ tomorrow 10/26
- Midterm 2 on the horizon (~~tentatively~~ November 4th), similar format
- What are you having trouble with? Feedback?
- special review session Wednesday evening
- MT 2 review next week

# Agenda

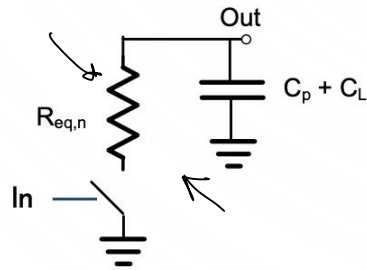
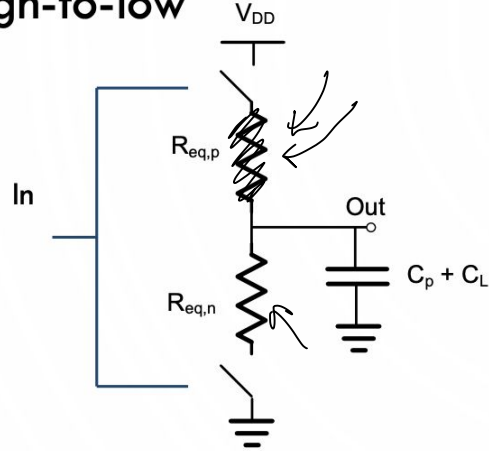
- Topics
  - Inverter delay and sizing
  - Logical effort
  - Path effort
  - Elmore delay
- How familiar/comfortable are you with:
  - transistor switch model?
  - inverter delay?
  - inverter delay optimization?
  - logical effort?
  - parasitic delay?
  - path effort/optimization?

# A Note on Notation and Values

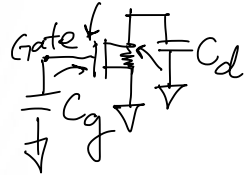
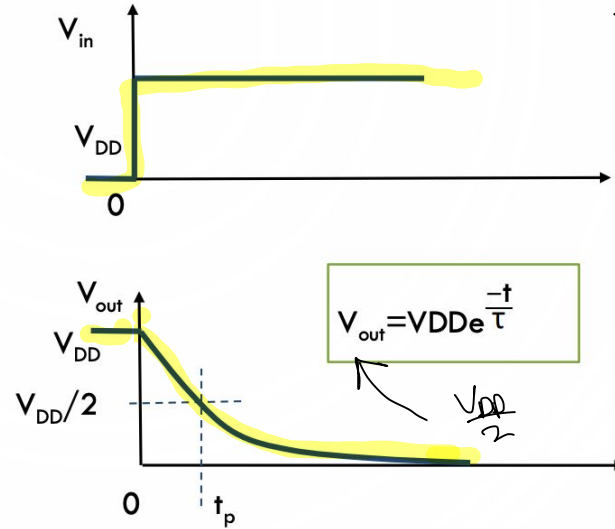
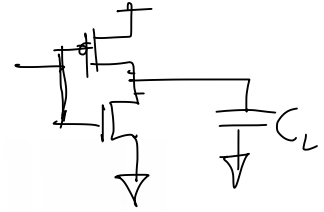
- PMOS / NMOS ratios
  - Old technologies/textbooks give 2:1, this class generally uses 1:1
- Ratio of  $C_d$  to  $C_g = \gamma$  (gamma) = 1
  - Set by process technology
  - $\sim 1.2$  in recent processes, but still keep it 1
- Logical effort
  - **LE** or **g** both used
- Fanout or electrical effort
  - **F** for total fanout
  - **f** for stage fanout
  - **h** also used  $H$

# Inverter RC Delay Model

High-to-low



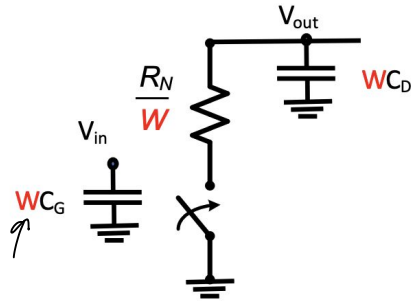
$$C_p = C_{int}$$



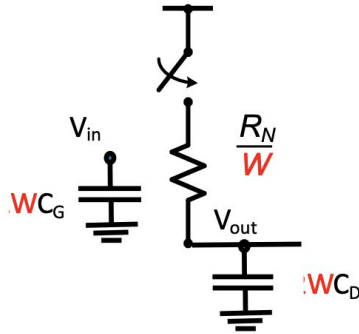
$$t_{p,HL} = (\ln 2) \tau = 0.7 \text{ Req}_{,n} (C_p + C_L)$$

$$\tau = \text{Req}_{,n} (C_p + C_L)$$

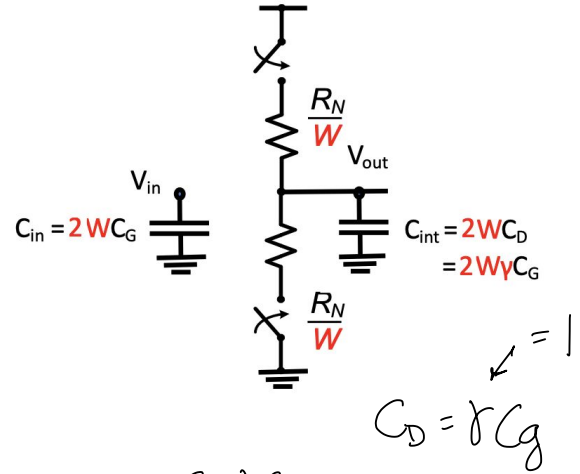
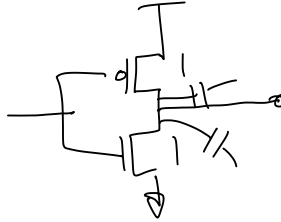
# Inverter Delay



NMOS with size W



PMOS with same R as NMOS



$$t_d = \frac{2WC_D}{t_p} = 0.69 \left( \frac{R_N}{W} \right) (2W\gamma C_G) = 0.69 (2\gamma) R_N C_G$$

Intrinsic inverter delay

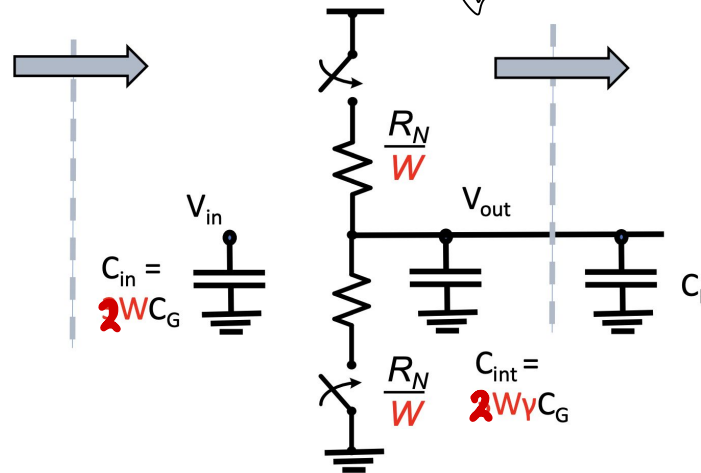
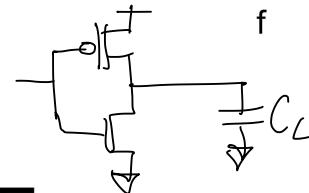
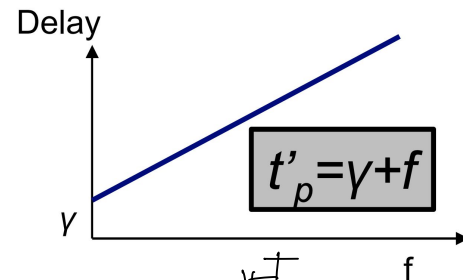
What if we make the inverter bigger?

# Inverter Delay

$$t_{inv}(1+f)$$

- Add a load capacitance now
- Two components
  - Intrinsic delay
  - Fanout,  $f = C_L / C_{in}$
- FO4 delay: how many unit delays?
  - Why is this a useful quantity?

$$\begin{aligned}
 t_p &= 0.69 \left( \frac{R_N}{W} \right) (C_{int} + C_L) \\
 &= 0.69 \left( \frac{R_N}{W} \right) (2W\gamma C_G + C_L) \\
 &= 0.69 (2C_G R_N) \left( \gamma + \frac{C_L}{C_{in}} \right) \\
 &= t_{inv} \left( \gamma + \frac{C_L}{C_{in}} \right) = t_0 (\gamma + f)
 \end{aligned}$$

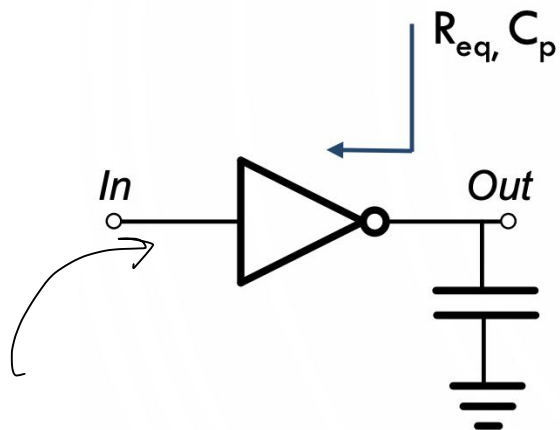


# Inverter Delay Scratch Area



# Inverter Sizing Thought Experiment

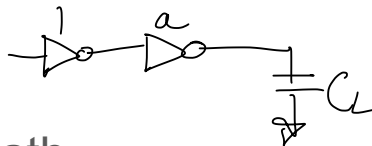
- Say we just have 1 inverter driving a load capacitance
  - We want to minimize delay
  - We can size it anyway we want
  - How should we size it?
- Be careful with this solution!



$C_L = C_{in}$  (next gate)

$$= t_{inv} \left( \gamma + \frac{C_L}{C_{in}} \right) = t_0 (\gamma + f)$$

# Inverter Chain Sizing

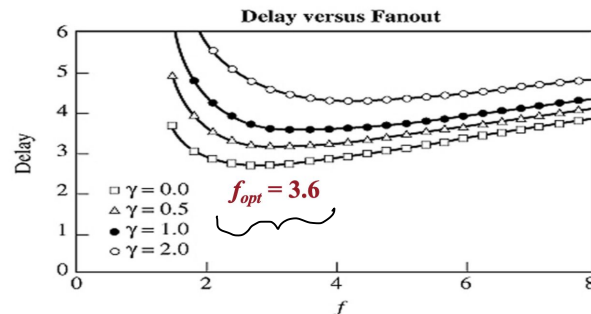
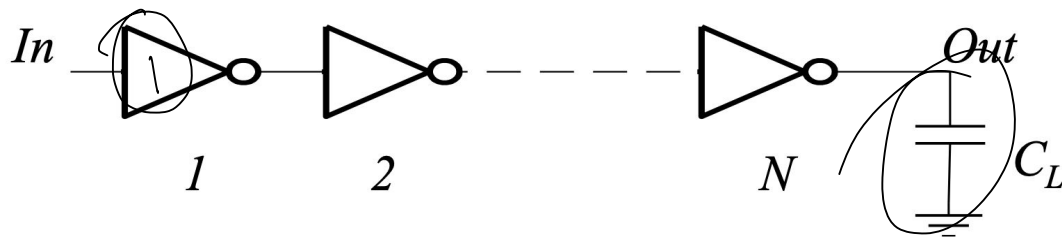


$$\frac{C_{in,j}}{C_{in,j-1}} = \frac{C_{in,j+1}}{C_{in,j}}$$

- Goal: minimize the delay of the path
  - Constrain the size of the first inverter + load capacitance in each case
  - What's a first pass solution?
- (1) Size a chain given N inverters
  - Key result: size stages to have identical fanout (minimize the total chain delay expression)
    - What does this say about each stage's delay?
  - Find  $f$ :  $f^N N = F = C_L / C_{in,1}$   $\sqrt[N]{F}$
  - Start from beginning or end of chain

$$t_p = N t_{inv} \left( \gamma + \sqrt[N]{F} \right), \quad F = C_L / C_{in}$$

- (2) Determine optimal N and size the chain
  - Assume fanout,  $f=4$  (from graph)  $\log_4(F) = N$
  - Find number of stages, N (integer): ?  $\sqrt[N]{F}$
  - Same steps as (1)

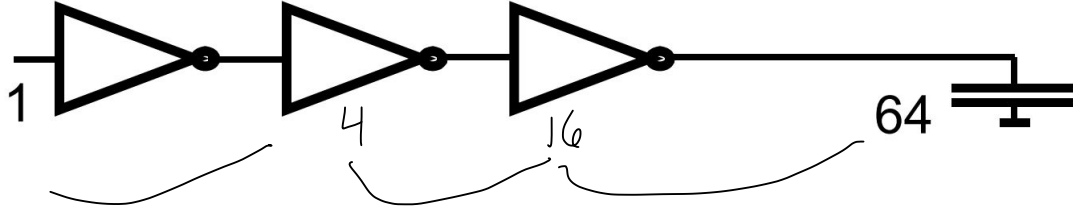


# Inverter Chain Sizing Examples

- Chain of 3 with load cap of 64:
  - What if we add a capacitance in the middle?

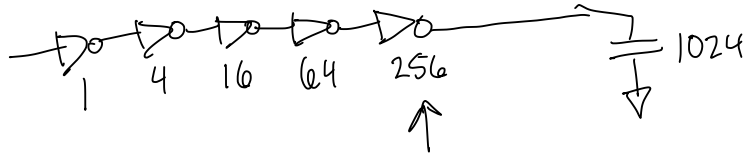
$$F = 64$$

$$\sqrt[3]{64} = 4$$



- Load cap. of 1024, give N and sizings:
  - What if non-integer?

$$\log_4(1024) = 5$$



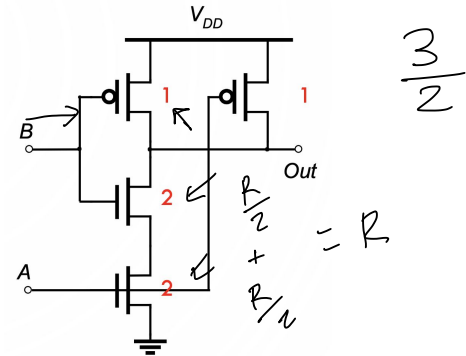
# Logical Effort and Parasitic Delay

- How much worse is a gate at driving a load capacitance than an inverter with the same input capacitance? (other ways to look at it) ←
  - Looks like an inverter, but the fanout seems larger
  - Easy way: size gate to deliver same as inverter current, take cap. Ratio
- $$LE = (R_{eq,gate} C_{in,gate}) / (R_{eq,inv} C_{in,inv}) \quad LE = \frac{C_{in,gate}}{C_{in,inv}}$$
- Parasitic delay: delay of gate driving no load (set by internal cap.)
  - Find gate RC delay, then extract  $t_{inv}$  term; ratio of internal cap to inverter

Effective Fanout (EF)

$$t_{pgate} = t_{inv} (p_{gate} + LE \cdot f)$$

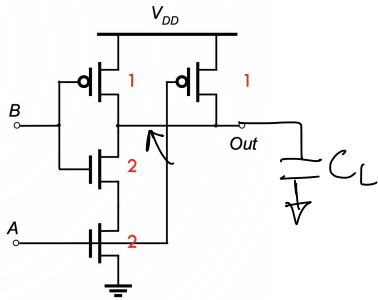
$t_{pgate}$  ← parasitic delay  $\neq f(W)$      
  $p_{gate}$  ← logical effort  $\neq f(W)$      
  $LE \cdot f$  ← electrical fanout



# Logical Effort/Parasitic Delay Examples

$$t_p = t_{inv} \left( 2\gamma + \frac{3}{2} f \right)$$

- Also, consider if the PMOS/NMOS resistances are different than nominal?

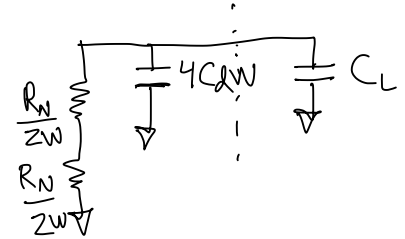


$$\ln(2) \left( \frac{R_N}{W} \right) (4W\gamma C_g + C_L)$$

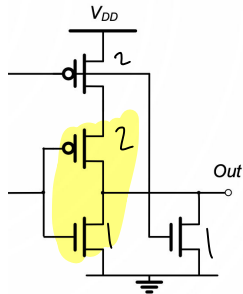
$$\ln(2) (4\gamma R_N C_g + C_L \cdot \frac{R_N}{W})$$

$$\underbrace{\ln(2) (2R_N C_g)}_{t_{inv}} \left( 2\gamma + C_L \cdot \frac{R_N}{W} \cdot \frac{1}{2R_N C_g} \right)$$

$$t_{inv} \left( \underset{P}{2\gamma} + \underset{g}{\frac{3}{2}} \underset{h}{\frac{C_L}{C_{in}}} \right)$$

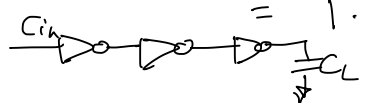


$$C_{in, NAND} = 3W C_g$$



# Path Delay

$$PE = \prod g_i \cdot H \cdot \prod b_i$$

$$= 1 \cdot \frac{C_L}{C_{in}} \cdot 1 = H$$


$$G = \prod g_i$$

$$F = \prod f_i = \prod g_i h_i$$

$$B = \prod b_i$$

- How do we minimize delay more generally?

$$\text{Delay} = t_{inv} \sum (p_i + LE_i \cdot f_i) \quad t_{inv}(p + f) \text{ inverter}$$

- Path fanout:  $F = C_L / C_{in}$

- Path LE:  $G = g_1 g_2 \dots g_N$

$$b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}}$$

$$t_{inv}(p + LE \cdot f) = t_{inv}(p + g \cdot h)$$

- Branching effort

- Use similar result to inverter chain

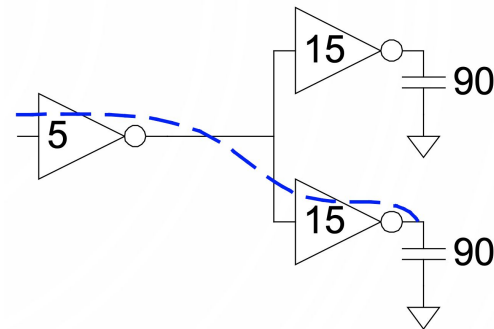
- Best EF is still around 4

- Design process:

- Calculate Path Effort:  $PE = GFB$
- Estimate best number of stages:  $N = \log_4 F$
- Calculate Effective Fanout per stage:  $EF = PE^{(1/N)}$
- Size the gates from beginning or end of chain

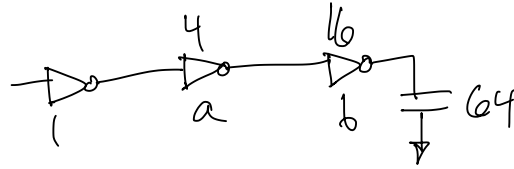
$$B = \prod b_i$$

$$N \sqrt{PE}$$



- Can always add inverters to the end of the chain

# Path Delay Scratch Area



$$\sqrt[3]{64}$$
$$= 4$$

$$f = \frac{C_L}{b}$$

$$4 = \frac{64}{b}$$

$$b = 16$$

$$f = \frac{b}{a}$$

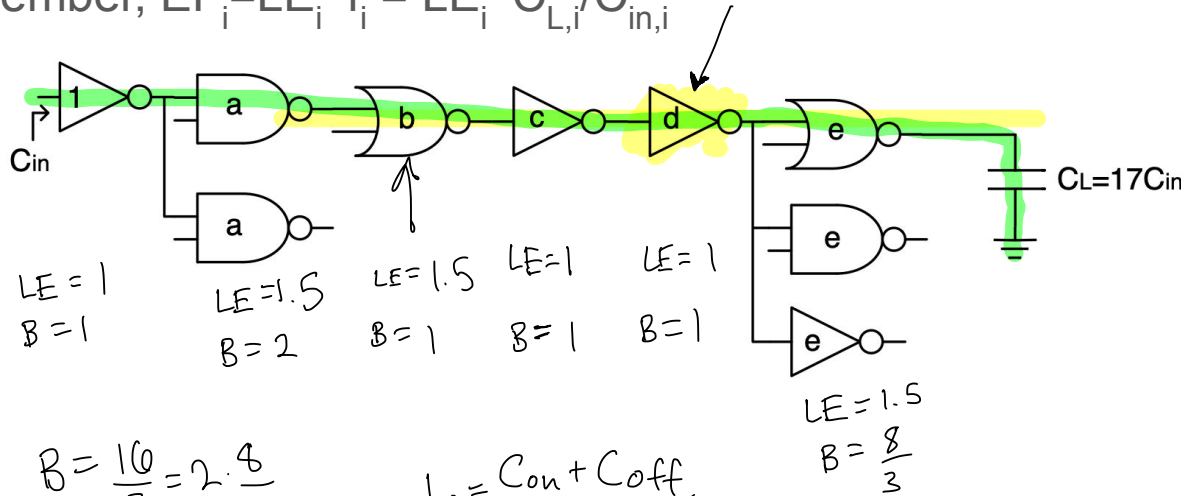
$$4 = \frac{16}{a}$$

$$a = 4$$

# Path Delay Example

- Remember,  $EF_i = LE_i \cdot f_i = LE_i \cdot C_{L,i} / C_{in,i}$

$$\frac{3+3+2}{3} = \frac{8}{3}$$



$$G = (1.5)^3$$

$$LE = 1$$

$$B = 1$$

$$LE = 1.5$$

$$B = 2$$

$$LE = 1.5$$

$$B = 1$$

$$LE = 1$$

$$B = 1$$

$$LE = 1$$

$$B = 1$$

$$LE = 1.5$$

$$B = \frac{8}{3}$$

$$b_i = \frac{C_{on} + C_{off}}{C_{on}}$$

$$H = 17$$

$$B = \frac{10}{3} = 2 \cdot \frac{8}{3}$$

$$N = 6$$

$$PE = GHB = (1.5)^3 \cdot 17 \cdot \frac{10}{3}$$

$$\sqrt[N]{PE} = EF$$

$$f^N = F$$

inverter chain

$$PE \sim F$$

$$EF \sim f$$

EF is same for all stages

$$EF_e = g_e \cdot h_e$$

$$\sqrt[N]{PE} = 1.5 \cdot \frac{C_L}{e}$$

$$EF_d = g_d \cdot h_d \cdot b$$

$$\sqrt[N]{PE} = 1 \cdot \frac{e}{d} \cdot \frac{8}{3}$$

$$EF_c = 1 \cdot \frac{d}{c}$$

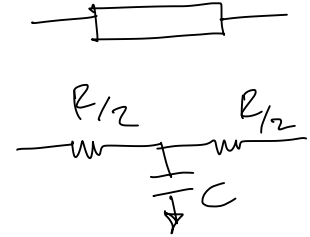
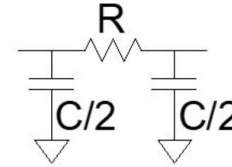
$$EF_b = g_b \cdot \frac{c}{b}$$

$$EF_a = g_a \cdot \frac{b}{a}$$

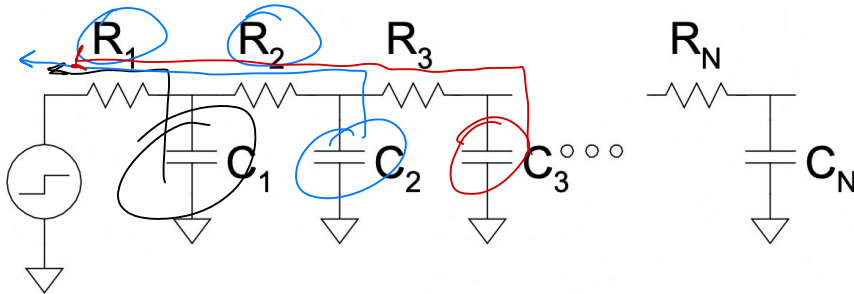


# Elmore Delay

- Approximate RC time constant of a tree network
- R's and C's include both transistors/parasitics and wires
  - Wire  $\pi$  model (where does the R and C come from?)
- Can think of it as:
  - $\sum [C_i \times (\text{sum of R's charging } C_i)]$
  - $\sum [R_i \times (\text{sum of C's that } R_i \text{ charges})]$



$$R_1 (C_1 + C_2 + C_3 + \dots C_N) + \dots$$



$$t_{pd} \approx \sum_{\text{nodes } i} R_{i\text{-to-source}} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + \dots + (R_1 + R_2 + \dots + R_N) C_N$$

$$+ (R_1 + R_2 + R_3) C_3$$

# Elmore Delay Examples

- What information do we need?
- Draw the equivalent model
- Calculate delay to outputs

