EECS 151/251A Homework 5

Due Friday, March 18th, 2022

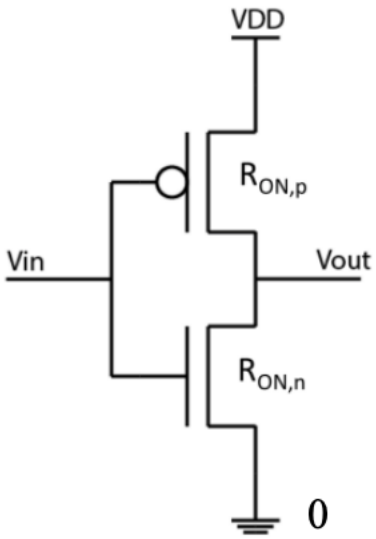
Problem 1: Static Complementary CMOS

(a) Draw the transistor implementation of the logic function OUT = [(AB + BC)*D]' using a complementary pull-up and pulldown network.

(b) Draw the transistor implementation of the logic function OUT = [A*C*B+D]' using a complementary pull-up and pulldown network.

(c) Draw the transistor implementation of the logic function OUT = [A*B + C*D]' using a complementary pull-up and pulldown network.

Problem 2: Inverter Delay



For this CMOS inverter, assume the PMOS effective on-resistance is the same as that of an NMOS (R_{ON}) for minimum sized transistors as well as the drain capacitance C_d.
V_{out} was previously 0, and then Vin was suddenly flipped to 0 (assume instantaneous transition). Sketch the resulting transition at V_{out} assuming a minimum sized PMOS and NMOS.

Using the RC time constant in terms of R_{on} and C_d, calculate and label propagation delay (t_p) on the plot.

If the size of the PMOS transistor doubles, sketch the new transition, with the new propagation delay labeled, on the same plot

If the size of the PMOS transistor halves, sketch the new transition, with the new propagation delay labeled, on the same plot.