EECS 151/251A SP2022 Discussion 6

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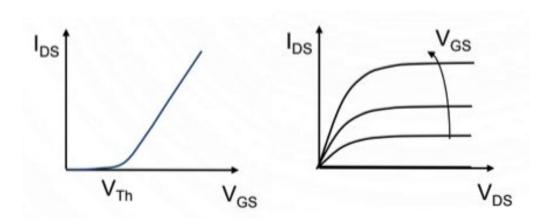
Agenda

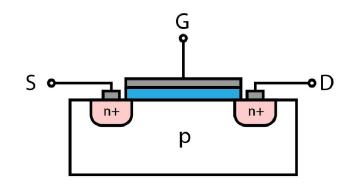
- MOS
- CMOS
- Inverters/Inverter Chain

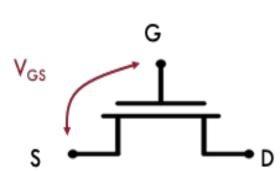
MOS

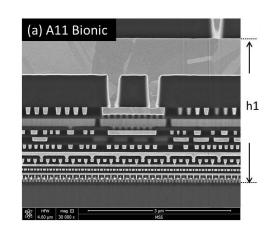
Metal Oxide Semiconductor (MOS) Transistors

- Used to be made in a planar process
 - Wafer is usually p-doped
 - 3 main contacts
 - Gate
 - Source
 - Drain
 - Gate controls current flow from Source to Drain



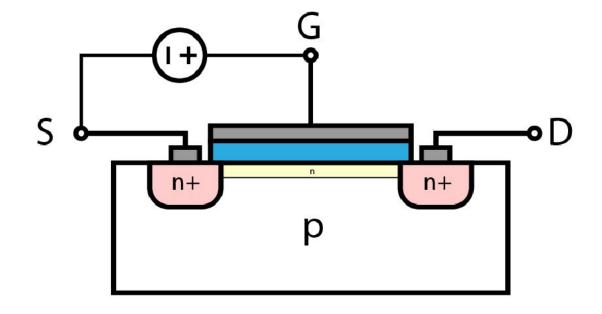






Metal Oxide Semiconductor (MOS) Transistors

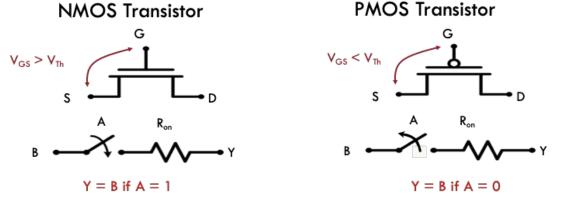
- MOS turns "on" when voltage applied across gate-source
- Voltage causes top layer of silicon to invert types, connecting S to D



Metal Oxide Semiconductor (MOS) Transistors

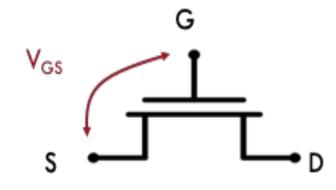
- MOS transistors are non-ideal switches
 - $0 < R_{ON} << R_{OFF} < \infty$
- NMOS
 - The source of NMOS always at lower voltage
 - Ideal for passing *low* voltage (0, gnd)
- PMOS
 - The source of PMOS always at higher voltage
 - Ideal for passing high voltage (1, vdd)
- The 'effective' source node can change depending on the voltage at the MOS' terminals





MOS

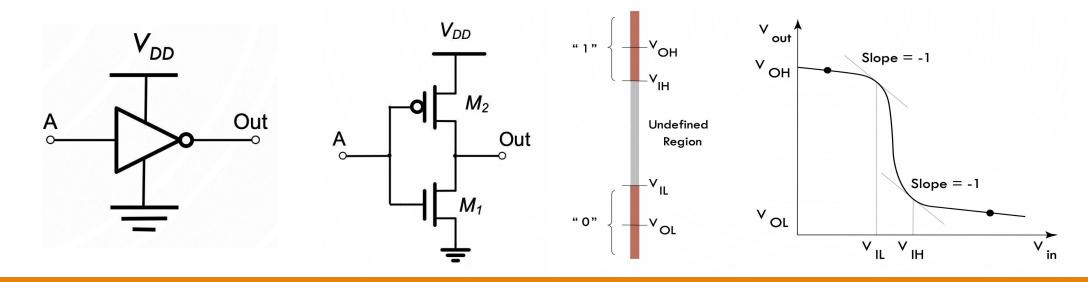
- In this class, you only need to know:
 - MOS switch model
 - On-resistance is proportional to Length/Width
 - Difference of NMOS/PMOS
 - NMOS: good for passing 0 (grounding) , bad 1
 - PMOS: good for passing 1 (supply voltage), bad 0
 - Simplified parasitic capacitance (C_p, C_{in})



CMOS

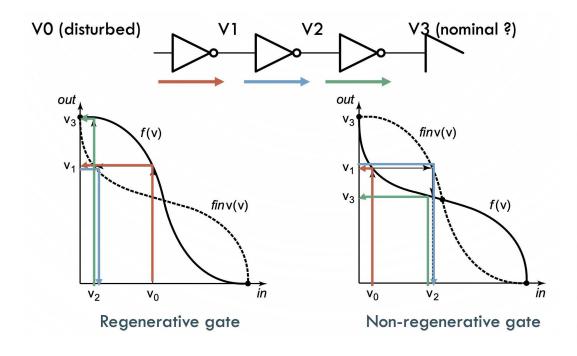
CMOS Inverter

- Complementary Metal Oxide Semiconductor
 - Inverter has 1 NMOS and 1 PMOS
- NMOS and PMOS each have an "on" and "off" resistance
- Voltage Transfer Curve (VTC)
 - Mid/switching-point is a function of PMOS vs NMOS strength



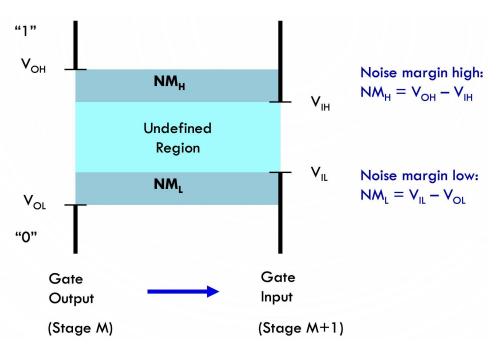
CMOS Margins

- Noisy, but still want 1s and 0s (digital)
 - "Restoration" / "regeneration" property



Noise margins

- The amount of noise that can be tolerated such that the signal can be correctly interpreted by the next gate
- Eg. in a chain of inverters

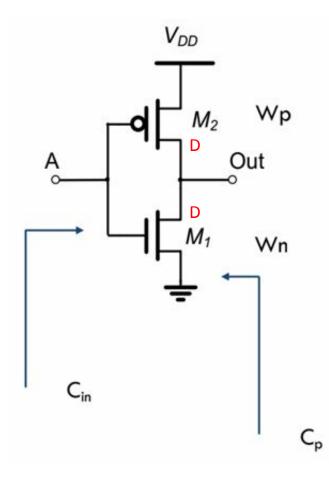


CMOS Exercise

• Implement a NAND gate in CMOS:

CMOS Inverters

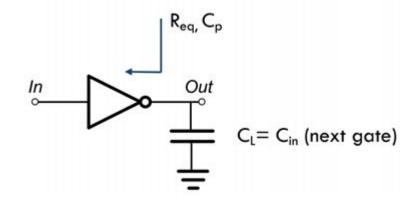
Impact of Inverter Sizing



- $C_{in} \propto WL, C_{p} \propto W$
 - C_{in} dominated by C_{g,pmos} + C_{g,nmos}
 - $C_p = \gamma C_{in} \cdot C_p$ is dominated by $C_{d,pmos} + C_{d,nmos} \cdot \gamma \approx 1$.
- $R_{eq} \propto L/W$
- Inverter usually sized for $t_{p,LH} = t_{p,HL}$
 - How is $W_p: W_n$ a function of $\rho_p: \rho_n$?
- How does the RC delay change if:
 - Either W_p or W_n doubled?
 - o Both W_p and W_n doubled?

Loaded Inverter Delay

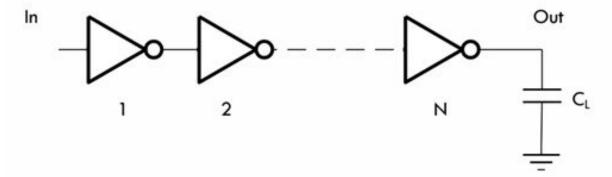
$$\begin{split} t_{p,inv} &= ln2 \cdot R_{eq} \left(C_{p,tot} + C_L \right) \\ &= ln2 \cdot R_{eq} C_{p,tot} \left(1 + \frac{C_L}{C_{p,tot}} \right) \\ &= ln2 \cdot R_{eq} C_{p,tot} \left(1 + \frac{C_L}{\gamma C_{in}} \right) \\ &= ln2 \cdot R_{eq} C_{p,tot} \left(1 + \frac{f}{\gamma} \right) \\ &= ln2 \cdot \tau_{inv} \left(1 + \frac{f}{\gamma} \right) \end{split}$$

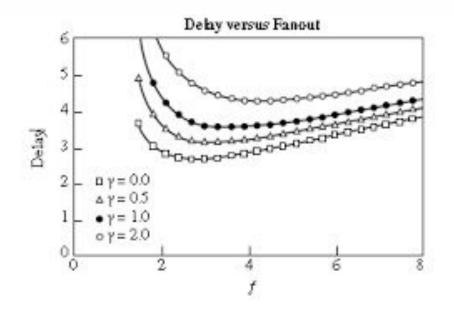


- Intrinsic vs. Extrinsic delay
 - $\circ \quad \text{Intrinsic } \tau_{\text{inv}} \text{ independent of sizing}$
- Fanout $\mathbf{f} = \mathbf{C_L}/\mathbf{C_{in}}$
- Generalizable to any CMOS gate

Inverter Chain Sizing

- Goal: minimize path delay
 - Assume 1st inverter has unit size $(C_{in.1} = 1)$
- Path delay D = $t_{p1} + ... + t_{pN} = (1 + f_1) + ... + (1 f_N)$
- Path fanout F = C_L / C_{in}
- Solution
 - Take partial derivatives w.r.t C₂, ..., C_N
 - \circ Get $f_1 = f_2 = ... = f_N$
 - Min. path delay = Nf + N = N \sqrt{F} + N
 - Size backwards





Questions?