

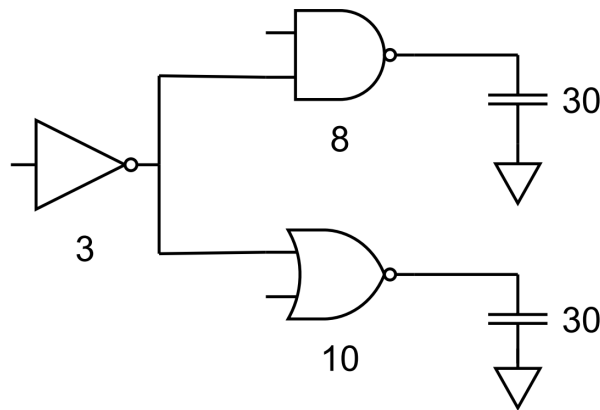
EECS 151/251A Homework 7

Due 11:59pm Friday, October 29th, 2021

Assume $\gamma = 1$, $L = L_{min}$, and $W_p = W_n$ for all problems unless otherwise specified. Delays should be answered in units of ps unless otherwise specified. Any logic gates pictured can be assumed to be static CMOS gates, as discussed in the course, unless otherwise specified. Submit your answers on Gradescope.

1 Logical Effort

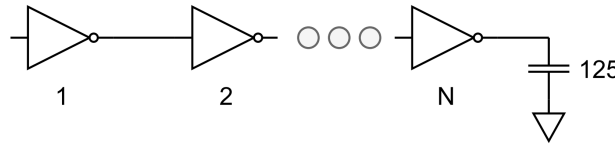
Consider the following set of gates. Each gate is sized as labeled. Fill in the values below according to the unit capacitance values given in the diagram. The path we care about is from the input on the left to the output on the top branch (through the NAND gate).



- B (branching effort) $\frac{8+10}{8}$
- G (path logical effort) $(1)(1.5)$
- H (total fanout) $\frac{30}{3}$
- PE (path effort) $\frac{3}{2} \cdot 10 \cdot \frac{9}{4}$
- h1 (fanout of first stage)
- h2 (fanout of second stage)

2 Minimum Delay

(a) Consider a chain of inverters starting with a unit input capacitance inverter (C_{in} of chain is 1) driving a capacitive load of 125. What is the number of inverters in the chain that will minimize the delay? What is the delay in terms of t_{inv} ?



$$\log_4(125) = 3.4$$

$$\sqrt[3]{125} = 5 \quad \sqrt[4]{125} = 3.3$$

$$t_{p3} = 3 \cdot t_{inv}(1+5) = 18t_{inv} > t_{p4} = 4 \cdot t_{inv}(1+3.3) = 17.2t_{inv}$$

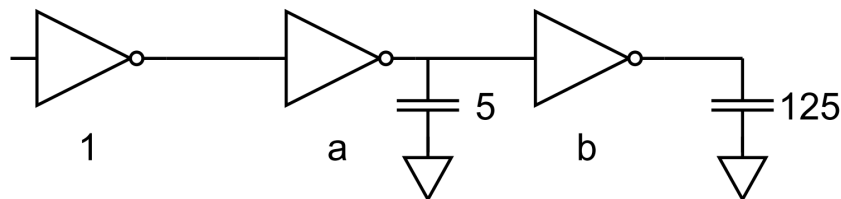
Optimal number of inverters:

4

Delay (t_{inv}):

17.2

(b) Now consider a chain of 3 inverters, again starting with a unit sized inverter and driving a capacitive load of 125. There is a parasitic capacitance of 5 in between the second and third inverters. Size the a and b inverters for minimum delay.



$$\frac{t_p}{t_{inv}} = \left(1 + \frac{a}{1}\right) + \left(1 + \frac{5+b}{a}\right) + \left(1 + \frac{125}{b}\right)$$

a

5.6

b

26.4

$$\frac{\partial t_p}{\partial a} = 1 - \frac{5+b}{a^2} = 0 \rightarrow a^2 = 5+b$$

$$\frac{\partial t_p}{\partial b} = \frac{1}{a} - \frac{125}{b^2} = 0 \rightarrow b^2 = 125a$$

3 Fanout-of-4

(a) A fanout-of-4 inverter is an inverter driving a capacitive load giving a fanout of 4 (eg. driving four other inverters of the same size). The delay of a fanout-of-4 inverter is a useful quantity for a designer to know. What is the delay of a fanout-of-4 inverter in terms of t_{inv} ?

5

$$t_p = t_{inv} (1 + f) = t_{inv} (1 + 4) = 5 t_{inv}$$

(b) Suppose that in a given process technology, the equivalent resistance of a unit transistor has an equivalent resistance of $12k\Omega$ and the equivalent drain capacitance is $0.15fF$. What is the delay of a FO4 inverter in ps ?

12.5

$$t_{inv} = \ln(2) \cdot 2RC = \ln(2) \cdot 2 \cdot 12k\Omega \cdot 0.15fF = 2.5ps$$

$$t_p = 5(2.5ps)$$

(b) We can similarly define other useful quantities like a fanout-of-3 NAND-2 gate.

(i) What is the delay of an FO3 NAND-2 gate in this technology?

15

$$t_{p,NAND} = t_{inv}(p + g_h) = (2.5ps)(2 + 1.5 \cdot 3)$$

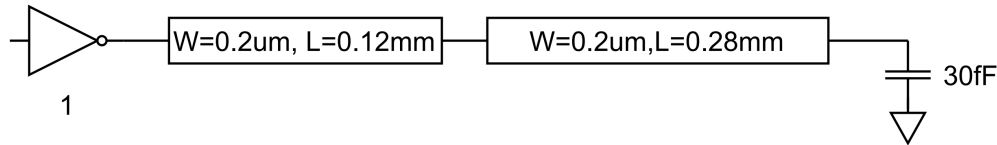
(ii) What is the delay of an FO3 NAND-2 gate in terms of FO4 delays?

1.2

$$\frac{15}{12.5}$$

4 Elmore Delay

Consider the following network of an inverter and two physical wires. The wire capacitance is $C_w = 0.2\text{fF}/\mu\text{m}$ and the wire resistance is $0.2\Omega/\text{square}$. A unit transistor has an equivalent resistance of $12\text{k}\Omega$ and the equivalent drain capacitance is 0.15fF . Estimate the delay of this network using Elmore delay.



$$R_{w1} \quad 120\Omega$$

$$C_{w1} \quad 24\text{fF}$$

$$R_{w2} \quad 280\Omega$$

$$C_{w2} \quad 56\text{fF}$$

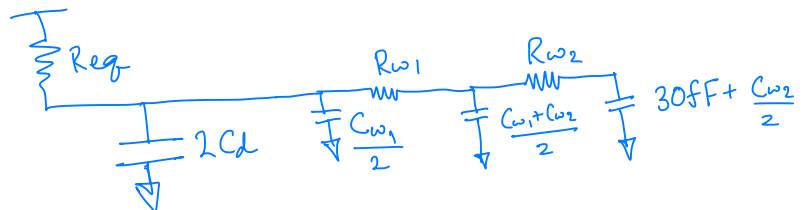
$$\text{Elmore Delay} \quad 1.4\text{ns}$$

$$R_{w1} = \frac{0.2\Omega}{\square} \times \frac{0.12\text{mm}}{0.2\mu\text{m}}$$

$$C_{w1} = \frac{0.2\text{fF}}{\mu\text{m}} \times 0.12\text{mm}$$

$$R_{w2} = \frac{0.2\Omega}{\square} \times \frac{0.28\text{mm}}{0.2\mu\text{m}}$$

$$C_{w2} = \frac{0.2\text{fF}}{\mu\text{m}} \times 0.28\text{mm}$$



$$\begin{aligned} t_p &\approx R_{eq} (2C_d + C_{w1} + C_{w2} + 30\text{fF}) + R_{w1} \left(\frac{C_{w1}}{2} + C_{w2} + 30\text{fF} \right) + R_{w2} \left(\frac{C_{w1} + C_{w2}}{2} + 30\text{fF} \right) \\ &\approx 12\text{k}\Omega (0.3\text{fF} + 24\text{fF} + 56\text{fF} + 30\text{fF}) + 120\Omega (12\text{fF} + 56\text{fF} + 30\text{fF}) + 280\Omega (28\text{fF} + 30\text{fF}) \\ &\approx 1.4 \times 10^{-9}\text{s} \end{aligned}$$

5 NAND-4

Here, we will explore two different ways of designing a NAND-4 gate driving a load that is 64x the input capacitance of the NAND-4 gate (ie. $C_L = 64C_{in}$).

(a) First, we can try building a single stage, unit size, four input NAND gate. We want to size the transistors to have a drive equal to a unit inverter.

(i) How would you size the PMOS transistors? 1

(ii) How would you size the NMOS transistors? 4

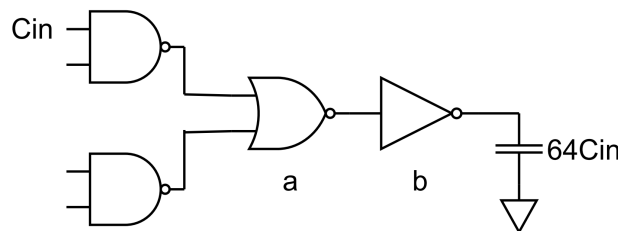
(iii) What is the logical effort of this gate? $\frac{5}{2}$

(iv) What is the parasitic delay of this gate? 4

(v) What is the overall delay of this NAND-4 gate driving C_L , in terms of number of t_{inv} ?

$$t_p = t_{inv} \left(4 + \frac{5}{2} \cdot 64 \right) = 164 t_{inv}$$

(b) Here is another way to design a NAND-4 gate. The input capacitance looking into one input is C_{in} (note that the C_L is $64C_{in}$ like in part (a)).



$$\begin{aligned} B &= 1 \\ F &= 64 \\ G &= (1.5)(1.5)(1) \end{aligned}$$

$$PE = 144$$

$$EF = \sqrt[3]{144} = 5.2$$

$$5.2 = 1.5 \cdot \frac{64 C_{in}}{b}$$

$$b = 12.3$$

$$5.2 = 1.5 \cdot \frac{12.3}{a}$$

$$a = 3.5$$

(i) How would you size the NOR gate (a) for optimal delay?

$$\boxed{3.5}$$

(ii) How would you size the inverter (b) for optimal delay?

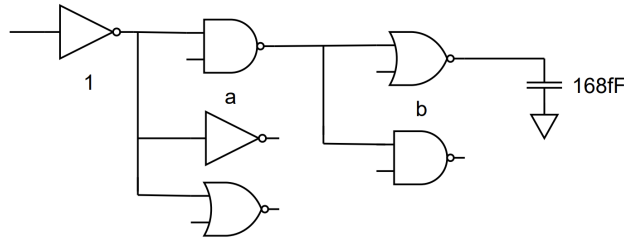
$$\boxed{12.3}$$

(iii) What is the total delay of this circuit in terms of t_{inv} ?

$$\frac{t_p}{t_{inv}} = \left(2 + 1.5 \frac{3.5}{C_{in}} \right) + \left(2 + 1.5 \frac{12.3}{3.5} \right) + \left(1 + \frac{64 C_{in}}{12.3} \right)$$

6 Path Effort

Consider the following chain of gates, which starts with a unit sized inverter. **Assume that the C_{in} looking into the first inverter is $2fF$.**



(a) Fill in the following values and size the gates for minimum delay **in terms of their input capacitance in units of fF .**

G

$1 \cdot 1.5 \cdot 1.5$

H

$\frac{168}{2}$

B

$3 \cdot 2$

Path Effort $(2.25)(84)(6)$

$\sqrt[3]{1134} = 10.4$

Size (a) NAND gate (fF)

$EF = LE \cdot f \cdot b$

$10.4 = 1.5 \cdot \frac{168}{b}$

Size (b) NOR gate (fF)

$10.4 = 1.5 \cdot \frac{24.2}{a} \cdot 2$

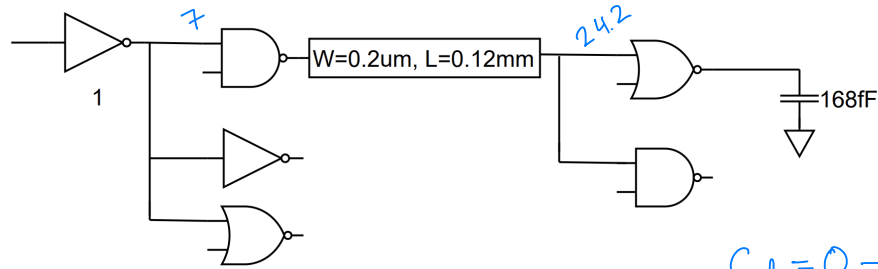
(b) **(251 only, 151 optional)** You are now allowed to add inverters to the end of the chain. How many inverters should you add to the end of the chain to give minimum delay, assuming all the gates were then sized optimally? Polarity of the output does not matter.

Number of inverters to add:

$\log_4(PE) = \log_4(1134) = 5$

(c) **(251 only, 151 optional)** Now, suppose there is a physical wire inserted into the circuit as below. The wire capacitance is $C_w = 0.2fF/\mu m$ and the wire resistance is $0.2\Omega/\text{square}$. **Also, suppose that the drain capacitance of all transistors is now 0, $C_d = 0$ (gate capacitance is unaffected).** Consider one parasitic inverter delay (t_{inv}) to be $1.7ps$. The capacitance looking into the first inverter is again $2fF$.

Using your gate sizes from part (a) (remember that we sized them in terms of their input capacitance), what is the total delay of this circuit in ps ?



$$R_w = \frac{0.2 \Omega}{\square} \cdot \frac{(0.12 \text{ mm})}{0.2 \mu\text{m}} = 12 \Omega$$

$$C_w = \frac{0.2 \text{ fF}}{\mu\text{m}} \times 0.12 \text{ mm} = 24 \text{ fF}$$

$$C_d = 0 \rightarrow p = 0$$

$$t_{\text{inv}} = 1.7 \text{ ps}$$

$$t_p = t_{\text{inv}} \cdot \frac{(3)(7 \text{ fF})}{2 \text{ fF}} + t_{\text{inv}} \cdot \frac{3}{2} \cdot \frac{C_w + (2)(24.2 \text{ fF})}{7 \text{ fF}} + \ln(2) \cdot 120 \Omega \cdot \left(\frac{C_w}{2} + (2)(24.2 \text{ fF}) \right) + t_{\text{inv}} \cdot \frac{3}{2} \cdot \frac{168 \text{ fF}}{24.2 \text{ fF}}$$

$$t_p \approx 67 \text{ ps}$$