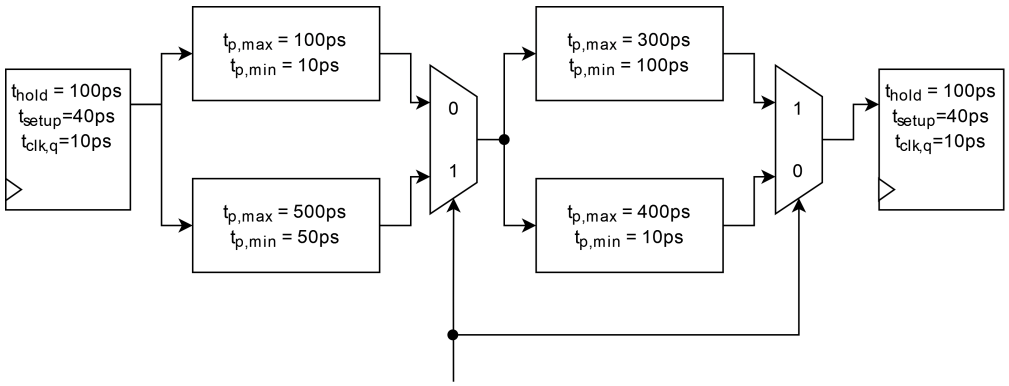
EECS 151/251A: Homework 9

Due Friday, April 29th

Problem 1: The evil, timing violation...

Consider the following sequential circuit, with the timing characteristics of the flip-flops and combinational blocks annotated. Assume that the muxes have no propagation delay, and that their inputs have been stabilized.



Part a)

Assuming no clock skew and no clock jitter, what is the minimum clock period of this design? Show your work.

Part b)

If this design runs at 1GHz, does it face any timing violations? If so, list them and explain.

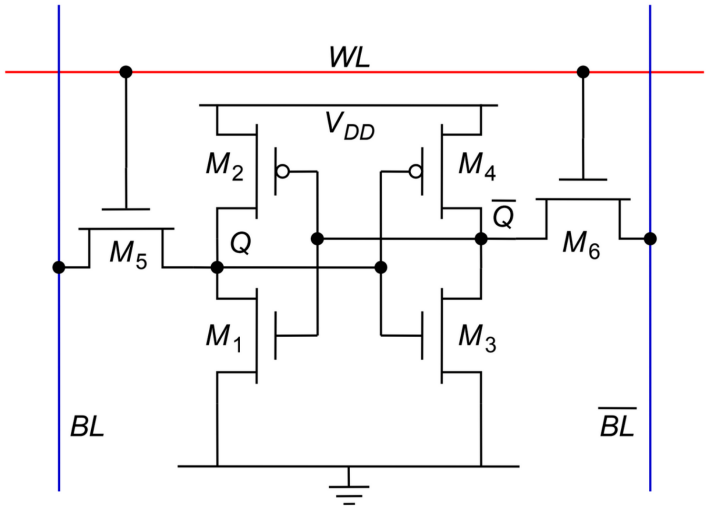
Part c)

You may now adjust the clock skew of the design. What is the clock skew that minimizes the clock minimum clock period while avoiding timing violations? What is the new minimum clock period? Show your work.

Problem 2: S(uper)RAM Design

Part a)

Consider the 6T SRAM design below. Assume that the SRAM operates at 1V, and that $V_{TH_N} = |V_{TH_P}| = 0.2V$.

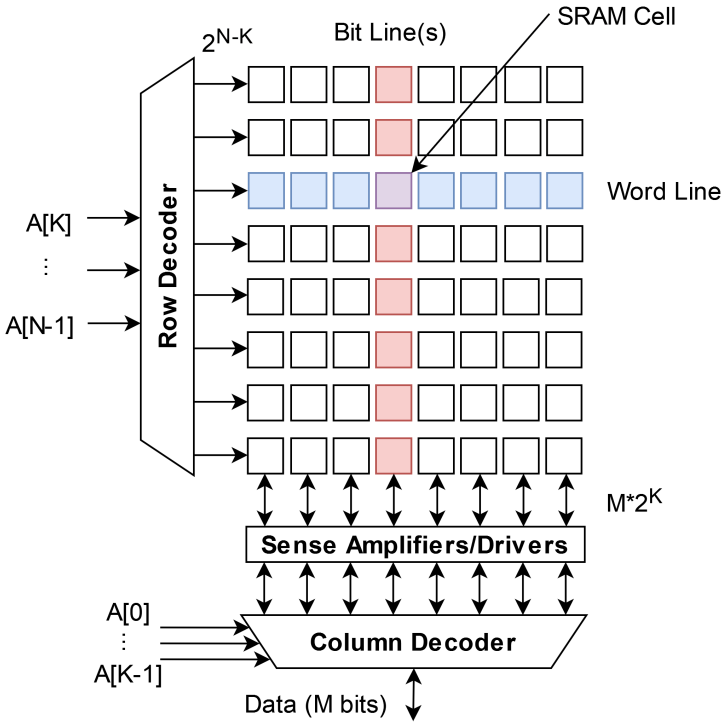


i) You want to ensure that this SRAM can do non-destructive reads. Assuming you are reading a value of $Q = 1$, list any constraints on the relative sizes of transistors in this design.

ii) You want to ensure that this SRAM is writable. If you are writing a value of $Q = 0$, list any constraints on the relative sizes of transistors in this design.

Part b)

You are tasked with designing a single-ported 128-bit wide word-addressable (128 bit words) SRAM with a capacity of 32KiB (32× 1024 Bytes). Consider the diagram below for reference.



i) How many address bits are needed for this SRAM?

ii) Assume you want the SRAM cells to be arranged to have a 1:2 aspect ratio (that is, twice as many columns as rows). How many address bits are used for the row decoder? What about the column decoder? Show your work.

Problem 3: Love $$$

Part a)

You are given several options for implementing a 32KB cache, and decide to explore the effect of cache associativity on performance. Rank each of the following designs (ranking the best performing as 1st) for each of the metrics listed below. If equivalent, give the same ranking.

Cache Parameter	**Direct Mapped**	**4-way set associative**	**Fully Associative**
Hit rate			
Hit time			
Tag check hardware complexity			
Cache placement flexibility			
Cache replacement policy flexibility			

Part b)

Calculate the number of bits in the offset, index, and tag fields for each of the following caches:

i) 32KB, direct mapped, 1KB block size, 32 bit words

ii) 1MB, 8-way set-associative, 4KB block size, 64 bit words

iii) 8KB, fully associative, 512B block size, 8 bit words