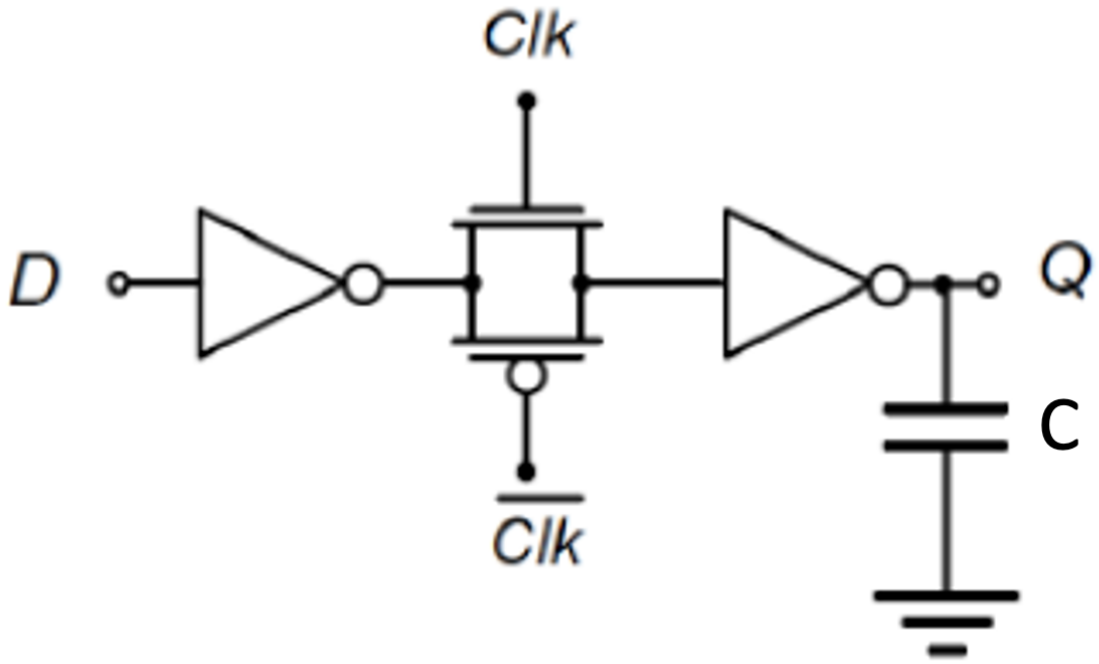
Homework 9

Due: 11/15/21 11:59pm

Problem 1: Latch Design

For this question, we will look into the latch design shown below. You may assume that the inverters are symmetrical with input capacitance C, self-loading capacitance also equal to C, and equivalent driving resistance R. Assume ideal VTCs for the inverters such that any tiny voltage above or below VDD/2 flips its output. The transmission gate is sized to have an equivalent resistance R and parasitic capacitance C on each side.



a) Calculate the Clk-Q delay as a function of R and C of this latch. (hint: draw the equivalent RC circuit). If R is 10kohm and C is 10pF, what is the total clk-Q delay?

_____ μs (round to tenth).

b) Calculate the D-Q delay as a function of R and C of this latch. (hint: draw the equivalent RC circuit). If R is 10kohm and C is 10pF, what is the total D-Q delay?

_____ μs (round to tenth).

c) What is the approximate setup time for this latch given R is 10kohm and C is 10pF?

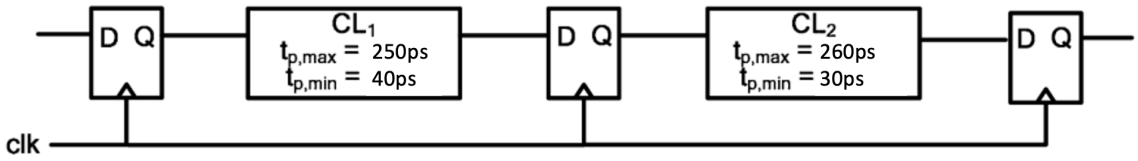
_____ μs (round to tenth).

d) What is the approximate hold time for this latch given R is 10kohm and C is 10pF?

_____ μs (round to tenth).

Problem 2: Timing and clock distribution

In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: t_{clk-q} = 40ps, t_{setup} = 35ps, and t_{hold} = 20ps. You can assume that the clock has no jitter.



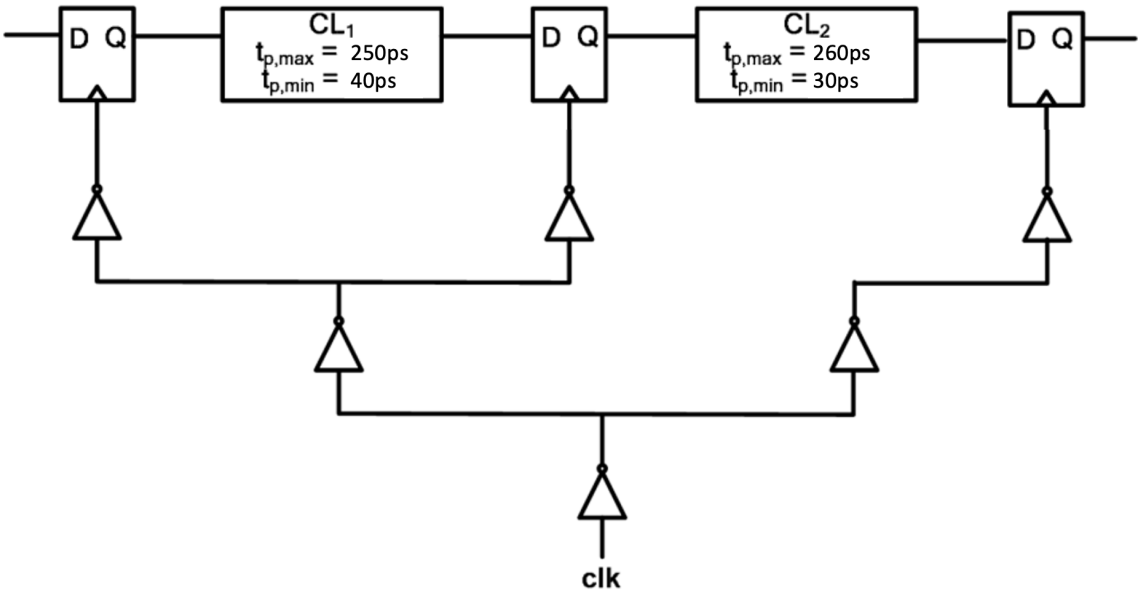
a) What is the minimum clock cycle time for this pipeline?

_____ ps

b) Are there any minimum delay violations (yes/no)?

_____

c) Now we include the clock distribution network for this pipeline. Assuming that the delay of each inverter is nominally 40ps, but that each inverter's delay varies randomly by +/- 15%, now what is the minimum clock cycle time?



_____ ps

d) Under these same conditions (i.e., 40ps nominal inverter delay, +/-15% delay variation), can this pipeline fail any minimum delay constraints (yes/no)?

_____