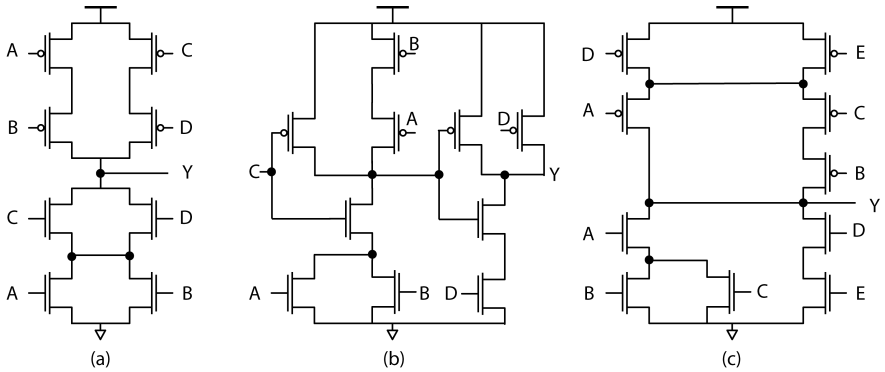
# EECS 151/251A Homework 5

Due 11:59pm Friday, October 15th, 2021

## 1 Complementary CMOS

Choose the simplified boolean expression for the function described by the CMOS circuit below.




**(a)**

A) $\overline{(A+B)(C+D)}$

B) $\overline{(AB+CD)}$

C) $\overline{(AC+DB)}$

D) $\overline{(A+C)(D+B)}$

**(b)**

A) $\overline{(C+AB)D}$

B) $C(A+B)+\overline{D}$

C) $\overline{\overline{C(A+B)}+D}$

D) $(C+AB)\overline{D}$

**(c)**

A) $\overline{A(B+C)+DE}$

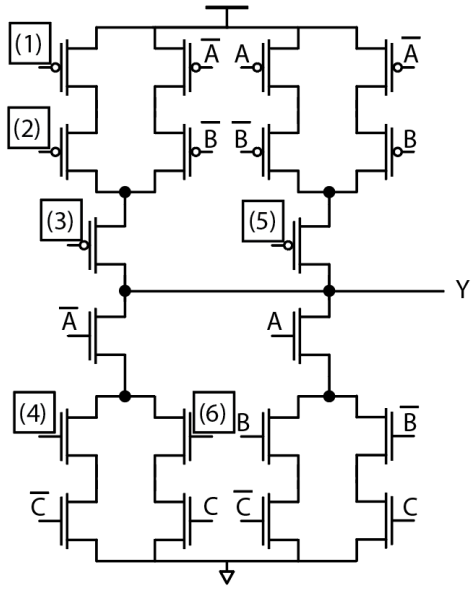
B) $(D+\overline{E})(\overline{A}+\overline{BC})$

C) $\overline{(D+E)(A+BC)}$

D) $(\overline{A}(\overline{B}+\overline{C})+\overline{DE})$

## 2 XOR

**(a)** Below is a CMOS implementation of a 3-input XOR gate. Complete the circuit by filling in the signal name in the boxes.




| 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|

A)

| A | B | C | $\overline{B}$ | $\overline{C}$ | B |
|---|---|---|---|---|---|

B)

| A | B | $\overline{C}$ | $\overline{B}$ | C | B |
|---|---|---|---|---|---|

C)

| A | B | C | B | $\overline{C}$ | $\overline{B}$ |
|---|---|---|---|---|---|

D)

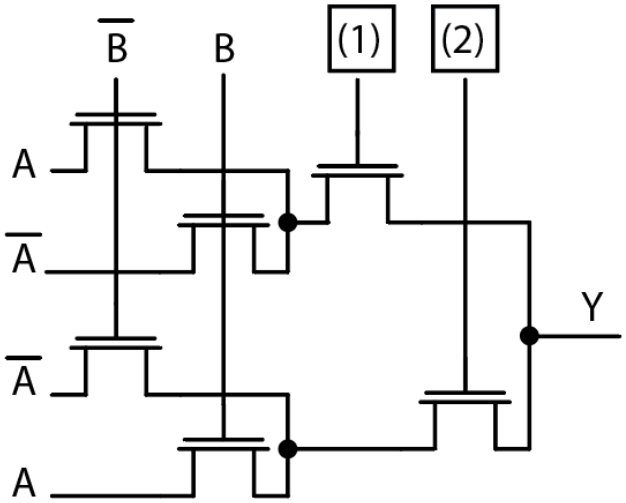
| A | B | $\overline{C}$ | B | C | $\overline{B}$ |
|---|---|---|---|---|---|

| |
|---|

**(b)** Is the gate shown above a complementary CMOS gate?

| |
|---|

**(c)** Below is a passgate logic implementation of a 3 input XOR gate. Choose the signals that connect to the second stage NMOS gates.




| 1 | 2 |
|---|---|

A)

| C | $\overline{C}$ |
|---|---|

B)

| $\overline{C}$ | C |
|---|---|

C)

| C | C |
|---|---|

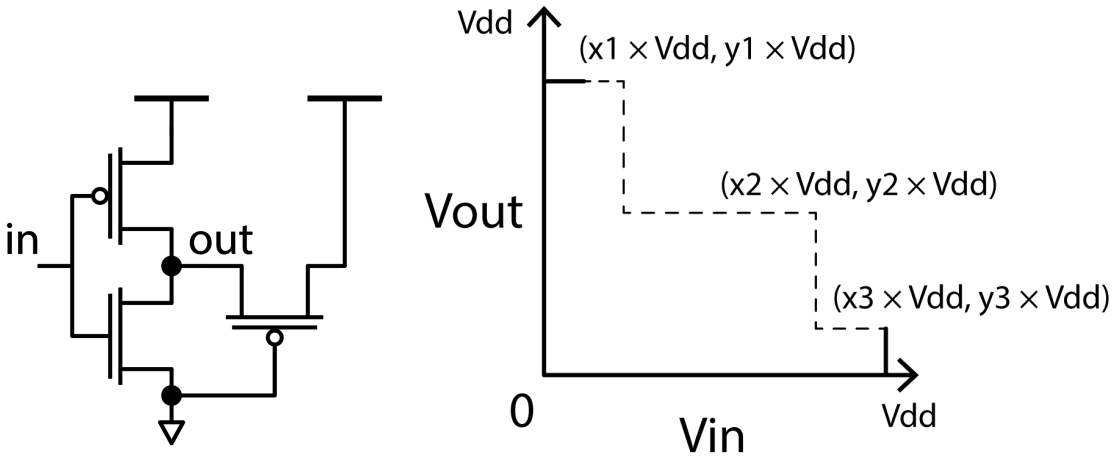
D)

| $\overline{C}$ | $\overline{C}$ |
|---|---|

| |
|---|

## 3 Voltage Transfer Characteristic (VTC)

Using the transistor-as-a-switch model, write transition points in the voltage transfer characteristic for the circuit below. You will eventually recognize this as half of a 6T CMOS SRAM bit-cell. Assume that $|V_{th,p}| = V_{th,n} = V_{DD}/4$ and that $R_{on,p} = R_{on,n}$. For example, if the transition point is $(\frac{1}{2}V_{dd}, \frac{1}{3}V_{dd})$, write $\frac{1}{2}, \frac{1}{3}$ in the boxes. If there is only one or two transition points in the middle of the VTC, write $0, 0$ in the boxes.




(x1,y1)

| | |
|---|---|
| | |

(x2,y2)

| | |
|---|---|
| | |

(x3,y3)

| | |
|---|---|
| | |