EECS 151/251A SP2022 Discussion 6

GSI: DIMA NIKIFOROV, YIKUAN CHEN

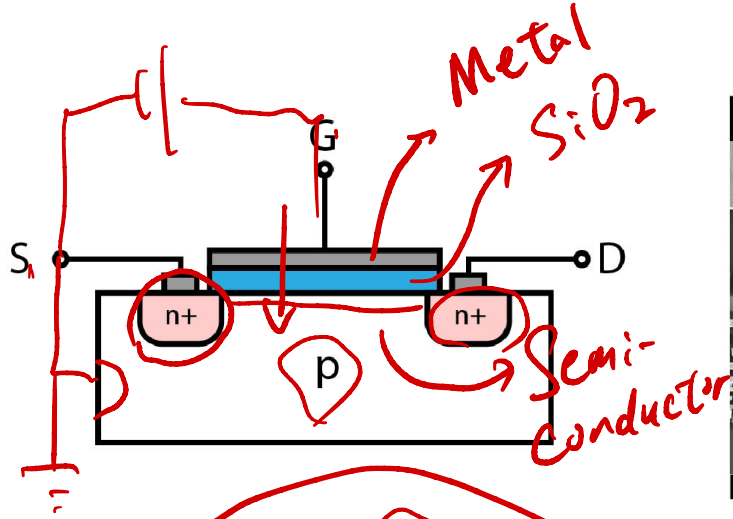
Agenda

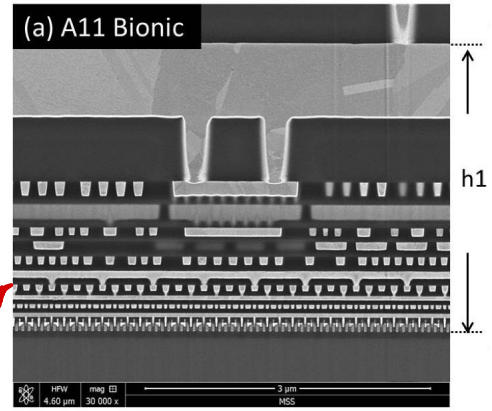
- MOS
- CMOS
- Inverters/Inverter Chain

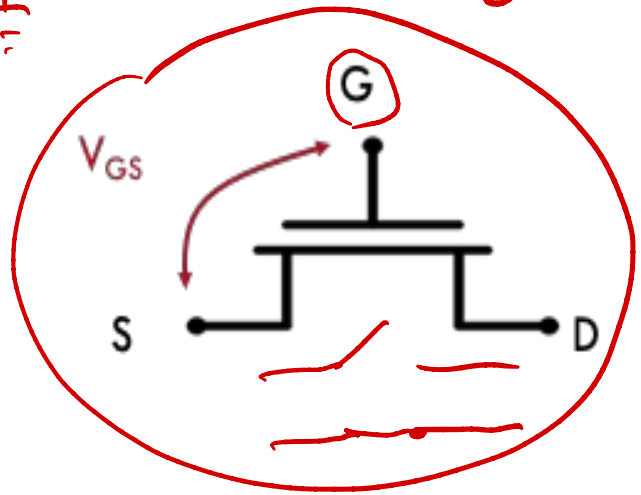
MOS

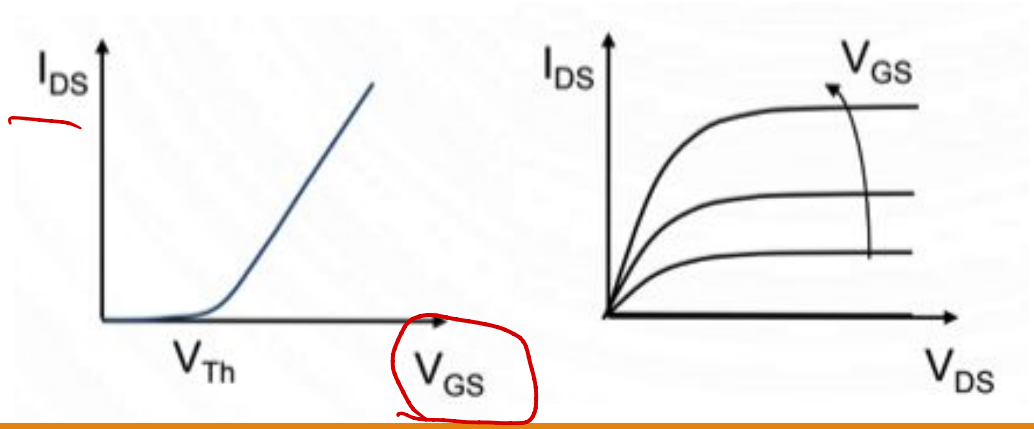
Metal Oxide Semiconductor (MOS) Transistors

- Used to be made in a planar process
  - Wafer is usually p-doped
  - 3 main contacts
    - Gate
    - Source
    - Drain
  - Gate controls current flow from Source to Drain



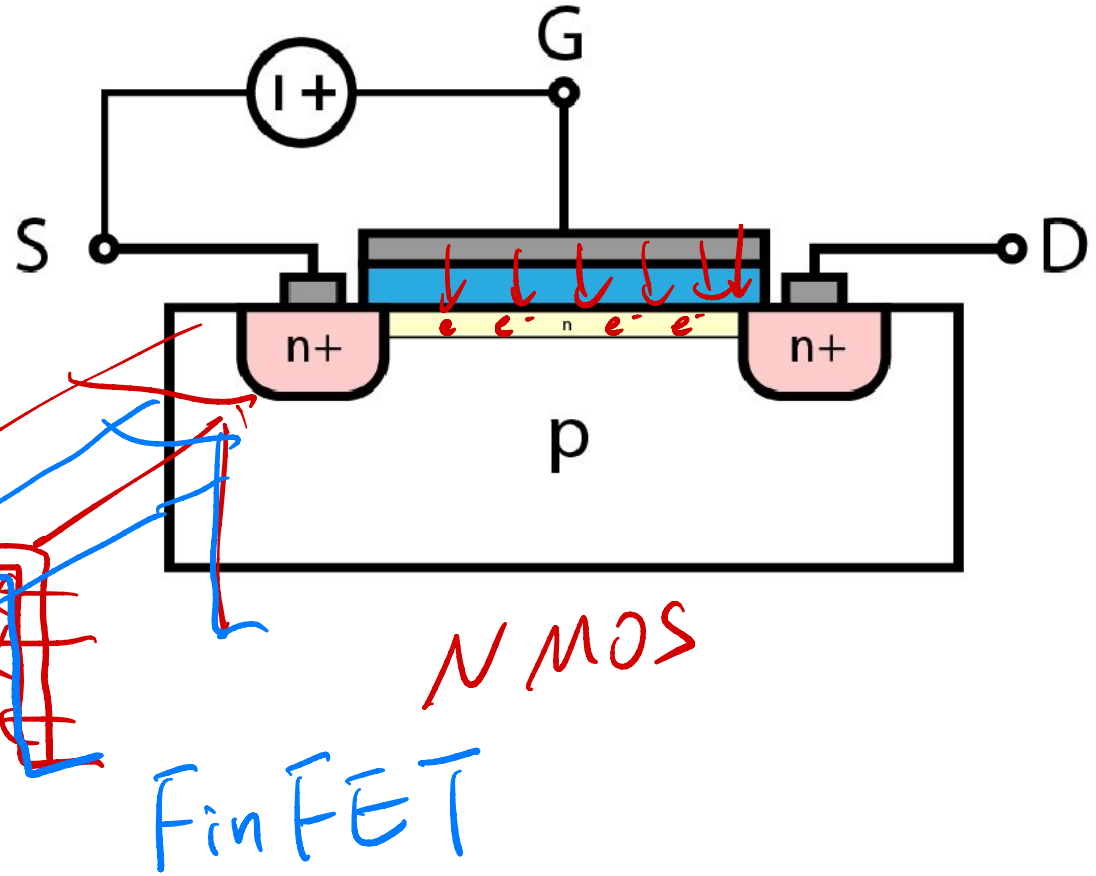






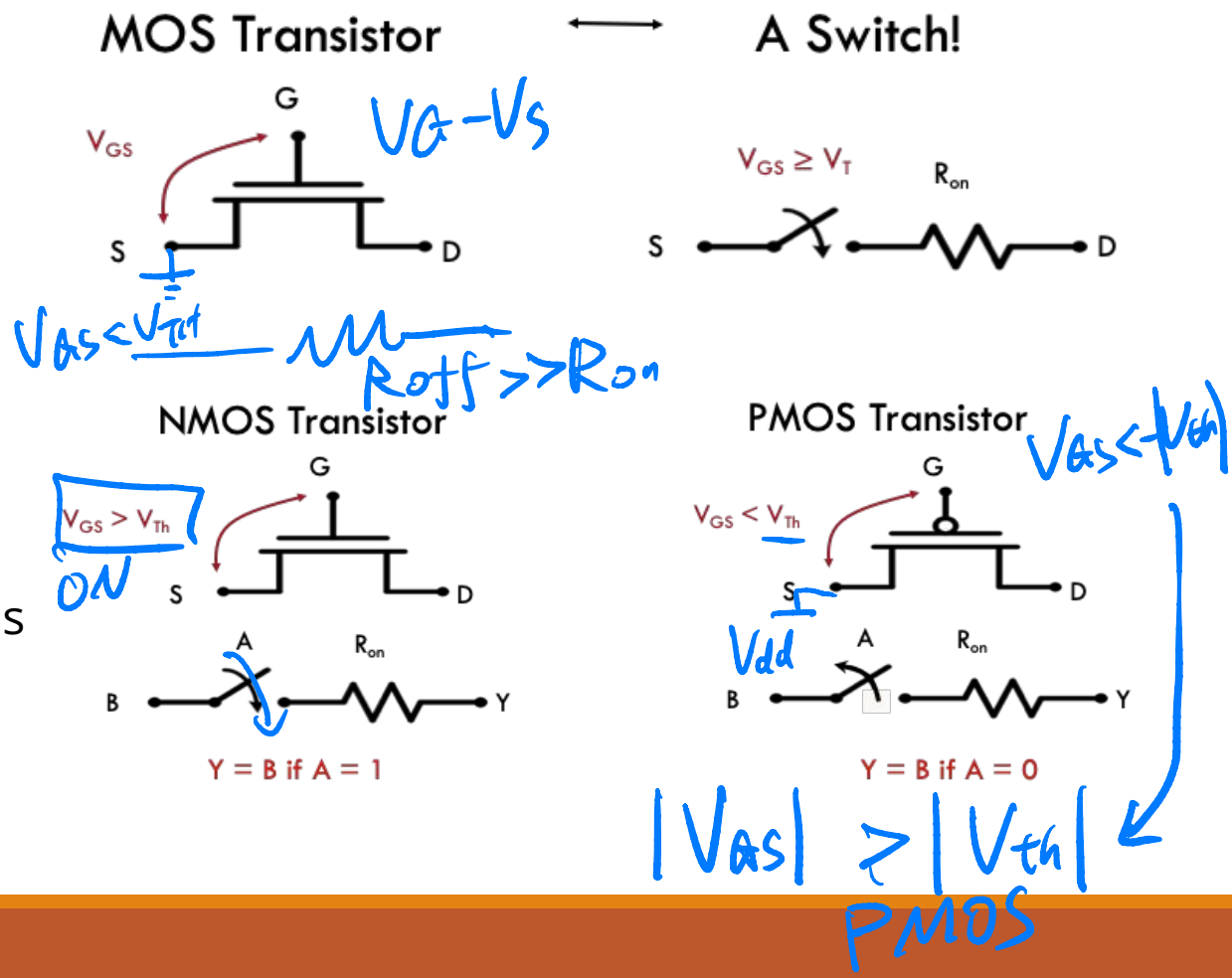
Metal Oxide Semiconductor (MOS) Transistors

- MOS turns “on” when voltage applied across gate-source
- Voltage causes top layer of silicon to invert types, connecting S to D

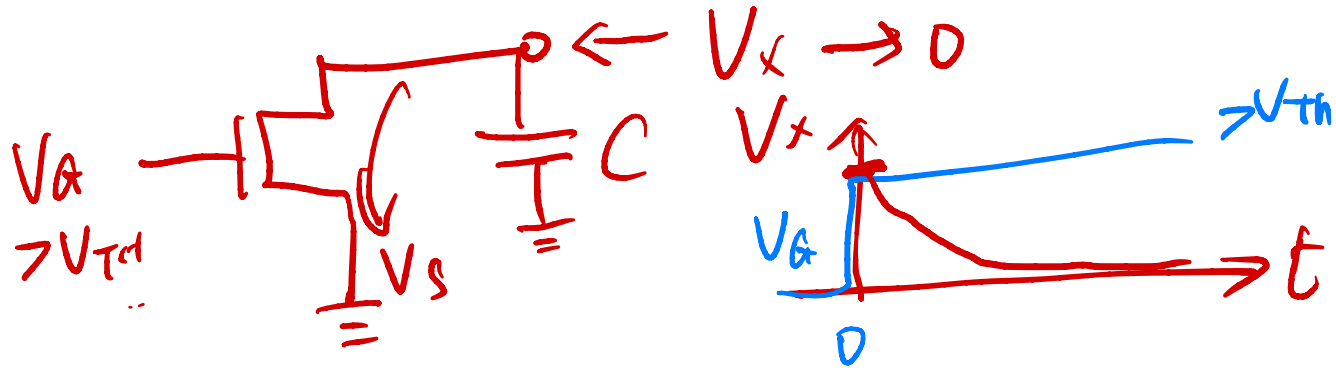


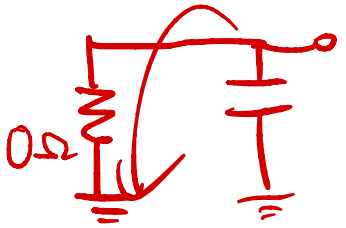
Metal Oxide Semiconductor (MOS) Transistors

- MOS transistors are non-ideal switches
  - $0 < R_{ON} << R_{OFF} < \infty$
- NMOS
  - The *source* of NMOS always at *lower* voltage
  - Ideal for passing *low* voltage (0, gnd)
- PMOS
  - The *source* of PMOS always at *higher* voltage
  - Ideal for passing high voltage (1, vdd)
- The 'effective' source node can change depending on the voltage at the MOS' terminals

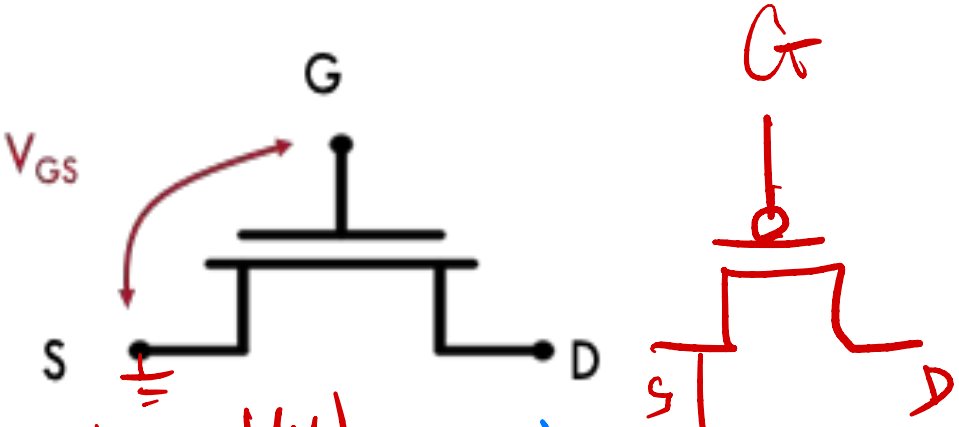


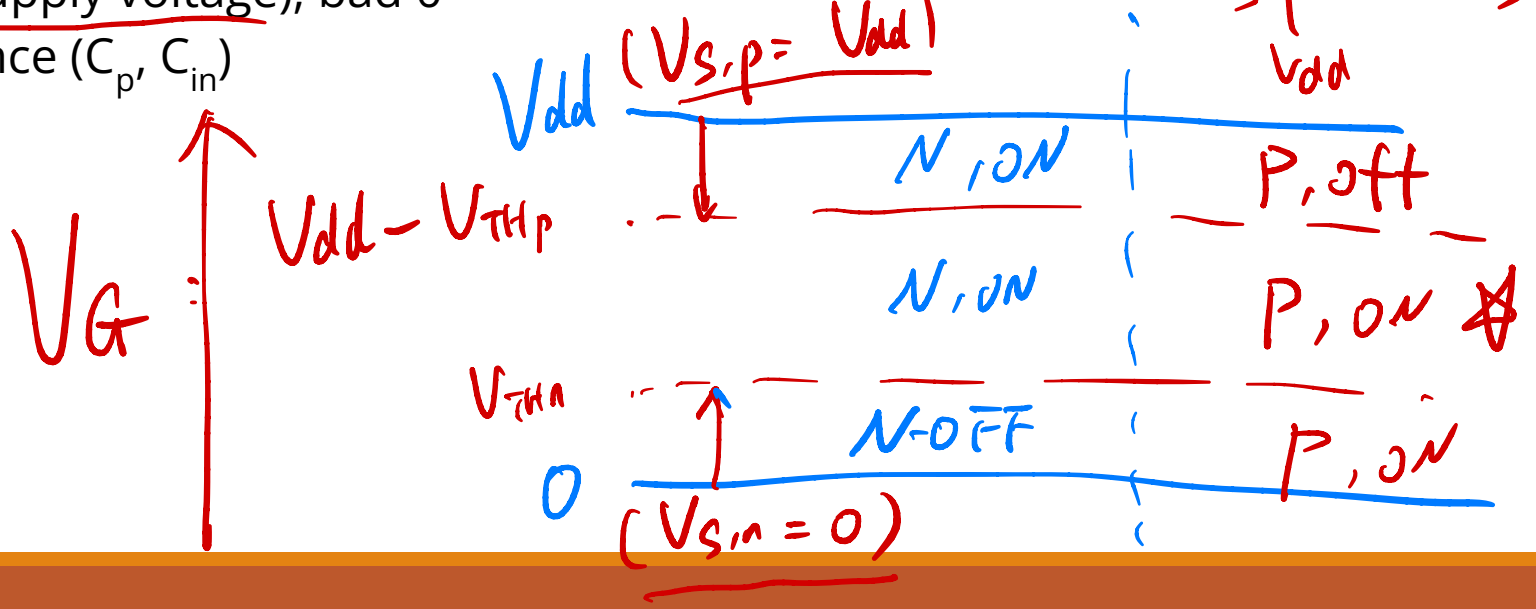
MOS

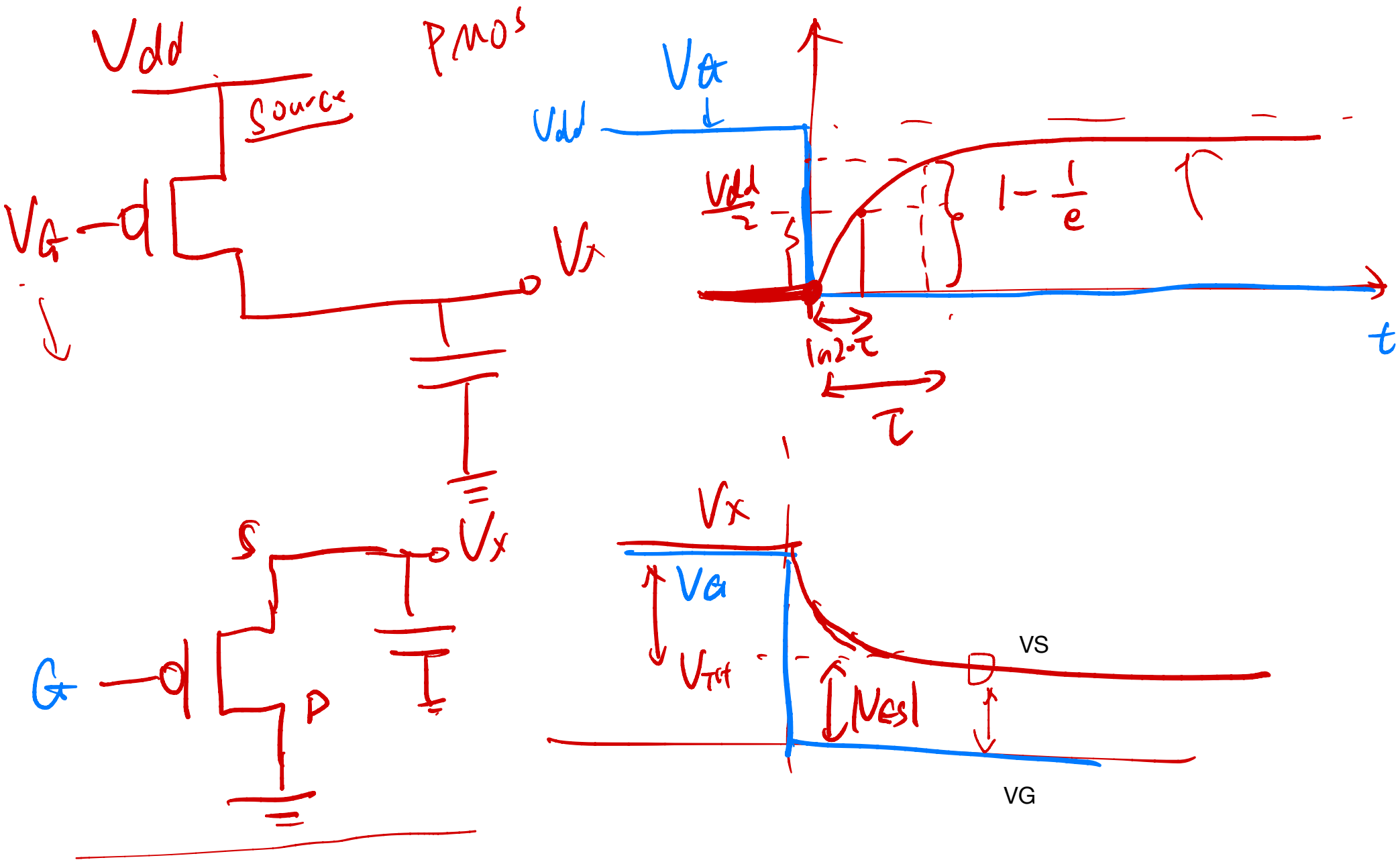




- In this class, you only need to know:
  - MOS switch model
  - On-resistance is proportional to Length/Width
  - Difference of NMOS/PMOS
  - NMOS: good for passing 0 (grounding), bad 1
  - PMOS: good for passing 1 (supply voltage), bad 0
  - Simplified parasitic capacitance (C_p, C_{in})





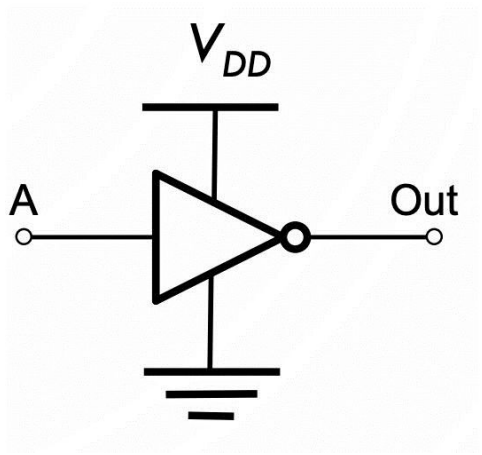


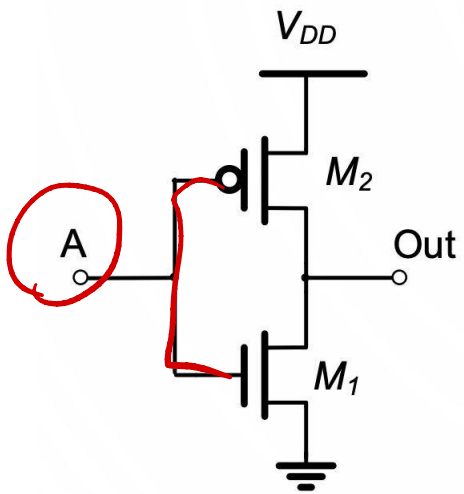
|VG-VS| > |VTH| —> channel forms, charge can flow

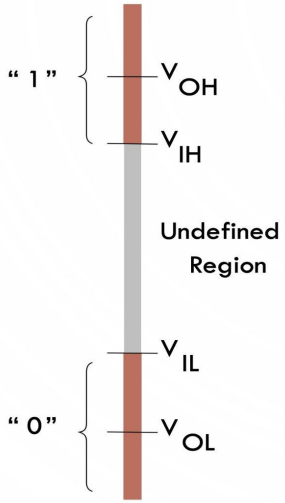
CMOS

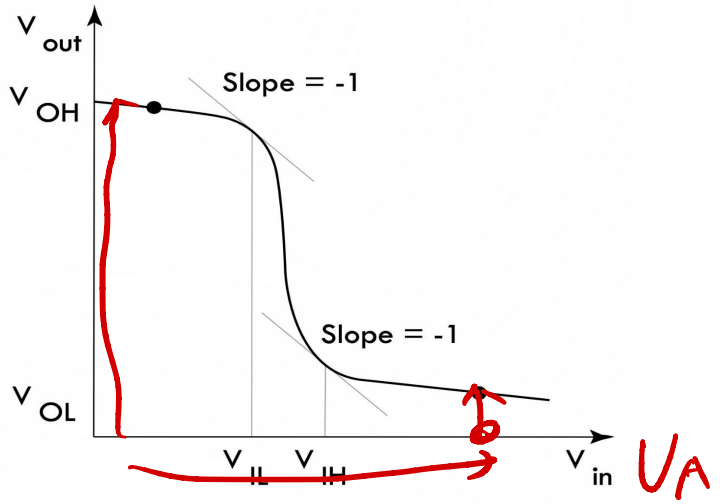
CMOS Inverter

- Complementary Metal Oxide Semiconductor
  - Inverter has 1 NMOS and 1 PMOS
- NMOS and PMOS each have an “on” and “off” resistance
- Voltage Transfer Curve (VTC)
  - Mid/switching-point is a function of PMOS vs NMOS strength

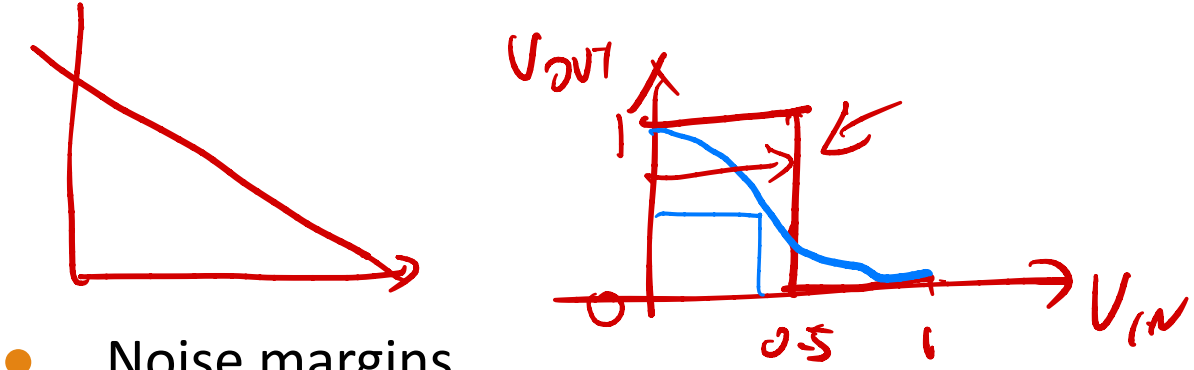




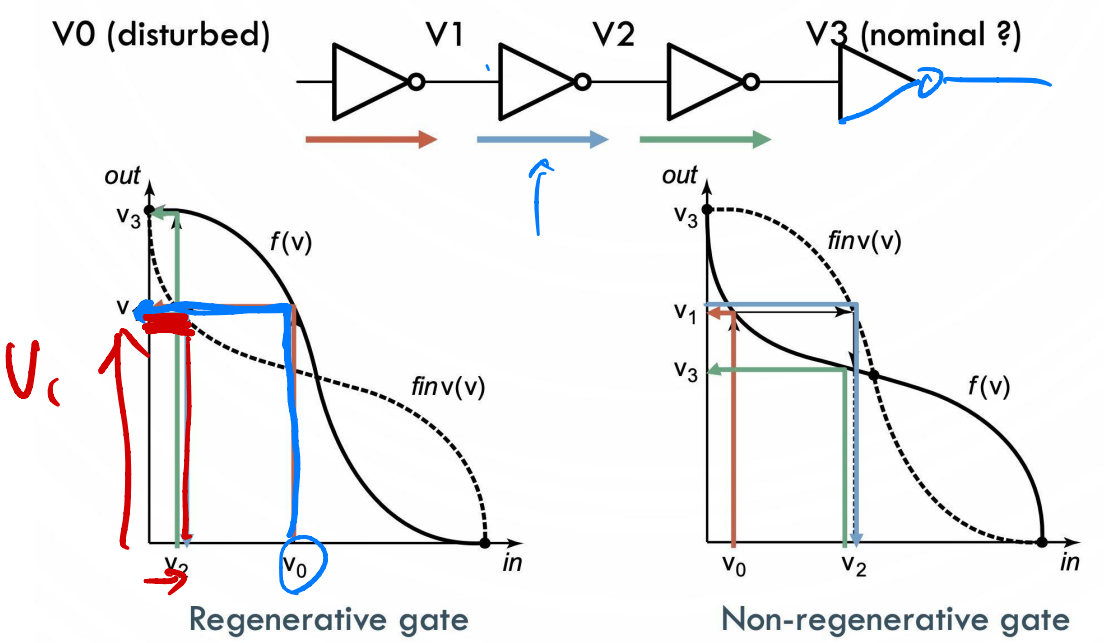




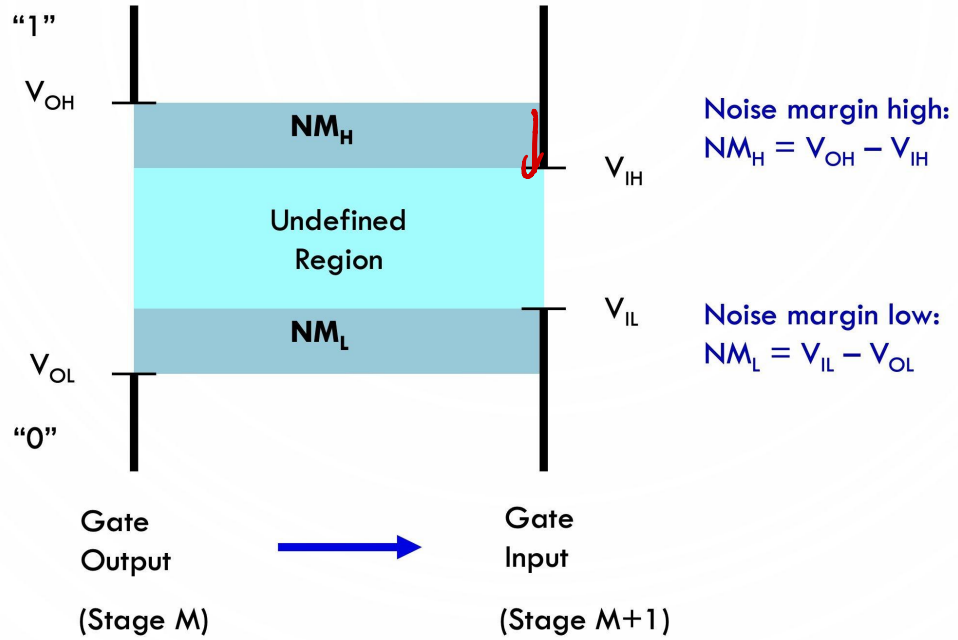
CMOS Margins



- Noisy, but still want 1s and 0s (digital)
  - "Restoration" / "regeneration" property



- Noise margins
  - The amount of noise that can be tolerated such that the signal can be correctly interpreted by the next gate
  - Eg. in a chain of inverters



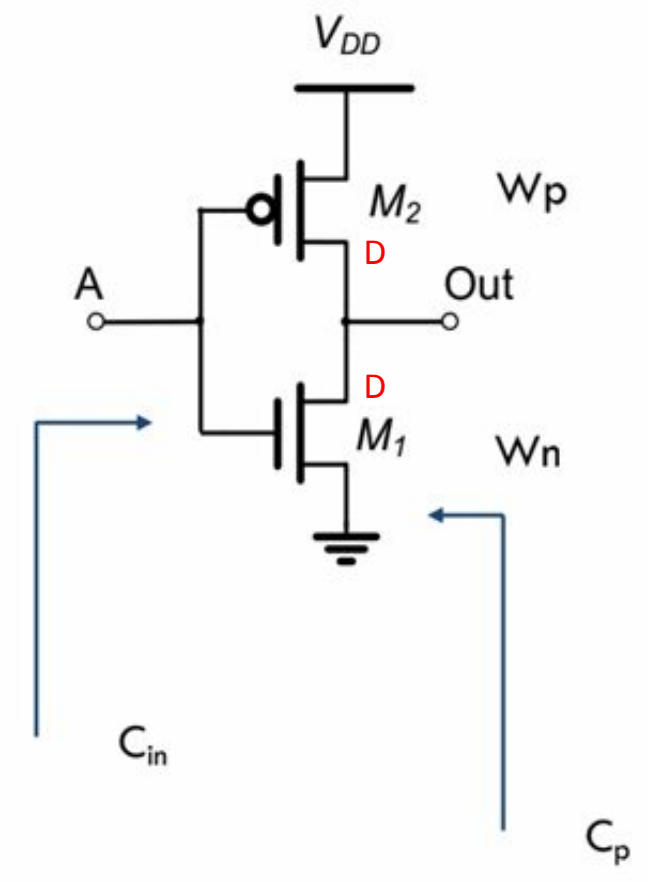
CMOS Exercise

- Implement a NAND gate in CMOS:

CMOS Inverters

Impact of Inverter Sizing

$\tau \propto R \cdot C$



- $C_{in} \propto WL$, $C_p \propto W$
  - C_{in} dominated by $C_{g,pmos} + C_{g,nmos}$
  - $C_p = \gamma C_{in}$. C_p is dominated by $C_{d,pmos} + C_{d,nmos}$. $\gamma \approx 1$.
- $R_{eq} \propto L/W$ $\quad R = \rho \cdot \frac{L}{A}$
- Inverter usually sized for $t_{p,LH} = t_{p,HL}$

$$\frac{R_{on,p} \cdot C = R_{on,n} \cdot C}{L}$$

$$R_p = R_n$$

$$\rho_p \cdot \frac{L_p}{W_p \cdot t} = \rho_n \cdot \frac{L_n}{W_n \cdot t}$$

$$\frac{W_p}{W_n} = \frac{\rho_n}{\rho_p}$$

  - How is $W_p : W_n$ a function of $\rho_p : \rho_n$?
- How does the RC delay change if:
  - Either W_p or W_n doubled?
  - Both W_p and W_n doubled?

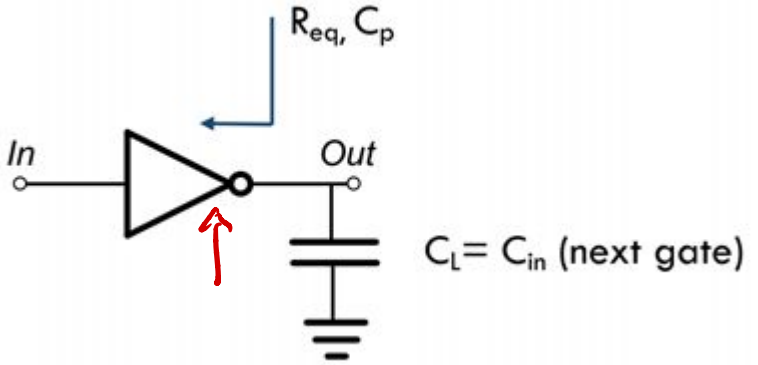
$\tau = R_{eq} \cdot C$

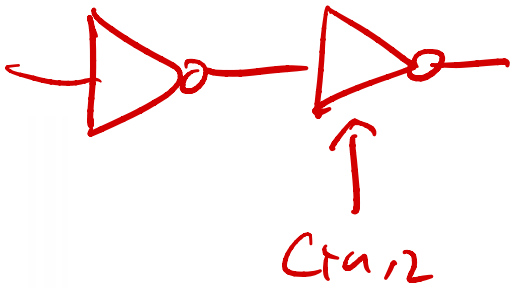
Loaded Inverter Delay

intrinsic Cap

$$t_{p,inv} = ln2 \cdot R_{eq}\left(C_{p,tot} + C_L\right)$$
$$= ln2 \cdot R_{eq} C_{p,tot}\left(1 + \frac{C_L}{C_{p,tot}}\right)$$
$$= ln2 \cdot R_{eq} C_{p,tot}\left(1 + \frac{C_L}{\gamma C_{in}}\right)$$
$$= ln2 \cdot R_{eq} C_{p,tot}\left(1 + \frac{f}{\gamma}\right)$$
$$= ln2 \cdot \tau_{inv}\left(1 + \frac{f}{\gamma}\right)$$

$C_p = C_{in} \cdot \gamma$

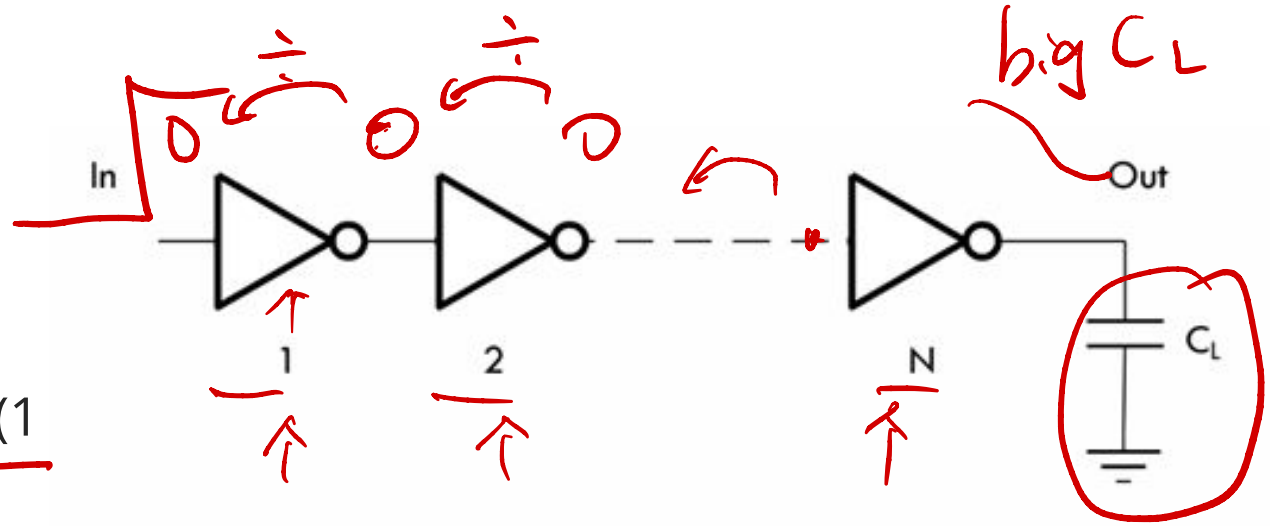




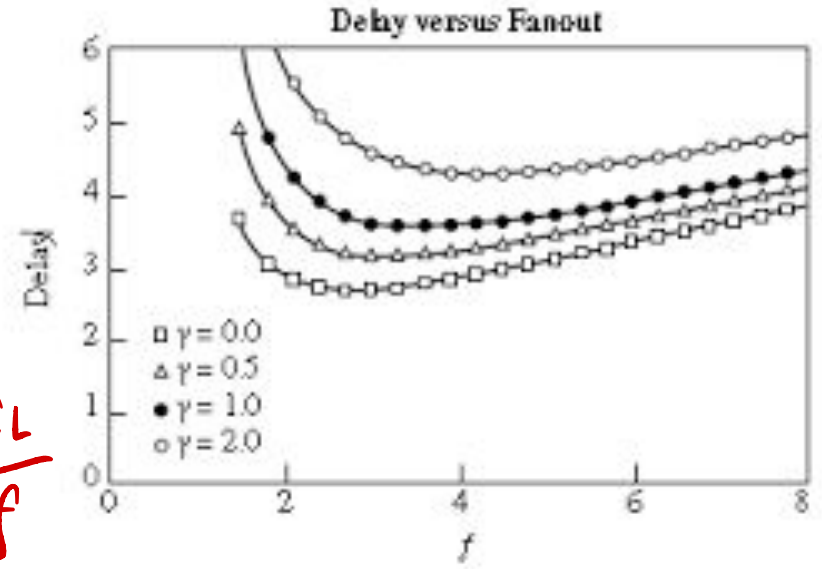
$= C_{L,1}$

- Intrinsic vs. Extrinsic delay
  - Intrinsic τ_{inv} independent of sizing
- Fanout **f = C_L/C_{in}**
- Generalizable to any CMOS gate

Inverter Chain Sizing



- Goal: minimize path delay
  - Assume 1st inverter has unit size ($C_{in,1} = 1$)
- Path delay $D = t_{p1} + \ldots + t_{pN} = (1 + f_1) + \ldots + (1 + f_N)$
- Path fanout $F = C_L / C_{in}$
- Solution
  - Take partial derivatives w.r.t $C_2, \ldots, C_N$
  - Get $f_1 = f_2 = \ldots = f_N$
  - Min. path delay = $Nf + N = N\sqrt[N]{F} + N$
  - Size backwards



Questions?