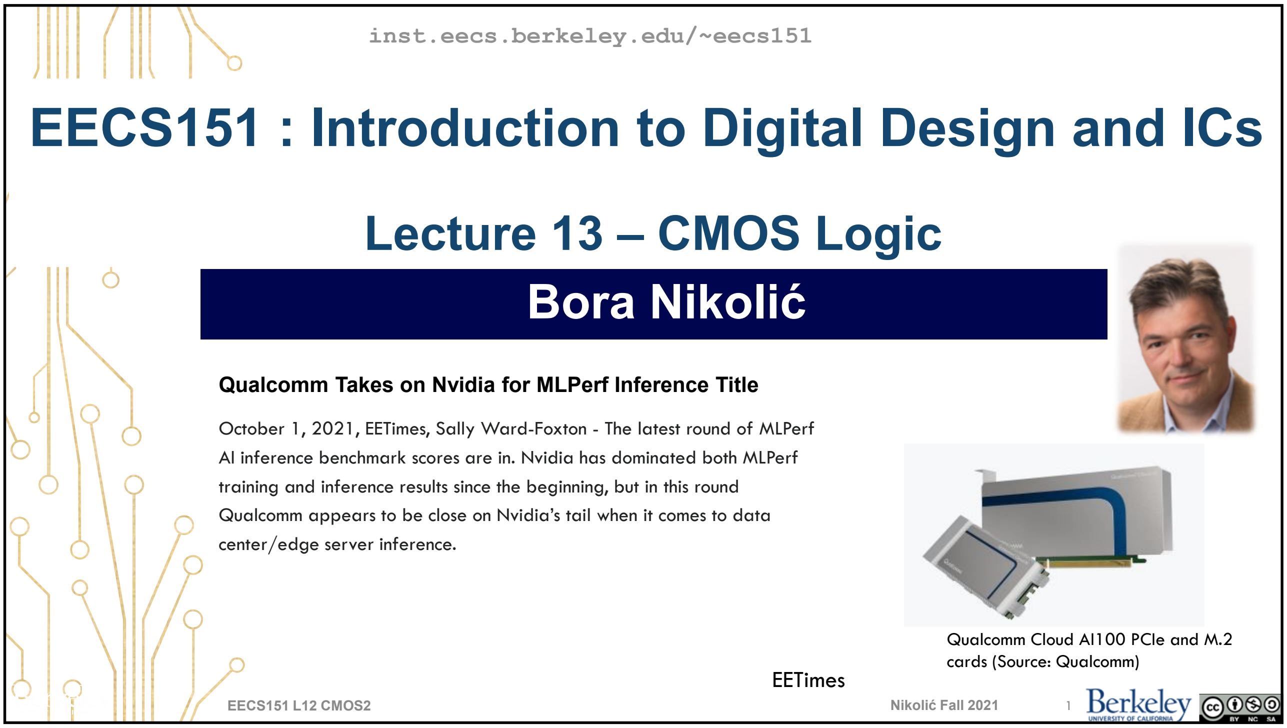

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EECS151 : Introduction to Digital Design and ICs

Lecture 13 – CMOS Logic

Bora Nikolić

Qualcomm Takes on Nvidia for MLPerf Inference Title

October 1, 2021, EETimes, Sally Ward-Foxton - The latest round of MLPerf AI inference benchmark scores are in. Nvidia has dominated both MLPerf training and inference results since the beginning, but in this round Qualcomm appears to be close on Nvidia's tail when it comes to data center/edge server inference.

Qualcomm Cloud AI100 PCIe and M.2 cards (Source: Qualcomm)

EETimes

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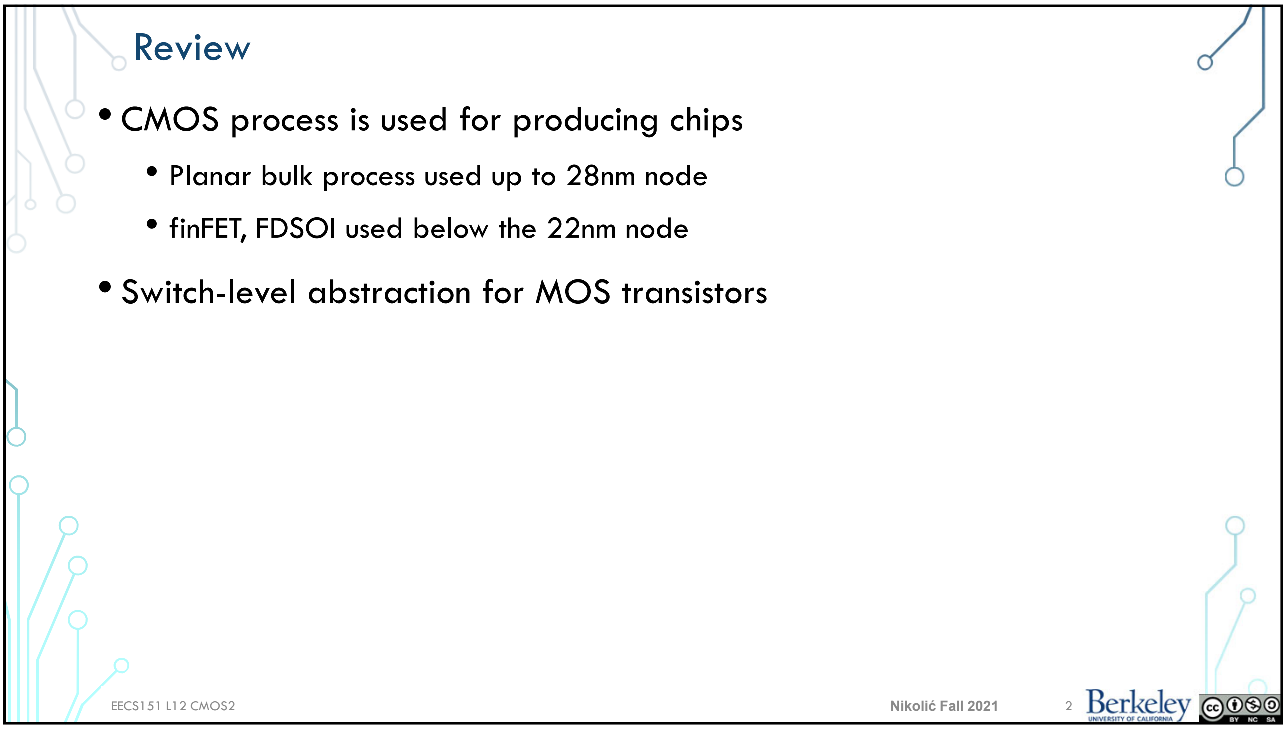

Review

- CMOS process is used for producing chips
  - Planar bulk process used up to 28nm node
  - finFET, FDSOI used below the 22nm node
- Switch-level abstraction for MOS transistors

2

MOS Switch

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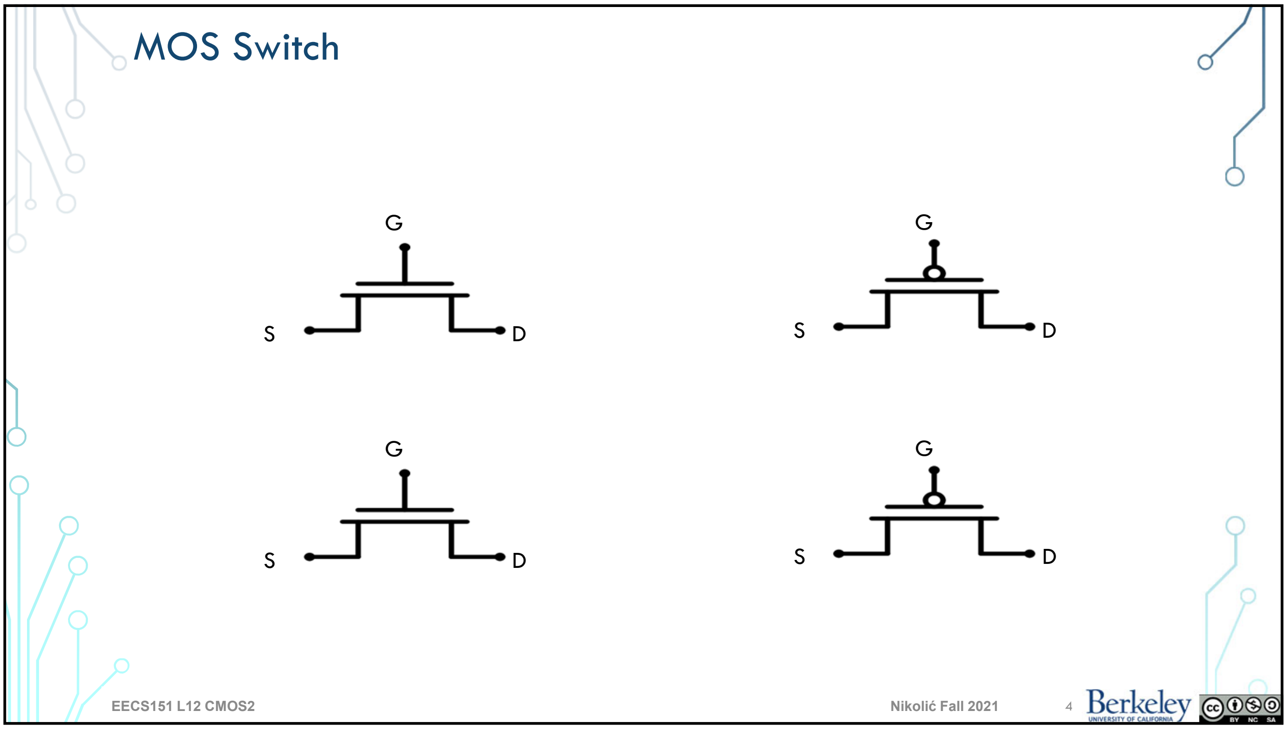

MOS Switch

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CMOS Inverter

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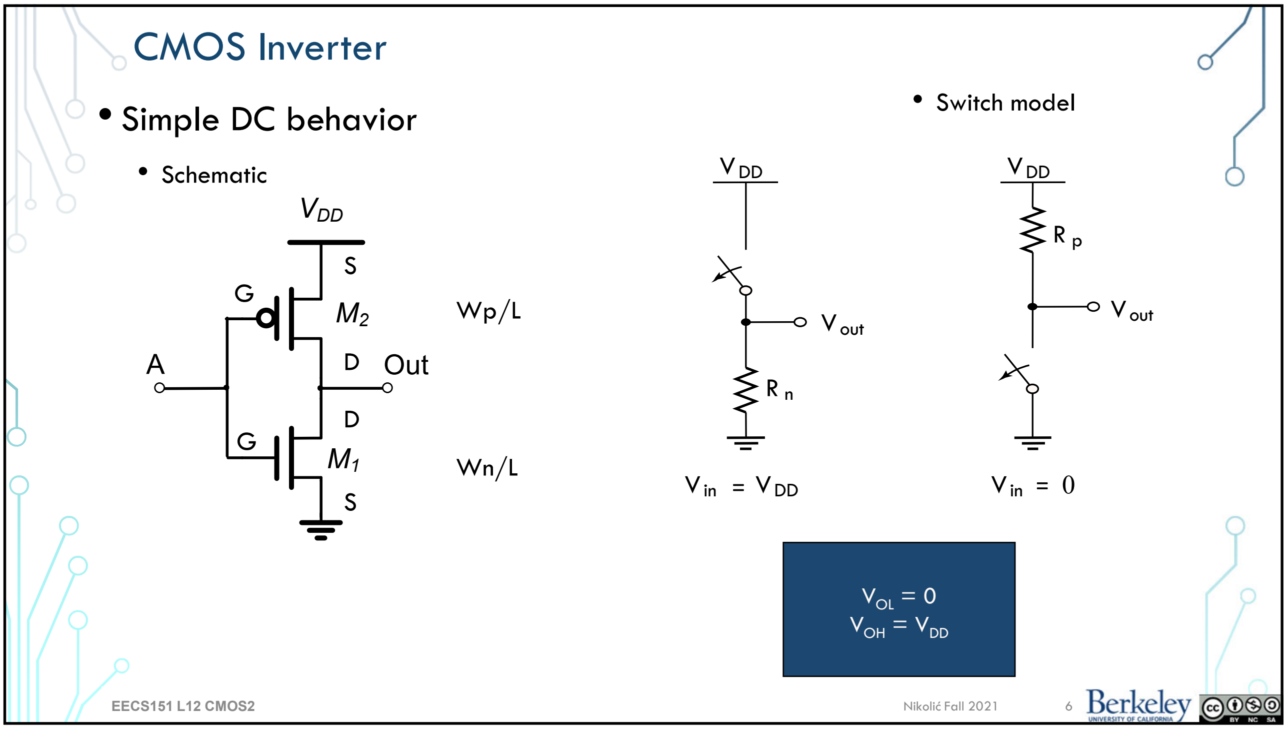

CMOS Inverter

- Simple DC behavior
  - Schematic

- Switch model

$V_{OL} = 0$
$V_{OH} = V_{DD}$

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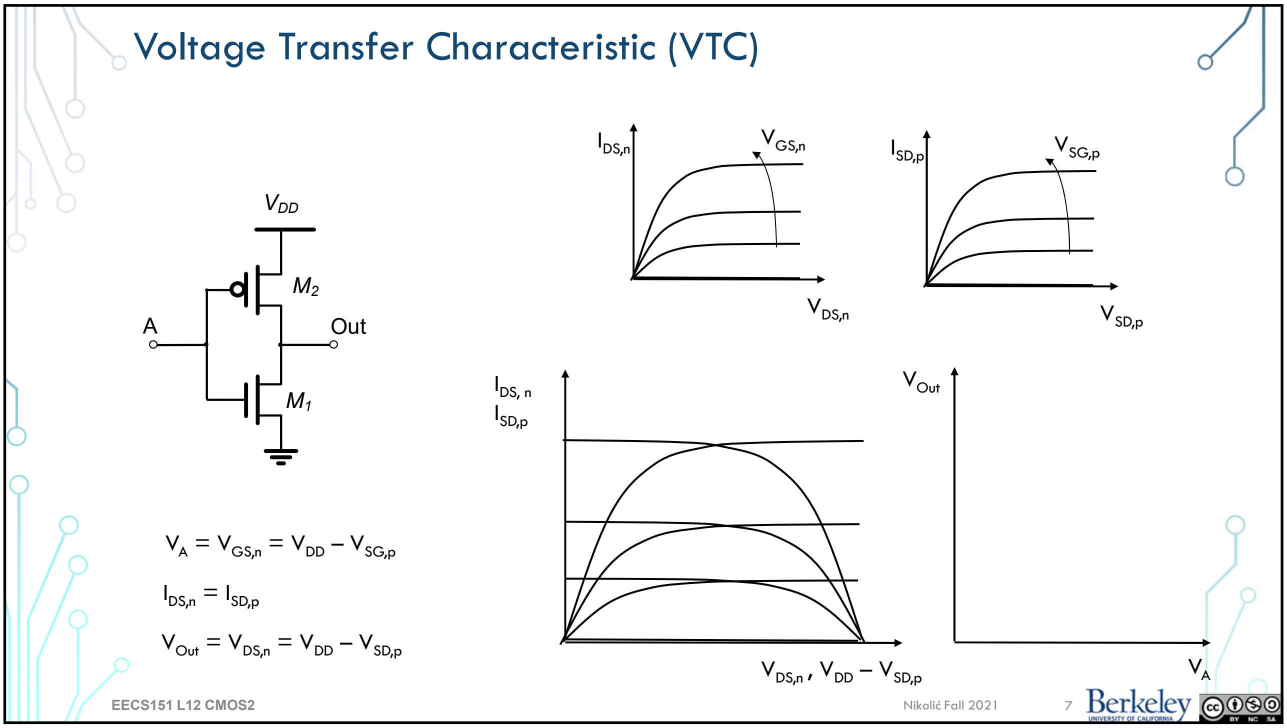
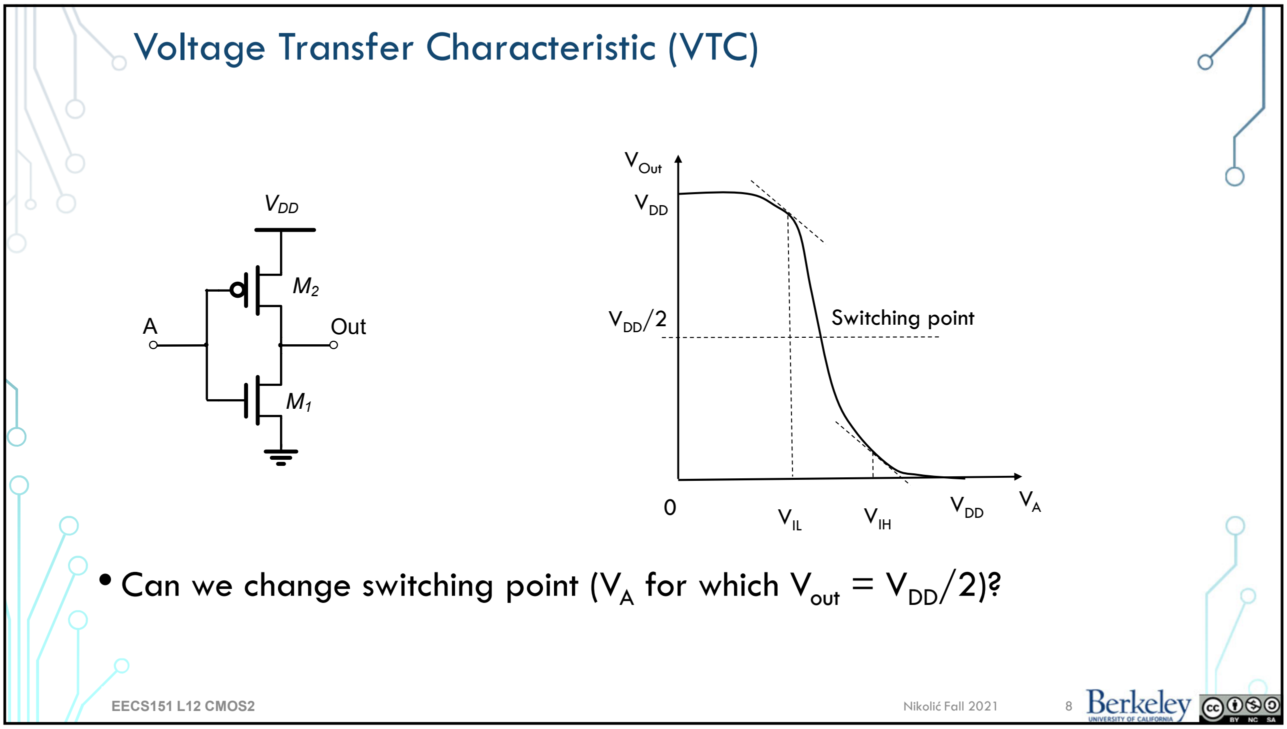


Voltage Transfer Characteristic (VTC)

$V_A = V_{GS,n} = V_{DD} - V_{SG,p}$

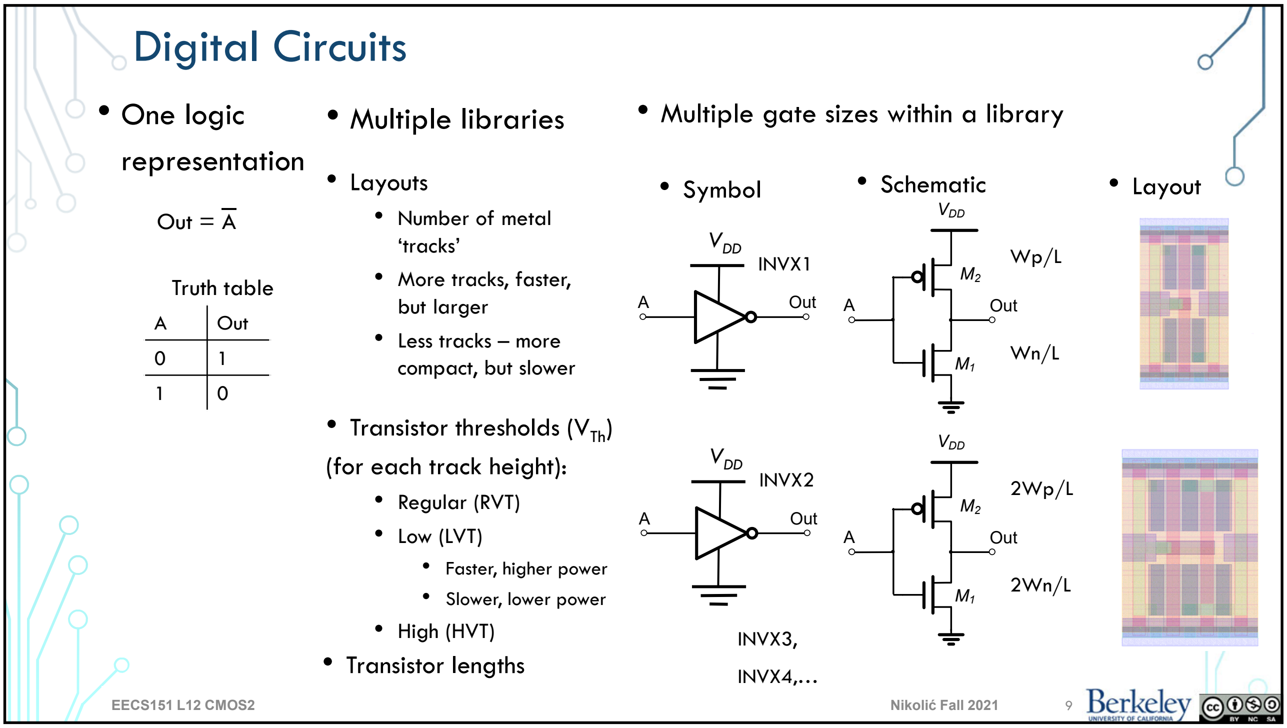
$I_{DS,n} = I_{SD,p}$

$V_{Out} = V_{DS,n} = V_{DD} - V_{SD,p}$



Voltage Transfer Characteristic (VTC)

- Can we change switching point (V_A for which $V_{out} = V_{DD}/2$)?



Digital Circuits

- One logic representation

  Out = $\overline{A}$

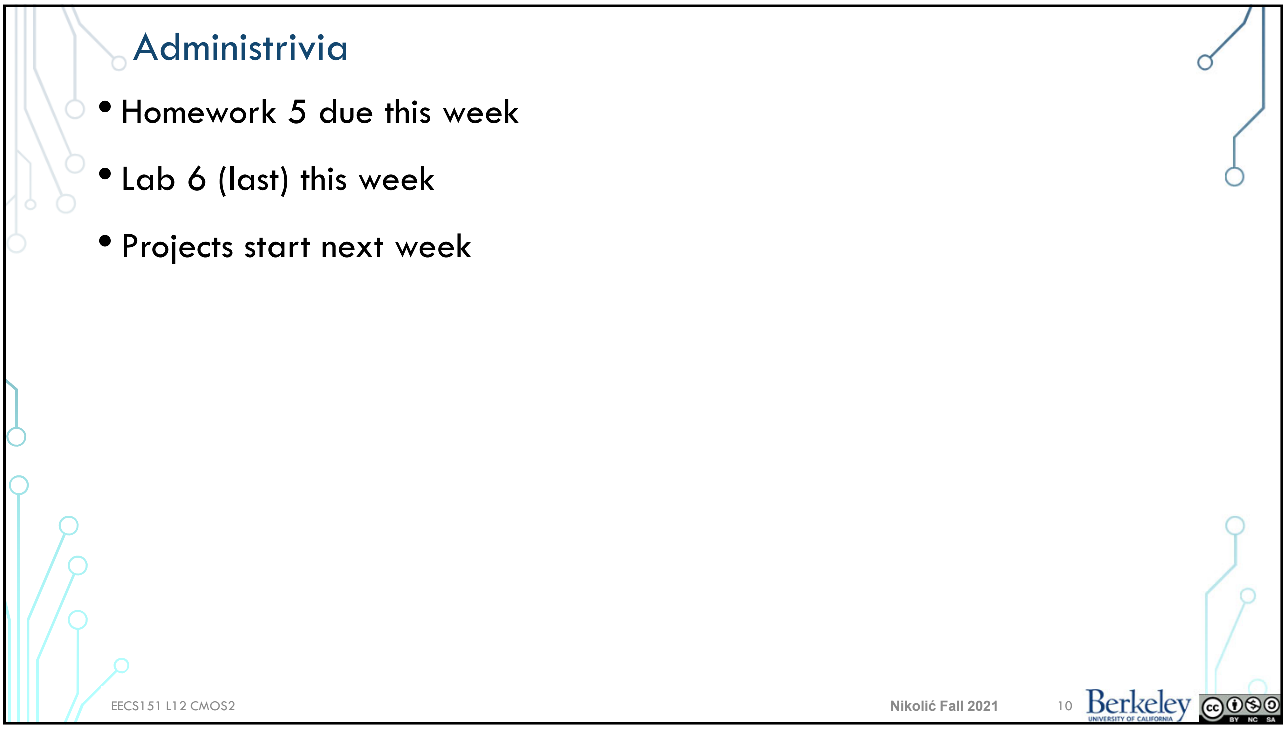
  Truth table

A	Out
0	1
1	0

- Multiple libraries
- Layouts
  - Number of metal 'tracks'
  - More tracks, faster, but larger
  - Less tracks – more compact, but slower
- Transistor thresholds (V_{Th}) (for each track height):
  - Regular (RVT)
  - Low (LVT)
    - Faster, higher power
    - Slower, lower power
  - High (HVT)
- Transistor lengths
- Multiple gate sizes within a library
  - Symbol
  - Schematic
  - Layout

INVX3,

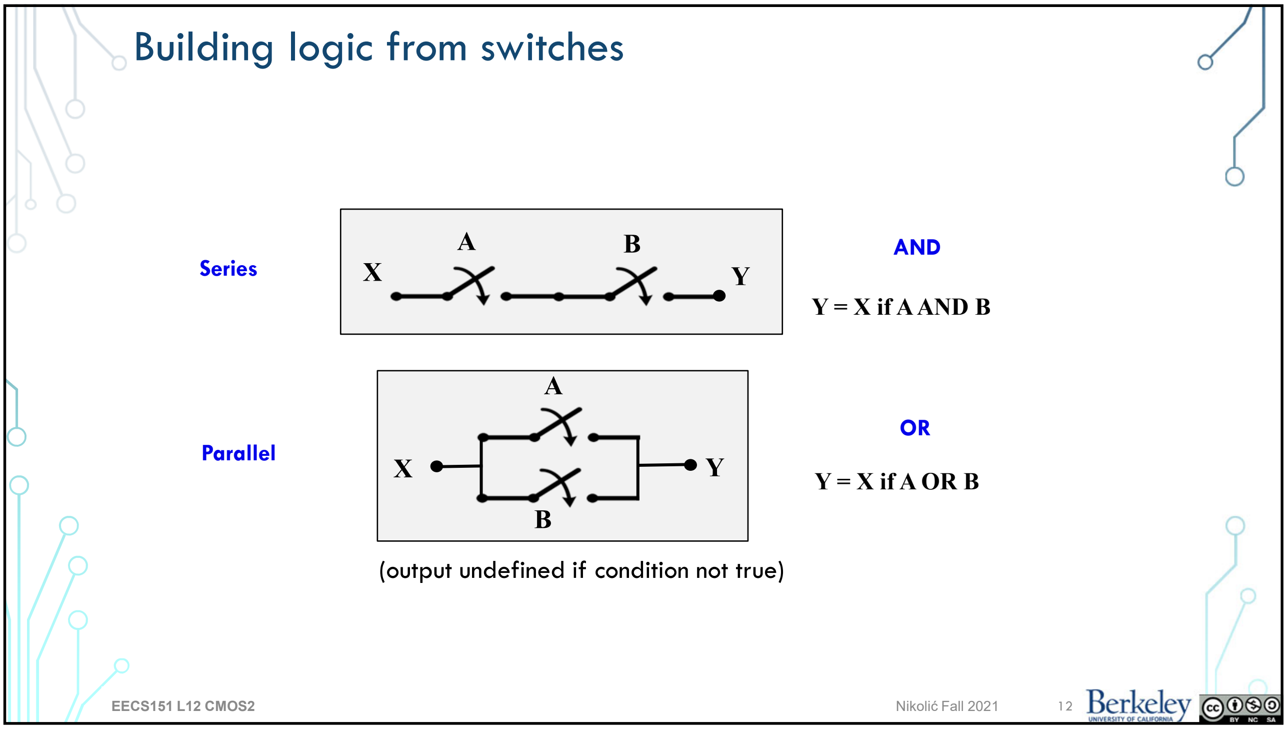
INVX4,…



Administrivia

- Homework 5 due this week
- Lab 6 (last) this week
- Projects start next week

CMOS Logic



Building logic from switches

Series

AND

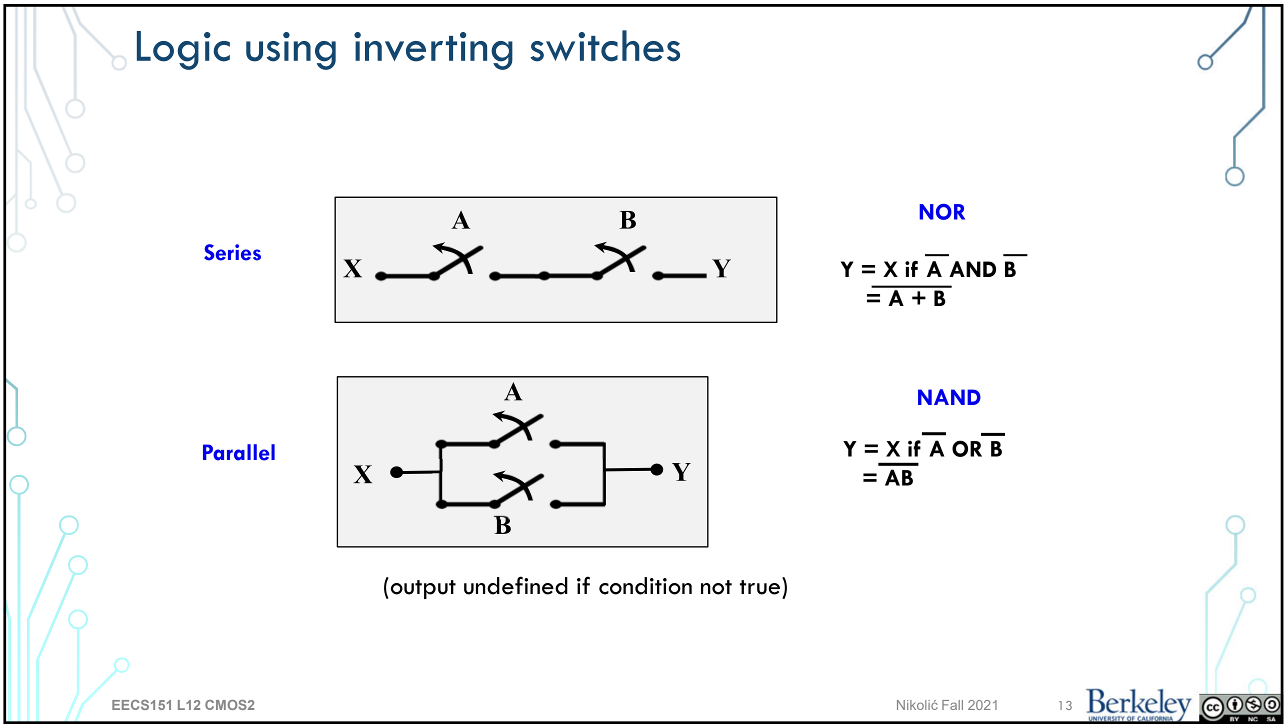
Y = X if A AND B

Parallel

OR

Y = X if A OR B

(output undefined if condition not true)



Logic using inverting switches

NOR

Y = X if $\overline{A}$ AND $\overline{B}$
= $\overline{A + B}$

NAND

Y = X if $\overline{A}$ OR $\overline{B}$
= $\overline{AB}$

(output undefined if condition not true)

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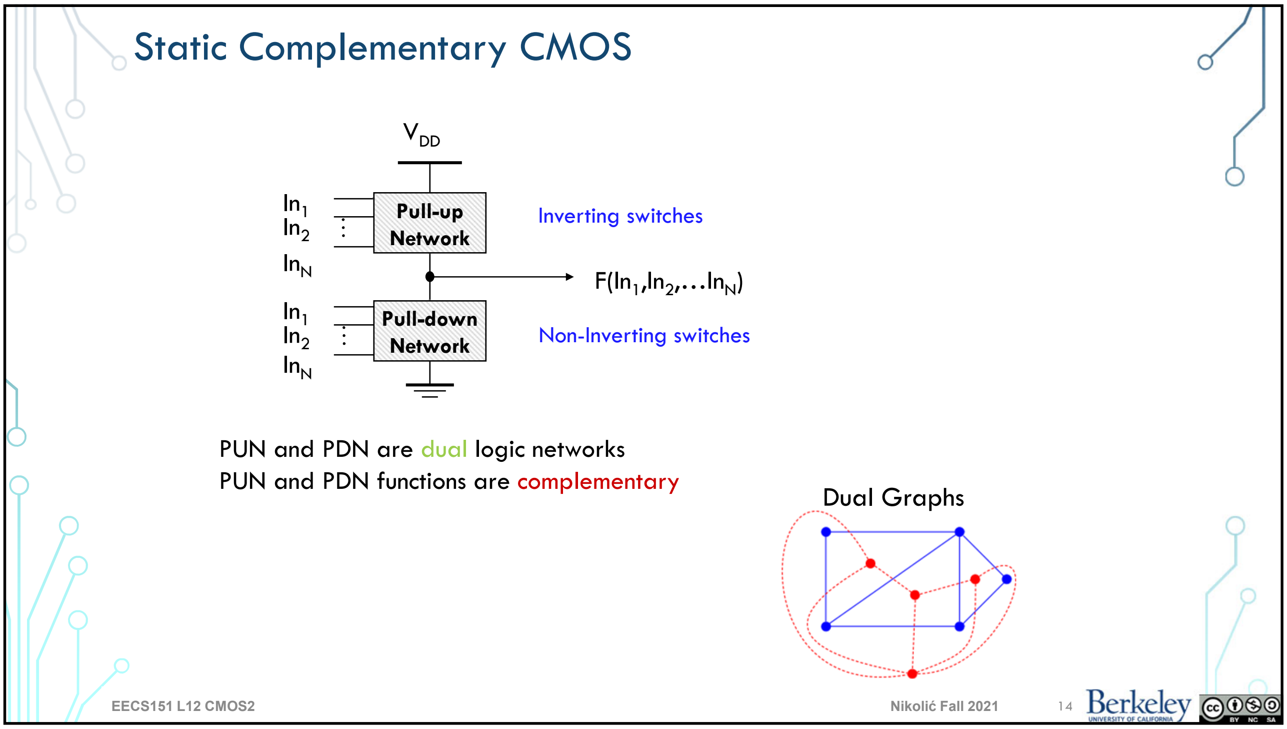

Static Complementary CMOS

Inverting switches

Non-Inverting switches

PUN and PDN are dual logic networks
PUN and PDN functions are complementary

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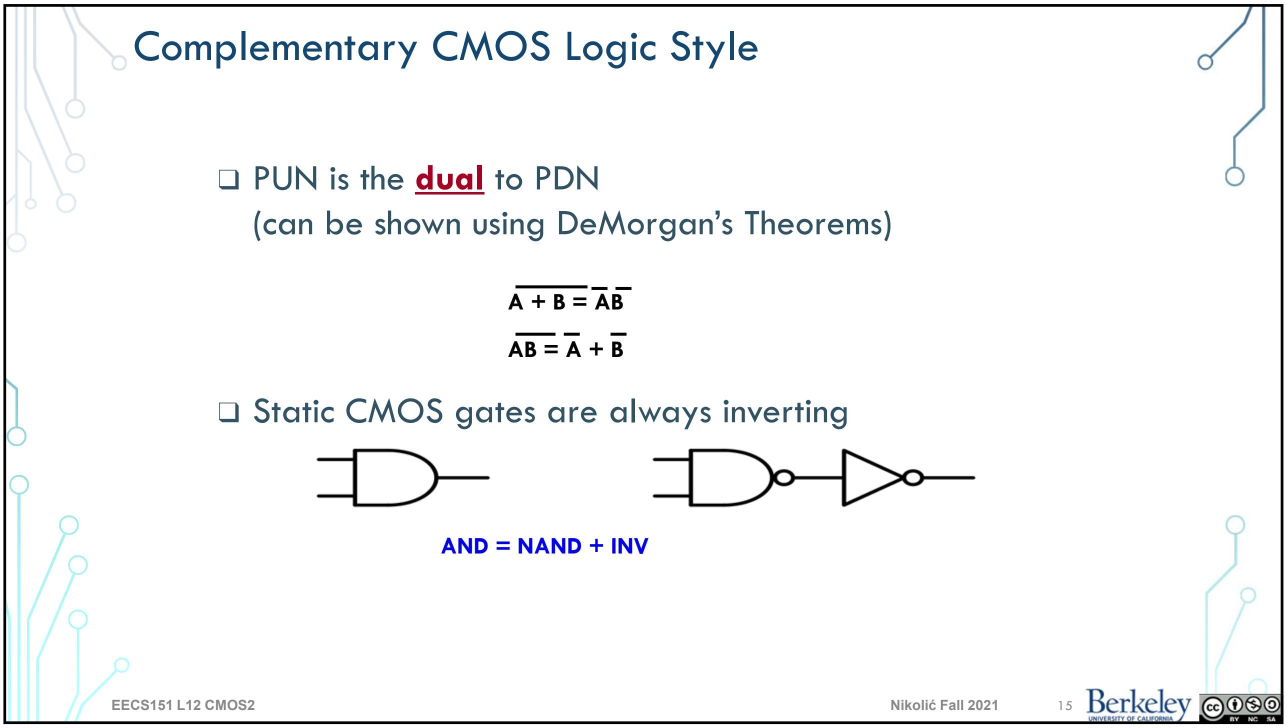

Complementary CMOS Logic Style

- PUN is the **dual** to PDN
  (can be shown using DeMorgan's Theorems)

$$\overline{A + B} = \overline{A}\,\overline{B}$$

$$\overline{AB} = \overline{A} + \overline{B}$$

- Static CMOS gates are always inverting

AND = NAND + INV

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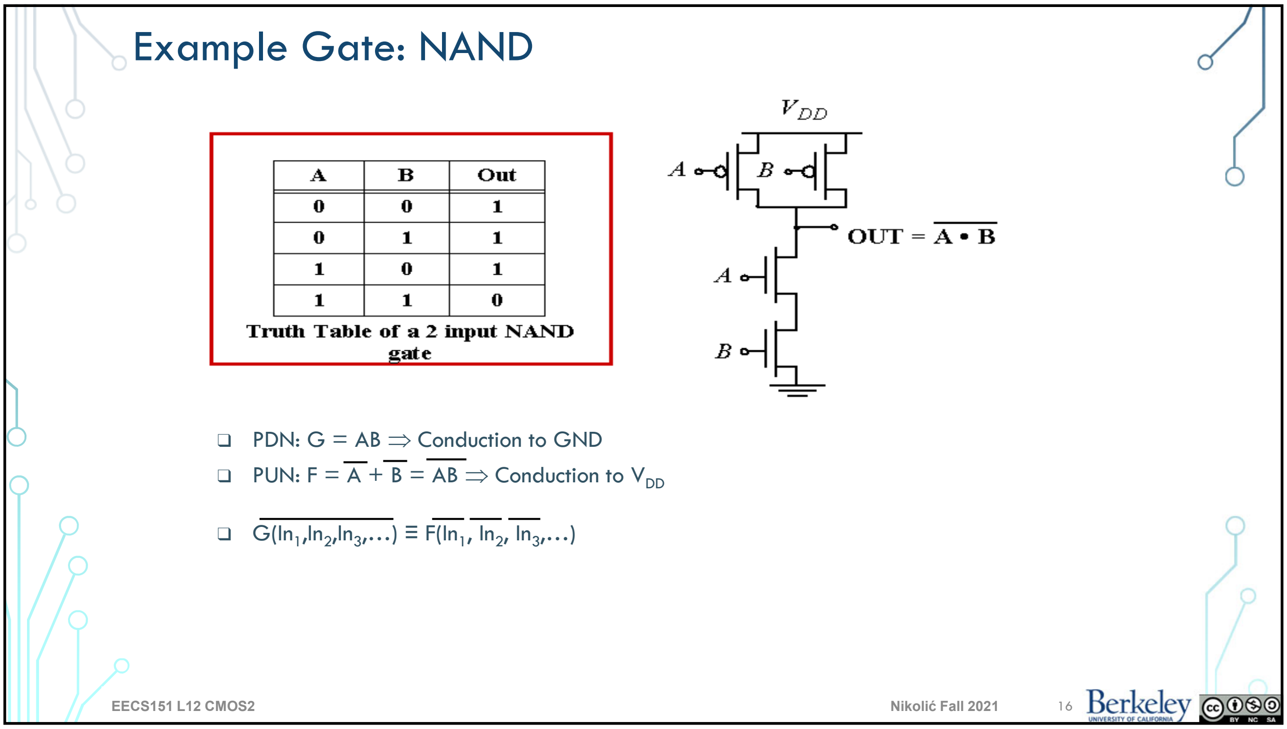

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

V_{DD}
A
B
OUT = $\overline{A \bullet B}$
A
B

- PDN: G = AB ⇒ Conduction to GND
- PUN: F = $\overline{A} + \overline{B} = \overline{AB}$ ⇒ Conduction to V_{DD}
- $\overline{G(In_1,In_2,In_3,\ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3},\ldots)$

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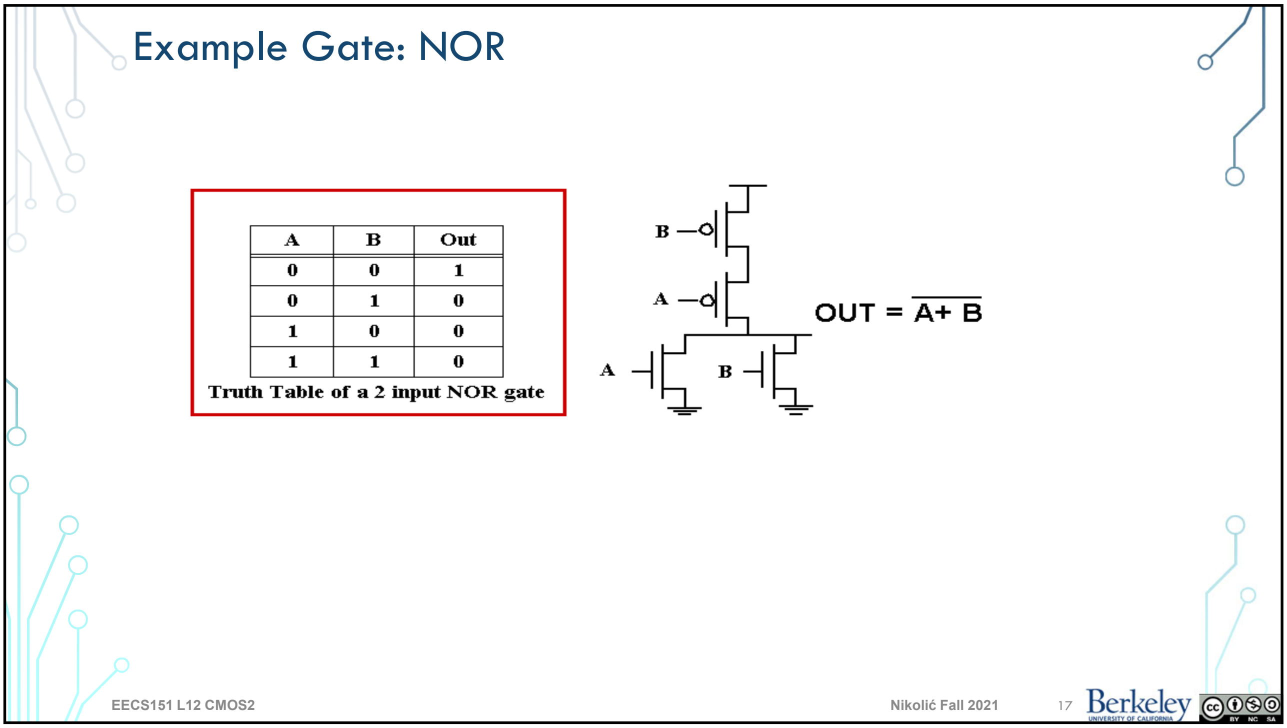

Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate

OUT = $\overline{A+B}$

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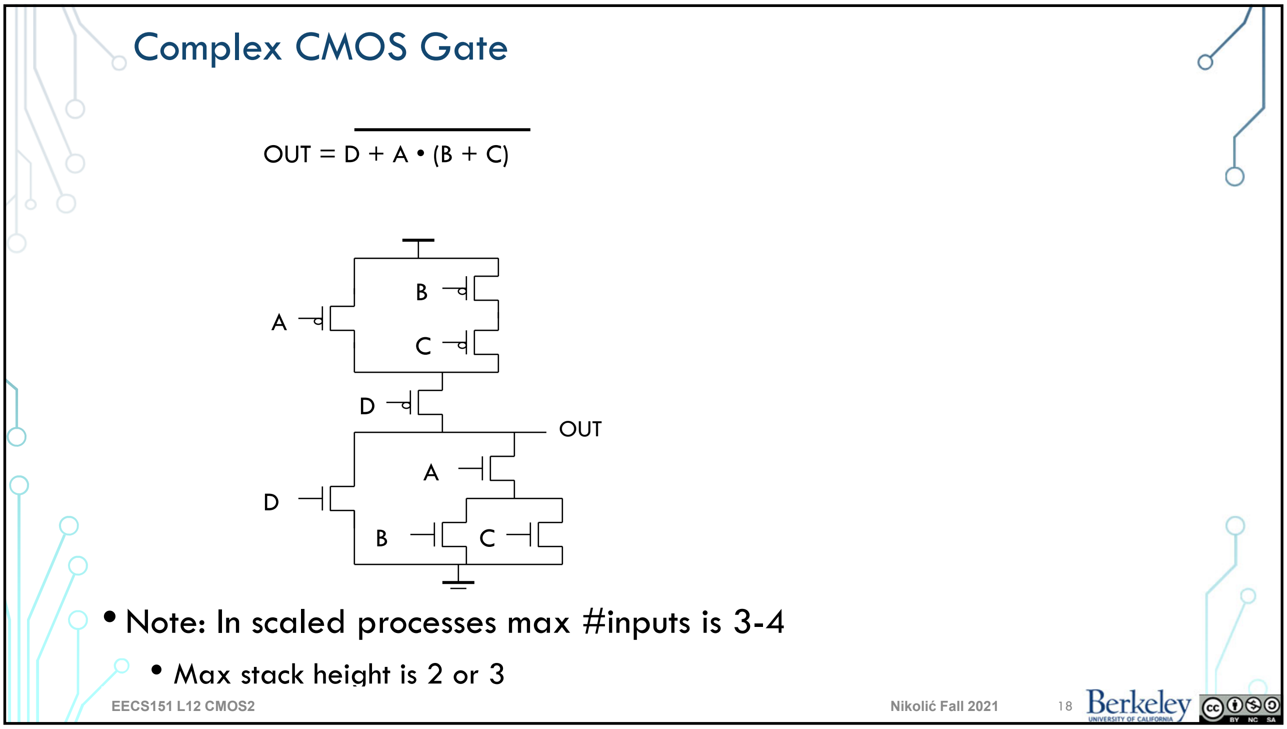

Complex CMOS Gate

OUT = $\overline{D + A \cdot (B + C)}$

- Note: In scaled processes max #inputs is 3-4
  - Max stack height is 2 or 3

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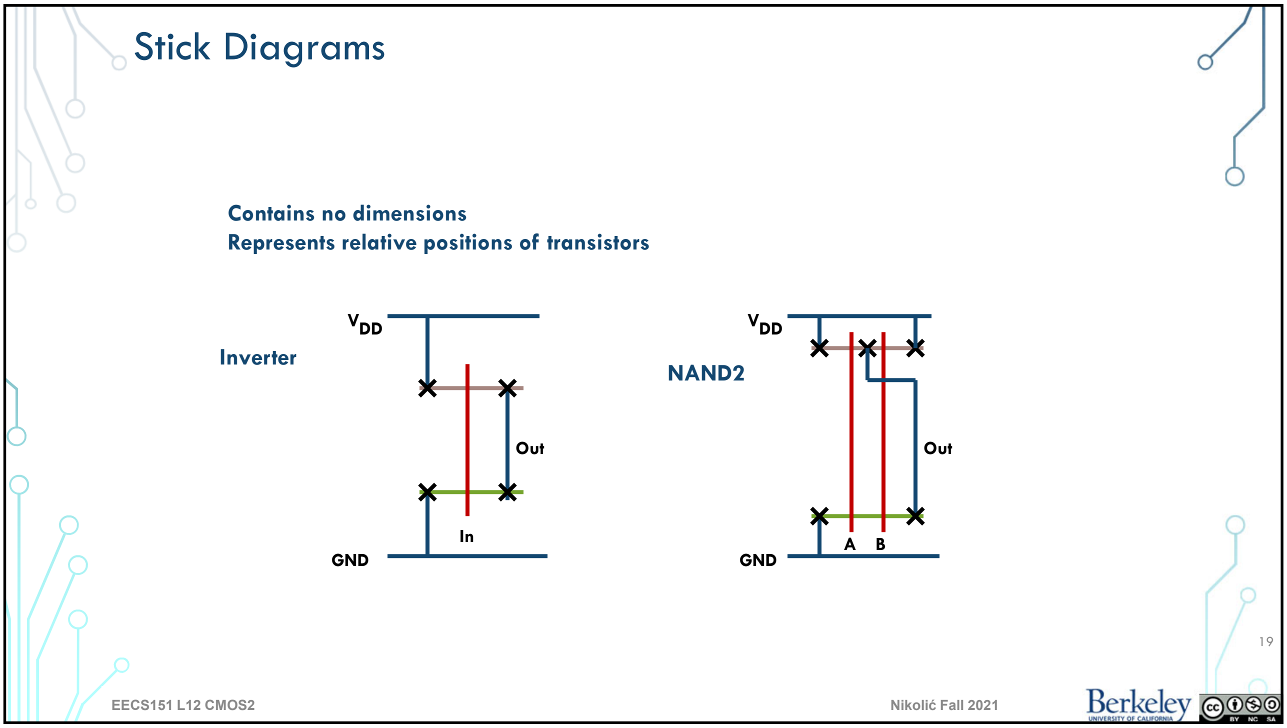
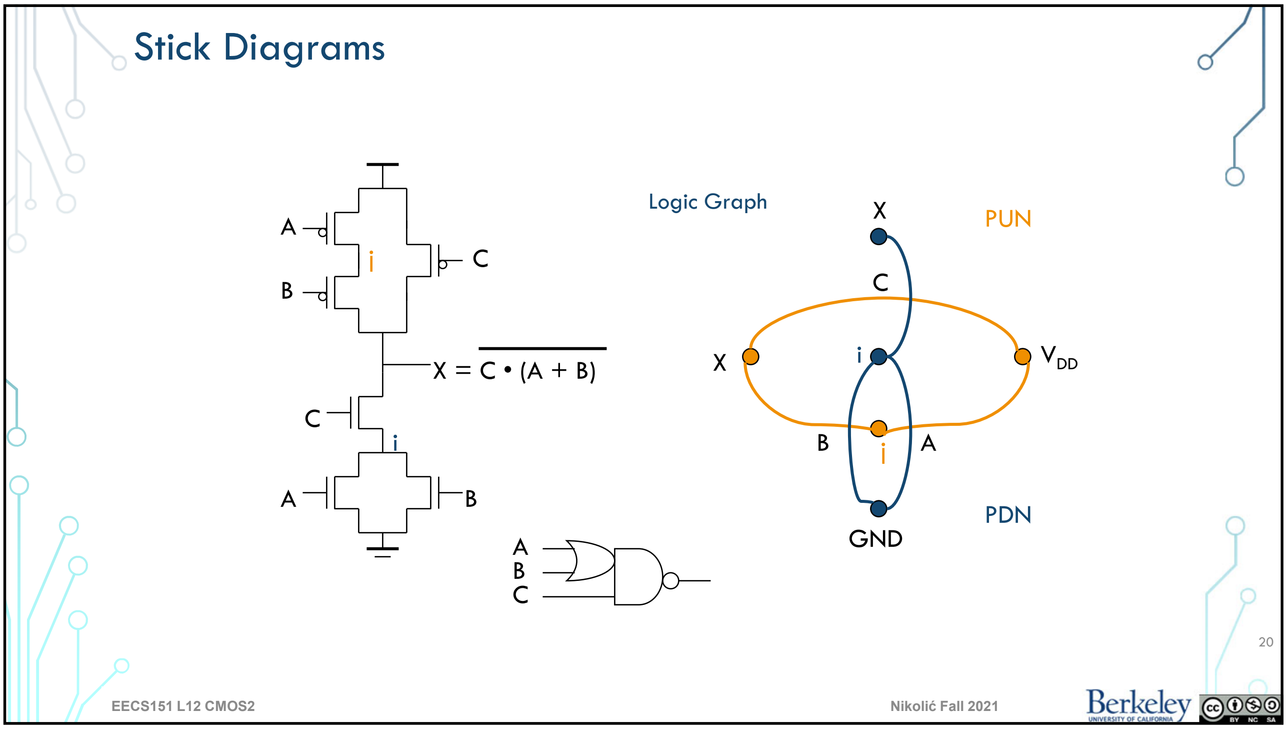
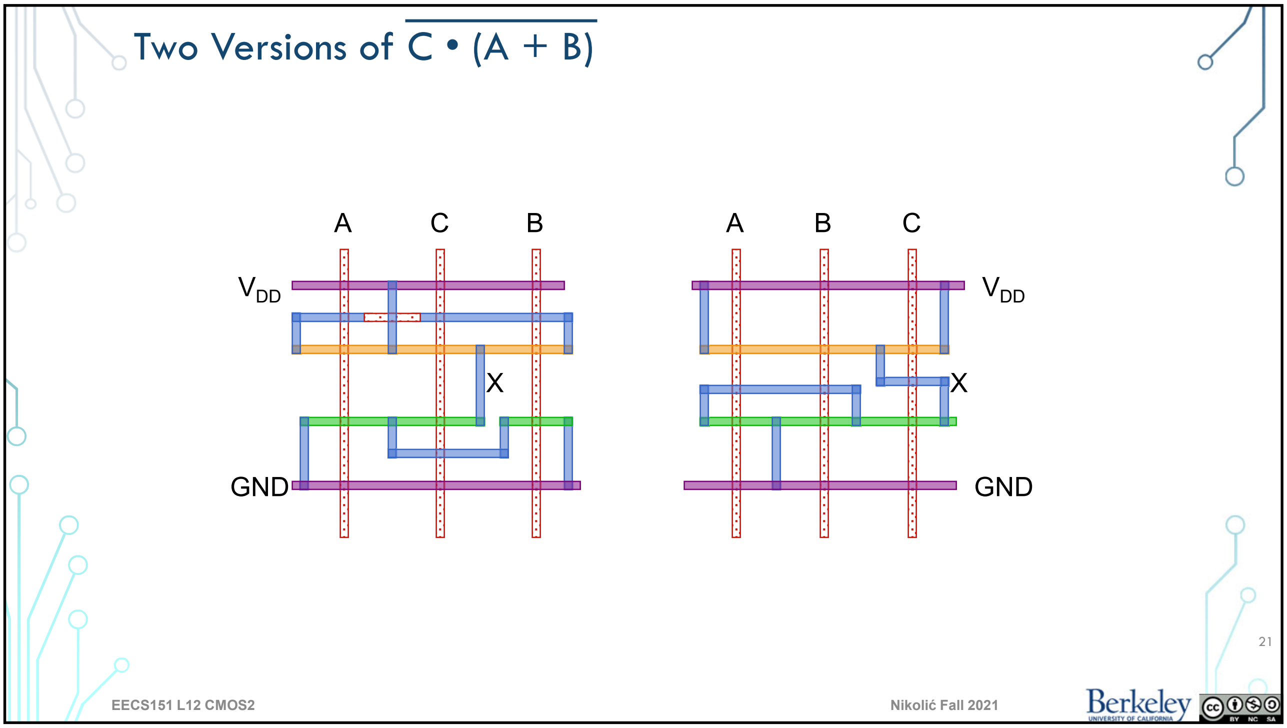


Stick Diagrams

Contains no dimensions
Represents relative positions of transistors



Stick Diagrams



Two Versions of $\overline{C \bullet (A + B)}$

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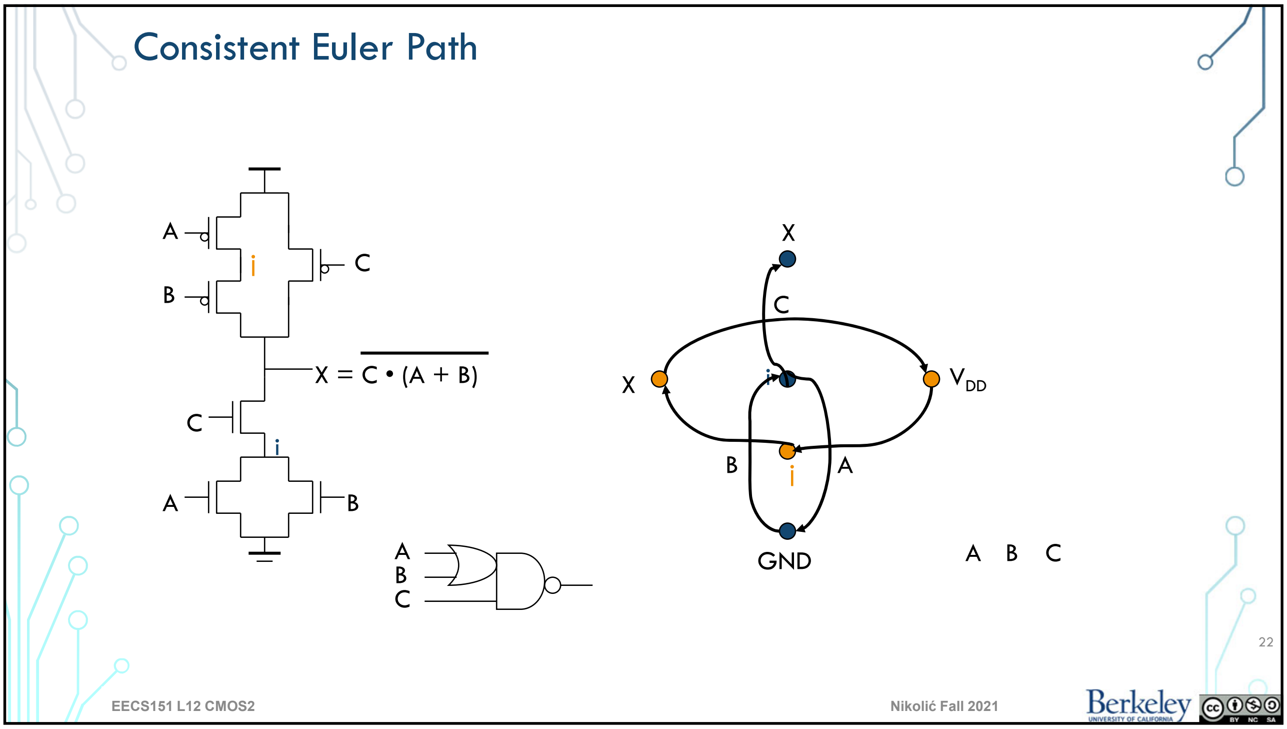

Consistent Euler Path

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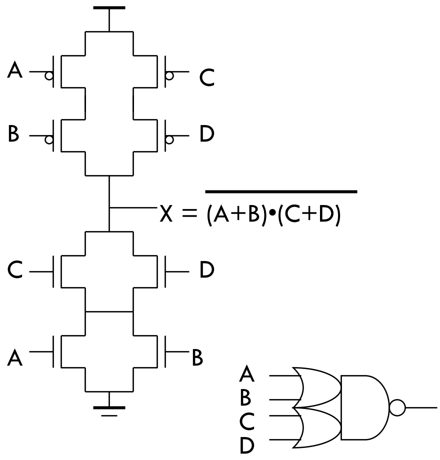
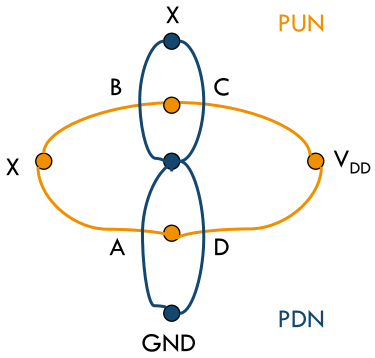
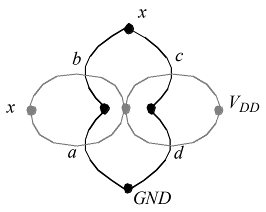
OAI22 Logic Graph

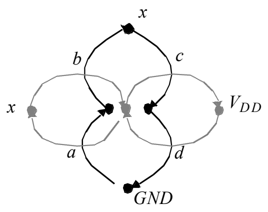




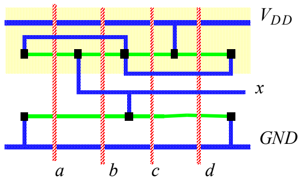
Example: x = $\overline{ab+cd}$



(a) Logic graphs for $\overline{(ab+cd)}$

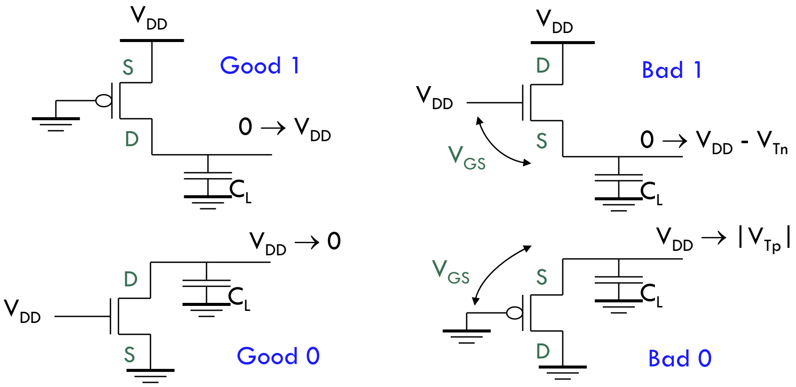


(b) Euler Paths {$a\ b\ c\ d$}



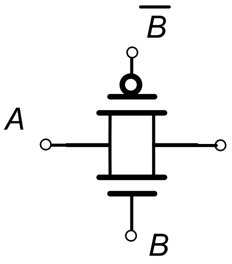
(c) stick diagram for ordering {a b c d}

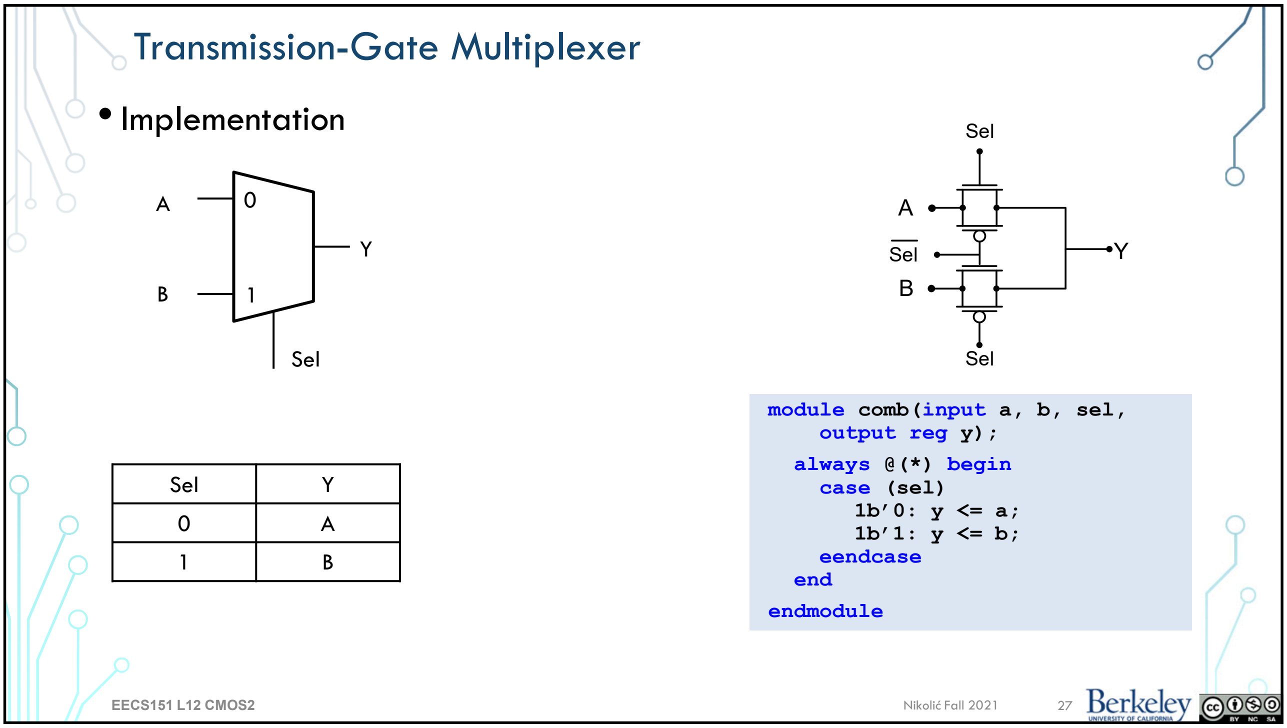
Switch Limitations



Transmission Gate

- Transmission gates are the way to build "switches" in CMOS.
- In general, both transistor types are needed:
  - ❑nFET to pass zeros.
  - ❑pFET to pass ones.
- The transmission gate is 'non-isolating'.



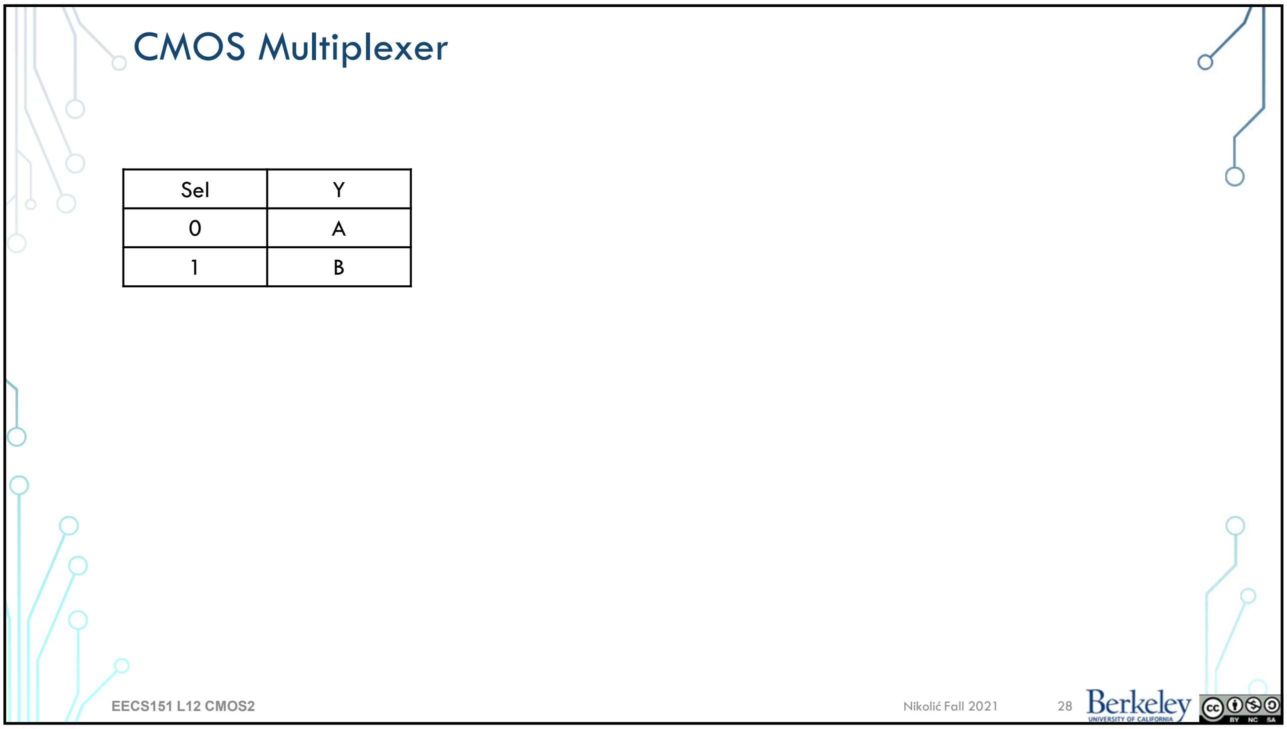


Transmission-Gate Multiplexer

- Implementation

Sel	Y
0	A
1	B

```
module comb(input a, b, sel,
    output reg y);
  always @(*) begin
    case (sel)
       1b’0: y <= a;
       1b’1: y <= b;
    eendcase
  end
endmodule
```



CMOS Multiplexer

Sel	Y
0	A
1	B

CMOS Sizing

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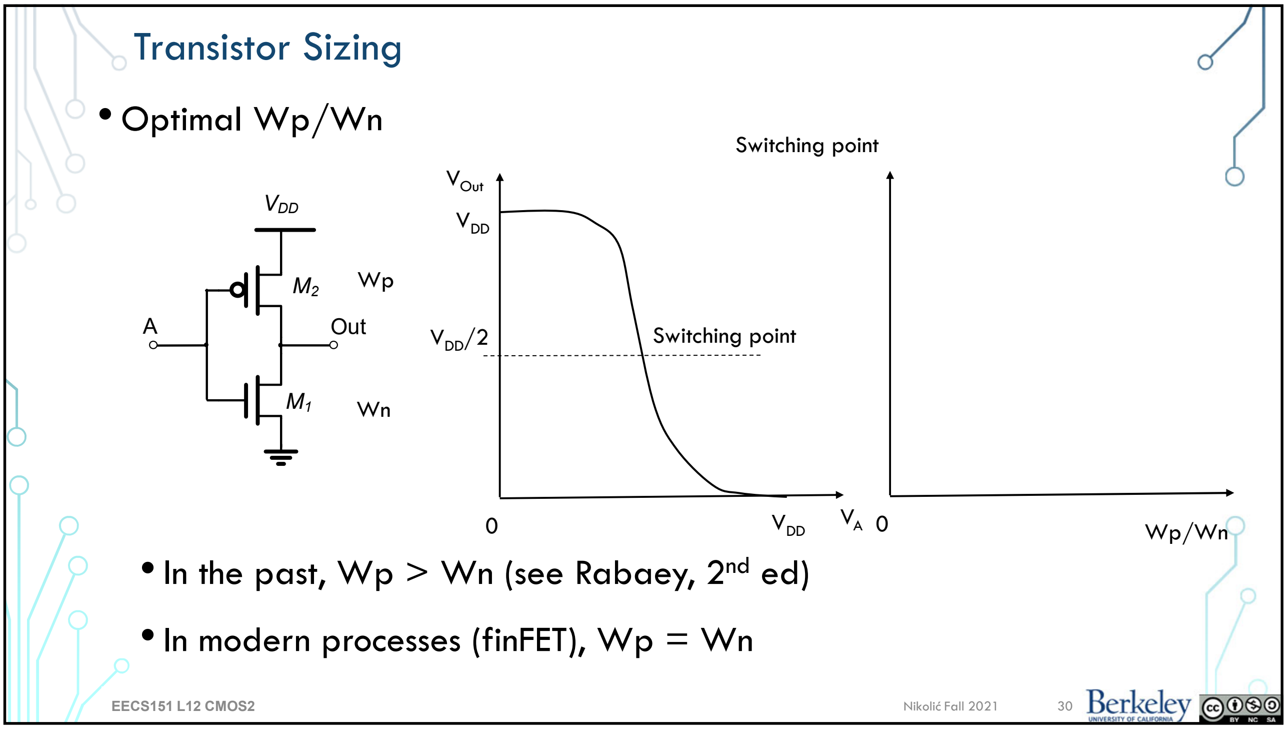

Transistor Sizing

- Optimal Wp/Wn

- In the past, Wp > Wn (see Rabaey, 2nd ed)
- In modern processes (finFET), Wp = Wn

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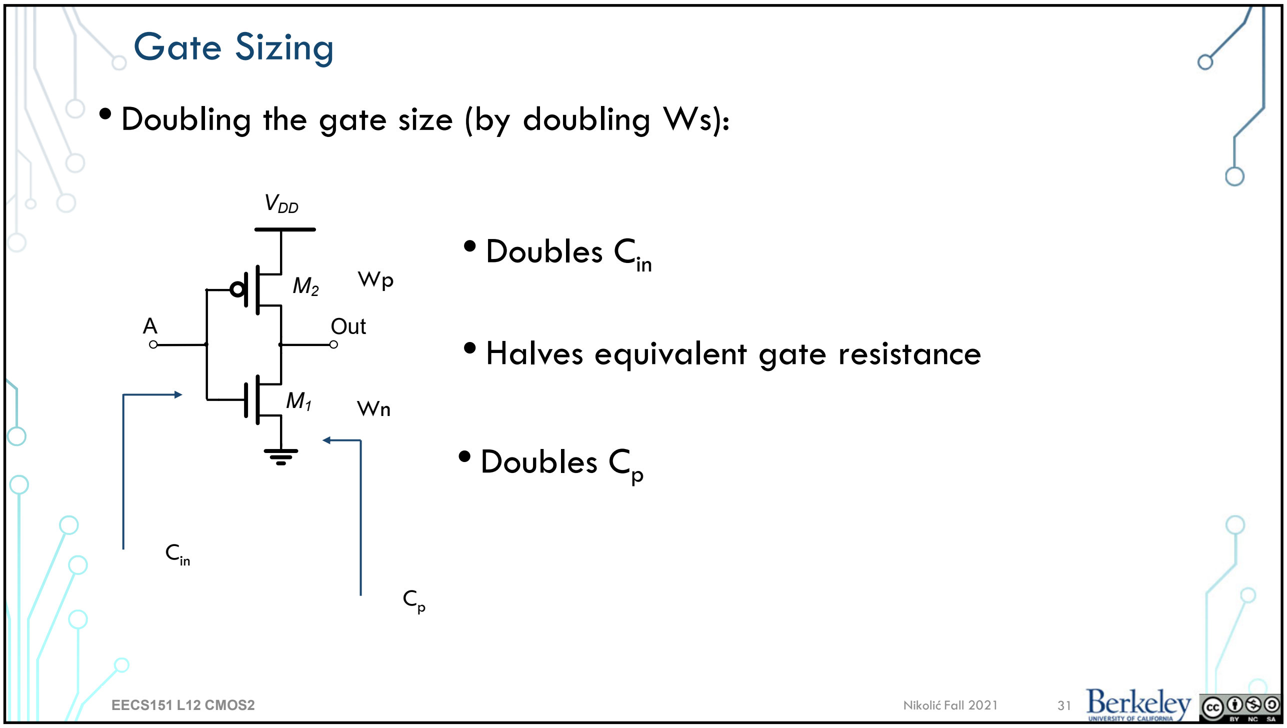
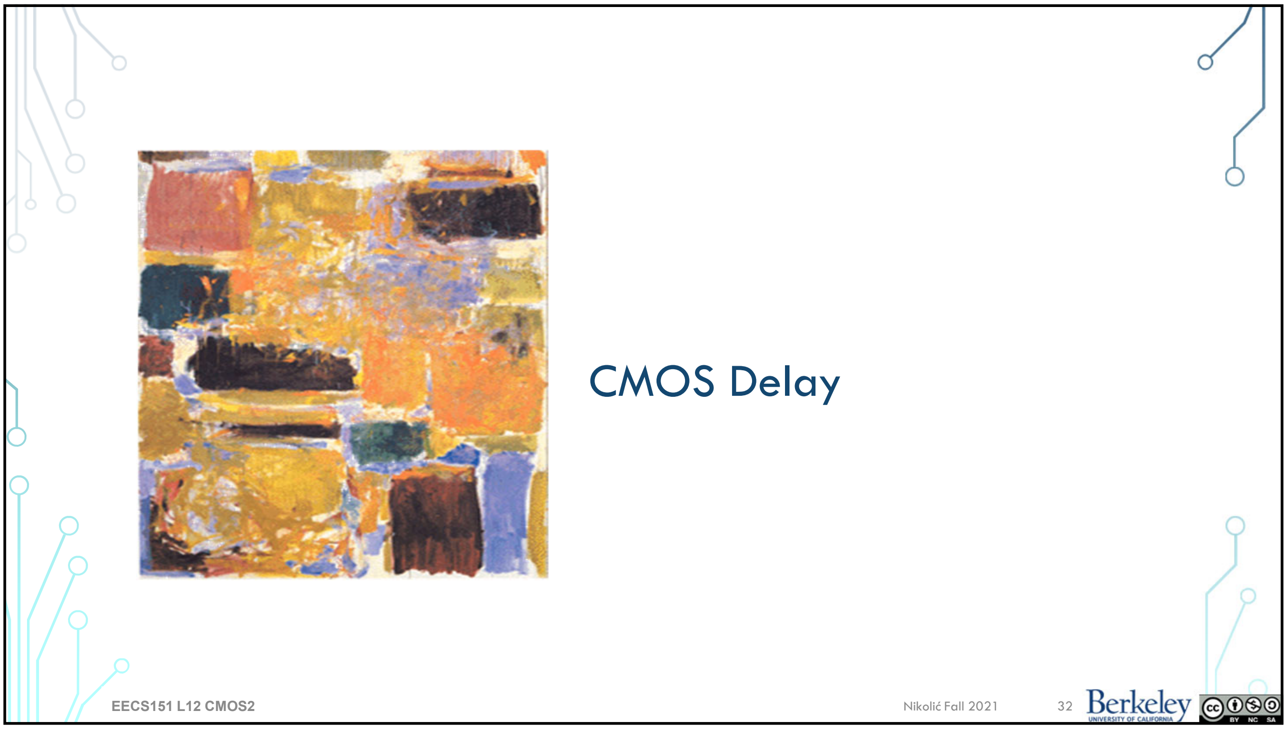


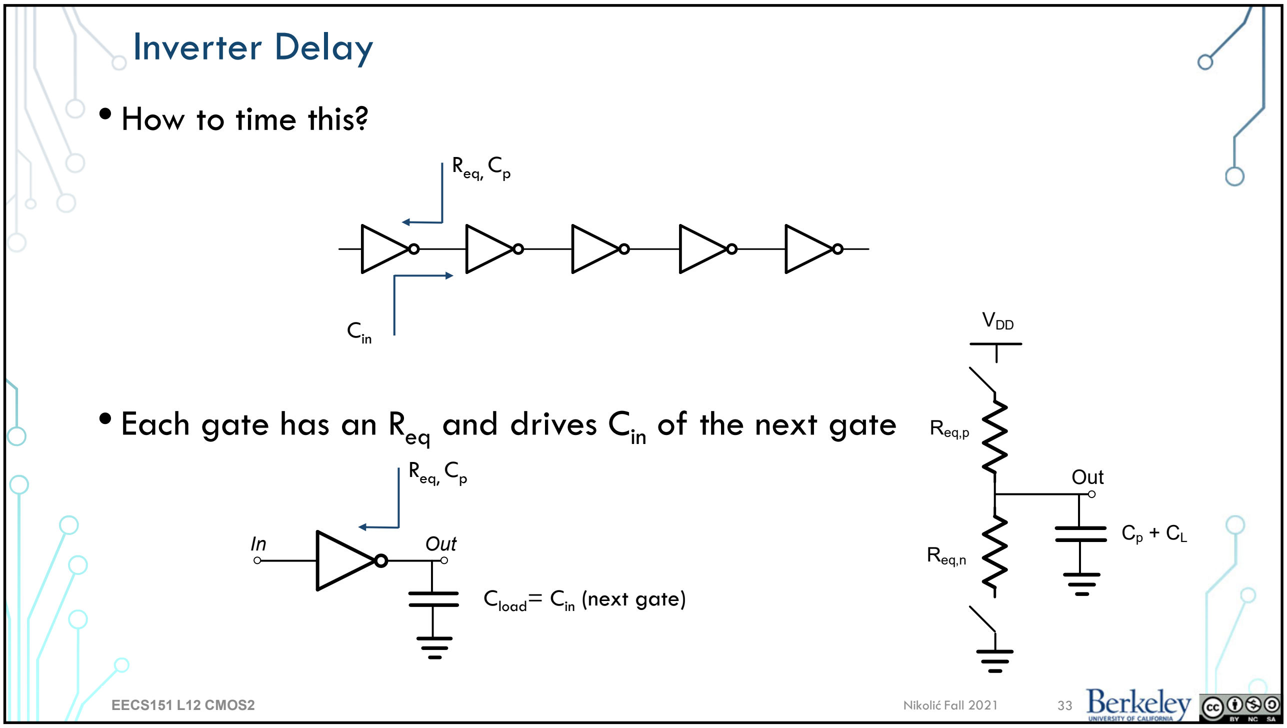
Gate Sizing

- Doubling the gate size (by doubling Ws):

- Doubles C_{in}
- Halves equivalent gate resistance
- Doubles C_p



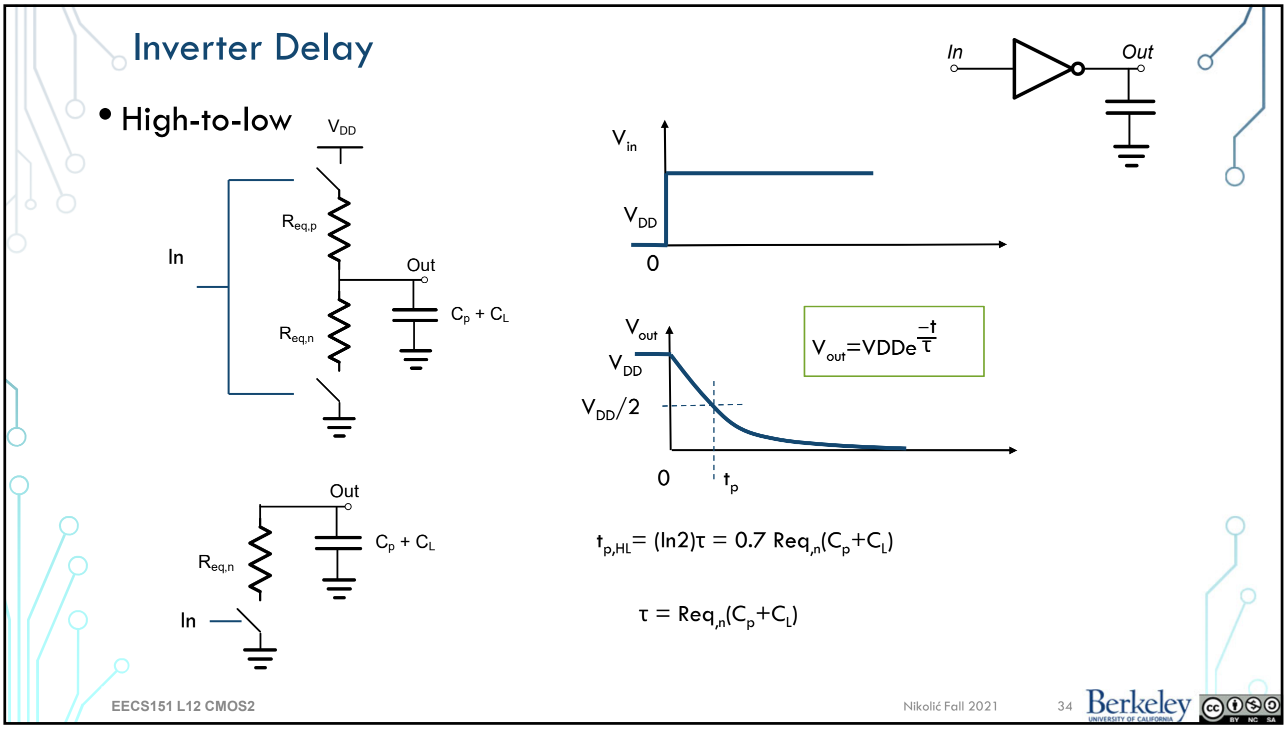
CMOS Delay



Inverter Delay

- How to time this?

- Each gate has an R_{eq} and drives C_{in} of the next gate



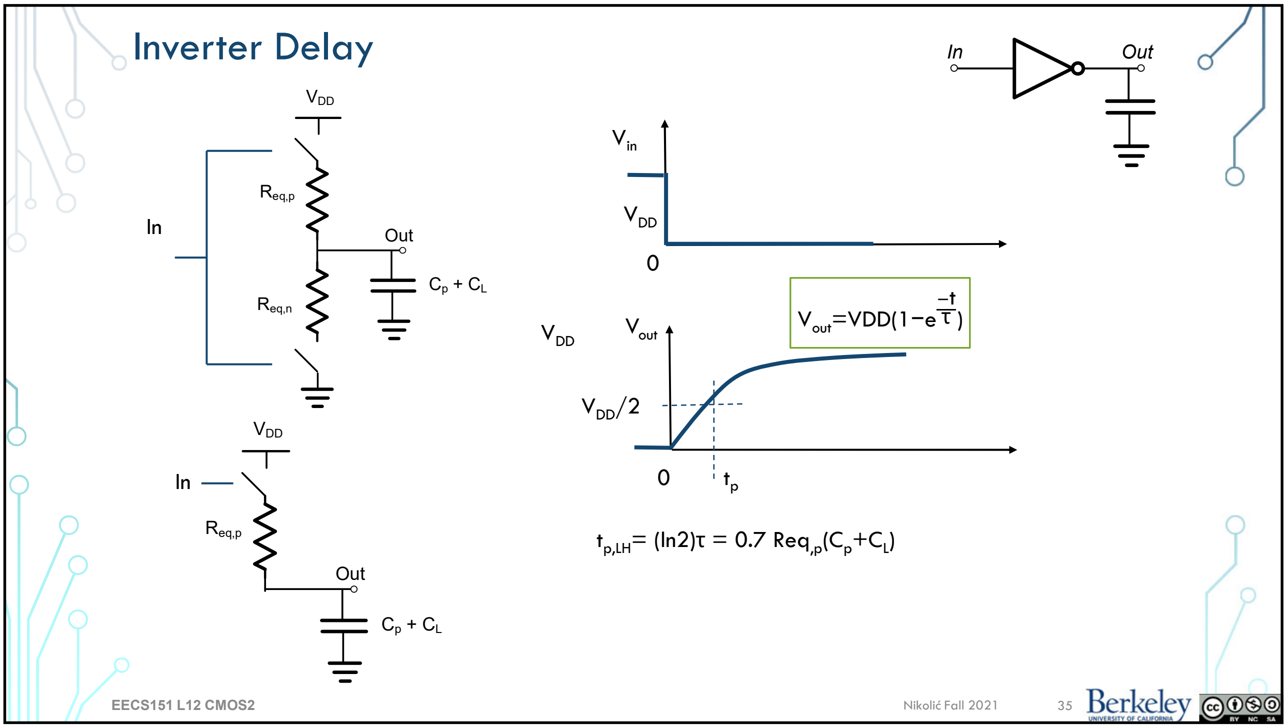
Inverter Delay

- High-to-low

V_{out}=$VDDe^{\frac{-t}{\tau}}$

$t_{p,HL}$= (ln2)τ = 0.7 $Req_{,n}(C_p+C_L)$

τ = $Req_{,n}(C_p+C_L)$



Inverter Delay

$V_{out}=VDD(1-e^{\frac{-t}{\tau}})$

$t_{p,LH}= (\ln 2)\tau = 0.7\ Req_{,p}(C_p+C_L)$

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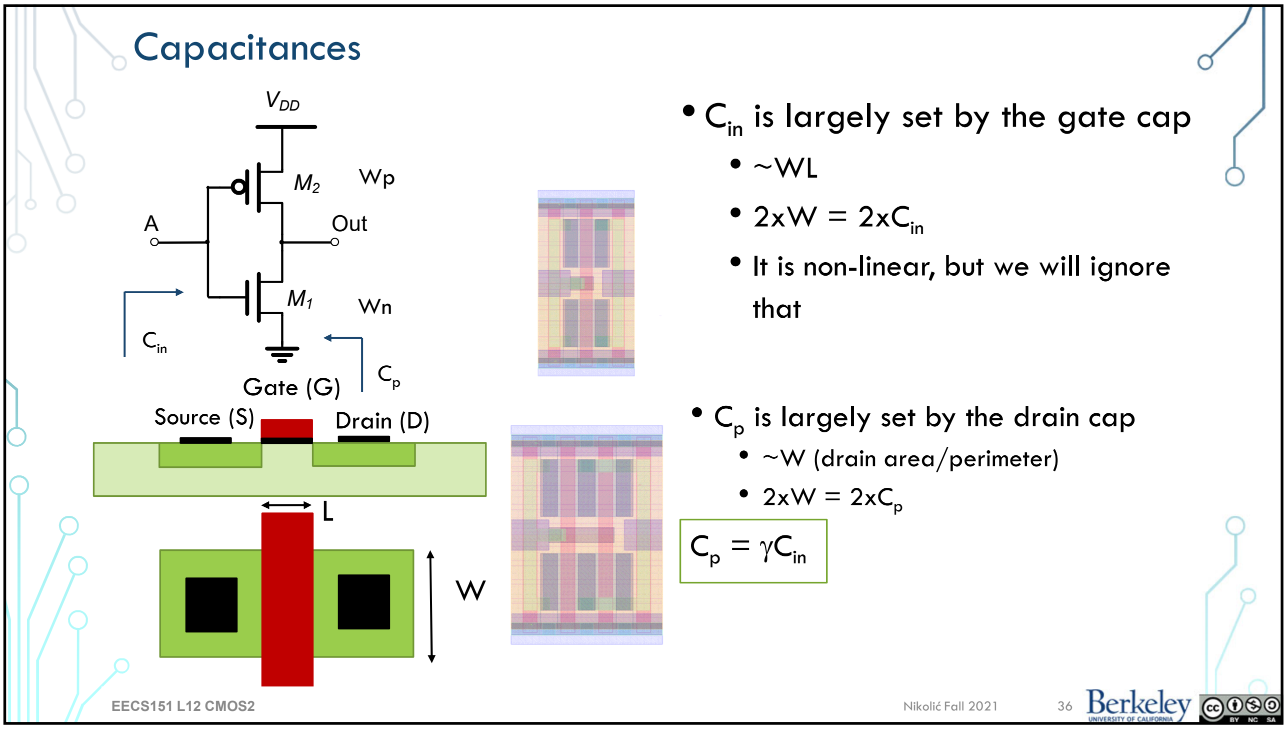

Capacitances

- C_{in} is largely set by the gate cap
  - ~WL
  - 2xW = 2xC_{in}
  - It is non-linear, but we will ignore that
- C_p is largely set by the drain cap
  - ~W (drain area/perimeter)
  - 2xW = 2xC_p

$\boxed{C_p = \gamma C_{in}}$

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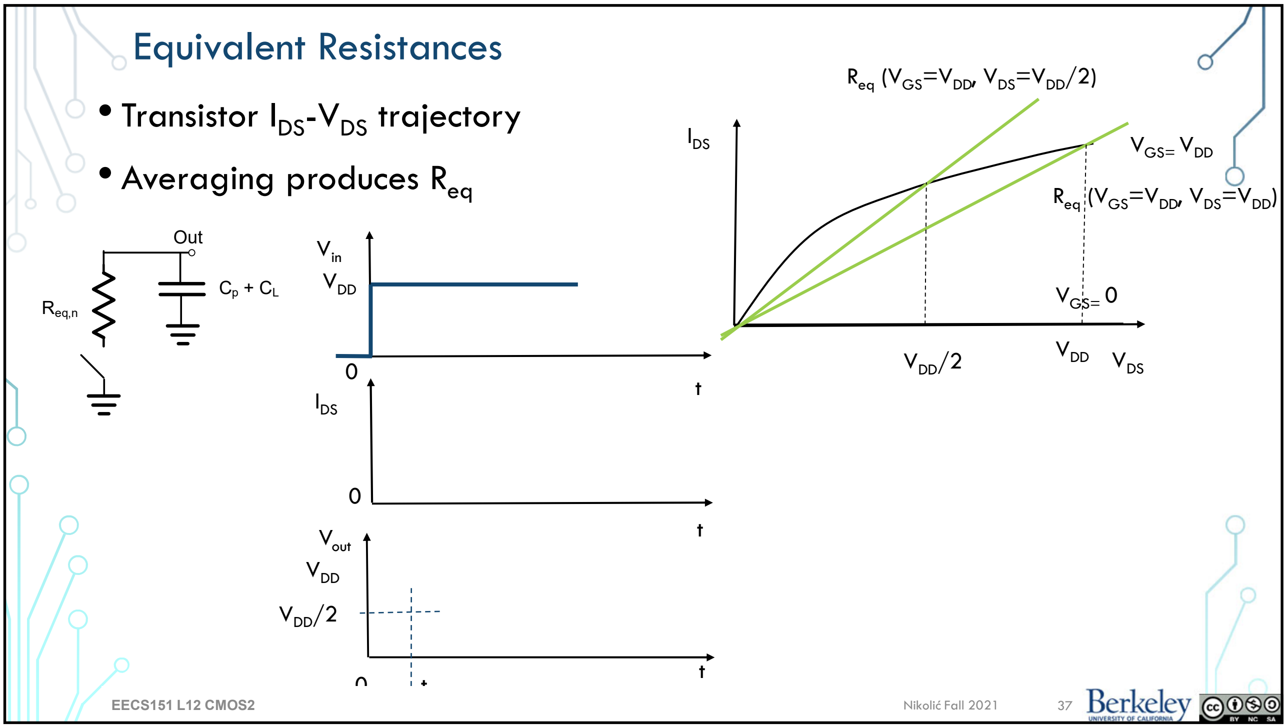

Equivalent Resistances

- Transistor I_{DS}-V_{DS} trajectory
- Averaging produces R_{eq}

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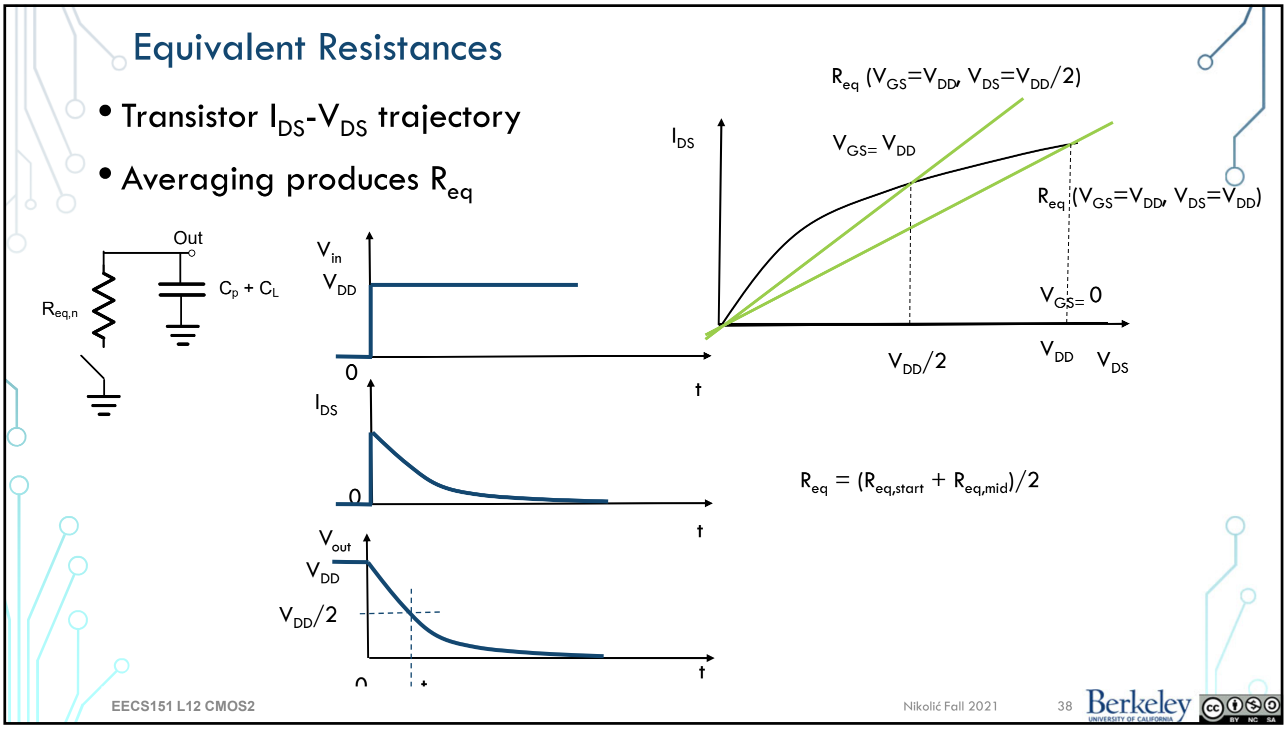

Equivalent Resistances

- Transistor I_{DS}-V_{DS} trajectory
- Averaging produces R_{eq}

$R_{eq} = (R_{eq,start} + R_{eq,mid})/2$

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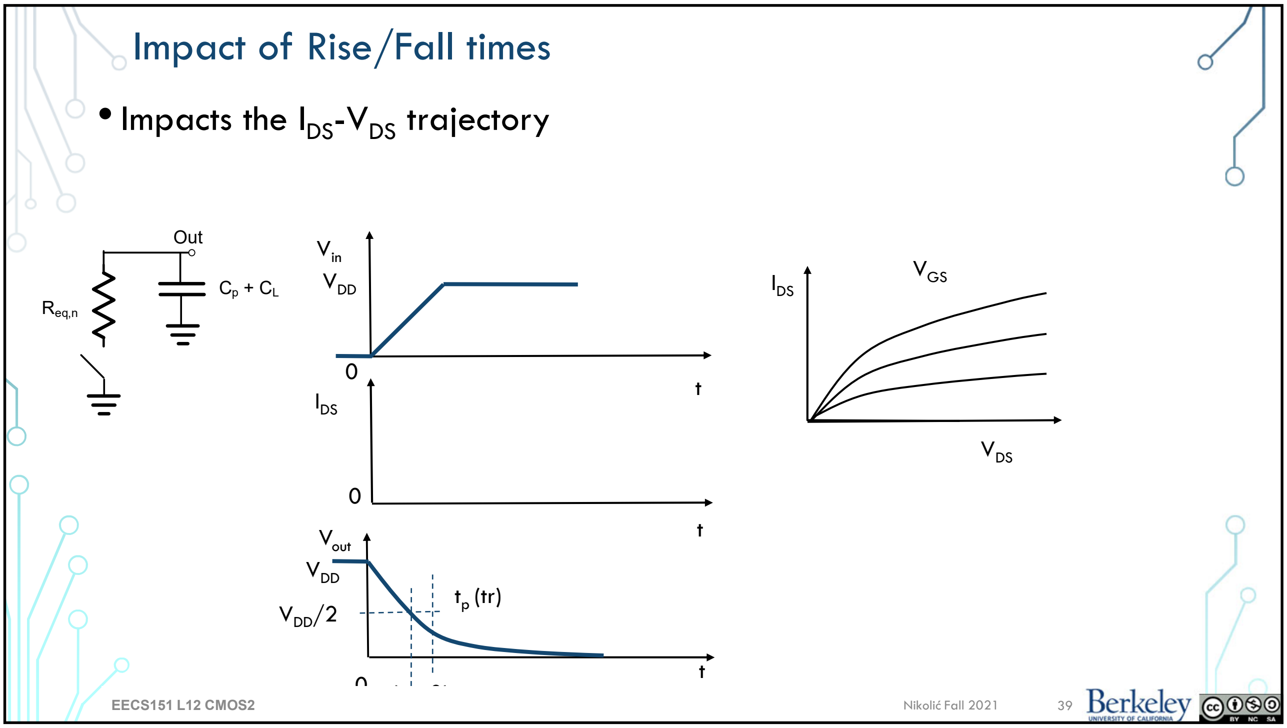

Impact of Rise/Fall times

- Impacts the I_{DS}-V_{DS} trajectory

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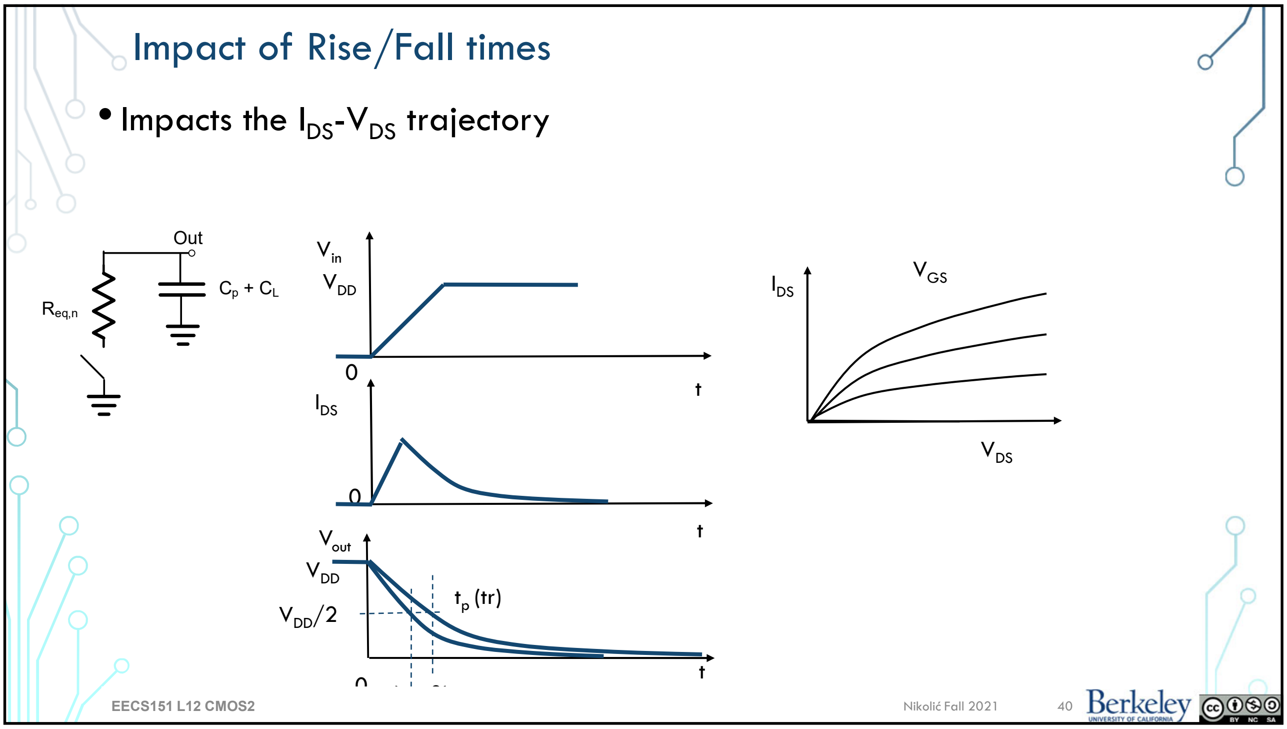

Impact of Rise/Fall times

- Impacts the I_{DS}-V_{DS} trajectory

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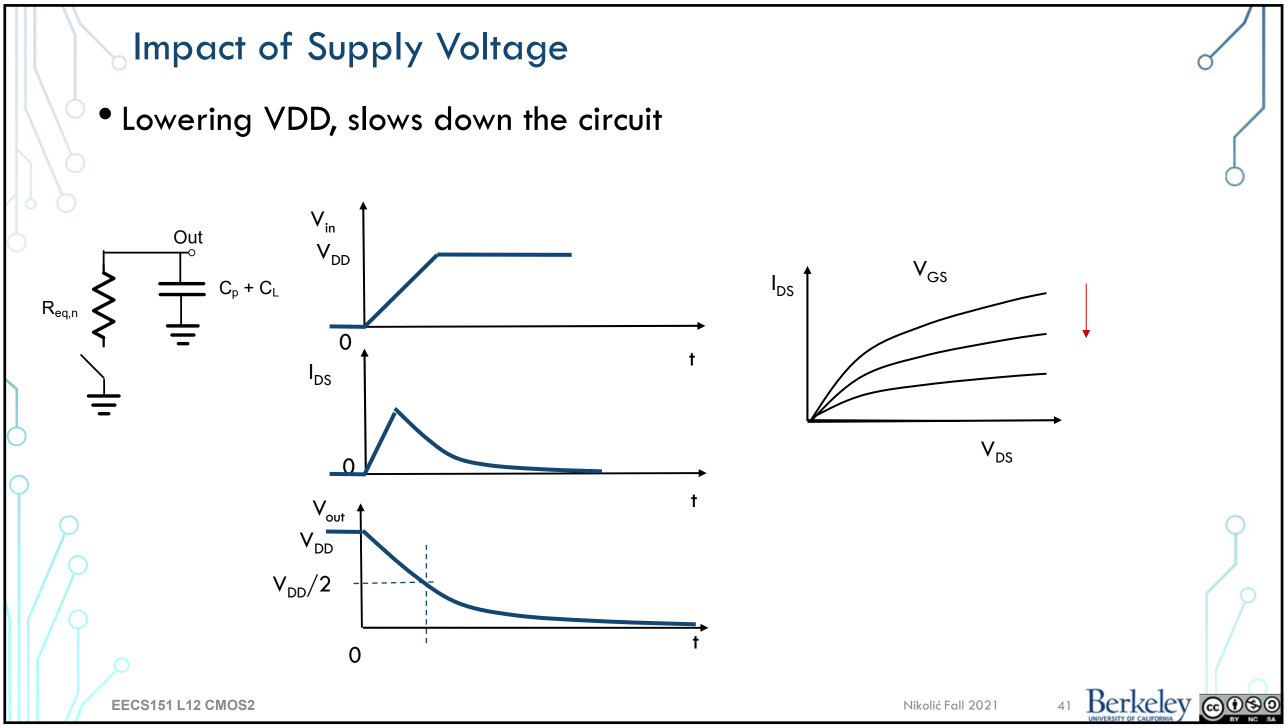

Impact of Supply Voltage

- Lowering VDD, slows down the circuit

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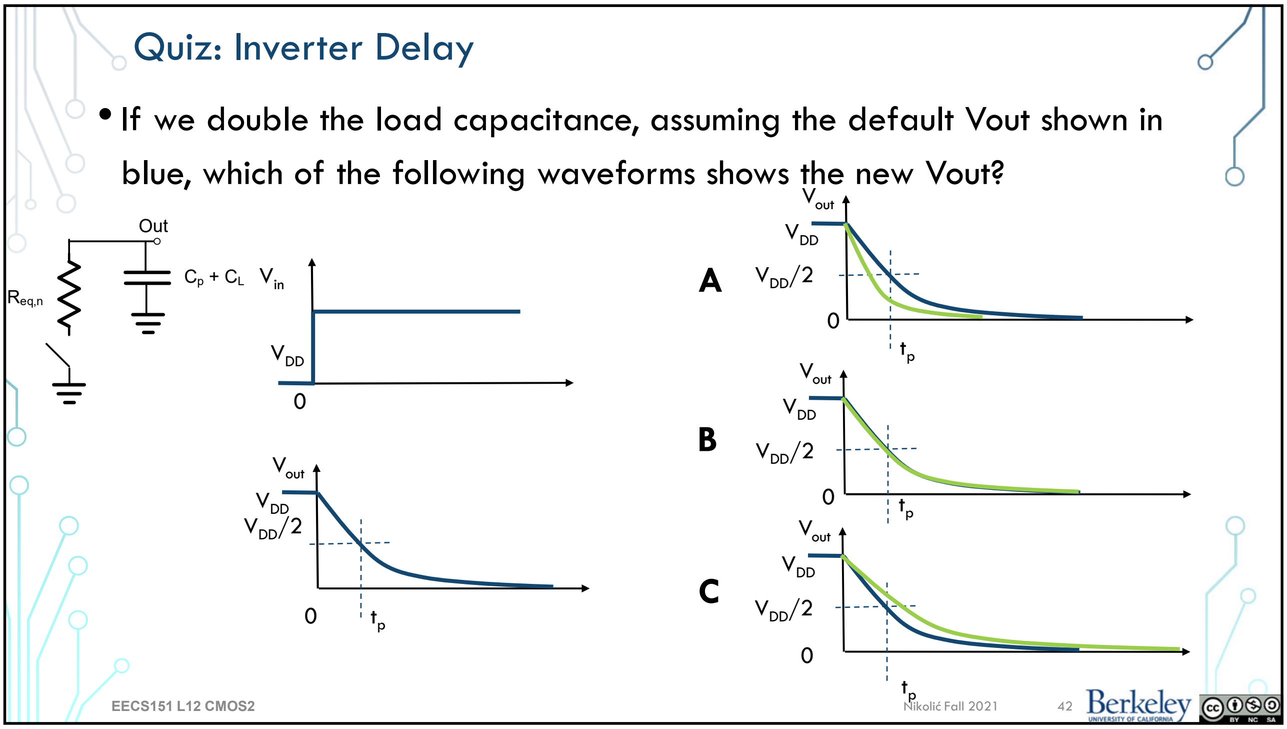

Quiz: Inverter Delay

- If we double the load capacitance, assuming the default Vout shown in blue, which of the following waveforms shows the new Vout?

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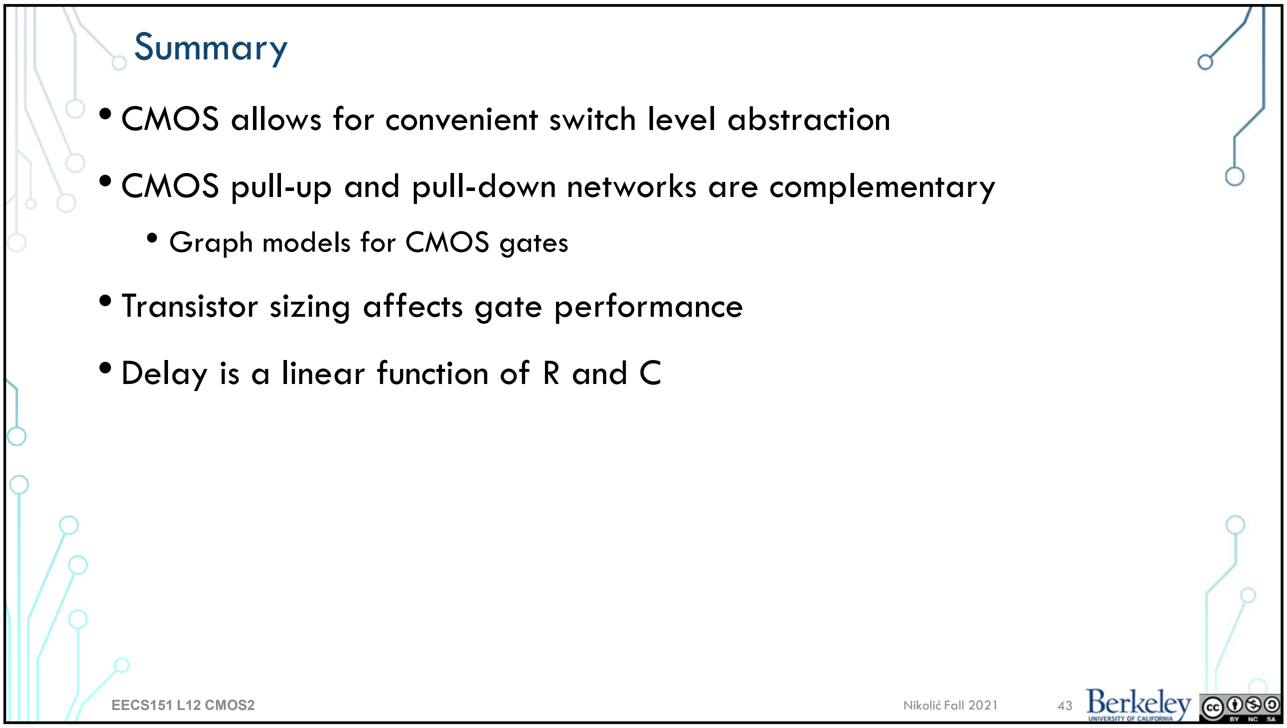

Summary

- CMOS allows for convenient switch level abstraction
- CMOS pull-up and pull-down networks are complementary
  - Graph models for CMOS gates
- Transistor sizing affects gate performance
- Delay is a linear function of R and C

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