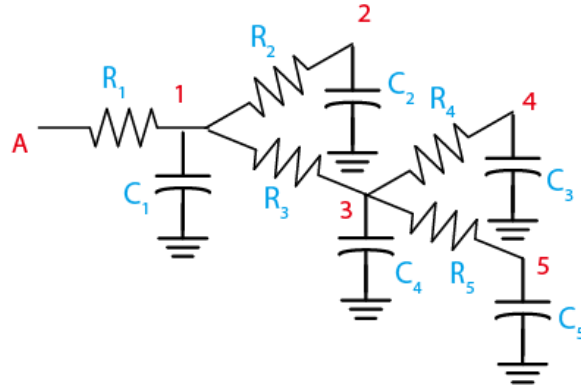


# EECS 151/251A Homework 7

Due Monday, April 11<sup>th</sup>, 2022

## Problem 1: Fun with RC Delay



The value of each component in the RC network here is listed below:

Name	Value	Name	Value
C1	100 fF (= $100 * 10^{-15} F$ )	R1	1000 $\Omega$
C2	50 fF	R2	1200 $\Omega$
C3	60 fF	R3	1500 $\Omega$
C4	20 fF	R4	1800 $\Omega$
C5	30 fF	R5	2000 $\Omega$

Find the RC delay constant  $\tau$  from node A to node 4.

First we calculate  $\tau$  of the net by viewing  $s$  as the input and  $i$  as the output:

$$\tau = \sum_n \left( R_n \sum_m C_m \right)$$

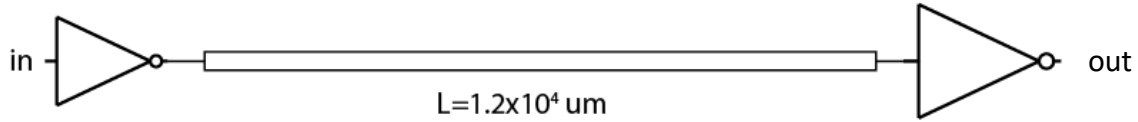
where  $R_n$  are resistors on the PATH from  $s$  to  $i$ , and  $C_m$  is the downstream capacitors for each  $R_n$  **on the path** from  $s$  to  $i$ .

$$\begin{aligned} \tau &= R_1(C_1 + C_2 + C_3 + C_4 + C_5) + R_3(C_3 + C_4 + C_5) + R_4C_3 \\ &= 1000 * (100 + 50 + 60 + 20 + 30) * 10^{-15} + 1500 * (60 + 20 + 30) * 10^{-15} \\ &\quad + 1800 * 60 * 10^{-15} = 5.33 * 10^{-10} s \end{aligned}$$

If the answer has an  $\ln(2)$  factor, it will also be accepted. i.e.  $3.69 * 10^{-10} s$  is also ok.

## Problem 2: Wires Aren't Just Lines

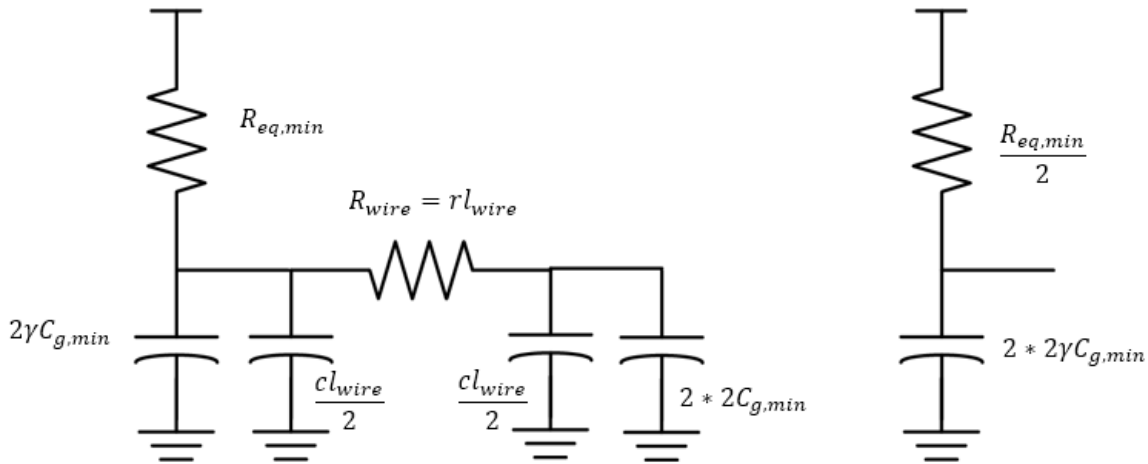
Assume we use a minimum sized inverter ( $C_{g,min} = 0.3fF$ ) to drive an inverter sized the twice of the first inverter (i.e. gate lengths are the same as the minimum inverter, but widths are doubled). The second inverter doesn't have any external load but only its own parasitic capacitance. There is a long piece of wire in between those two inverters and its delay cannot be ignored.



The intrinsic delay the first inverter,  $t_0 = \ln 2 * R_{eq,min} \gamma * 2C_{g,min}$  (notice this definition has  $\gamma$ ) is 4ps.  $\gamma = 1.5$  for this technology. The resistance and capacitance of this wire is  $r = 0.05\Omega/\mu m$  and  $c = 0.2fF/\mu m$ , respectively. The length of the wire is  $L = 1.2 * 10^4 \mu m$ .

- (a) What is the total delay,  $t$ , of this circuit (from input to the output)? Show your steps and write your final numerical answer.

The corrected way is to use the following Elmore delay model:



$$\ln(2) R_{eq} = \frac{4 * 10^{-12} s}{\gamma * 2 * 0.3 * 10^{-15} F} = 4444\Omega$$

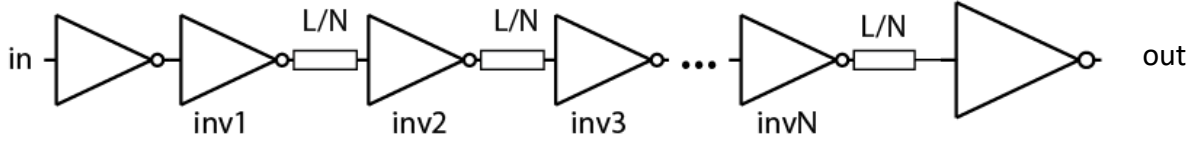
$$t = \ln 2 * R_{eq,min} \left( 2\gamma C_{g,min} + \frac{cl_{wire}}{2} * 2 + 4C_{g,min} \right) + \ln 2 * r l_{wire} \left( \frac{cl_{wire}}{2} + 4C_{g,min} \right) + \ln 2 * \frac{R_{eq,min}}{2} * 4\gamma C_{g,min}$$

$$\begin{aligned}
&= 4444 * \left( 2 * 1.5 * 0.3 * 10^{-15} + 0.2 * 10^{-15} * \frac{1.2 * 10^4}{2} * 2 + 4 * 0.3 * 10^{-15} \right) + \ln 2 * 0.05 \\
&\quad * \frac{1.2 * 10^4}{2} * \left( 0.2 * 10^{-15} * \frac{1.2 * 10^4}{2} + 4 * 0.3 * 10^{-15} \right) + \frac{4444}{2} * 4 * 1.5 * 0.3 \\
&\quad * 10^{-15} \\
&= 4444 * 2.4021 * 10^{-12} + 207.944 * 1.2012 * 10^{-12} + 4 * 10^{-12}
\end{aligned}$$

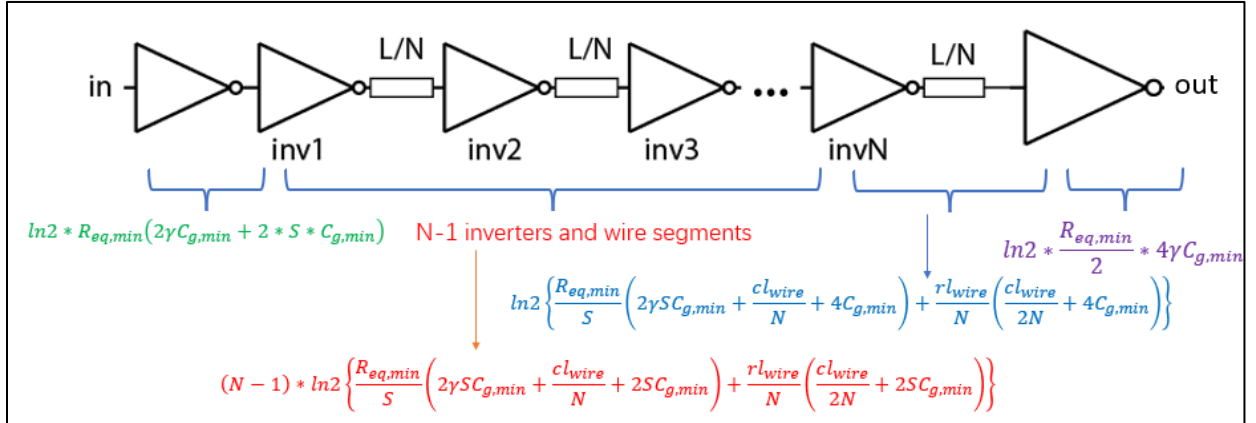
$$\cong 1.093 * 10^{-8} s \text{ or } 10.93 \text{ ns}$$

If the answer is missing  $\ln(2)$ , i.e. if the answer is  $1.58 * 10^{-8} s$ , lose one point

- (b) Now we are breaking up the wire into N equal segments and insert N identically sized inverters to achieve lower delay (there is no wire between the original first inverter and the inv1 we insert). If we cannot ignore the delay due to the inverters, what is the new total delay (in terms of N and the size of these inverters, S, and parameters given above. No need to write the numerical values.)



Using the similar Elmore model like above, the answer will be:



$$t = \ln 2 * R_{eq,min} (2\gamma C_{g,min} + 2 * S * C_{g,min})$$

$$+ (N-1) * \ln 2 \left\{ \frac{R_{eq,min}}{S} \left( 2\gamma S C_{g,min} + \frac{cl_{wire}}{N} + 2S C_{g,min} \right) + \frac{rl_{wire}}{N} \left( \frac{cl_{wire}}{2N} + 2S C_{g,min} \right) \right\}$$

$$+ \ln 2 \left\{ \frac{R_{eq,min}}{S} \left( 2\gamma S C_{g,min} + \frac{cl_{wire}}{N} + 4C_{g,min} \right) + \frac{rl_{wire}}{N} \left( \frac{cl_{wire}}{2N} + 4C_{g,min} \right) \right\}$$

$$+ \ln 2 * \frac{R_{eq,min}}{2} * 4\gamma C_{g,min}$$

- (c) **Optional Part** (this subpart won't be graded): People have found that, if the delay introduced by one inverter is equal to  $\ln 2 * R_{eq,min} \gamma 2C_{g,min}$ , then the minimum delay of inverter+wire segments is achieved when the number of stage, N, satisfies the following equation:

$$\frac{L}{N} = \sqrt{\frac{2R_{eq,min}2C_{g,min}(1 + \gamma)}{rc}}$$

If we use this conclusion, what would be the  $N_{optimum}$  for (b)?

(NOT GRADED)

$$\begin{aligned} N_{optimum} &\cong \sqrt{\frac{rcl^2}{2R_{eq,min}2C_{g,min}(1 + \gamma)}} \\ &= \sqrt{\frac{0.05 * 0.2 * 10^{-15} * (1.2 * 10^4)^2}{4 * \frac{4444}{\ln 2} * 0.3 * 10^{-15} (1 + 1.5)}} \cong 9 \text{ segments} \end{aligned}$$