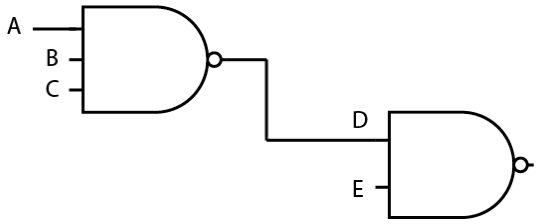
EECS 151/251A Homework 6

Due Friday, April 1st, 2022

Problem 1: Not So Much Effort

Consider a NAND3 gate that drives one of the input of a NAND2 gate:



For this problem, assume you have a reference inverter with $W_P = W_N = 1$ and $R_p = R_n = R_{eq}$. This technology has $\gamma \equiv \frac{C_d}{C_g} = 1.5$.

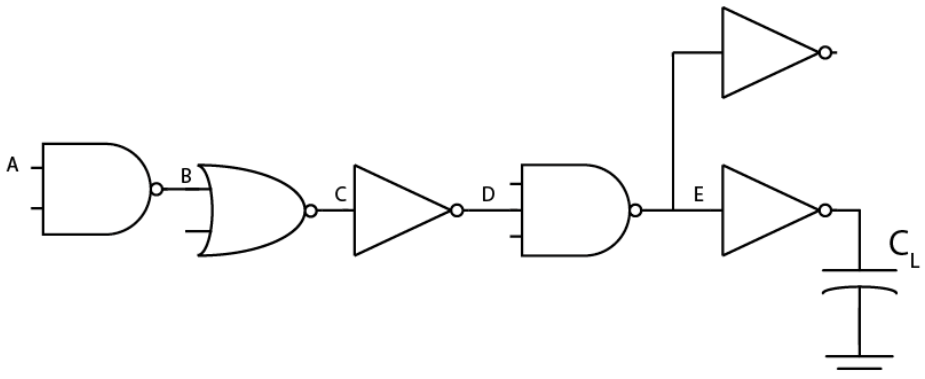
(a) Assume PMOS has unit size ("1"). Draw the transistor-level schematic for the circuit above and size all the NMOS transistors such that the equivalent delay of each gate without load is the same as a reference inverter.

(b) What is the Logical Effort of each gate? Show your steps.

(c) Now let the second NAND gate drive a load C_L. Assume the PMOS of the reference inverter has gate capacitance C_g. Write the delay from A to the output driving C_L.

Problem 2: More Effort

Consider the following multi-stage network. The two inverters in the last stage are identical.



Again, assume you have a reference inverter with $W_P = W_N = 1$ and $R_p = R_n = R_{eq}$. This technology has $\gamma \equiv \frac{C_d}{C_g} = 1.5$.

(a) The input capacitance of A is C_{in} and the load $C_L = 48 * C_{in}$. Determine the path effort from A to the output load C_L.

(b) Determine the optimum stage effort (SE) that results in minimum delay.

(c) Express the minimum delay in terms of the intrinsic delay of the reference inverter, τ_{inv}.

(d) Based on your answers above, find the optimum input capacitance of the gates of each stage on the critical path.