

inst.eecs.berkeley.edu/~eecs151

# EECS151 : Introduction to Digital Design and ICs

## Lecture 27 – Chips, Summary

**Bora Nikolić**



### Lotfi Zadeh

**Lotfi Aliasker Zadeh** (February 1921 – 6 September 2017)<sup>[1][2]</sup> was a mathematician, computer scientist, electrical engineer, artificial intelligence researcher, and professor<sup>[2]</sup> of [computer science](#) at the [University of California, Berkeley](#). Zadeh is best known for proposing [fuzzy mathematics](#), consisting of several fuzzy-related concepts: [fuzzy sets](#),<sup>[3]</sup> [fuzzy logic](#),<sup>[3]</sup> fuzzy algorithms,<sup>[10]</sup> fuzzy semantics,<sup>[11]</sup> fuzzy languages,<sup>[12]</sup> [fuzzy control](#),<sup>[13]</sup> [fuzzy systems](#),<sup>[14]</sup> fuzzy probabilities,<sup>[15]</sup> fuzzy events,<sup>[15]</sup> and fuzzy information.<sup>[16]</sup> Zadeh was a founding member of the [Eurasian Academy](#).<sup>[17]</sup>

[Wikipedia](#)



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## Review

- Flash
  - Single-level vs multi-level
  - Read and Write Flash Cell
  - NAND vs NOR
- NVRAM
- CAM
- Parallelism for higher performance and lower power

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## Chip Packaging, I/O

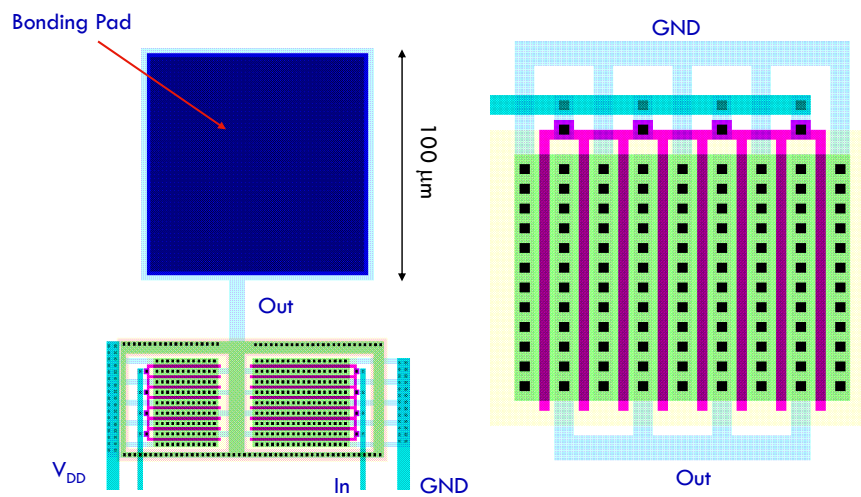
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## Bonding Pad Design



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## ESD Protection

- When a chip is being connected to a board, there is unknown (potentially large) static voltage difference
- Equalizing potentials requires (large) charge flow through the pads
- Diodes sink this charge into the substrate – need guard rings to pick it up.

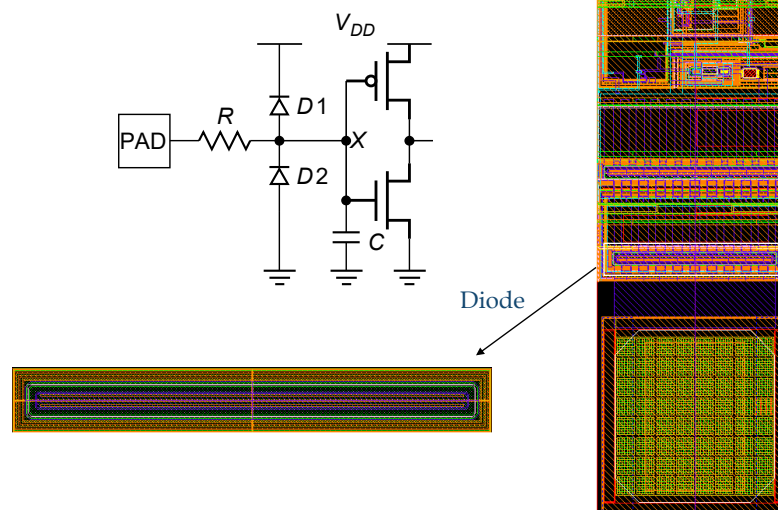
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## ESD Protection



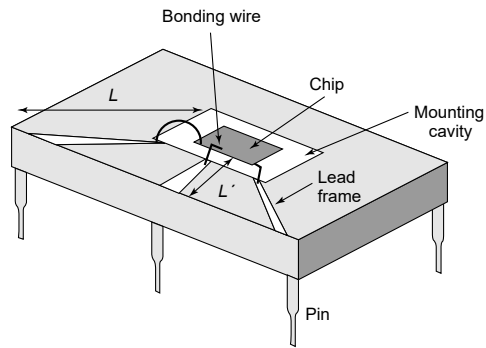
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## Chip Packaging



- Bond wires ( $\sim 20\mu\text{m}$ ) are used to connect the package to the chip

- Pads are arranged in a frame around the chip

- Pads are relatively large  $\sim 20\text{-}100\mu\text{m}$  ( $40\text{-}200\mu\text{m}$  pitch)

- Many chips areas are 'pad limited'

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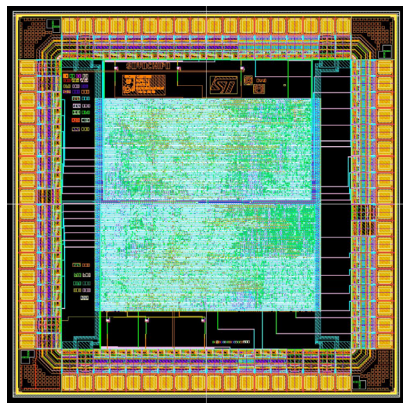
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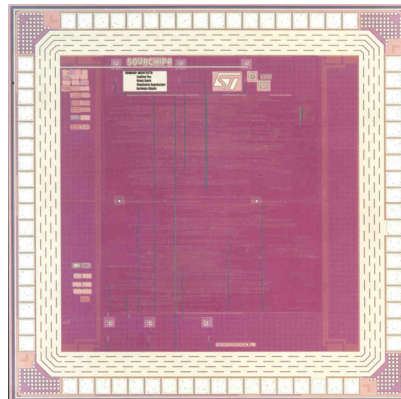
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## Pad Frame

Layout



Die Photo



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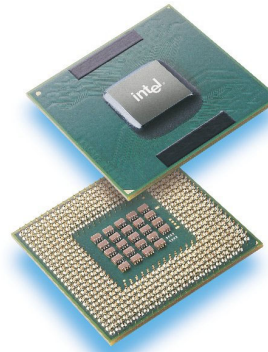
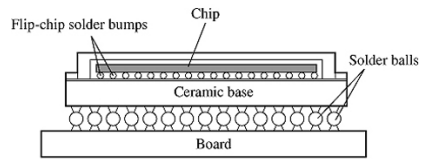
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## Chip Packaging

- Most modern chips are 'flip-chip' packaged
  - Pads are distributed around the chip
  - The soldering balls are placed on pads
  - The chip is 'flipped' onto the package
  - Can have many more pads



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## Supply Distribution

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## Impact of Resistance

- Impact of resistance is commonly seen in power supply distribution:
  - IR drop
  - Voltage variations
- Power supply is distributed to minimize the IR drop and compensate for the inductances

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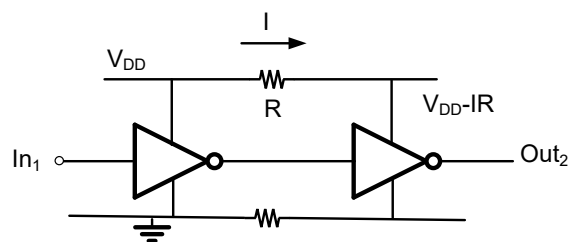
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## RI Introduced Voltage Drop and Noise

- Supply current:
  - Average
  - Time varying component, depends on activity



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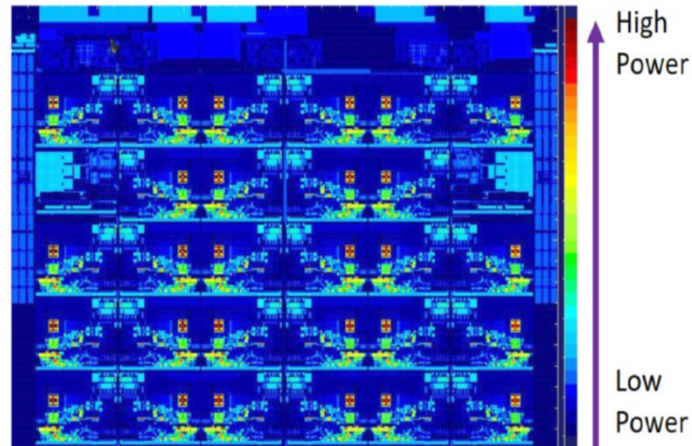


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## Resistance and the Power Distribution Problem

- Intel Skylake-SP power map
  - Power draw varies a lot across the die



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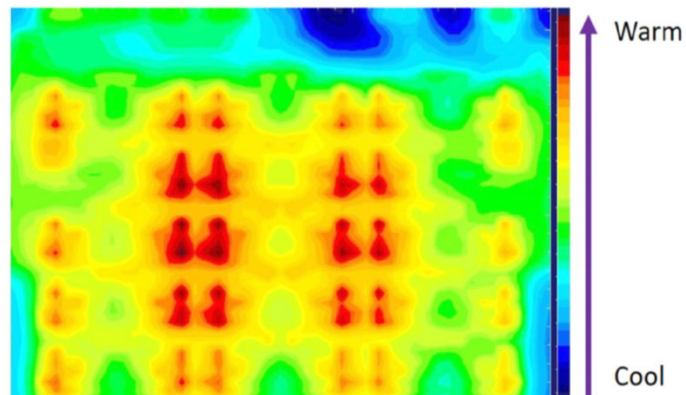
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## Power Converts to Heat

- Intel Skylake-SP thermal map
  - Temperature varies across the die
  - Leakage strongly depends on temperature



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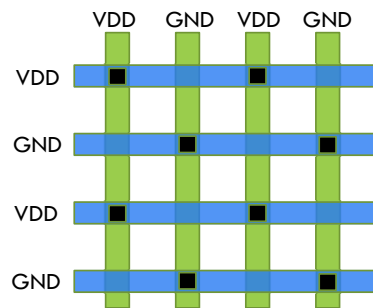
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## Power Distribution

- Low-level distribution is in Metal 1/2
- Power has to be 'strapped' in higher layers of metal.
- The spacing is set by IR drop, electromigration, inductive effects
- Always use multiple contacts on straps



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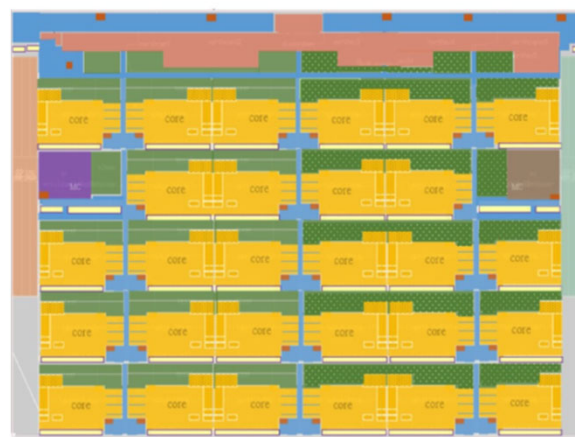
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## Modern Example: Intel Skylake-SP

- Many power domains



- Vcc: core supply (per core)
- Vccclm: Un-core supply
- Vccsa: System Agent supply
- Vccio: Infrastructure supply
- Vccsfr: PLL supply
- Vccddrd: DDR logic supply
- Vccddra: DDR I/O supply

- 9 primary VCC domains are partitioned into 35 VCC planes

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S.Tam, ISSCC'18

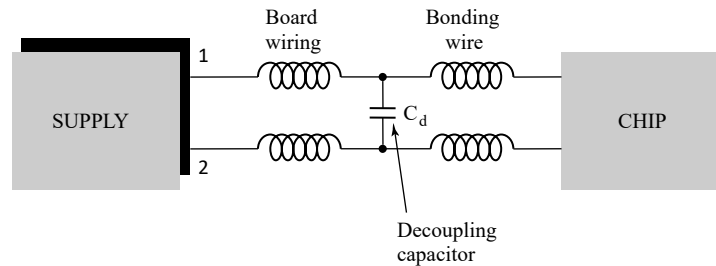
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## Decoupling Capacitors



### Decoupling capacitors are added:

- ☐ On the board (right under the supply pins)
- ☐ On the chip (under the supply straps, near large buffers)

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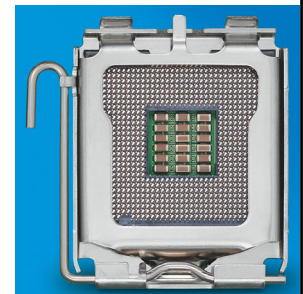
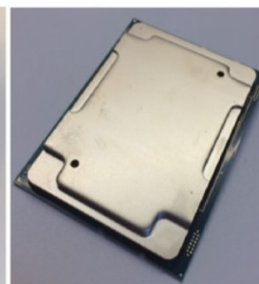
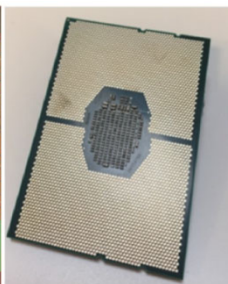
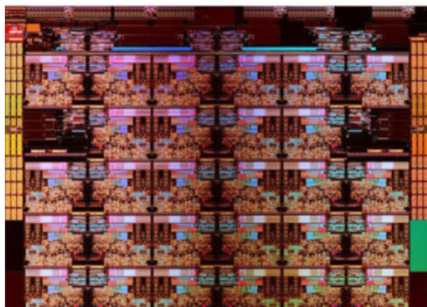
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## Decoupling Capacitors

- Under the die



- Intel Skylake-SP

- Intel Pentium 4 socket

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## Administrivia

- Special lecture on Monday, Dec 6. at 11:00am
  - FPGA prototyping
  - Not on final, but very useful
- Project, project, project !
  - Final checkoffs on Dec. 7
- Homework 11 due Dec 3.
- Final is on December 13, 11:30-2:30
  - Review session next Wednesday



This Class

## What This Class is All About?

- **Introduction to digital integrated circuit and system engineering**
  - Key concepts needed to be a good digital system designer
  - Discover your own creativity!
- **Learn models that allow reasoning about design behavior**
  - Manage design complexity through abstraction and understanding of tools
  - Allow analysis and optimization of the circuit's performance, power, cost, etc.
- **Learn how to make sure your circuit and system works**
  - *There are way more ways to mess up a chip than to get it right.*

**Learn by doing!**

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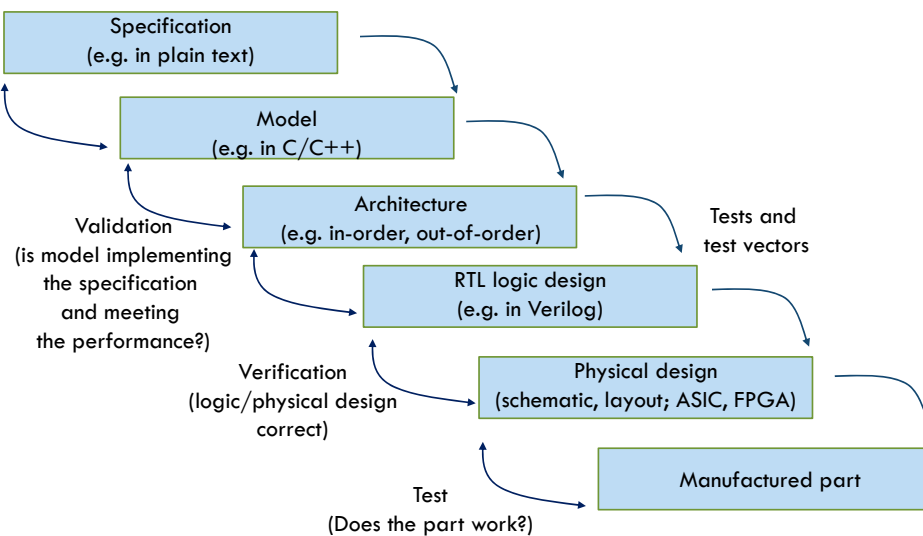
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## Design Process

- Design through layers of abstractions



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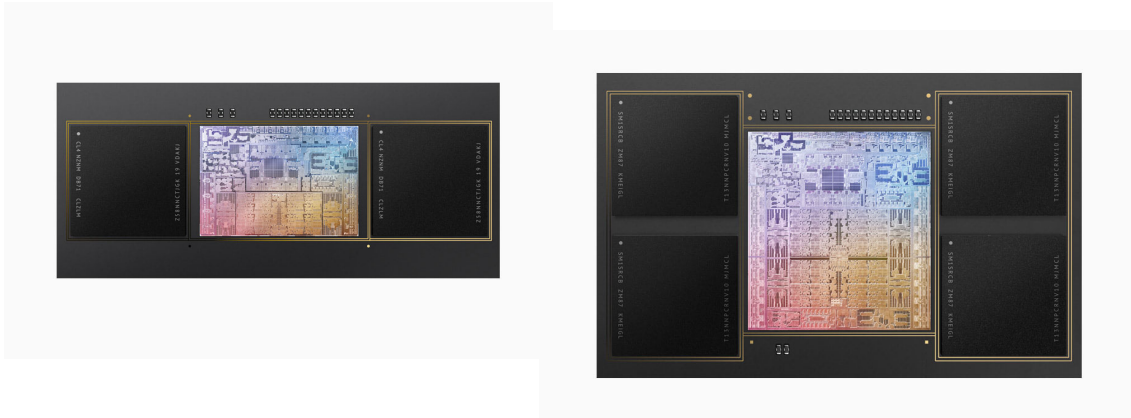
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## Field Has Advanced

- Apple M1Pro and M1Max



<https://www.apple.com/newsroom/2021/10/introducing-m1-pro-chips-apple-has-ever-built/>

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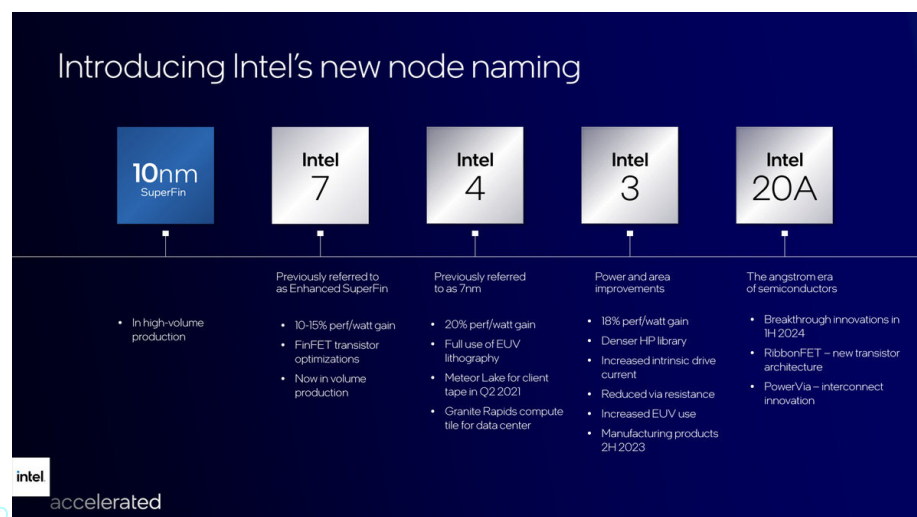
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## Field Has Advanced

- Intel's roadmap to 18A



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To Probe Further

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## CS152/252 – Computer Architecture and Engineering

- Some have taken before EECS151
  - Taught only in Spring
- (More) advanced topics in computer architecture: Superscalar, out-of-order machines, vectors, GPUs, multithreading, memory hierarchy

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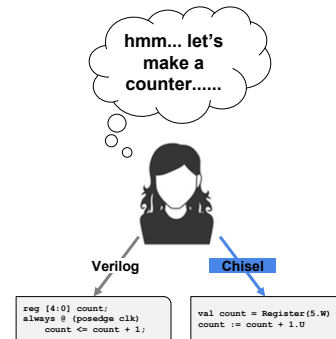
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## Digital Systems/Computer Architecture Research

- Exploring new areas by using high productivity design

- Language: Chisel
- Same control over RTL as Verilog
- Higher software abstraction level
  - Powerful parameterization, functional and object-oriented programming, static typing
  - Huge base of existing software libraries



<https://www.chisel-lang.org/>

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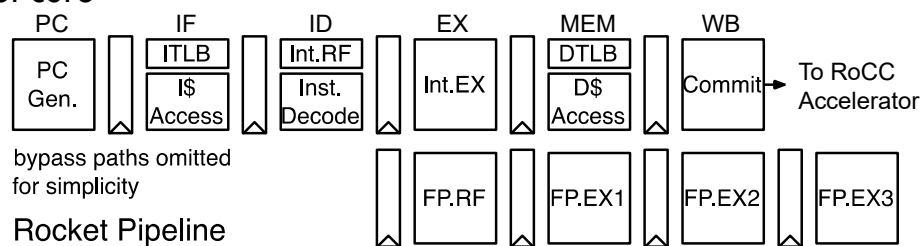
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## RISC-V Rocket and BOOM

- Rocket core



- 64-bit 5-stage single-issue in-order pipeline
- Design minimizes impact of long clock-to-output delays of compiler-generated RAMs
- 64-entry BTB, 256-entry BHT, 2-entry RAS (parameterized)
- MMU supports page-based virtual memory
- IEEE 754-2008-compliant FPU
  - Supports SP, DP FMA with hw support for subnormals

<https://github.com/chipsalliance/rocket-chip>

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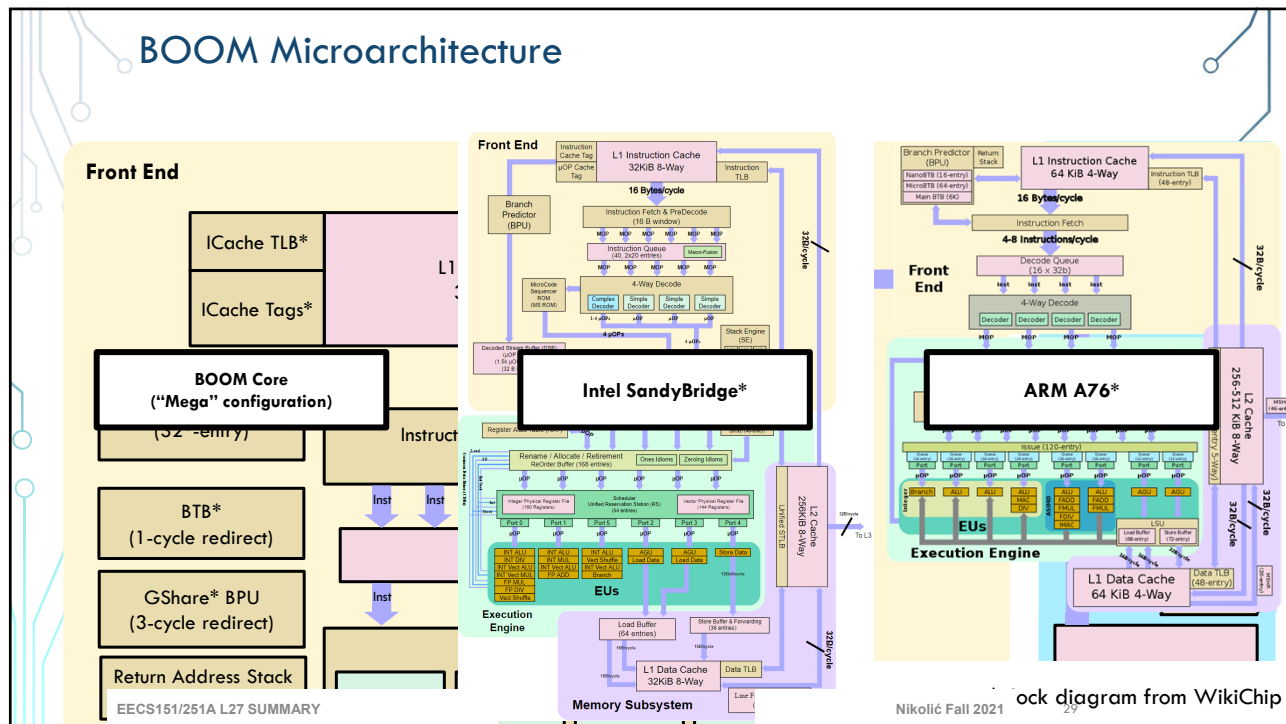
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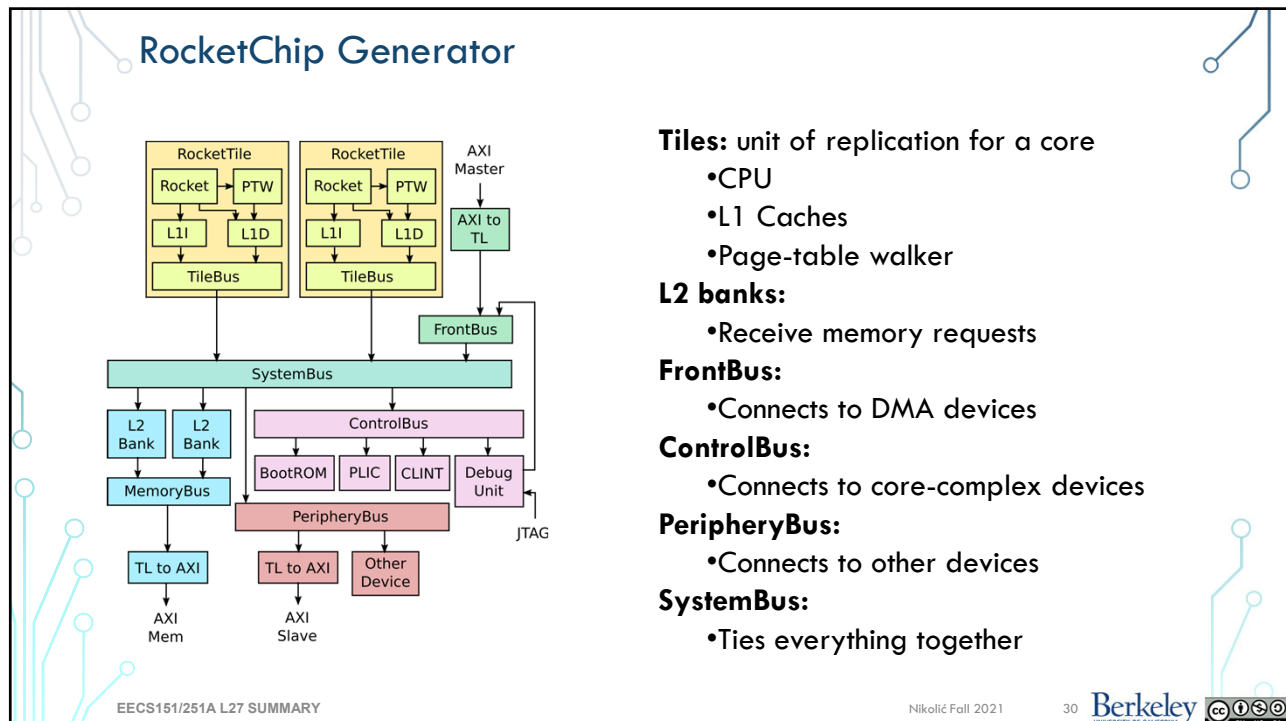


## BOOM Microarchitecture



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## RocketChip Generator



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## Building Complete SoCs

- Design and simulate complete prototype systems



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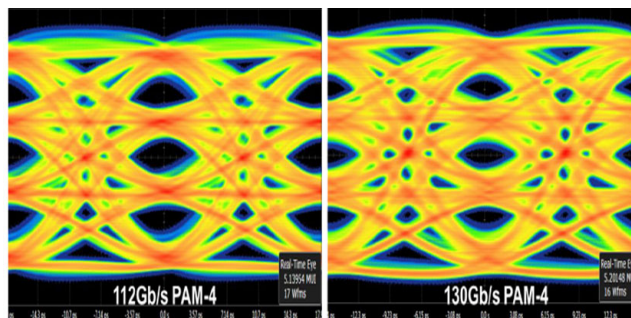
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## High-Speed I/O

- 28Gb/s → 56Gb/s → 112Gb/s → 224Gb/s → Optical ?



TSMC, IEDM'19

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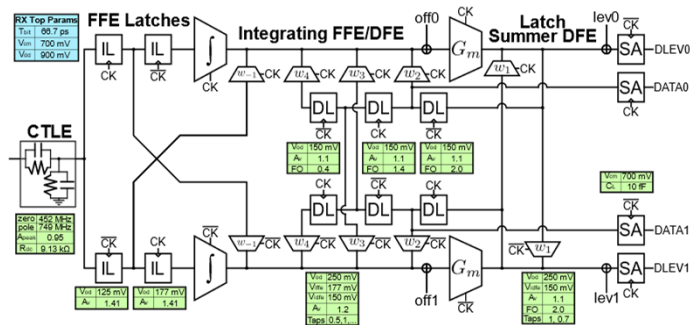
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## We Have a Generator For That, Too!

- But it is mostly analog
- Designed as a Berkeley Analog Generator (BAG)



- Deeper prerequisite chain
- EE105 → EE140/240A → EE240C or 290C (high-speed links)

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## EE251B – Advanced Digital Circuits

- Starts with a deeper dive into technology, devices and models
- SoC architecture, interconnect
- Variability and a case study of large SRAM arrays
- Most of the class is low-power design and power management
- ASIC projects
- Pending campus approval

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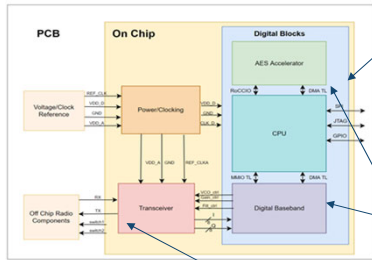
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## EE194/290 – Advanced Topics Classes

- **Spring'22 Tapeout class (+ testing class, Fall'22)**



Berkeley Analog Generator  
(BAG) - generated SAR  
ADC

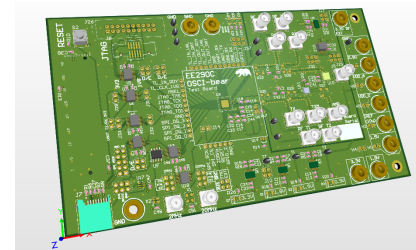
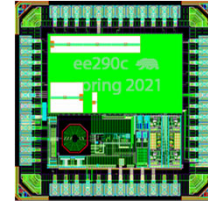


<https://github.com/ucb-bar/chipyard>  
Processor core, interfaces  
Software tools



<https://www.chisel-lang.org/>  
Custom BLE digital baseband,  
accelerator wrappers

1mm x 1mm in 28nm



- **Spring'22 class will use Intel 16**
  - Organizational meeting next Friday
  - Compute accounts, NDAs for technology access

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## Summary

- We accomplished a lot in this class
  - We hope changes we made were seamless
  - Worked nearly as hard as you did ☺
- We had a ton of fun
- And hope you had too!

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