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EECS151 : Introduction to Digital Design and ICs

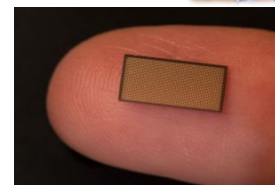
Lecture 11 – CMOS

Bora Nikolić



Intel Unveils Second-Generation Neuromorphic Chip

October 5, 2021, Intel has unveiled its second-generation neuromorphic computing chip, Loihi 2, the first chip to be built on its Intel 4 process technology. Designed for research into cutting-edge neuromorphic neural networks, Loihi 2 brings a range of improvements. They include a new instruction set for neurons that provides more programmability, allowing spikes to have integer values beyond just 1 and 0, and the ability to scale into three-dimensional meshes of chips for larger systems.



Intel's Loihi 2 second-generation neuromorphic processor. (Source: Intel)

EETimes

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Review

- Core FPGA building blocks:
 - Configurable Logic Blocks (CLBs)
 - Configurable Interconnect
 - Switch boxes
- Modern FPGA Designs:
 - BRAMs, DSPs, and AI Engines
- CMOS process is used for producing chips
 - Planar bulk process used up to 28nm node
 - finFET and FDSOI used below the 22nm node

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MOS Transistors

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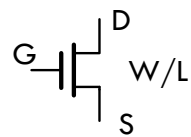
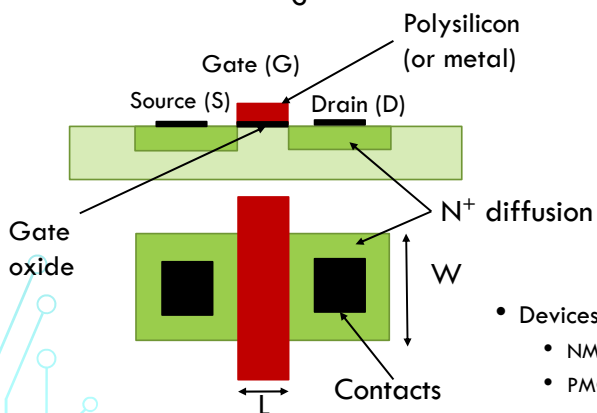
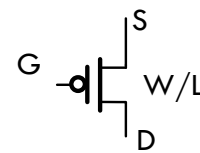
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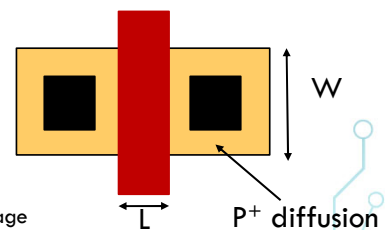
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MOS Transistors

• Symbol

 N-type
NMOS

 P-type
PMOS


- Devices are symmetrical
 - NMOS: Drain is at higher voltage
 - PMOS: Source is at higher voltage



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Different Kinds of MOS Transistors

- Planar bulk CMOS

N-type NMOS

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- FinFET

W is discrete!

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Transistor Dimensions are Quantized

- FinFET widths are discrete ($W = kW_{\text{unit}}$)
 - k is an integer
- Lengths are quantized because of lithography
 - Also are quantized lower metal layers, contacts...

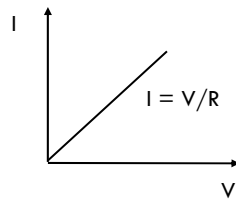
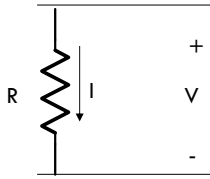
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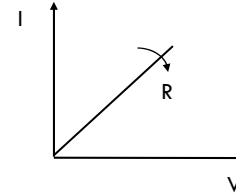
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Ohm's Law

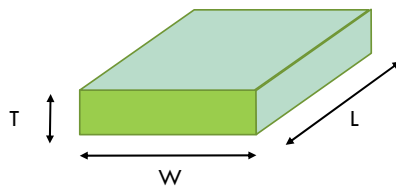
- Resistors



- Variable resistors



- Physical resistors



$$R = \rho \frac{L}{TW}$$

- In a planar process, designer controls W and L

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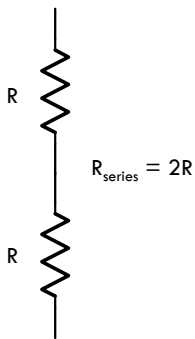
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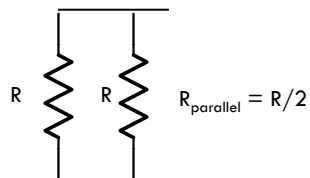
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Series and Parallel

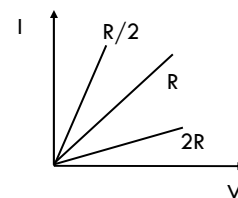
- With two identical resistors, R



Equivalent to doubling
length



Equivalent to doubling
width



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An n-Channel MOS Transistor

Polysilicon gate, dielectric, and substrate form a capacitor.

When $V_{GS} < V_{Th}$ transistor is off

$V_D = 0V$, $V_G = 0V$, $V_S = 0V$, $I = 0$

$V_D > 0$, $V_G = 0V$, $V_S = 0V$, $I > 0$

$V_{DS} > 0$, transistor leaks $I_{DS} \sim nA$

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An n-Channel MOS Transistor

When $V_{GS} < V_{Th}$ transistor is off

$V_D = 0V$, $V_G = 0V$, $V_S = 0V$, $I = 0$

$V_D > 0$, $V_G > V_{Th}$, $V_S = 0V$, $I > 0$

$V_G > V_{Th}$, small region near the surface turns from p-type to n-type.

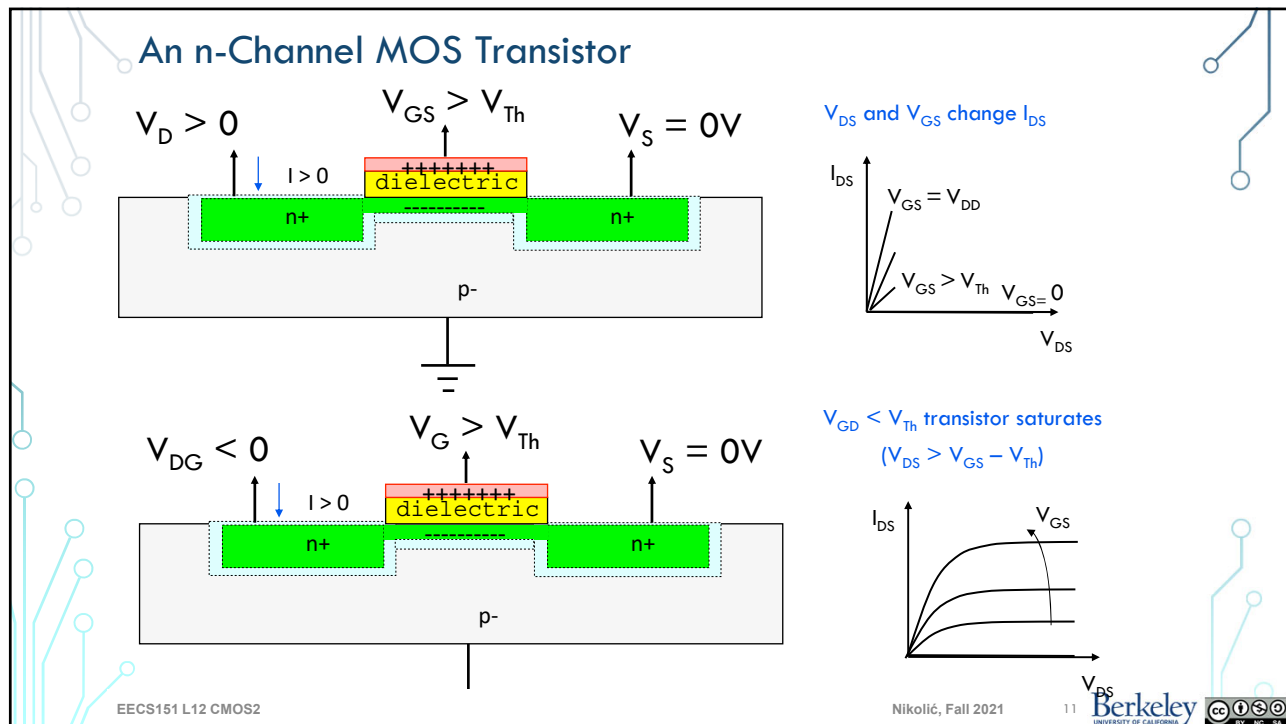
nFet is on.
Current is proportional to V_{DS}

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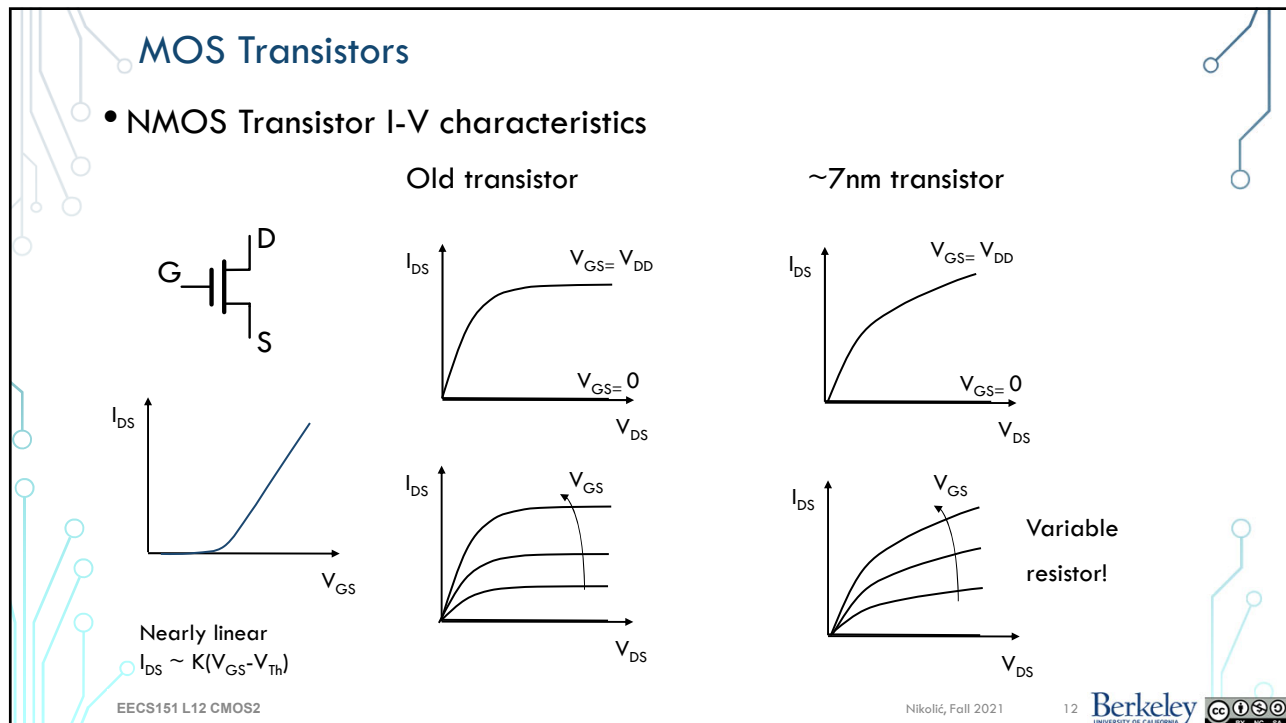
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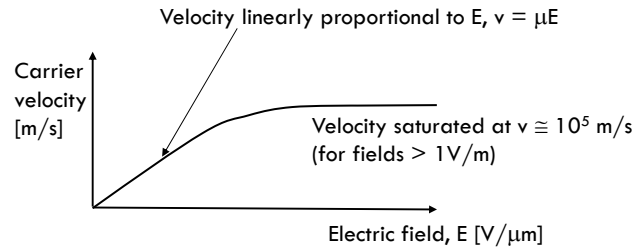
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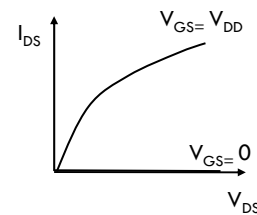
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Velocity Saturation

- Carrier velocity in the channel saturates



- All submicron transistors are velocity saturated
- Other effects (drain-induced barrier lowering) cause I_{DS} to increase in saturation



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Administrivia

- Homework 5 will be posted later this week, due next week
- No lab this week
 - Lab 6 (last) after the midterm
- Midterm 1 on October 7, 7-8:30pm
 - You will be assigned a classroom
 - One double-sided page of notes allowed
 - Material includes FPGAs

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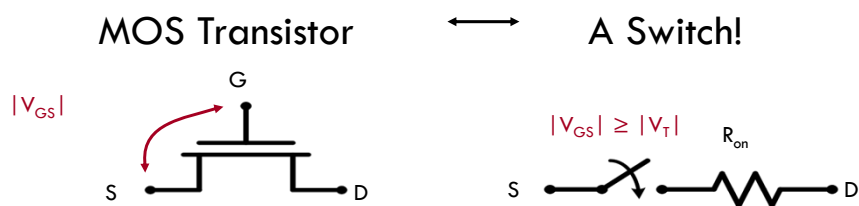
MOS Transistor as a Switch

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MOS Transistor as a Resistive Switch

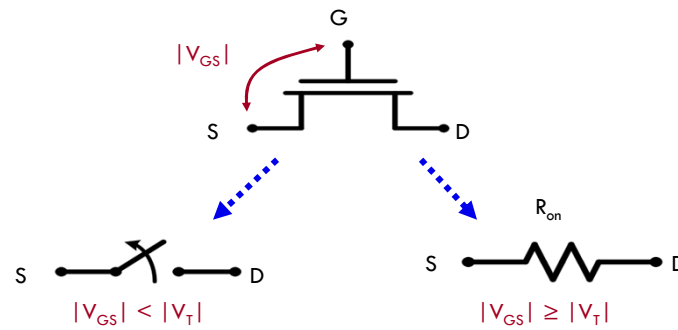


- V_{GS} controls the switch
- (it also charges the channel capacitor)

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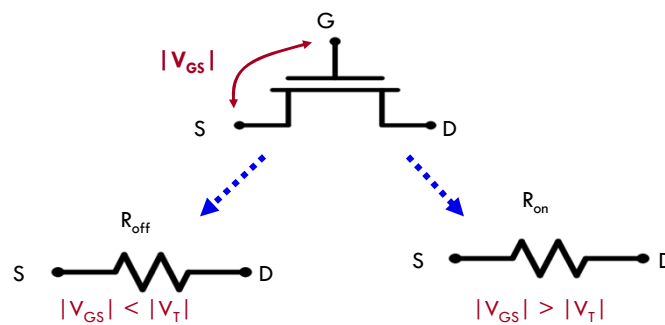
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ON/OFF Switch Model of MOS Transistor



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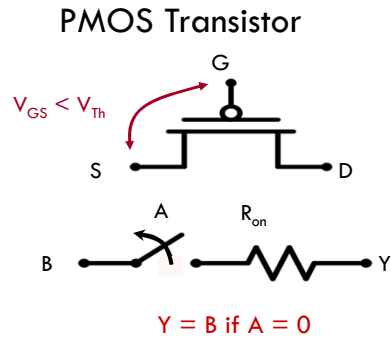
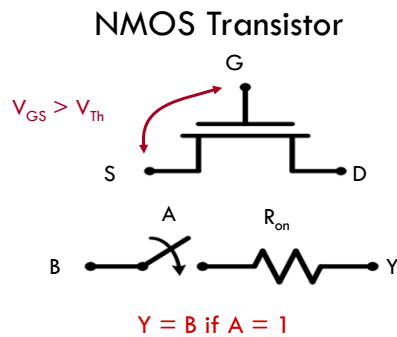
A More Realistic Model



- It is a dimmer!

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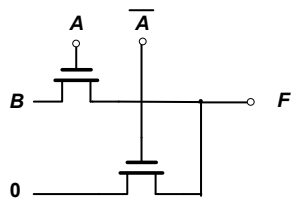
A Logic Perspective



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AND and OR

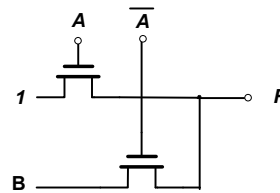
• AND



$$F = AB$$

$$(F = AB + \bar{A} \cdot 0)$$

• OR



$$F = A+B$$

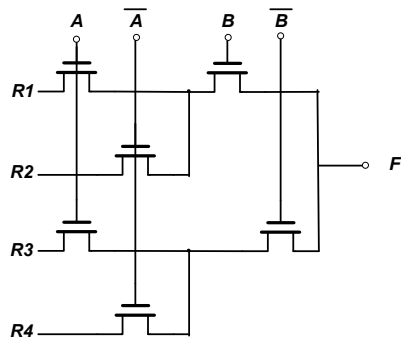
$$(F = A \cdot 1 + \bar{A}B)$$

- Keep in mind – single NMOS/PMOS transistors are imperfect switches!
 - Turns off when $|V_{GS}| = |V_{Th}|$

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Peer Instruction

- Switch logic
- Which combination of inputs implements $F = AB$?



	R1	R2	R3	R4
a)	1	X	X	X
b)	0	X	X	X
c)	1	0	0	0
d)	1	1	1	0
e)	1	1	1	1
f)	None of the above			

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Summary

- CMOS process is used for producing chips
 - Planar bulk process used up to 28nm node
 - finFET, FDSOI used below the 22nm node

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