

EECS 151/251A

Discussion 12

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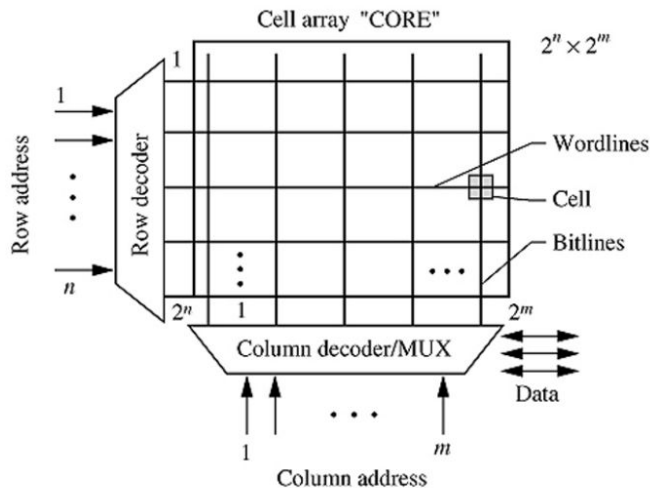
Agenda

- SRAMs
 - Architecture
 - 6T SRAM Read
 - 6T SRAM Write
 - Multi-Voltage SRAM
- Memory decoding
 - Design example

SRAMs

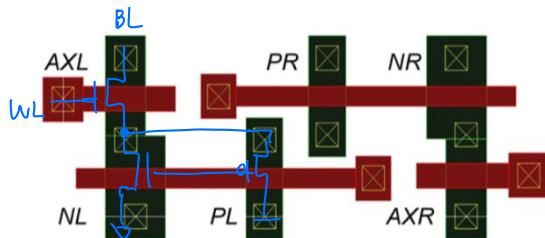
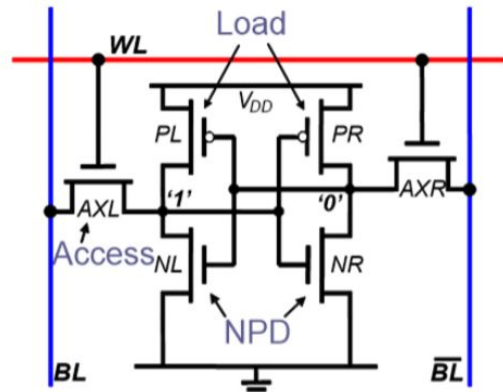
SRAM Architecture

- Grid of SRAM bitcells: $1:1$
○ width = word size $2:1$ aspect ratio
○ height = # of words
- **Bitlines** (vertical) are shared across cells in a column
 - Long wires with a large capacitive load (drains of access transistors, read/write circuits)
- **Wordlines** (horizontal) are shared across cells in a row
 - Also long with large capacitive load (gates of access transistors)
- Peripheral circuitry (bitline drivers, sense amp, decoders)
 - Need to reduce the total number of pins, $N+M$ address lines for 2^{N+M}
 - Ex: if $N+M=20 \rightarrow 2^{20} = 1 \text{ Mb}$



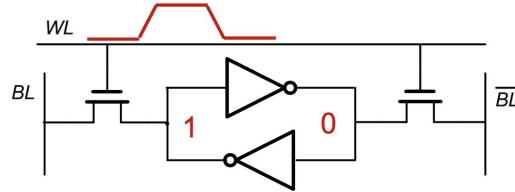
The 6T SRAM Cell

- Inverters (PL NL and PR NR)
 - in positive feedback form the memory element (like a latch!)
- AXL and AXR are the access transistors
 - Allow the bitlines to access the memory nodes (Q, Qbar) when WL = 1
- Only 1 WL in an SRAM array is active at a time
 - Addresses an entire row of SRAM cells
- Bitlines are controlled differently for read and write

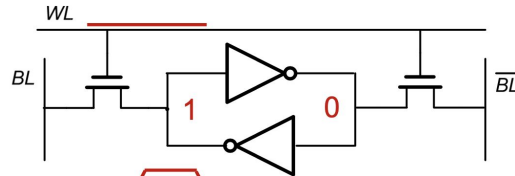


6T SRAM Cell: 3 Modes of Operation

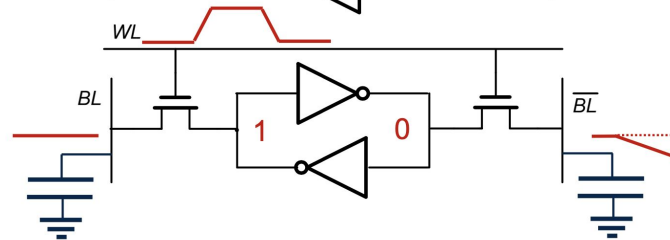
Write



Retention



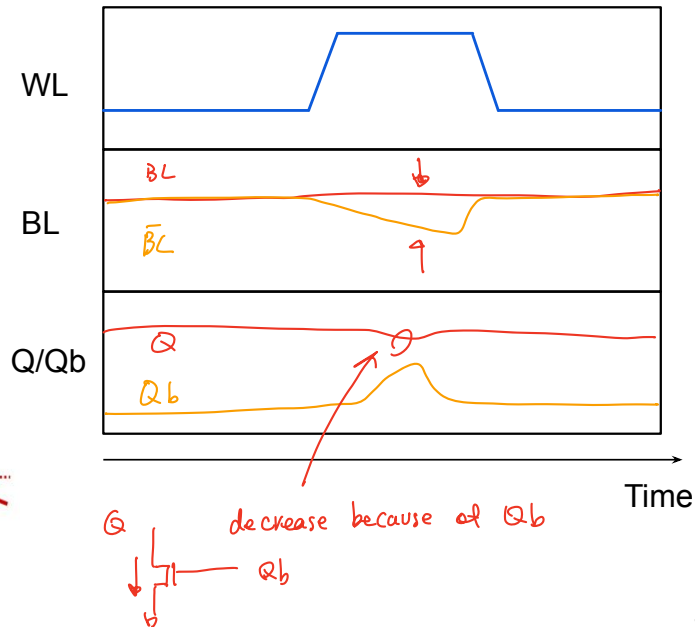
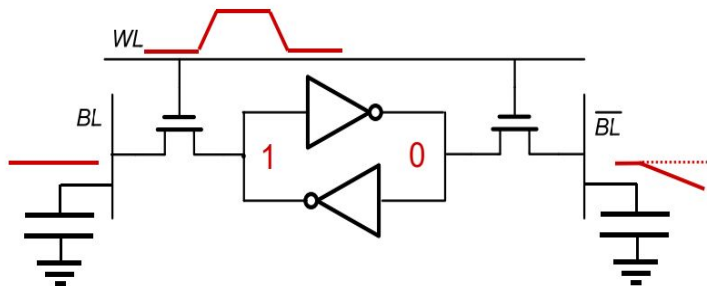
Read



SRAM Read Operation

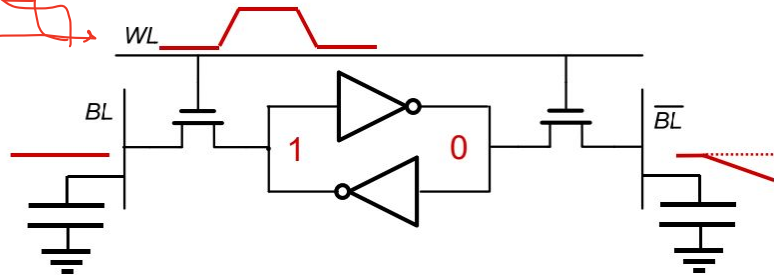
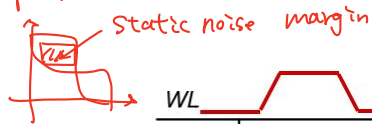
- Procedure:

- Precharge BL and BLbar to VDD
- Raise WL
- Sense dip on one bitline with sense amp
- Lower WL
- Discharge bitlines

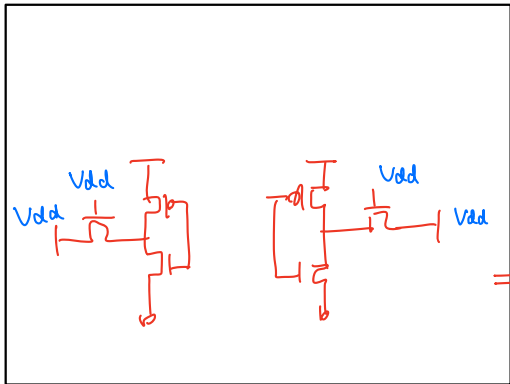


SRAM Read Stability

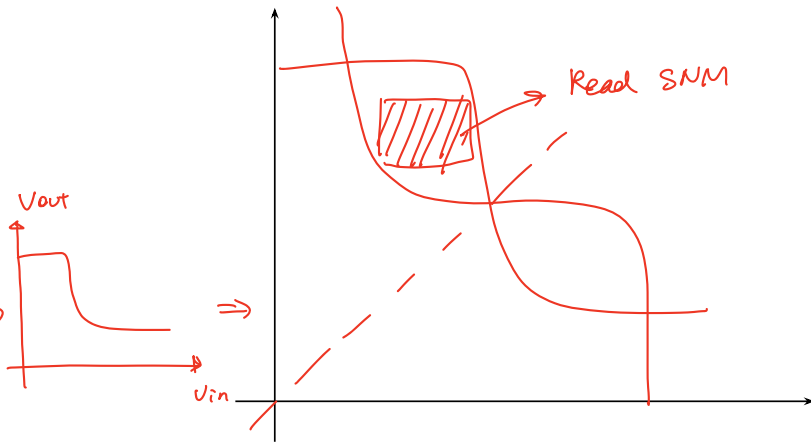
For cross-coupled INV



- Read stability = reading doesn't corrupt the value stored in Q and Qbar
 - The access transistor shouldn't overpower the node storing a '0' and flip its state
 - Sizing: make the latch NMOS stronger than the access transistor = ($W_n > W_{\text{access}}$)



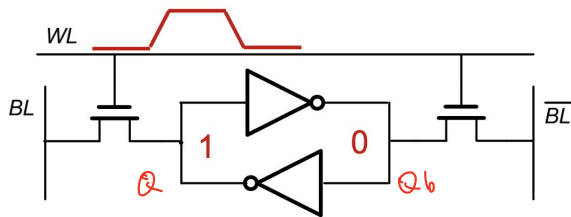
Equivalent Circuit



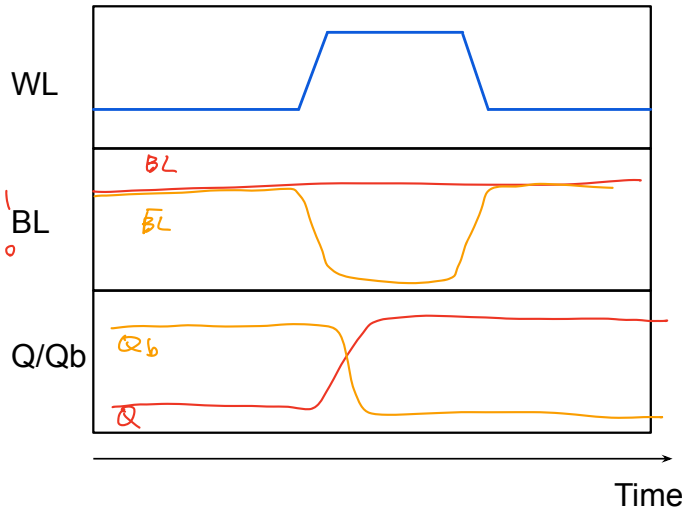
Read SNM

SRAM Write Operation

- Procedure:
 - Drive BL and BLbar with data to write
 - Raise WL
 - Wait some amount of time (write time)
 - Lower WL
 - Discharge bitlines

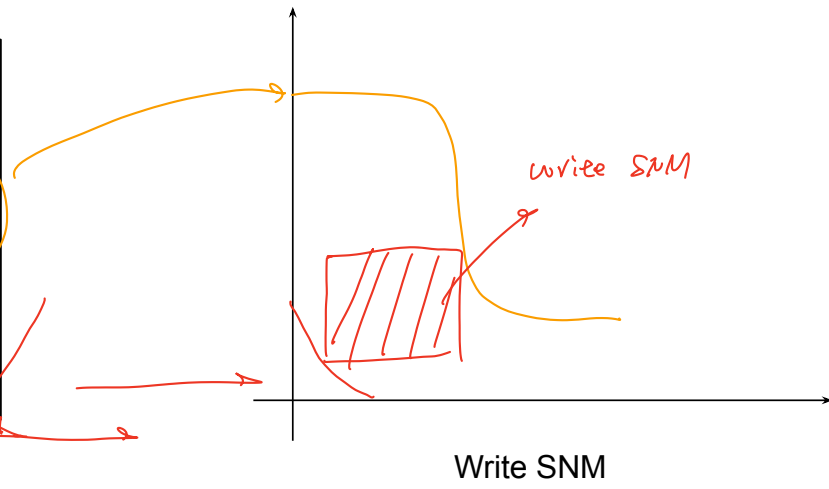
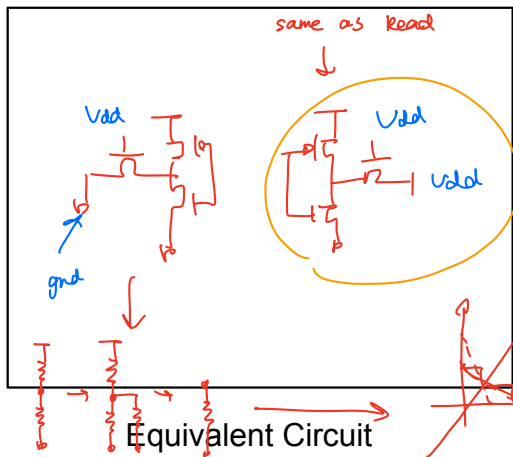
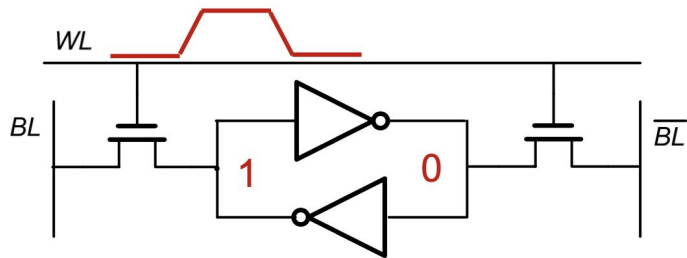


assume $Q: 0 \rightarrow 1$
 $Q_b: 1 \rightarrow 0$



SRAM Write

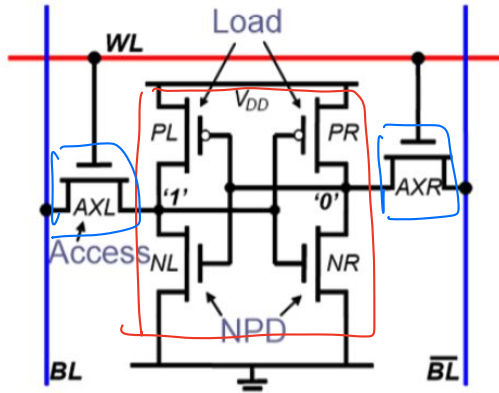
- Write-ability = the cell's memory value can be changed
 - Access transistor must overpower latch
 - Assuming the cell is read stable ($W_n > W_{\text{access}}$), the node with '0' can't be overpowered \Rightarrow so we *must* overpower PMOS ($W_{\text{access}} > W_p$) and override the '1' node



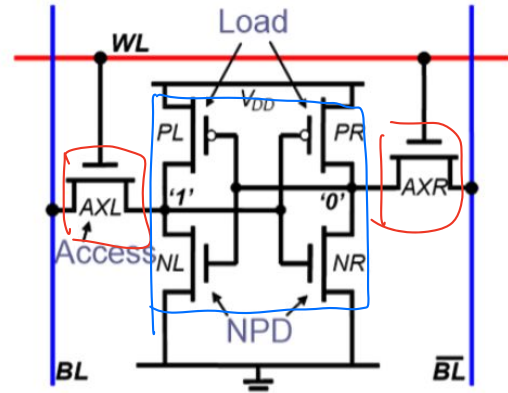
Conflicts between read and write

Size 6T the SRAM cell for optimized read and write operation separately:

 Small
 Large



Read optimized



Write optimized

different supply :

V_{dd-BL} V_{ss-BL}

V_{dd-WL}

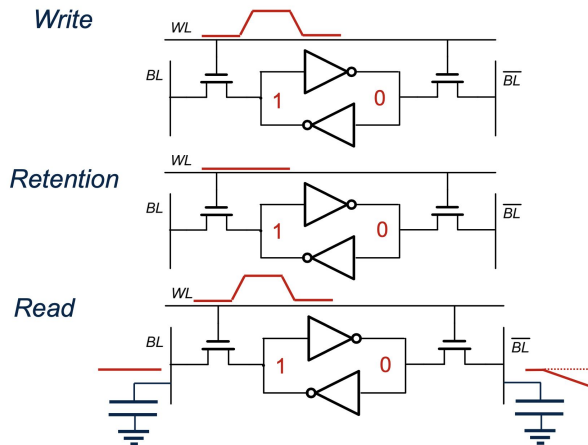
V_{dd-inv} V_{ss-inv}

Multi-Voltage SRAM

You have 3 high voltage levels to choose: 0.9V, 1.0V(ref), 1.1V;

3 low voltages: -0.1V, 0V(ref), 0.1V

Which voltage is preferred?



Read speed

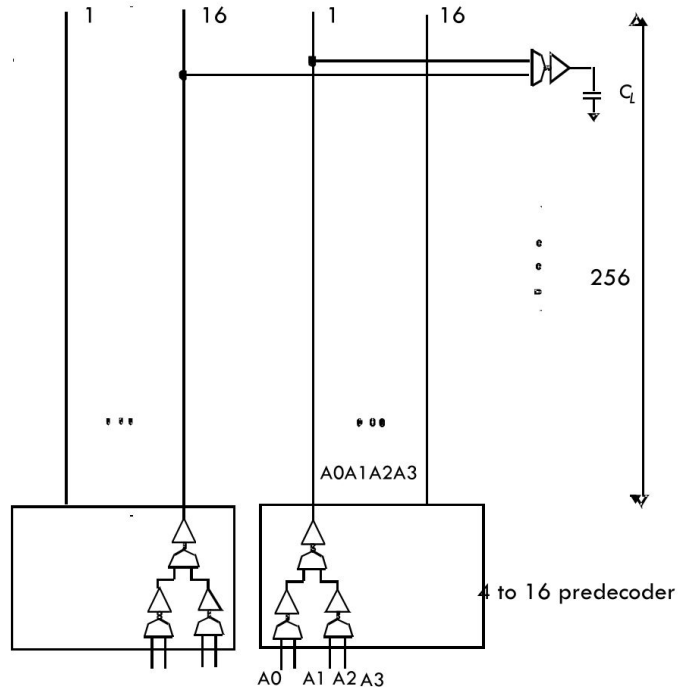
*stability
during reading*

	Readability.	Read Stability	Writability
WL	1.1V	0.9V	1.1V
BL	don't care	0.9V	1.1V / -0.1V
VDD	1.1V	1.1V	0.9V
GND	-0.1V	-0.1V	0.1V

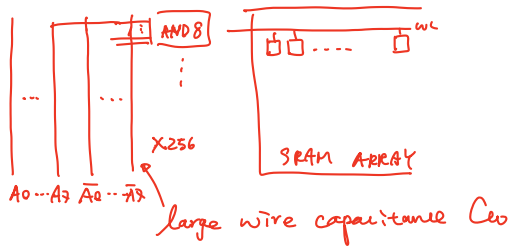
Memory Decoders

2-Stage Decoding

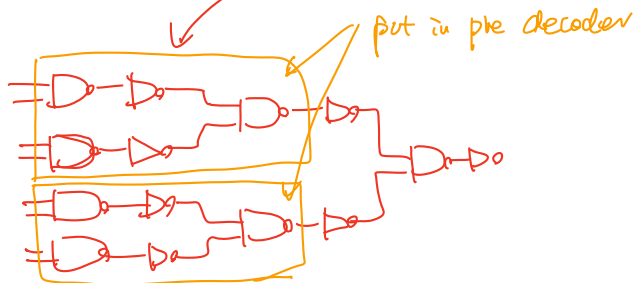
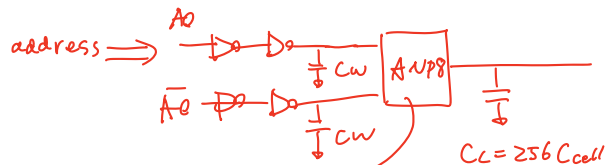
- Problem: each distinct address => 1 WL
 - Binary-to-thermometer conversion!
 - Naive method: each WL has its own NAND + inverter tree (a lot of load & logic!)
- 2-stage decoding: predecoders and final decoders
 - Decode some bits first, then the rest (MSB/LSB doesn't matter)
 - Larger predecode is better (this is just a path delay w/ branching problem)



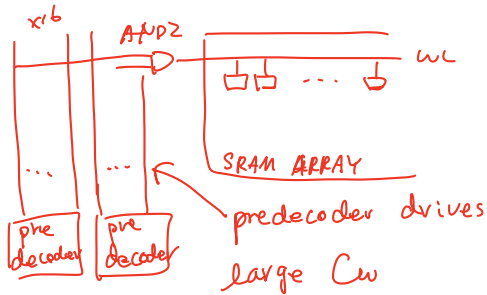
w/o predecoder



each addr drives 128 wire $B=128$



w/ predecoder



each output of predecoder drives $\times 16$ AND2

$\Rightarrow B=16$

