EECS151 : Introduction to Digital Design and ICs

Lecture 11 – CMOS

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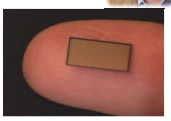
Intel Unveils Second-Generation Neuromorphic Chip

October 5, 2021, Intel has unveiled its second-generation neuromorphic computing chip, Loihi 2, the first chip to be built on its Intel 4 process technology. Designed for research into cutting-edge neuromorphic neural networks, Loihi 2 brings a range of improvements. They include a new instruction set for neurons that provides more programmability, allowing spikes to have integer values beyond just 1 and 0, and the ability to scale into three-dimensional meshes of chips for larger systems.

EETimes



Intel's Loihi 2 second-generation neuromorphic processor. (Source: Intel)

Review

- Core FPGA building blocks:
  - Configurable Logic Blocks (CLBs)
  - Configurable Interconnect
    - Switch boxes
- Modern FPGA Designs:
  - BRAMs, DSPs, and AI Engines
- CMOS process is used for producing chips
  - Planar bulk process used up to 28nm node
  - finFET and FDSOI used below the 22nm node

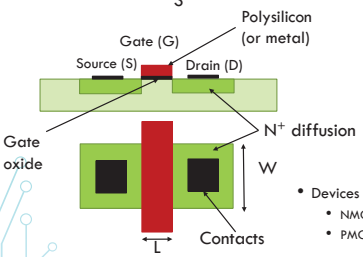
MOS Transistors

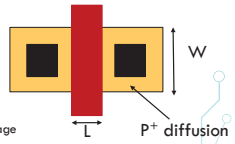
MOS Transistors

- Symbol

N-type NMOS: G, D, S, W/L

P-type PMOS: G, S, D, W/L



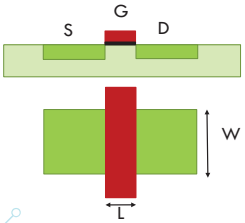


- Devices are symmetrical
  - NMOS: Drain is at higher voltage
  - PMOS: Source is at higher voltage

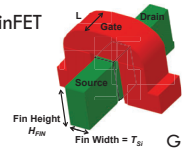
Different Kinds of MOS Transistors

- Planar bulk CMOS

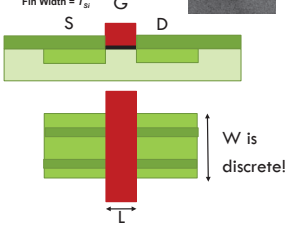
N-type NMOS: G, D, S, W/L



- FinFET



Intel 10nm IEDM 2017

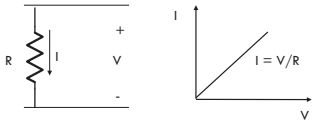


Transistor Dimensions are Quantized

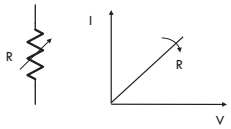
- FinFET widths are discrete ($W = kW_{unit}$)
  - k is an integer
- Lengths are quantized because of lithography
  - Also are quantized lower metal layers, contacts…

Ohm's Law

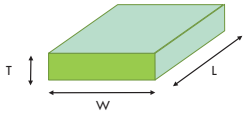
- Resistors



- Variable resistors



- Physical resistors

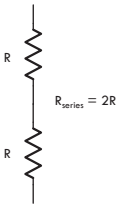


$R = \rho \frac{L}{TW}$

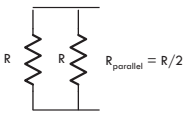
- In a planar process, designer controls W and L

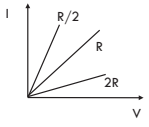
Series and Parallel

- With two identical resistors, R



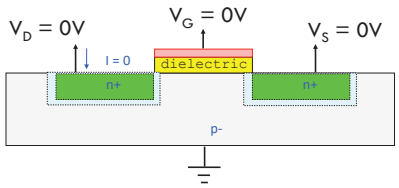
Equivalent to doubling length





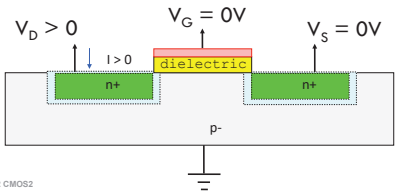
Equivalent to doubling width

An n-Channel MOS Transistor



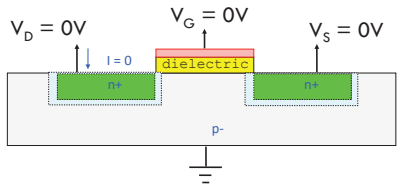
Polysilicon gate, dielectric, and substrate form a capacitor.

When $V_{GS} < V_{Th}$ transistor is off

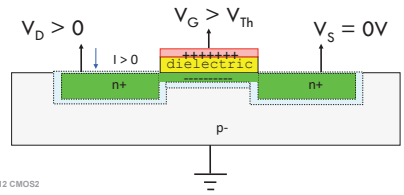


$V_{DS} > 0$, transistor leaks $I_{DS} \sim$ nA

An n-Channel MOS Transistor



When $V_{GS} < V_{Th}$ transistor is off

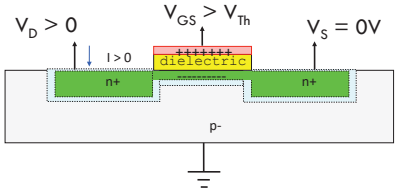


$V_G > V_{Th}$, small region near the surface turns from p-type to n-type.

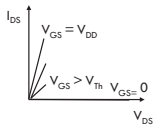
nFet is on.

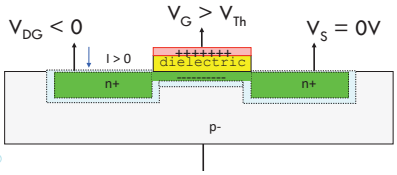
Current is proportional to V_{DS}

An n-Channel MOS Transistor

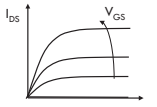


V_{DS} and V_{GS} change I_{DS}



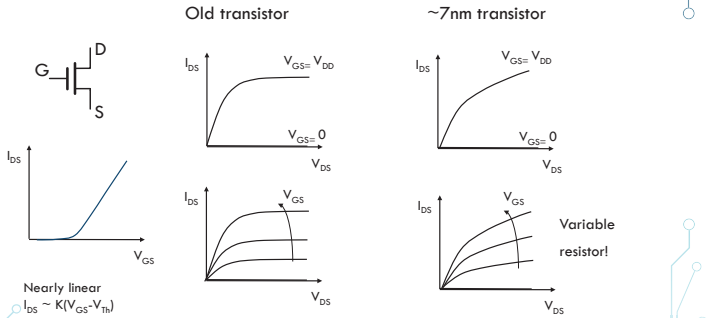


$V_{GD} < V_{Th}$ transistor saturates ($V_{DS} > V_{GS} - V_{Th}$)



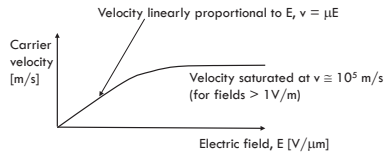
MOS Transistors

- NMOS Transistor I-V characteristics

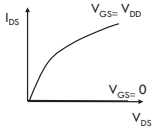


Velocity Saturation

- Carrier velocity in the channel saturates

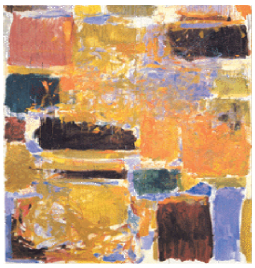


- All submicron transistors are velocity saturated
- Other effects (drain-induced barrier lowering) cause I_{DS} to increase in saturation



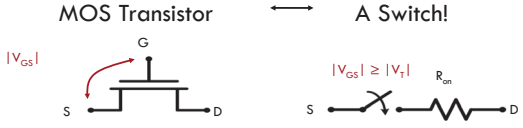
Administrivia

- Homework 5 will be posted later this week, due next week
- No lab this week
  - Lab 6 (last) after the midterm
- Midterm 1on October 7, 7-8:30pm
  - You will be assigned a classroom
  - One double-sided page of notes allowed
  - Material includes FPGAs



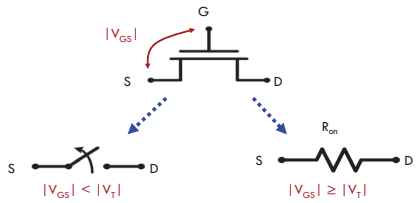
MOS Transistor as a Switch

MOS Transistor as a Resistive Switch

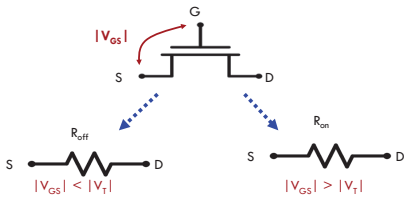


- V_{GS} controls the switch
  - (it also charges the channel capacitor)

ON/OFF Switch Model of MOS Transistor



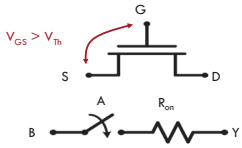
A More Realistic Model



- It is a dimmer!

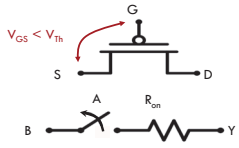
A Logic Perspective

NMOS Transistor



Y = B if A = 1

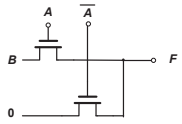
PMOS Transistor



Y = B if A = 0

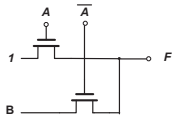
AND and OR

- AND



F = AB
(F = AB + $\overline{A}$·0)

- OR

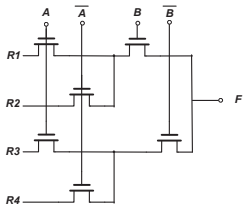


F = A+B
(F = A·1 + $\overline{A}$B)

- Keep in mind – single NMOS/PMOS transistors are imperfect switches!
  - Turns off when $|V_{GS}| = |V_{Th}|$

Peer Instruction

- Switch logic
- Which combination of inputs implements F = AB?



	R1 R2 R3 R4
a)	1 X X X
b)	0 X X X
c)	1 0 0 0
d)	1 1 1 0
e)	1 1 1 1
f)	None of the above

Summary

- CMOS process is used for producing chips
  - Planar bulk process used up to 28nm node
  - finFET, FDSOI used below the 22nm node