inst.eecs.berkeley.edu/~eecs151

EECS151 : Introduction to Digital Design and ICs

Lecture 1 – Introduction

Bora Nikolić

Mondays and Wednesdays 11am-12:30pm

Cory 540AB and on-line

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Class Goals and Expected Outcomes

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What This Class is All About?

- **Introduction to digital integrated circuit and system engineering**
  - Key concepts needed to be a good digital system designer
  - Discover you own creativity!
- **Learn models that allow reasoning about design behavior**
  - Manage design complexity through abstraction and understanding of automated tools
  - Allow analysis and optimization of the circuit's performance, power, cost, etc.
- **Learn how to make sure your circuit and the whole system work**
  - *There are way more ways to mess up a chip than to get it right.*

Digital design is not twitch.com!
Learn by doing!

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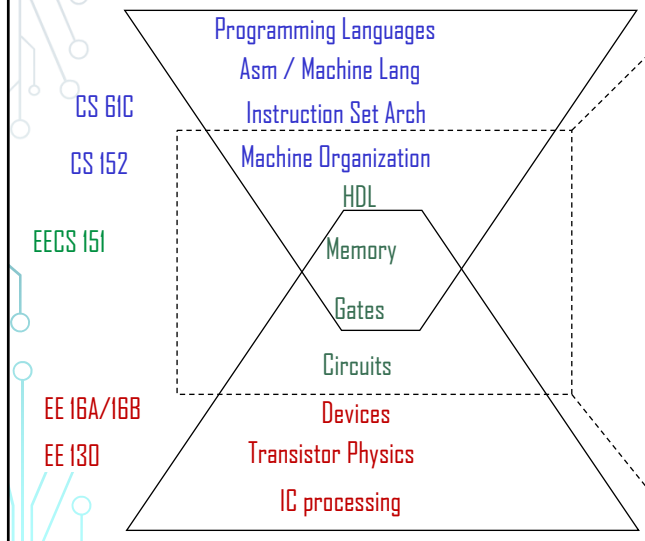
Course Focus



Deep Digital Design Experience

- Fundamentals of Boolean Logic
- Synchronous Circuits
- Finite State Machines
- Timing & Clocking
- Device Technology & Implications
- Controller Design
- Arithmetic Units
- Memories
- Testing, Debugging, Verification
- Hardware Architecture
- Hardware Description Languages (HDL)
- Design Flows (CAD)

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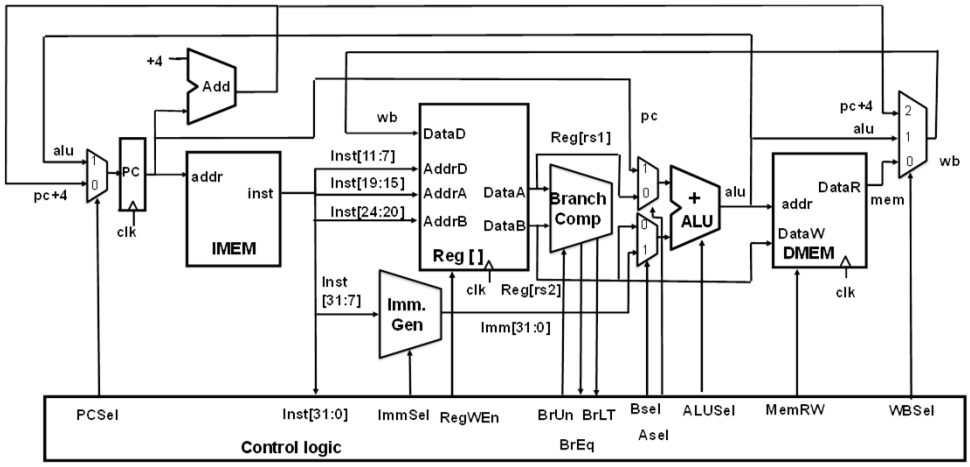
Prerequisites

- CS61C
  - C, Boolean logic, RISC-V ISA
  - We will review combinational and sequential logic and RISC-V datapath, pipelining (but go much more in depth)
- EE16A/B
  - Digital gates, RC networks
  - We will review transistor operation and design of CMOS logic

Possible Course Sequences

- Computer Engineering/Architecture/Hardware
- $\left[\begin{matrix}\text{CS 61C}\\ \text{EE 16A/B}\end{matrix}\right] \rightarrow \text{EECS 151} \rightarrow \text{CS152} \rightarrow \ldots$
- $\left[\begin{matrix}\text{CS 61C}\\ \text{EE 16A/B}\end{matrix}\right] \rightarrow \text{CS 152} \rightarrow \text{EECS151} \rightarrow \ldots$
  - With a 151/152 background should be able to take any graduate-level course in architecture/digital systems
- Circuits: EECS 151 + EE 140 is a springboard into integrated circuits

CS61C Background – RV32I



- Don't worry about details – we will rebuild it and make it work!

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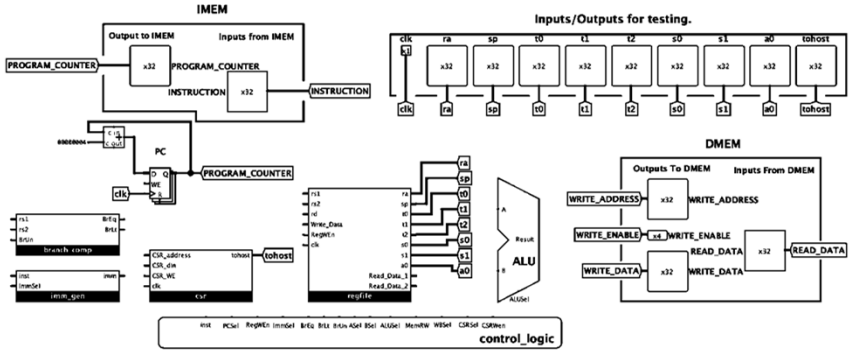
Processor Design Project in CS61C

- Designed in LogiSim
- From Fall'20 onwards, able to run RV32I compliance tests
  - Exported Verilog, ran synthesis and simulation (R. Lund, *et al*, WCAE'21)



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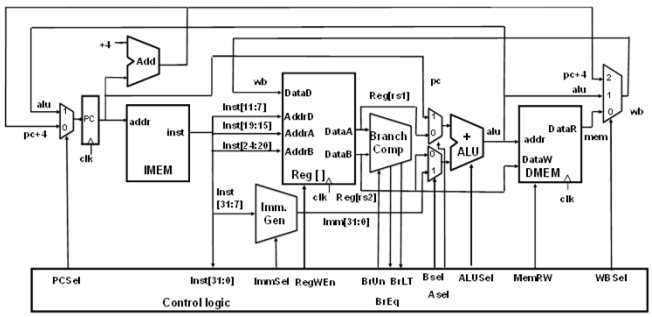
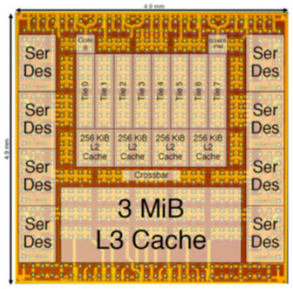
At the end of EECS 151

- Should be able to build a complex digital system





Berkeley chip in 2021
of IEEE Solid-State Circuits Conference

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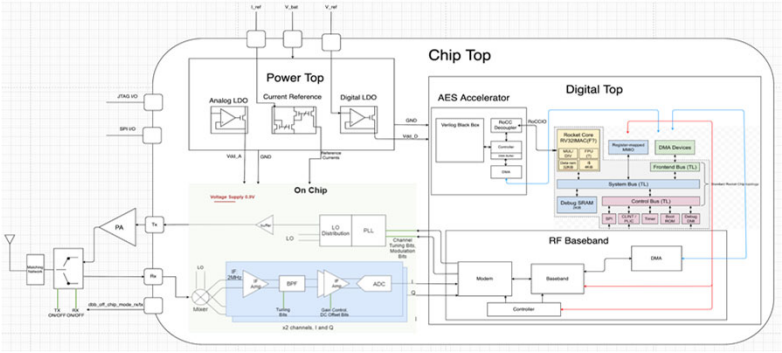
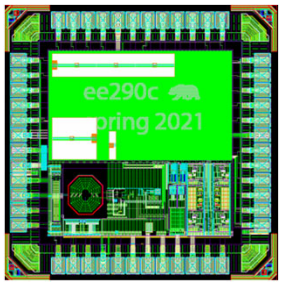
The Tapeout Class (EE194/290C)

- In Spring 2021, 19 students completed a 28nm chip design in a semester (14 weeks)
  - Just returned from fabrication
  - Prerequisites: Either EECS151 (ASIC lab preferred) or EE140





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Careers in Hardware

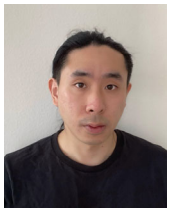
- Apple's New Silicon Initiative event tonight
  - Please come (it is on-line) and ask questions
  - Your chance to meet Apple's Fellows
  - Fellowships and scholarships available
- Undergraduate scholarships for students interested in System-on-a-Chip design
  - Applications next week!

Administrivia

EECS151/251A Crew

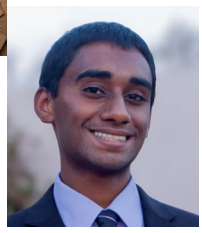
Professor Borivoje Nikolić (Bora)
509 Cory Hall
bora@berkeley.edu
Office Hours:
TBD

Alisha Menon
FPGA Labs
Office Hours:
M 2-3pm



Zhaokai Liu
ASIC Labs
Discussions
Office Hours:
F 2-3pm

All TA OHs held in 111 Cory.



Vighnesh Iyer
FPGA Labs
Office Hours:
M 10am-11am

Daniel Grubb
ASIC Labs
Discussions
Office Hours:
Tu 11-12pm

Charles Hong
FPGA Labs
Office Hours:
W 2-3pm

Zhenghan Lin
FPGA Labs
Office Hours:
W 5-6pm

Nayiri Krzysztofowicz
ASIC Labs
Office Hours:
Th 11-12pm

Reader: Bob Zhou

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Course Information

- Basic Source of Information, class website:

  http://inst.eecs.berkeley.edu/~eecs151/fa21/

  - Lecture notes and video modules
  - Assignments and solutions
  - Lab and project information
  - Exams
  - Piazza Discussion Forum
  - Many other goodies …

Print only what you need: Save a tree!

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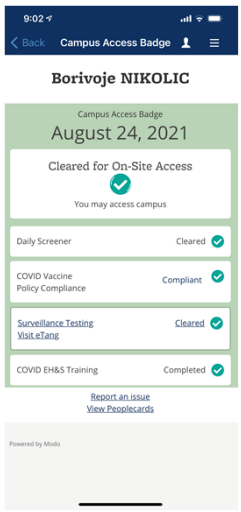
Health and Safety

- You need to have a green badge to come to in-person lectures, labs discussions!
- If you are feeling sick, please stay home!
  - Everything is available on-line
  - And I will switch to on-line lectures if I get sick



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Class Organization

- Lectures
- Discussion sessions (M 3-4pm, W 3-4pm, W 8-9am (online))
- Office hours (8 hours per week!)
- Problem Sets (~1 per week)
- Labs – FPGA or ASIC
  (or both, but only if you are sure that you have time)
- Design project
- 2 Midterms + 1 Final

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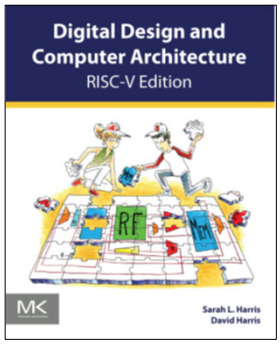
Lectures

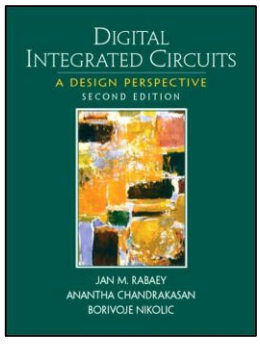
- Slides available on website before the lecture
- Lectures are webcast!
  - Recordings available as well
  - But please do come to lectures!
  - We like interactive lectures!

Class Textbooks

No Required Book this semester



Recommended (previously required)



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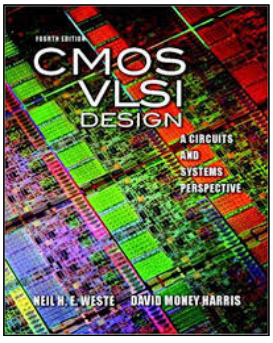


Useful

- Useful LA lab reference (EE151/251LA):
  - Erik Brunvand: Digital VLSI Chip Design with Cadence and Synopsys CAD Tools

Discussion Sessions

- Start next week!
- Review of important concepts from lecture (remember - no required textbook)
- Help with problem sets

Problem Sets

- Approximately 10 over the course of the semester (one per week)
- Posted on Thursday, due on Friday 11:59pm, 8 days later
- Essential to understanding the material
- Ok to discuss with colleagues but need to turn in your own work / write-up
- Late turn-in: 20% point deduction per day, except with documented medical excuse
- Solutions posted the week after due date

Labs

- Choose either FPGA or ASIC or both
- 6 FPGA / 6 ASIC lab exercises, done solo
  - Lab report (check off) due by next lab session
- Design project lasts 7 weeks, done with partner
  - Project demo/interview RRR week
  - Project report due RRR week
- All labs held in 111/117 Cory
  - ASIC: M 5-8PM, W 8-11am (online + 111 Cory), F 11am-2pm
  - FPGA: W 6-9PM, Th 11am-2pm, F 8-11AM (fourth lab may be opened)
- All labs start next week!

Midterm and Final

- Midterms scheduled in evening
- Review session in advance
  - Midterms:
    - Th. Oct. 7, 7-9pm (tentative)
    - Th. Nov. 4, 7-9pm (tentative)
- Final: M, Dec 13, 11:30am-2:30PM

All exams are closed book – with one double sided 8.5x11 sheet of notes

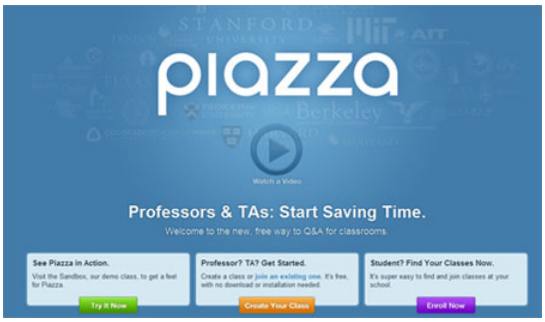
Clobber Policy

- The clobber policy allows you to:
  - Override your Midterm 1 score with the score on the final if you perform better on the final, and
  - Override your Midterm 2 score with the score on the final exam if you perform better on the final.
  - Note that the reverse is not true - you must take the entire final exam, regardless of your Midterm 1 and Midterm 2 scores.

Course Information

- For interactions between faculty, GSIs and fellow students – we are using Piazza

  For fastest response **post your questions on Piazza.**



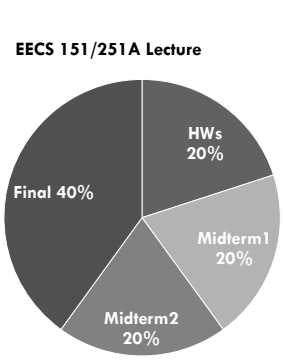
(make sure to register ASAP if you don't want to miss any of the action)

https://piazza.com/berkeley/fall2021/eecs151251a

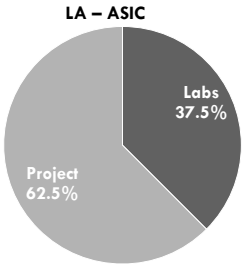
Policy on Academic Dishonesty

- Details of our cheating policy on the class web site. Please read it and ask questions.
- If you turn in someone else's work as if it were your own, you are guilty of academic dishonesty. This includes problem sets, answers on exams, lab exercise checks, project design, and any required course turn-in material.
- Also, if you knowingly aid in cheating, you are guilty.
- However, it is okay to discuss with others lab exercises and the project (obviously, okay to work with project partner). Okay to discuss homework with others. But everyone must turn in their own work.
- Do not post your work on public repositories like github (private o.k.)
- If we catch you cheating, you will get **negative points** on the assignment: It is better to not do the work than to cheat!
  If it is a midterm exam, final exam, or final project, you get an F in the class.
- All cases of cheating reported to the Center for Student Conduct.

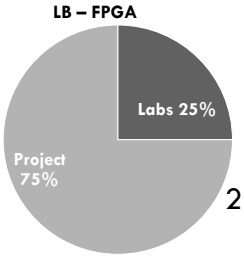
Grading Breakdown



3 units



2 units



2 units

Tips on How to Get a Good Grade

The lecture material is not the most challenging part of the course.

- You should be able to understand everything as we go along.
- Do not fall behind in lecture and tell yourself you "will figure it out later from the notes or book".
- Notes will be online before the lecture (usually the night before). Study them before class.
- Ask questions in class and stay involved in the class - that will help you understand. Come to office hours to check your understanding or to ask questions.
- Complete all the homework problems - even the difficult ones.
- The exams will test your depth of knowledge. You need to understand the material well enough to apply it in new situations.

You need to enroll in both the lab and the course.

- Take the labs very seriously. They are an integral part of the course.
- Choose your project partner carefully. Your best friend may not be the best choice!
- Most important (this comes from 30+ years of hardware design experience):
  - Be well organized and neat with homework, labs, project.
  - In lab, add complexity a little bit at a time - always have a working design.
  - Don't be afraid to throw away your design and start fresh.

Getting Started

- Discussions and labs start next week
- Lab 1 assigned later this week – complete the setup before coming to the lab!
  - Come prepared to the lab session
- Register on Piazza as soon as possible
- Register for your EECS151 class account at inst.eecs.berkeley.edu/webacct
- If you are registering through concurrent enrollment:
  - ❑ See us in person this week

Digital Integrated Circuits and Systems

Past, Present and Future

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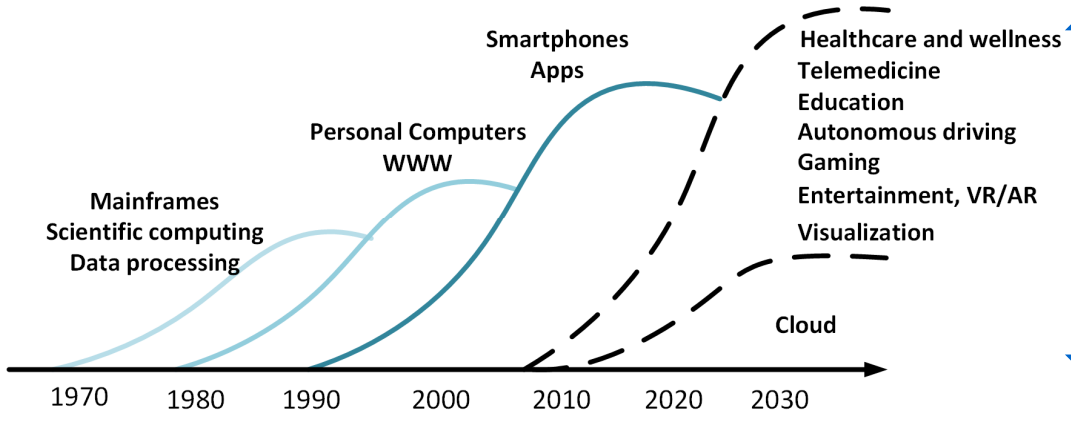
Diversifying Applications



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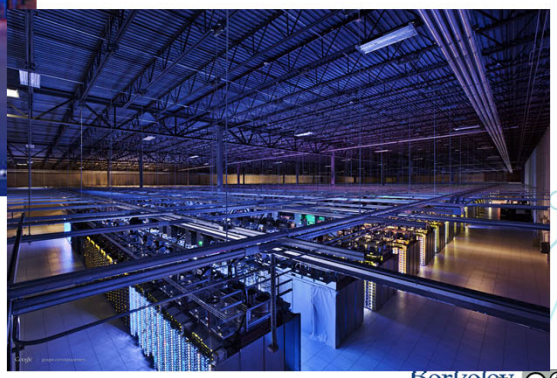
Remember: My Other Computer …



- It is being customized as well!

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How Did All This Arise?

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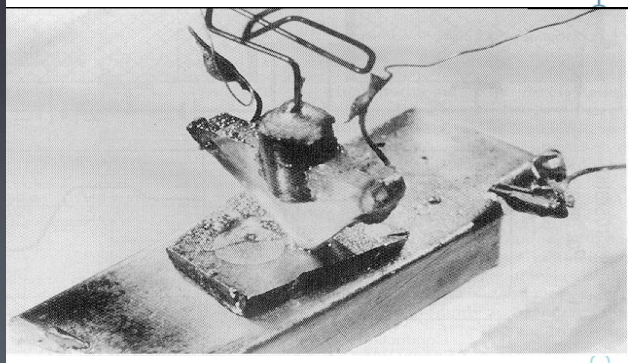
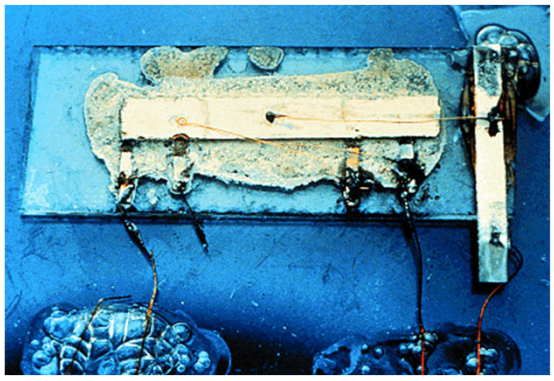
The Transistor Revolution



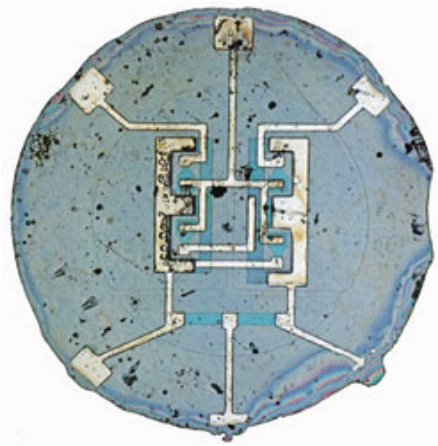
First transistor
Bell Labs, Dec 1947

First Integrated Circuits (1958-59)



Jack Kilby, Texas Instruments

Bob Noyce, Fairchild



Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 12 months.
- He made a prediction that semiconductor technology will double its effectiveness every ~~12~~ ~~18~~ 24 months

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term, this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000."
Gordon Moore, Cramming more Components onto Integrated Circuits, (1965).

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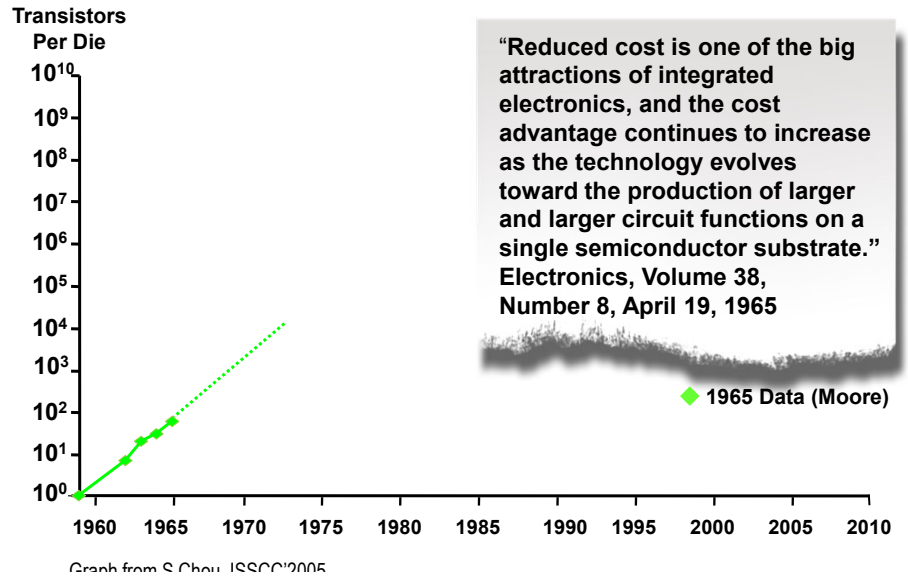
Moore's Law - 1965



"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."
Electronics, Volume 38, Number 8, April 19, 1965

Graph from S Chou, ISSCC'2005

Source: Intel

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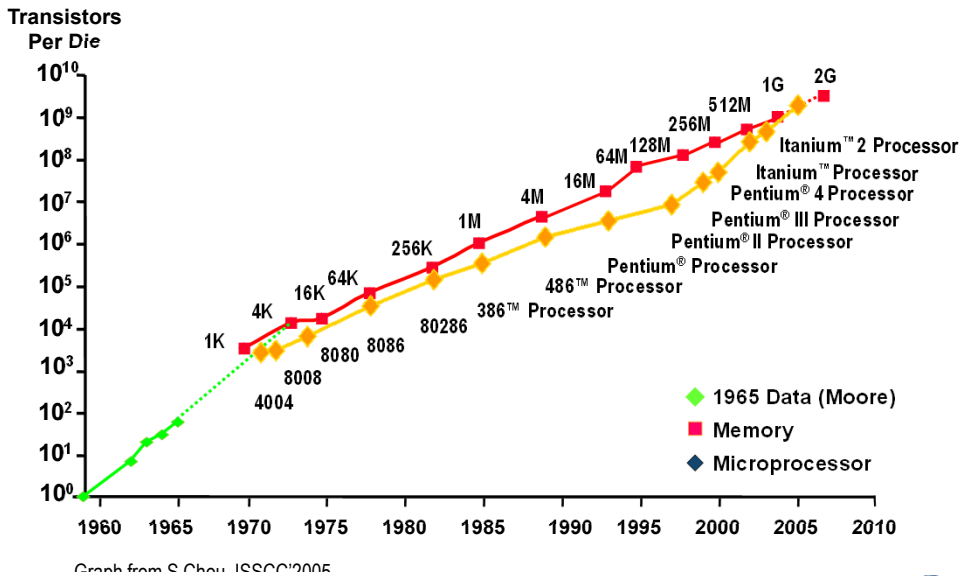
Moore's Law - 2005



Source: Intel

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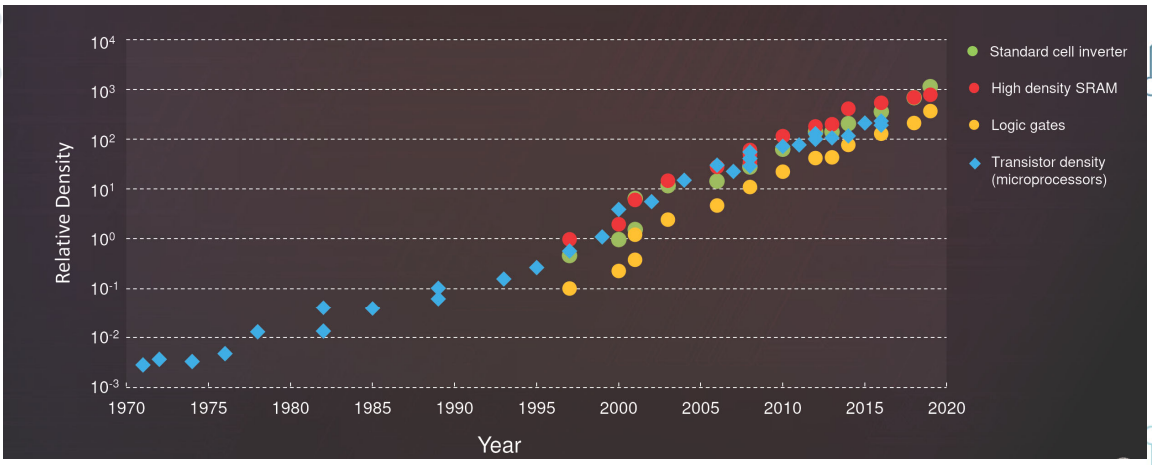
Transistor Counts



H.-S. P. Wong, HotChips, August 2019.

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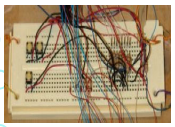
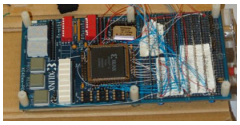
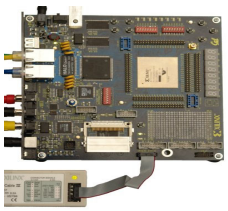
CS150/EECS151 Project Complexity



1980 Pong game
10's of logic gates

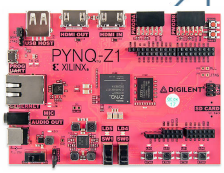


1995 MIDI synthesizer
1000's of logic gates



2000-2010 eTV tuner
10K's logic gates

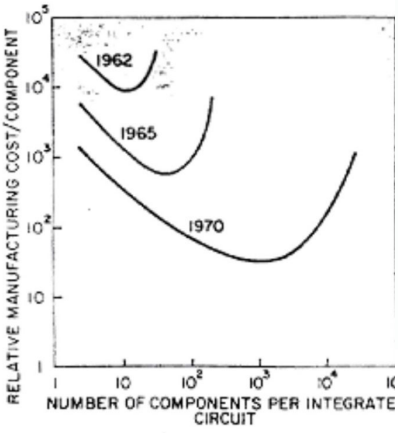
2010-2017 MIPS CPU or BYO
1M logic gates

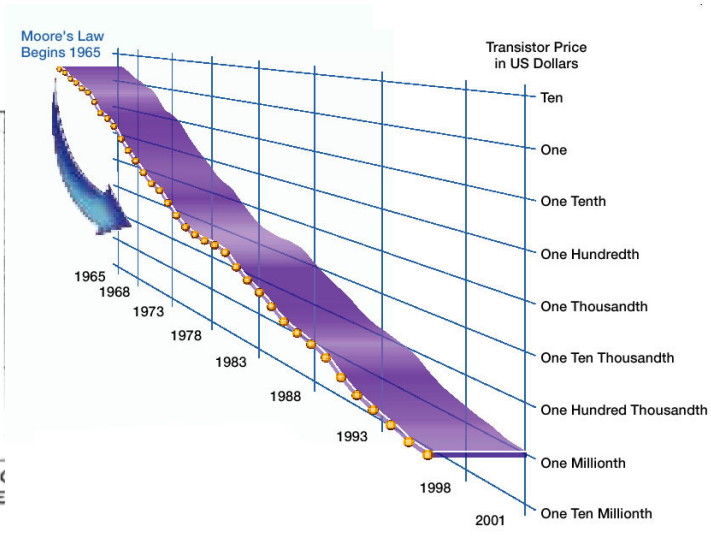


2018 MIPS CPU
Programmable SOC: dua
core ARM, 85K logic cells
220 MACC

The Key: Cost

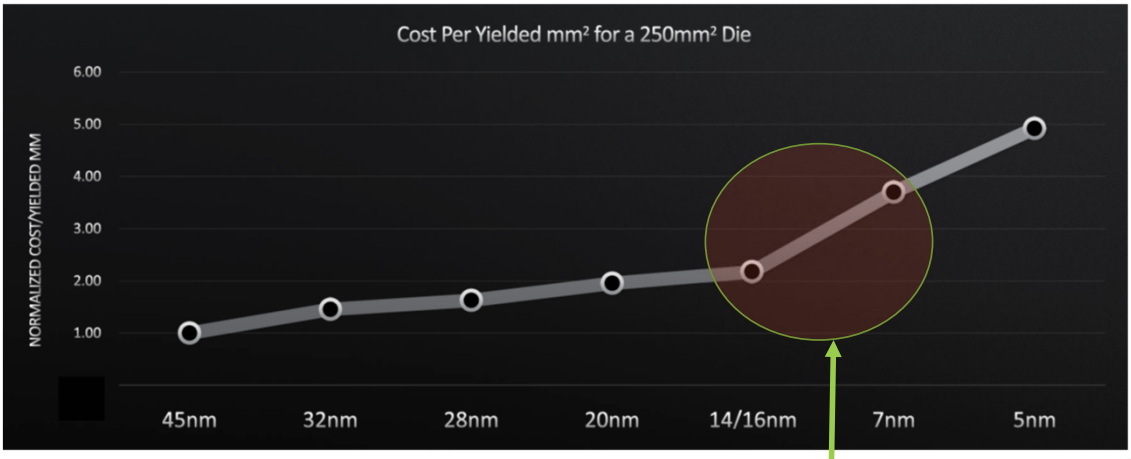
Moore's 1965 paper:





Moore's Law ends when cost reduction stops

Recent Cost Trend



L. *Su, HotChips, August 2019.*

Cost nearly doubled!

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The Other Trends

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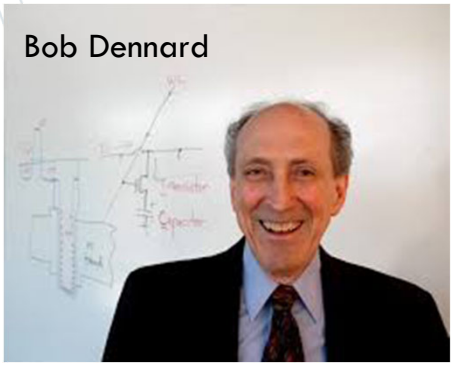
Dennard Scaling (1974)

Bob Dennard



- Voltages (and currents) should be scaled proportionally to the dimensions of the transistor
- If so, delay and power should scale

$$Delay \approx C \cdot V / I_{avg}$$

$$P \approx C \cdot V^2 / Delay$$

- And, in theory, power *density* constant!
- We are not following Dennard's scaling since ~2005

R.H. Dennard, F. Gaensslen, H.-N. Yu, L. Rideout, E. Bassous, A. LeBlanc, Andre "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid State Circuits*. SC-9 (5), 1974.

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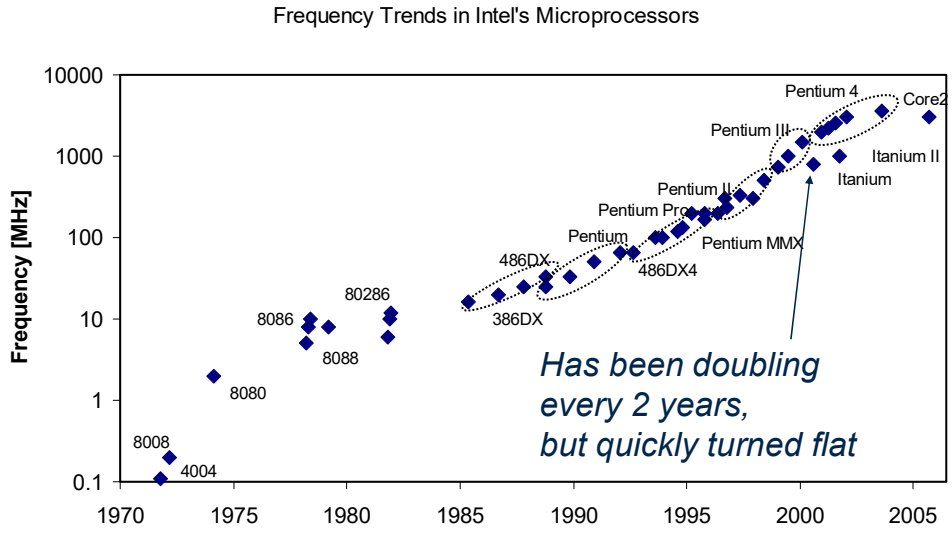
Frequency



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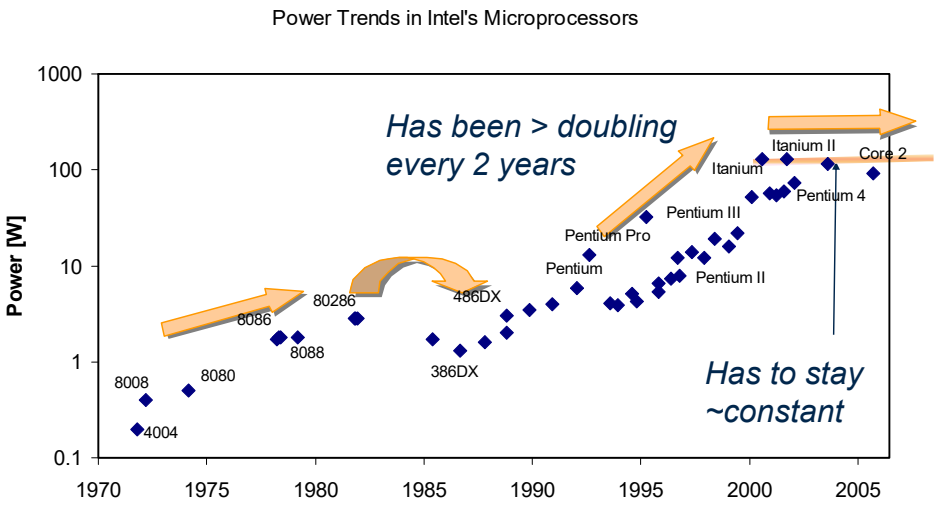
Power Dissipation



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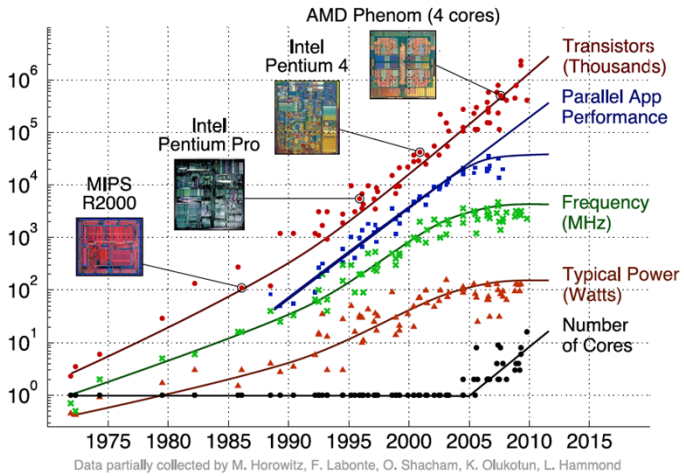
Power and Performance Trends

- What do we do next?



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The Other Demon: Complexity and Design Costs

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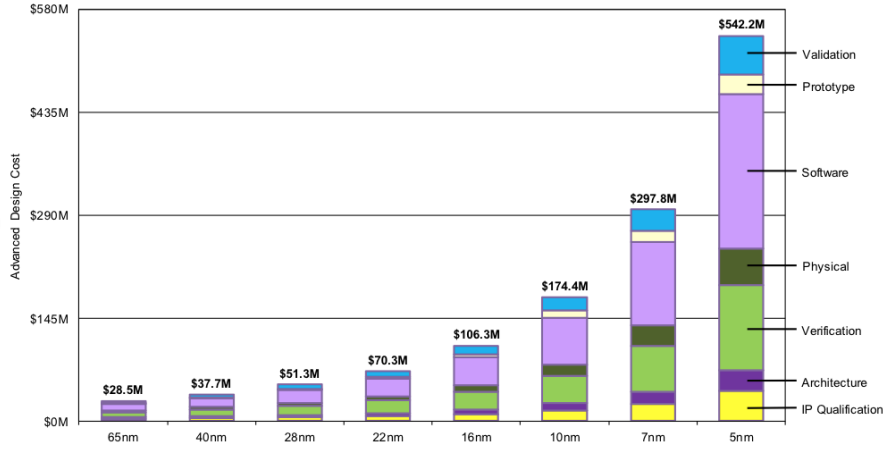
Cost Of Developing New Products



- These are non-recurring (NRE) costs, need to be amortized over the lifetime of a product
- We will attempt to dismantle this…

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Solutions

- Software faced the complexity issues as well
- Solutions: Increase abstraction level, be modular, improve reuse, rely on open source, be agile…
- Apply to hardware design

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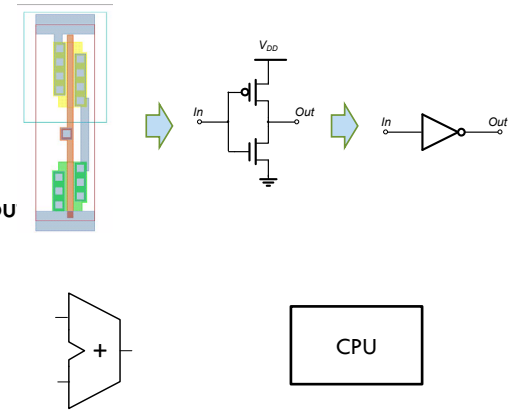
Abstraction

- How to design a Pong game
  - Hand layout
  - Gate-level design (semi custom)
  - Describe in HDL Synthesis, place and rou
  - HLS, HCL
  - "Computer, design a pong game"



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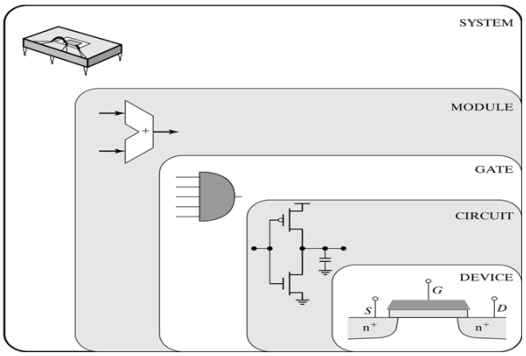
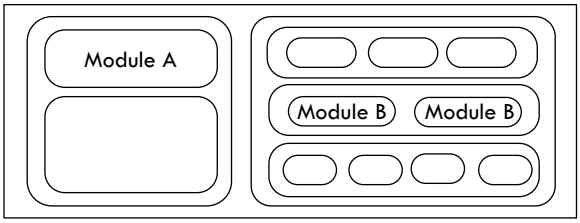
Hierarchy in Designs – Complexity Control

- Design Abstraction
  - Hide details and reduce number of things to handle at any time
- Modular design
  - Divide and conquer
  - Simplifies implementation and debugging
- Regularity
  - Instantiate identical modules





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Digital Design: What's it all about?

Given a functional description and performance, cost, & power constraints, come up with an implementation using a set of primitives.

- How do we learn to do this?
  1. Learn about the design primitives and how to use them.
  2. Learn about design representations.
  3. Learn formal methods and tools to manipulate the representations.
  4. Study design examples.
  5. Have robust approach to verification.
  6. Use trial and error - CAD tools and prototyping. Practice!
- Digital design is a bit an art as well as a science. The creative spirit is critical in combining primitive elements & other components in new ways to achieve a desired function.
- However, unlike art, we have objective measures of a design:

Performance Cost Power

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