EECS 151/251A Discussion 10/worksheet

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Administrativia

- Midterm 2 on Thursday 11/4
- Midterm review session Tuesday 11/2 (problems 4-7)
- How is the project?

Agenda

- Midterm worksheet/problem examples

Midterm 2 Topics!

Including:

- CMOS
- Delay optimization and logical effort
- Power and energy
- Wires and RC models
- Arithmetic

Problem 1 – CMOS Gate (Fa20 m2)

In this problem, use the process that has $W_n = W_p = 1$ in a reference inverter, and $\gamma = 1$.

(a) Design a complex CMOS gate: $Y = \overline{(A + B) \cdot C + D}$. Size the transistors so that the gate has the same pull-up and pull-down strength as a reference inverter.

251A only: Also make sure the parasitic delay (P) is minimized in your design.

Problem 1 – CMOS Gate (Fa20 m2)

(b) Calculate the logic effort for each input (LE_A, LE_B, LE_C, LE_D).

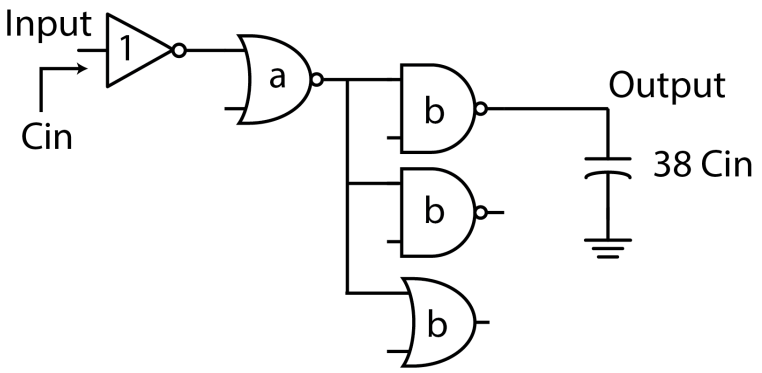
Problem 1 – CMOS Gate (Fa20 m2)

(c) **251A only:** Calculate the optimized parasitic delay P.

Problem 2 – Logical effort (Fa18 m2)

Reference inverter: $W_p = 2W_n = W$, $t_{p,inv} = 32ps$, $\gamma = 2$

a) Determine path effort and optimal stage effort



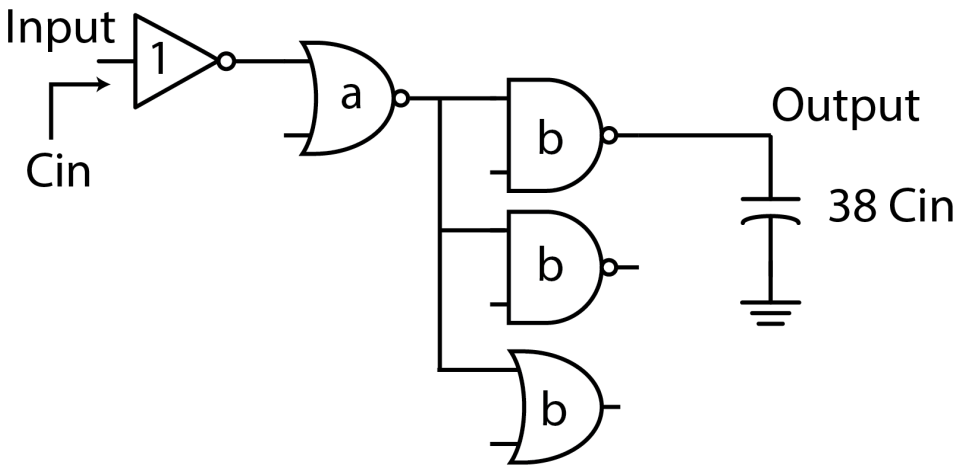
b) Find optimal a and b for minimum delay

c) Is this the optimal number of stages for delay? If not, what is?

Problem 2 – Logical effort (Fa18 m2)

Reference inverter: $W_p = 2W_n = W$, $t_{p,inv} = 32ps$, $\gamma = 2$

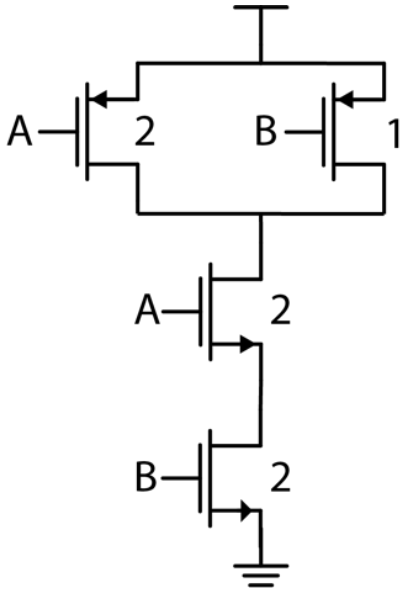
d) If we could add a single inverter anywhere along the critical path, where would be the best for the minimum total area?



Problem 2 – Logical effort (Fa18 m2)

Reference inverter: $W_p = 2W_n = W$, $t_{p,inv} = 32ps$, $\gamma = 2$

e) "Better" NAND gate logical effort?

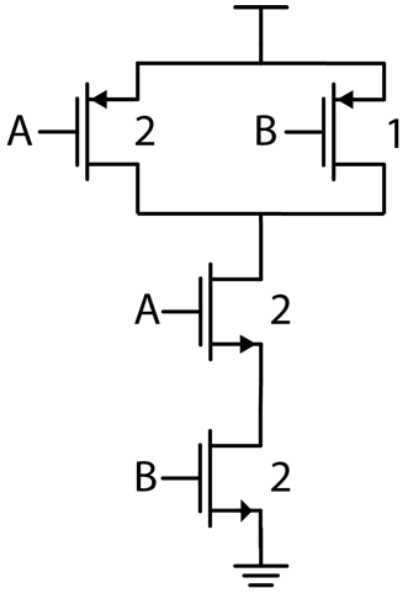


Problem 2 – Logical effort (Fa18 m2)

Reference inverter: $W_p = 2W_n = W$, $t_{p,inv} = 32ps$, $\gamma = 2$

f) "Better" NAND gate intrinsic delay parameter (p)?

$$t_{p,inv} = \ln(2)\, R_{eq,inv} C_{in,inv}$$



g) How does this affect the delay of our original chain?

Problem 3 (Fa19 m2)

4) *Delays and Adders* (18 points, 22 minutes)

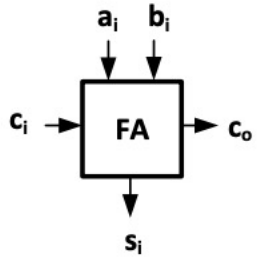
You are designing a datapath in a brand-new CMOS FinFET technology, where NMOS and PMOS devices have equal strength. In particular, it has only four CMOS gates: 2- input NAND, 2-input NOR, 2-input XOR, and an OAI21 gate ($Y = \overline{(A+B)C}$). Gate capacitance equals drain capacitance per unit area ($\gamma = 1$), and the four gates come in with only one size each, i.e., you do not need to size gates in this problem.

a) If both the 2-input NAND gate and the 2-input NOR gate have a delay dependence on a fanout, f, given as $t_{NAND2} = t_{NOR2} = 2ns(4 + 3f)$, what is the delay dependence on the fanout of the input C of the OAI21 gate (C is in the critical path)?

t_{AOI21} = _____.

Problem 3 (Fa19 m2)

b) Draw a fast full-adder using the four types of gates and calculate the ci->sum and ci->cout delay. Note that using an OAI21 gate could potentially simplify the logic for C_out. Assume the capacitance driven by the sum and the carry bits is equal to the capacitance of inputs a_i, b_i and t_{XOR2} = 2ns (8 + 8f).

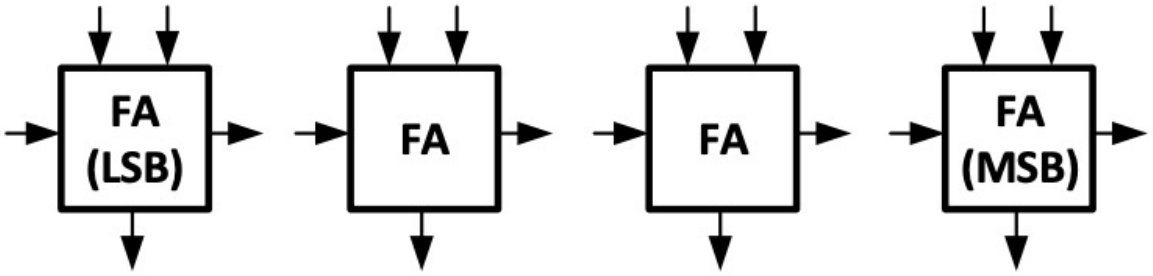


$t_{FA,Ci \rightarrow Co}$ = _____.

$t_{FA,Ci \rightarrow S}$ = _____.

Problem 3 (Fa19 m2)

c) Complete the drawing and label all inputs and outputs for an 4-bit ripple-carry adder in figure below by using full-adder (FA) cells from part b). Inputs are a[3:0] and b[3:0] and there is no carry-in to the least-significant bit.



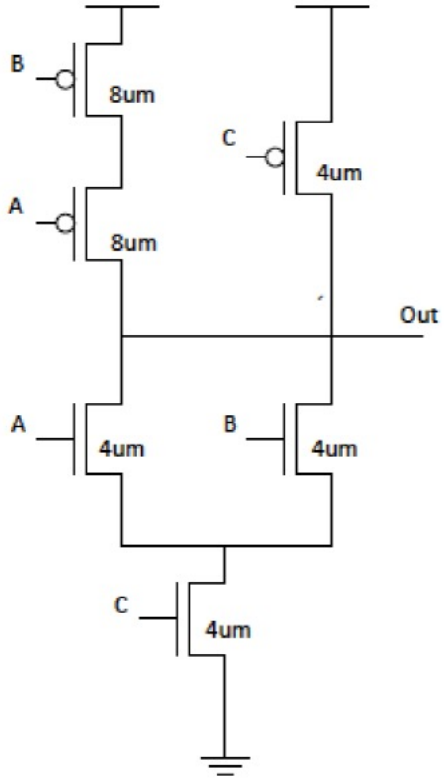
Problem 3 (Fa19 m2)

d) Find the critical path delay for the circuit in part c), if the capacitance driven by the sum and the carry bits is equal to the input a_i, b_i capacitance. If you are not confident in your answer in part b), you can express the delay in terms of $t_{FA,Ci\rightarrow Co}$, and $t_{FA,Ci\rightarrow S}$

Critical path = _____.

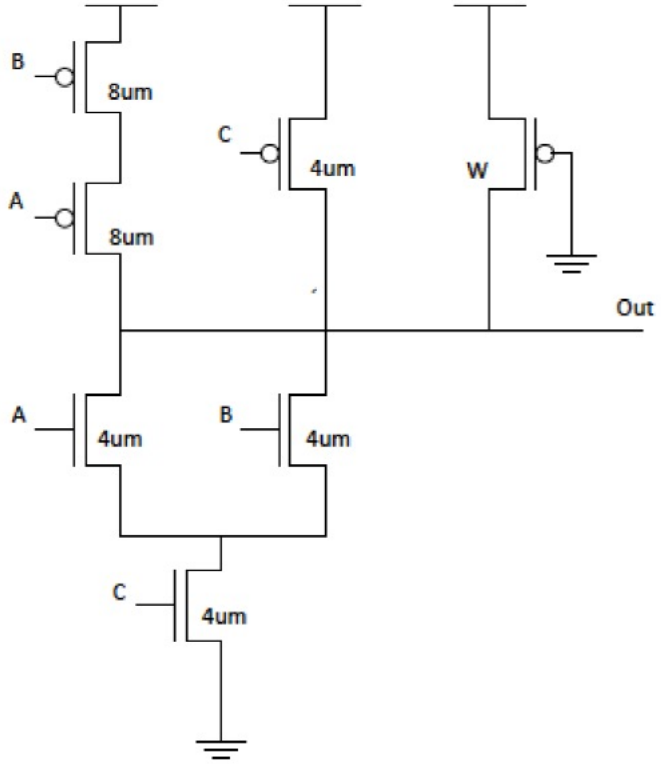
Problem 4 Logical effort (Sp13)

Logical effort and
intrinsic delay?



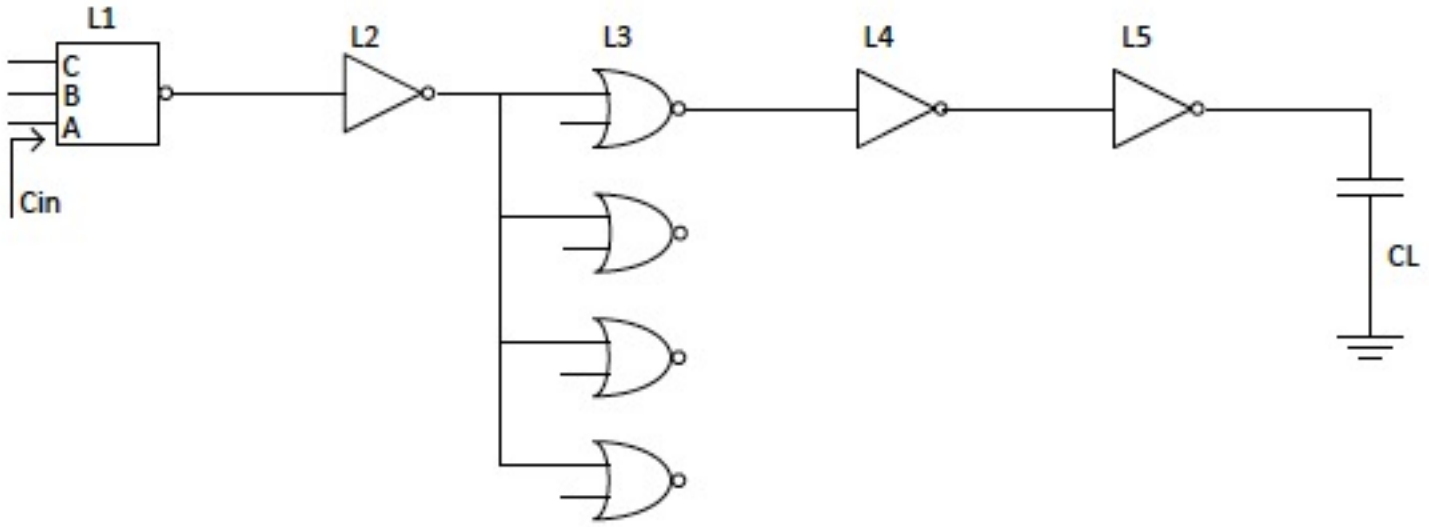
Problem 4 Logical effort (Sp13)

- Made a mistake in layout! What is the effect on L-H transition? H-L transition?



Problem 4 Logical effort (Sp13)

- Delay optimization with **fixed gate**
- Using A input with Cin = 24 fF, CL = 75Cin

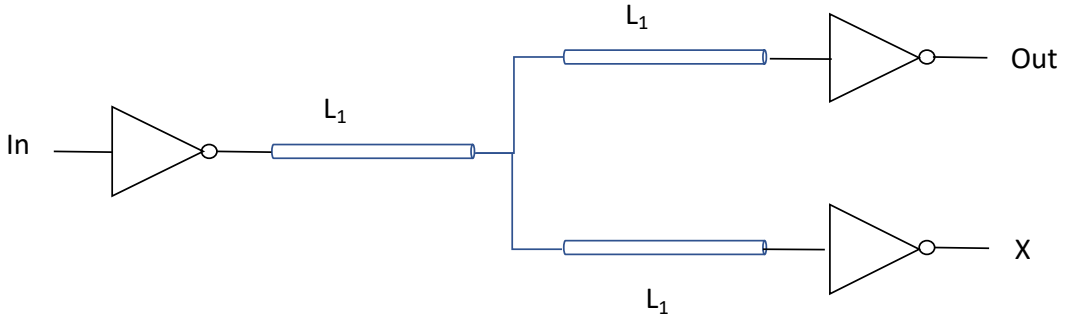


Problem 5 – Wires and repeaters (fa18 m2)

Min. inverter: drive resistance R_d, input cap C_{in}, intrinsic cap C_{int}

Wire: r_w , c_w (per unit length)

a + b) Propagation delay from *in* to *out* (using distributed model for wires)

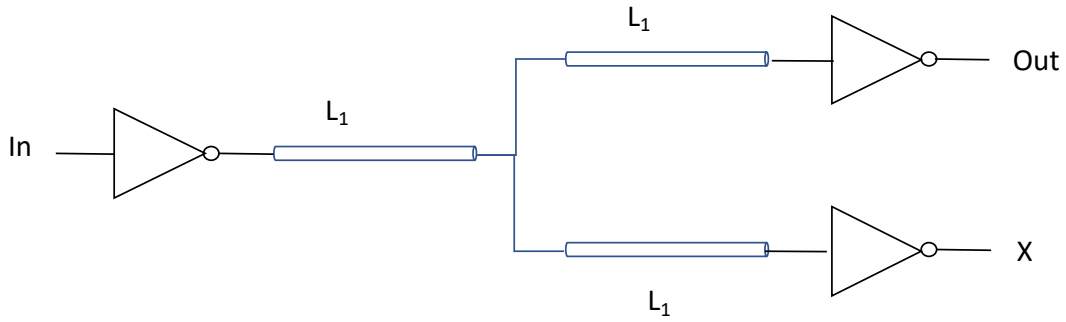


Problem 5 – Wires and repeaters (fa18 m2)

Min. inverter: drive resistance R_d, input cap C_{in}, intrinsic cap C_{int}

Wire: r_w , c_w (per unit length)

c) Derive reduction in delay by increasing the first inverter as much as possible:

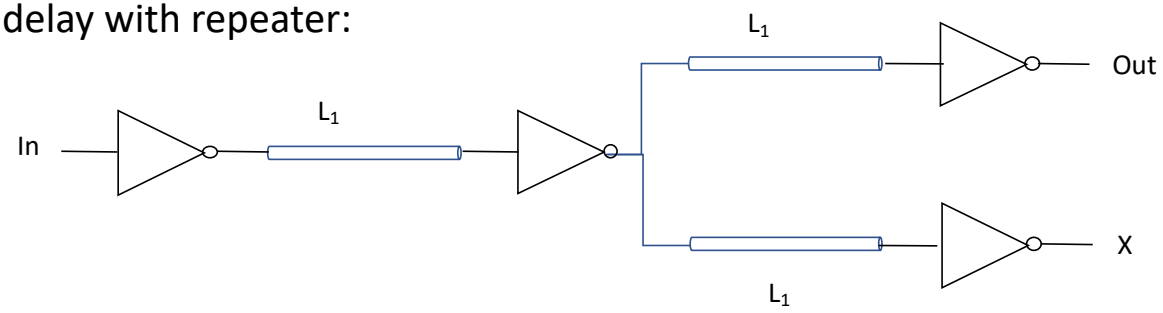


Problem 5 – Wires and repeaters (fa18 m2)

Min. inverter: drive resistance R_d, input cap C_{in}, intrinsic cap C_{int}

Wire: r_w , c_w (per unit length)

d) Propagation delay with repeater:

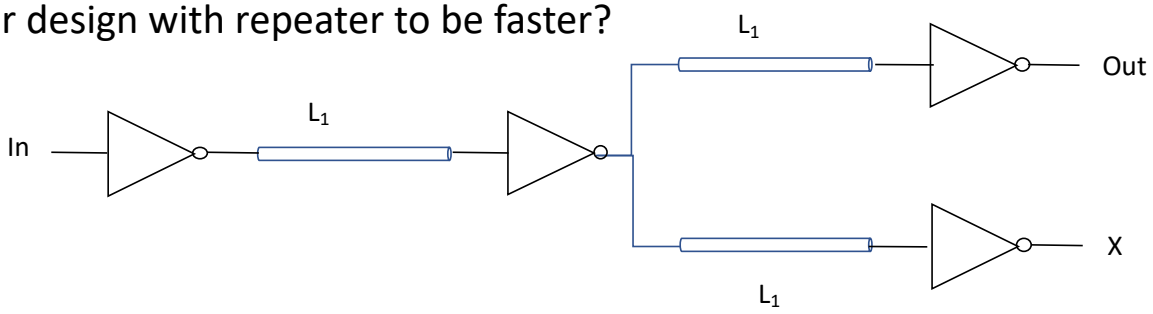


Problem 5 – Wires and repeaters (fa18 m2)

Min. inverter: drive resistance R_d, input cap C_{in}, intrinsic cap C_{int}

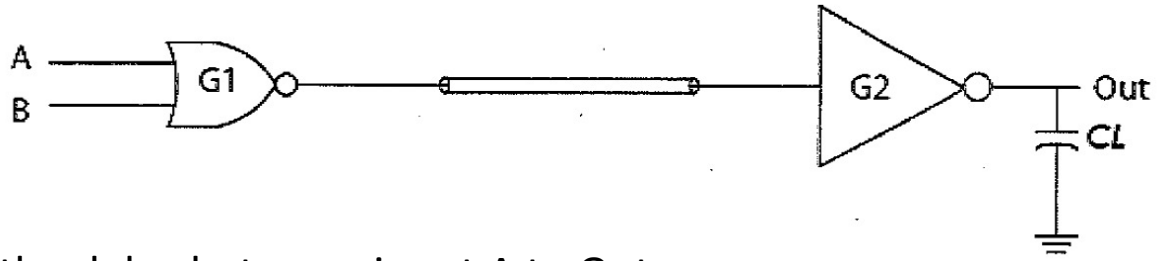
Wire: r_w , c_w (per unit length)

e) Conditions for design with repeater to be faster?



Problem 6 - Wires and Energy (Sp16)

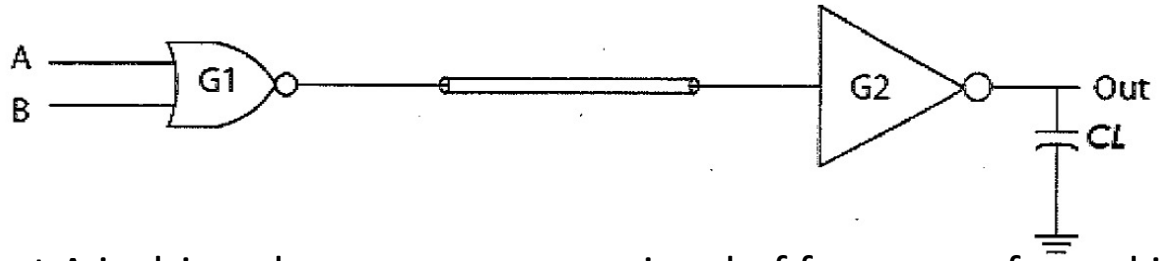
A NOR gate (G1) with input capacitance C_1 is driving a wire with total resistance R_W and total capacitance C_W, and an inverter with input capacitance C_2. Inverter G2 is driving an external load of C_L. The on-resistance of G1 and G2 are R_1 and R_2, respectively. Assume $\gamma = 1$ and $2R_N = R_P$. The power supply has a voltage of V_{DD}.



a) Determine the delay between input A to Out

Problem 6 - Wires and Energy (Sp16)

A NOR gate (G1) with input capacitance C_1 is driving a wire with total resistance R_W and total capacitance C_W, and an inverter with input capacitance C_2. Inverter G2 is driving an external load of C_L. The on-resistance of G1 and G2 are R_1 and R_2, respectively. Assume $\gamma = 1$ and $2R_N = R_P$. The power supply has a voltage of V_{DD}.



b) Assume input A is driven by a square-wave signal of frequency f_{clk} and input B is driven by a square wave signal of frequency $\frac{1}{3}f_{clk}$. Derive an expression for total dynamic power consumption of the circuit.

Problem 7 - adder (Sp19 final)

22. Adder Design [5pts]: The carry-select technique presented in lecture can be applied hierarchically. Imagine applying the technique in a binary way—a larger adder is divided in half using the carry-select and then the same technique is applied to the sub-adders, etc. The process would stop at 4-bit ripple adders.

    (a) Assuming a FA and a MUX both have unit delay (delay = 1), what would be the delay (from data in to carry out) of a 32-bit adder?

    (b) How would the delay scale with the size of the adder?

Problem 7 - adders (Sp19 final)

23. Adder Design [6pts]: A carry-lookahead adder used to add A to B is organized into groups of 4-bits. A group has carry into the group, c_{i-1} and carry out of the group, c_{i+3}.

(a) In terms of the propagate and generate signals, p_i and g_i, of the individual bit stages, write an expression for the *group propagate signal*, P and *group generate signal*, G.

(b) Write an expression for c_{i+3} based on the group P and G.

(c) Write an expression for the bit stage sum output, s_i.