EECS 151/251A Homework 1

Due Friday, Jan 28th, 2022

Problem 1: Dennard Scaling

Assuming ideal Dennard scaling, you have previously designed a microprocessor that runs at 5GHz but dissipates 55W. In the next technology node, with features that are scaled by 0.6x, what will be the power and performance of your microprocessor?

Circuit delay reduces by 40% (0.6x), voltage reduces by 40% to maintain electric field (0.6x), f increases by 67% (1/0.6), C reduces by 40% (0.6). Power is proportional to CV_{dd}^2f so the new power is $55W*0.6*0.6^2*1/0.6 = 19.8W$

Power ___19.8W____
Performance ___8.33_____

Problem 2: Power/energy

- If you have a biomedical sensor interface to monitor a signal long term with on-chip processing where the chip is in contact with human skin and powered by a battery, what could be a primary concern for
    - Power consumption

      _____ (heat/burn/too hot on skin)

    - Energy consumption

      _____ (battery life)

- If the sensor dissipates 200mW and you expect it to have 6 hours of battery life, how much energy in Joules must the battery hold at full charge?

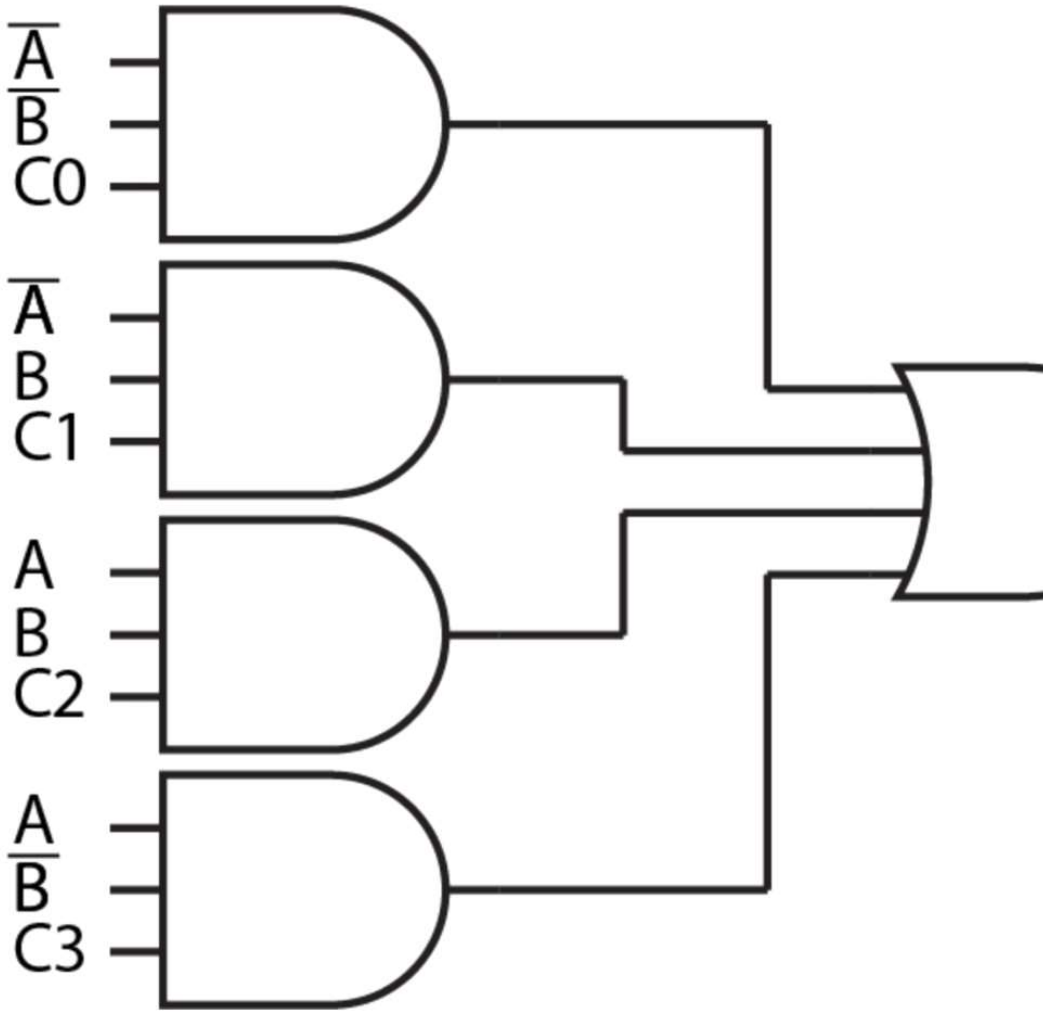
  _____ (1.2 watt-hours = 4320J)

- The user removes the sensor to charge it while they sleep. It can take 8 hours to recharge, how much power should the charger be able to supply to make this possible?

_____ (0.15W)

Problem 3: Boolean Algebra

Consider the given circuit. All inputs (A, B, C0, C1, C2, C3) must be either 0 or 1. What must C0, C1, C2, and C3 be such that the circuit computes the function XNOR (A, B)?



C0: _____ (1)

C1: _____ (0)

C2: _____ (1)

C3: _____ (0)

Problem 4: Avoid unintentional latch synthesis

For each of the following Verilog modules, which variables will generate latches? If none, write none.

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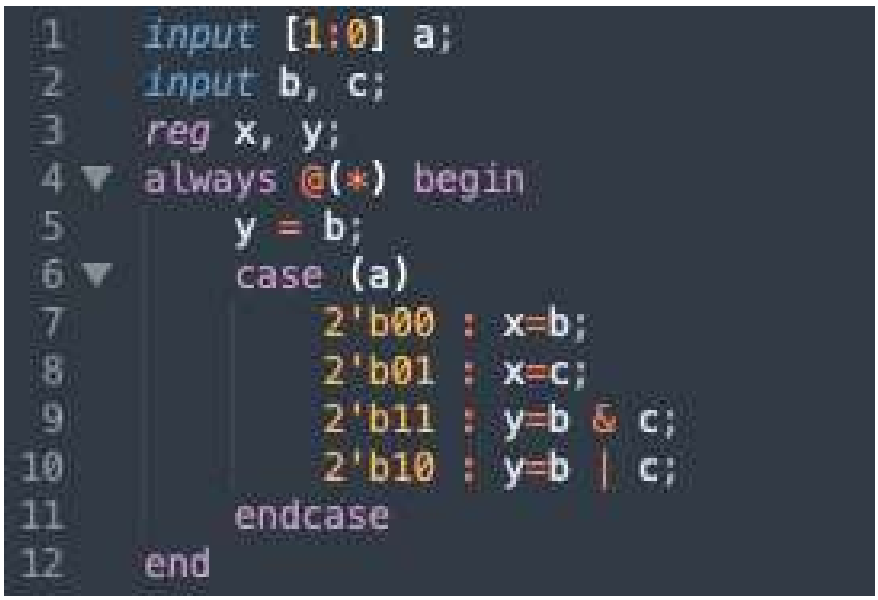

```
1   input [1:0] a;
2   input b, c;
3   reg x, y;
4   always @(*) begin
5       y = b;
6       case (a)
7           2'b00 : x=b;
8           2'b01 : x=c;
9           2'b11 : y=b & c;
10          2'b10 : y=b | c;
11      endcase
12  end
```

_____ (x)

-

```
input a;
output reg [1:0] y;
always@ (*)
    if (a)
        y = 2'b01;
    else begin
        y[0] = 1;
        y[1] = 0;
    end
end
```

_____ (none)

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```
input x, y;
reg [1:0] d, c;
always @(*) begin
    d = 2'b00;
    if (x && y) begin
        d = 2'b01;
        c = 2'b00;
    end
    else if (x)
        d = 2'b11;
end
```

_____ (c)

Problem 5: Find the Verilog error

Find the line which has the Verilog error and rewrite it correctly

```
1   module mux_4to1 (
2       input a,b,c,d,
3       input [1:0] sel,
4       output out
5       );
6       always @(sel) begin
7           case (sel)
8               2'b00 : out = a;
9               2'b01 : out = b;
10              2'b10 : out = c;
11              2'b11 : out = d;
12          endcase
13      end
14  endmodule
```

_____
(line 4, should be output reg out;
line 6, should be always @(*) or always @(a or b or c or d or sel))