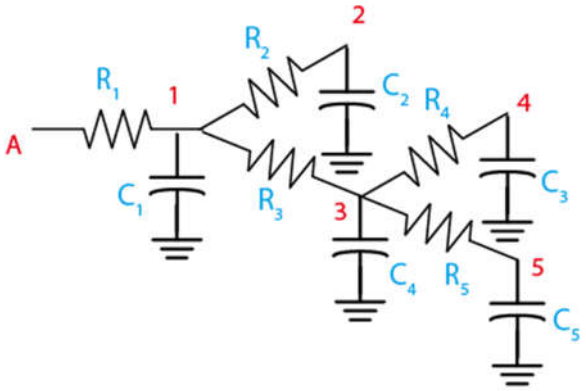
EECS 151/251A Homework 7

Due Monday, April 11th, 2022

Problem 1: Fun with RC Delay



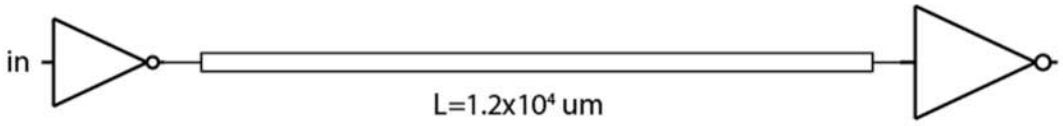
The value of each component in the RC network here is listed below:

Name	Value	Name	Value
C1	100 fF $(= 100 * 10^{-15} F)$	R1	1000 Ω
C2	50 fF	R2	1200 Ω
C3	60 fF	R3	1500 Ω
C4	20 fF	R4	1800 Ω
C5	30 fF	R5	2000 Ω

Find the RC delay constant τ from node A to node 4.

Problem 2: Wires Aren't Just Lines

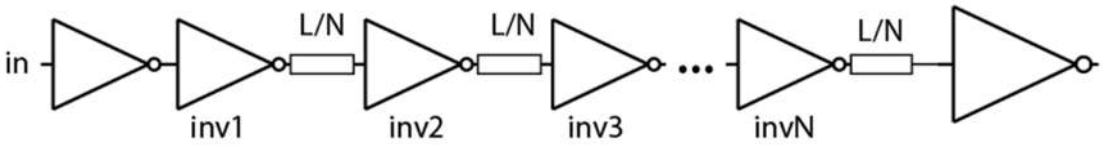
Assume we use a minimum sized inverter ($C_{g,min} = 0.3fF$) to drive an inverter **sized the twice of the first inverter** (i.e. gate lengths are the same as the minimum inverter, but widths are doubled). There is a long piece of wire in between those two inverters and its delay cannot be ignored.



The intrinsic delay the first inverter, $t_0 = ln2 * R_{eq,min}\gamma C_{g,min}$ is 4ps. $\gamma = 1.5$ for this technology. The resistance and capacitance of this wire is $r = 0.05\Omega/\mu m$ and $c = 0.2fF/\mu m$, respectively. The length of the wire is $L = 1.2 * 10^4 \mu m$.

(a) What is the total delay, t, of this circuit? Show your steps and write your final numerical answer.

(b) Now we are breaking up the wire into N equal segments and insert N identically sized inverters to achieve lower delay (there is no wire between the original first inverter and the inv1 we insert). If we cannot ignore the delay due to the inverters, what is the new total delay (in terms of N and the size of these inverters, S, and parameters given above. No need to write the numerical values.)



(c) **Optional Part** (this subpart won't be graded): People have found that, if the delay introduced by one inverter is equal to $ln2 * R_{eq,min}\gamma C_{g,min}$, then the minimum delay of inverter+wire segments is achieved when the number of stage, N, satisfies the following equation:

$$\frac{L}{N} = \sqrt{\frac{2R_{eq,min}C_{g,min}(1+\gamma)}{rc}}$$

If we use this conclusion, what would be the $N_{optimum}$ for (b)?