

# EECS 151/251A

## Discussion 10/worksheet

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# Administrativa

- Midterm 2 on Thursday 11/4
- Midterm review session Tuesday 11/2 (problems 4-7)
- How is the project?

# Agenda

- Midterm worksheet/problem examples

# Midterm 2 Topics!

Including:

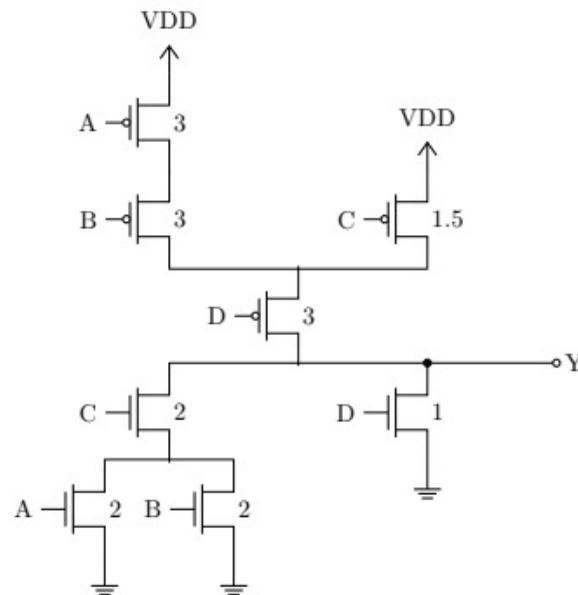
- CMOS
- Delay optimization and logical effort
- Power and energy
- Wires and RC models
- Arithmetic

# Problem 1 – CMOS Gate (Fa20 m2)

In this problem, use the process that has  $W_n = W_p = 1$  in a reference inverter, and  $\gamma = 1$ .

- (a) Design a complex CMOS gate:  $Y = \overline{(A + B) \cdot C + D}$ . Size the transistors so that the gate has the same pull-up and pull-down strength as a reference inverter.

**251A only:** Also make sure the parasitic delay ( $P$ ) is minimized in your design.



Sizing from worst-case path will guarantee the minimum overall area. In PMOS, A-B-D is the worst case and should be sized to 3. In NMOS, A/B-C is the worst case and should be sized to 2. The overall area (width) for PMOS is:  $3 + 3 + 3 + 1.5 = 10.5$ .

# Problem 1 – CMOS Gate (Fa20 m2)

(b) Calculate the logic effort for each input ( $LE_A, LE_B, LE_C, LE_D$ ).

$$LE_A = LE_B = \frac{3 + 2}{2} = 2.5$$

$$LE_C = \frac{1.5 + 2}{2} = 1.75$$

$$LE_D = \frac{3 + 1}{2} = 2$$

$$P = \frac{3 + 2 + 1}{2} = 3$$

# Problem 1 – CMOS Gate (Fa20 m2)

(c) **251A only:** Calculate the optimized parasitic delay  $P$ .

To minimize parasitic delay, we need to reduce the total parasitic capacitance at the output node. Moving smaller sized transistors in serial to the output can help. For example, in the schematic above, if NMOS A//B switch with NMOS C, the parasitic delay will be  $P = (3 + 2 + 2 + 1)/2 = 4$  instead.

We didn't require the minimum area in the description so other solutions will also be taken. For example, in PMOS network, if you size C and D to 2, then A in serial with B should have the same resistance with C, so  $A = B = 4$  ( $1/4 + 1/4 = 1/2$ ). The overall area for PMOS is:  $4 + 4 + 2 + 2 = 12 > 10.5$ .

As long as the logic effort calculation matches your schematic, you'll also get full credit in the second (and third) part.

# Problem 2 – Logical effort (Fa18 m2)

Reference inverter:  $W_p = 2W_n = W$ ,  $t_{p,inv} = 32\text{ps}$ ,  $\gamma = 2$

a) Determine path effort and optimal stage effort

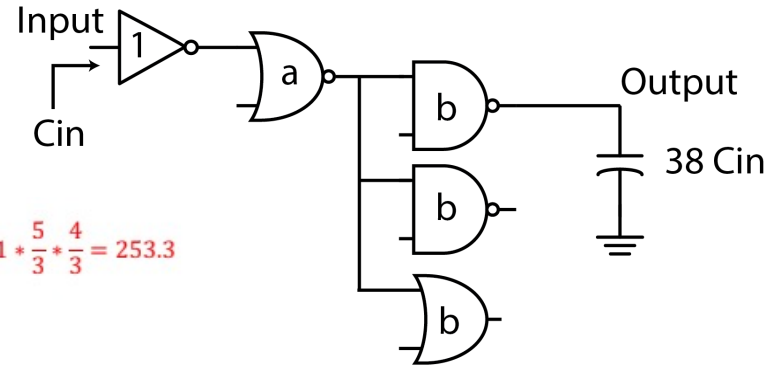
$$F = 38 \quad B = 3 \quad G = 20/9$$

$$PE = 253.3$$

$$EF = \sqrt[3]{PE} = 6.3$$

$$PE = F \Pi B \Pi LE = 38 * 3 * 1 * \frac{5}{3} * \frac{4}{3} = 253.3$$

$$EF_{opt} = \sqrt[3]{253.3} = 6.3$$



b) Find optimal a and b for minimum delay

$$b = \frac{\frac{1}{3} * 38 C_{in}}{6.3} = 8 C_{in}$$

$$a = \frac{\frac{5}{3} * 3 * 8 C_{in}}{6.3} = 6.3 C_{in}$$

$$= \frac{\frac{4}{3} * 38 C_{in}}{6.3} = 8 C_{in}$$

$$= \frac{\frac{5}{3} * 3 * 8 C_{in}}{6.3} = 6.3 C_{in}$$

c) Is this the optimal number of stages for delay? If not, what is?

$$N_{opt} = \frac{\log(253.3)}{\log(4)} \approx 4$$

Assuming fanout of 4:

$$EF^N = PE \rightarrow N = \frac{\log(253.3)}{\log(4)} = 4$$

So we should add an extra stage to minimize the delay.

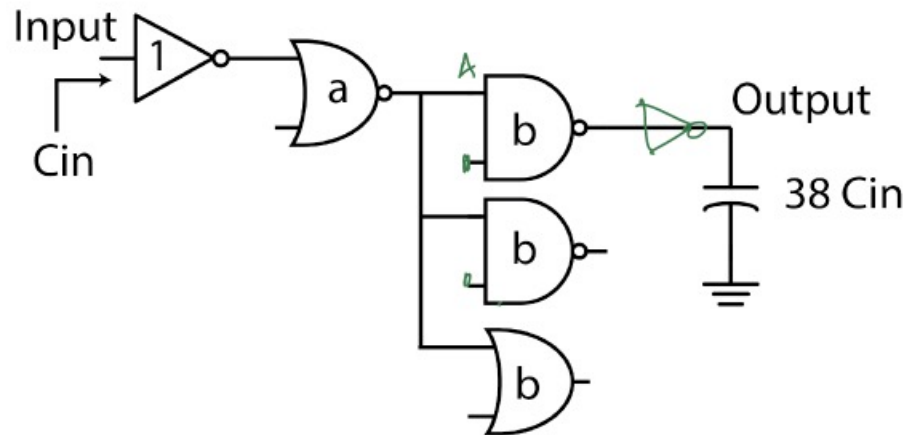


# Problem 2 – Logical effort (Fa18 m2)

Reference inverter:  $W_p = 2W_n = W$ ,  $t_{p,inv} = 32\text{ps}$ ,  $\gamma = 2$

- d) If we could add a single inverter anywhere along the critical path, where would be the best for the minimum total area?

$$EF = LE \cdot f$$



We would want to add the extra inverter at the end of the chain to minimize the area. The intuition is that we are going to have four stages with equal effective fanouts ( $EF=LE \cdot f$ ). If  $LE$  is smaller (inverter has the smallest), fanout would be larger. So putting the gate with larger fanout towards the end will reduce the input cap of the stage more, which results in smaller area.

# Problem 2 – Logical effort (Fa18 m2)

Reference inverter:  $W_p = 2W_n = W$ ,  $t_{p,inv} = 32\text{ps}$ ,  $\gamma = 2$

e) “Better” NAND gate logical effort?

$$LE_A = \frac{R_n (4C_j)}{R_n (3C_j)} = \frac{4}{3}$$

$$LE_{B \rightarrow H} = \frac{2R_n (3C_j)}{R_n (3C_j)} = 2$$

$$LE_{B \rightarrow L} = \frac{R_n (3C_j)}{R_n (3C_j)} = 1$$

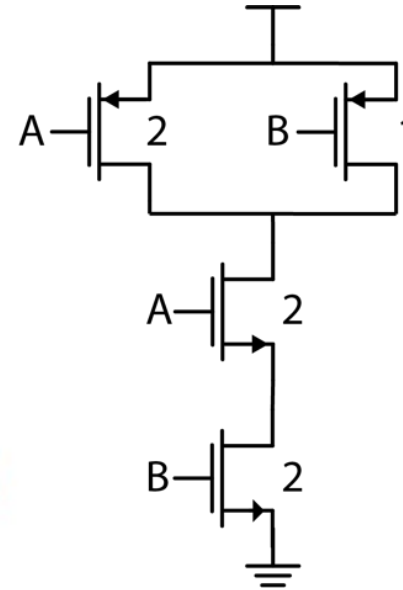
$$LE_B = \frac{3}{2}$$

$$LE_A = \frac{R_n (2C_g + 2C_g)}{R_n (2C_g + C_g)} = \frac{4}{3}$$

$$LE_{B,LH} = \frac{2R_n (C_g + 2C_g)}{R_n (2C_g + C_g)} = 2$$

$$LE_{B,HL} = \frac{R_n (C_g + 2C_g)}{R_n (2C_g + C_g)} = 1$$

$$LE_B = \frac{LE_{B,LH} + LE_{B,HL}}{2} = \frac{2 + 1}{2} = \frac{3}{2}$$



# Problem 2 – Logical effort (Fa18 m2)

Reference inverter:  $W_p = 2W_n = W$ ,  $t_{p,inv} = 32\text{ps}$ ,  $\gamma = 2$

f) “Better” NAND gate intrinsic delay parameter (p)?

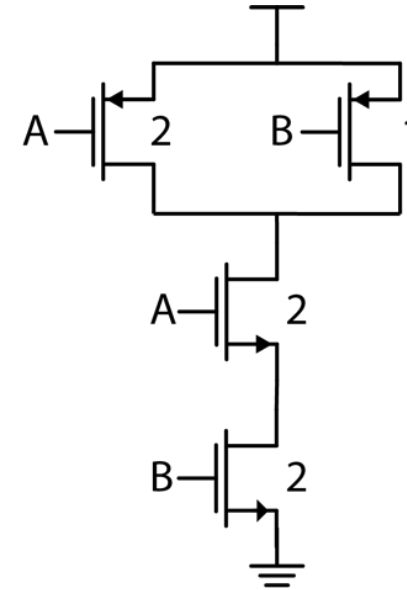
$$t_{p,inv} = \ln(2) R_{eq,inv} C_{in,inv}$$

$$p_A = \frac{R_n 5C_d}{R_n 3C_d} \gamma = \frac{10}{3}$$

$$p_{B \rightarrow H} = \frac{2R_n (5C_d)}{R_n (3C_d)} \gamma = \frac{20}{3}$$

$$p_{B \rightarrow L} = \frac{R_n (5C_d)}{R_n (3C_d)} = p_A = \frac{10}{3} \quad p_B = 5$$

$t_{p,calc} = t_{p,inv} (p + \dots)$   
 $\uparrow$   
 has to include  $\gamma$



$$p_A = \frac{R_n (5C_d)}{R_n (3C_d)} \gamma = \frac{5}{3} * 2 = \frac{10}{3}$$

$$p_{B,LH} = \frac{2R_n (5C_d)}{R_n (3C_d)} \gamma = \frac{10}{3} * 2 = \frac{20}{3}$$

$$p_{B,HL} = \frac{R_n (5C_d)}{R_n (3C_d)} \gamma = \frac{5}{3} * 2 = \frac{10}{3}$$

$$p_B = \frac{p_{B,LH} + p_{B,HL}}{2} = 5$$

g) How does this affect the delay of our original chain?

$p_A$  has been reduced from 4 to 3.3 which means faster critical path. However, the other path through B input is now slower. Also logical effort of B is increased which means more drive strength is needed for it.

# Problem 3 (Fa19 m2)

## 4) Delays and Adders (18 points, 22 minutes)

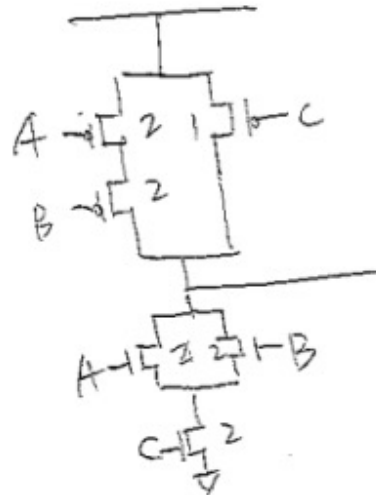
You are designing a datapath in a brand-new CMOS FinFET technology, where NMOS and PMOS devices have equal strength. In particular, it has only four CMOS gates: 2- input NAND, 2-input NOR, 2-input XOR, and an OAI21 gate ( $Y = \overline{(A+B)C}$ ). Gate capacitance equals drain capacitance per unit area ( $\gamma = 1$ ), and the four gates come in with only one size each, i.e., you do not need to size gates in this problem.

- a) If both the 2-input NAND gate and the 2-input NOR gate have a delay dependence on a fanout,  $f$ , given as  $t_{\text{NAND}2} = t_{\text{NOR}2} = 2\text{ns}(4 + 3f)$ , what is the delay dependence on the fanout of the input C of the OAI21 gate (C is in the critical path)?

$$p = \frac{7}{2}$$

$$q = 2$$

$$t_{\text{AOI21}} = \underline{2\text{ns}(7 + 4f)}$$

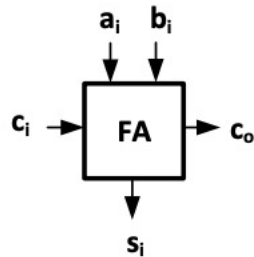


$$p = \frac{3+2+2}{2} = \frac{7}{2}$$

$$q = \frac{2+2}{2} = 2$$

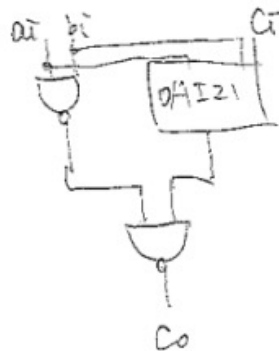
# Problem 3 (Fa19 m2)

- b) Draw a fast full-adder using the four types of gates and calculate the  $c_i \rightarrow \text{sum}$  and  $c_i \rightarrow \text{cout}$  delay. Note that using an OAI21 gate could potentially simplify the logic for  $C_{\text{out}}$ . Assume the capacitance driven by the sum and the carry bits is equal to the capacitance of inputs  $a_i$ ,  $b_i$  and  $t_{\text{XOR2}} = 2\text{ns} (8 + 8f)$ .



$$S = a_i \oplus b_i \oplus C_{\text{out}}$$

$$C_o = \overline{a_i b_i} + (a_i + b_i) C_i = (\overline{a_i b_i}) \cdot \overline{(a_i + b_i) C_i}$$



$$\therefore t_{FA, c_i \rightarrow C_o} = 2\text{ns} (7 + 4f + 4 + 3f) = 2\text{ns} (11 + 7f)$$

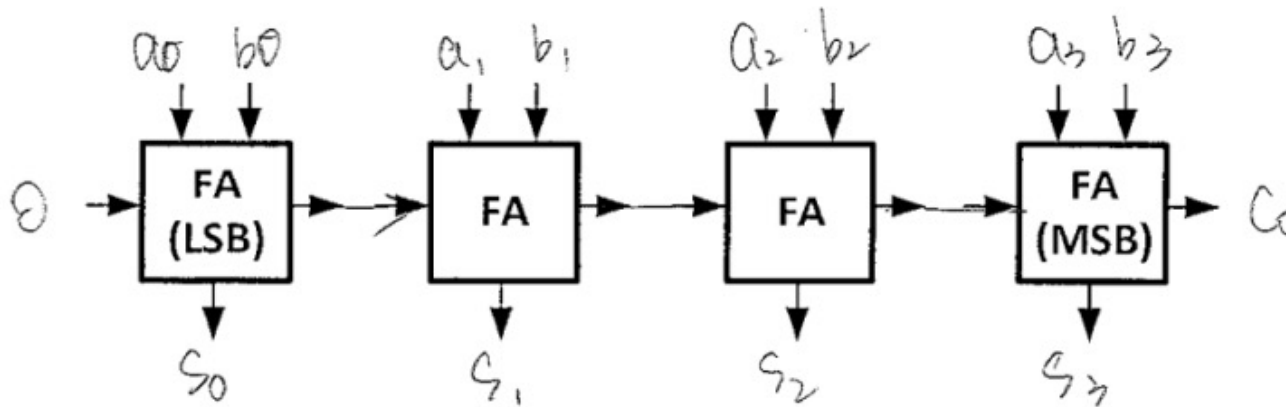
$$a_i \Rightarrow \text{XOR} \Rightarrow \text{XOR} \Rightarrow S \quad C_i \Rightarrow \text{AND} \Rightarrow S \quad \therefore t_{FA, c_i \rightarrow S} = 2\text{ns} (8 + 8f)$$

$$t_{FA, c_i \rightarrow C_o} = \underline{2\text{ns} (11 + 7f)}$$

$$t_{FA, c_i \rightarrow S} = \underline{2\text{ns} (8 + 8f)}$$

# Problem 3 (Fa19 m2)

- c) Complete the drawing and label all inputs and outputs for an 4-bit ripple-carry adder in figure below by using full-adder (FA) cells from part b). Inputs are  $a[3:0]$  and  $b[3:0]$  and there is no carry-in to the least-significant bit.



# Problem 3 (Fa19 m2)

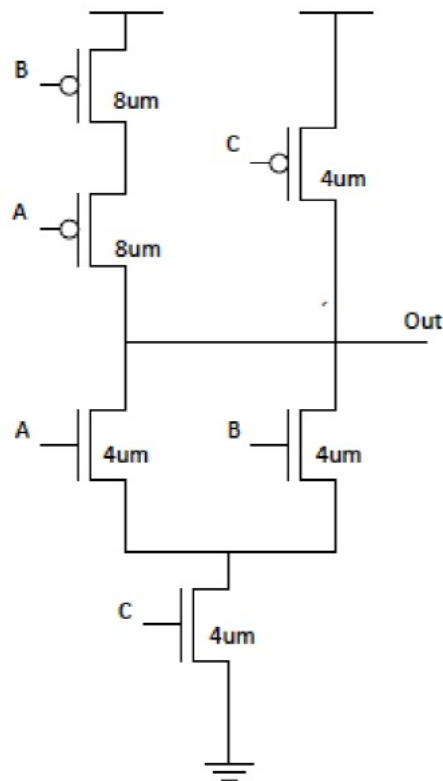
- d) Find the critical path delay for the circuit in part c), if the capacitance driven by the sum and the carry bits is equal to the input  $a_i$ ,  $b_i$  capacitance. If you are not confident in your answer in part b), you can express the delay in terms of  $t_{FA,Ci \rightarrow Co}$ , and  $t_{FA,Ci \rightarrow S}$

$$t_{\text{delay}} = 3t_{FA,Ci \rightarrow Co} + t_{FA,Ci \rightarrow S}$$

Critical path = \_\_\_\_\_.

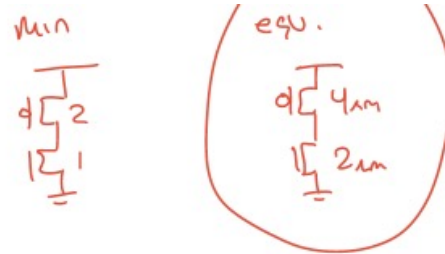
# Problem 4 Logical effort (Sp13)

Logical effort and intrinsic delay?



$$R_p = 2R_n$$

$$\gamma = 1$$



$$LE = \frac{R_{gate} C_{gate}}{R_{inv} C_{inv}}$$

$$LE_A = LE_B = \frac{12C_g}{6C_g} = 2$$

$$p = \frac{20C_D}{6C_g} \gamma = \frac{10}{3}$$

Note that the resistance is not matched with that of the reference inverter. One way to deal with this is to assume that your reference inverter is a 4um/2um inverter. Now the resistance is matched and you can work only with capacitances. (Alternatively, you can use the equation

$$LE = \frac{R_{gate} C_{gate}}{R_{inv} C_{inv}}$$

$$LE_A = \frac{(8um + 4um)C_g}{(4um + 2um)C_g} = \frac{12}{6} = 2$$

$$LE_B = \frac{(8um + 4um)C_g}{(4um + 2um)C_g} = \frac{12}{6} = 2$$

$$LE_C = \frac{(4um + 4um)C_g}{(4um + 2um)C_g} = \frac{8}{6} = \frac{4}{3}$$

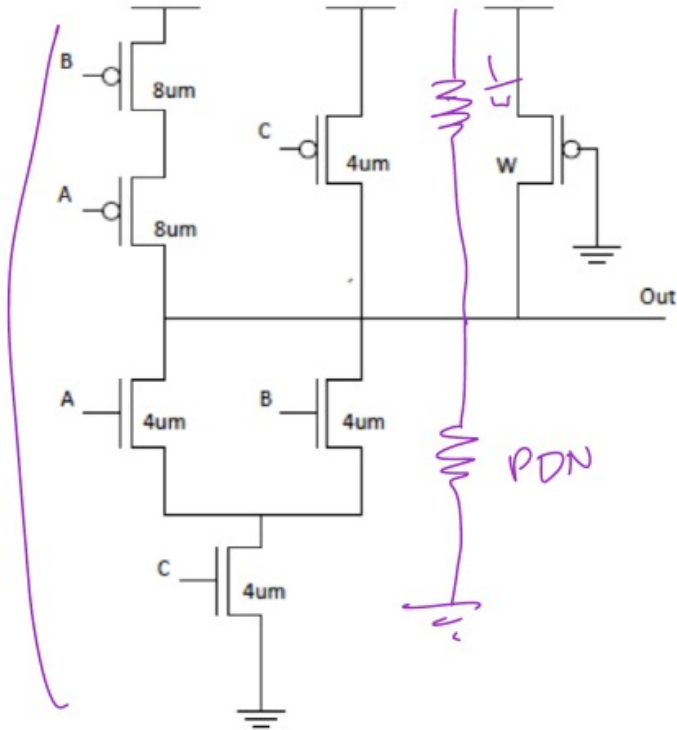
$$\begin{aligned} LE_A &= 2 \\ LE_B &= 2 \\ LE_C &= 4/3 \end{aligned}$$

$$p = \frac{(8um + 4um + 4um + 4um)C_d}{(4um + 2um)C_g} = \frac{20}{6} \gamma = \frac{10}{3}$$



# Problem 4 Logical effort (Sp13)

- Made a mistake in layout! What is the effect on L-H transition? H-L transition?



L → H : PMOS helps pull high  
→ faster !

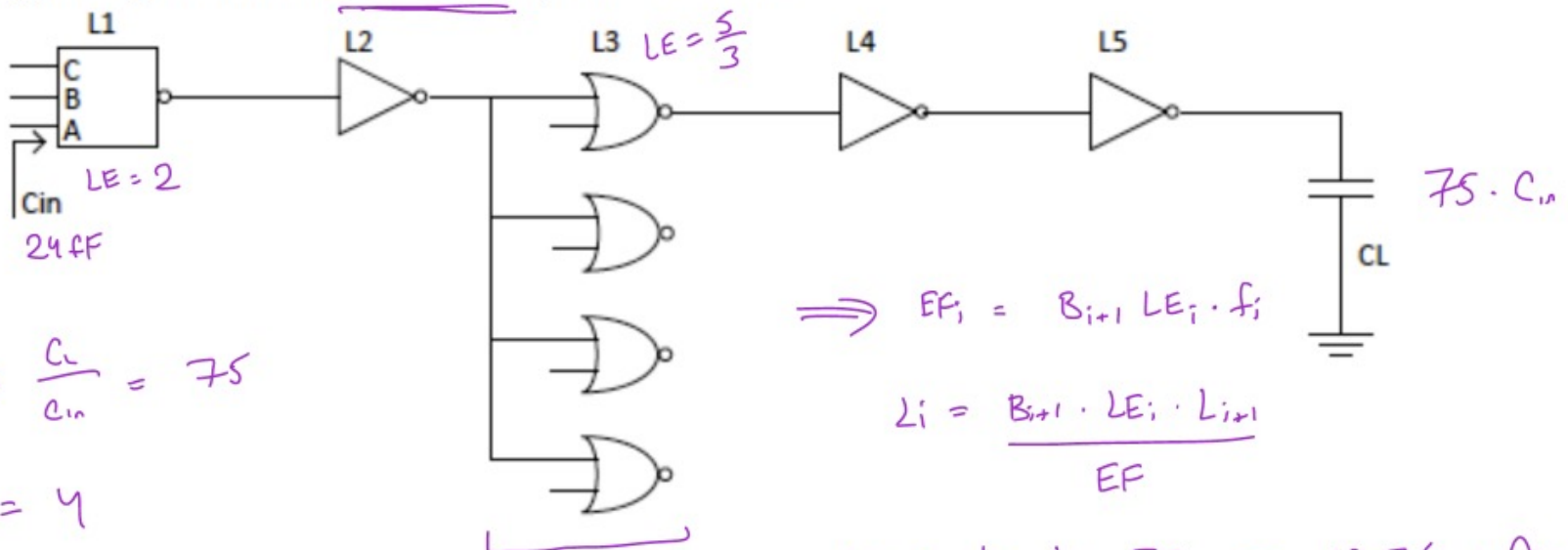
H → L : PMOS works against PDN  
→ slower !

# Problem 4 Logical effort (Sp13)

- Delay optimization with **fixed gate**
- Using A input with  $C_{in} = 24 \text{ fF}$ ,  $C_L = 75C_{in}$

$$B = \frac{C_{total}}{C_{core\ object}}$$

$$\gamma = 1 \cdot 2 \cdot 1.95$$



$$F = \frac{C_L}{C_{in}} = 75$$

$$B = \gamma$$

$$G = \frac{10}{3}$$

$$PE = FB6 = 1000$$

$$EF = \sqrt[5]{1000} \approx 4$$

$$\Rightarrow EF_i = B_{i+1} LE_i \cdot f_i$$

$$L_i = \frac{B_{i+1} \cdot LE_i \cdot L_{i+1}}{EF}$$

$$L_5 = \frac{1 \cdot 1 \cdot 75}{4} = 18.75 \cdot C_{in}$$

$$L_4 = \frac{1 \cdot 1 \cdot 18.75}{4} \approx 4.69$$

$$L_3 = \frac{1 \cdot \frac{5}{3} \cdot 4.69}{4} \approx 1.95$$

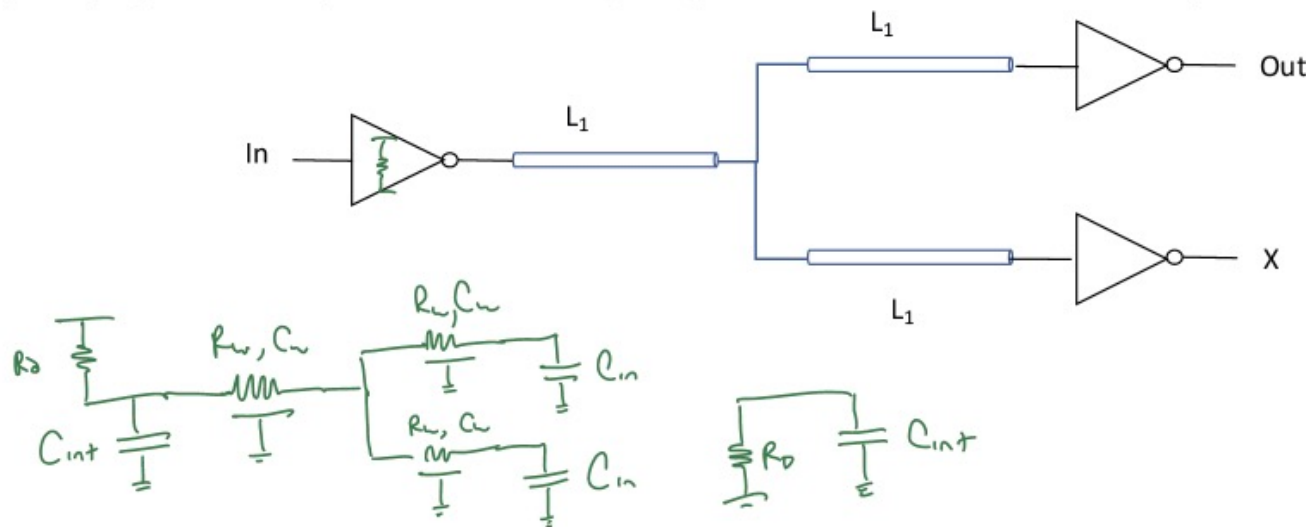
$$L_2 = \frac{4 \cdot 1 \cdot 1.95}{4} = 1.95$$

# Problem 5 – Wires and repeaters (fa18 m2)

Min. inverter: drive resistance  $R_d$ , input cap  $C_{in}$ , intrinsic cap  $C_{int}$

Wire:  $r_w$ ,  $c_w$  (per unit length)

a + b) Propagation delay from *in* to *out* (using distributed model for wires)



$$R_w = L_1 r_w$$

$$C_w = L_1 c_w$$

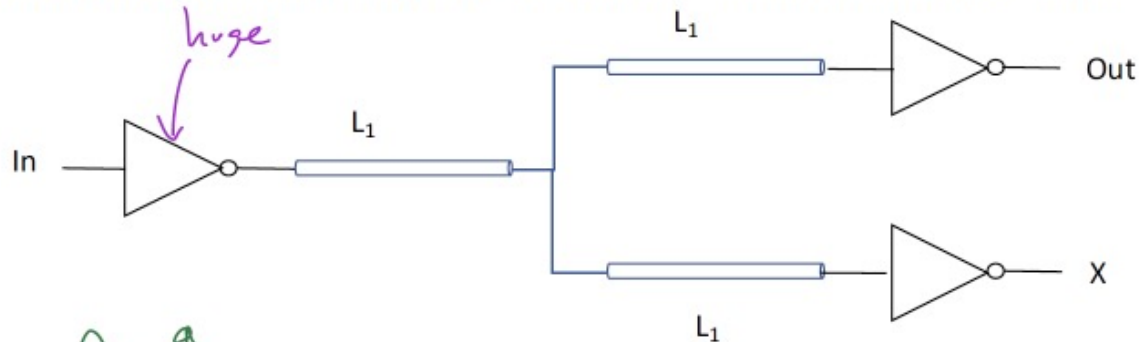
$$t_d = \ln(2) \left[ R_d (C_{int} + 3C_w + 2C_{in}) + R_w \left( \frac{C_w}{2} + 2C_w + 2C_{in} \right) + R_w \left( \frac{C_w}{2} + C_{in} \right) + R_d C_{int} \right]$$

# Problem 5 – Wires and repeaters (fa18 m2)

Min. inverter: drive resistance  $R_d$ , input cap  $C_{in}$ , intrinsic cap  $C_{int}$

Wire:  $r_w$ ,  $c_w$  (per unit length)

c) Derive reduction in delay by increasing the first inverter as much as possible:



$R_d \downarrow$ ,  $C_{int} \uparrow$

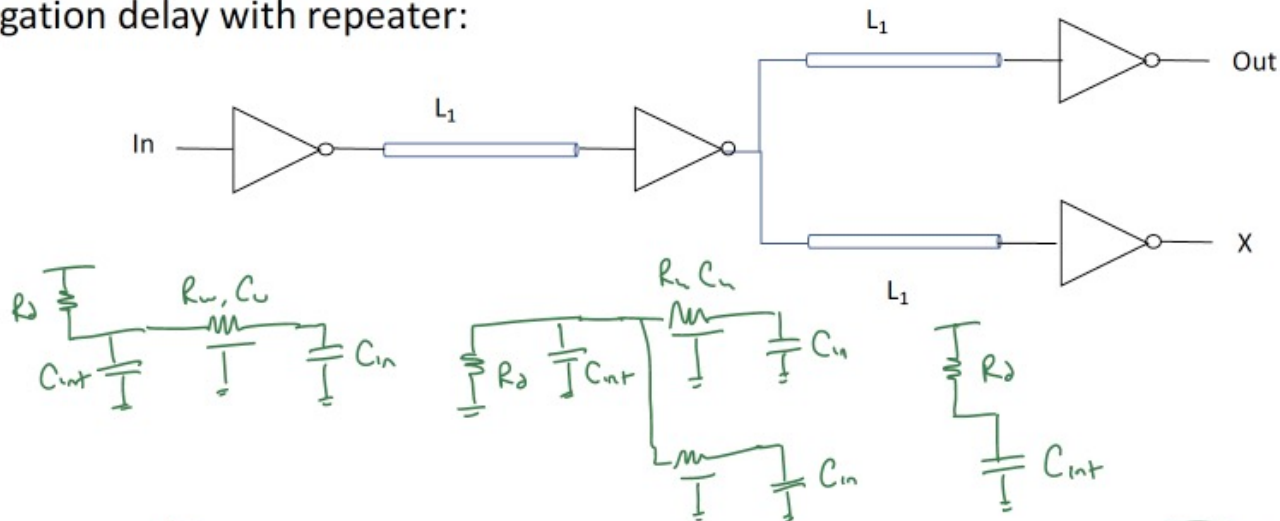
$$t_d = \ln(2) \left[ \overbrace{R_d (C_{int} + \underline{3C_w} + \underline{2C_n})}^{R_d C_{int}} + R_w \left( \frac{C_w}{2} + 2C_w + 2C_n \right) + R_w \left( \frac{C_w}{2} + C_n \right) + R_d C_{int} \right]$$

# Problem 5 – Wires and repeaters (fa18 m2)

Min. inverter: drive resistance  $R_d$ , input cap  $C_{in}$ , intrinsic cap  $C_{int}$

Wire:  $r_w$ ,  $c_w$  (per unit length)

d) Propagation delay with repeater:



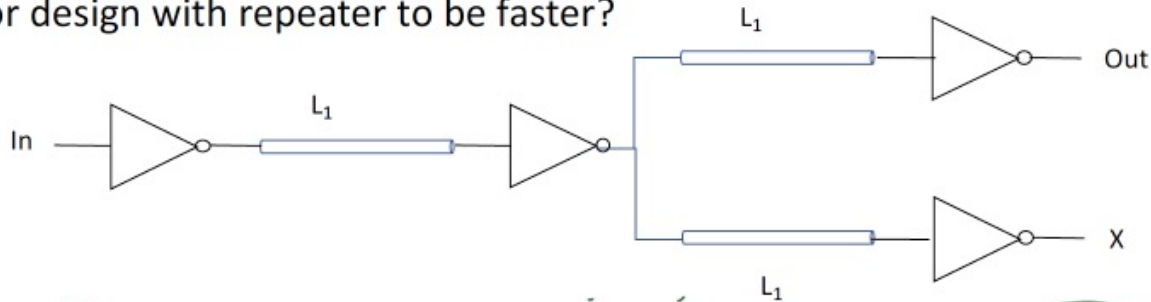
$$t_d = \ln(2) \left[ \begin{aligned} &R_d (C_{int} + C_w + C_{in}) + R_w \left( \frac{C_w}{2} + C_{in} \right) \\ &+ R_d (C_{int} + 2C_w + 2C_{in}) + R_w \left( \frac{C_w}{2} + C_{in} \right) \\ &+ R_d C_{int} \end{aligned} \right]$$

# Problem 5 – Wires and repeaters (fa18 m2)

Min. inverter: drive resistance  $R_d$ , input cap  $C_{in}$ , intrinsic cap  $C_{int}$

Wire:  $r_w$ ,  $c_w$  (per unit length)

e) Conditions for design with repeater to be faster?



$$t_d = \ln(2) \left[ \begin{aligned} &R_d (C_{int} + C_w + C_n) + R_w \left( \frac{C_w}{2} + C_n \right) \\ &+ R_d (C_{int} + 2C_w + 2C_n) + R_w \left( \frac{C_w}{2} + C_n \right) \\ &+ R_d C_{int} \end{aligned} \right]$$

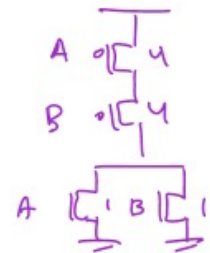
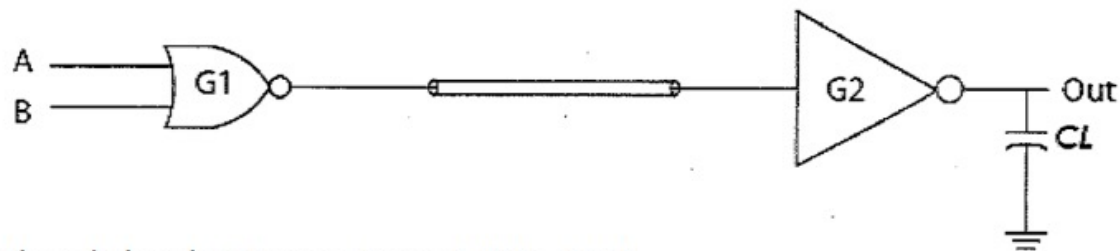
additional  
 $R_d (C_{int} + C_n)$

lost  
 $R_w (2C_w + C_n)$

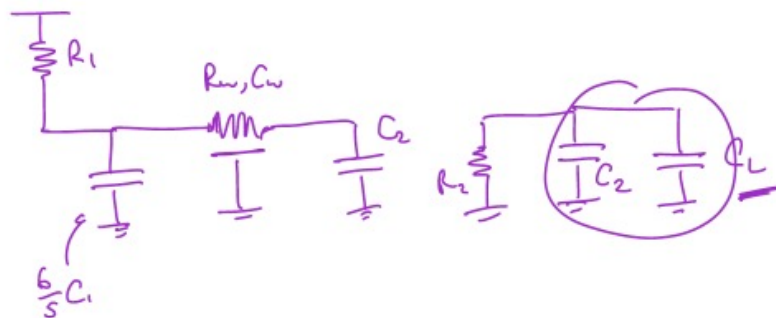
$$t_d = \ln(2) \left[ \begin{aligned} &R_d (C_{int} + 3C_w + 2C_n) + R_w \left( \frac{C_w}{2} + 2C_w + 2C_n \right) \\ &+ R_w \left( \frac{C_w}{2} + C_n \right) + R_d C_{int} \end{aligned} \right]$$

# Problem 6 - Wires and Energy (Sp16)

A NOR gate (G1) with input capacitance  $C_1$  is driving a wire with total resistance  $R_W$  and total capacitance  $C_W$ , and an inverter with input capacitance  $C_2$ . Inverter G2 is driving an external load of  $C_L$ . The on-resistance of G1 and G2 are  $R_1$  and  $R_2$ , respectively. Assume  $\gamma = 1$  and  $2R_N = R_P$ . The power supply has a voltage of  $V_{DD}$ .



a) Determine the delay between input A to Out



$$\begin{aligned} C_{in} &= 5C_1 \\ C_{int} &= 6C_1 = 6C_2 \\ &= \frac{6}{5}C_{in} \end{aligned}$$

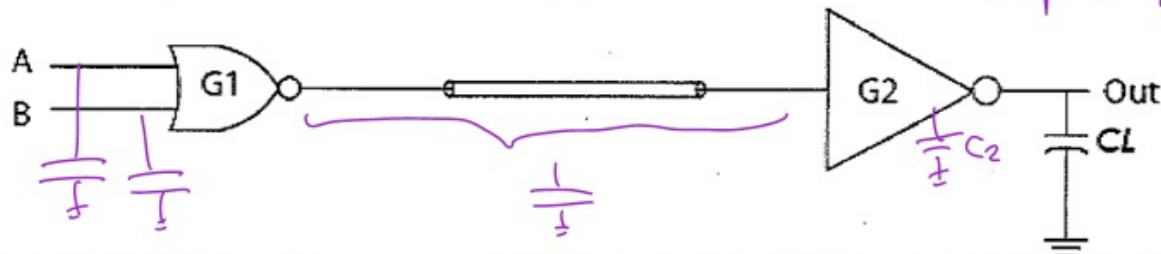
$$\begin{aligned} \tau &= R_1 \left( \frac{6}{5}C_1 + C_W + C_2 \right) + R_W \left( C_2 + \frac{C_W}{2} \right) + R_2 (C_2 + C_L) \\ t_p &= \ln(2) \tau \end{aligned}$$



# Problem 6 - Wires and Energy (Sp16)

A NOR gate (G1) with input capacitance  $C_1$  is driving a wire with total resistance  $R_W$  and total capacitance  $C_W$ , and an inverter with input capacitance  $C_2$ . Inverter G2 is driving an external load of  $C_L$ . The on-resistance of G1 and G2 are  $R_1$  and  $R_2$ , respectively. Assume  $\gamma = 1$  and  $2R_N = R_P$ . The power supply has a voltage of  $V_{DD}$ .

$$P = \alpha_{2 \rightarrow 1} C V_{DD}^2 f$$



b) Assume input A is driven by a square-wave signal of frequency  $f_{clk}$  and input B is driven by a square wave signal of frequency  $\frac{1}{3}f_{clk}$ . Derive an expression for total dynamic power consumption of the circuit.

A

B

G1 out

$$P_{in1} = f_{clk} C_1 V_{DD}^2 + \frac{f_{clk}}{3} C_1 V_{DD}^2$$

$$P_{out1} = \frac{2}{3} f_{clk} \left( \frac{6}{5} C_1 + C_W + C_2 \right) V_{DD}^2$$

$$P_{out2} = \frac{2}{3} f_{clk} (C_2 + C_L) V_{DD}^2$$



# Problem 7 - adder (Sp19 final)

22. Adder Design [5pts]: The carry-select technique presented in lecture can be applied hierarchically. Imagine applying the technique in a binary way—a larger adder is divided in half using the carry-select and then the same technique is applied to the sub-adders, etc. The process would stop at 4-bit ripple adders.

(a) Assuming a FA and a MUX both have unit delay (delay = 1), what would be the delay (from data in to carry out) of a 32-bit adder?

(b) How would the delay scale with the size of the adder?

# Problem 7 - adders (Sp19 final)

23. Adder Design [6pts]: A carry-lookahead adder used to add  $A$  to  $B$  is organized into groups of 4-bits. A group has carry into the group,  $c_{i-1}$  and carry out of the group,  $c_{i+3}$ .
- (a) In terms of the propagate and generate signals,  $p_i$  and  $g_i$ , of the individual bit stages, write an expression for the *group propagate signal*,  $P$  and *group generate signal*,  $G$ .
- (b) Write an expression for  $c_{i+3}$  based on the group  $P$  and  $G$ .
- (c) Write an expression for the bit stage sum output,  $s_i$ .