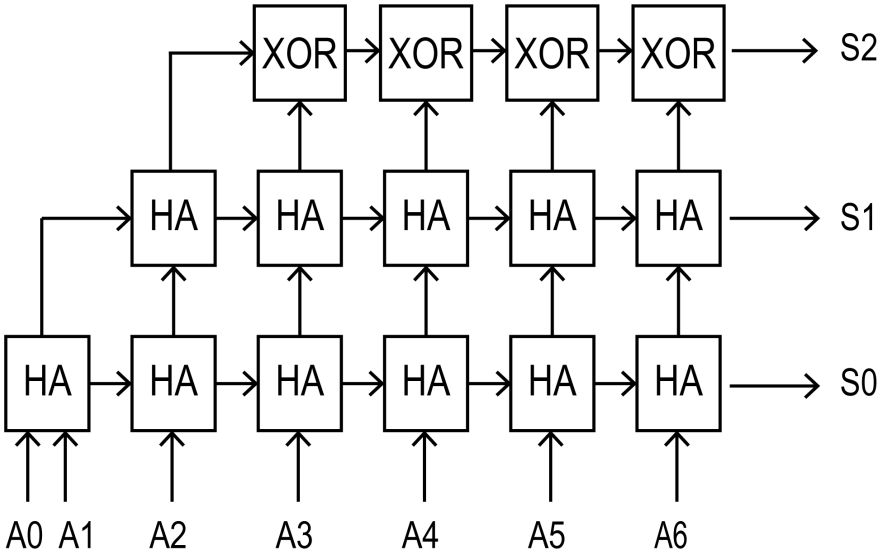
EECS 151/251A Homework 8

Due 11:59pm Monday, November 8th, 2021

1 Adder

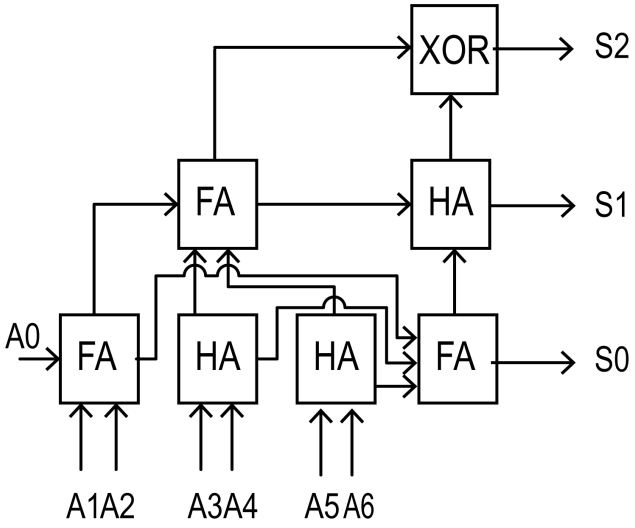
In this problem we will look at designing a circuit that adds together seven 1-bit binary numbers $A_{6:0}$ into one 3-bit output $S_{2:0}$ (whose value ranges from 0 to 7).

a Shown below is a simple implementation of this circuit that uses only half adders (HA), and XOR gates. Assuming that the sum and carry delays of the half adders are equal to each other and to the delay of the XORs (all of them equals t_{gate}), How many gate delays are there on the critical path of this circuit?



The critical path delay = [ ] gate delays (t_{gate}).

Solution:
8 (6 HA in first layer + 1 HA in the second layer and + 1XOR))



b A better implementation for this circuit is shown above. Under the same assumptions as part (a) and assume the delay for carry and sum output of full adder (FA) are also t_{gate}. How many gate delays are on the critical path of this circuit.

The critical path delay = [ ] gate delays (t_{gate}).

Solution:
4 (lower left FA + HA that generates S0 + HA that generate S1 + XOR)

c (251 only) Still using only full adders, half adders, and XORs, draw an implementation for this circuit that has the minimum critical path. Write the number of each blocks you used in your design and the critical path delay in the blanks below. Again, assume all blocks have same delay.

Write numbers of each gate you used:

[ ] × Full Adders

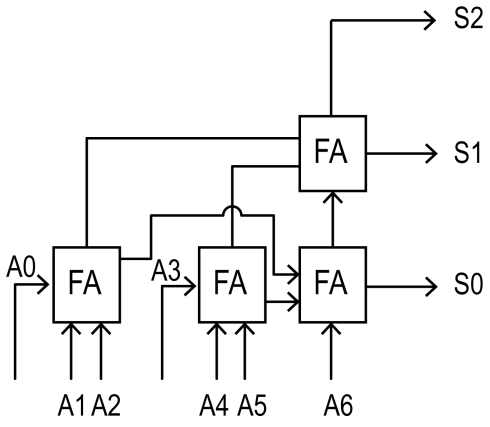
[ ] × Half Adders

[ ] × XOR Gates

The critical path delay = [ ] gate delays (t_{gate}).

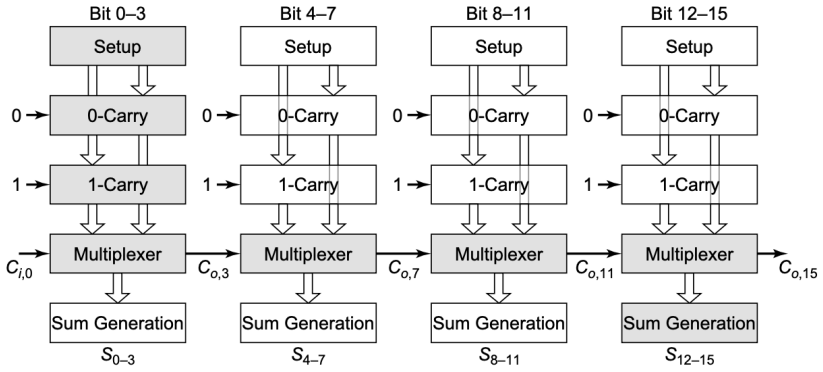
Solution:

4 FA, t = 3 unit delays



2 Carry Select Adder

a Consider the design of a 36-bit carry select adder (The pictures shown below is an example of 16-bit). Assume uniform block size (each block has same input bit width), what block sizes would you use to result in the minimum worst case delay? Assume that $\tau_{setup} = \tau_{carry} = \tau_{mux} = \tau_{sum} = \tau_u$. Here, τ_{carry} and τ_{sum} are the delay for a full(half) adder. What's the total delay of the critical path? Write your answer in terms of τ_u



The critical path delay= [ ] τ_u.

Solution:

$t_{critical} = \tau_{setup} + \tau_{sum} + 6\tau_{FA} + 6\tau_{mux} = 14\tau_u$

b (251 only) Consider the design of a 36-bit carry select adder. But it allows to use variable size of blocks, the input width for each block can be any integer larger than 2. Try to minimize the worst case delay of the critical path. Assume that $\tau_{setup} = \tau_{carray} = \tau_{mux} = \tau_{sum} = \tau_u$.

Size the blocks in your design from LSB to MSB, write your answer in the blank below, separated by `,` . For example [`4, 4, 4, 4, 4, 4, 4, 4, 4`] And what's the total delay of the critical path in your design? Write your answer in terms of τ_u

From LSB to MSB the block sizes are: [ ]

The critical path delay = [ ] τ_u.

Solution:

Two possible solutions are: 4, 5, 6, 6, 7, 8 or 3, 3, 4, 5, 6, 7, 8(From LSB to MSB) $t_{critical} = \tau_{setup} + \tau_{sum} + 8\tau_u = 12\tau_u$

It might be better solution. we want our blocks to compute their addition just in time for the signal to be available to the select MUX. That signal arrives from upstream (lesser significant bits). We can afford to compute an extra bit of addition while waiting for the MUX. So each subsequent block downstream should be 1 extra bit in width.

3 Booth Recording

a Calculate this multiplication use booth recording

```
 01101 (A)
×01010 (B)
```

It's translated(encoded) to several actions, select the correct actions

A) Add 0, Sub A, Add A

B) Sub 2A, Sub A, Add A

C) Sub A, Sub A, Add A, Add A

D) Add 0, Add A, Add A

E) None of the above

Solution:

B - 100 (Sub 2A), 101(Sub A), 001(Add A)

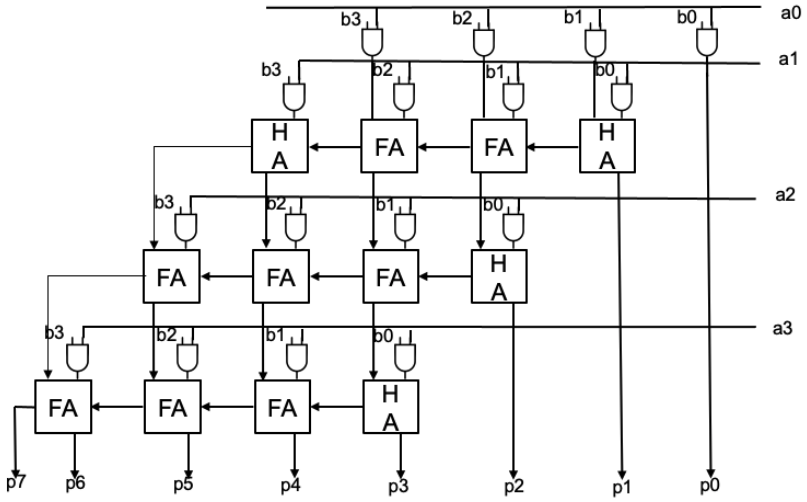
b What's the result of multiplication?: (in a 10-bit binary)

Solution:

0010000010

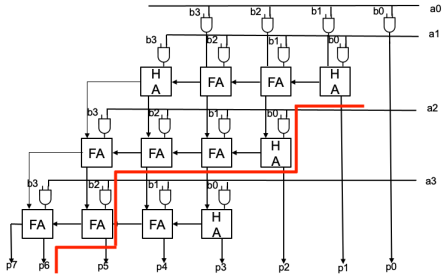
4 Multiplication

a Following is the multiplier structure in the lecture slides (4x4, diagram shown below), compute the critical path for a 5 x 5 multiplier. Assume FA and HA have $t_{HA,carry} = t_{FA,carry} = t_{HA,sum} = t_{FA,sum} = t_{FA}$. Write your answer in terms of t_{FA} and t_{and}.



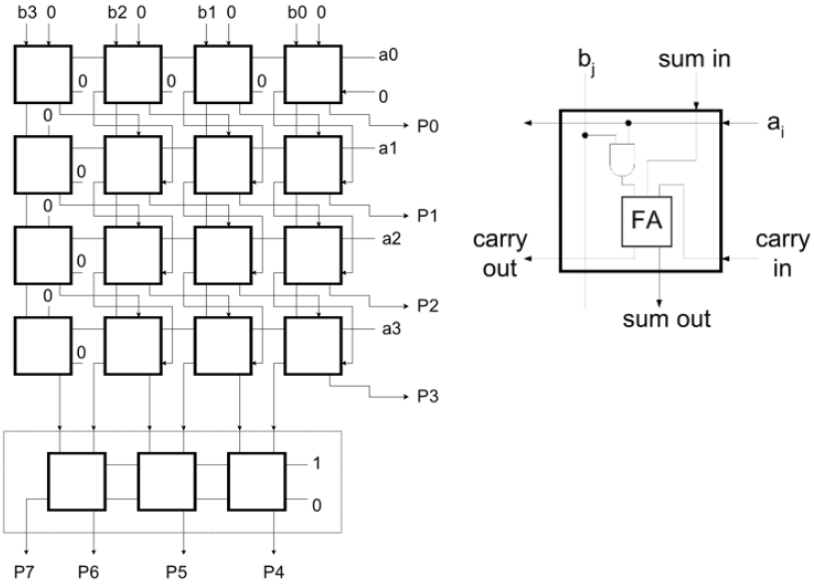
The critical path delay = $\square \times t_{FA} + \square \times t_{and}$

Solution:



$$t_{critical} = 11t_{FA} + t_{and}$$

b Now consider the array multiplier using carry-save addition, for a 5 x 5 carry-save multiplier and compute the critical path. The figure below shows a 4x4 example from lecture slides. Again, assume FA have $t_{FA,carry} = t_{FA,sum} = t_{FA}$ and the final stage carry propagate adder takes t_{add}.



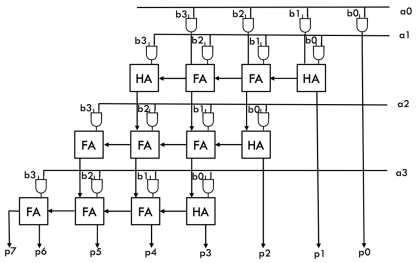
The critical path delay = $\square \times t_{add} + \square \times t_{FA} + \square \times t_{and}$

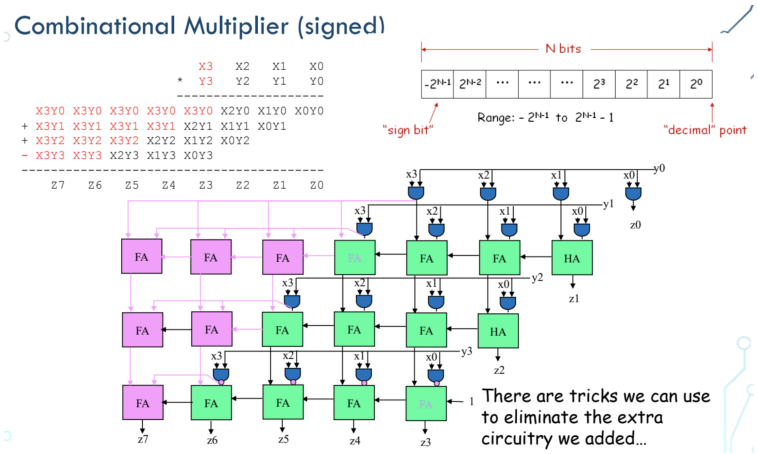
Solution:

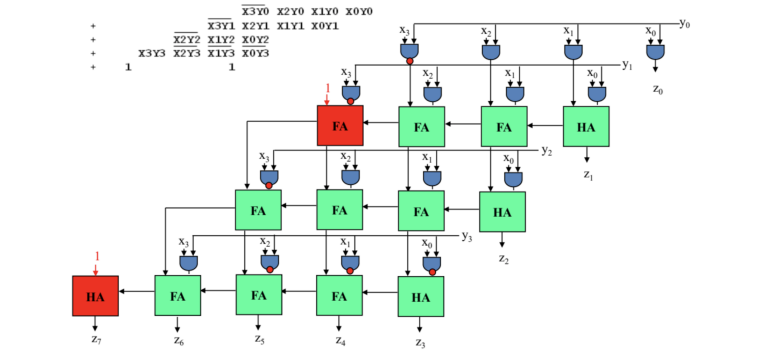
$t_{critical} = t_{add} + 5t_{FA} + t_{and}$

5 Signed multiplier

Refer to the diagrams below. For each of the multiplier below. Count how many FA and HA are needed.







a A 4-bit x 4-bit unsigned multiplier.

Write the numbers of each block needed:

☐ × Full Adders

☐ × Half Adders

b A 4-bit x 4-bit signed combinational multiplier

Write the numbers of each block needed:

☐ × Full Adders

☐ × Half Adders

c) A 4-bit x 4-bit signed 2's complement (Baugh-Wooley) multiplier

Write the numbers of each block needed:

☐ × Full Adders

☐ × Half Adders

Solution:

1. 8 full adders and 4 half adders
2. 16 full adders and 2 half adders
3. 9 full adders and 4 half adders