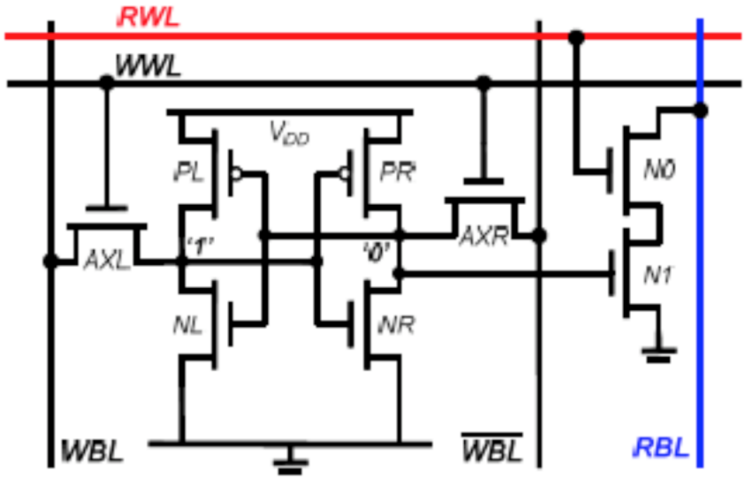
EECS 151/251A Homework 10

Due 11:59pm Tuesday, November 23th, 2021

1 8T SRAM Cell

Consider the 8T SRAM cell given below. With this design, there is a Write Word Line (WWL) that is used to write the values of the Write Bit Line (WBL) and $\overline{WBL}$ into the cell, and a separate Read Word Line (RWL) that is used to read the contents of the cell on the Read Bit Line (RBL). Refer to any transistor by the label in the diagram (eg. PL).



(a) List the transistors that are involved in a Write operation in order of relative strength (from strongest to weakest), if there is any such ordering.

(b) For the same cell, determine which transistors are involved in a Read operation, and list them in order of relative strength (from strongest to weakest), if there is any such ordering.

(c) True or false: the 4 transistors in the cross-coupled inverters in this cell may all be made minimum size without worsening read stability.

(d) True or false: the 4 transistors in the cross-coupled inverters in this cell may all be made minimum size without worsening writeability.

2 Physical Array Organization

You would like to instantiate an SRAM array that has 1024 entries of 8 bits. Assume an SRAM cell is $0.12\mu m$ high and $0.5\mu m$ wide (where the wordline is horizontal and the bitline is vertical). Assume wire capacitance of $0.2fF/\mu m$, and supply voltage of 0.9V.

(a) What are the dimensions of an array that has 1024 rows and 8 columns (assume that the cells directly abut)?

(b) If you build an array of 1024 rows and 8 columns, how much energy is used to drive the wordline?

(c) If you build an array of 1024 rows and 8 columns, how much energy is discharged from the bitlines (assuming the wordline is left on for a long time)?

(d) You can change the physical shape of an array by using bit-interleaving. For a 4 to 1 interleaved design, every 4th bit in a row belongs to a single word (the 0th, 4th, 8th, ... bits form entry 0, the 1st, 5th, 9th, ... bits form entry 1, the 2nd, 6th, 10th, .. bits form entry 2, and the 3rd, 7th, 11th, ... bits form entry 3 along a single row). If the 1024 entry x 8 bit word design is interleaved 4 to 1, how many rows and columns are there?

(e) Assuming the same interleaving as part (d), which address bits are used to select the word?

(f) Assuming the same interleaving as part (d), which address bits are used for the column select mux?

(g) Assuming the same interleaving, how much energy is used in the wordlines?

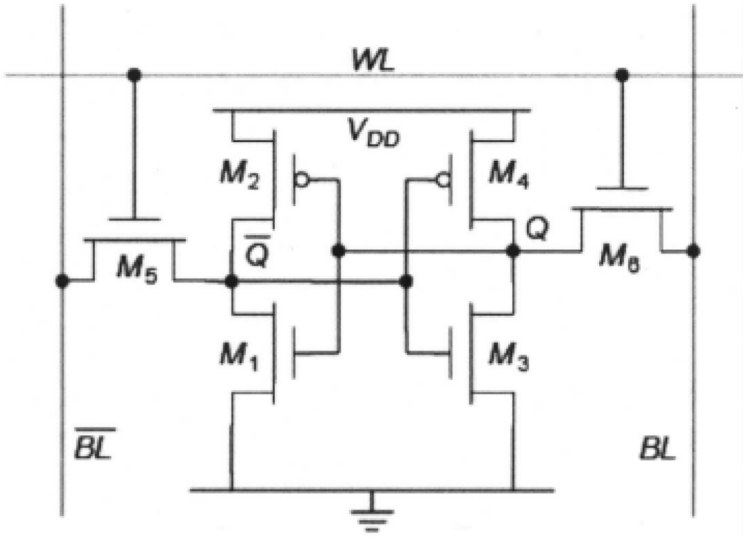
(h) Assuming the same interleaving, how much energy is used in the bitlines?

(i) (**EECS251A Only**) Suppose we want to design a row decoder for the reshaped array in part (d). Assume the input capacitance of each cell is $0.2fF$, and the decoder input capacitance is constrained to be $0.8fF$. Note that with the minimum possible transistor size in this technology, the C_{in} for an inverter is $0.1fF$. What is the total fanout for one bit of the decoder?

(j) (**EECS251A Only**) What is the optimal number of stages to minimize the delay of the decoder for a given input bit?

3 6T SRAM Cells

For the SRAM cell shown below, the widths of M1 and M3 are $240nm$, the widths of M2 and M4 are $120nm$, and the widths of M5 and M6 are $120nm$.



For this technology, you are given that $V_{DD} = 1V$ and $C_D = C_G = 2fF/\mu m$. The dimensions of the cell are $3\mu m$ x $3\mu m$ and the cell is part of a 256 x 256 memory array. Each bitline runs in Metal 2 with $0.12\mu m$ width and $C_{pp} = 7aF/\mu m^2$, $C_{fr} = 14aF/\mu m$. Bitlines are pre-charged to V_{DD} for read, and in order to speed up the read operation, thay are connected to (ideal) differential sense amplifiers, which instantly evaluate the correct output once their input differential voltage is $500mV$.

(a) Looking at the whole memory block, calculate the read access time assuming $R_N = 1.5k\Omega * \mu m$. (Note: assume device capacitance on internal cell nodes is negligible)

(b) How much energy is consumed by the memory for every read/precharge operation?

(c) Assume that the supply of the cross-coupled pair in the cell is lowered to $V_{DD}/2$, while the bitline is still precharged to V_{DD}. True or false: the read margin becomes worse than in the original design.

(d) Assume the same operating conditions as in part (c). True or false: the write margin becomes worse than in the original design.