EECS151 : Introduction to Digital Design and ICs

Lecture 11 – CMOS

Bora Nikolić

RISC-I: Reduced Instruction Set Computing

On February 12, 2015, IEEE installed a plaque at UC Berkeley to commemorate the contribution of RISC-I. The plaque reads:

UC Berkeley students designed and built the first VLSI reduced instruction-set computer in 1981. The simplified instructions of RISC-I reduced the hardware for instruction decode and control, which enabled a flat 32-bit address space, a large set of registers, and pipelined execution. A good match to C programs and the Unix operating system, RISC-I influenced instruction sets widely used today, including those for game consoles, smartphones and tablets.

https://risc.berkeley.edu/risc-i/reunion/

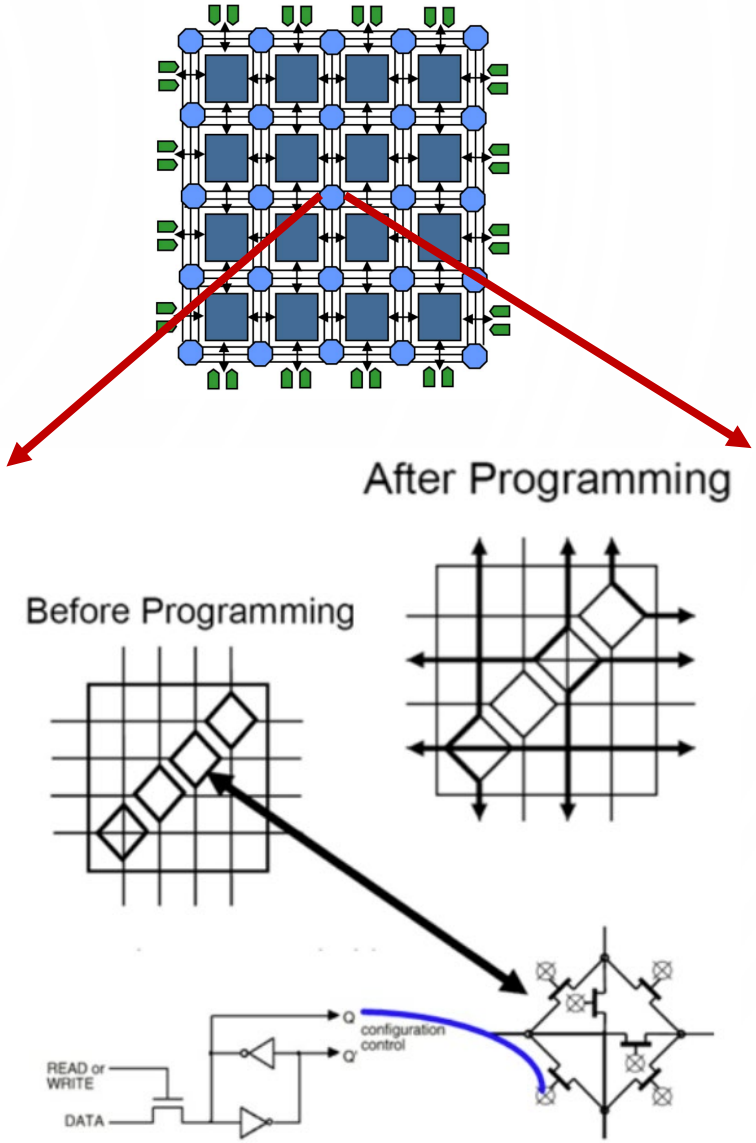
Review

- Pipelining increases throughput
  - Structural, control and data hazards exist
- FPGAs are widely used for hardware prototyping and accelerating key applications.
- Core FPGA building blocks:
  - Configurable Logic Blocks (CLBs)
    - Slices
      - Look-Up Tables
      - Flip-Flops
      - Carry chain
  - Configurable Interconnect

FPGA Interconnect

Configurable Interconnect

- Between rows and columns of CLBs are wiring channels.
- These are programable. Each wire can be connected in many ways.
- Switch Box:
  - Each interconnection has a transistor switch.
  - Each switch is controlled by 1-bit configuration register.



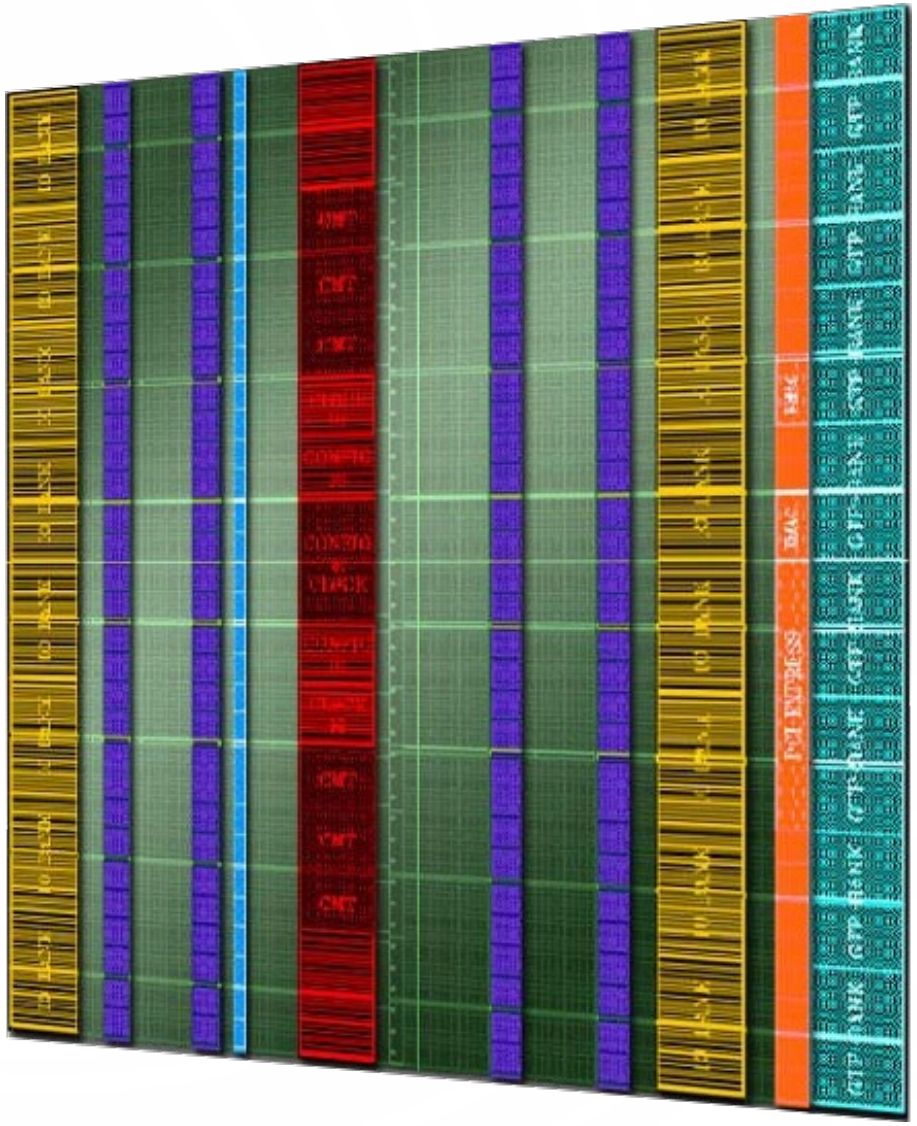
FPGA Features: BRAMs, DSP, AI

Diverse Resources on FPGA

Colors represent different types of resources:

- Logic
- Block RAM
- DSPs
- Clocking
- I/O
- Serial I/O + PCI

A routing fabric runs throughout the chip to wire everything together.



Virtex-5 Die Photo
[Xilinx]

Block RAM

- Block Random Access Memory
- Used for storing large amounts of data:
  - 18Kb or 36Kb
  - Configurable bitwidth
  - 2 read and write ports
- More recently
  - UltraRAM in UltraScale+ devices

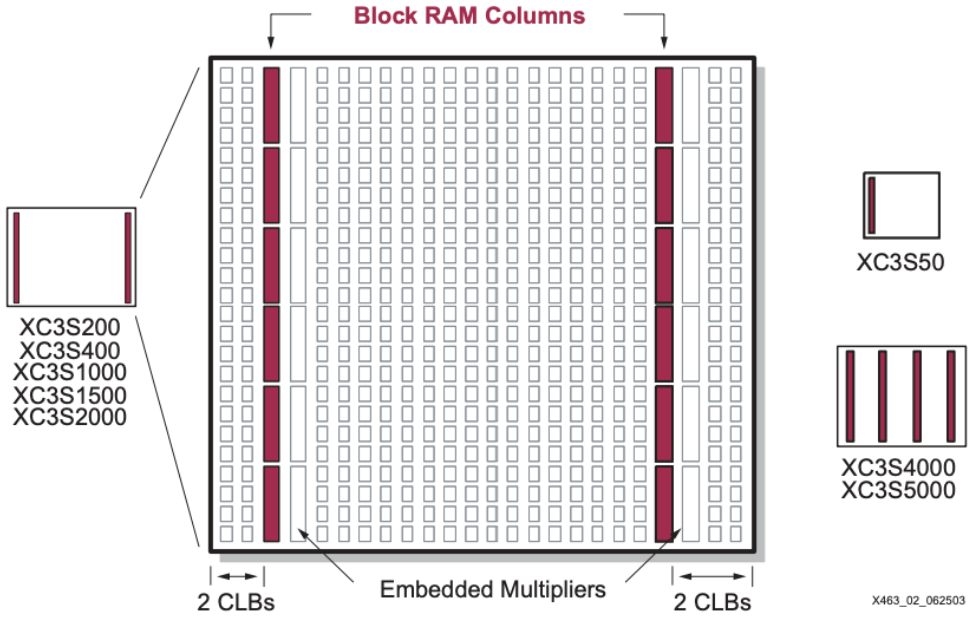
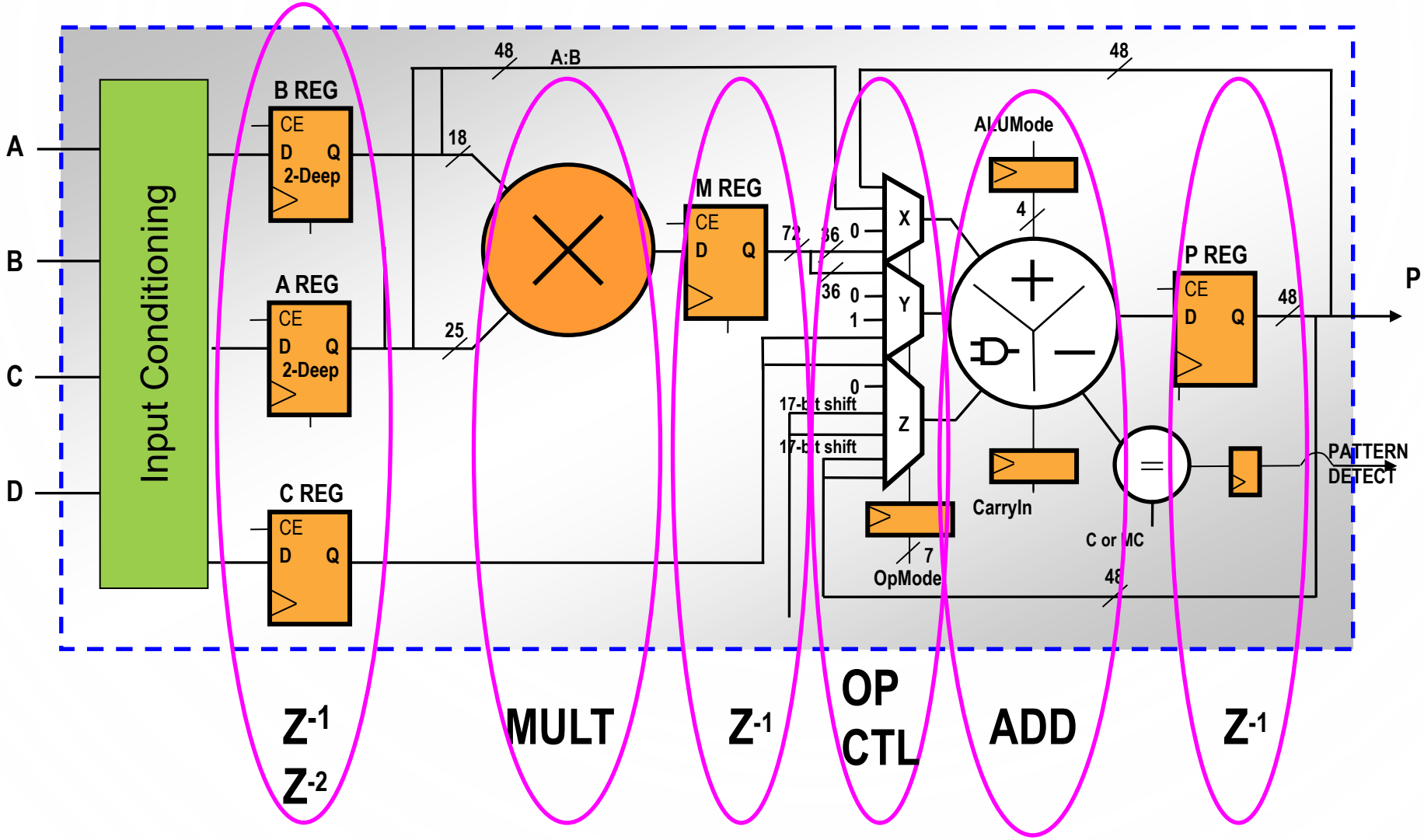


Figure 2: **Block RAMs Arranged in Columns with Detailed Floorplan of XC3S200**

Xilinx Datasheet

DSP Slice

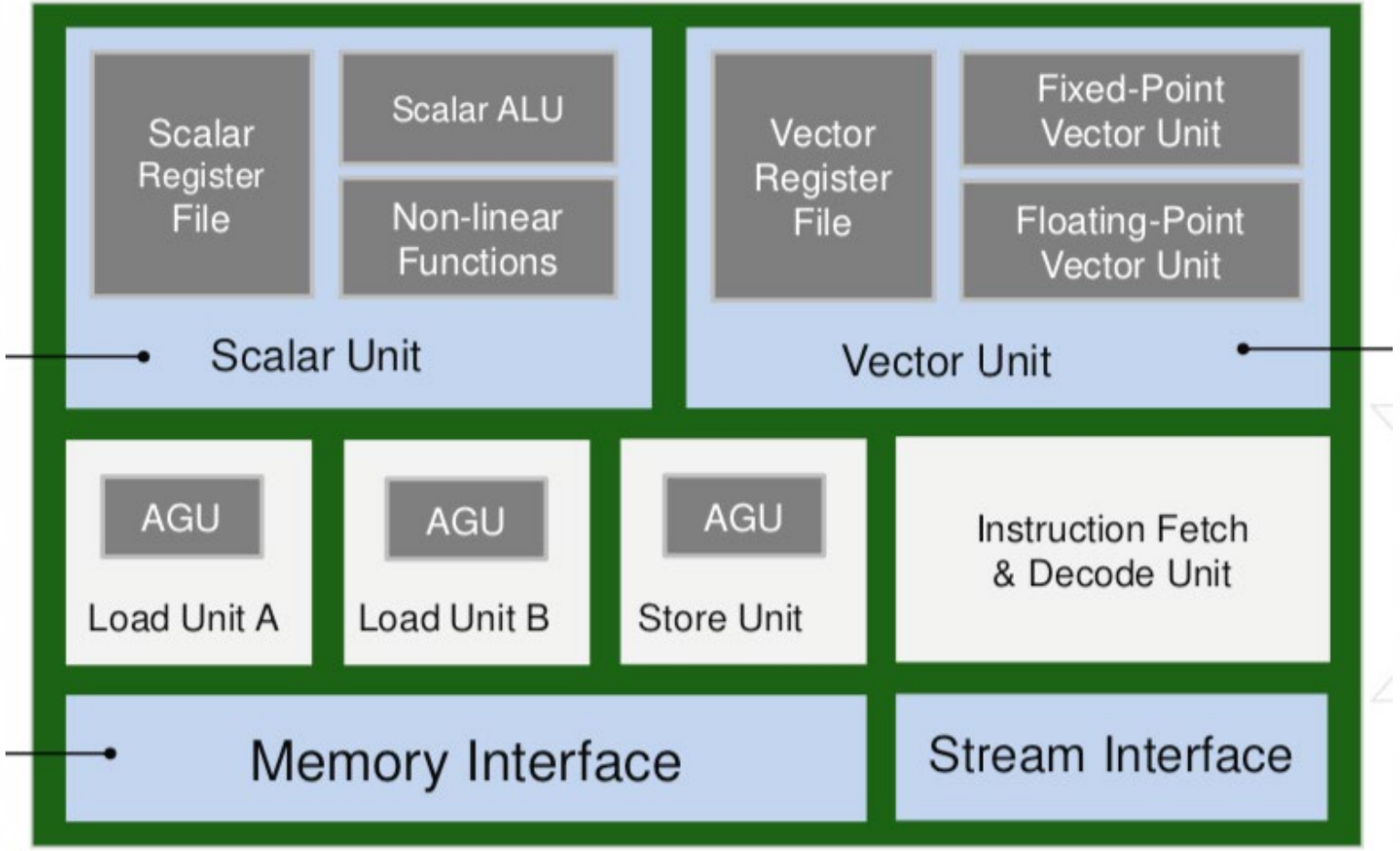


Efficient implementation of multiply, add, bit-wise logical.

Xilinx Resource

AI Engine

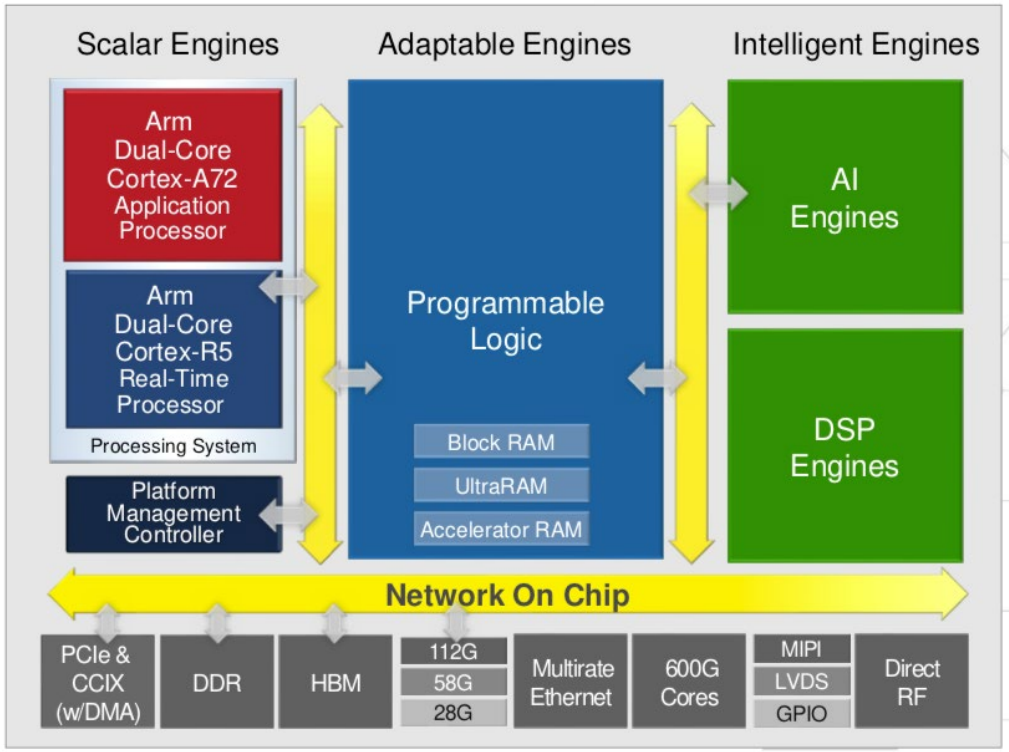
- Versal AI Core

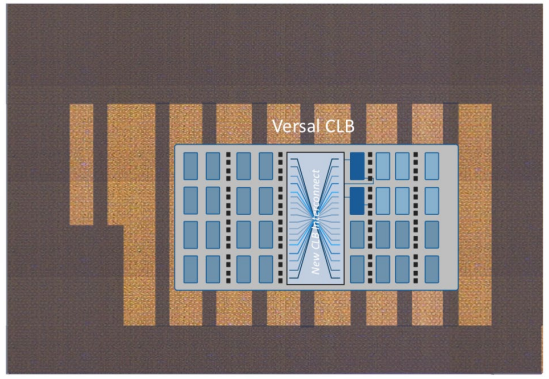


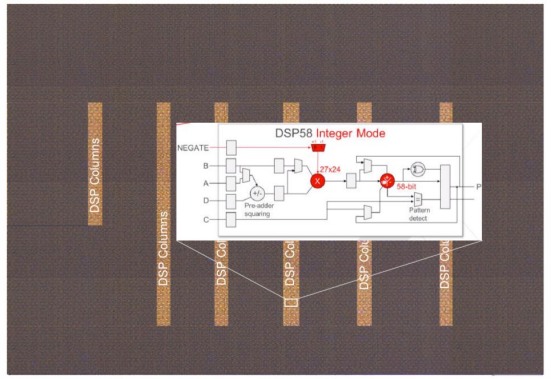
Xilinx HotChips'2019

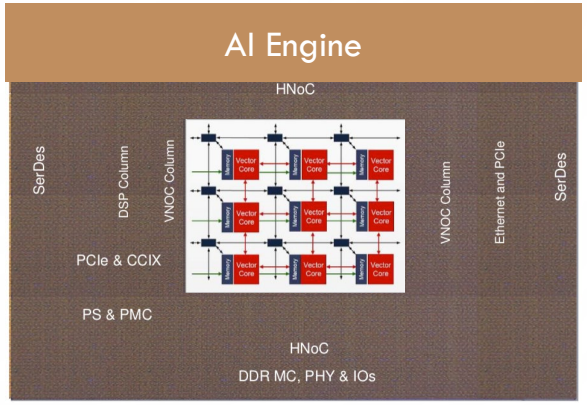
State-of-the-art Xilinx FPGA Platform

- Versal (ACAP: Adaptive Compute Acceleration Platform)







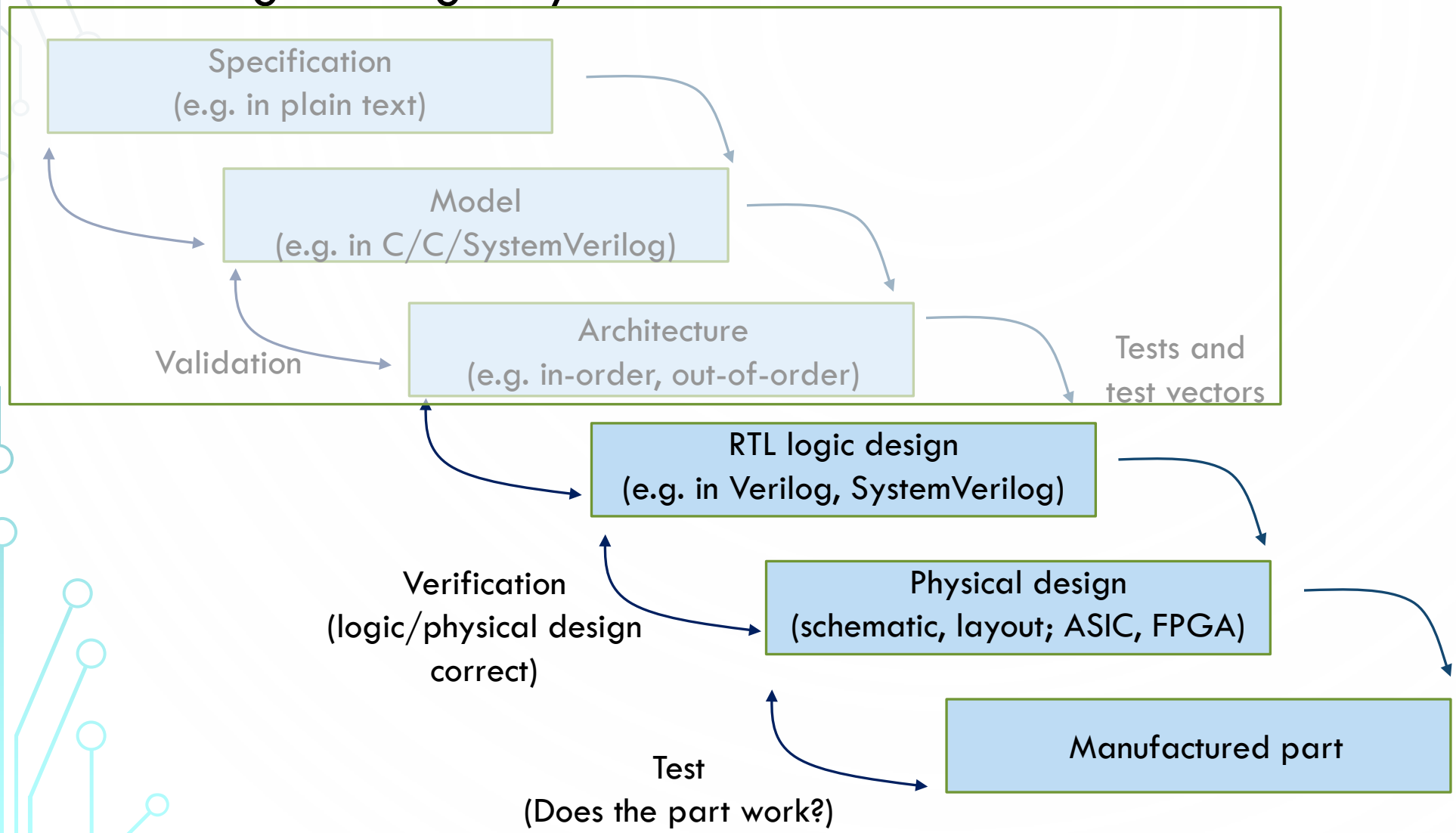


Xilinx HotChips'2019

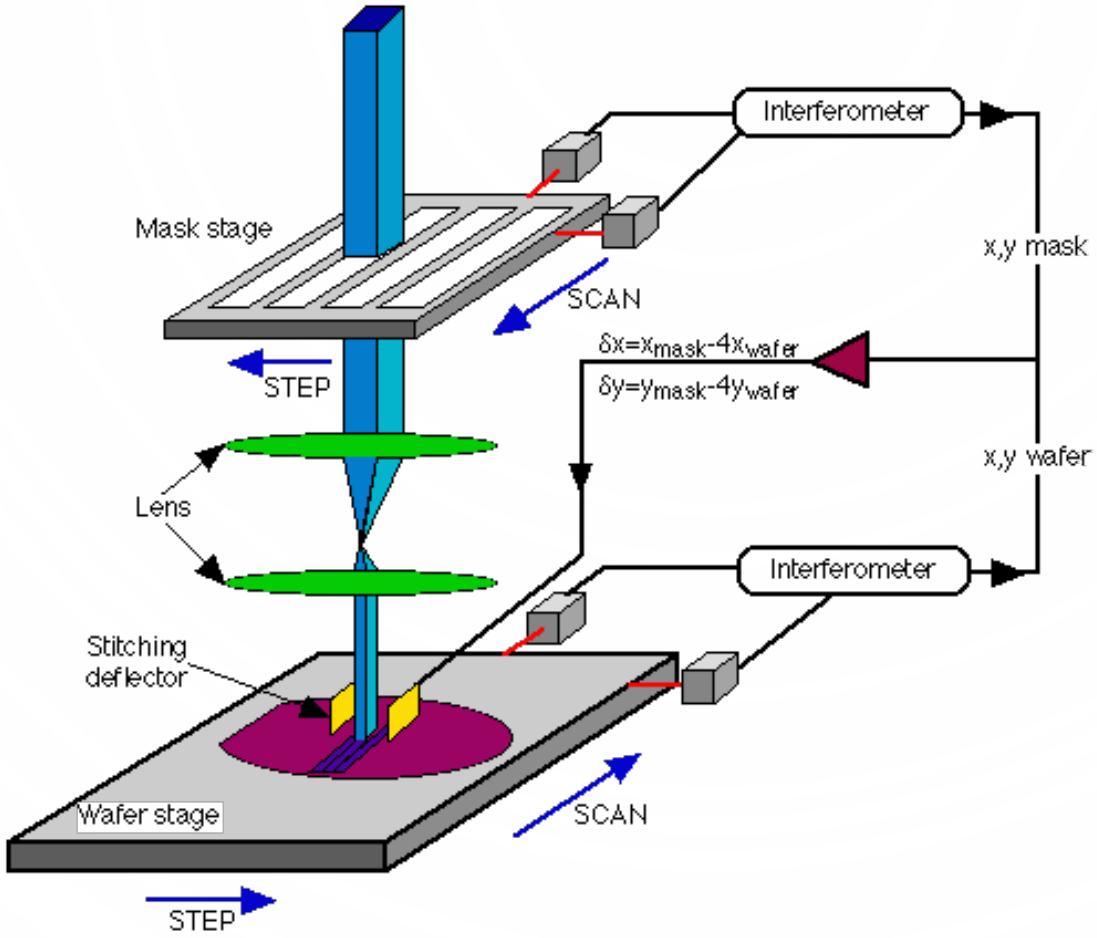
CMOS Process

Design Process

- Design through layers of abstractions

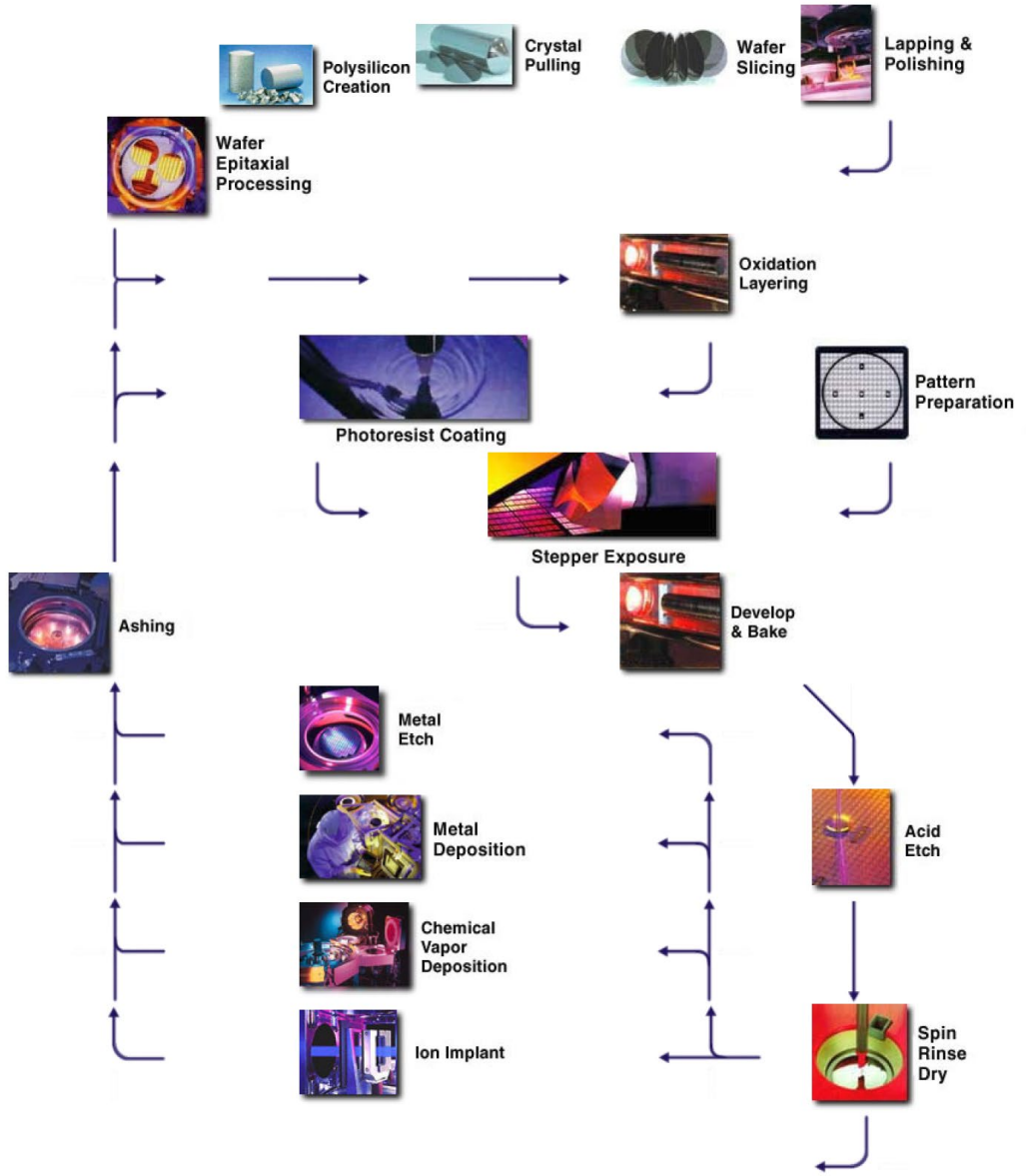


Step-and-Scan Lithography



Semiconductor Manufacturing

- Repetitive steps (40-70 masks):
  - Passivation
  - Photoresist coating
  - Patterning (stepper)
  - Develop
  - Etch
  - Process step
    - Etching
    - Deposition
    - Implant
  - Remove resist
  - Repeat
- Zoom into a chip:

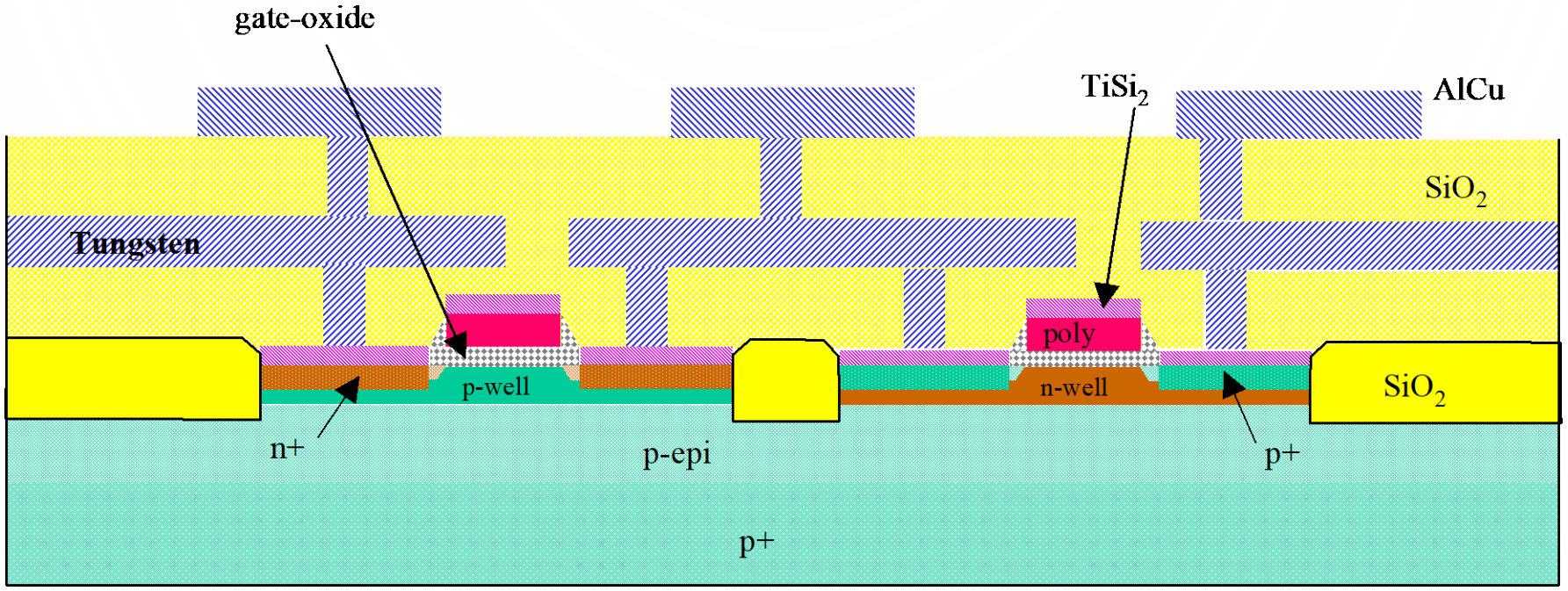


https://youtu.be/Fxv3JoS1uY8

http://laplace.ucv.cl/Charlas/Semiconductors/Chip/semiconductors.html

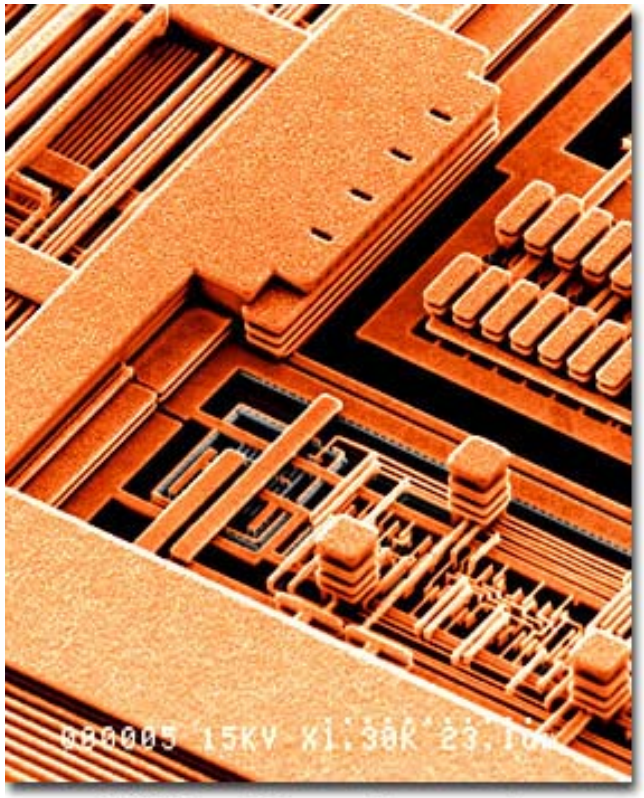
CMOS Process

- Post ~250nm CMOS
- Shallow-trench isolation, dual/triple-well process



Metal Stack

- Interconnect is predominantly copper

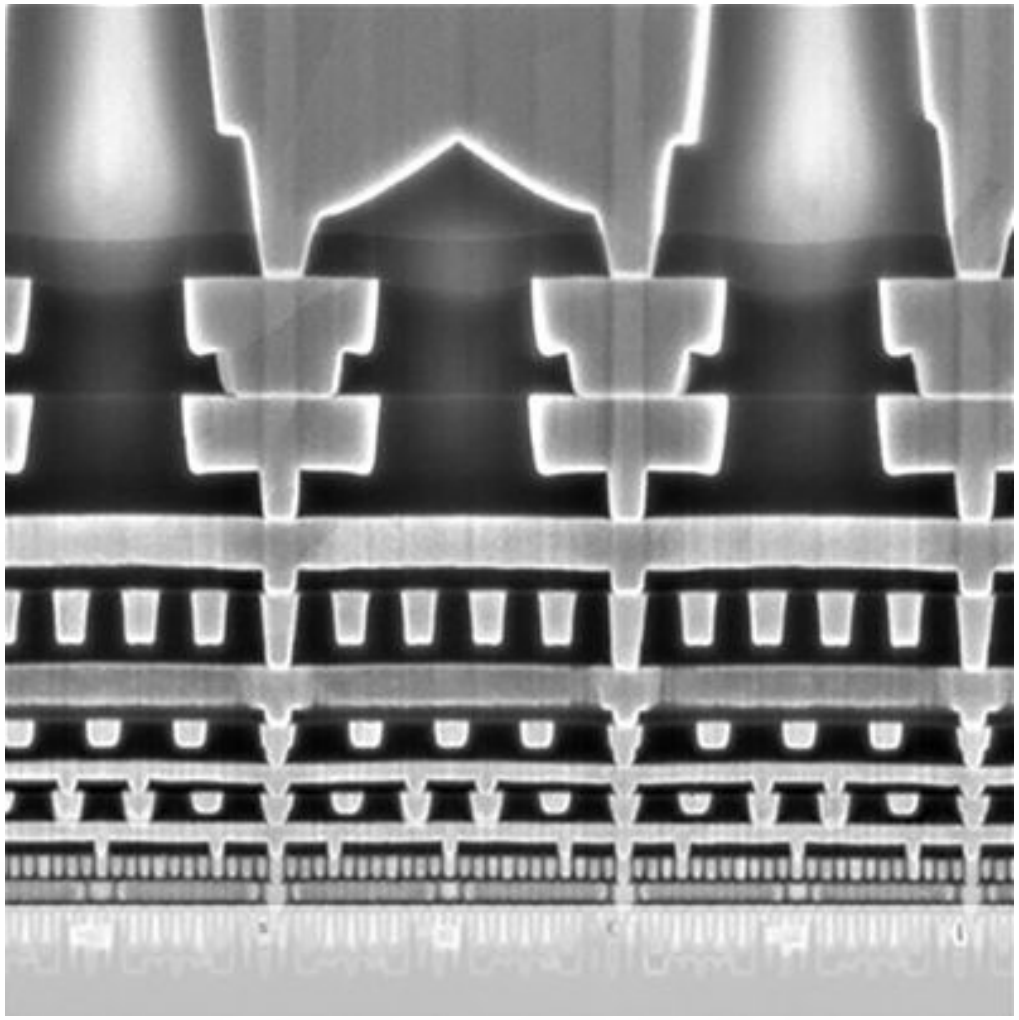


SEM view of Copper Interconnect
(IBM Microelectronics)

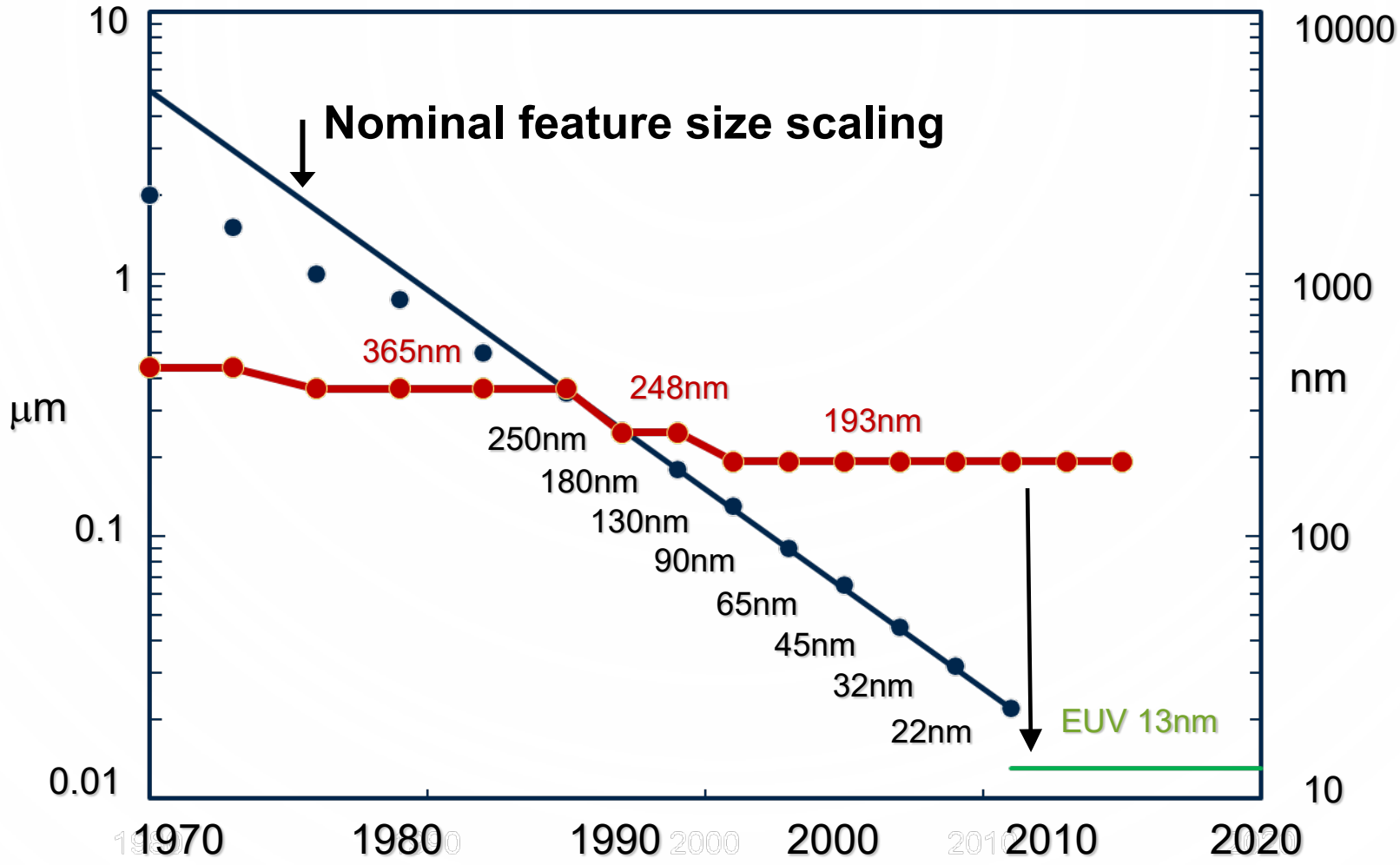
SEM view of Copper Interconnect
(IBM Microelectronics)

Metal Stack in Modern Processes

- Metal stack
  - Bottom layers have pitch that matches transistors
  - Intermediate are 2-4x
  - Top layers are wide and thick: Power distribution, clock



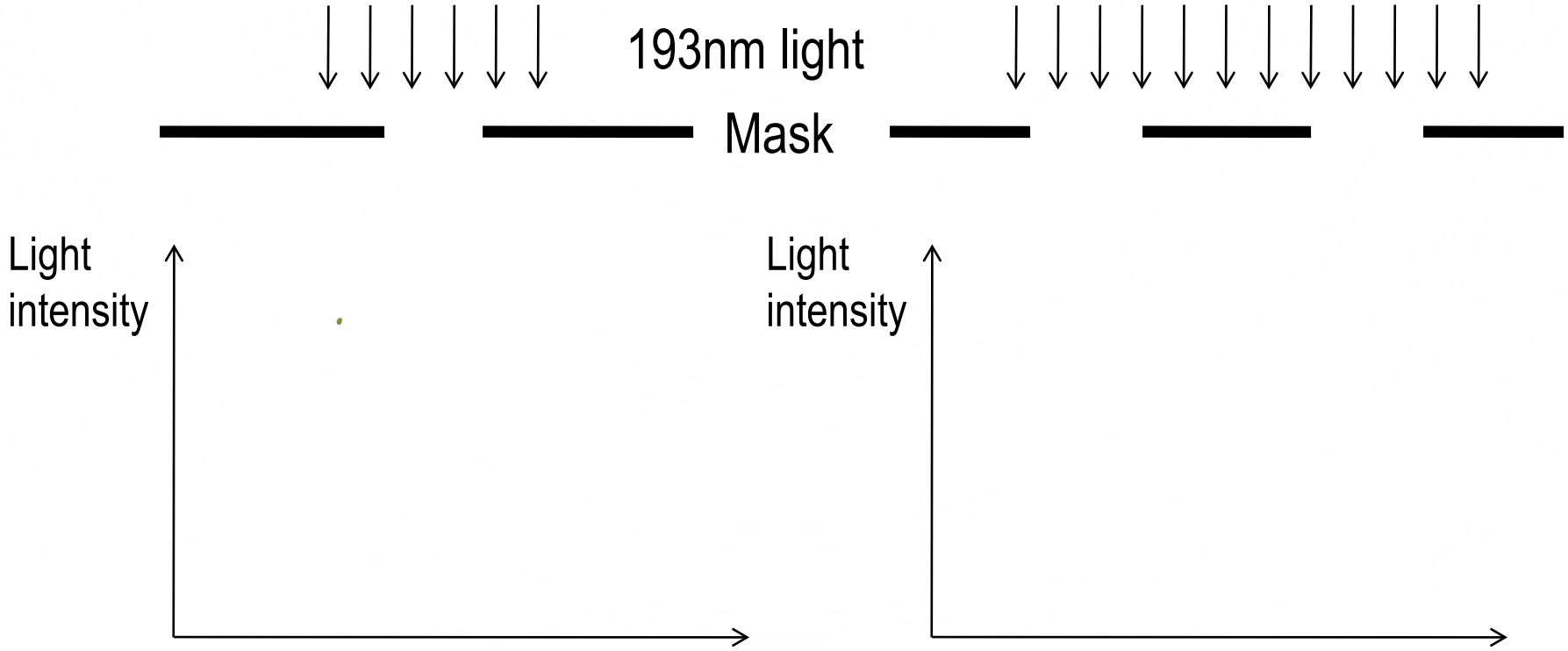
Lithography Scaling



EUV – Expected in volume this year

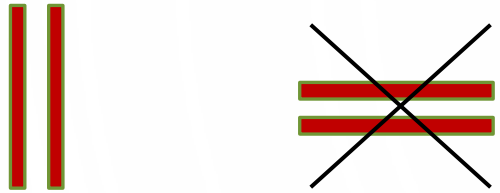
Sub-Wavelength Lithography

- Light projected through a gap

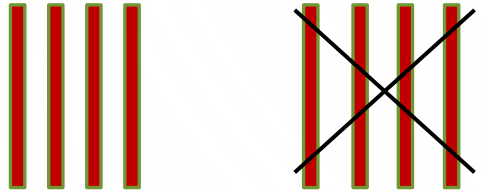


Lithography Implications

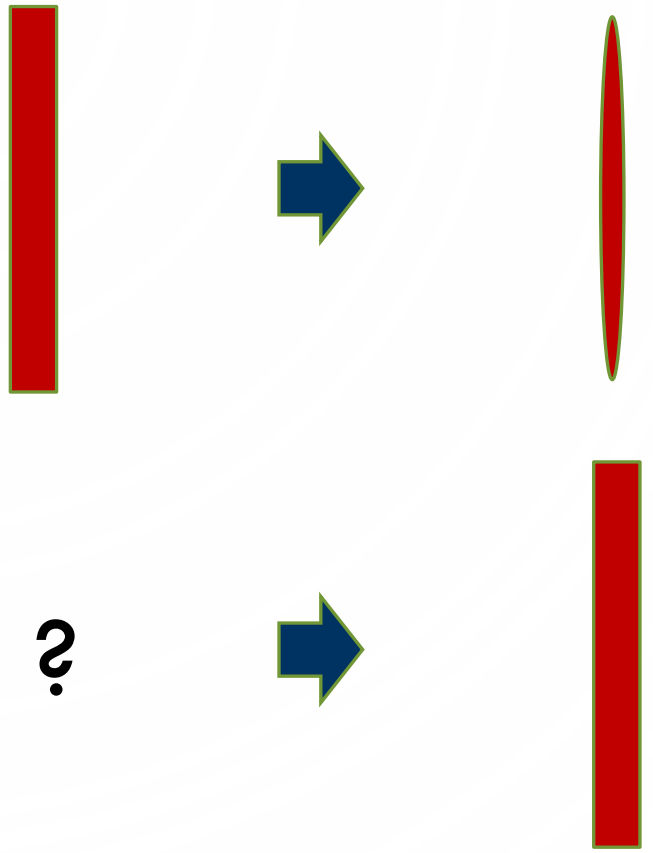
- Forbidden directions



- Forbidden pitches



- Optical proximity correction (OPC)



We Would Just Like a Square Contact…

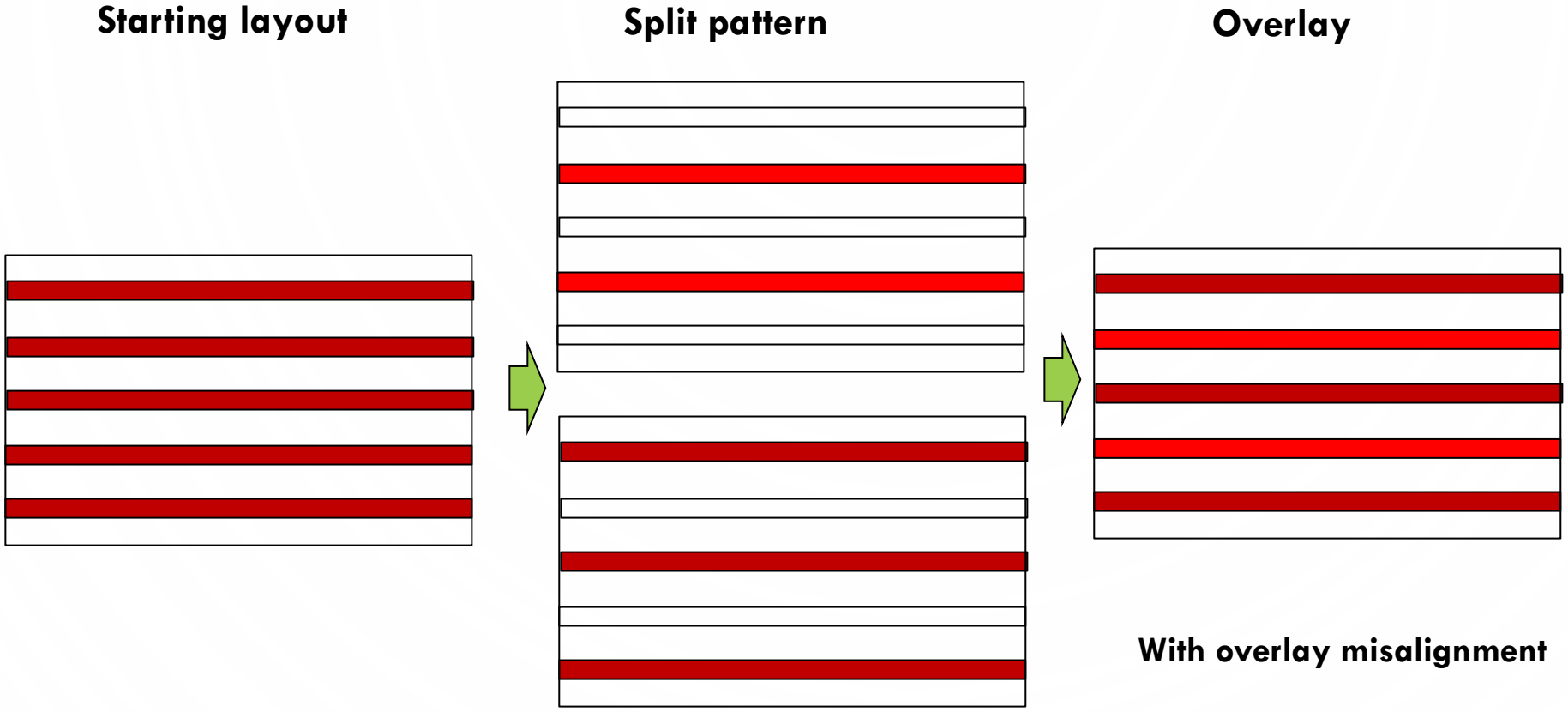
- OPC vs. ILT

Optical Proximity Correction		Inverse Lithography Technology	
45 nm node	28 nm node	14 nm node	7 nm node
without OPC	normal OPC	normal ILT	ideal ILT

https://semiengineering.com/what-happened-to-inverse-lithography/

Multiple Patterning

- Double patterning (pitch-split double exposure)



- "Layout coloring"
- 7nm process is quadruple patterned (w/o EUV)

Lithography and Processing Takeaways

- 193nm lithography impacts many of the design rules in modern processes:
  - Preferred and forbidden directions
  - Forbidden pitches
  - Multiple patterning
- EUV relaxes many of the restrictions in sub 5nm processes

Administrivia

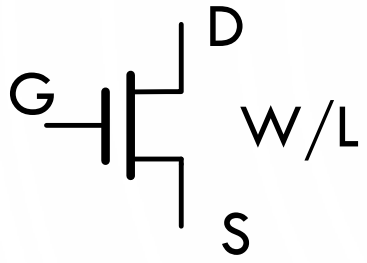
- Semiconductor Workforce Fellowships in the area of SoC design
  - 8 undergraduate scholarships (4k each), applications due October 15
- Homework 4 is due today
  - No new homework this week
  - Homework 5 will be posted later this week, due next week
- No lab this week
  - Lab 6 (last) after the midterm
- Midterm 1on October 7, 7-8:30pm
  - You will be assigned a classroom
  - One double-sided page of notes allowed
  - Material includes FPGAs

MOS Transistors

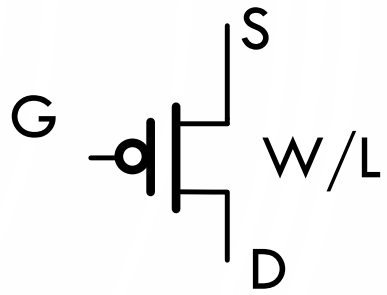
MOS Transistors

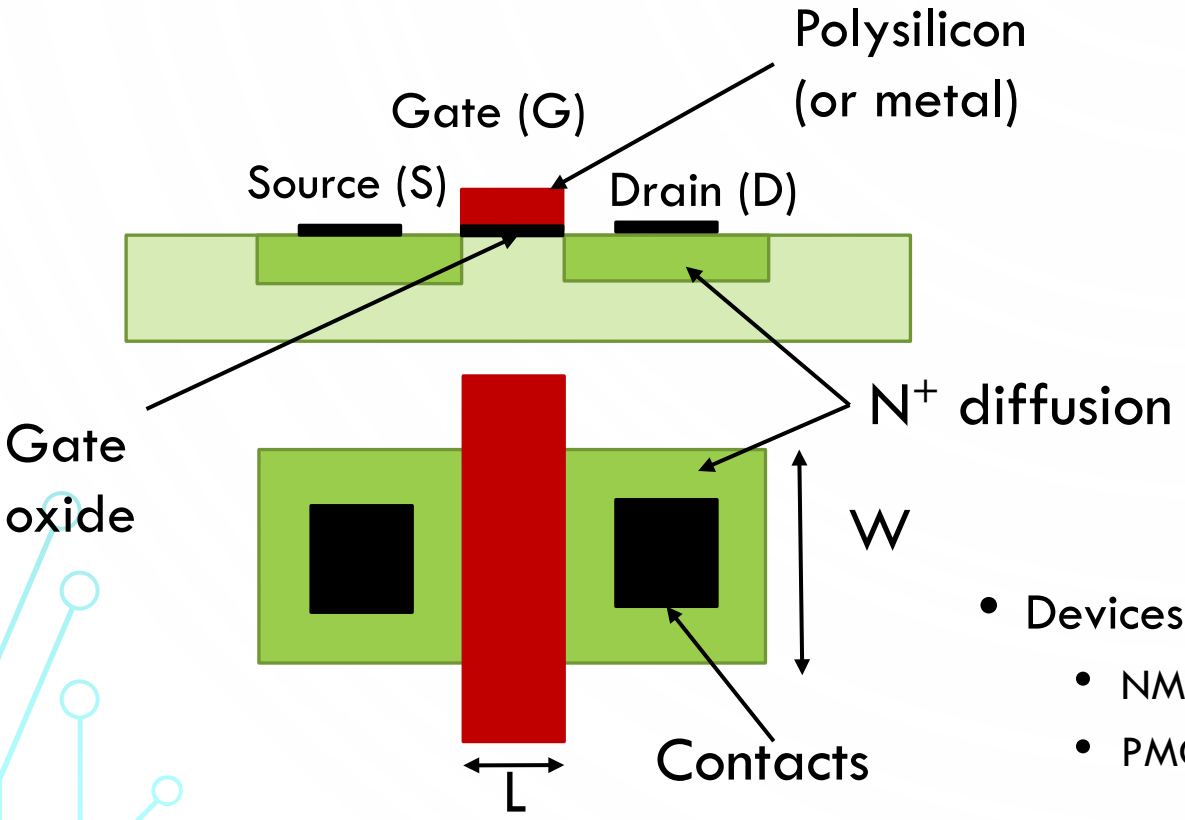
- Symbol

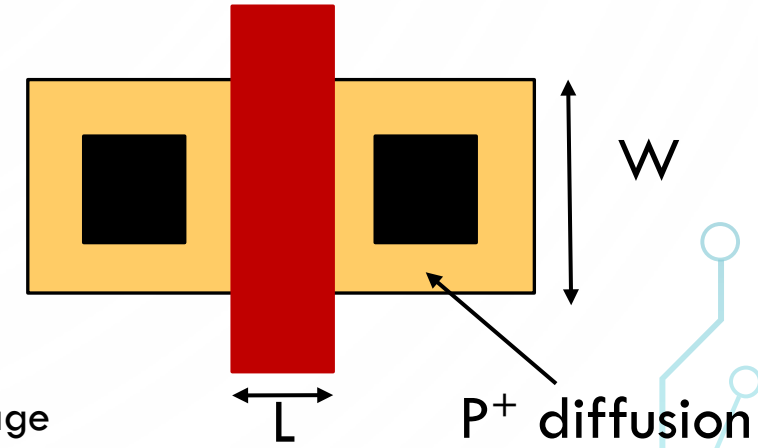
N-type NMOS



P-type PMOS





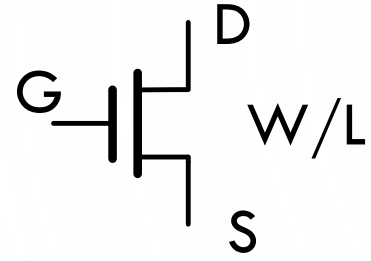


- Devices are symmetrical
  - NMOS: Drain is at higher voltage
  - PMOS: Source is at higher voltage

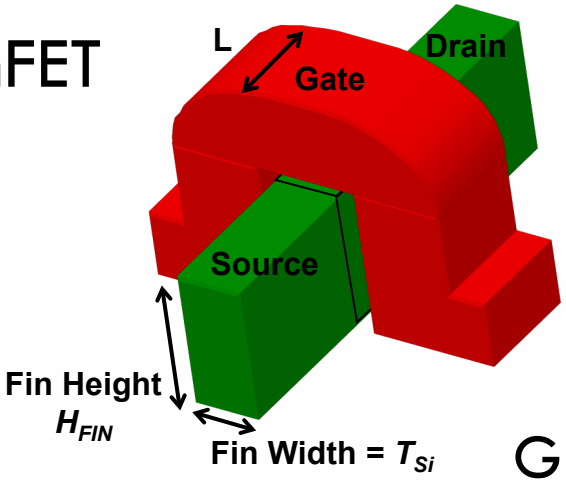
Different Kinds of MOS Transistors

- Planar bulk CMOS

N-type NMOS

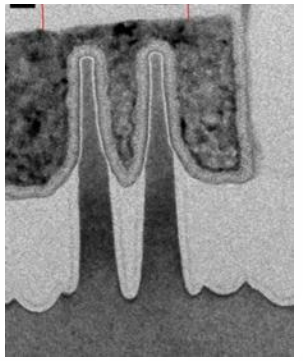


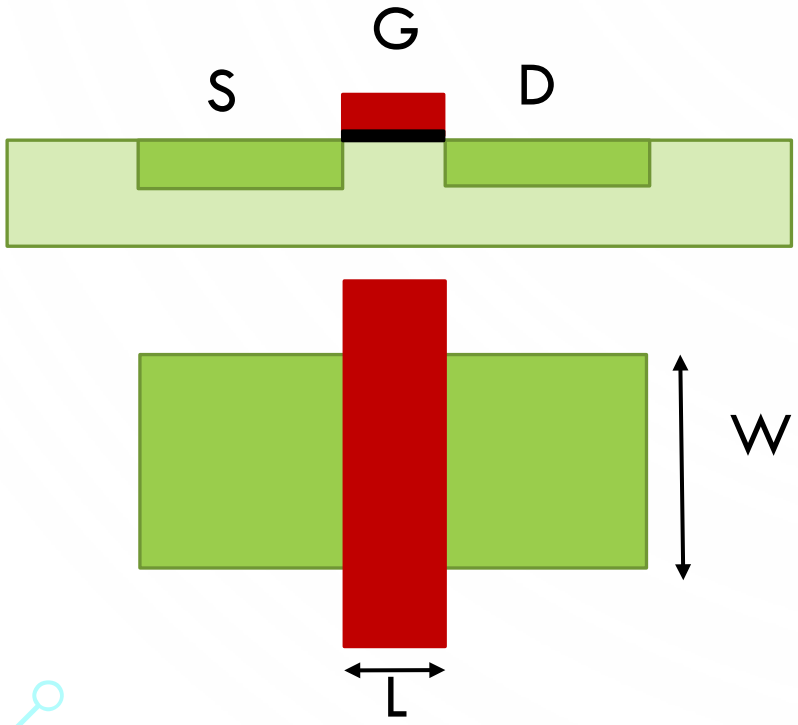
- FinFET

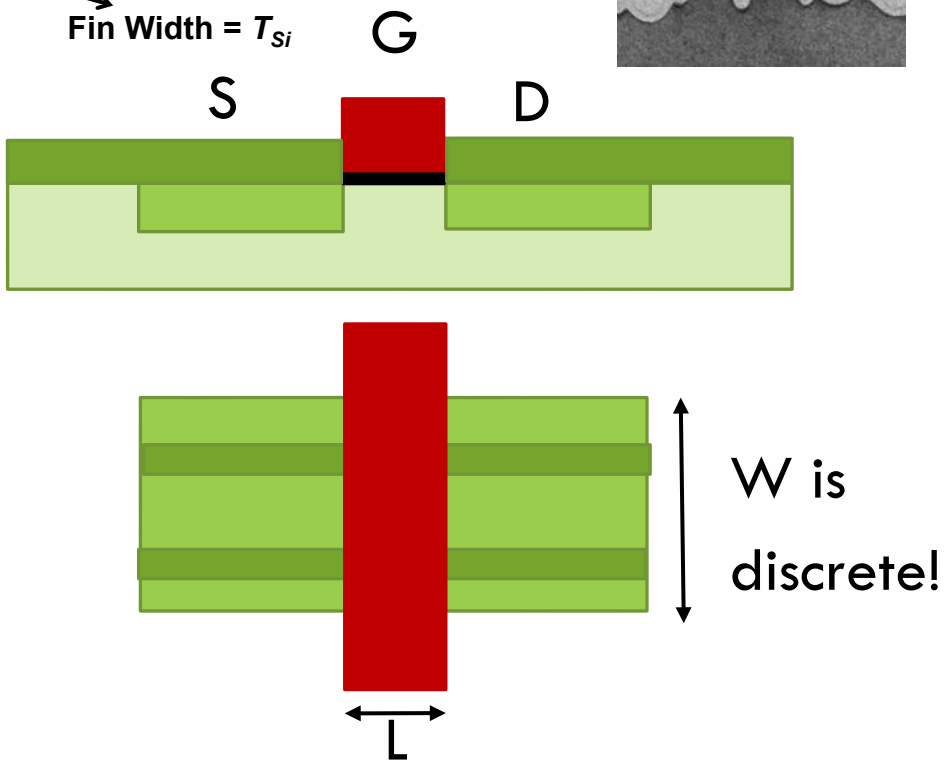


Intel 10nm

IEDM 2017



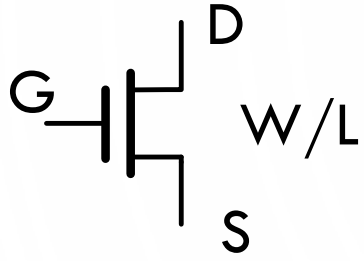




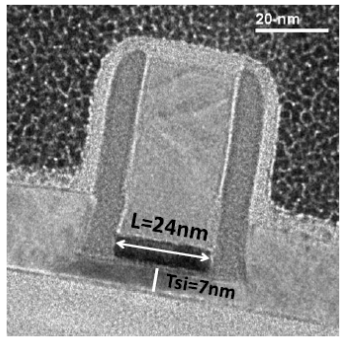
Different Kinds of MOS Transistors

- Planar bulk CMOS

N-type NMOS

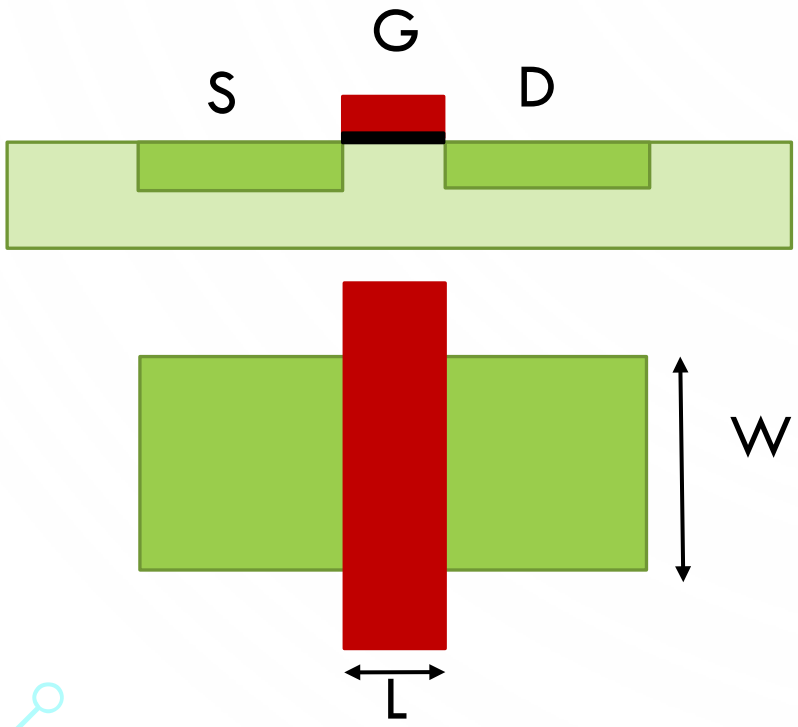


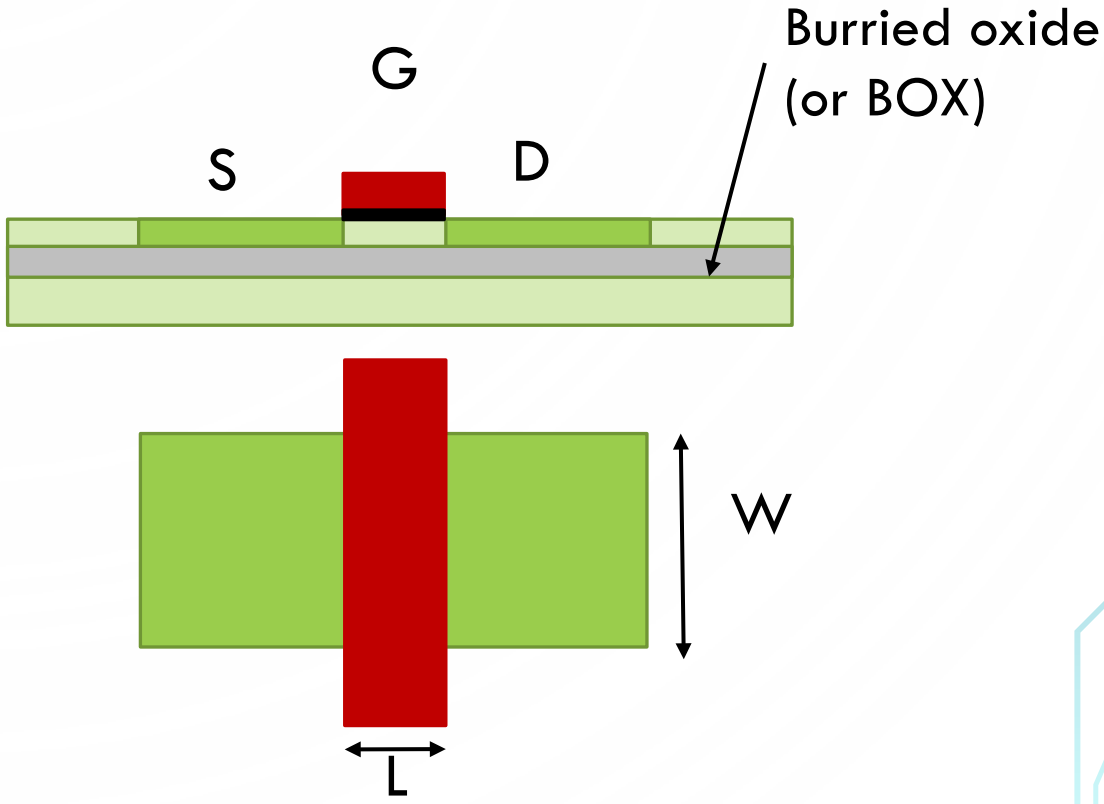
- Fully-depleted SOI



ST 28nm

VLSI 2012



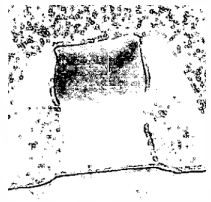


Transistors are Changing

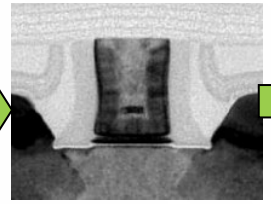
- From bulk to finFET and FDSOI

65/55 nm | 45/40 nm | 32/28nm | 22/20nm | 16/14nm | 10nm | 7nm

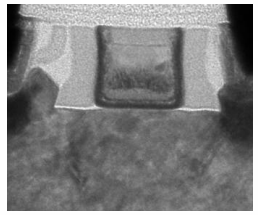
Bulk



SiO_2/SiN Strain



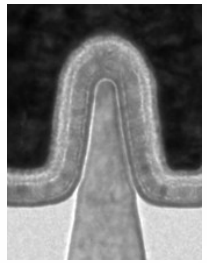
Intel, IEDM'07 HK/MG Strain

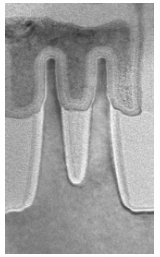


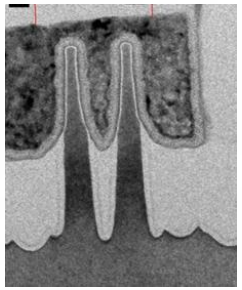
Intel, IEDM'09

TSMC, Samsung

FinFET





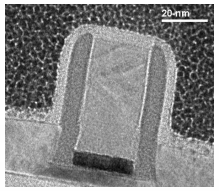


Intel, IEDM'12

Intel, VLSI'14

Intel, IEDM'17

FDSOI



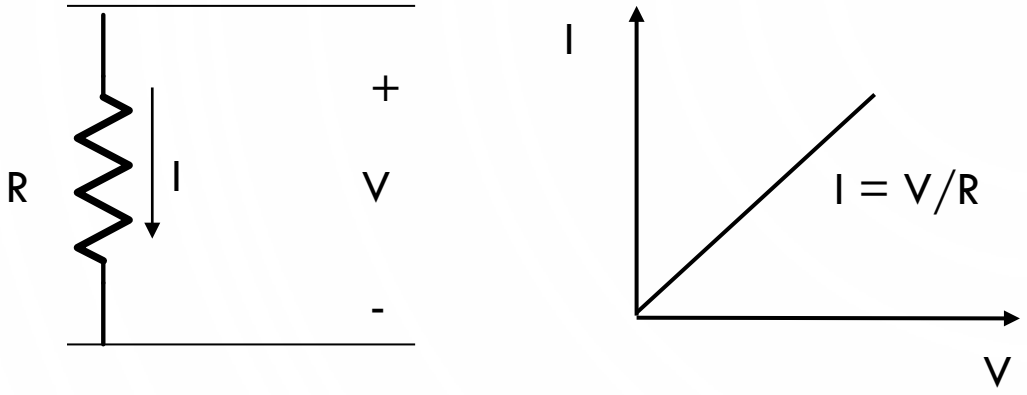
ST, VLSI'12

Transistor Dimensions are Quantized

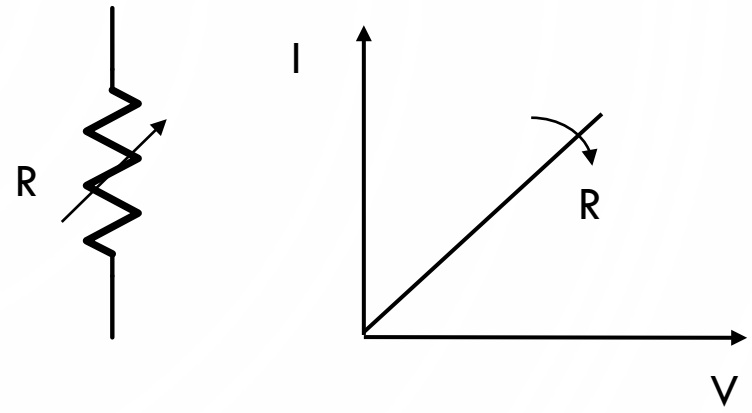
- FinFET widths are discrete ($W = kW_{unit}$)
  - k is an integer
- Lengths are quantized because of lithography
  - Also are quantized lower metal layers, contacts…

Ohm's Law

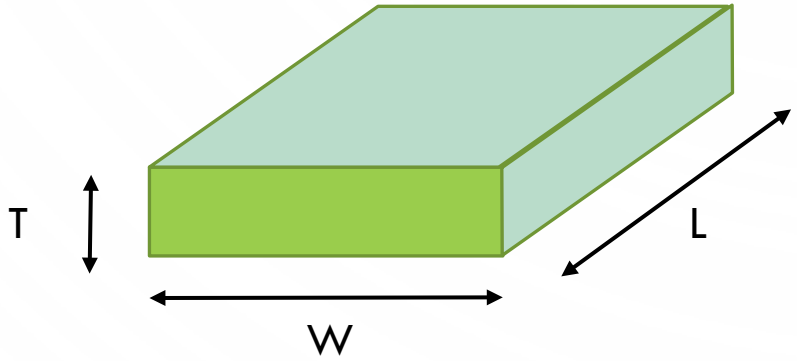
- Resistors



- Variable resistors



- Physical resistors

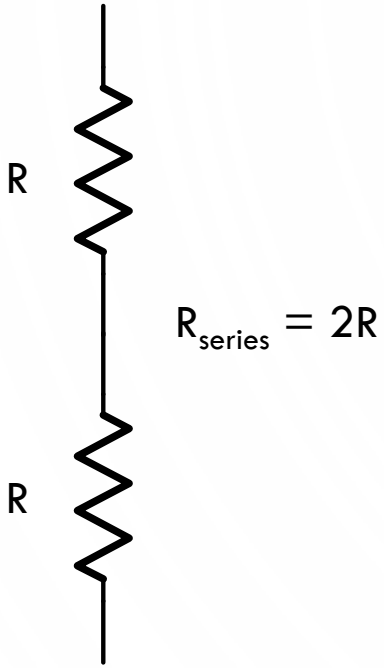


$$R = \rho \frac{L}{TW}$$

- In a planar process, designer controls W and L

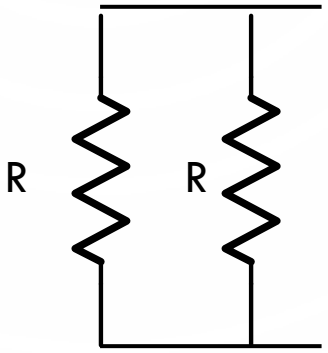
Series and Parallel

- With two identical resistors, R



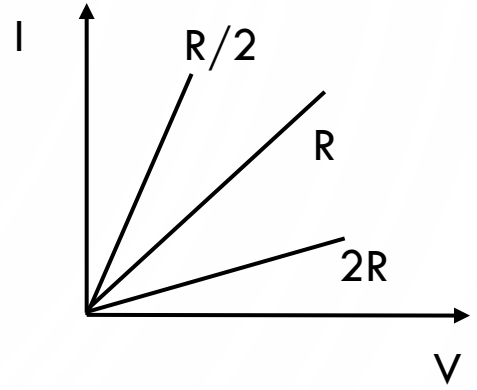
$R_{series} = 2R$

Equivalent to doubling length

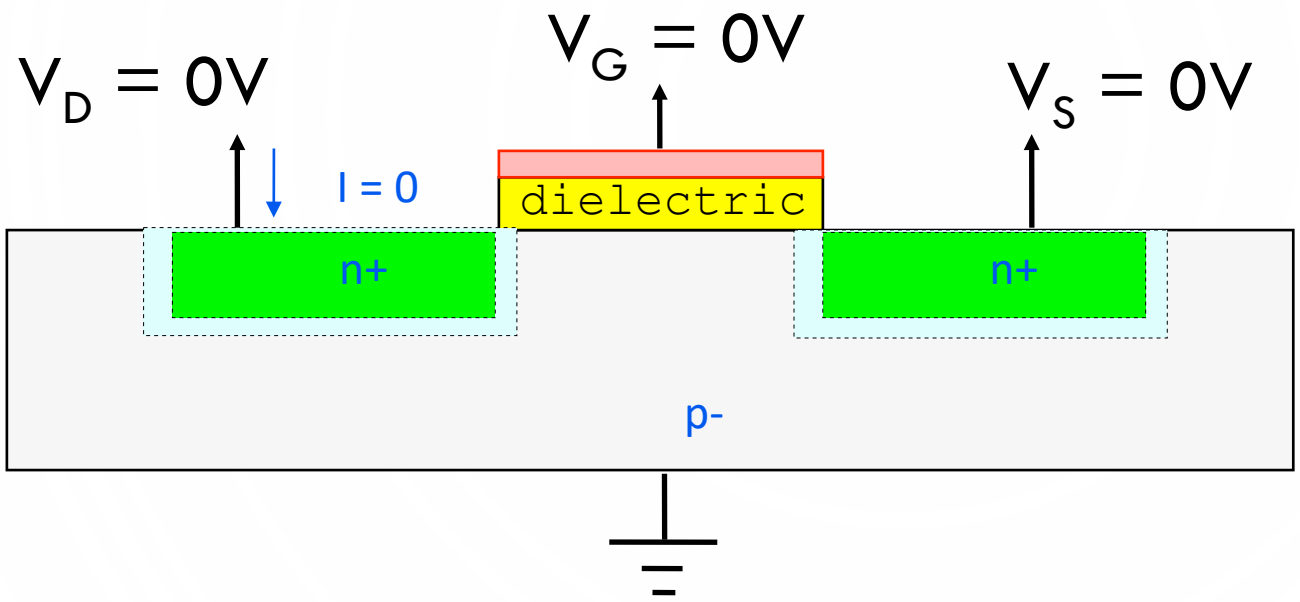


$R_{parallel} = R/2$

Equivalent to doubling width

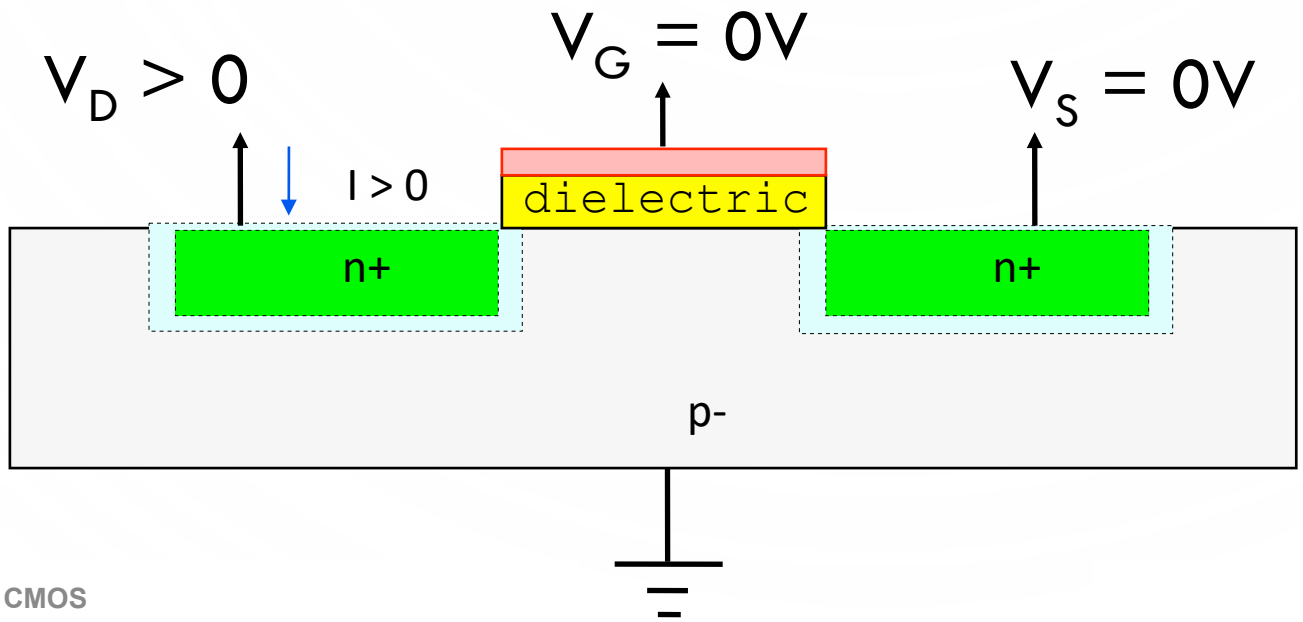


An n-Channel MOS Transistor



Polysilicon gate, dielectric, and substrate form a capacitor.

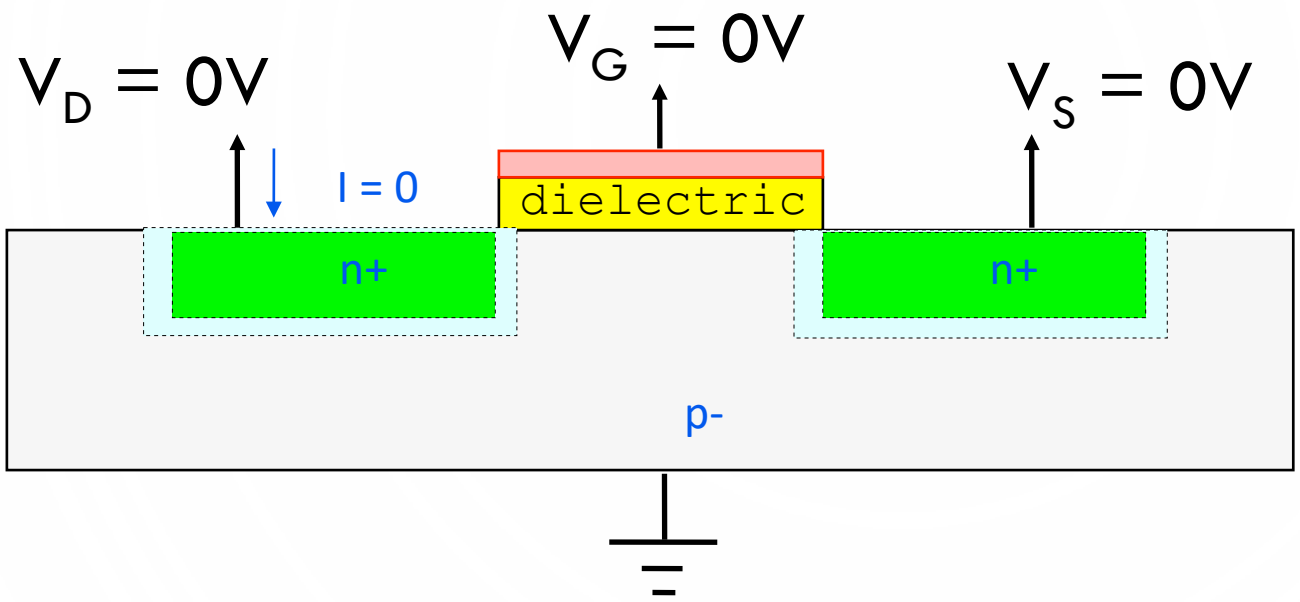
When $V_{GS} < V_{Th}$ transistor is off



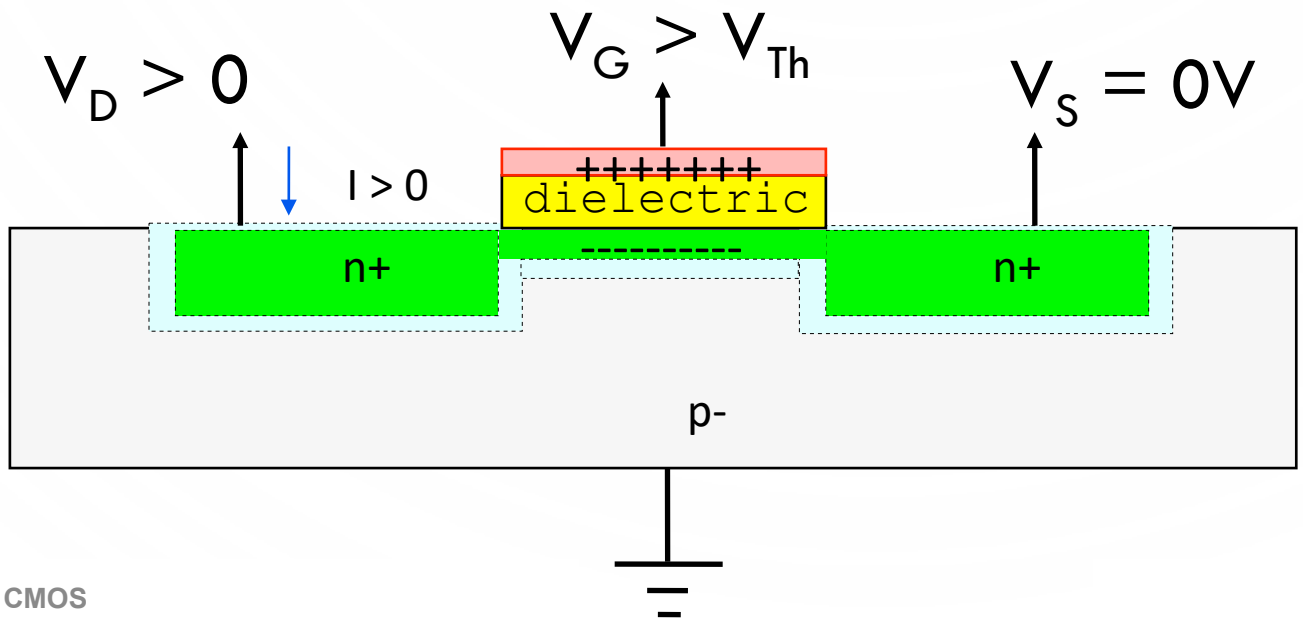
$V_{DS} > 0$, transistor leaks

$I_{DS} \sim$ nA

An n-Channel MOS Transistor



When $V_{GS} < V_{Th}$ transistor is off

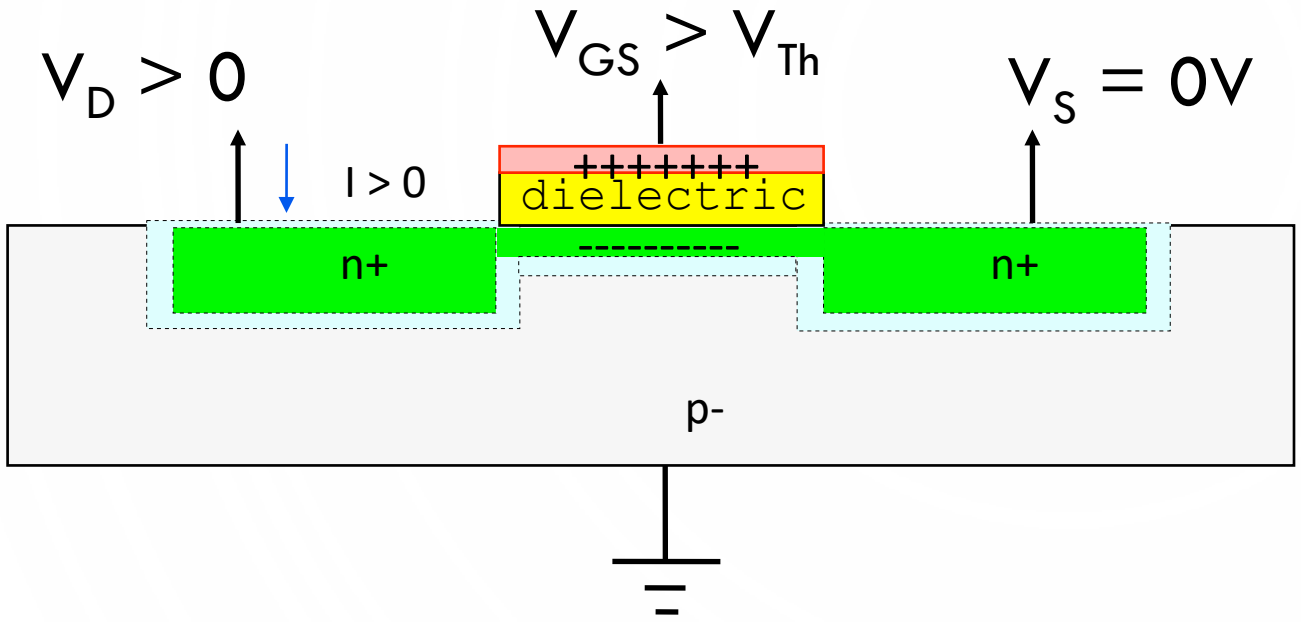


$V_G > V_{Th}$, small region near the surface turns from p-type to n-type.

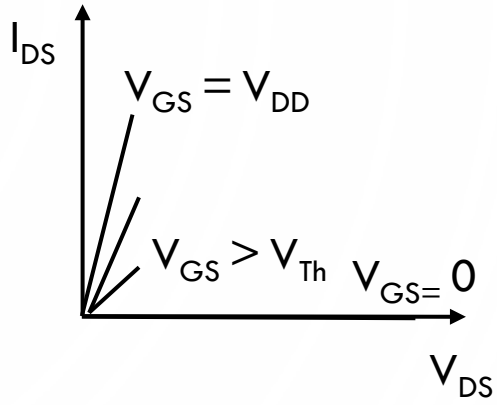
nFet is on.

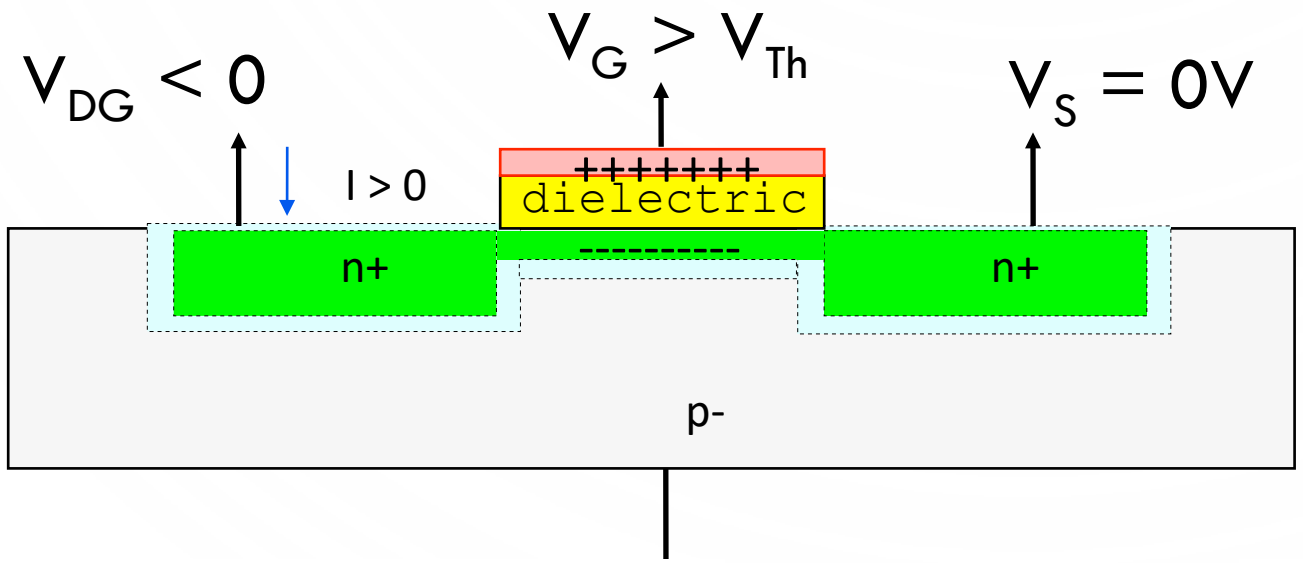
Current is proportional to V_{DS}

An n-Channel MOS Transistor



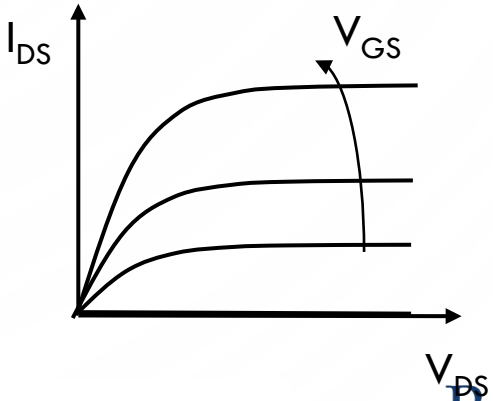
V_{DS} and V_{GS} change I_{DS}





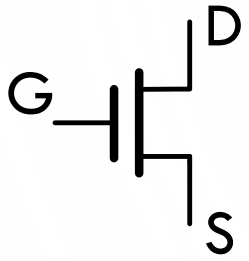
$V_{GD} < V_{Th}$ transistor saturates

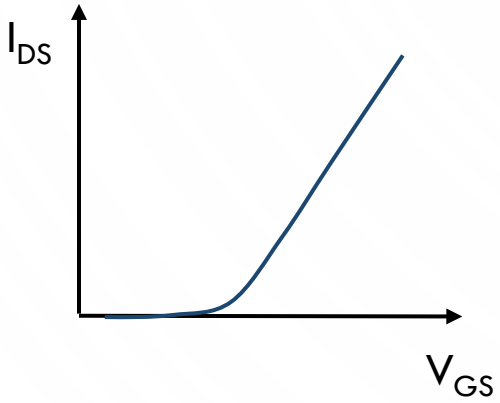
($V_{DS} > V_{GS} - V_{Th}$)



MOS Transistors

- NMOS Transistor I-V characteristics

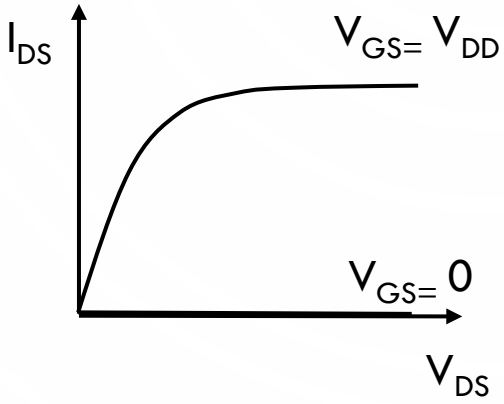


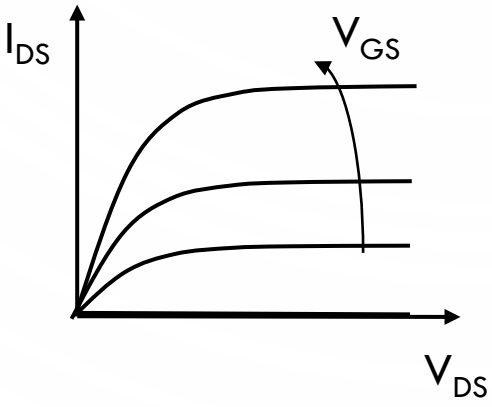


Nearly linear

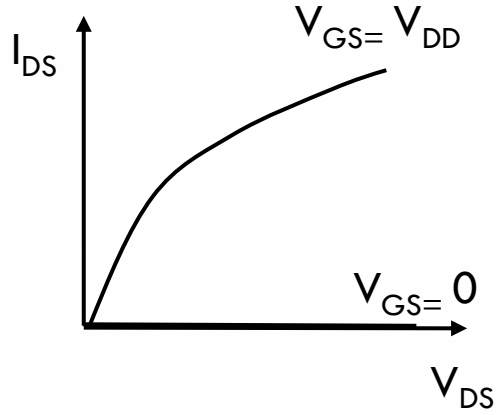
$I_{DS} \sim K(V_{GS}-V_{Th})$

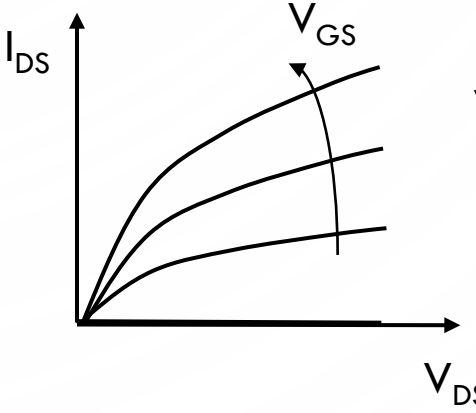
Old transistor





~7nm transistor

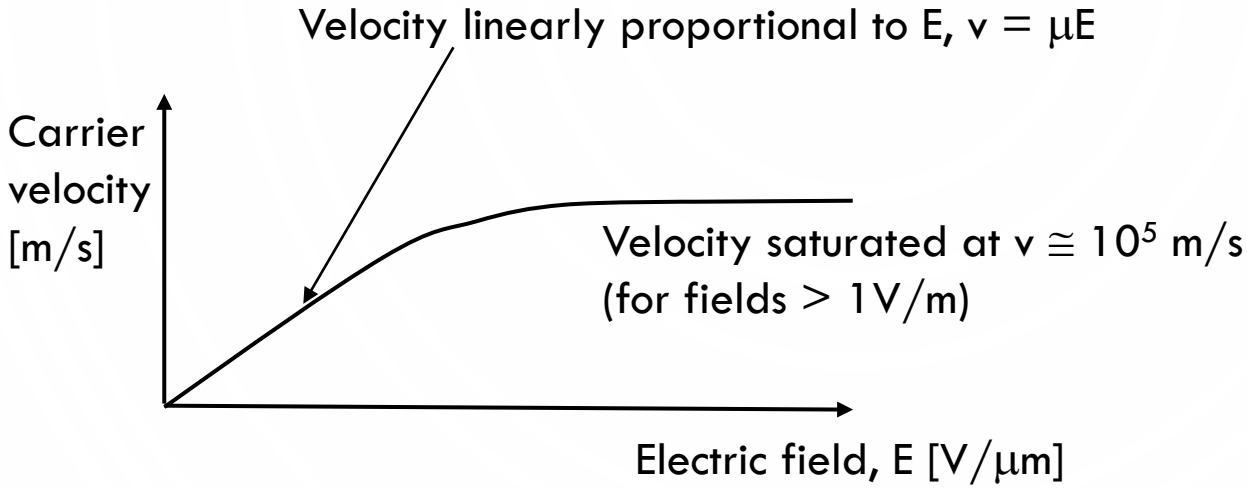




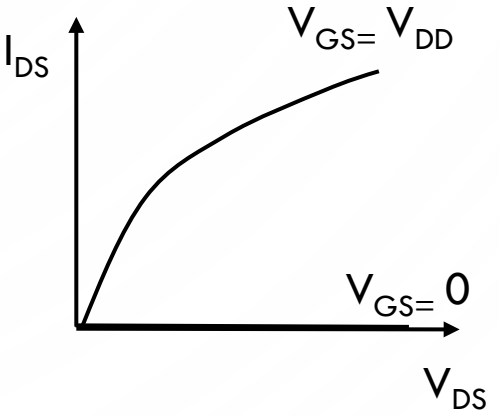
Variable resistor!

Velocity Saturation

- Carrier velocity in the channel saturates



  - All submicron transistors are velocity saturated
  - Other effects (drain-induced barrier lowering) cause I_{DS} to increase in saturation



Summary

- Core FPGA building blocks:
  - Configurable Logic Blocks (CLBs)
  - Configurable Interconnect
    - Switch boxes
- Modern FPGA Designs:
  - BRAMs, DSPs, and AI Engines
- CMOS process is used for producing chips
  - Planar bulk process used up to 28nm node
  - finFET used below the 22nm node
    - Also FDSOI, but we didn't talk about it