SOLUTION *Your Name (first last)* *← Name of person on left (or aisle)*	**UC Berkeley EECS151** **EECS251A** **Fall 2021 Midterm 2** Room _____ Lab *TA name*	*SID* *Name of person on right (or aisle) →*

Fill in your student ID at the top of every page.

Question	1	2	3	4	5	6	Total
Minutes	16	10	12	12	12	13	**75**
Max Points (151)	12	8	12	12	6	11	**61**
Max Points (251A)	16	8	12	12	12	11	**71**
Points							

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1) *CMOS logic* (16 points, 16 minutes)

A slightly unusual logic gate is shown in Figure 1.

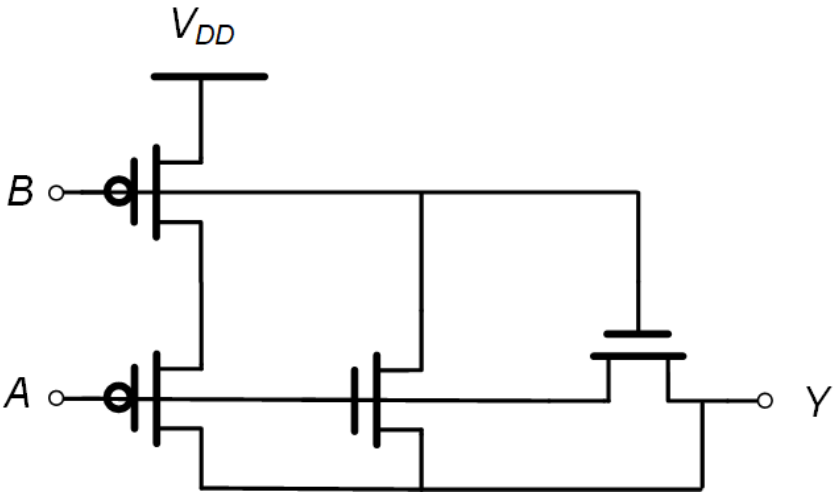
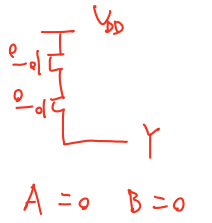
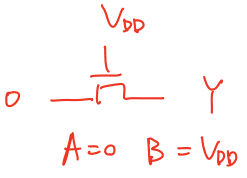


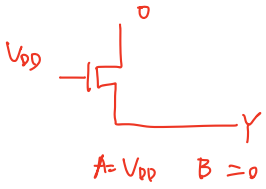
Figure 1.

a) (4 pts) For all the possible combinations of inputs *A* and *B* find the output voltage levels. Supply voltage is V_{DD} and transistors have a threshold of $|V_{Th}|$.

A	*B*	*Y*
0	0	V_{DD}
0	V_{DD}	0
V_{DD}	0	0
V_{DD}	V_{DD}	$V_{DD} - \|V_{Th}\|$

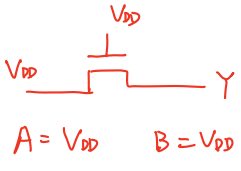






b) (4 pts) What logic function $Y = f(A, B)$ is implemented by this network?

Y = XNOR $(\overline{A \wedge B})$



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c) (4 pts) As you are browsing a library of standard cells, you find one without any schematic or notes about its function. Being a curious person, you decide to investigate this mysterious layout, so you jot down the following stick diagram:

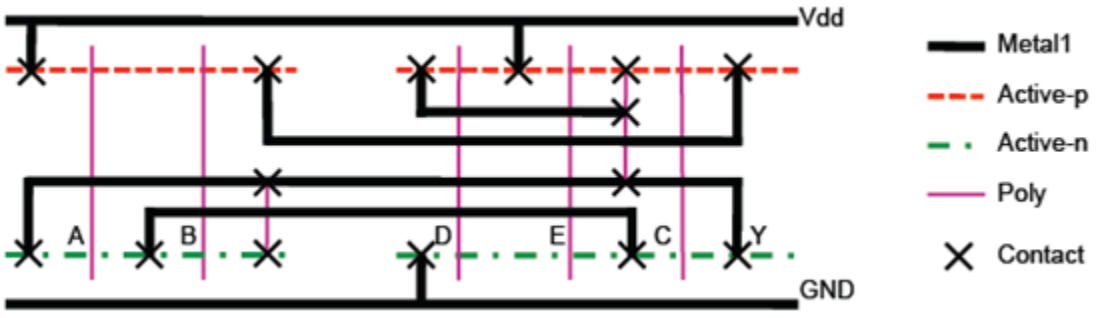
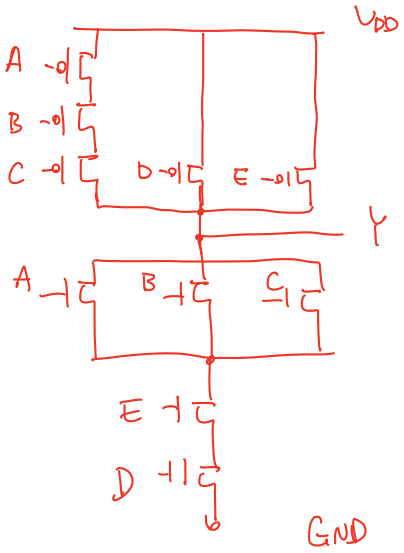


Figure 2.

Active-n and Active-p are n- and p-type diffusions, respectively, and Poly is the gate. What is the logic function of the circuit described by the stick diagram from Figure 2?



Y = $\overline{(A+B+C)\cdot D\cdot E}$.

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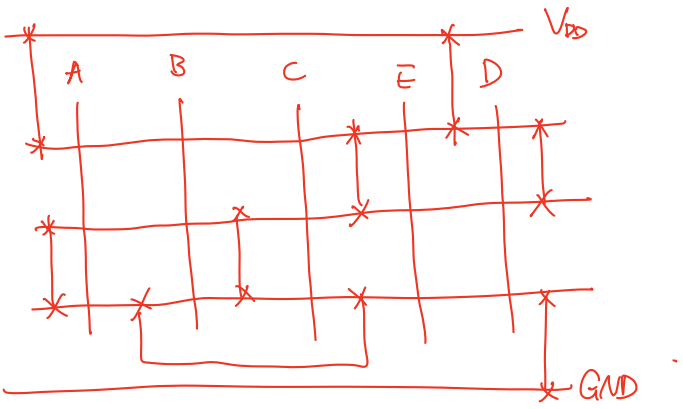
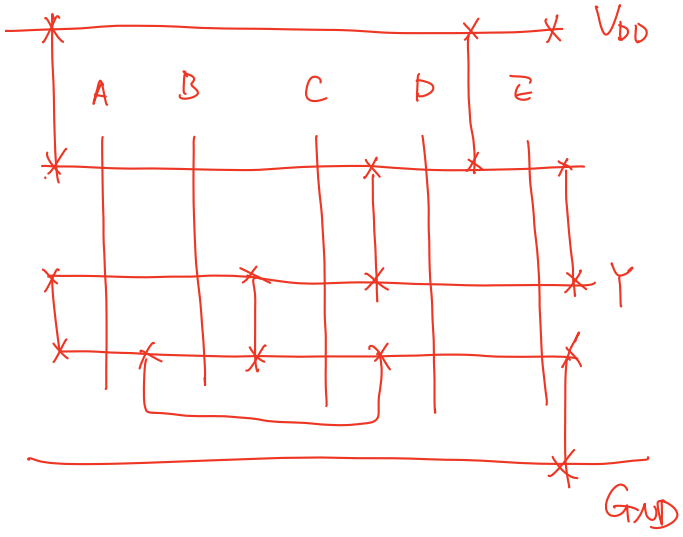
d) (4 pts) **(EECS251A only)** You realize that someone who did not take this class made the layout in Figure 2, because it is clearly not optimal. Reorder the inputs A, B, D, E, C (for the exact same logic gate) such that the layout can be realized with no diffusion breaks while still having straight polysilicon gates.





Ordering: A B C E D

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2) *Logic delay* (8 points, 10 minutes)

The delay of two logic gates, an inverter and a 2-input NOR, has been measured, and the results are plotted in Figure 3.

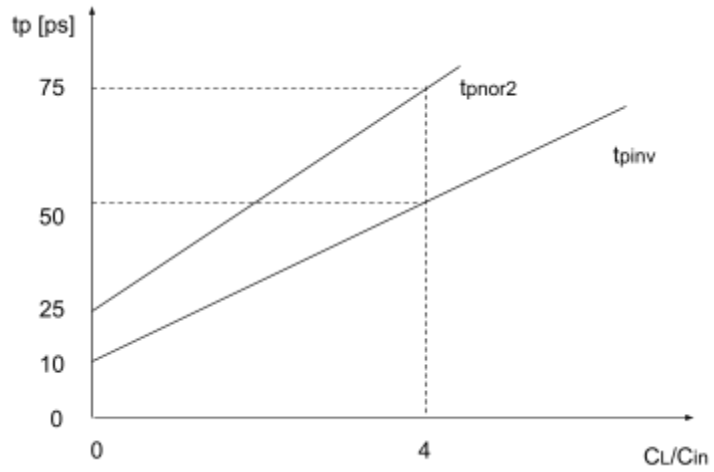

Figure 3.

a) (4 pts) Inverter delay can be modeled as $t_{pInv} = t_{p0}(p_{inv} + C_L/C_{in})$. Find the values of t_{p0}, and p_{inv} from the graph.

ps ps unitless

slope = $t_{p0} = \frac{50-10}{4-0} = 10ps.$

when $C_L/C_{in} = 0$, $10 = 10 \cdot (p_{inv} + 0)$

$\Rightarrow p_{inv} = 1$

t_{p0} = 10ps.

p_{inv} = 1.

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b) (4 pts) Find the logical effort and the intrinsic delay of the NOR2 from the graph.

$$t_{p_{nor2}} = t_{p0}\left(p_{nor2} + g_{nor2}\frac{C_L}{C_{in}}\right)$$

$$\text{slope} = t_{p0} \cdot g_{nor2} = 10\, g_{nor2}$$

$$= \frac{75-25}{4-0} = 12.5$$

$$\Rightarrow g_{nor2} = 1.25$$

when $C_L/C_{in} = 0$, $25 = 10(p_{nor2} + 1.25 \times 0)$

$$\Rightarrow p_{nor} = 2.5$$

g_{NOR2} = 1.25.

p_{NOR2} = 2.5.

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3) *Fast circuits* (12 points, 12 minutes)

A decoder logic path is shown in Figure 4. Cin, a and b are the capacitances of input pins of respective gates. Equally sized PMOS and NMOS transistors have equal on resistances and the self-loading capacitance per unit width equals the input capacitance ($\gamma = C_p/C_g = 1$).

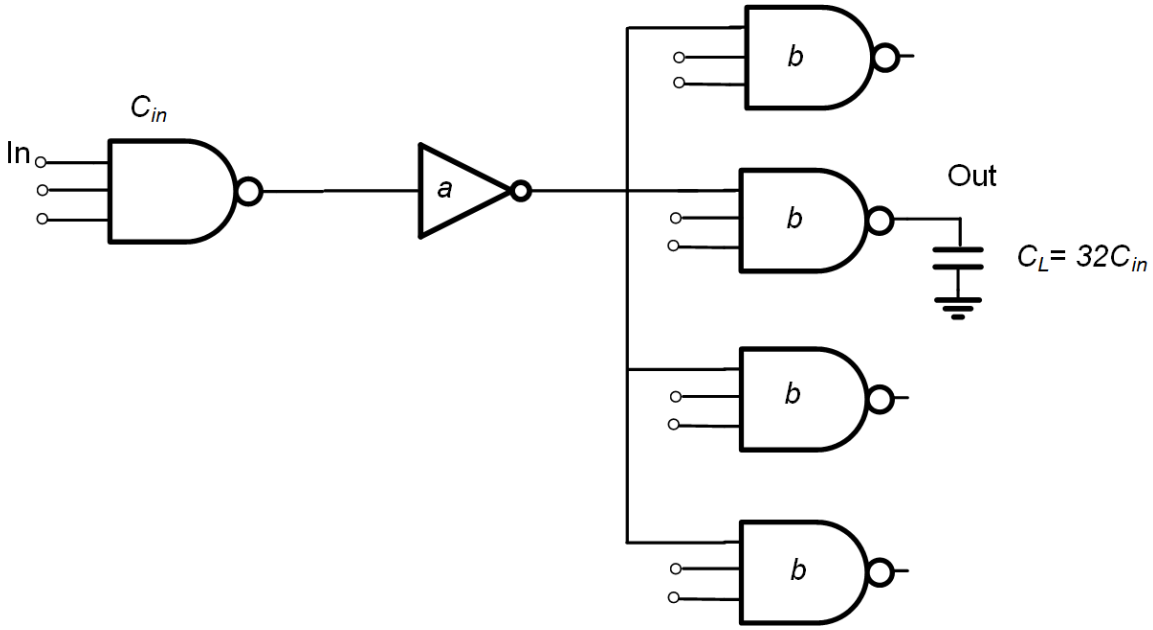

Figure 4.

a) (4 pts) What is the path effort from In to Out?

$F = 32$

$G = (2)(1)(2)$

$B = 4$

$g_{NAND3} = 2$

$GFB = (4)(32)(4)$

Path effort: H = 512.

b) (4 pts) What effort per stage, h, minimizes the delay of this decoder?

3 stages $\longrightarrow \sqrt[3]{512}$

Effort per stage: h = 8.

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c) (4 pts) Size the gates to minimize the delay from In to Out:

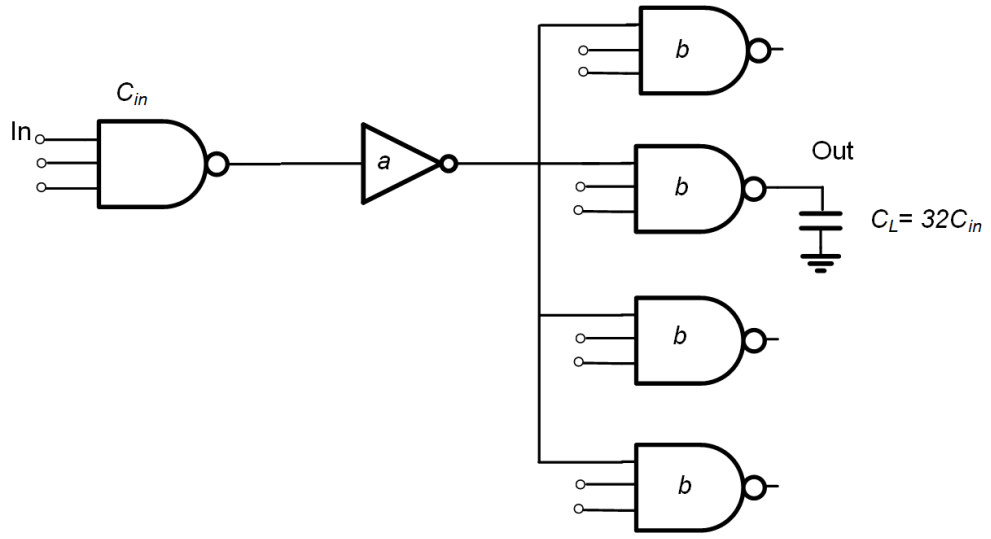

Figure 4, repeated for convenience

$EF/_{stage} = 8$

$EF_b = LE_b \cdot f_b$

$8 = 2 \cdot \frac{32C_{in}}{b}$

$b = 8C_{in}$

$EF_a = LE_a \cdot f_a \cdot 4$

$8 = 1 \cdot \frac{b}{a} \cdot 4$

$a = 4C_{in}$

Check:

$8 = 2 \cdot \frac{4C_{in}}{C_{in}}$ ✓

Gate	*Input capacitance, normalized to Cin*
a	4
b	8

4) *Energy* (12 points, 12 minutes)

We would like to examine some properties of a single-cycle RISC-V datapath. The datapath has the following properties:

- Total capacitance of all gates: 10nF
- Max Frequency @ 1.0V: 200 MHz
- Supply voltage: 1.0V

The CPU runs a workload with the following properties:

- Activity factor α: 0.1
- Number of instructions: 1000

In this question, you may ignore leakage and short-circuit power (though this is unwise in a real design).

a) (2 pts) What is the dynamic power consumption?

$0.1 * 10\,nF * (1.0\,V)^2 * 200\,MHz = 200\,mW$

P = _____ mW.

b) (2 pts) How much energy is consumed by this workload?

$200\,mW * \frac{1\frac{cycle}{inst}}{200*10^6\frac{cycle}{s}} * 1000\,inst$

$= 0.2\frac{J}{s} * 0.5 * 10^{-8}\frac{s}{inst} * 1000\,inst$

$= 0.1 * 10^{-8}\frac{J}{inst} * 1000\,inst$

$= 0.1 * 10^{-5} J = 1\,\mu J$

E = _____ µJ.

c) (8 pts) If we lower the the supply to 0.9V:

- The new clock frequency will be (assuming that the drain current is linearly proportional to supply voltage):

$$200\ MHz\ *\ \frac{0.9\ V}{1.0\ V} = 180\ MHz$$

f_{Clk} = _____ MHz.

- The compute time for the workload will be:

$$1000\ inst\ *\ 1\frac{cycle}{inst} * \frac{1}{180 * 10^{6}\frac{cycle}{s}}$$
$$= 1000\ cycle\ * \frac{1}{180} * 10^{-6}\frac{s}{cycle}$$
$$= \frac{1}{180} * 10^{-3}\ s$$
$$= \frac{1}{180} ms$$
$$= \frac{1000}{180}\mu s = \frac{50}{9}\mu s = 5.56\ \mu s$$

T = _____ µs.

- The new total energy will be:

$$P = 0.1\ *\ 10\ nF\ *\ (0.9\ V)^2\ *\ 180\ MHz = 145.8\ mW$$
$$E = P\ *\ T = 145.8\ mW\ *\ 5.56\ \mu s = 0.81\ \mu J$$

E = _____ µJ.

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5) *Wires* (6/12 points, 12 minutes)

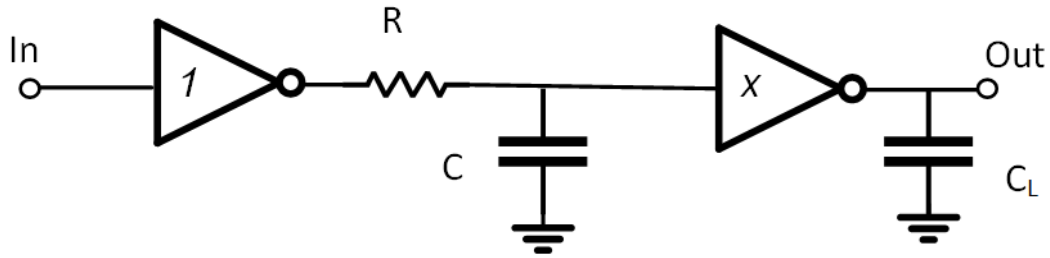
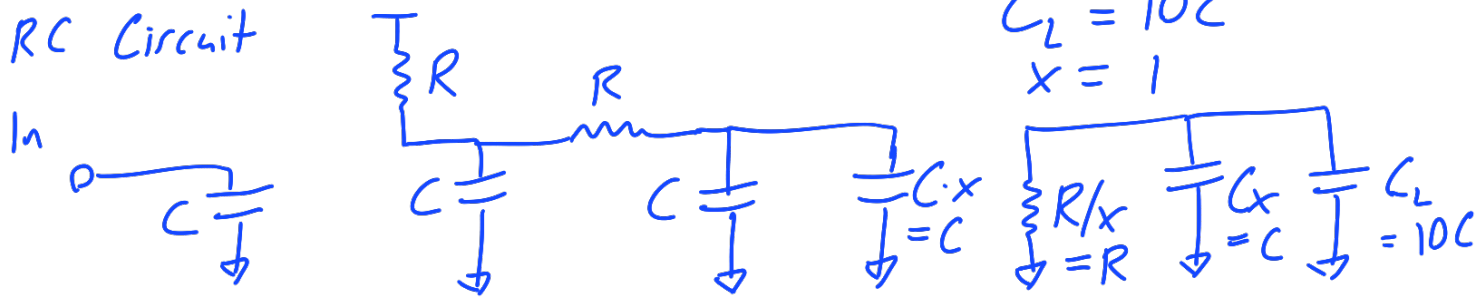


Figure 5.

A pair of inverters are shown in Figure 5. The input inverter is unit-sized, with an on-resistance R and an input capacitance that equals self-loading capacitance of C (γ = 1). The second inverter has a size that is x times the unit inverter. A wire in between the two inverters has the resistance R and capacitance C that equals the input capacitance and on-resistance of a unit inverter. Output capacitance, C_L, is 10 times the unit capacitance. The delay of a fanout-of-1 inverter is 10ps.

a) (6 pts) Find the propagation delay from input (In) to the output (Out), for x =1. When calculating the delay, assume that both inverters have step transitions at their inputs.

(1) RC Circuit

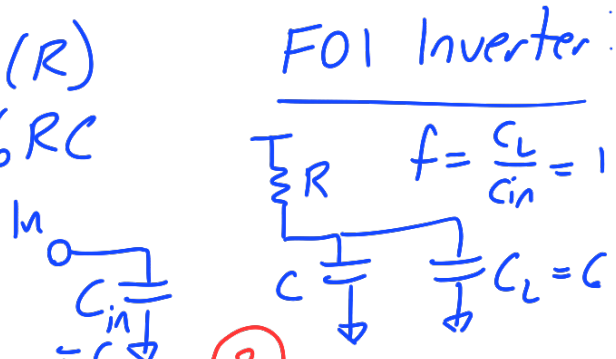


(2) $\tau_d = C(R) + (2C)(2R) + (11C)(R)$
$= RC + 4RC + 11RC = 16RC$

(4) $t_d = \ln(2) \cdot \tau_d = \ln(2) \cdot 16RC$
$= 2\ln(2)RC \cdot 8$
$= 10ps \cdot 8$

tp= 80 ps.

FO1 Inverter:



(3) $t_{FO1} = \ln(2)R(2C)$
$= 10ps$

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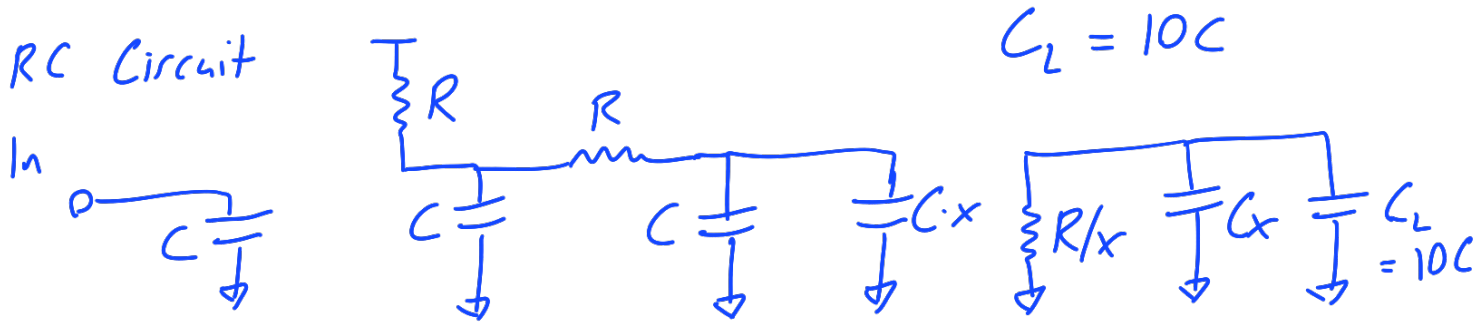
b) (6 pts) **(EECS251A only)** Find the size of the second inverter, x, that minimizes the propagation delay.



① $\tau_d = C(R) + ((+Cx)(2R) + (Cx+10C)\left(\frac{R}{x}\right)$

$= RC + 2RC + 2RCx + RC + 10RC/x$

$= 4RC + 2RCx + 10RC/x$

$\frac{\partial \tau_d}{\partial x} = 2RC - \frac{10RC}{x^2} = 0$

②

$\frac{10RC}{x^2} = 2RC$

$x^2 = \frac{10RC}{2RC} = 5 \rightarrow x = \sqrt{5}$

③

x = $\sqrt{5}$.

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6) *Adders* (11 points, 13 minutes)

a) (4 pts) A single-bit full adder, with inputs A, B and Ci and outputs Co and S, is shown in Figure 6. In this case, the propagate signal P, is defined as
P = A XOR B. Please fill in the boxes with signals (A, B, C_i), or their complements, that would make the adder operate correctly. Also, please label the corresponding multiplexed inputs as 0 or 1.

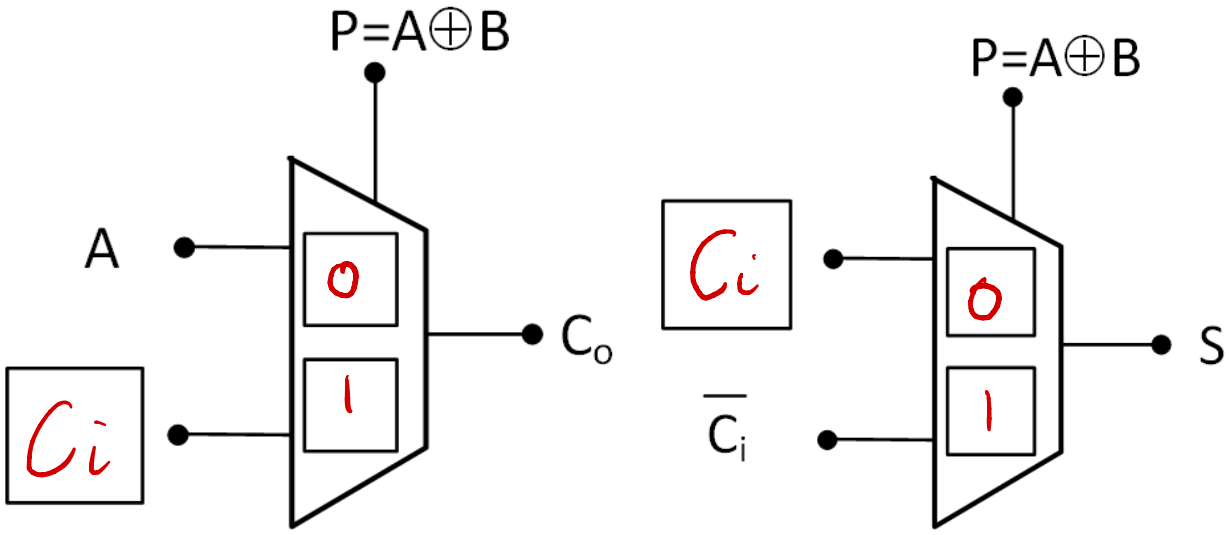

Figure 6

A	B	Ci	P	Co
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	1

$P = A \oplus B$
$= \bar{A}B + \bar{B}A$

$S = A \oplus B \oplus C_i$
$= P \oplus C_i = \bar{P}C_i + \bar{C}_i P$

$P = A \oplus B$
$C_o = AB + (A+B)C_i$

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b) (6 pts) Consider a carry-bypass (sometimes called 'carry-skip') adder, shown in Figure 7. Each full adder cell (labeled as a '+' box in the diagram) can be assumed to have one multiplexer delay from C_i to C_O.and one multiplexer delay from C_i to S. You can assume that the sum and carry paths have been realized by the circuits from part a) and therefore have equal delays. For an N-bit adder divided into k uniform b-bit groups, find the optimal b that minimizes the overall delay from $C_{i,0}$ to S_{N-1} (in terms of N).

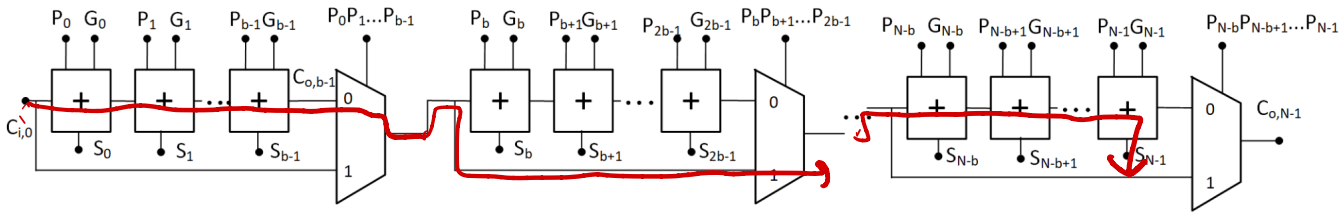

Figure 7

$$t_{p_{C_{i,0}\to S_{N-1}}} = b\cdot t_{carry} + \left(\frac{N}{b}-1\right)t_{mux} + (b-1)t_{carry} + t_{sum}$$

$$= b\cdot t_{mux} + \left(\frac{N}{b}-1\right)t_{mux} + (b-1)t_{mux} + t_{mux}$$

$$\frac{d\,t_{p_{C_{i,0}\to S_{N-1}}}}{db} = t_{mux} - \frac{N}{b^2}t_{mux} + t_{mux}$$

$$0 = 2t_{mux} - \frac{N}{b^2}t_{mux}$$

$$\frac{N}{b^2} = 2,\quad b^2 = \frac{N}{2},\quad b = \sqrt{N/2}$$

b = $\sqrt{\frac{N}{2}}$ bits.

c) (1 pt) Evaluate part b) for N=128

$$\sqrt{128/2} = \sqrt{64} = 8$$

b = 8 bits.