EECS 151/251A Discussion 7

Alisha Menon

10/12/21, 10/13/21, 10/18/21

Administrativia

- Slip week for labs – lab 5 due **10/15, 11:59pm**
- Homework 5 posted, due **10/15, 11:59pm**

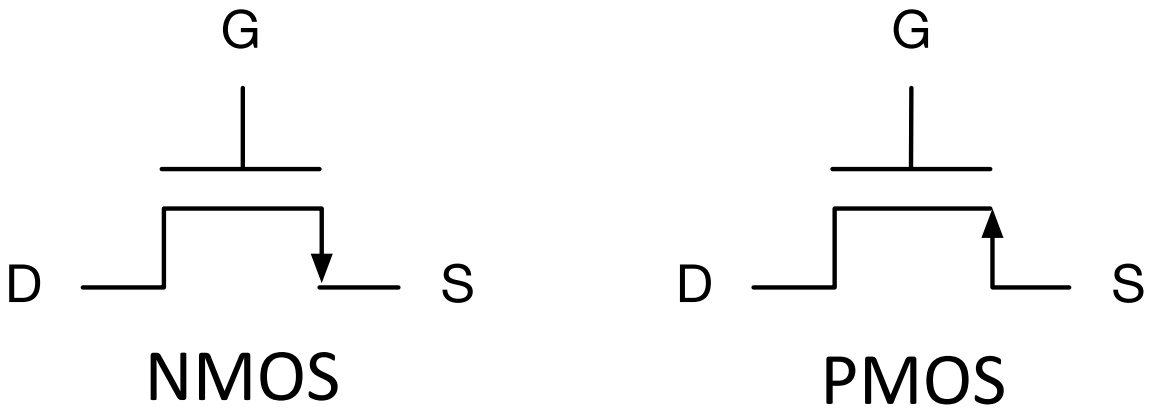
Agenda

- Transistor as a switch model
- Inverter
- Complementary CMOS gates

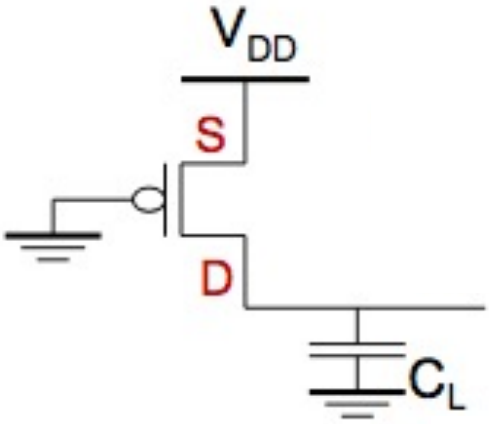
Transistor Models

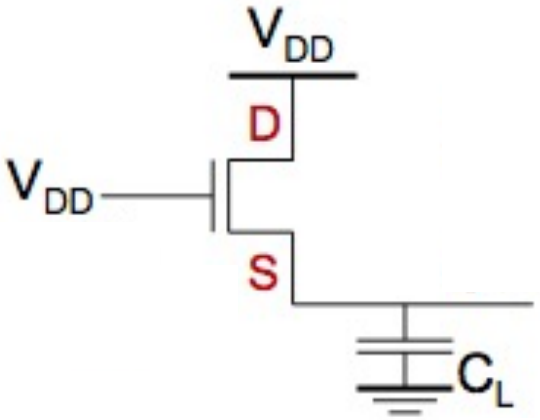
Transistor review

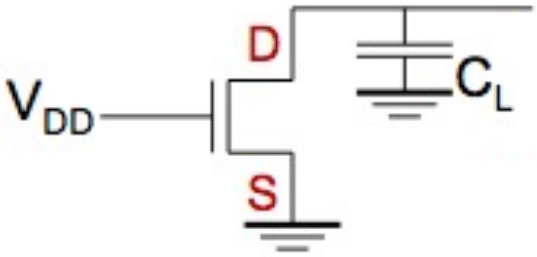
- CMOS
  - Complementary Metal Oxide Semiconductor (FET)
- Transistor basics
  - N-type or P-type – based on carrier type
  - Potential between source and gate forms a “channel”
  - Channel connects source and drain
  - Defined by “threshold” voltage V_{th}

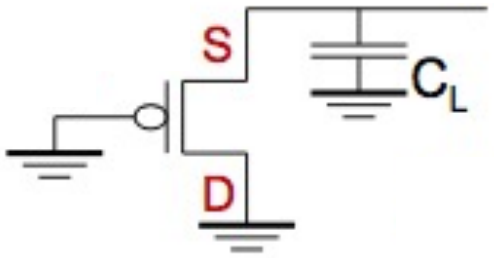


Transistors connect outputs to supplies

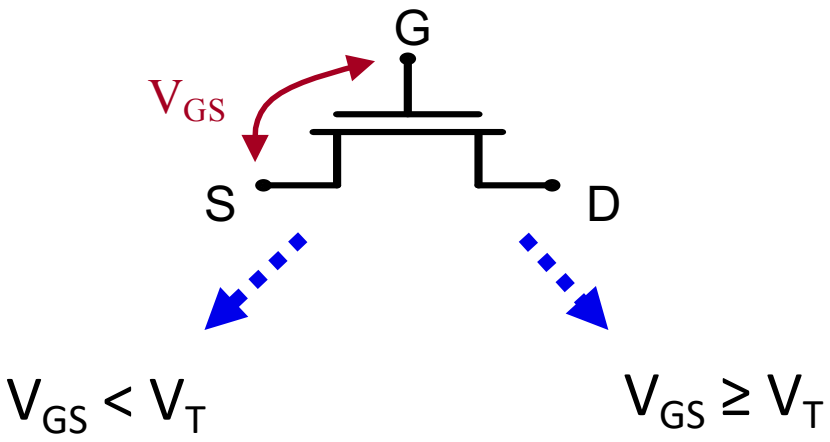








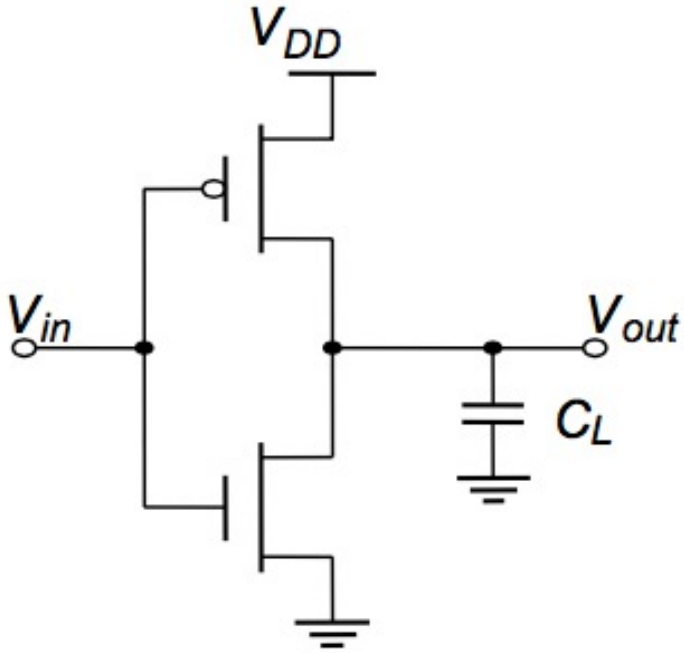
Transistors as switches

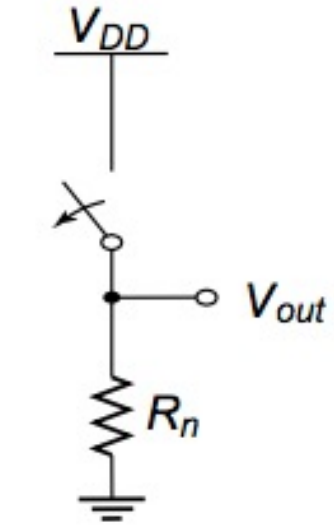


Inverters

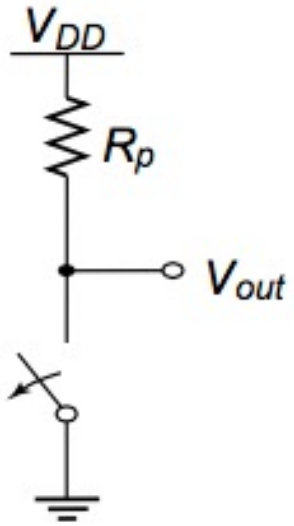
CMOS inverter

Most basic CMOS logic gate





$V_{in} = V_{DD}$

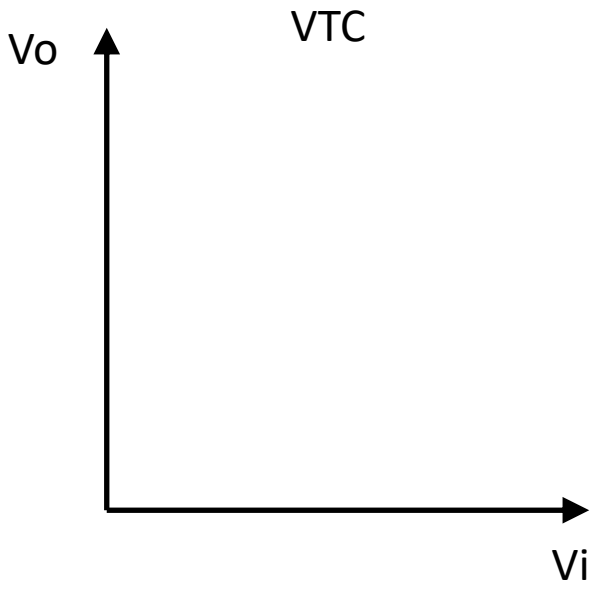


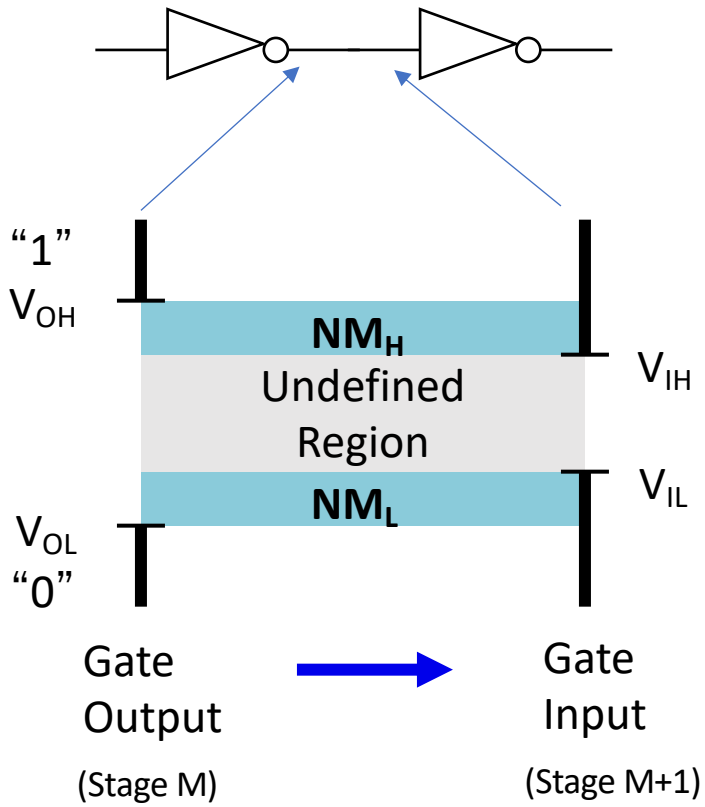
$V_{in} = 0$

Inverter noise margins

Noise margin high:
$NM_H = V_{OH} - V_{IH}$

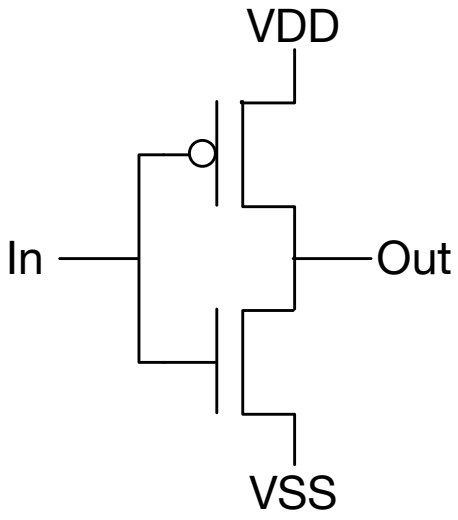
Noise margin low:
$NM_L = V_{IL} - V_{OL}$





Static complementary CMOS

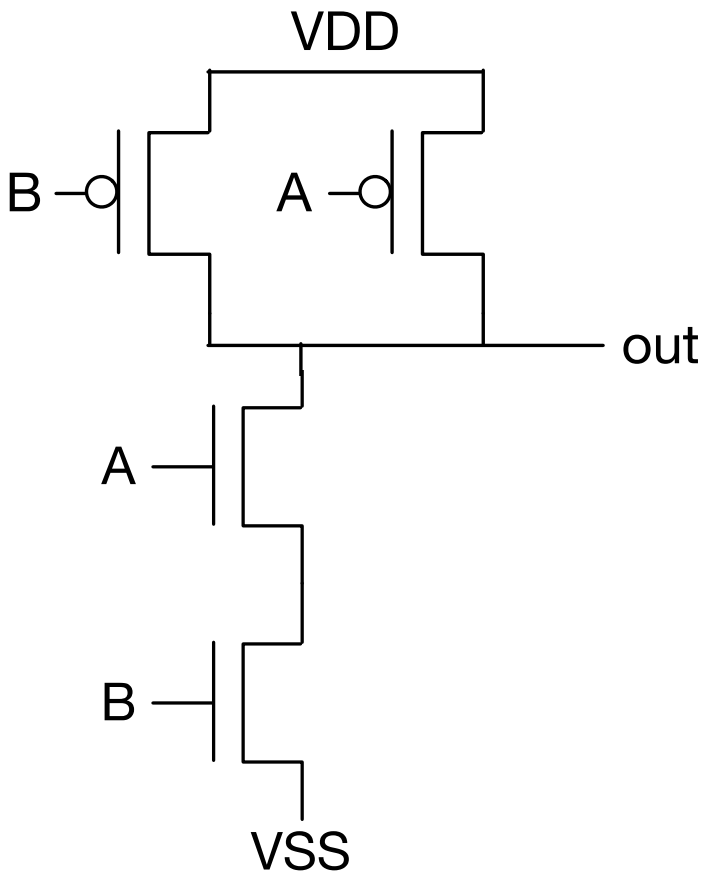
Static gates



Static complementary CMOS

NAND gate

NAND gate



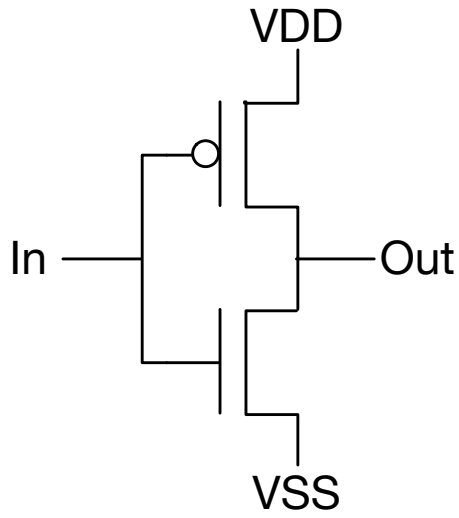
- Notice that the PUN and PDN are "opposite"
  - Meaning serial vs. parallel
  - This concept known as "duality"
- Also notice that the gate was inverting
  - How do we make an AND? (next slides)
- Easiest way to make a gate is to define the PDN first
  - Make the PUN by flipping the branches of the PDN

XNOR gate

AND gate

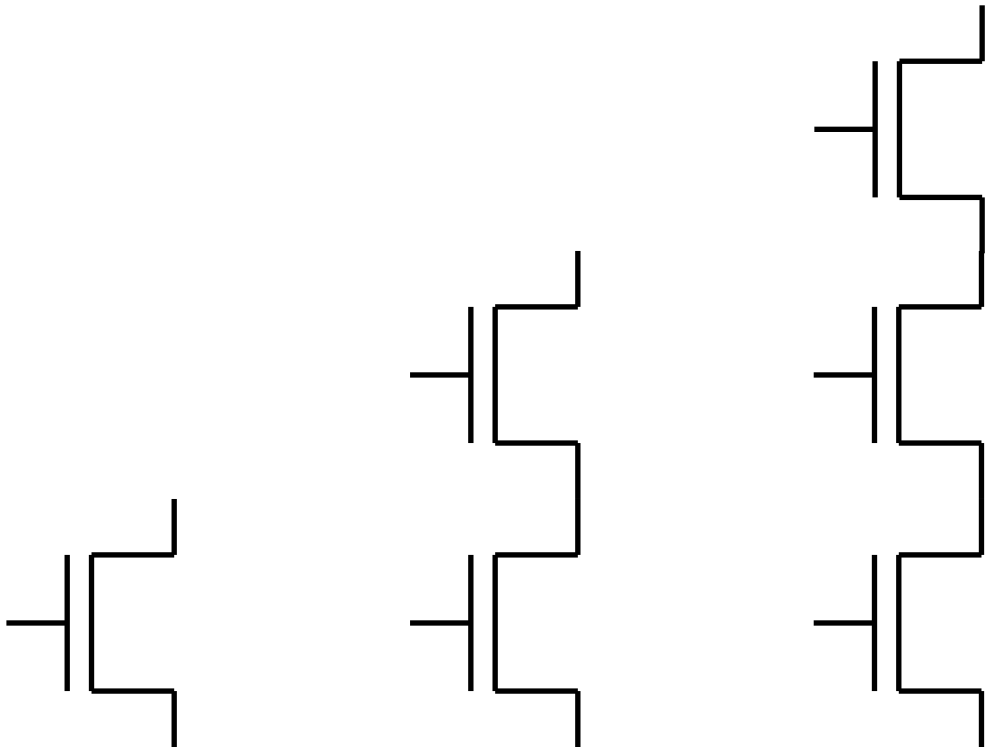
CMOS gate sizing

- Choosing the width of a transistor (typically use minimum length)
- Minimum sized inverter:

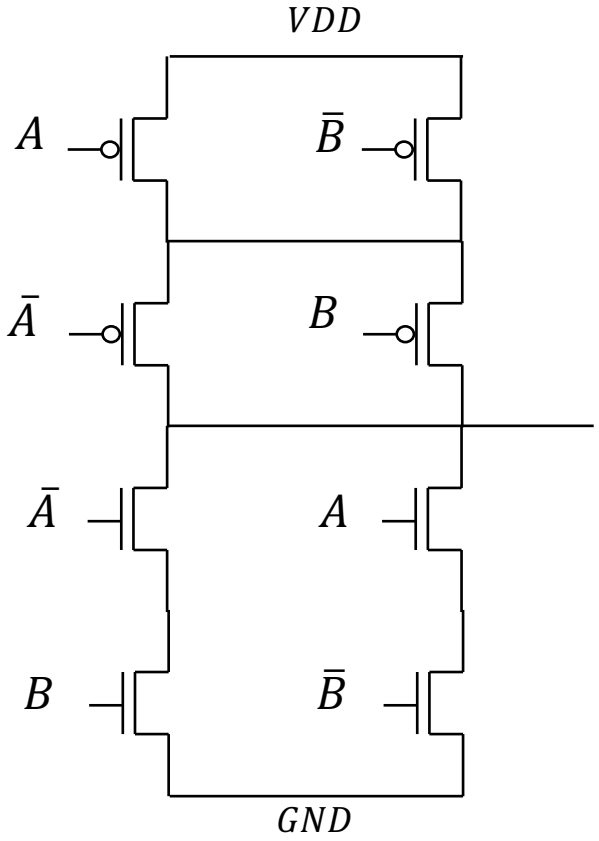


- **Unless otherwise stated**, complex gates should:
  - Have equal pull-up and pull-down resistances
  - Pull-up and pull-down resistances equivalent to minimum sized inverter

Transistor stacks – R vs. W

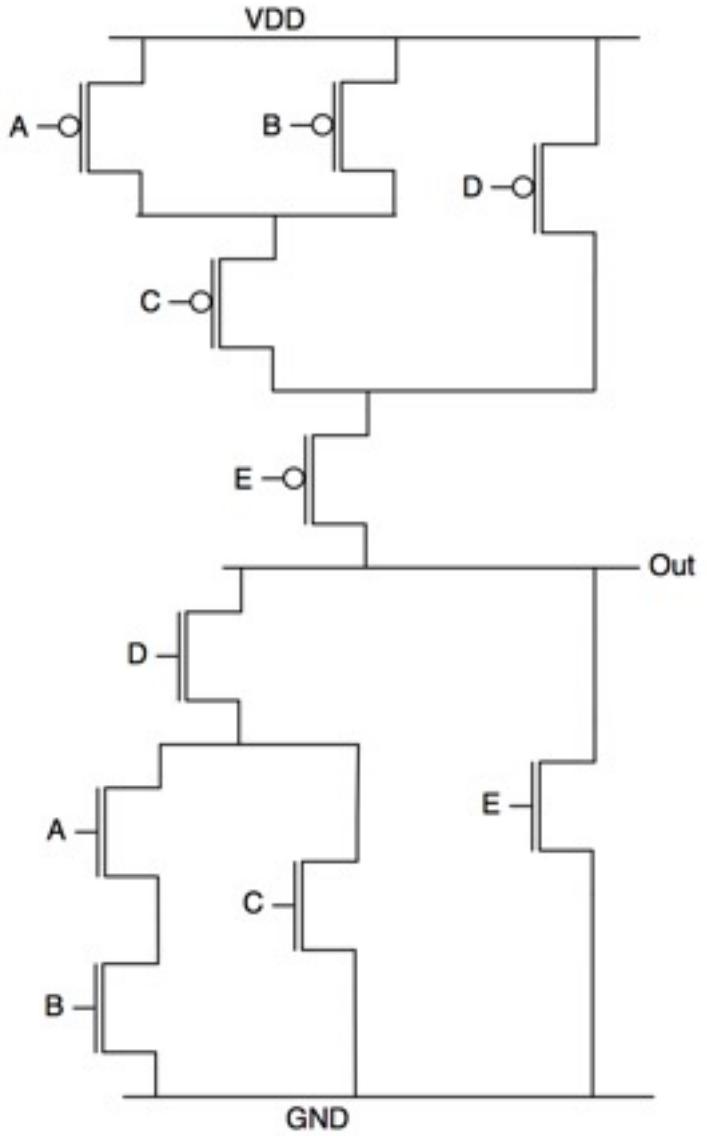


Gate sizing example – XNOR



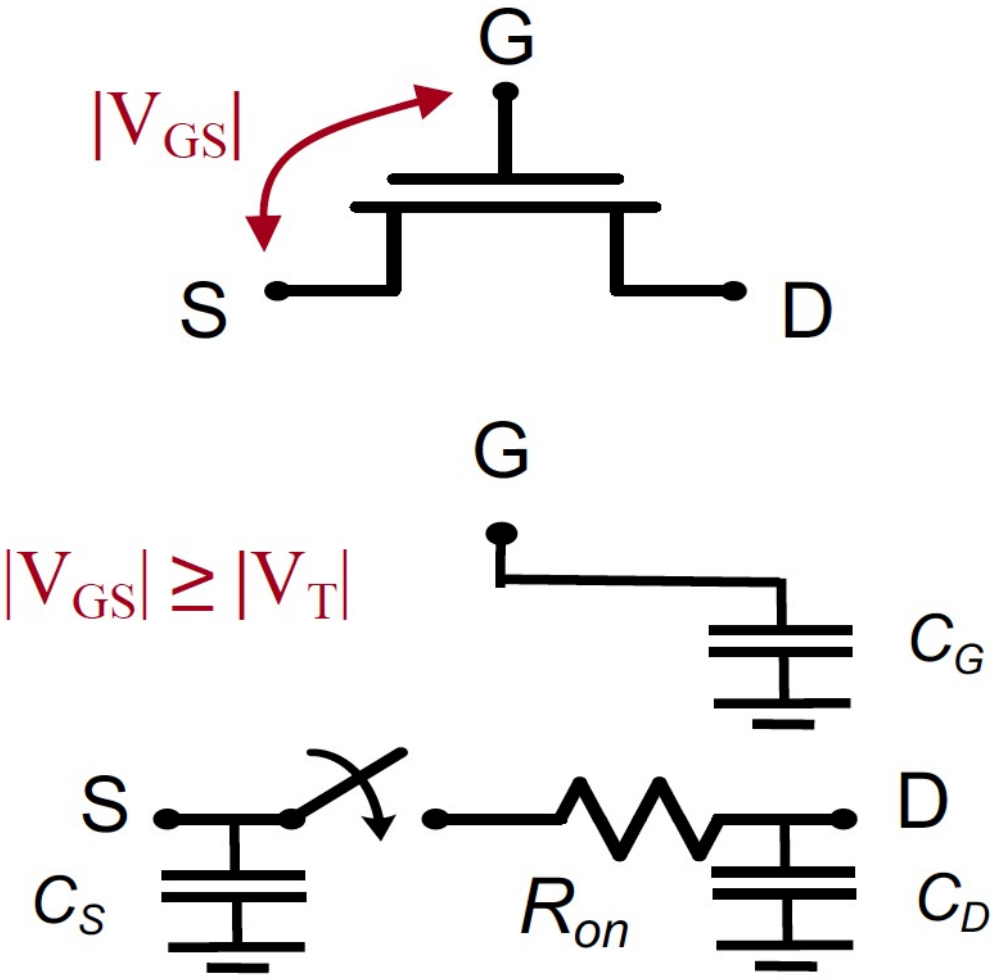
Gate sizing example

$R_{on,p} = 3*R_{on,n}$

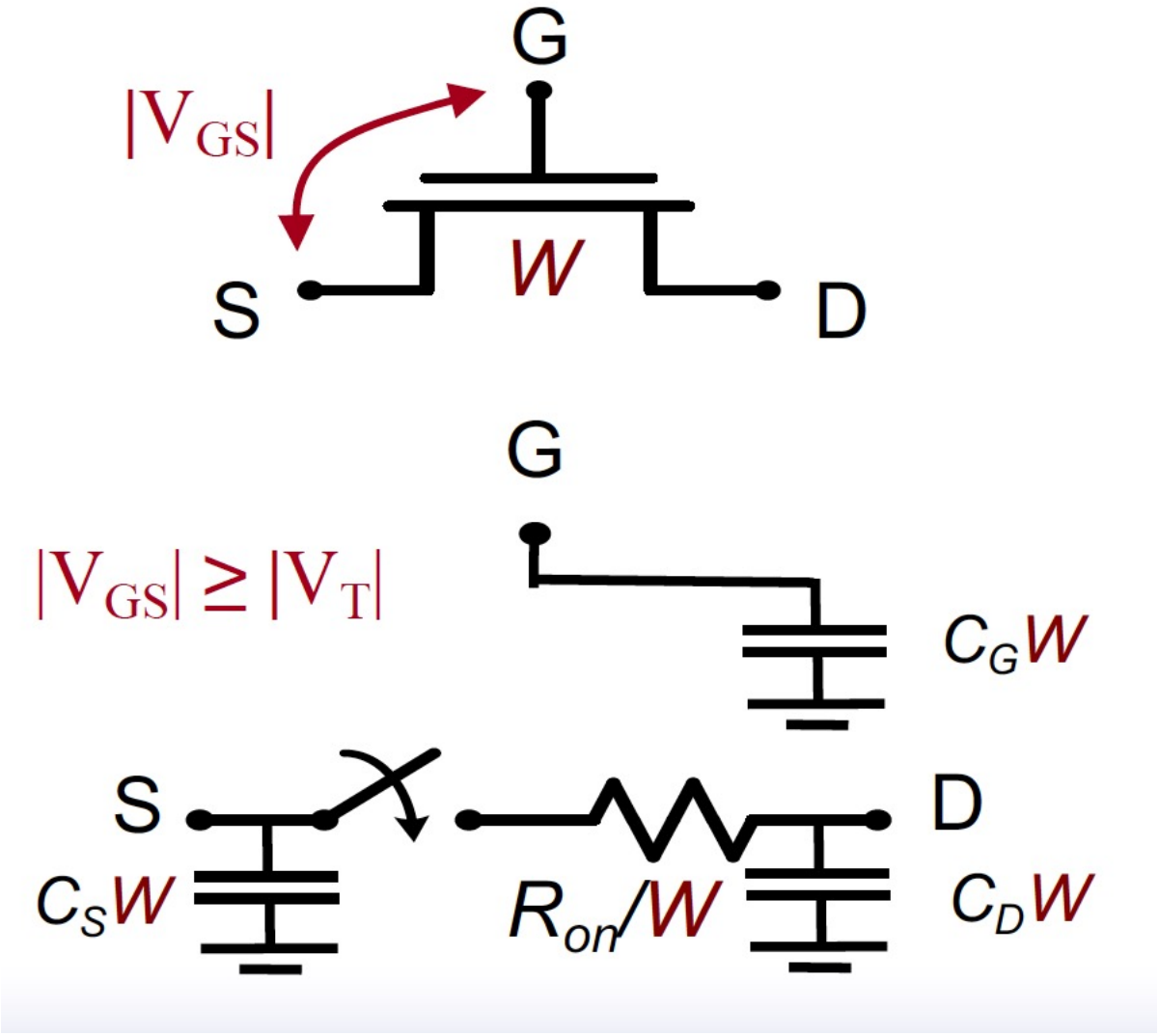


Inverter delay

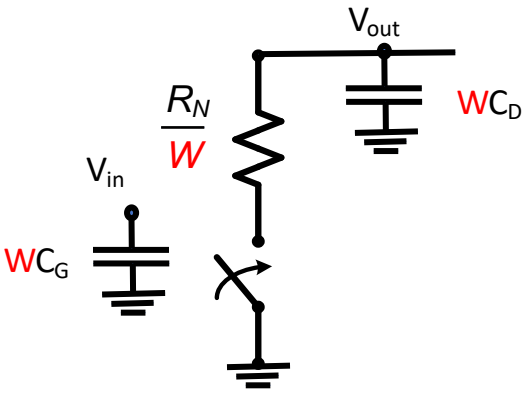
Simple dynamic model



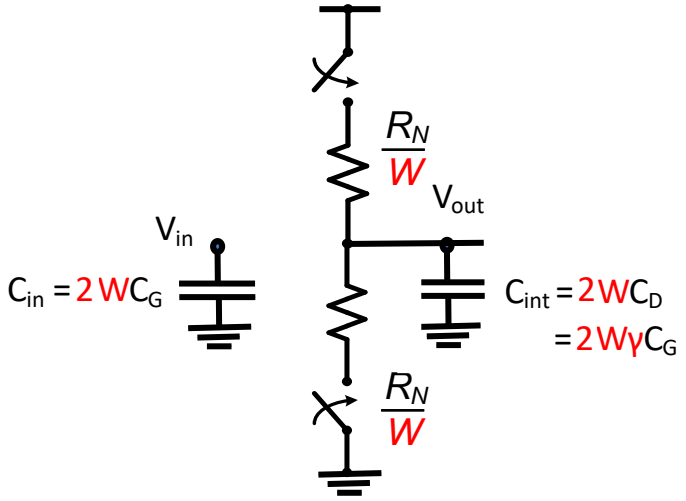
Simple dynamic model

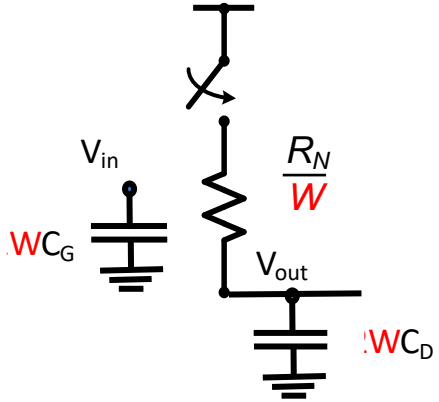


Inverter delay



NMOS with size W





PMOS with same R as NMOS

Inverter fanout