EECS 151/251A SP2022 Discussion 4

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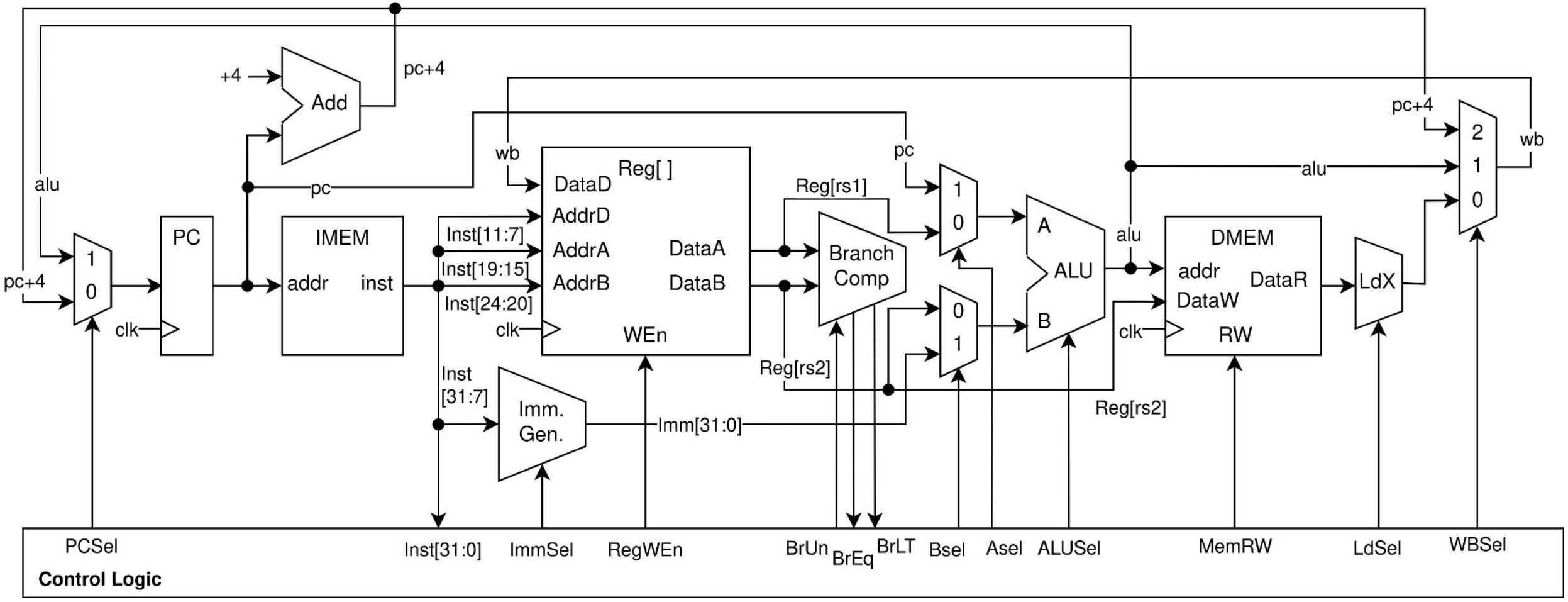
Agenda

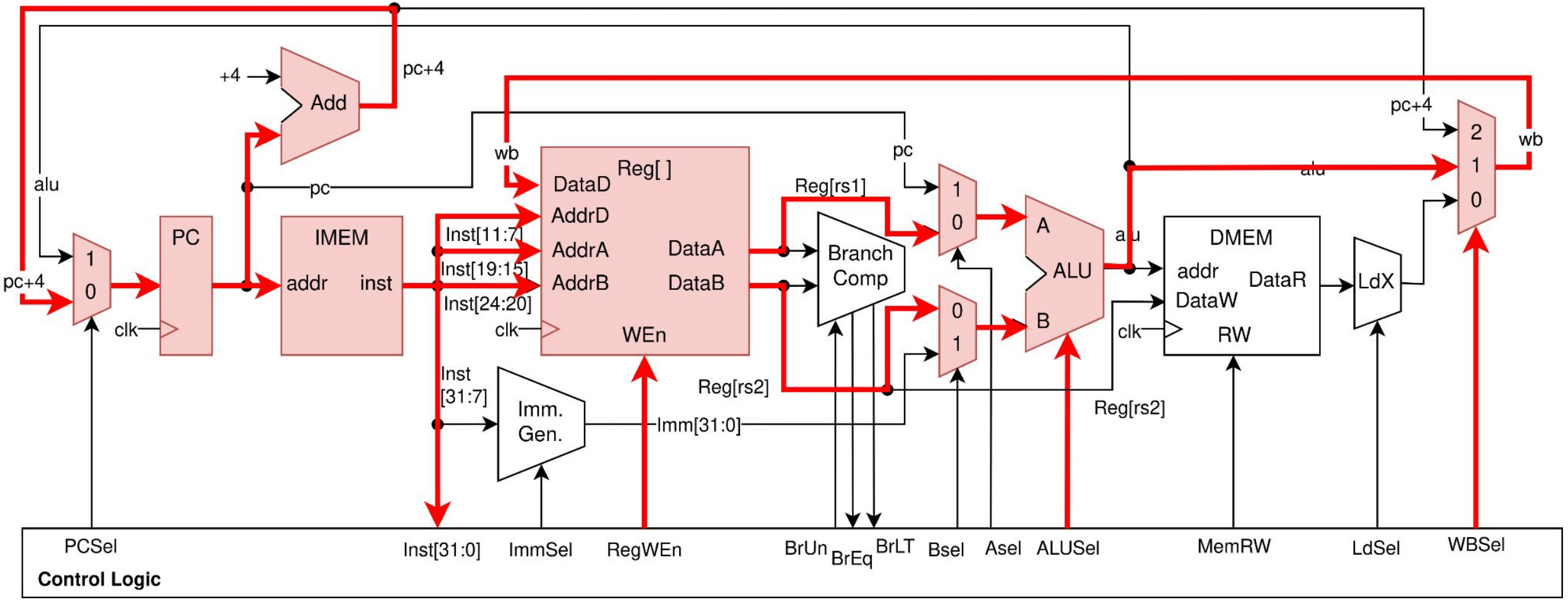
- Datapath
- Pipelining
- Hazards

Datapath

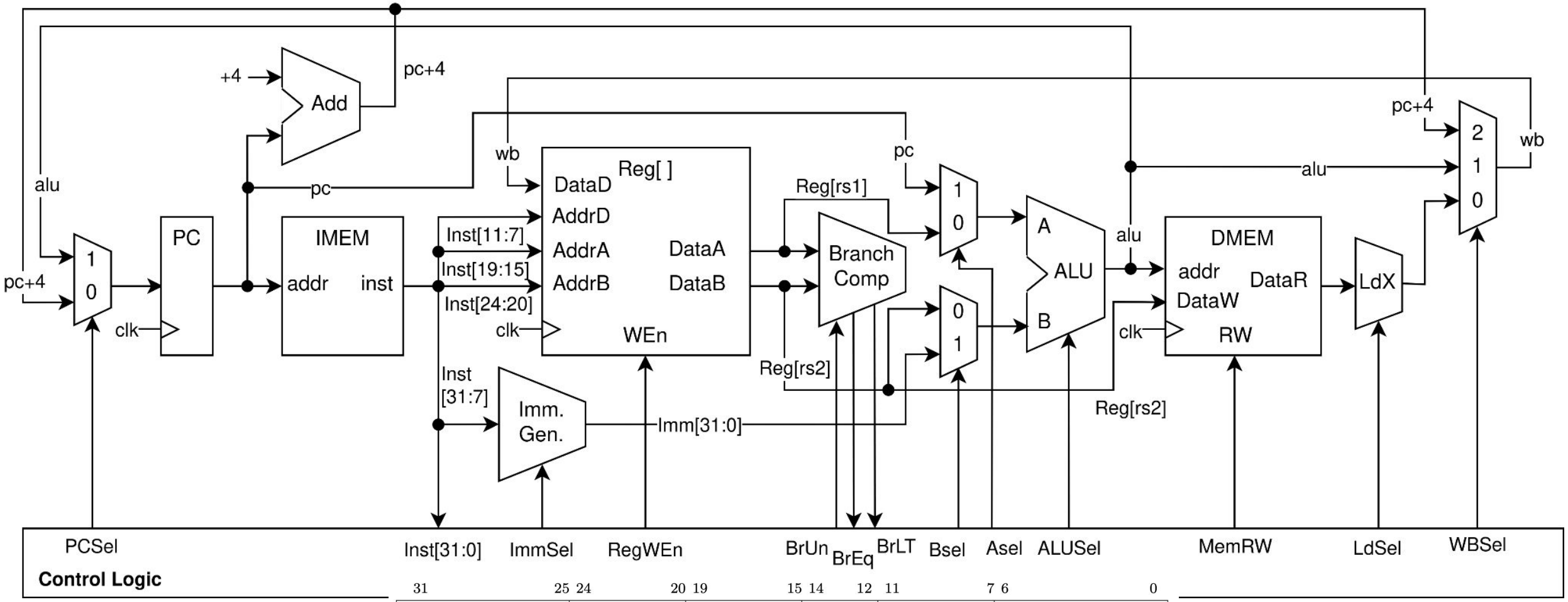
Full RISC-V Datapath



Full RISC-V Datapath: add

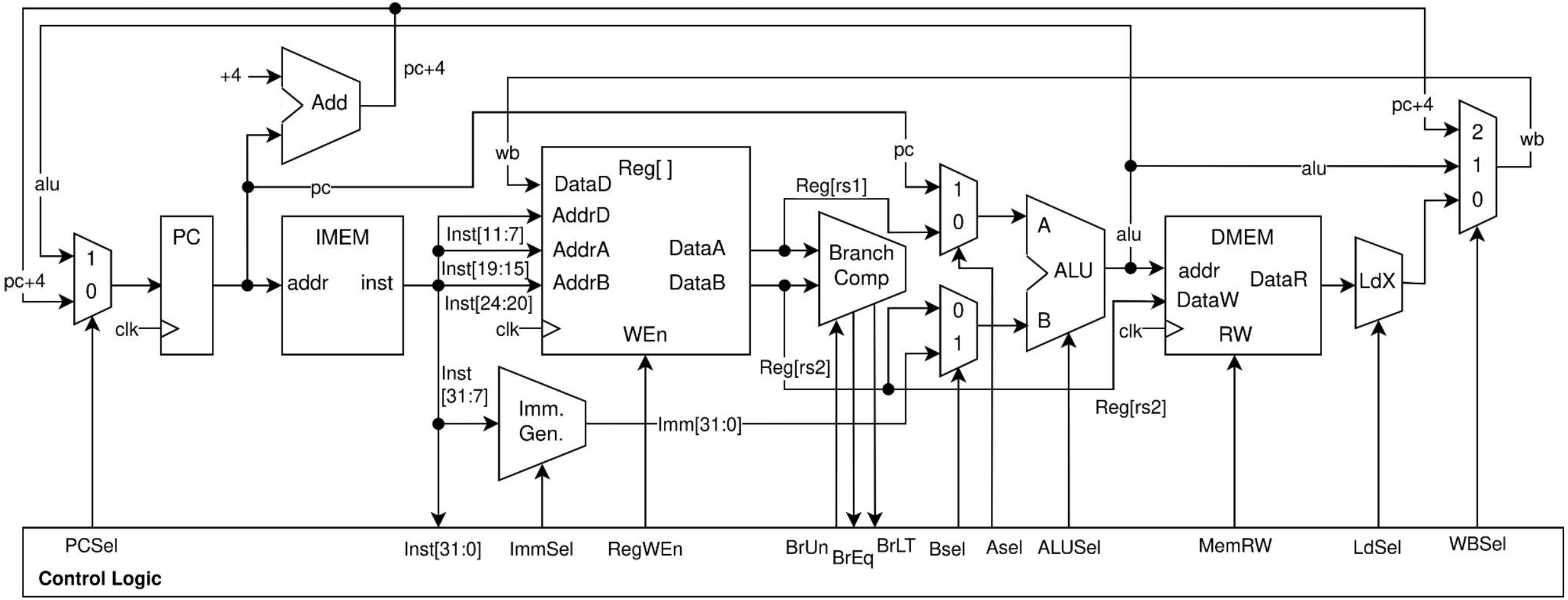


Full RISC-V Datapath: sw exercise



31 25	24 20	19 15	14 12	11 7	6 0
imm[11:5]	rs2	rs1	funct3	imm[4:0]	opcode
7	5	5	3	5	7
offset[11:5]	src	base	width	offset[4:0]	STORE

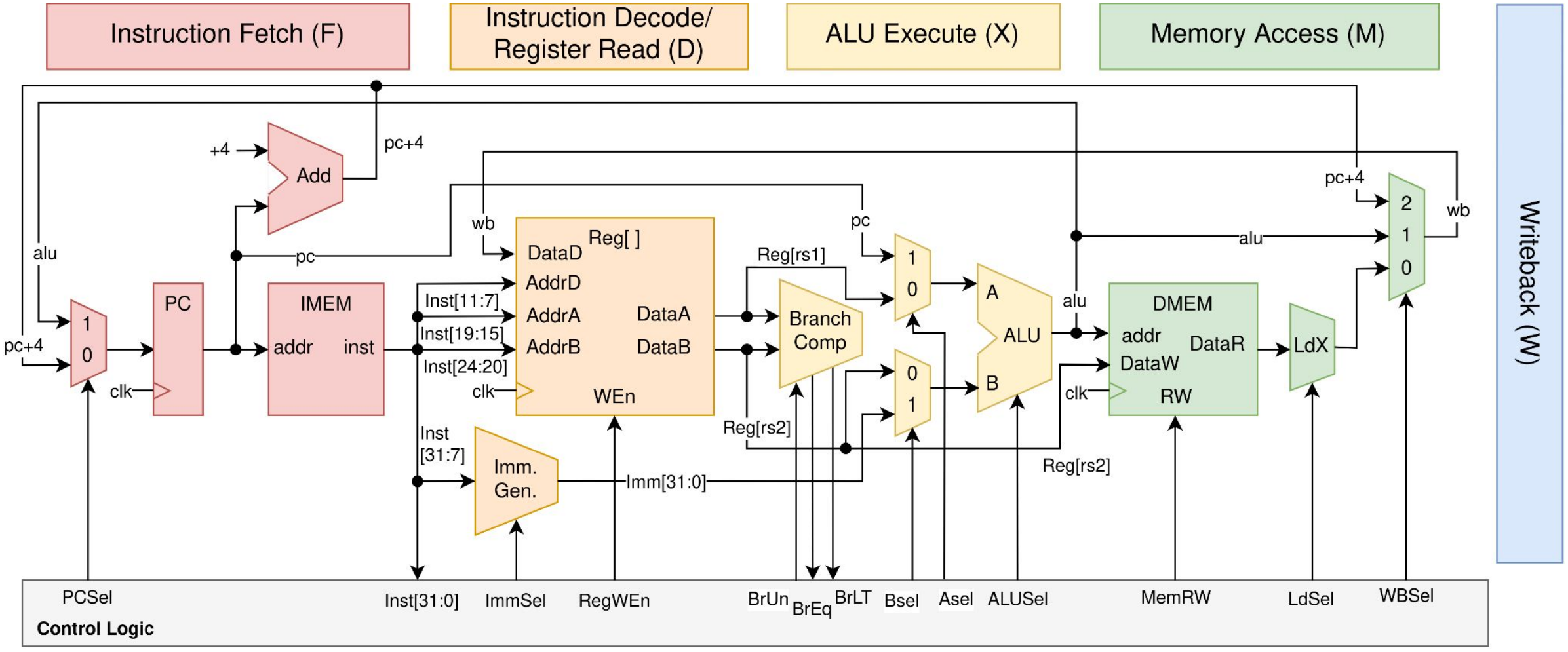
Full RISC-V Datapath: beq exercise



31	30 25	24 20	19 15	14 12	11 8	7	6 0
imm[12]	imm[10:5]	rs2	rs1	funct3	imm[4:1]	imm[11]	opcode
1	6	5	5	3	4	1	7

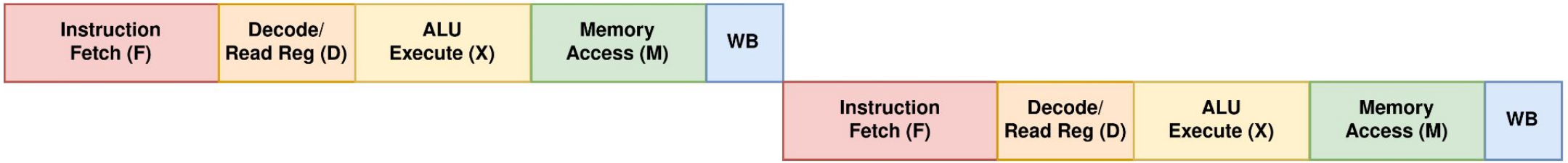
Pipelining

Full RISC-V Datapath: Stages

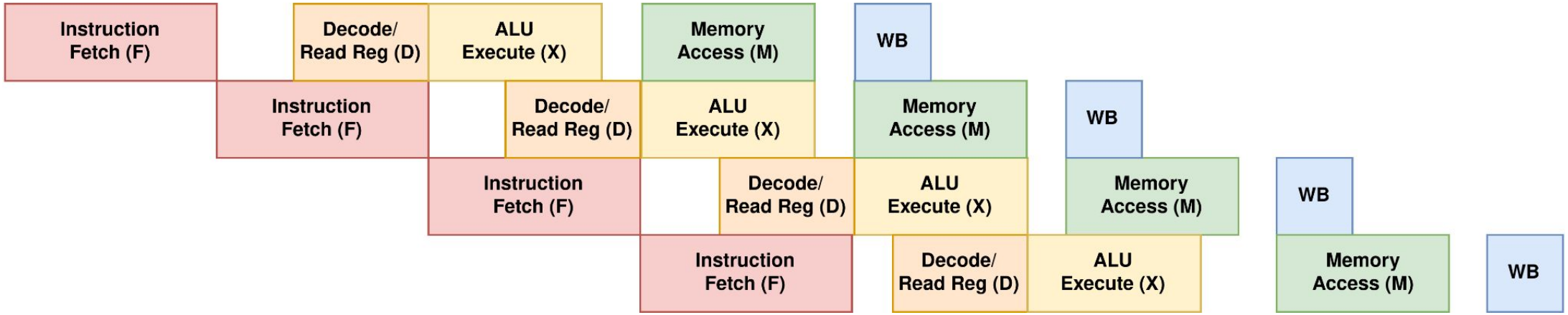


Why Pipeline?

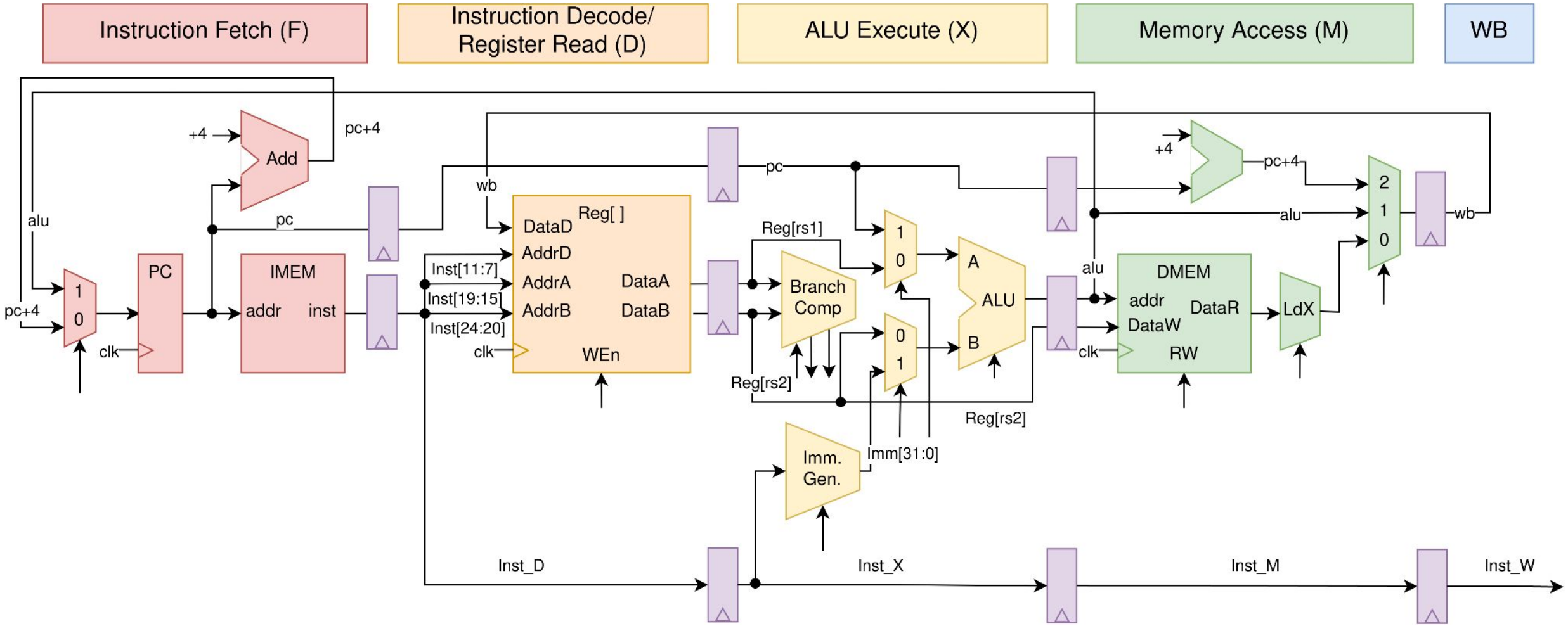
Single Cycle



Pipelined



Converting To Pipelined Design



Hazards

Hazards

- Structural hazard
  - A single resource is required by more than one instructions
  - We have solved some structural hazard! (e.g. RegFile with 2 reading port)
- Data hazard
  - One (or more) source register is not ready when being used
  - Can be solved by forwarding (trade complexity for performance)
- Control hazard
  - For branch instructions, we cannot know if it is taken at next cycle
  - branch prediction

Data Hazard - Stall

- Consider a 5-stage pipeline:

```
add x3, x1, x2
sub x4, x1, x2
xor x5, x1, x3
or  x6, x2, x5
```

#	IF	D	EX	M	WB
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					

Data Hazard - Stall

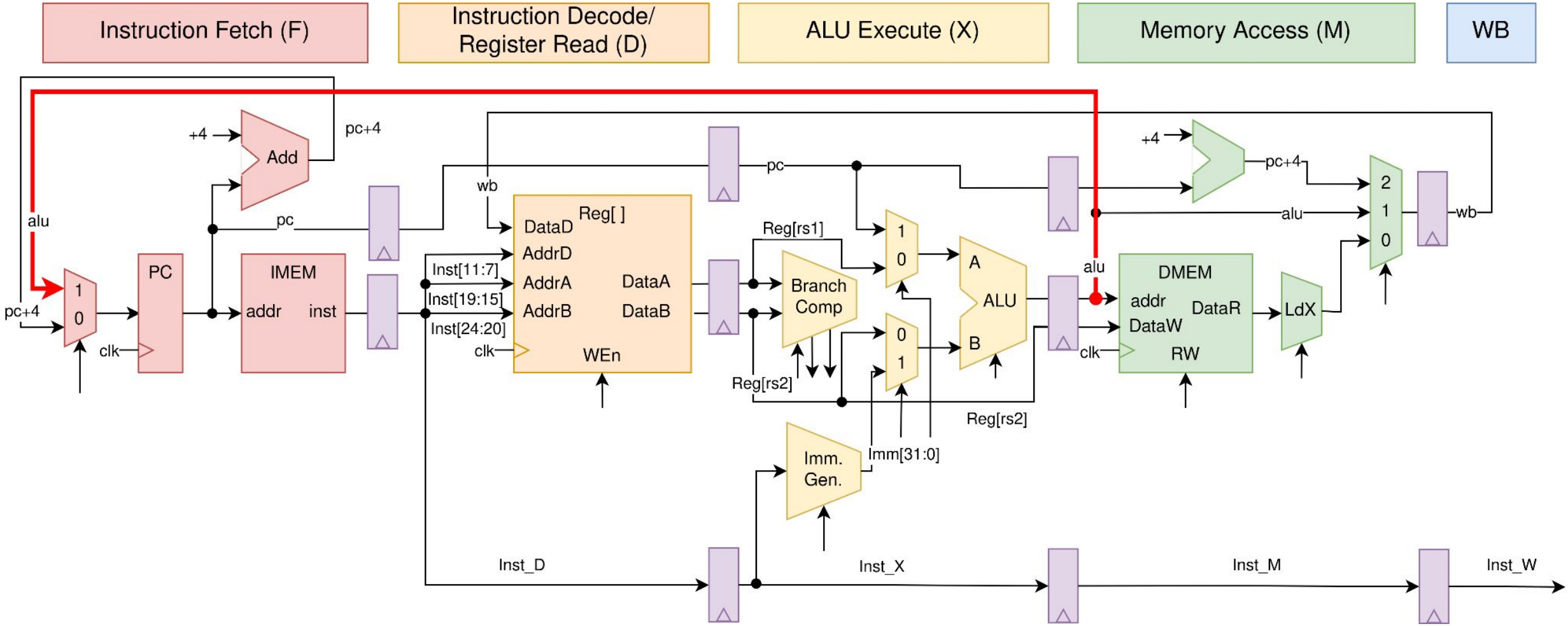
- Consider a 5-stage pipeline:

```
add x3, x1, x2
sub x4, x1, x2
xor x5, x1, x3
or  x6, x2, x5
```

#	IF	D	EX	M	WB
1	add				
2	sub	add			
3	xor	sub	add		
4	or	xor	sub	add	
5	or	xor	-	sub	add
6		or	xor	-	sub
7		or	-	xor	-
8		or	-	-	xor
9			or	-	-
10				or	-
11					or

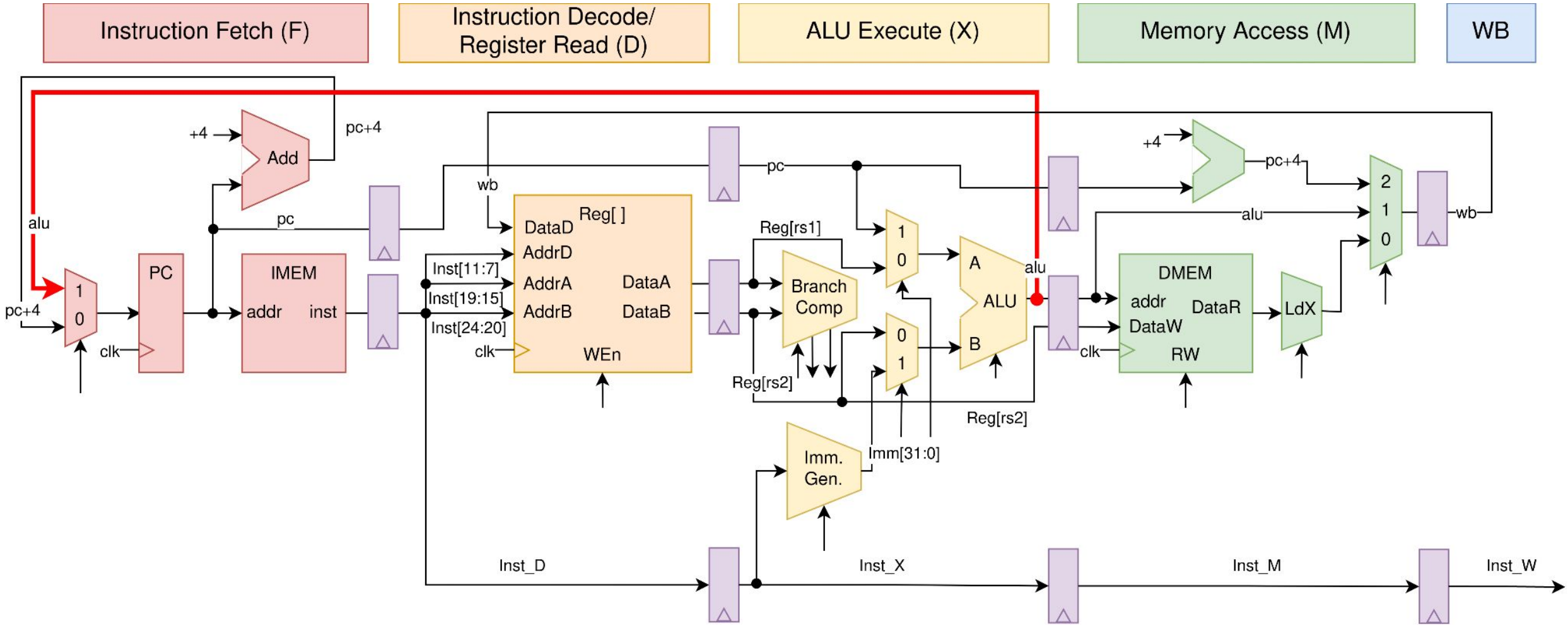
Control Hazard

How many missed cycles on a mispredict?



Control Hazard

How many missed cycles on a mispredict?



Questions?