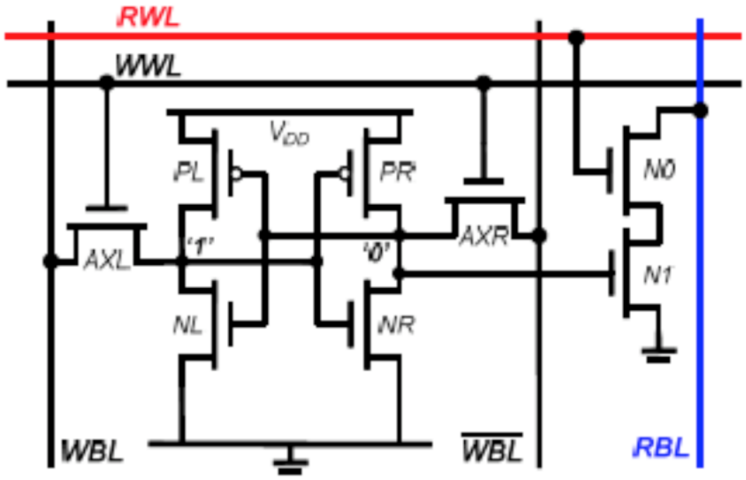
EECS 151/251A Homework 10

Due 11:59pm Tuesday, November 23th, 2021

1 8T SRAM Cell

Consider the 8T SRAM cell given below. With this design, there is a Write Word Line (WWL) that is used to write the values of the Write Bit Line (WBL) and $\overline{WBL}$ into the cell, and a separate Read Word Line (RWL) that is used to read the contents of the cell on the Read Bit Line (RBL). Refer to any transistor by the label in the diagram (eg. PL).



(a) List the transistors that are involved in a Write operation in order of relative strength (from strongest to weakest), if there is any such ordering.

Same operation as a 6T SRAM cell: (AXL, AXR) stronger than (PL, PR).

(b) For the same cell, determine which transistors are involved in a Read operation, and list them in order of relative strength (from strongest to weakest), if there is any such ordering.

The read operation is done through N0 and N1 (no sizing constraints for stability).

(c) True or false: the 4 transistors in the cross-coupled inverters in this cell may all be made minimum size without worsening read stability.

True. The read stability is not affected by the sizing of the transistors in the cross-coupled pair because there is a separate read port. In a normal 6T SRAM, the pull down (PD) must be stronger than the access transistor/pass gate (PG) which must be stronger than the pull up (PU).

PD stronger than the PG is required for read stability, and PG stronger than PU is required for writeability. By not using any of these transistors for reads, this trade-off disappears. In this case, both the PD and PU can be minimum sized.

(d) True or false: the 4 transistors in the cross-coupled inverters in this cell may all be made minimum size without worsening writeability.

True. The cross-coupled inverter transistors may be made minimum size, but should still follow the relative sizing set out in the answer to part (a) (i.e. PU weaker than PG).

2 Physical Array Organization

You would like to instantiate an SRAM array that has 1024 entries of 8 bits. Assume an SRAM cell is $0.12\mu m$ high and $0.5\mu m$ wide (where the wordline is horizontal and the bitline is vertical). Assume wire capacitance of $0.2fF/\mu m$, and supply voltage of 0.9V.

(a) What are the dimensions of an array that has 1024 rows and 8 columns (assume that the cells directly abut)?

$1024 \cdot 0.12\mu m = 122.88\mu m$ by $8 \cdot 0.5\mu m = 4\mu m$

(b) If you build an array of 1024 rows and 8 columns, how much energy is used to drive the wordline?

$E_{wl} = C_{wl} \cdot V^2 = 8cells \cdot \frac{0.5\mu m}{cell} \cdot 0.2\frac{fF}{\mu m} \cdot (0.9V)^2 = 0.65fJ$ (one wordline turns on)

(c) If you build an array of 1024 rows and 8 columns, how much energy is discharged from the bitlines (assuming the wordline is left on for a long time)?

$E_{bl} = C_{bl} \cdot V^2 = 8columns \cdot 1024\frac{cells}{column} \cdot \frac{0.12\mu m}{cell} \cdot 0.2\frac{fF}{\mu m} \cdot (0.9V)^2 = 159fJ$ (all of the bitlines discharge)

(d) You can change the physical shape of an array by using bit-interleaving. For a 4 to 1 interleaved design, every 4th bit in a row belongs to a single word (the 0th, 4th, 8th, ... bits form entry 0, the 1st, 5th, 9th, ... bits form entry 1, the 2nd, 6th, 10th, .. bits form entry 2, and the 3rd, 7th, 11th, ... bits form entry 3 along a single row). If the 1024 entry x 8 bit word design is interleaved 4 to 1, how many rows and columns are there?

Now the memory has 1024/4=256 rows and 8*4=32columns.

(e) Assuming the same interleaving as part (d), which address bits are used to select the word?

For 1024 entries, there are 10 address bits total. The lower 2 bits are used to select the column.

(f) Assuming the same interleaving as part (d), which address bits are used for the column select mux?

The upper 8 bits are used to select the row. It is ok if the lower and upper are switched, i.e. upper 2 bits select the column and lower 8 bits select the row.

(g) Assuming the same interleaving, how much energy is used in the wordlines?

$E_{wl} = C_{wl} \cdot V^2 = 32cells \cdot \frac{0.5\mu m}{cell} \cdot 0.2\frac{fF}{\mu m} \cdot (0.9V)^2 = 2.5fJ$ (one wordline turns on)

(h) Assuming the same interleaving, how much energy is used in the bitlines?

$E_{bl} = C_{bl} \cdot V^2 = 32 columns \cdot 256 \frac{cells}{column} \cdot \frac{0.12 \mu m}{cell} \cdot 0.2 \frac{fF}{\mu m} \cdot (0.9V)^2 = 159 fJ$ (all of the bitlines discharge)

Note that the energy is almost the same, because each bitline has less capacitance, but more bitlines discharge by the same factor.

(i) (**EECS251A Only**) Suppose we want to design a row decoder for the reshaped array in part (d). Assume the input capacitance of each cell is $0.2fF$, and the decoder input capacitance is constrained to be $0.8fF$. Note that with the minimum possible transistor size in this technology, the C_{in} for an inverter is $0.1fF$. What is the total fanout for one bit of the decoder?

$C_{wl} = 32 cells \cdot (0.2 \frac{fF}{cell} + 0.5 \frac{\mu m}{cell} + 0.2 \frac{fF}{\mu m}) = 9.6 fF$

Since the design is symmetric (i.e. all input bits go through essentially the same logic), we will do the optimum sizing only for the A_0 address bit. A_0 only drives half of the rows, and the other half is driven by $\overline{A_0}$. So, the branching factor would be $B = 256/2 = 128$.

$F = B \cdot \frac{C_{wl}}{C_{in}} = 128 \cdot \frac{9.6fF}{0.8fF} = 1536$

(j) (**EECS251A Only**) What is the optimal number of stages to minimize the delay of the decoder for a given input bit?

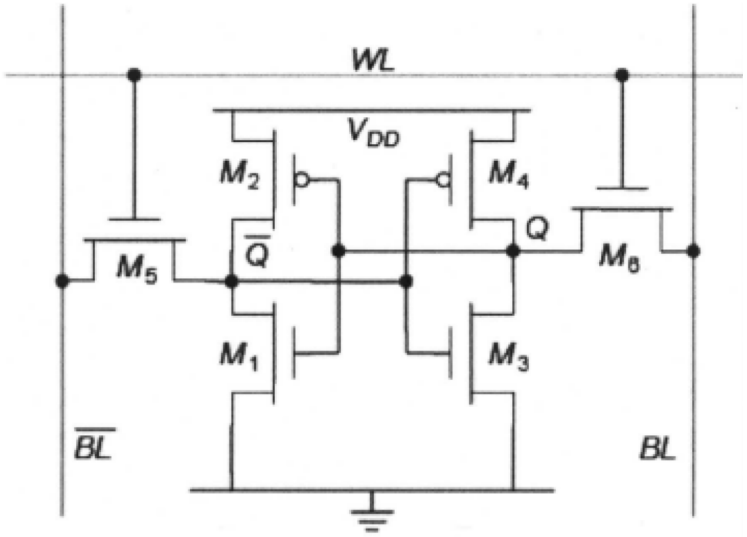
To approximately find the number of stages, we assume an effective fanout of 4:

$log_4(1536) = 5.3$ stages

We can then use 2-to-4 and 4-to-16 predecoders to generate all combinations of the address bits and use AND2 gates to drive each wordline. The sizing of these gates can be found as normal.

3 6T SRAM Cells

For the SRAM cell shown below, the widths of M1 and M3 are $240nm$, the widths of M2 and M4 are $120nm$, and the widths of M5 and M6 are $120nm$.



For this technology, you are given that $V_{DD} = 1V$ and $C_D = C_G = 2fF/\mu m$. The dimensions of the cell are $3\mu m$ x $3\mu m$ and the cell is part of a 256 x 256 memory array. Each bitline runs in Metal 2 with $0.12\mu m$ width and $C_{pp} = 7aF/\mu m^2$, $C_{fr} = 14aF/\mu m$. Bitlines are pre-charged to V_{DD} for read, and in order to speed up the read operation, they are connected to (ideal) differential sense amplifiers, which instantly evaluate the correct output once their input differential voltage is $500mV$.

(a) Looking at the whole memory block, calculate the read access time assuming $R_N = 1.5k\Omega{*}\mu m$. (Note: assume device capacitance on internal cell nodes is negligible)

Assuming the input capacitance of the sense amplifier and other peripheral circuits is negligible, the bit line capactiance is approximately:

$C_{BL} = 256W_{M5}C_D + C_{pp}W_{BL}(256 \cdot L_{cell}) + 2C_{fr}(256 \cdot L_{cell}) = 83.7fF$

From here, the read access time can be calculated:

$t_{ra} = ln2 \cdot (R_{M5} + R_{M1})C_{BL} = ln2 \cdot (\frac{1.5k\Omega{*}\mu m}{0.120\mu m} + \frac{1.5k\Omega{*}\mu m}{0.240\mu m}) \cdot 83.7fF = 1087.8ps \approx 1.1ns$

Note that we have used $ln2RC$ since the sense amp switching voltage happens to be $\frac{V_{sw}}{V_{DD}} = 0.5$.

(b) How much energy is consumed by the memory for every read/precharge operation?

In each cycle, 256 bitlines are discharged to $V_{DD} - \Delta V_{sense}$ and then charged up to V_{DD}, so:

$E = Q \cdot V_{DD} = (256 \cdot C_{BL} \cdot \Delta V_{sense}) \cdot V_{DD} = 10.7pJ$

(c) Assume that the supply of the cross-coupled pair in the cell is lowered to $V_{DD}/2$, while the bitline is still precharged to V_{DD}. True or false: the read margin becomes worse than in the original design.

True. The read margin is worse because the pull-down transistors are weaker.

(d) Assume the same operating conditions as in part (c). True or false: the write margin becomes worse than in the original design.

False. The write margin is better because the pull-up transistors are weaker.