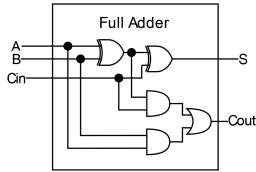# EECS 151/251A: Homework № 8

Due Friday, April 15th

Problem 1: Energy Adds Up!

You have been tasked with designing an 8 bit adder to use within an ASIC that needs to meet certain performance and power constraints.
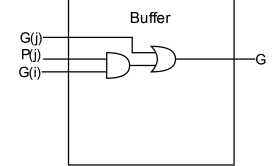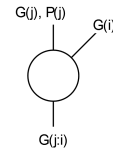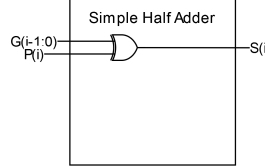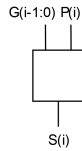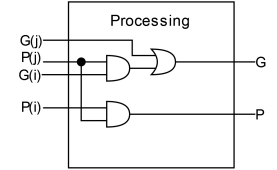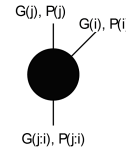
Part a)

Draw a block diagram for both an 8-bit ripple carry adder as well as an 8 bit radix-2 Kogge-Stone adder. Use the following blocks for the implementation of your designs:
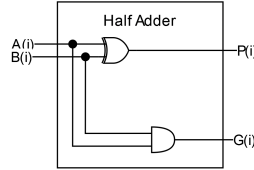
Part b)

At a voltage of 1.0V, you are given the following propagation delays:

$$t_{\mathrm{AND}} = 5\mathrm{ps}, \quad t_{\mathrm{OR}} = 4\mathrm{ps}, \quad t_{\mathrm{XOR}} = 7\mathrm{ps}$$

For each design in part a), derive the critical path and maximum clock frequency.

Part c)

You are given the following capacitance for each logic gate.

$$C_{\mathrm{AND}} = 2\mathrm{fF}, \quad C_{\mathrm{OR}} = 3\mathrm{fF}, \quad C_{\mathrm{XOR}} = 4\mathrm{fF}$$

i) Running at a voltage of 1.0V and assuming an activity factor of $\alpha = 0.2$ across both designs, what is the energy consumed for one add operation for each of the designs?

ii) Assuming both adders are operating at their maximum frequency and that they are processing one addition every cycle. What is the power consumption of each of the designs? Only consider dynamic power.

Part d)

You are tasked to find the design that can run at a clock frequency of 10GHz while minimizing power. You perform some simulations on your design and find that the propagation delay of all gates can be reduced to 2/3 of the original value by raising the operating voltage to 1.2V.

In order to minimize power consumption while meeting the 10GHz requirement, which design should you choose (ripple-carry or Kogge-Stone), and at what voltage should it operate (either 1.0V or 1.2V)?

Problem 2: Product Design

Part a)

i) Draw a block diagram for a parallel (array) multiplier that multiplies an 8-bit integer by a 2-bit integer. Assume you use the same full and half adders as in Problem 1.

ii) You are given that the propagation delays are the following:

$$t_{\text{AND}} = 5\text{ps}, \quad t_{\text{OR}} = 4\text{ps}, \quad t_{\text{XOR}} = 7\text{ps}$$

Draw the critical path of the design, and calculate the path delay.

Part b)

i) You are then tasked to design a 4x4 multiplier. Draw a block diagram for a Wallace-Tree multiplier, and highlight the critical path. Calculate the propagation delay for the design.

ii) You then discover that in your application, exactly one bit of the multiplicand is equal to 1. What kind of operation is this, and how would this simplify your multiplier design?

iii) Draw a block diagram for your design in part b), highlight the critical path, and calculate the propagation delay. Hint: the propagation delay for a 2-input multiplexer is given as

$$t_{\text{MUX}} = 6ps$$