LAB08 APAI:
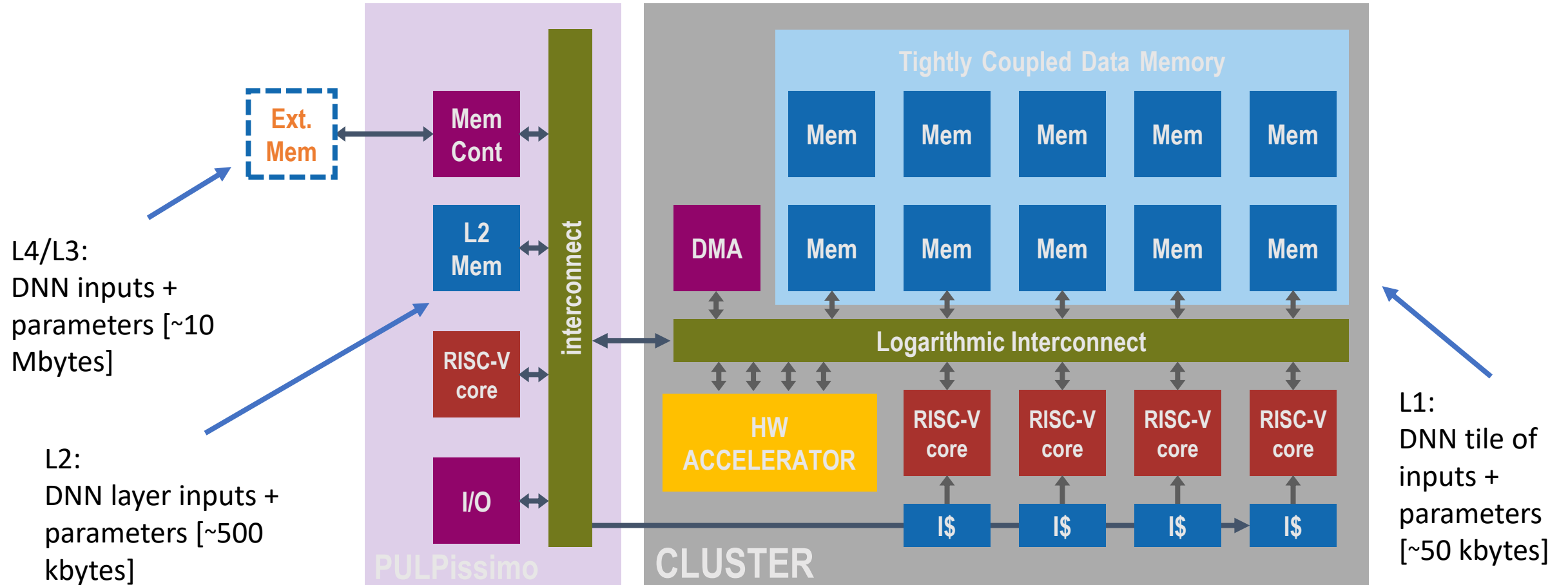# Tiling on PULP

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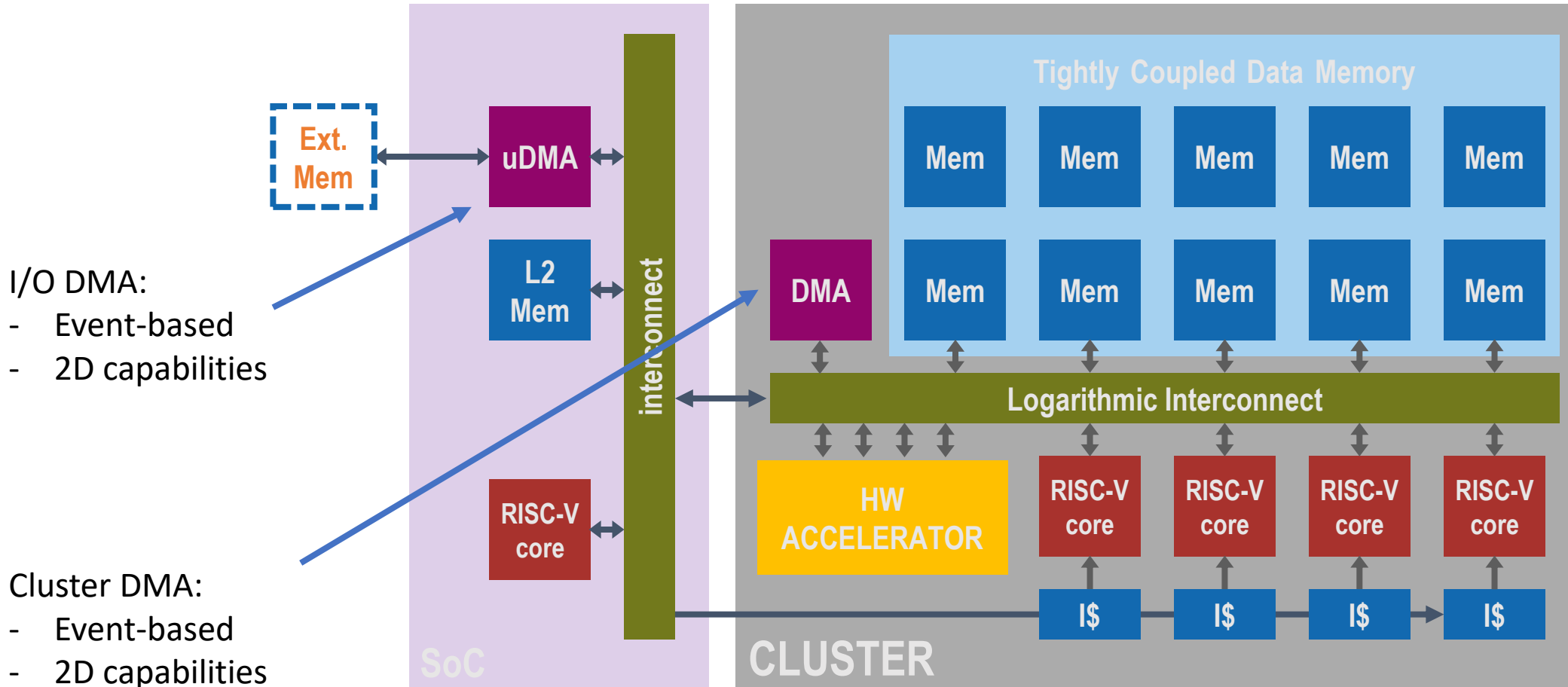
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PULP Architecture

L4/L3:
DNN inputs +
parameters [~10
Mbytes]

L2:
DNN layer inputs +
parameters [~500
kbytes]

L1:
DNN tile of
inputs +
parameters
[~50 kbytes]

Ext. Mem

Mem Cont

L2 Mem

RISC-V core

I/O

interconnect

PULPissimo

CLUSTER

DMA

Tightly Coupled Data Memory

Mem Mem Mem Mem Mem
Mem Mem Mem Mem Mem

Logarithmic Interconnect

HW ACCELERATOR

RISC-V core RISC-V core RISC-V core RISC-V core

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PULP Architecture

I/O DMA:
- Event-based
- 2D capabilities

Cluster DMA:
- Event-based
- 2D capabilities

PULP-SDK: GVSoC

- https://github.com/pulp-platform/pulp-sdk

- Includes a set of scripts to test DNN: Flasher
- Includes all the useful functions to efficiently program PULP: PMSIS APIs
- Includes all the useful functions to control external devices: PMSIS BSPs
- Includes PULP chips simulator: GVSoC

Assignment

- 3 hours together in LAB1
- 1 week to deliver all the requirements
- Open-chat on Teams for late questions

- Deadline: 23/12/2021 at 4 PM
- Usual ranking policy

- https://www.github.com/EEESlab/APAI-LAB08-Tiling-PULP