Electrical Characteristics ADS1299

specifications are at AVDD – AVSS = 5 V, DVDD = 3.3 V, V_{REF} = 4.5 V, external f_{CLK} = 2.048 MHz, data rate = 250 SPS, and gain = 12 (unless otherwise noted)

Gain = 12 , 55kHz

Register Bits: 6-4

GAINn[2:0] = 101

Register: CHnSET

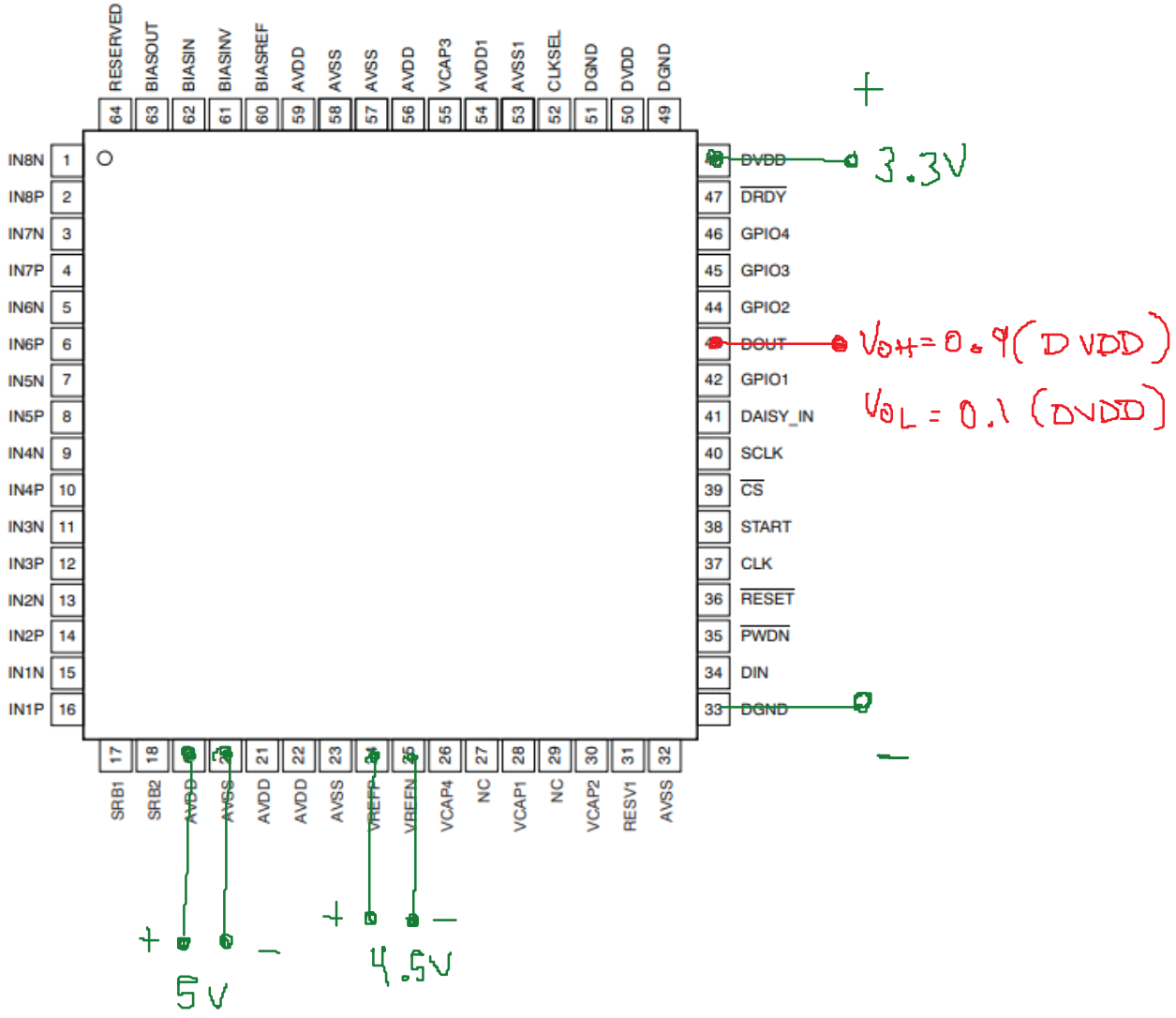
CHnSET → GAINn[2:0] = 101

Data rate: 250

CONFIG1 = 110

CONFIG1 → DR[2:0] = 110

PAG Package
64-Pin TQFP
Top View



TEST SIGNAL

Figure 51. CONFIG1: Configuration Register 1

01h CONFIG1 →

7	6	5	4	3	2	1	0
1	DAISY_EN	CLK_EN	1	0	DR[2:0]		
R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-6h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

6 $\overline{\text{DAISY\_EN}}$ = 0 (Daisy-chain mode)

5 CLK_EN = 0 (Oscillator clock output disable)

2:0 DR[2:0] = 110 (Data Rate 250 SPS)

02h CONFIG2 →

7	6	5	4	3	2	1	0
1	1	0	INT_CAL	0	CAL_AMP	CAL_FREQ[1:0]	
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

4 INT_CAL = 1 (T.S. Generated Internally)

2 CAL_AMP = 0 (T.S. Amplitude VREF/2.4)

1:00 CAL_FREQ[1:0] = 00 ($f_{clk}/2^{21}$)

03h CONFIG3 →

7	6	5	4	3	2	1	0
PD_REFBUF	1	1	BIAS_MEAS	BIASREF_INT	PD_BIAS	BIAS_LOFF_SENS	BIAS_STAT
R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7 $\overline{\text{PD\_REFBUF}}$ = 1 (Enable internal reference buffer)

4 BIAS_MEAS = 0 (Open)

3 BIASREF_INT = 0 (BIASREF fed externally)

2 $\overline{\text{PD\_BIAS}}$ = 0 (buffer is powered down)

04h LOFF →

7	6	5	4	3	2	1	0
COMP_TH[2:0]			0	ILEAD_OFF[1:0]		FLEAD_OFF[1:0]	
R/W-0h			R/W-0h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7:5 COMP_TH[2:0] = 0x00 (Lead off-comp threshold, P=95%, N=5%)

3:2 ILEAD_OFF[1:0] = 00 (LOFF current 6nA)

1:0 FLEAD_OFF[1:0] = 00 (DC lead-off detection)

05h to 0Ch CHnSET →

7	6	5	4	3	2	1	0
PDn	GAINn[2:0]			SRB2	MUXn[2:0]		
R/W-0h	R/W-6h			R/W-0h	R/W-0h		

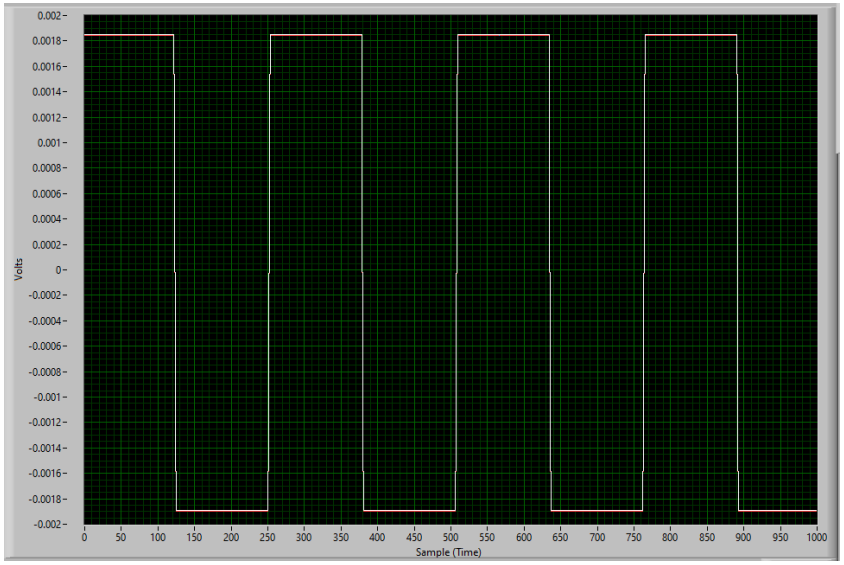
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

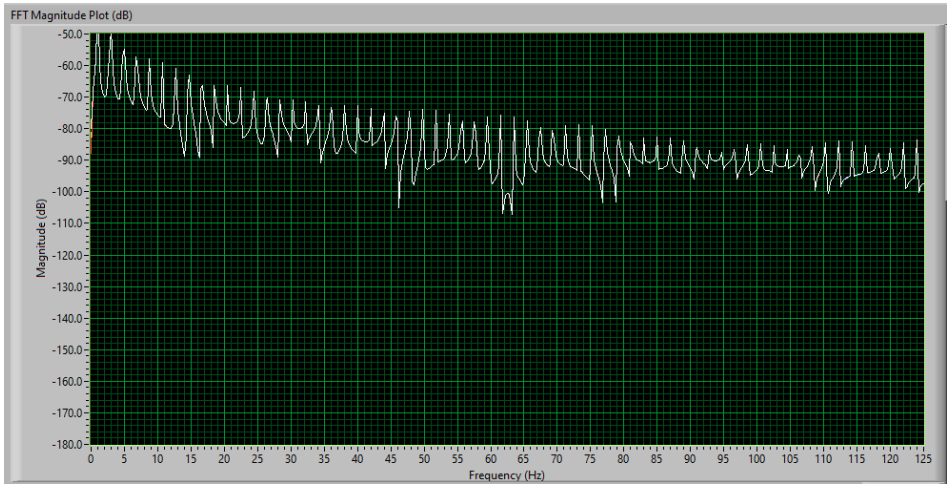
7 PDn = 0 (Normal Operation)

6:4 GAINn[2:0] = 110 (PGA gain 24)

3 SRB2 = 0 (Open/Off)

2:0 MUXn[2:0] = 101 (Test signal)





DEFAULTS CONNECTIONS (JP) by FE EVM Board