Digital Integrated Circuits

#Home Work 6 2025.05.15 (Due:05.23 13:20)

Reference to the class note: B4 Static SRAM and Shifter

1. Design an embedded SRAM contains 256 X12-bit words.

(a) Plan A: Draw the memory array architecture like that shown in Fig.12.2(a) of class note page 2. **Mark necearry inputs, outputs and signals** (20%)
(b) Plan B: If it is physically arranged in a square fashion like that shown in Fig.11.2 (b) with proper k address bits used in the column decoder, draw the memory architecture. Indicate the number of inputs to each column multiplexer. **Mark necearry inputs, outputs and signals (20%)**
(C) **List in table form** for Design A and B of the following items: (20%)
(i) The number of Worldline and the the number of memory cell in a Wordline,
(ii) The number of Bitline and the the number of memory cell in a Bitline
(D) Why Plan B is better than A? Compare from Area (the decoder size), Speed (Worldline and Bitline loading) and Power point of view. You shall describe the factors and facts (20%)
(E) Propose two designs of Plan B (i)precoding for row decoder and (ii) Hierarchical wordline). You shall describe the factor and facts that these two methods can reduce area and/or delay time. (20%)

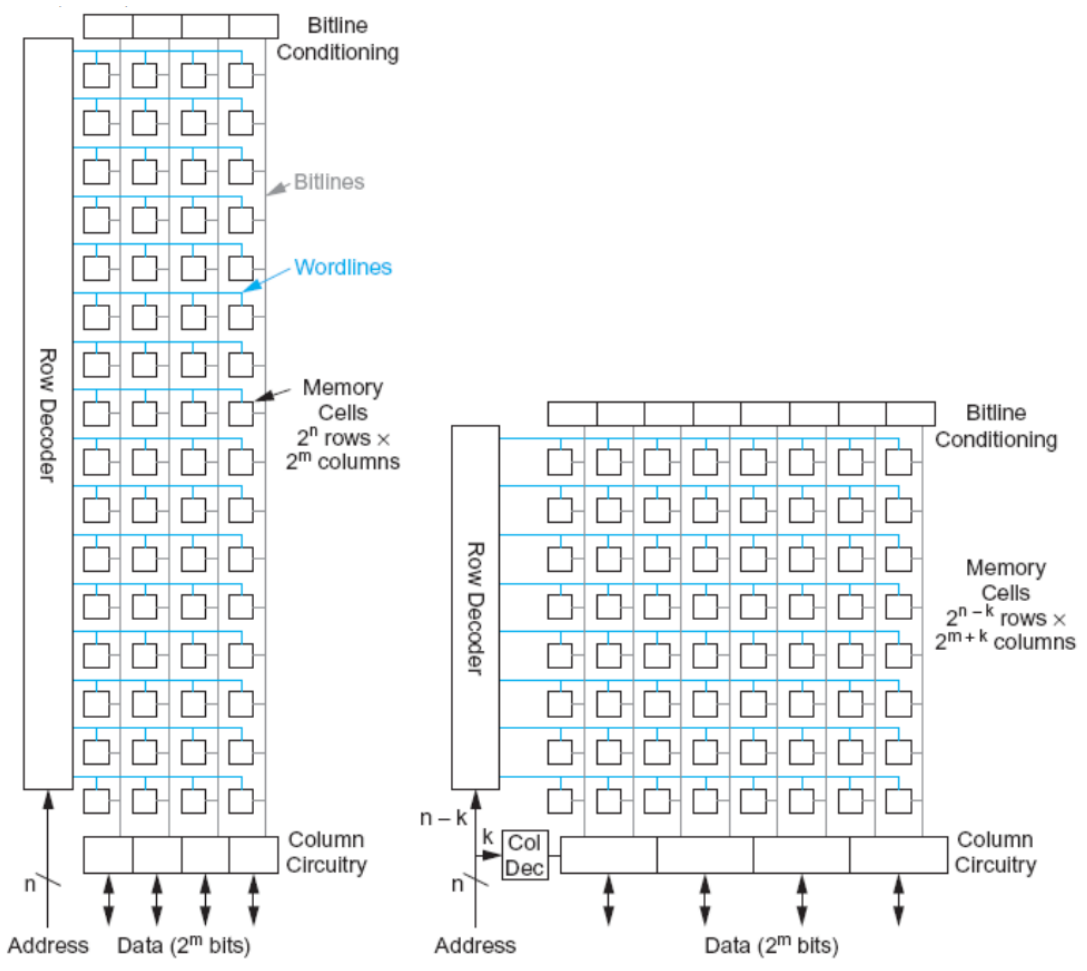

Fig.12.2 (a) and (b)