Digital Integrated Circuits

#Homework 2 2025.03.12 (Due: 03.21, 13:20)

1. (30%)
   (a) (20%) Draw the circuit schmetic of the attached layout. The signal name of each node shall be marked at the schematic. The area (26X45) shown in the figure is defined within the rectangular dash line.
   Hint : bit, bit-b and word are all input, Q is output.
   (b) (10%) Indicate the W/L ratio (X.Y) and AD/AS (in terms of λ) of each transistor.

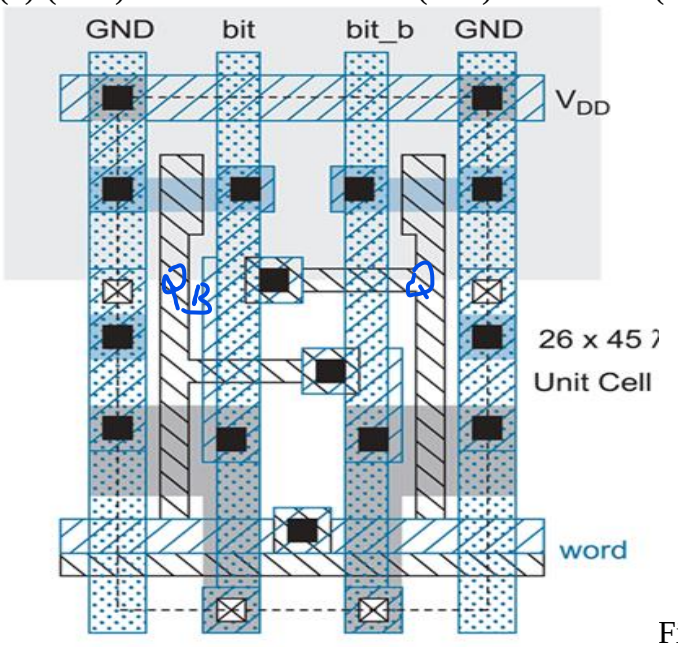

Fig.1

/* 32 nm CMOS devices with VDD= 1 V, Wmin=64nm, Lmin=32nm; using standard Vt */

2. Timing and power analysis(70%)

(a)(20%) Run SPICE to get the input and output capacitance of the circuit in Fig.1. Keep word as 1, Q initial as 1/0, simulate Bit input 0/1 respectively. (2 scenario)

You shall estimate reasonable AD, AS, PD and PS using the micro rule listed in the page 3-19 (Table 3.1) of the note with scale ratio (32/65). Explain the AD, AS, PD and PS used and list the result in Table form.

(b) (20%) With input signal like a pulse clock waveform with duration of 3ns (with tr=0.1ns and tf=0.1ns defined as 0%-100%), run spice (6ns) to get the tpdf, ptdr, tr, tf of the schmitt trigger in HW1.

(c) (30%) Do the timing and power analysis of a three-stage-Schmitt_trigger as a ring oscillator. Run Spice (4ns) to get the timing (tdf and tdr) and power waveform. Then list in table form with the clock period, tdf, tdr, tr, tf, average power, peak power and leakage power dissipation of the ring oscillator. Discuss why the tpdf, tpdr, tr, tf is different from that of part (b)