# Digital Integrated Circuits homework 8

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Consider the circuit in Fig.8. Modules A and B have a delay of 20 ns and 30 ns at 1.0 V ($V_{dd}$), and switch 20 pF and 35 pF ($C$) respectively. All the buses in Fig.8 are 16 bits. The register has a 0.4 ns delay and switches 0.05 pF. The clock rate of Fig.7 is thus 1/(50.4 ns) and the power dissipation is $P_0$. The power dissipation can be estimated by $P = C \cdot V_{dd}^2 \cdot F$ and the delay with respect to $V_{dd}$ can be approximated by $k/(V_{dd} - V_t)$ with $V_t$ equals 0.3 V. $k$ is a constant and is different for A and B. You can use the information of delay time, $V_{dd}$ and $V_t$ to calculate $k$.

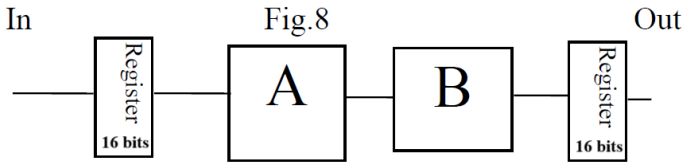



Fig.8

根據題目給的條件可以計算出：

$$t_A = \frac{k_A}{1.0\,V - 0.3\,V} = 20\,ns \implies k_A = 14 \times 10^{-9}\ (V \cdot s)$$

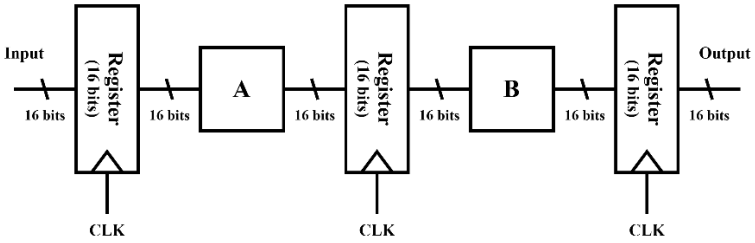
$$t_B = \frac{k_B}{1.0\,V - 0.3\,V} = 30\,ns \implies k_B = 21 \times 10^{-9}\ (V \cdot s)$$

$$P_0 = (20\,pF + 35\,pF + 2 \cdot 16 \cdot 0.05\,pF) \times (1.0\,V)^2 \times \left(\frac{1}{50.4\,ns}\right)$$

$$= (56.6 \cdot 10^{-12}) \times (1) \times (1.9841 \cdot 10^{7}) = 1.123 \times 10^{-3}\,W$$

(a) Adding a pipeline register between A and B allows for reduction of the supply voltage (A and B can use different $V_{dd}$) while maintaining throughput ($P_1$). Show the block diagram, explain the operation and calculate the power reduction ratio, $P_1/P_0$.

- **Block diagram**:




- **Explain the operation**:

為了達到 Low power design 的目的，我們可以透過下降提供給 A, B module 的 Power supply ($V_{dd}$) 來達成，但由於下降 $V_{dd}$ 會使電路的充放電

速度都變慢，因此在此小題的設計中是藉由 Pipeline 的方式，來讓 A, B module 都擁有完整的一個 Cycle time (= 50.4 ns)可以運算，一旦運算完成所需的時間變長了，就可以下降 $V_{dd}$ 了。

假設 Pipeline registers 的 $V_{dd}$ 不變(則 $t_{reg} = t_{pcq} = 0.4$ ns 也不變)，要符合的 Timing constraint (設 $t_{setup}$ 為 0)為：

$$t_A, t_B \leq T_{cycle} - t_{pcq} = 50\ ns$$

接著由題目提供的估算式可以推算出適合的 $V_{dd}$：

$$t_A = \frac{14 \times 10^{-9}}{V_{dd,A} - 0.3} \leq 50 \times 10^{-9} \implies \text{Let } V_{dd,A} = 0.58\ (V)$$

$$t_B = \frac{21 \times 10^{-9}}{V_{dd,B} - 0.3} \leq 50 \times 10^{-9} \implies \text{Let } V_{dd,B} = 0.72\ (V)$$

- **Calculate the power reduction ratio**:

計算 Pipeline 後的 Power dissipation:

$$\begin{aligned} P_1 &= P_A + P_B + 3 \cdot P_{reg} \\ &= 1.3349 \times 10^{-4} + 3.6 \times 10^{-4} + 4.7619 \times 10^{-5} \\ &= 5.411 \times 10^{-4}\ W \end{aligned}$$

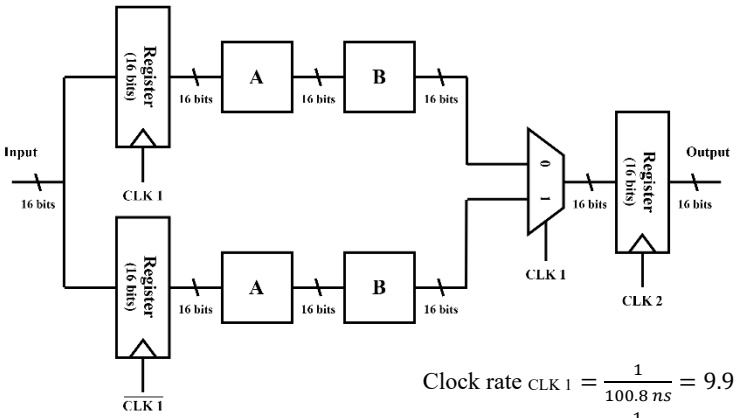
與原先的 Power dissipation 相比計算 Ratio:

$$\frac{P_1}{P_0} = \frac{5.411 \times 10^{-4}}{1.123 \times 10^{-3}} = 48.18\%$$

(節省了 $1 - 48.18\% = 51.82\%$)

(b) Assume that a 2-to-1 multiplexer has a delay of 0.4 ns at 1.0 V and switches 0.05 pF. Try parallel version with two copies (using two A and B modules) while maintaining data rate ($P_2$). Show the block diagram, explain the operation and calculate power reduction ratio, $P_2/P_0$.

- **Block diagram**:




Clock rate $_{\text{CLK 1}} = \frac{1}{100.8\ ns} = 9.920 MHz$

Clock rate $_{\text{CLK 2}} = \frac{1}{50.4\ ns} = 19.841 MHz$

- **Explain the operation**:

用 Parallel 的方式來做 Low power design 是透過降低 Clock rate 來讓 F 變小，同時因為 F 的降低使 Timing slack 變大，就可以跟(a)小題一樣再降低 Power supply ($V_{dd}$)來達到降低功耗的效果。

將同樣的電路複製為兩組並將(CLK 1) Clock rate 降低為一半，假設 CLK 1 與 CLK 2 對齊在一開始一起 Positive trigger，則接下來上面一組的電路是在 CLK1 positive trigger 後(到下下次的 CLK 2 positive trigger 之間, 即下一次 CLK 1 positive trigger 期間內)進行運算，而下面一組的電路則是在 CLK 1 negative trigger 後(到下一次 CLK 1 negative trigger 期間內)進行運算，再經由 MUX 來選擇要輸出的訊號是來自哪一組硬體即可，這樣就可以在 Clock rate 降低的情況下維持跟原本一樣的 Throughput。

因此電路要符合的 Timing constraint (設 $t_{setup} = 0$)為：

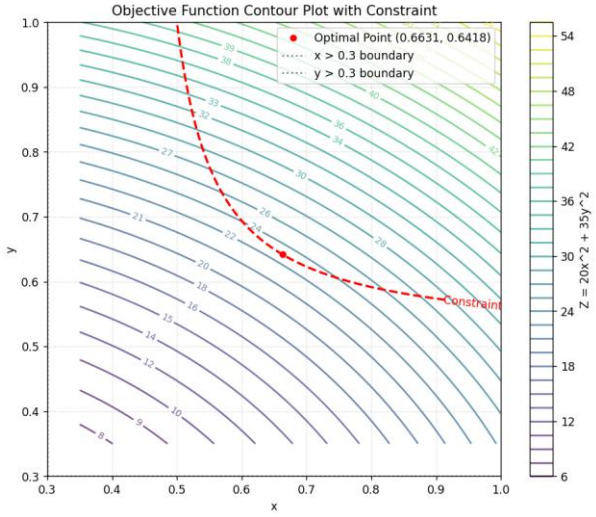
$$t_A + t_B \leq T_{cycle\,1} - t_{pcq} - t_{MUX} = 100\,ns$$

接續，由於提供給 Pipeline registers 與 MUX 的 $V_{dd}$ 都確定為 1.0V 不會再進行優化，因此考量從 A, B modules 的 Power dissipation 進行優化。此題並沒有規定 A, B modules 的 $V_{dd}$ 要一致，假設它們可以自由設置，則我們可以寫出的最佳化函數與限制條件式寫為：

$$\begin{cases} \text{minimize } P_A + P_B \;\propto\; 20 \cdot V_{dd,A}^2 + 35 \cdot V_{dd,B}^2 \\ \text{subject to } \dfrac{14 \times 10^{-9}}{V_{dd,A} - 0.3} + \dfrac{21 \times 10^{-9}}{V_{dd,B} - 0.3} \leq 100 \times 10^{-9}, \quad V_{dd,A} > 0.3, \quad V_{dd,B} > 0.3 \end{cases}$$

接著我使用 Python 搭配 scipy 套件以程式求解，算得最佳解為：

$$V_{dd,A} = 0.6631\,(V), \qquad V_{dd,B} = 0.6418\,(V)$$



- **Calculate the power reduction ratio**:

  計算 Power dissipation:

$$P_2 = \left[2 \cdot \left(P_A + P_B + P_{reg}\right) + P_{MUX}\right]_{@F=9.920MHz} + \left[P_{reg}\right]_{@F=19.841MHz}$$
$$= 4.8434 \times 10^{-4} + 1.5873 \times 10^{-5}$$
$$= 5.002 \times 10^{-4}\ W$$

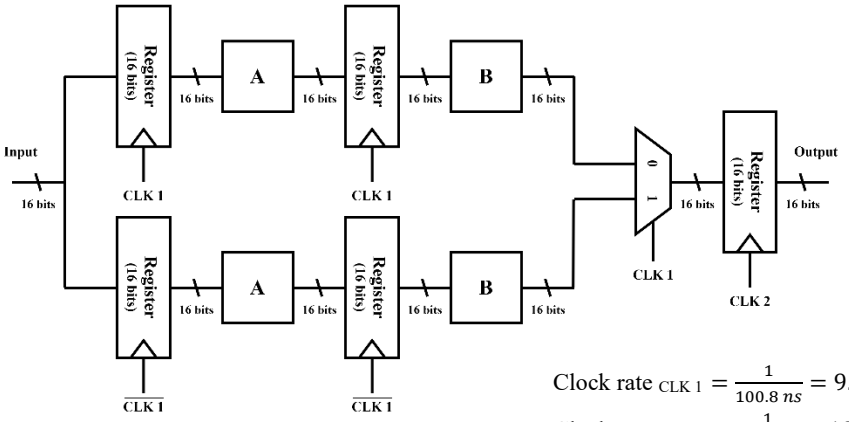
  與原先的 Power dissipation 相比計算 Ratio:

$$\frac{P_2}{P_0} = \frac{5.002 \times 10^{-4}}{1.123 \times 10^{-3}} = 44.54\%$$

  (節省了 $1 - 44.54\% = 55.46\%$)

(c) Try to combine (a) and (b) to design a parallel-pipeline version while maintaining data rate ($P_3$). Show the block diagram, explain the operation and calculate power reduction ratio, $P_3/P_0$.

- **Block diagram**:




Clock rate $_{\text{CLK 1}} = \frac{1}{100.8\ ns} = 9.920MHz$

Clock rate $_{\text{CLK 2}} = \frac{1}{50.4\ ns} = 19.841MHz$

- **Explain the operation**:

  此設計結合(a)小題的 Pipeline 方法與(b)小題的 Parallel 方法來更進一步的給予較大的 Timing slack，使得充放電速度相較於(b)的設計可以再更慢一些，$V_{dd}$ 也就可以再下降更多以節省功耗。

  在此小題中，要符合的 Timing constraints (設 $t_{setup} = 0$)為：

$$t_A \leq T_{cycle\,1} - t_{pcq} = 100.4\ ns$$

$$t_B \leq T_{cycle\,1} - t_{pcq} - t_{MUX} = 100\ ns$$

  接著由題目提供的估算式可以推算出適合的 $V_{dd}$：

$$t_A = \frac{14 \times 10^{-9}}{V_{dd,A} - 0.3} \leq 100.4 \times 10^{-9} \implies \text{Let } V_{dd,A} = 0.4394 \ (V)$$

$$t_B = \frac{21 \times 10^{-9}}{V_{dd,B} - 0.3} \leq 100 \times 10^{-9} \implies \text{Let } V_{dd,B} = 0.51 \ (V)$$

- **<u>Calculate the power reduction ratio</u>**:

  計算 Power dissipation:

$$P_2 = \left[2 \cdot \left(P_A + P_B + 2 \cdot P_{reg}\right) + P_{MUX}\right]_{@F=9.920MHz} + \left[P_{reg}\right]_{@F=19.841MHz}$$

$$= 2.9692 \times 10^{-4} + 1.5873 \times 10^{-5}$$

$$= 3.128 \times 10^{-4} \ W$$

  與原先的 Power dissipation 相比計算 Ratio:

$$\frac{P_3}{P_0} = \frac{3.128 \times 10^{-4}}{1.123 \times 10^{-3}} = 27.85\%$$

  (節省了 $1 - 27.85\% = 72.15\%$)