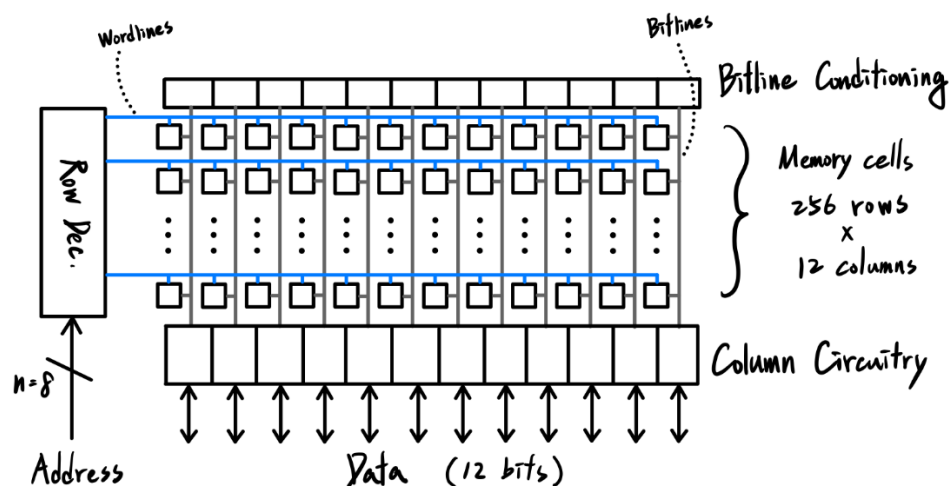# Digital Integrated Circuits homework 6 電子所 陳柏翔 313510156

**1.** Design an embedded SRAM contains **256 x 12-bit** words.

(a) **Plan A**: Draw the memory array architecture like that shown in Fig.12.2(a) of class note page 2. Mark necessary inputs, outputs and signals.

(b) **Plan B**: If it is physically arranged in a square fashion like that shown in Fig.11.2 (b) with proper k address bits used in the column decoder, draw the memory architecture. Indicate the number of inputs to each column multiplexer. Mark necessary inputs, outputs and signals.

先找出最接近正方形分布的 rows × columns：
- Rows: $\log_2 \sqrt{256 \times 12} = 5.7925 \approx 6$ → 設 Number of rows $= 2^6 = 64$
- Columns: $256 \times 12 \div 64 = 48$ → 設 Number of columns $= 48$
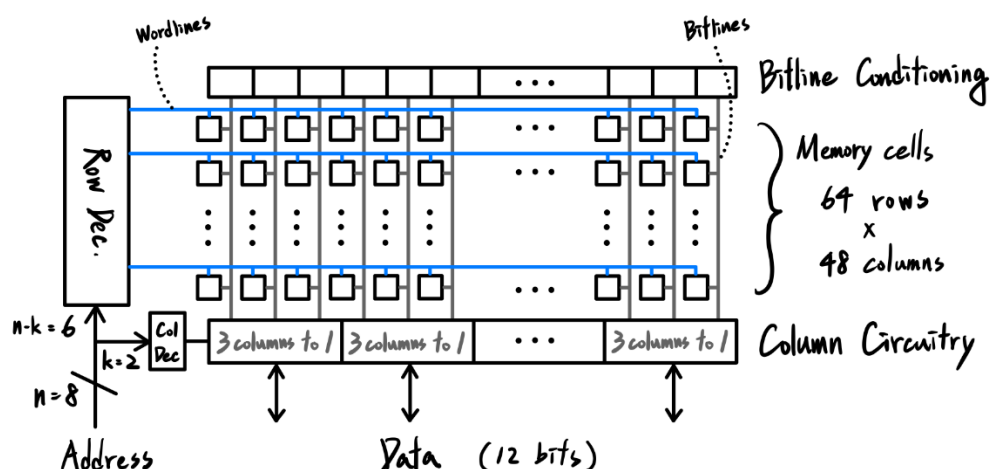
(c) List in table form for Design A and B of the following items:

   (i)   The number of Wordline and the number of memory cell in a Wordline.

   (ii) The number of Bitline and the the number of memory cell in a Bitline.

Table of (i)	Plan A	Plan B
Wordline	256	64
Memory cells	12	48

Table of (ii)	Plan A	Plan B
Bitline	12	48
Memory cells	256	64

(d) Why Plan B is better than A? Compare from Area (the decoder size), Speed (Worldline and Bitline loading) and Power point of view. You shall describe the factors and facts.

1. **Area (Decoder size)**:
   - Plan A: row decoder 需要 8 × Inverters / 256 × 8-input AND Gate.
   - Plan B: row decoder 需要 6 × Inverters / 64 × 6-input AND Gate,
       column decoder 需要 2 × Inverters / 3 × 2-input AND Gate.
   ⟹ Plan B所需的Gate數量與面積都遠小於Plan A。

2. **Speed**:

	Plan A	Plan B
Wordline loading	12	48
Bitline loading	256	64

   - Wordline loading: Plan A ＜ Plan B　(Plan A好一些)
   - Bitline loading: Plan A ≫ Plan B　(Plan B好很多)
   ⟹ 對於Critical path而言，Plan A需走256個memory cells (loading較大)，遠大於Plan B的64個memory cells。

3. **Power**: $P = fCV^2 \propto C$
   - Decoder power: Plan A所需Gate數遠大於Plan B，因此Dynamic power會較大。
   - Wordline power: Plan A的Wordline loading較Plan B來得小，因此Dynamic power會較小。
   - Bitline power: Plan A的Bitline loading較Plan B大很多，因此Dynamic power會較大。

   總結：在Area與Speed方面都是Plan B較佳，而Power方面除了Wordline loading的面向上Plan A會較佳，其他都是Plan B較佳，因此整體而言Plan B是較好的設計。

(e) Propose two designs of **Plan B** (i) **precoding for row decoder** and (ii) **Hierarchical wordline**. You shall describe the factor and facts that these two methods can reduce area and/or delay time.

(i) **Precoding**:
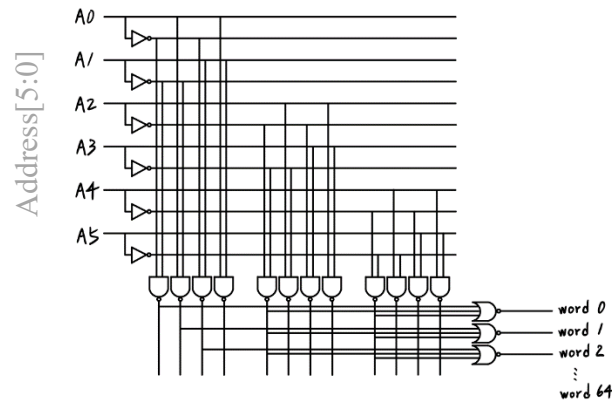
透過Precoding，可以利用邏輯共用的方式，省去大部分繁冗的NAND gates以有效reduce area。同上課講義所述，由於路徑上與原先的設計一樣需要經過INV-NAND-NOR或者NAND-NOR，因此path effort不改變，而此設計優化的重點不在速度上。

(ii) **Hierarchical wordline**:
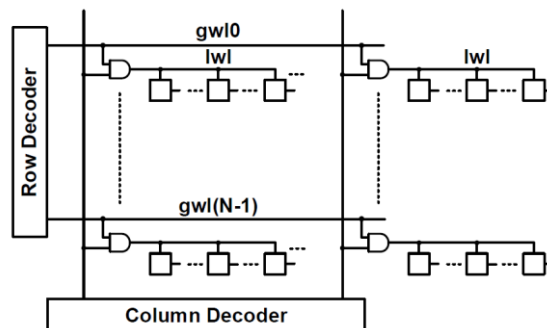
在Hierarchical wordline的方法中，將wordline分成global wordline(gwl)與local wordline(lwl)，因為這樣的做法取代了原先直接看到的大量memory cells，而是只在global層只看到AND gate的輸入端loading、在local層看到少量的memory cells的loading，因此能讓整體速度提升(降低看到的電容以減少充放電所需時間)。並且由於只有被local wordline啟動的bitlines才會動作，所以功耗也能有效下降。