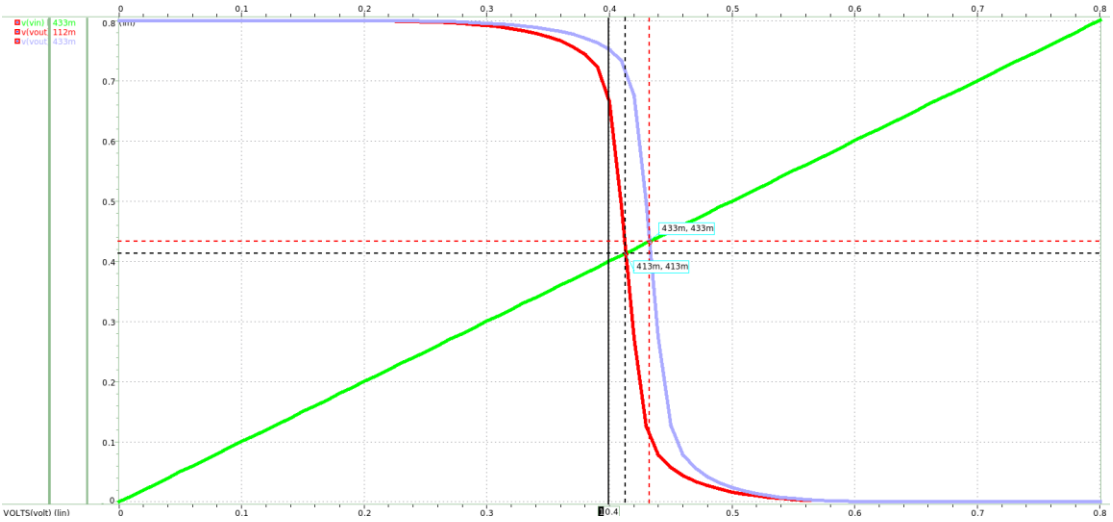
Digital Integrated Circuits homework 3 陳柏翔 313510156

1. Inverter and Ring oscillator (50%)

(a) Inverter (20%)

Keep a unit size inverter with NMOS n=1 and choose the n of PMOS for n=1 and 2. Run SPICE to show the logic threshold voltage. Verify and discuss your results by showing simulated waveforms.



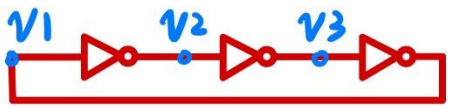
上圖為實驗結果，首先將NMOS的nfin個數固定設置為 1 ，將PMOS的nfin設置為 1 的話會得到左曲線(紅色線)、而將PMOS的nfin設置為 2 的話會得到右曲線(藍色線)，測量結果如下：

NMOS Fin n	PMOS Fin n	Logic Threshold
1	1	0.413 V
1	2	0.433 V

由以上實驗結果可以發現，如果PMOS設置得較寬(較多fins)會使從V_{DD}留下來的電流較大，使得Logic Threshold較高；而當N/PMOS的nfin皆設置為 1 的話Logic Threshold較接近$0.5V_{DD}$，同時nfin較少也意味著面積較小，根據這樣的結果及理由，我接下來選擇將N/PMOS的nfin皆設置為 1 。

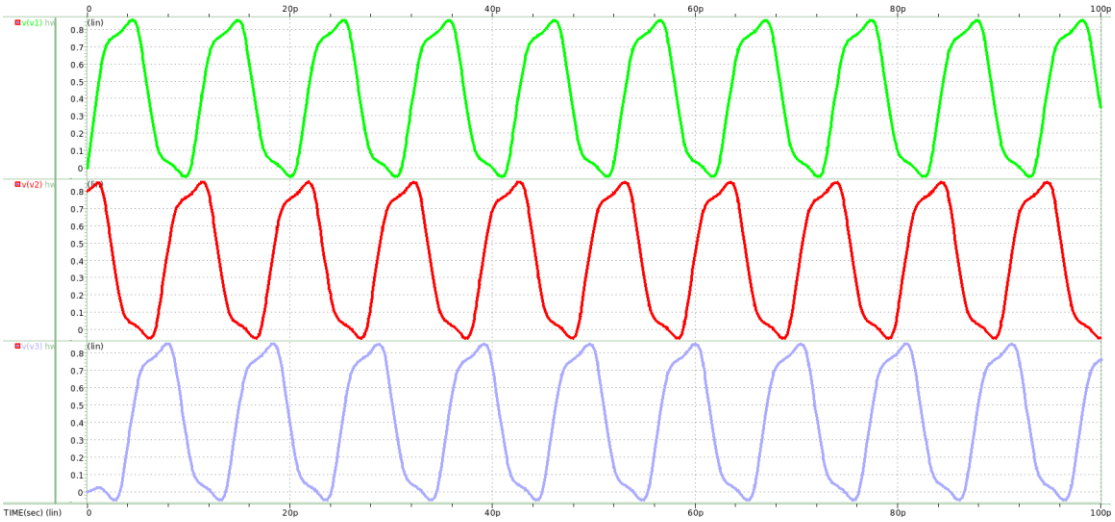
(b) Ring oscillator (30%)

According to the results of 1(a), design a 3-stage inverter-based ring oscillator with unit size inverter of a better logic threshold voltage. Set the initial voltage of each node so that it can oscillate. Show in table form, the SPICE simulation results of oscillation frequency and power consumption.

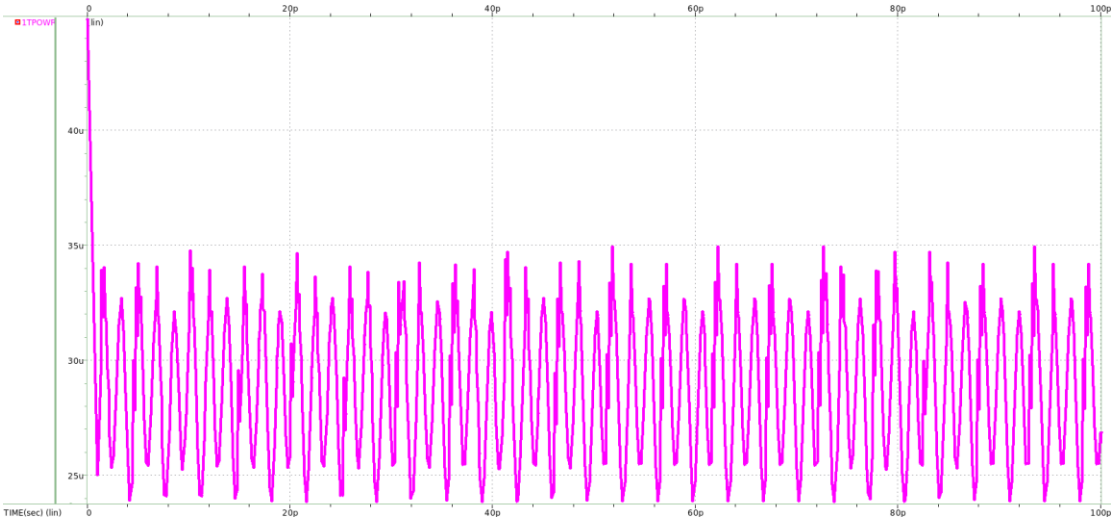


按題目要求根據1(a)的結果，能得到較好的logic threshold的N/PMOS之nfin比例為 1: 1。且由於題目沒有要求oscillator有更高的震盪頻率或其他要求，所以我的設計就將N/PMOS的nfin皆設置為 1，這樣能具有較小的面積，且擁有較好的logic threshold。下方為Transient模擬100ps的結果：

Voltage (3 nodes) waveform:



Power waveform:



Oscillation frequency and power consumption:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
  avg_power=  29.2002u  from=   5.0000p     to= 100.0000p
 peak_power=  34.9413u    at=  37.9528p    from=   5.0000p    to= 100.0000p
clk_period1=  10.4197p  targ=  21.7090p   trig=  11.2893p
clk_period2=  10.4149p  targ=  28.6508p   trig=  18.2359p
clk_period3=  10.4144p  targ=  25.1791p   trig=  14.7646p
  clk_freq1=  95.9720g
  clk_freq2=  96.0164g
  clk_freq3=  96.0206g

        ***** job concluded
```

```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:v1      =   9.9124f 0:v2      = 799.9995m 0:v3      = 762.4462n
+0:v4      = 799.9996m 0:vdd     = 800.0000m 0:vss     =   0.

**** voltage sources

subckt
element  0:vgnd     0:vvdd
 volts      0.      800.0000m
 current  440.5955p -441.5868p
 power      0.      353.2694p

    total voltage source power dissipation=  353.2694p      watts
```

```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:v1      = 800.0000m 0:v2      = 762.4351n 0:v3      = 799.9995m
+0:v4      = 758.9958n 0:vdd     = 800.0000m 0:vss     =   0.

**** voltage sources

subckt
element  0:vgnd     0:vvdd
 volts      0.      800.0000m
 current  551.6713p -546.1750p
 power      0.      436.9400p

    total voltage source power dissipation=  436.9400p      watts
```

Average Power	Peak Power	Leakage Power ($v_1 = 0$)	Leakage Power ($v_1 = V_{DD}$)
29.20 μW	34.94 μW	353.27 pW	436.94 pW

Oscillation Frequency (node v1)	Oscillation Frequency (node v2)	Oscillation Frequency (node v3)
95.97 GHz	96.02 GHz	96.02 GHz

以上結果中所測量的震盪頻率以及功耗分析，都按照與Homework 2相同的方式進行測量。同樣的，在模擬的最開始(t=0.)電壓會有一個非常高的Peak，我認為是數值計算上的問題不應該考慮進來，因此我在測量Power的時候是從5 ps以後開始測量。

此外，跟Homework 2的Ring Oscillator進行比較的話，可以發現震盪的週期快了約 9 倍、功耗縮小約 5 倍，較先進的製程整體都有明顯較好的結果。

2. Design a static **D register** as shown in Fig.1 with propose size of NMOS and PMOS to have better **t_{setup}, t_{pcq}, ~~t_{pdq}~~**(此項不用測) and **t_{hold}** time. The loading of Q and Q- have **2 unit size inverters** as loading. Both D and CLK has **rise time and fall time of 0.1ns** (0V-0.8V). (50%)

(a) Explain your sizing principle of each MOS to have least **t_{setup}, t_{pcq}, ~~t_{pdq}~~**(此項不用測) and **t_{hold}** time for register 1 and 0.

(b) Run SPICE to verify your results and list the results in table form for part (b).

在此題當中，