Digital Integrated Circuits

#Homework 1 2025.03.05 (Due:03.14 13:20; in the class)

/* Using 32 nm CMOS devices with VDD= 1 V, Wmin=64 nm, Lmin=32nm with resolution of 1nm; there are three kinds of Vt: High Vt, medium Vt and low Vt CMOS*/

(1) Design a CMOS Schmitt trigger shown at Fig.1 using medium Vt such that Vout=0.5 VDD when V^+ = 0.46-0.49 VDD, V^- = 0.44~0.41VDD and both rising and falling △V are the same. Fig.2(VDD=VCC) proposes an extra bias voltage VB and extra transistors P4 and N4 to control the two threshold voltages VL and VH .

a) Give the W/L of each device and V^+ , V^- (**in table form**) of the circuits at Fig.1/Fig.2. Discuss your design procedures to determine the size of each transistor. (60%)

b) Run SPICE to verify your results. Your report must have the figures of VTC and Isc (current from Vdd to GND) vs Vin (40%)

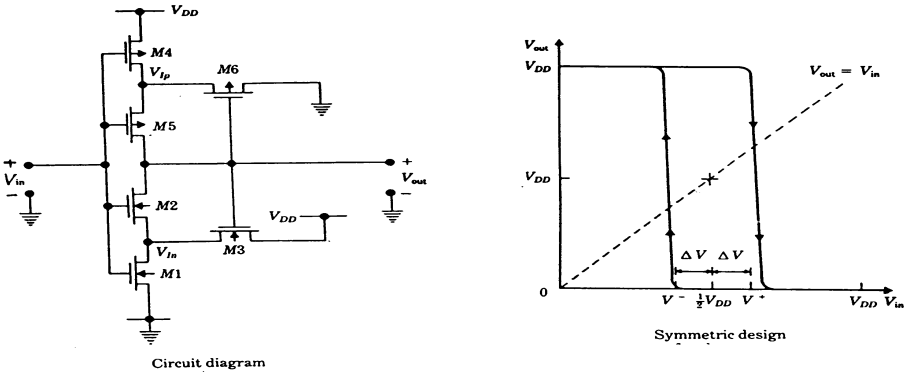

Fig.1 Schmitt Trigger circuit I

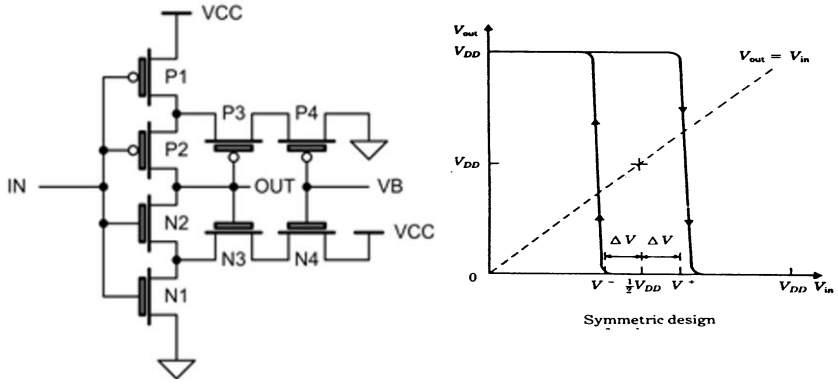

Fig.2 Schmitt Trigger circuit II