Digital Integrated Circuits

#Home Work 5 2025.05.02 (Due:05.09 13:20)

Reference to the class note: Chapter 3 Two-Operand Adder/Subtractor, Chapter 4 Multioperand adder

1. Design a 20-bit 2's complement multioperand adder (A+B+C+D) using Carry-Save Adder + Carry skip adder. To further optimize the delay, each module can have different size. **The goal is to have minimum critical path delay time with the least gate count. Assum there is no overflow during the additions. The internal word length of each module is 20 bits** (50)

(a) Show your block diagram like that shown in Fig.1. The CPA in Fig.1 shall be the carry skip adder with variable group size (Fig.2). Indicate the critical path. Expalin your design concept (20)

(b) For each block, you shall show its logic design diagram. Indicate the critical path. Explain your design concepts (20).

(c) Calculate the critical path delay in terms of the sum of 1-bit FA, 1-bit PG, Mux2, Valency-2 cells and XOR2 delay, etc..(10)

(d) Indicate the overall module used in terms of the number of 1-bit FA, 1-bit PG, Mux2, Valency-2 cells and XOR2. (10)

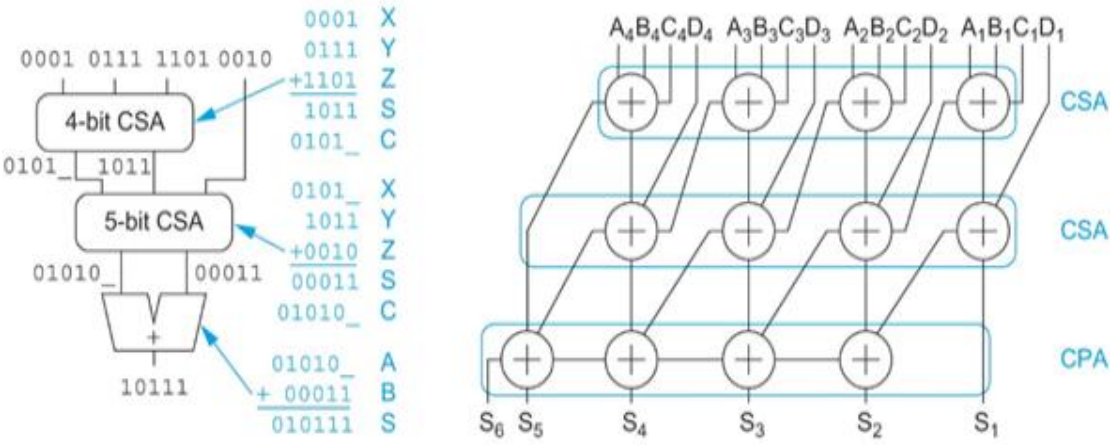

Fig.1

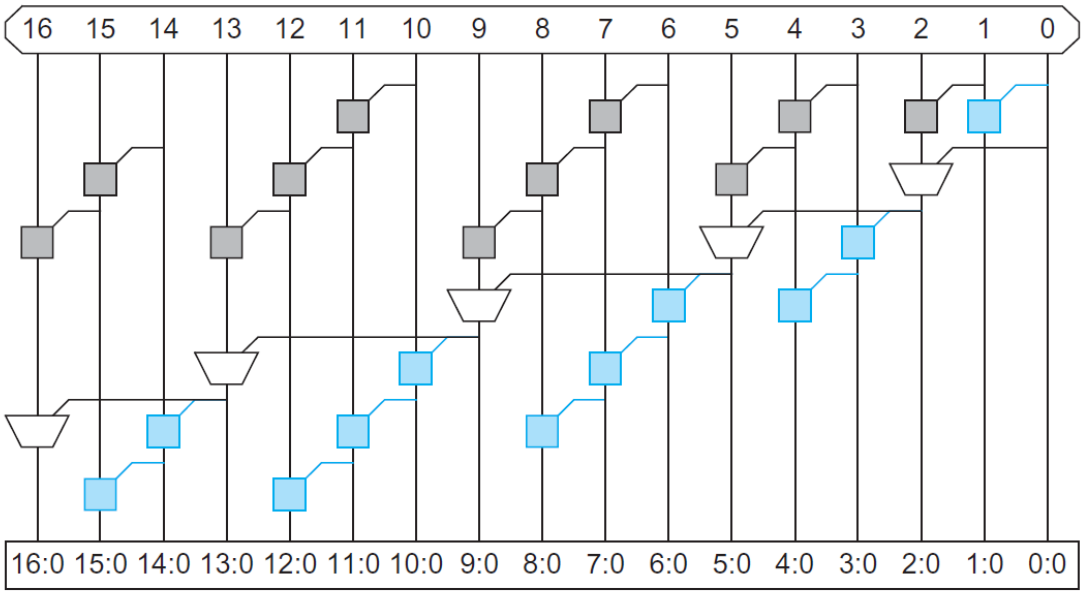

FIGURE 11.19 Variable group size carry-skip adder PG network

Fig.2

2. Pipeling design of 1 (40)

(a) Show the block diagram of the design with three pipelining stages (with DFFs) within the mutioperand adder. (20)

(b) List the number of DFF used. (10)

(c) List the clock cycle time of this pipeling design with tpd of the module used in the critical path (10)

$$t_{pd} \leq T_c - \underbrace{\left(t_{\text{setup}} + t_{pcq}\right)}_{\text{sequencing overhead}}$$