Digital Integrated Circuits homework 7

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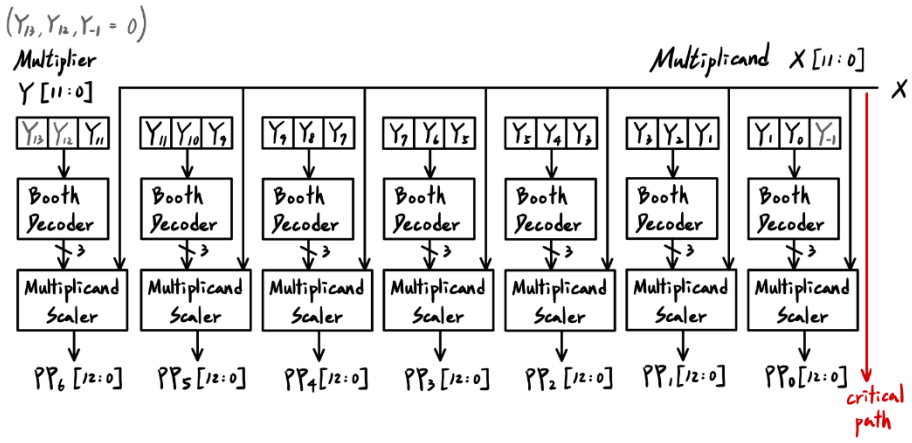
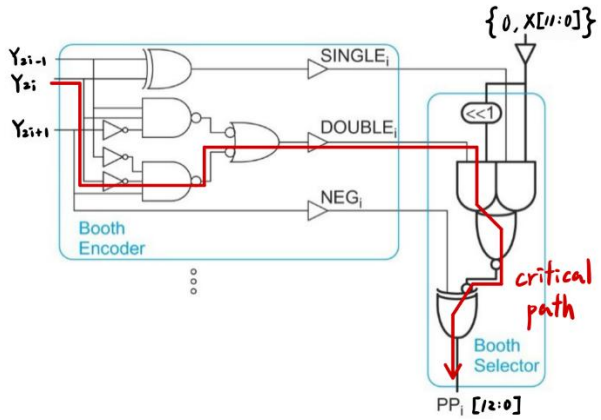
1. Design a 12-bit unsigned multiplier (X: 12 bits, Y: 12 bits, P: 24 bits) $P = X \times Y$ by using Radix-4 Booth multipliers. The goal is to have minimum critical path delay time with the least gate count.

(1) Show your block diagram as shown in Fig.1 below (example for the case of 8-bit; booth decoder and Multiplicand scale corresponding to Booth Encoder and Booth selector of Fig.10.80). For each block, you shall show its logic design diagram. Indicate the critical path. Explain your design concepts.

- **Block diagram (& Critical path)**:



- **Logic design for each block (& Critical path)**:



Booth Encoder (Left) & **Booth Selector** (Right)

(此作業中的 **Booth Decoder** block) (此作業中的 **Multiplicand Scaler** block)

- **Design concepts**:

如同課程中所學的 Radix-4 Booth multiplier 的操作原理，將 Y 向前與向後各看一個 Bit，組成為 $(Y_{2i+1}, Y_{2i}, Y_{2i-1})$ 並從 $i = 0, 1, 2, \ldots$ 開始掃描，

此外還需要補上 0，也就是設 $Y_{13}, Y_{12}, Y_{-1} = 0$，當掃完所有的三個 Bits 群組後，放入 Booth Decoder 產生 SINGLE_i, DOUBLE_i, NEG_i，再和 X 經過 Multiplicand Scaler 產生 $-2X, -X, 0, X, 2X$ 五種情形(如下 Table)，可以讓 CSA array 的層數大幅降低，達到高的運算速度：

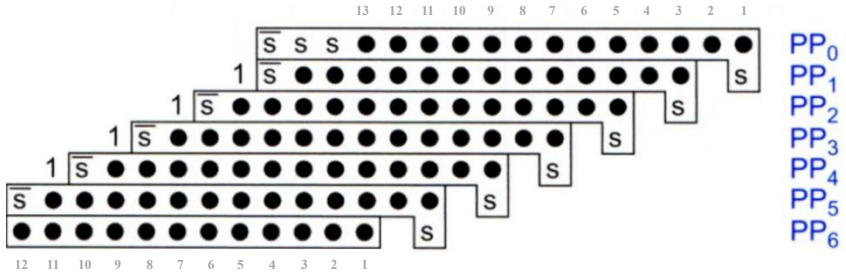
Y_{2i+1}	Y_{2i}	Y_{2i-1}	PP_i	SINGLE_i	DOUBLE_i	NEG_i
0	0	0	0	0	0	0
0	0	1	+X	1	0	0
0	1	0	+X	1	0	0
0	1	1	+2X	0	1	0
1	0	0	-2X	0	1	1
1	0	1	-X	1	0	1
1	1	0	-X	1	0	1
1	1	1	0	0	0	1

其中：

$$\text{SINGLE}_i = Y_{2i-1} \cdot \overline{Y_{2i}} + \overline{Y_{2i-1}} \cdot Y_{2i} = Y_{2i-1} \oplus Y_{2i}$$
$$\text{DOUBLE}_i = Y_{2i-1} \cdot Y_{2i} \cdot \overline{Y_{2i+1}} + \overline{Y_{2i-1}} \cdot \overline{Y_{2i}} \cdot Y_{2i+1}$$
$$\text{NEG}_i = Y_{2i+1}$$

而 SINGLE 的意思就是乘上 1 倍；DOUBLE 的意思就是乘上 2 倍(即左移 1 位)；兩者都為 0 的話就是乘上 0；而 NEG 的意思是乘上負號。最後再根據這個規則經過 Multiplicand Scaler 來輸出 Partial Products (PP_i)。

(2) Shown the Radix Booth-4 encoded partial products with simplified sign extension like that shown in Fig.10.82.



先把 sign bit 做 signed extension，再將所有的 1 先加起來，便可化簡成上圖。在 0~5 層的 Partial Products 會有 13 bits 而非 12 bits 是因為可能有兩倍的情況，而第 6 層的掃描數值 (Y_{13}, Y_{12}, Y_{11}) 中的前兩個為 0，因此 Partial Product 僅可能是 0 倍或 1 倍，故只需要 12 bits。

(3) Design the partial products with Dadda method shown in Fig.5.19. Carry-ripple adder is used in the last stage of CPA. Show the critical path and indicate the dely time in terms of number of HA and FA. For area, show the number of FA and HA used. Explain your design concepts.