Digital Integrated Circuits
#Home work 4   2025.04.16(Due: 04.25, 13:20)

/* Using 16 nm ADFP FiFFT devices with VDD= 0.8 V, FF process corner and medium Vt CMOS process*/
/*Rise time and fall time of input signals and clock are all 0.01ns (0V-0.8V)*/

1.   A 6-bit one stage pipelining <u>ripple adder</u> as shown at Fig.4.1(a) is designed with Fully Complementary Static Logic Gate for the 1-bit FA as shown at Fig4.1(c) and the D-register as shown at Fig.4.1(b). Input signals are A[5:0], B[5:0] and Cin which are provided by a unit size inverter. Outputs are Cout@Sum [6:0] with loading of 4 unit size inverters (FO4) connected in parallelism. You shall provide SPICE simulation results of timing and power waveforms.

(1)   Try your best to design the <u>fastest</u> adder without pipelining registers. First, show your <u>block diagrams</u> in terms of the 1-bit Full-Adder(FA). Second, show the <u>circuit schematic of each block</u>. Use logic effort concepts (you do not have to write down the procedure) to design <u>transistor widths (in table form)</u>. **Describe your design concept.** (40%)

(2)   Based on the design of (1), run SPICE to find the the <u>propagation delay time</u> (with pattern from 0000001111110 to 0000001111111 (A[5:0]@B[5:0]@Cin). Determine the <u>minimum </u>clock cycle time with the delay time estimated by SPICE. (20%)

(3)   Run SPICE to get the <u>average, peak </u>and <u>leakage power dissipation and energy/bit, respectively</u> of this adder with loading (FO4) when working at the maximum working frequency. (20%)

(4)   Add one pipelining stage using the designed D register (Fig.4.1(b)) into the 6-bit ripple adder as shown at Fig.4.1(a). Run SPICE to find the the <u>propagation delay time</u> (with pattern from 0000001111110 to 0000001111111 (A[5:0]@B[5:0]@Cin) between pipelining stages to determine the <u>maximum working frequency</u> of the clock with the delay time estimated by SPICE. (20%)
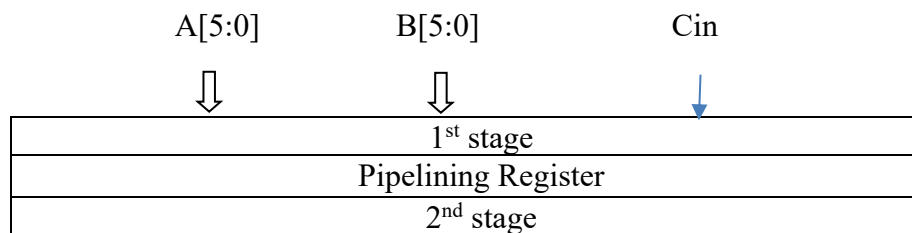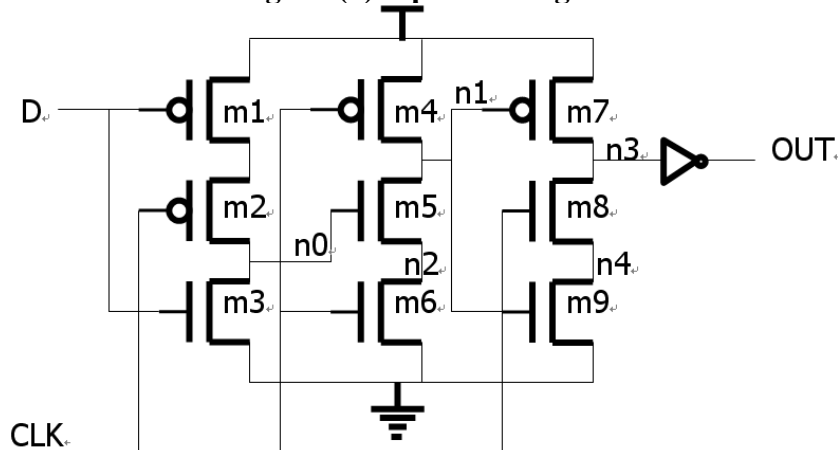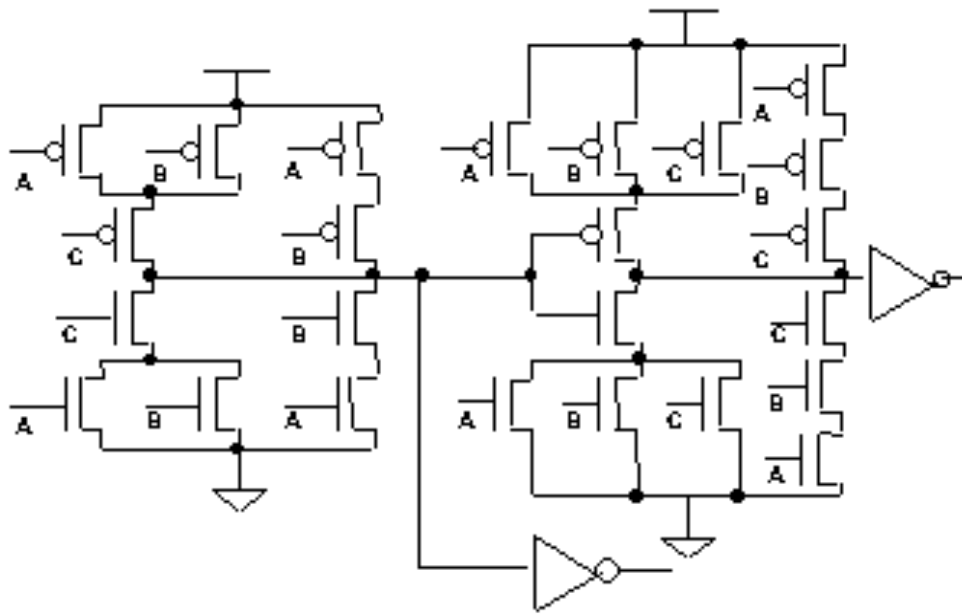

Fig. 4.1(a) Pipeline design of 4 bit adder

Fig.4.1 (b) Dynamic D register .

Fig.4.1 (c) 1-bit static Full addrer.

/*You should provide the SPICE input description, timing and power waveforms*/