Digital Integrated Circuits

#Homework 3
04.09 (Due: 04.18, 13:20)

/* Using 16 nm ADFP FiFFT devices with VDD= 0.8 V, FF process corner and medium Vt CMOS process*/
/*Rise time and fall time of input signals and clock are 0.01ns (0V-0.8V)*/

1. Inverter and Ring oscillator (50%)
   a) Inverter (20%)
   Keep a unit size inverter with NMOS n=1and choose the n of PMOS for n=1 and 2. Run SPICE to show the logic threshold voltage. Verify and discuss your results by showing simulated waveforms.
   b) Ring oscillator (30%)
   According to the results of 1a), design a 3-stage inverter-based ring oscillator with unit size inverter of a better logic threshold voltage. Set the initial voltage of each node so that it can oscillate. Show **in table form**, the SPICE simulation results of oscillation frequency and power consumption.
2. (50%) Design a static D register as shown in Fig.1 with propose size of NMOS and PMOS to have better tsetup, tpcq, tpdq and thold time. The loading of Q and Q-have 2 unit size inverters as loading. Both D and CLK has rise time and fall time of 0.1ns (0V-0.8V).
   a) Explain your sizing principle of each MOS to have least tsetup, tpcq, tpdq and thold time for register 1 and 0.
   b) Run SPICE to verify your results and list the results in table form for part (b).

Fig.1