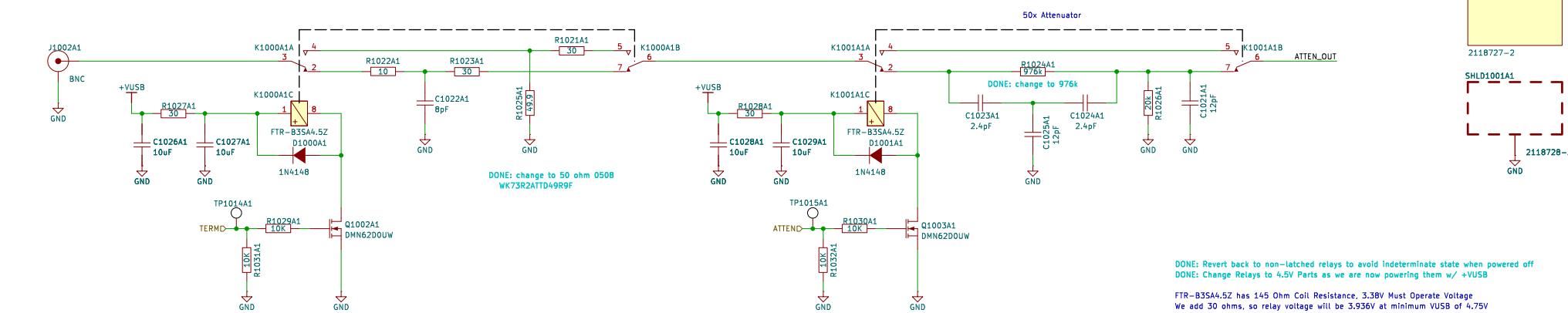
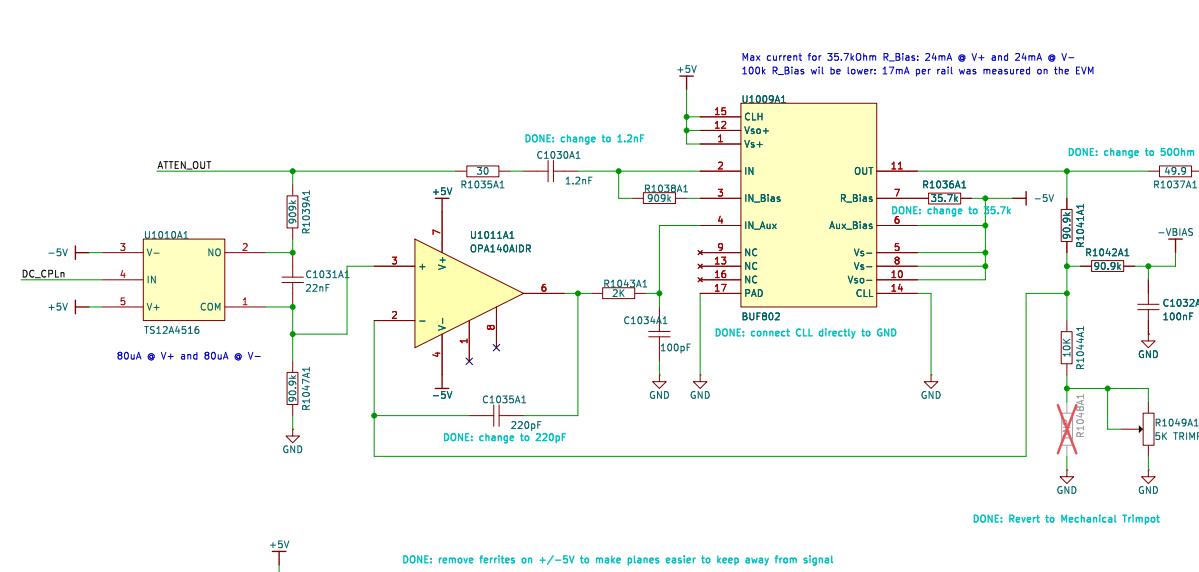


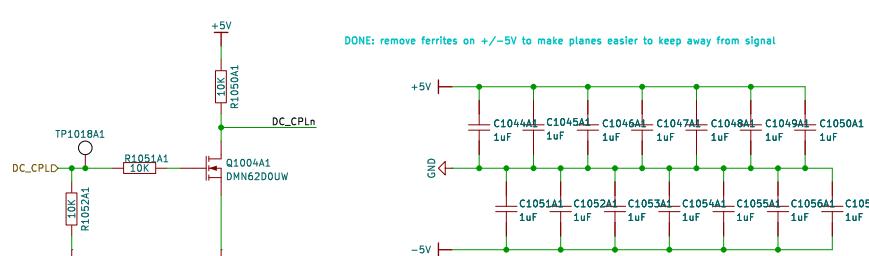
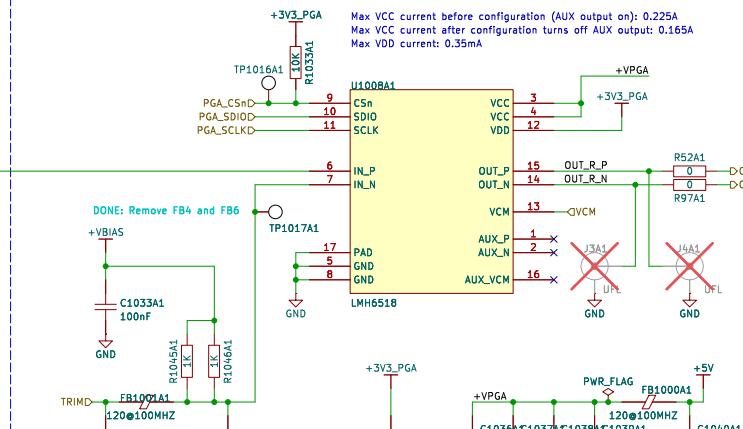
## Termination and Attenuation



## Input Buffer and AC/DC Coupling

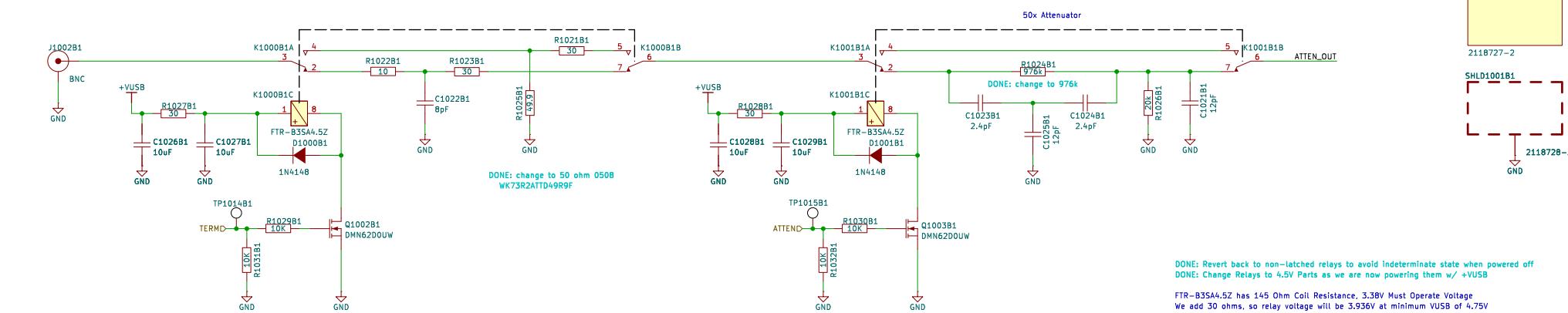


## Programmable Gain Amplifier

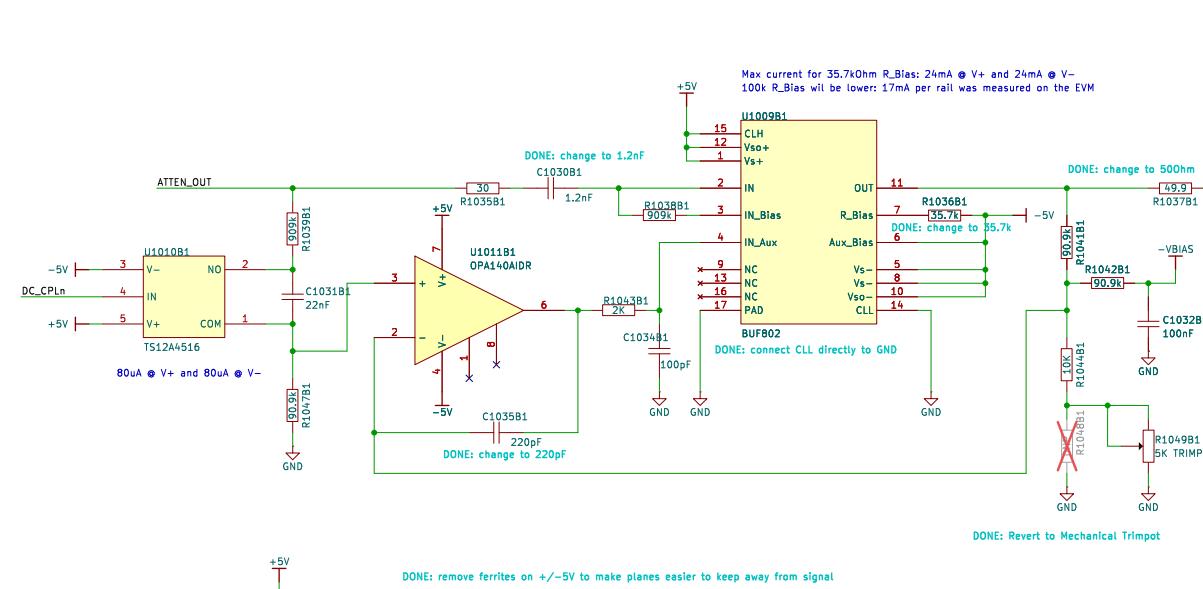


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Title: ThunderScope  
Size: A3 Date: Rev: 5  
KiCad E.D.A. 8.99.0-3402-gadd58faa30 Id: 2/16

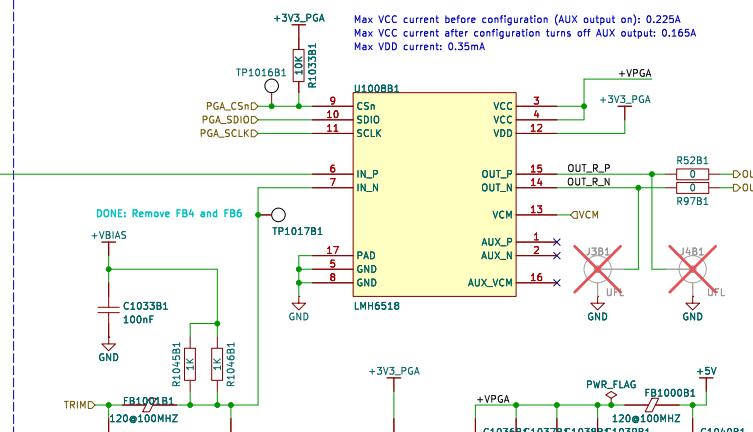
## Termination and Attenuation



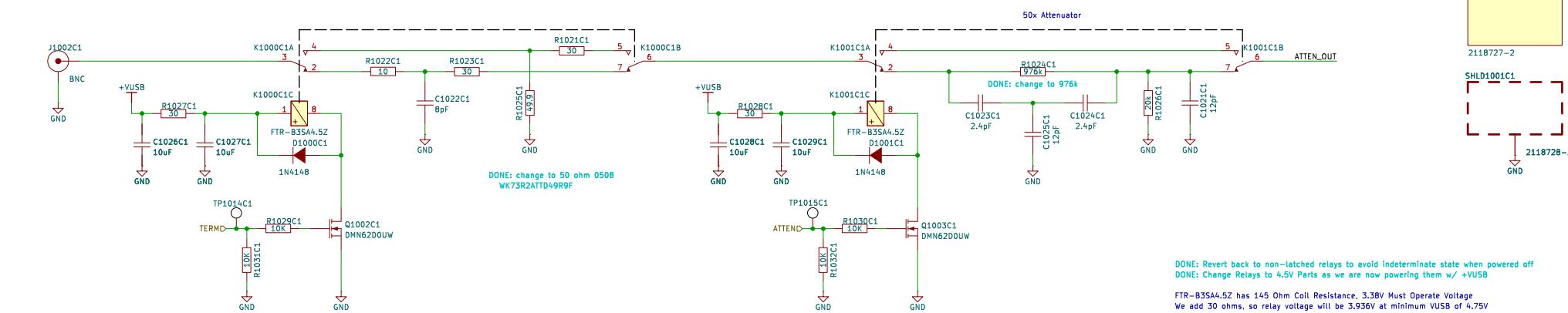
## Input Buffer and AC/DC Coupling



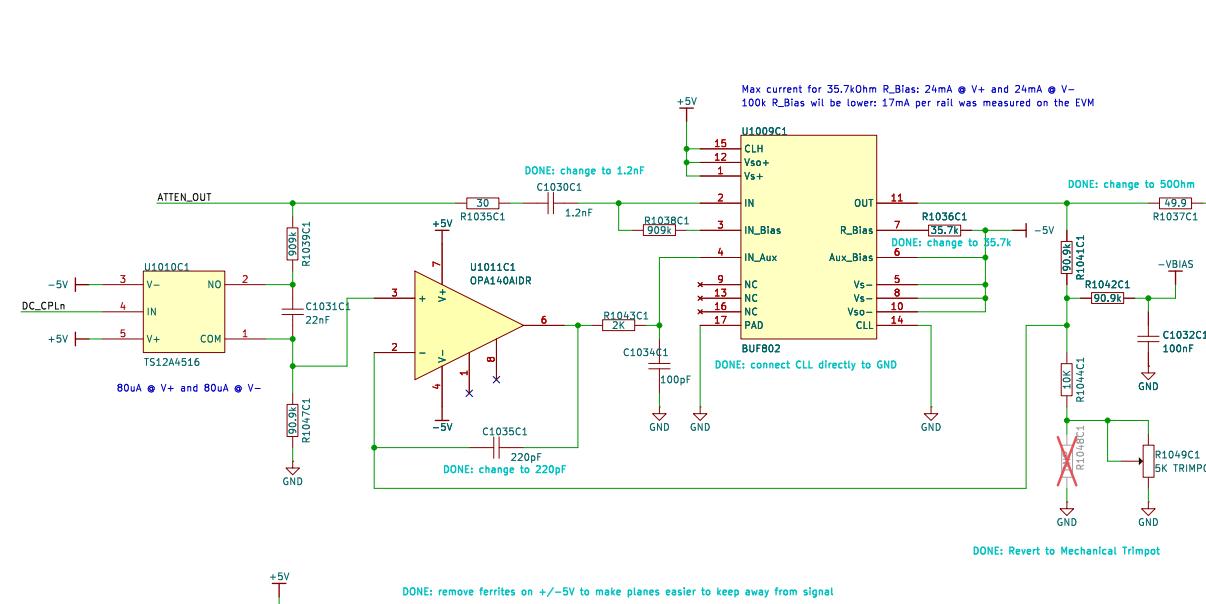
## Programmable Gain Amplifier



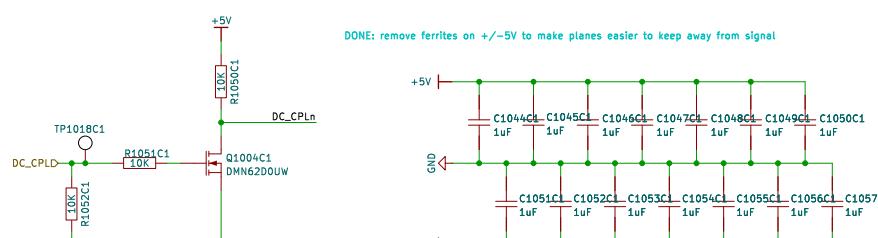
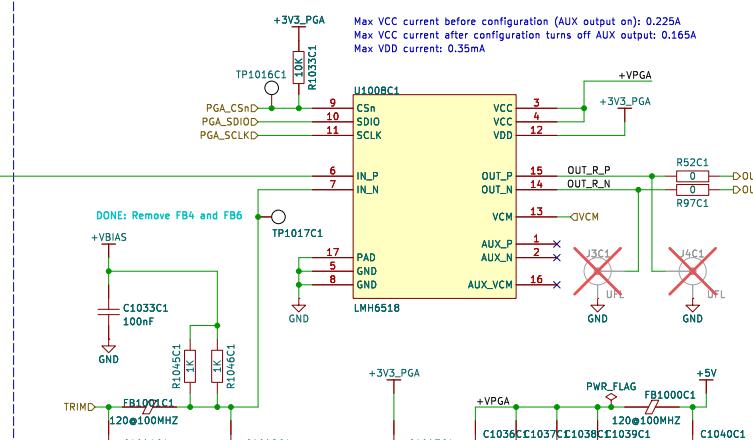
## Termination and Attenuation



## Input Buffer and AC/DC Coupling

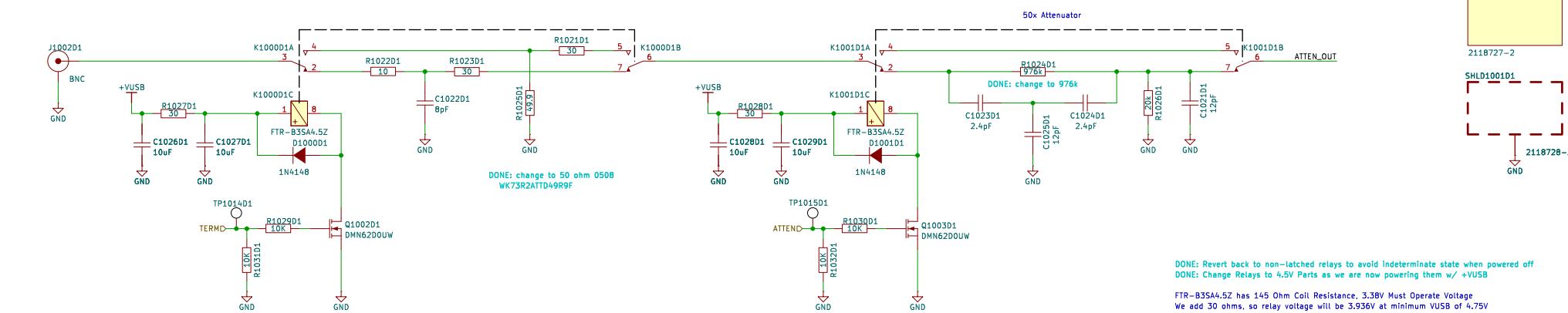


## Programmable Gain Amplifier

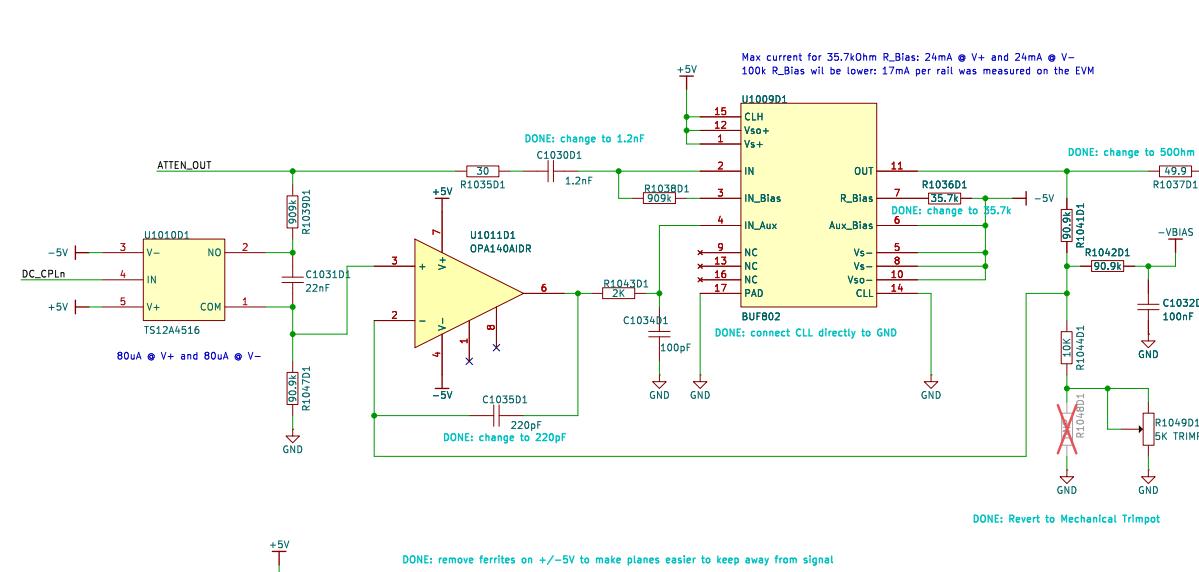


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Size: A3 Date: Rev: 5  
KiCad E.D.A. 8.99.0-3402-gadd58faa30 Id: 2/16

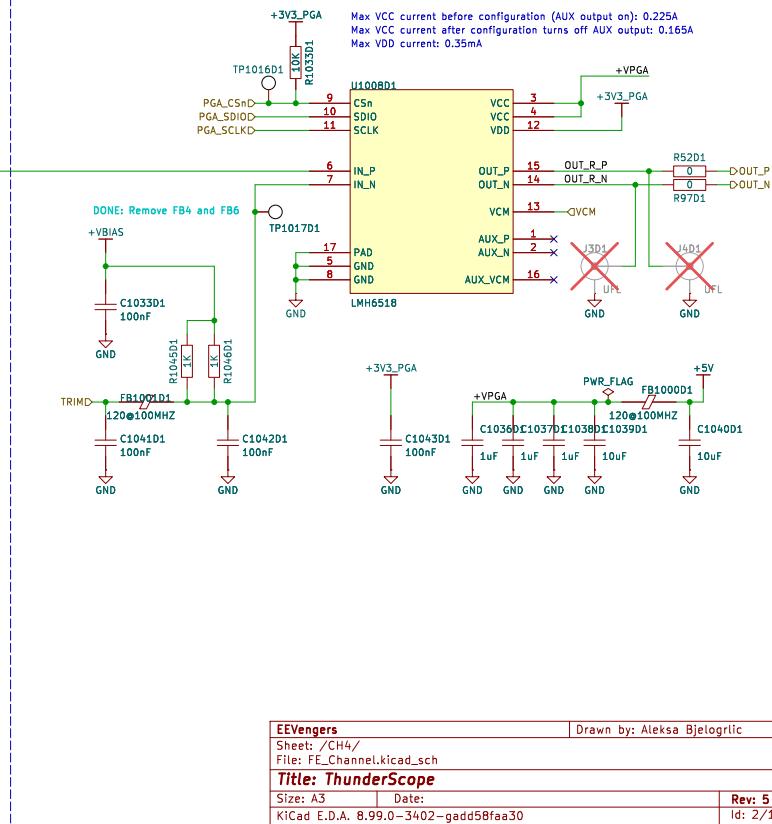
## Termination and Attenuation



## Input Buffer and AC/DC Coupling



## Programmable Gain Amplifier

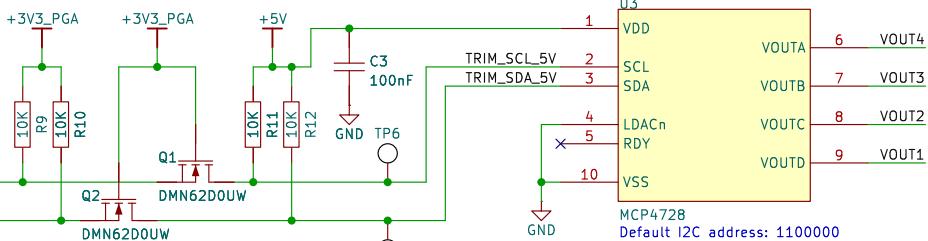


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Title: ThunderScope  
Size: A3 Date: Rev: 5  
KiCad E.D.A. 8.99.0-3402-gadd58faa30  
Id: 2/16

1 2 3 4 5 6

## Offset Voltage Trim and User Offset Control

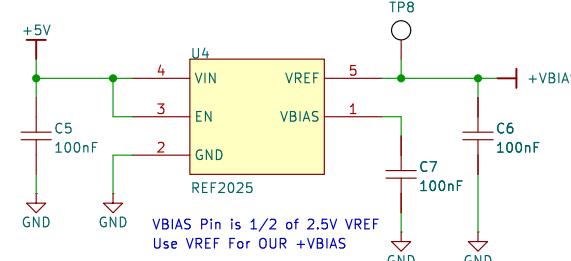
A



B

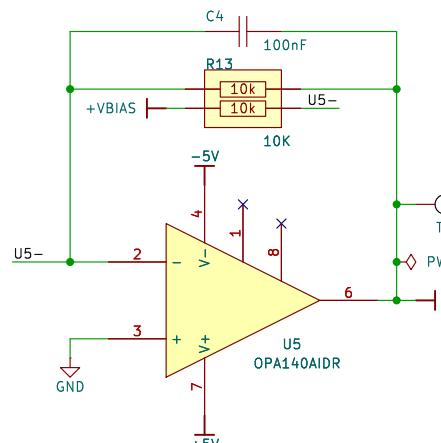
## Bias Voltage Generation

C



D

Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140  
-Max resistance is  $(575/4 // 10k) = 141.7 \text{ Ohm}$   
-Worst case current is  $17.64\text{mA}$   
-Use REF2025, has max current of  $20\text{mA}$   
-Change U5 divider to matched resistor network  
-ACASN1002S1002P1AT



EEVengers

Sheet: /Front End Trim and Bias/  
File: FE.kicad\_sch

Title: ThunderScope

Size: A4 Date:  
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

Rev: 5  
Id: 3/16

1

2

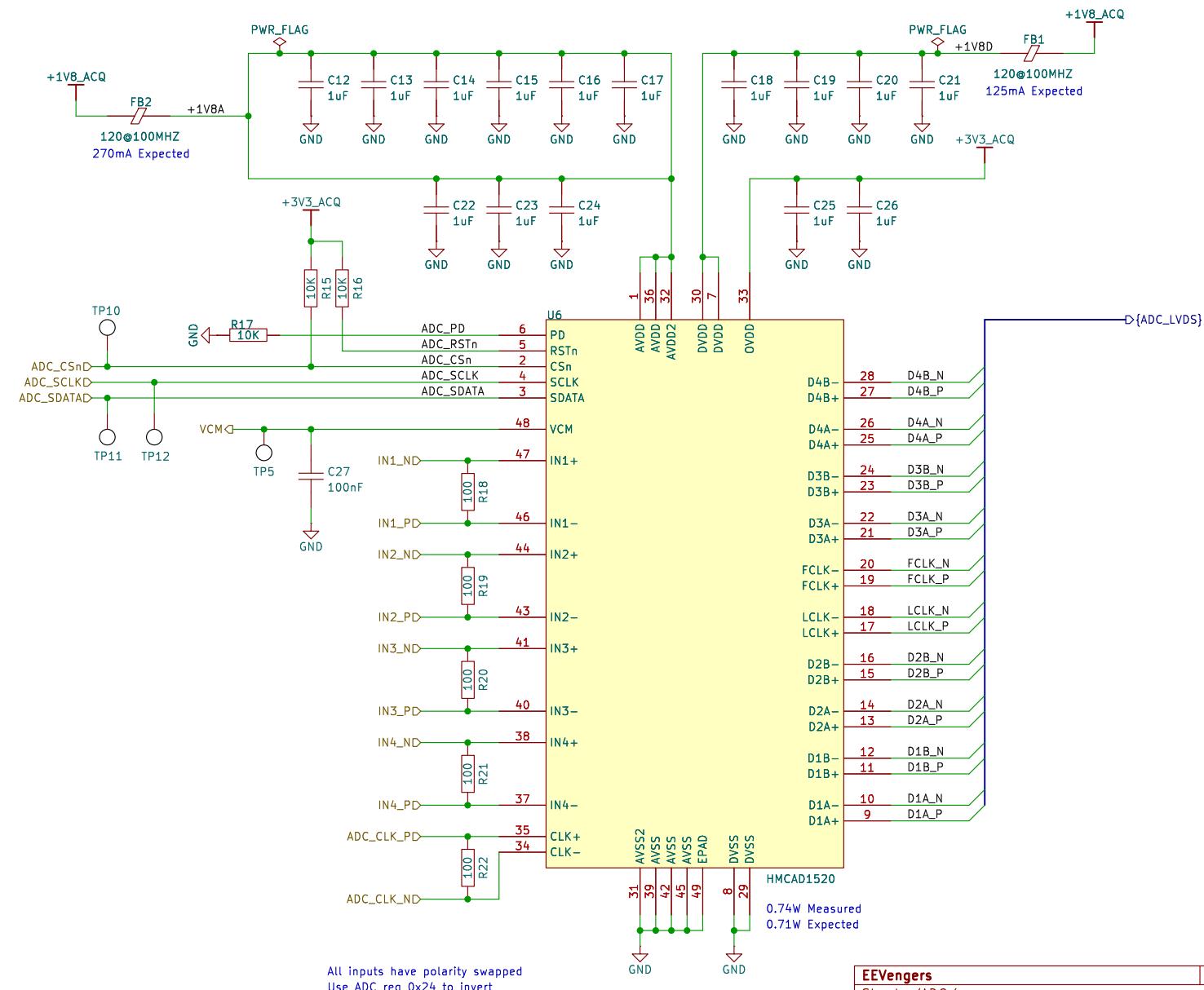
3

4

5

6

1 2 3 4 5 6

**ADC**

All inputs have polarity swapped  
Use ADC reg 0x24 to invert

**EEVengers**

Drawn by: Aleksa Bjelogrlic

Sheet: /ADC/  
File: ADC.kicad\_sch**Title: ThunderScope**

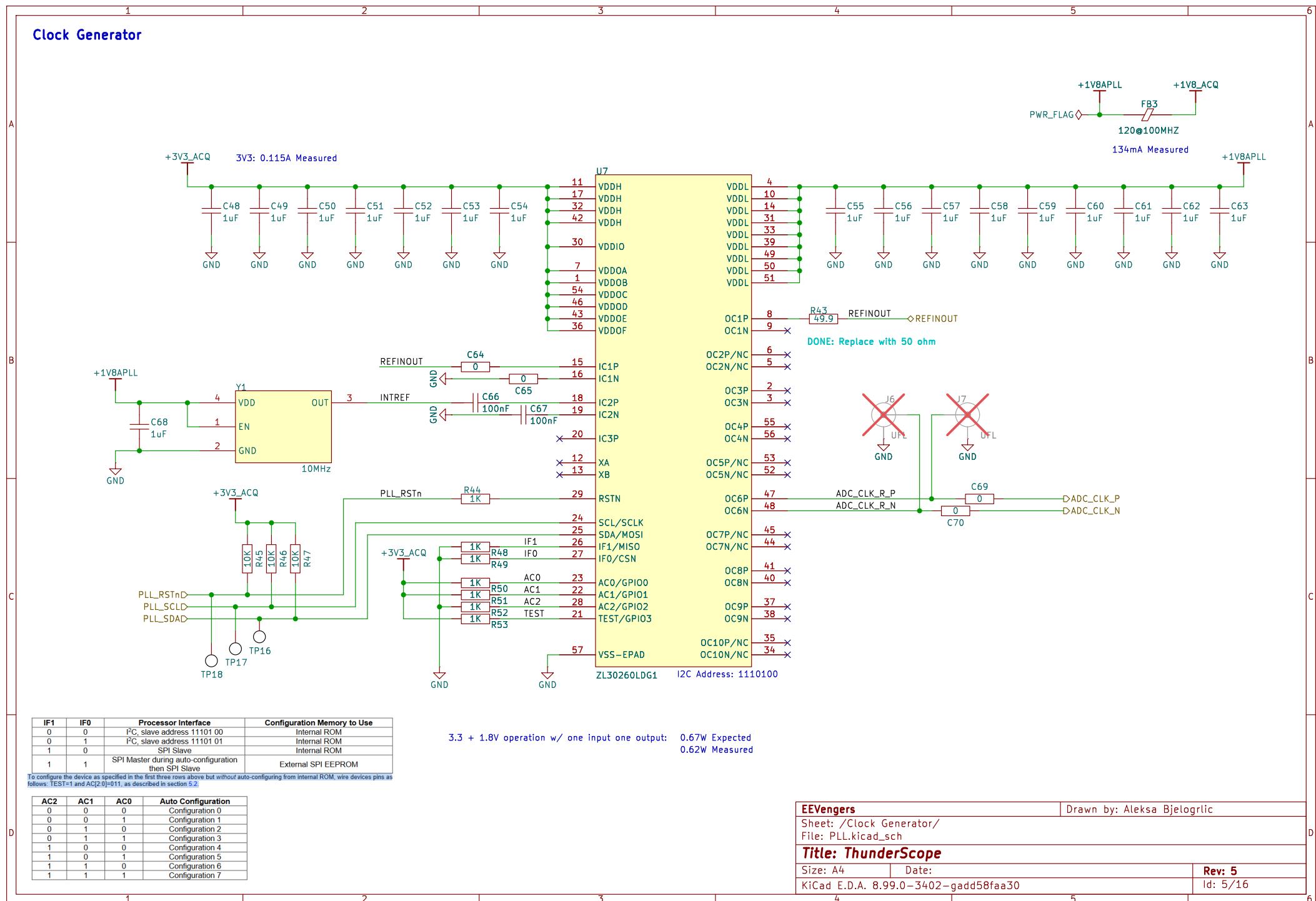
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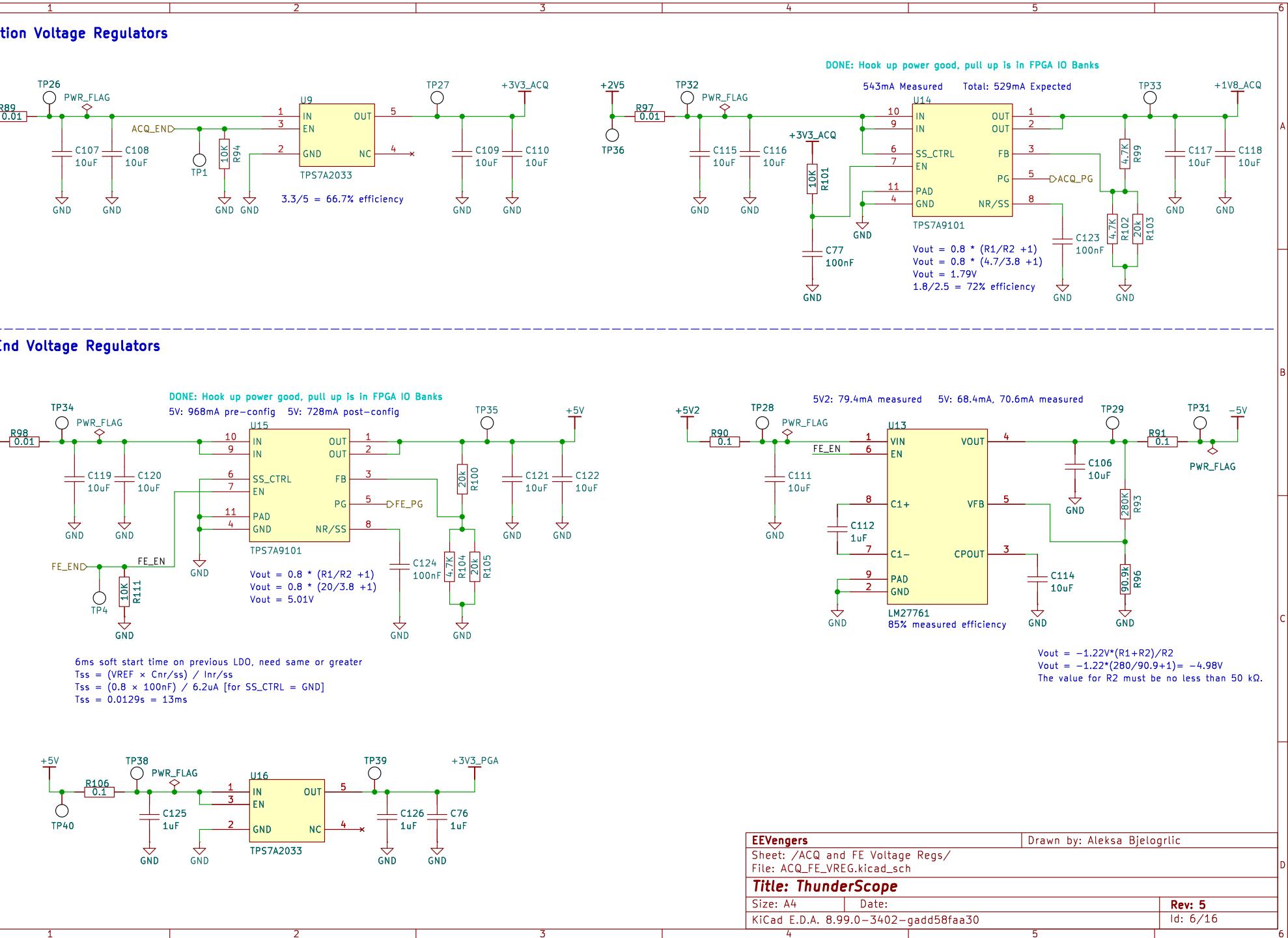
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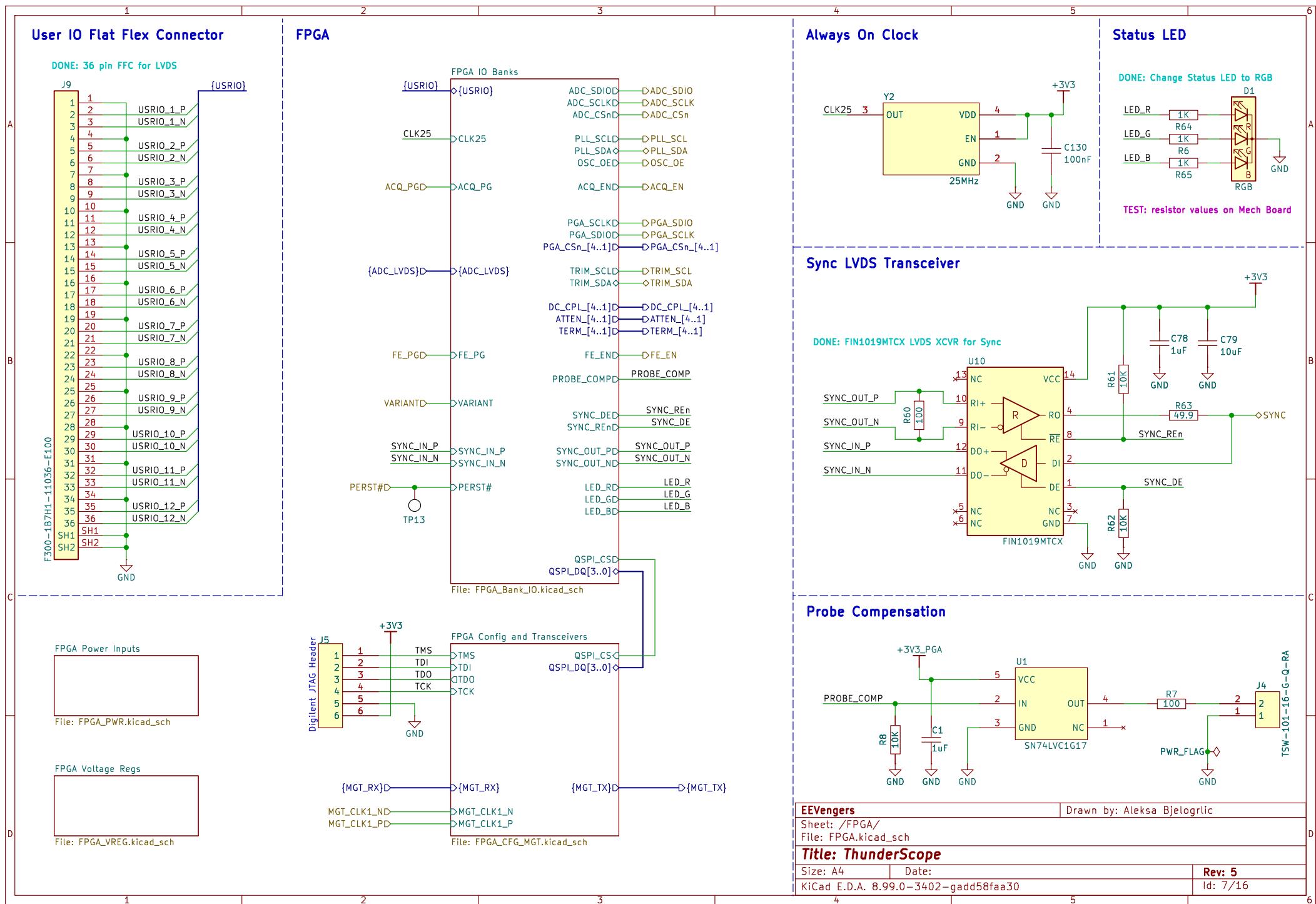
Rev: 5

Id: 4/16

1 2 3 4 5 6

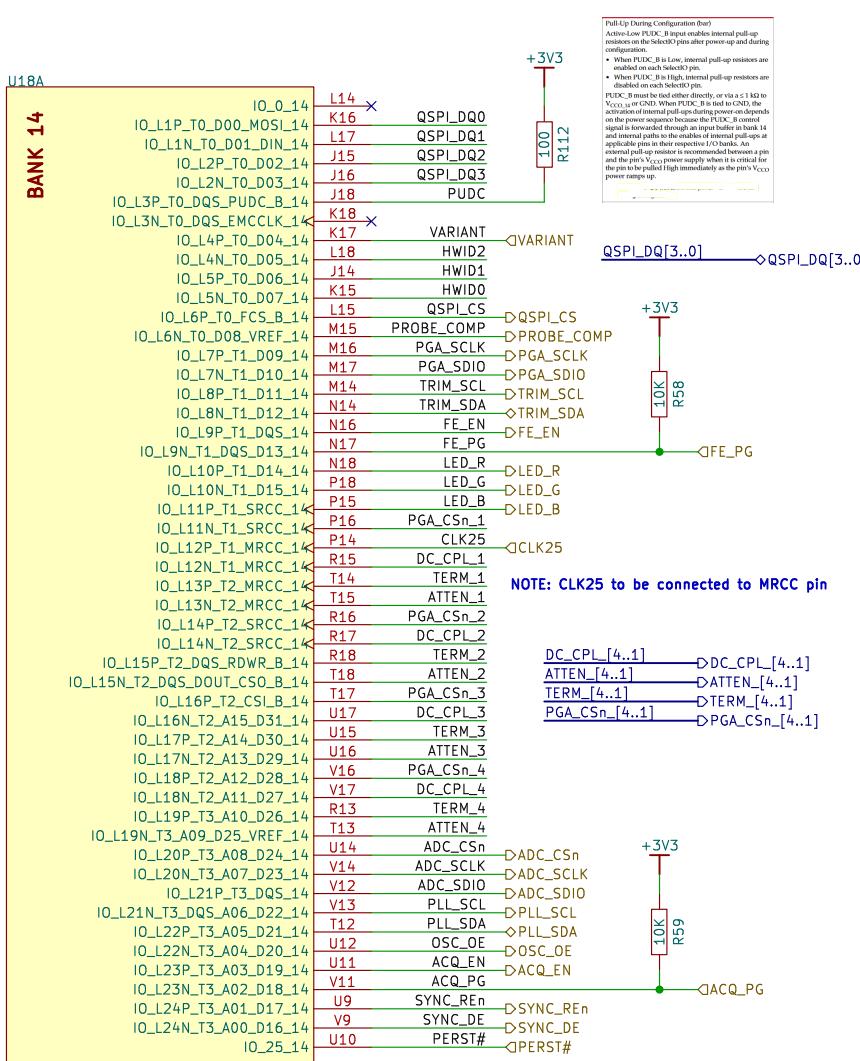




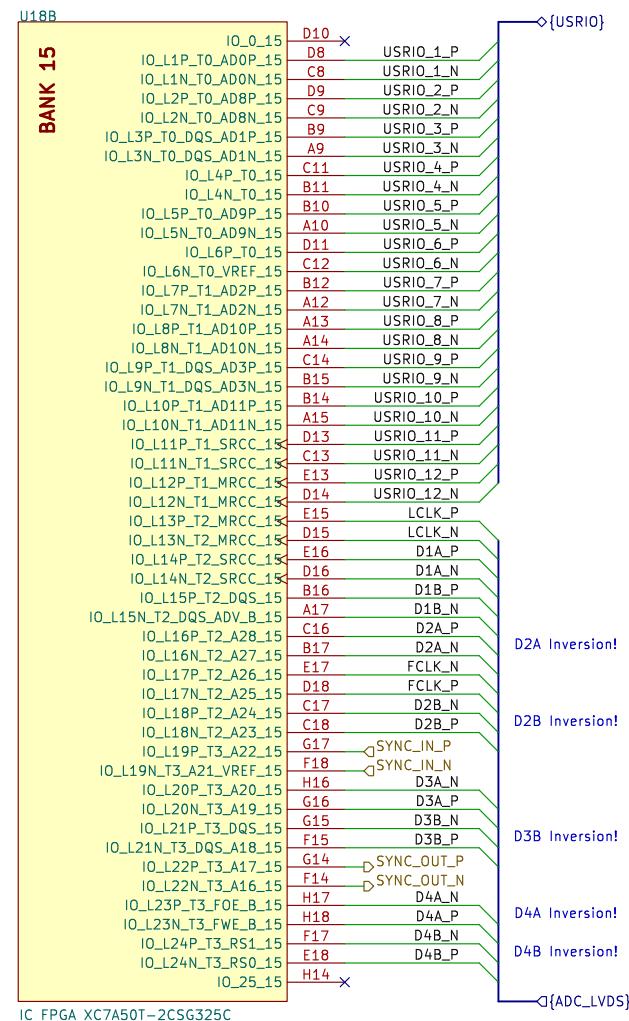


**FPGA IO Banks**

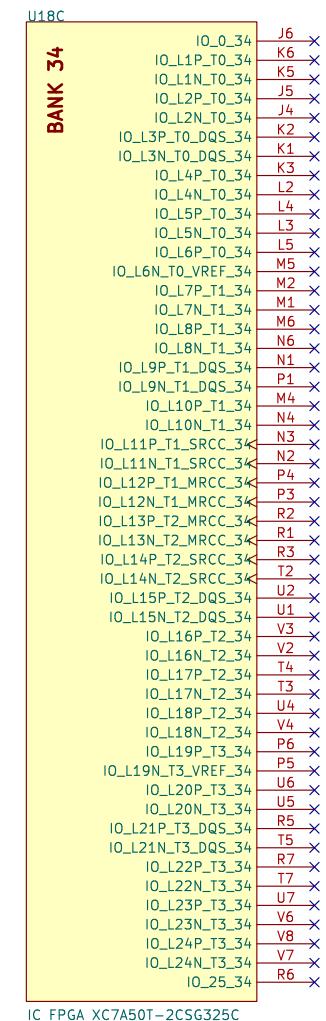
A



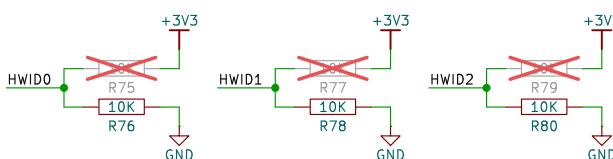
B



C



D

**EEVengers**

Sheet: /FPGA/FPGA IO Banks/  
File: FPGA\_Bank\_IO.kicad\_sch

Drawn by: Aleksa Bjelogrlic

**Title: ThunderScope**

Size: A4 Date:  
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Rev: 5  
Id: 8/16

## FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

**Note:** DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

Connect INIT\_B to a ≤ 4.7 kΩ pull-up resistor to V<sub>CCO\_0</sub> to ensure clean Low-to-High transitions.

Connect PROGRAM\_B to an external ≤ 4.7 kΩ pull-up resistor to V<sub>CCO\_0</sub> to ensure a stable High input, and

Table 2-1: 7 Series FPGA Configuration Modes				
Configuration Mode	M2[0]	Bus Width	CCLK Direction	
Master SPI	001	x1, x2, x4	Output	

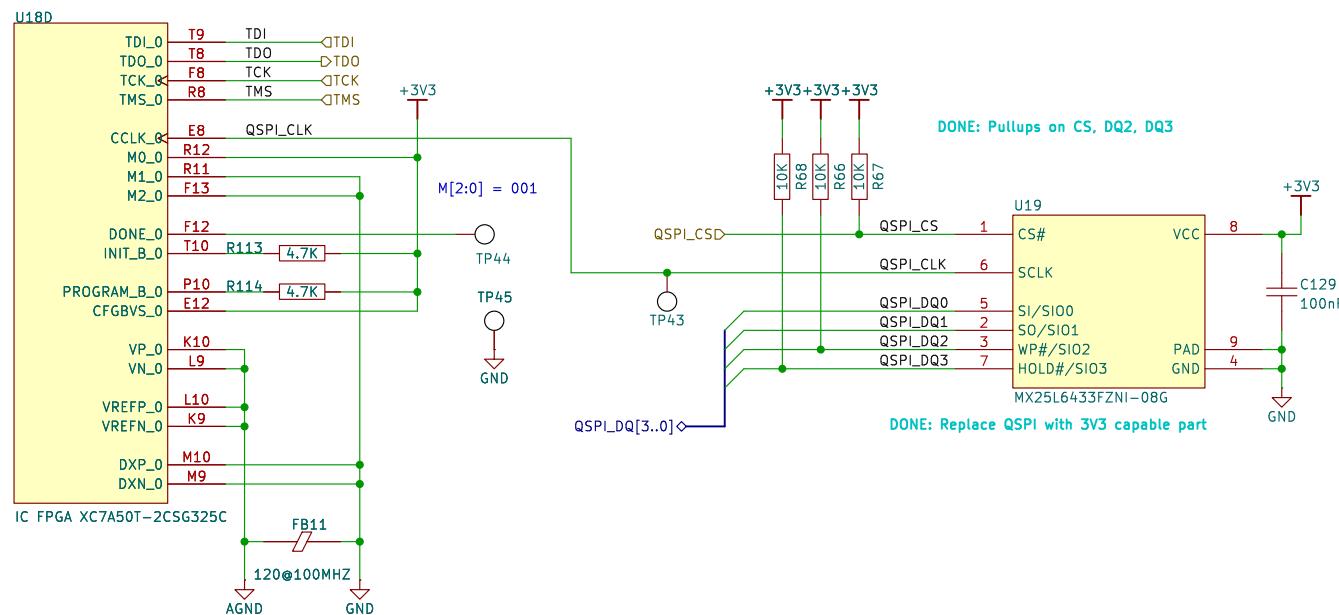
Table 2-2: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Bank Used	Configuration Interface I/O	HR Bank 0 V <sub>CCO</sub> 0	HR Bank 14 V <sub>CCO</sub> 14	HR Bank 15 V <sub>CCO</sub> 15	CFGBVS
JTAG (only)	0	VREFP_0	2.3V	2.3V	Any	VCCO_0
		VREFN_0	2.3V	2.3V	Any	VCCO_0
		DXP_0	1.8V	1.8V	Any	GND
		DXN_0	1.8V	1.8V	Any	GND
Serial SPI or SelectMAP	0, 14 <sup>(1)</sup>	VREFP_0	2.3V	2.3V	2.3V	VCCO_0
		VREFN_0	2.3V	2.3V	2.3V	VCCO_0
		DXP_0	1.8V	1.8V	1.8V	GND
		DXN_0	1.8V	1.8V	1.8V	GND
		VREFP_0	3.3V	3.3V	3.3V	VCCO_0
		VREFN_0	3.3V	3.3V	3.3V	VCCO_0
		DXP_0	1.5V	1.5V	1.5V	GND
BPI <sup>(2)</sup>	0, 14, 15	VREFP_0	2.3V	2.3V	2.3V	VCCO_0
		VREFN_0	2.3V	2.3V	2.3V	VCCO_0
		DXP_0	1.8V	1.8V	1.8V	GND
		DXN_0	1.8V	1.8V	1.8V	GND

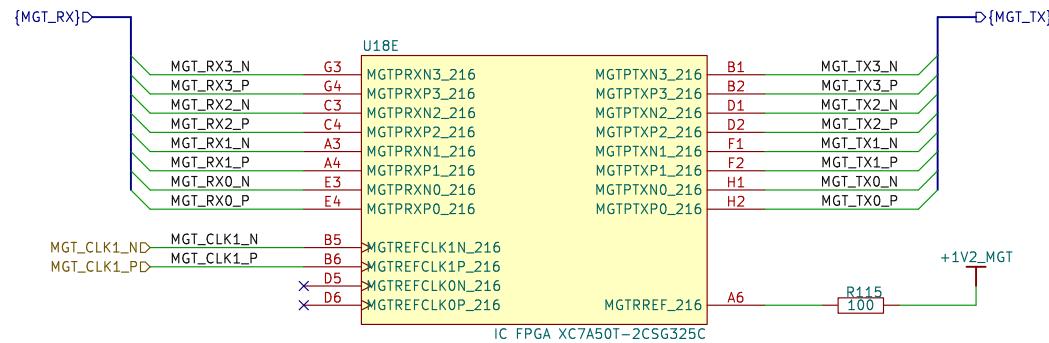
Notes:

1. RS232 for Multiflash or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.

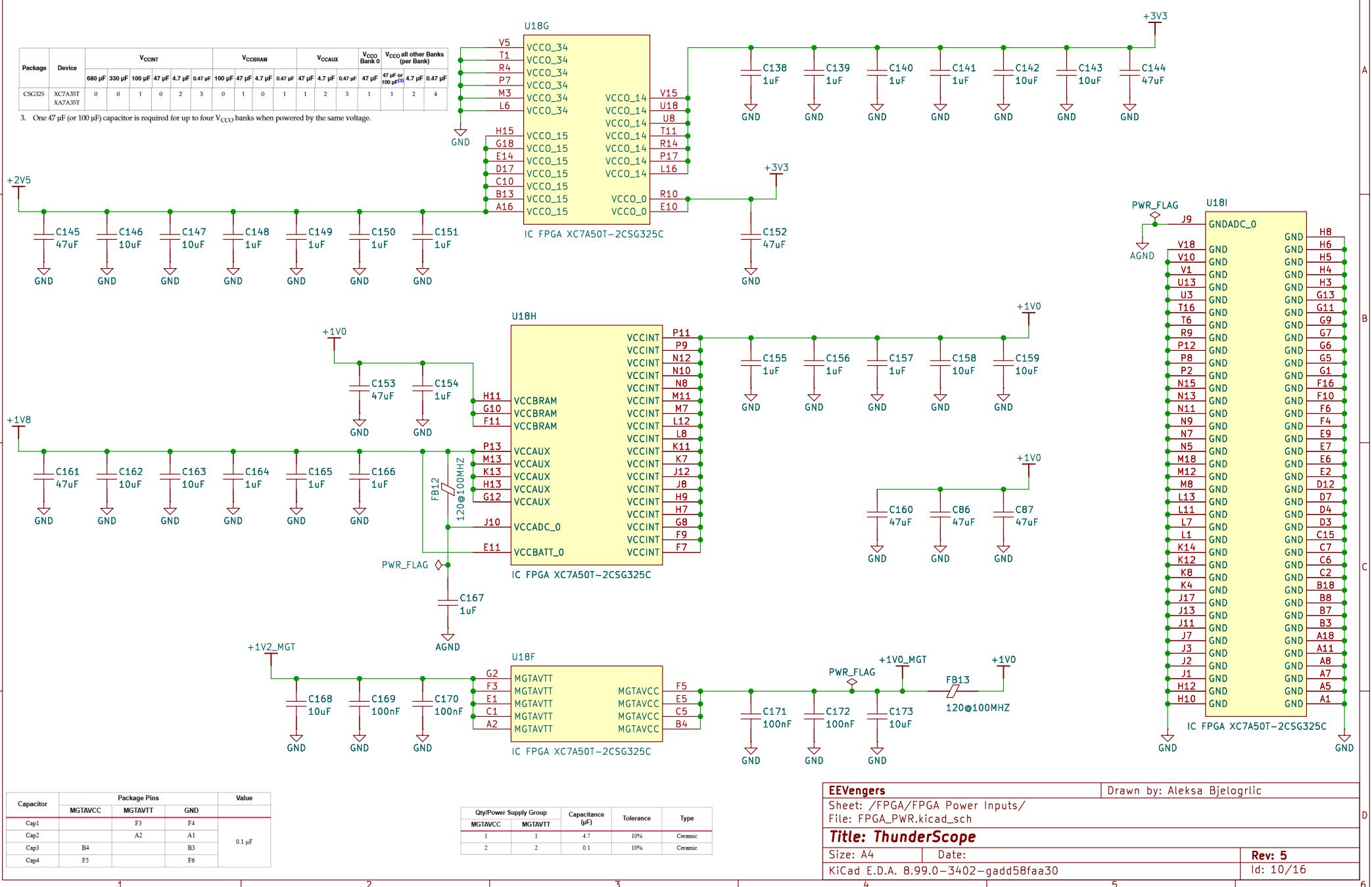
2. BPI mode is not available in the Spartan-7 family.



## FPGA Transceivers



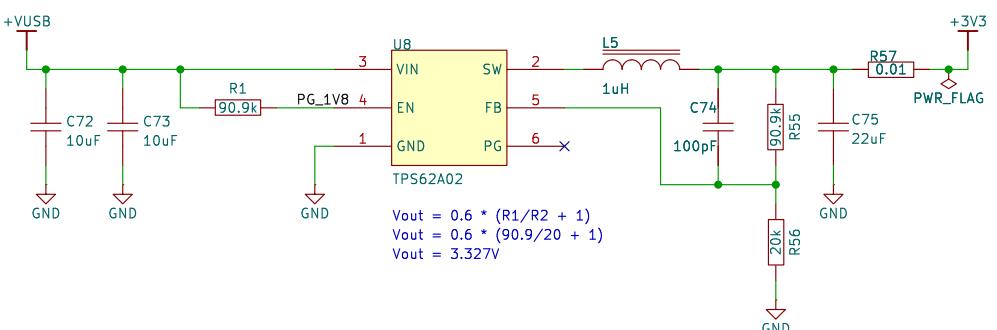
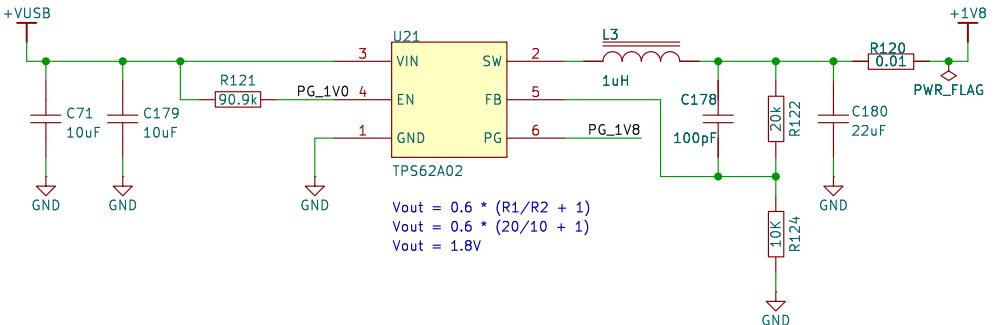
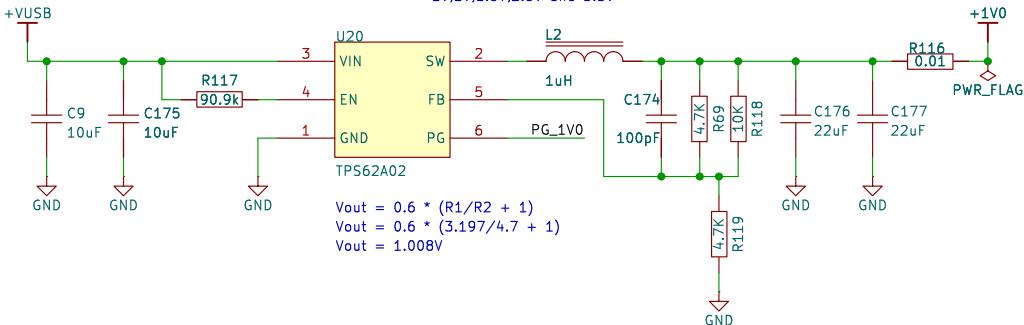
## PAGE 1: FPGA Power Inputs



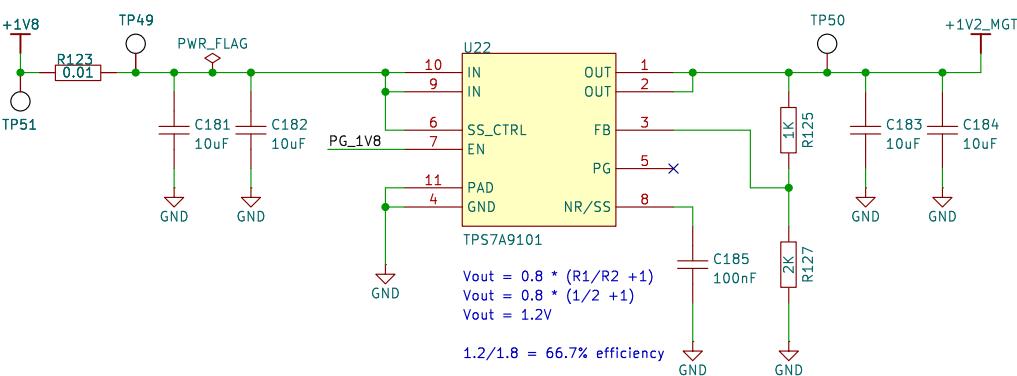
1 2 3 4 5 6

## FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO  
1V,1V,1.8V,2.5V and 3.3V



Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V <sub>CCO</sub>	Supply Voltage		2.375	2.500	2.625	V

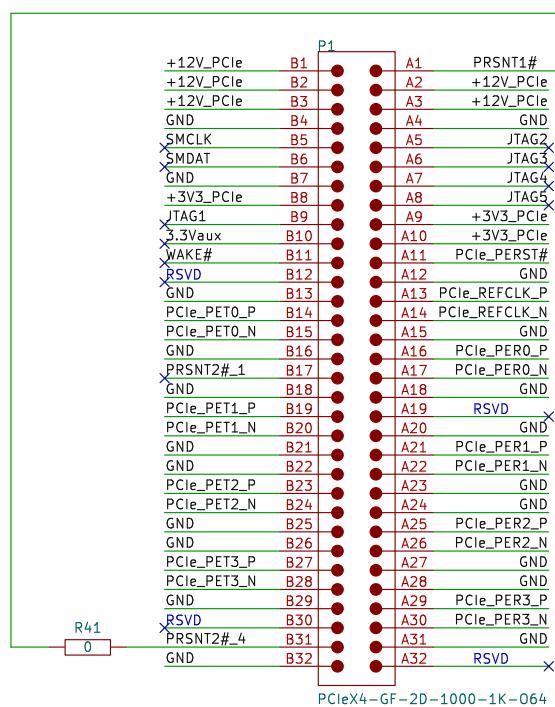


The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT  
1V,1V,1.2V

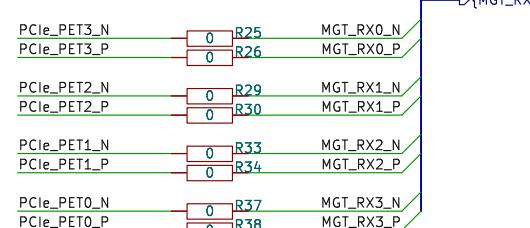
EEVengers	Drawn by: Aleksa Bjelogrlic
Sheet: /FPGA/FPGA Voltage Regs/	
File: FPGA_VREG.kicad_sch	
<b>Title: ThunderScope</b>	
Size: A4	Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30	Rev: 5
	Id: 11/16

1 2 3 4 5 6

### PCIe x4 Edge Connector

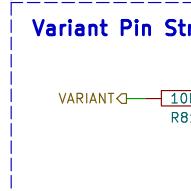
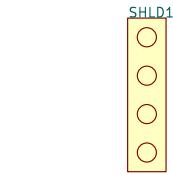


PCIe\_PERST# → 49.9 R23 PERST# → PERST#

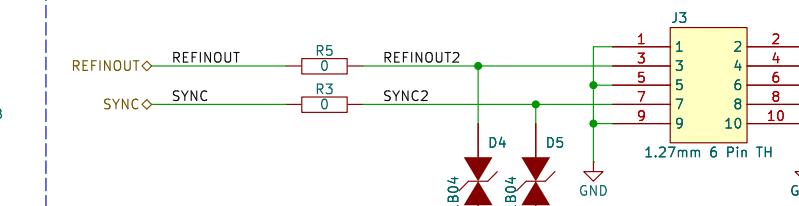


AC Couple PER Lines with 100nF  
AC Couple REFCLK Lines with 100nF

PCIe\_REFCLK\_N → C44 → MGT\_CLK1\_N, PCIe\_REFCLK\_P → C45 → MGT\_CLK1\_P, 100nF, MGT\_CLK1\_N → MGT\_CLK1\_P, MGT\_CLK1\_P → MGT\_CLK1\_N.

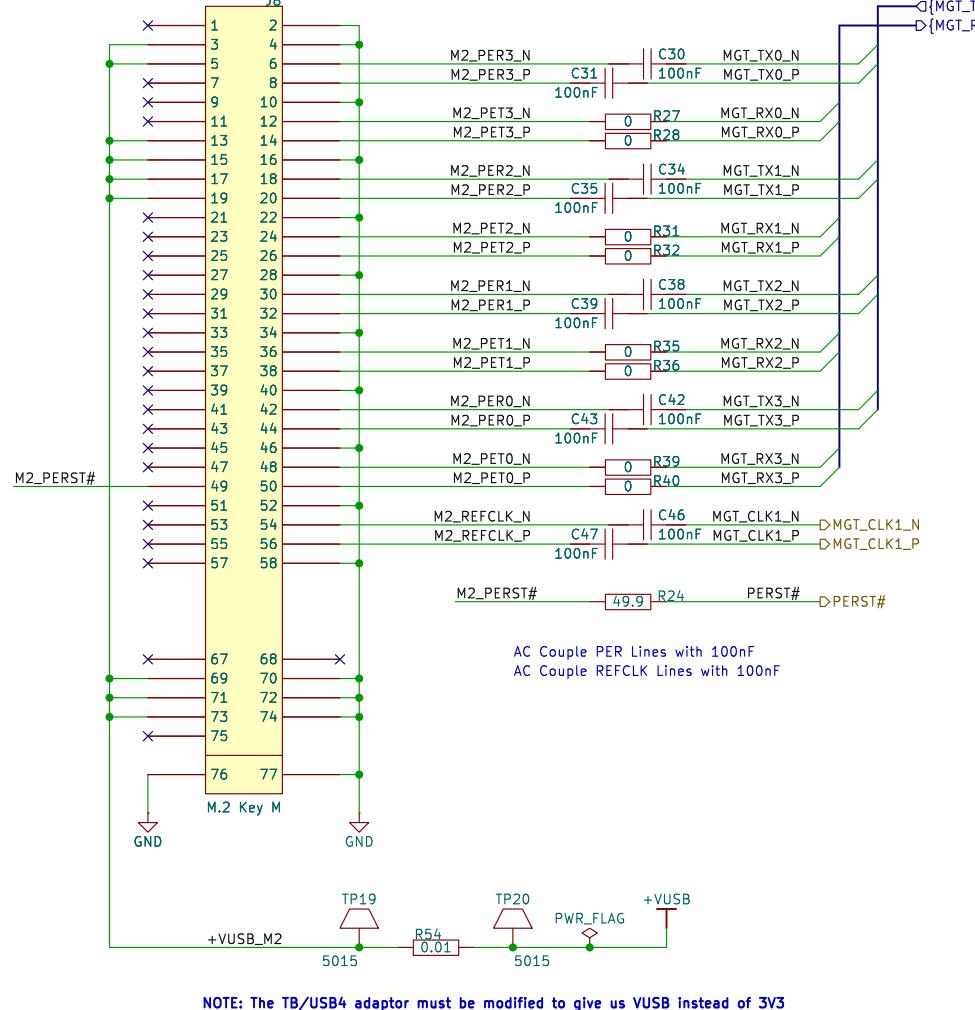


### Refclock and Sync Header

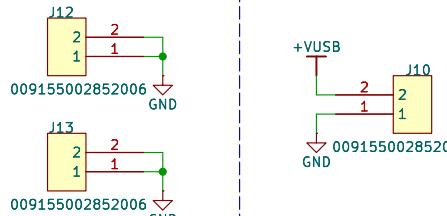


**EEVengers** | Drawn by: Aleksa Bjelogrlic  
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**Title: ThunderScope**  
Size: A4 Date:  
KiCad E.D.A. 8.99.0-3402-gadd58faa30 Rev: 5  
Id: 12/16

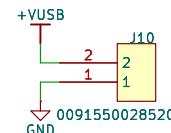
## M.2 Key M Connector – Custom Pinout



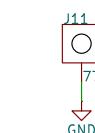
## EMI Spring Grounds



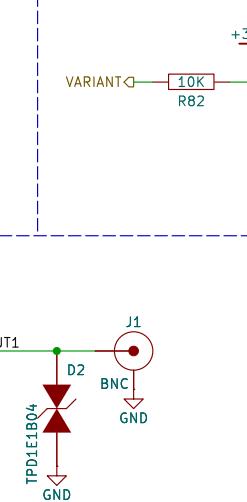
## Fan Connector



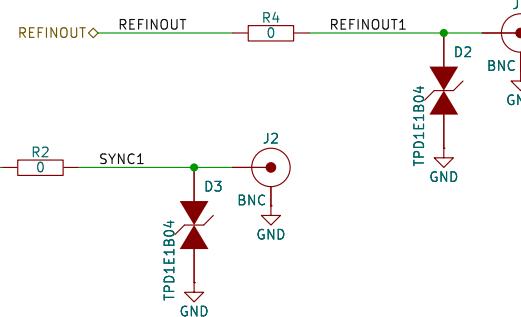
## Ground Lug



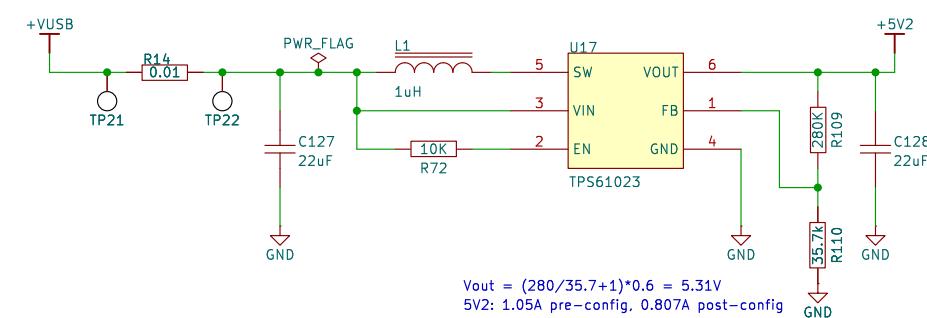
## Variant Pin Strap



## Refclock and Sync BNCs



## 5V2 Boost Converter



EEVengers

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File: M2\_KEY\_M.kicad\_sch

Title: ThunderScope

Size: A4 Date:  
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

Rev: 5  
Id: 13/16