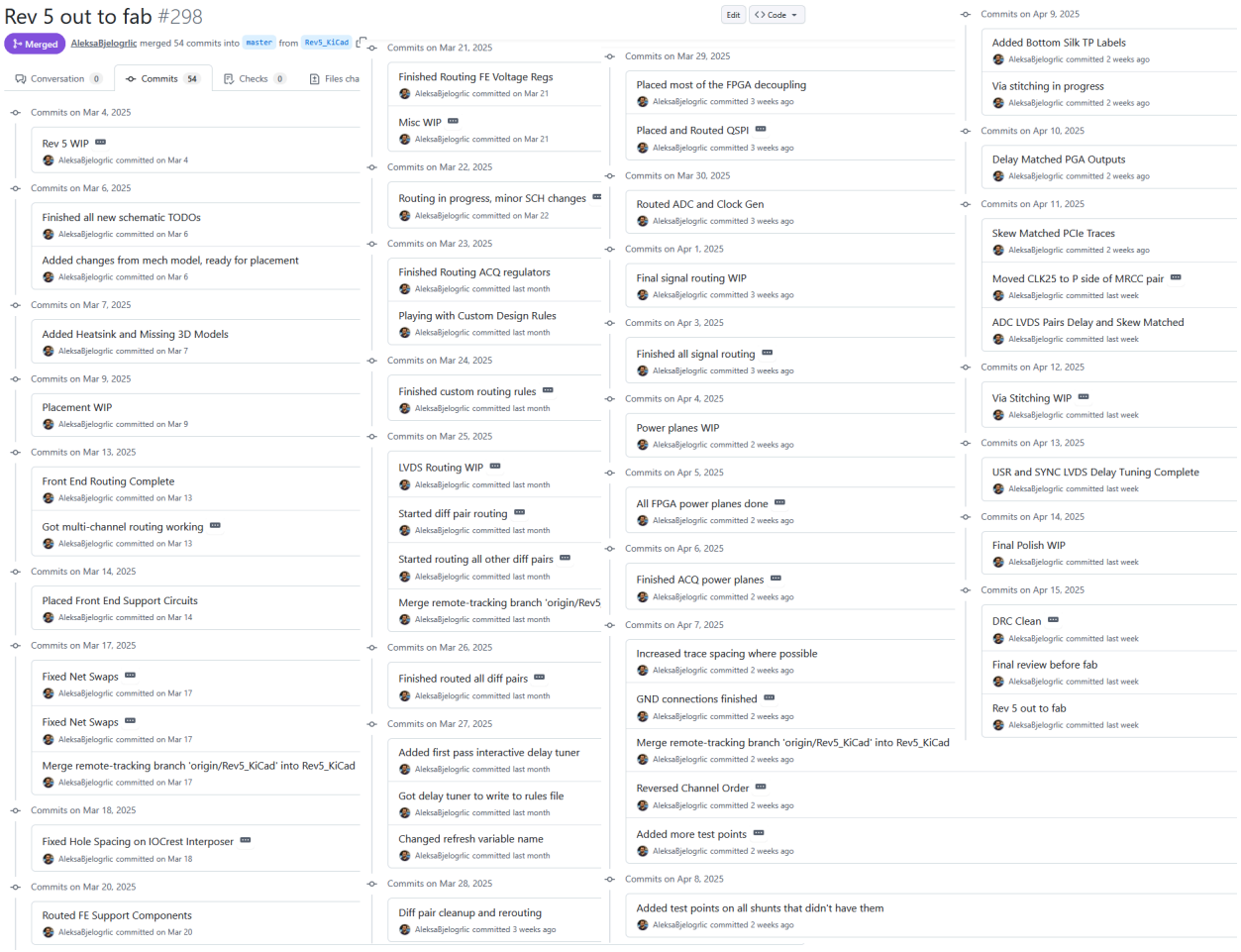
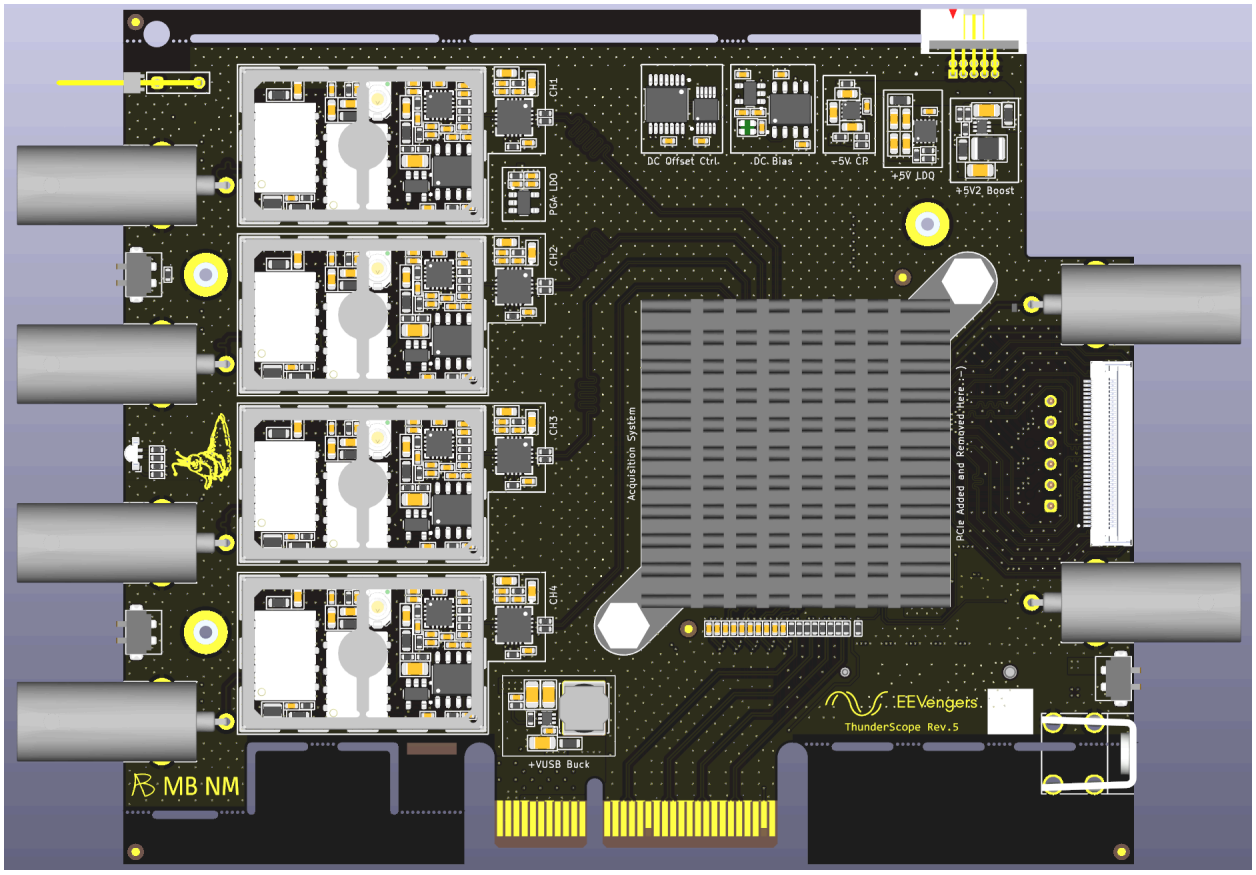
Revving Up for Production

Hi all,

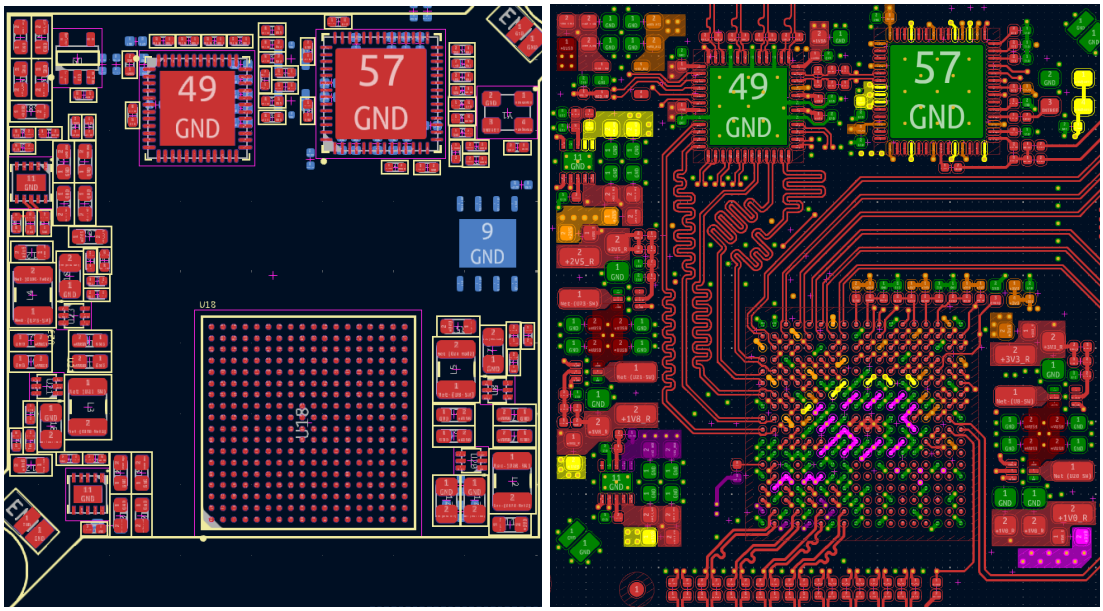
I spent the last month and a half heads down on the PCB layout for Rev 5…



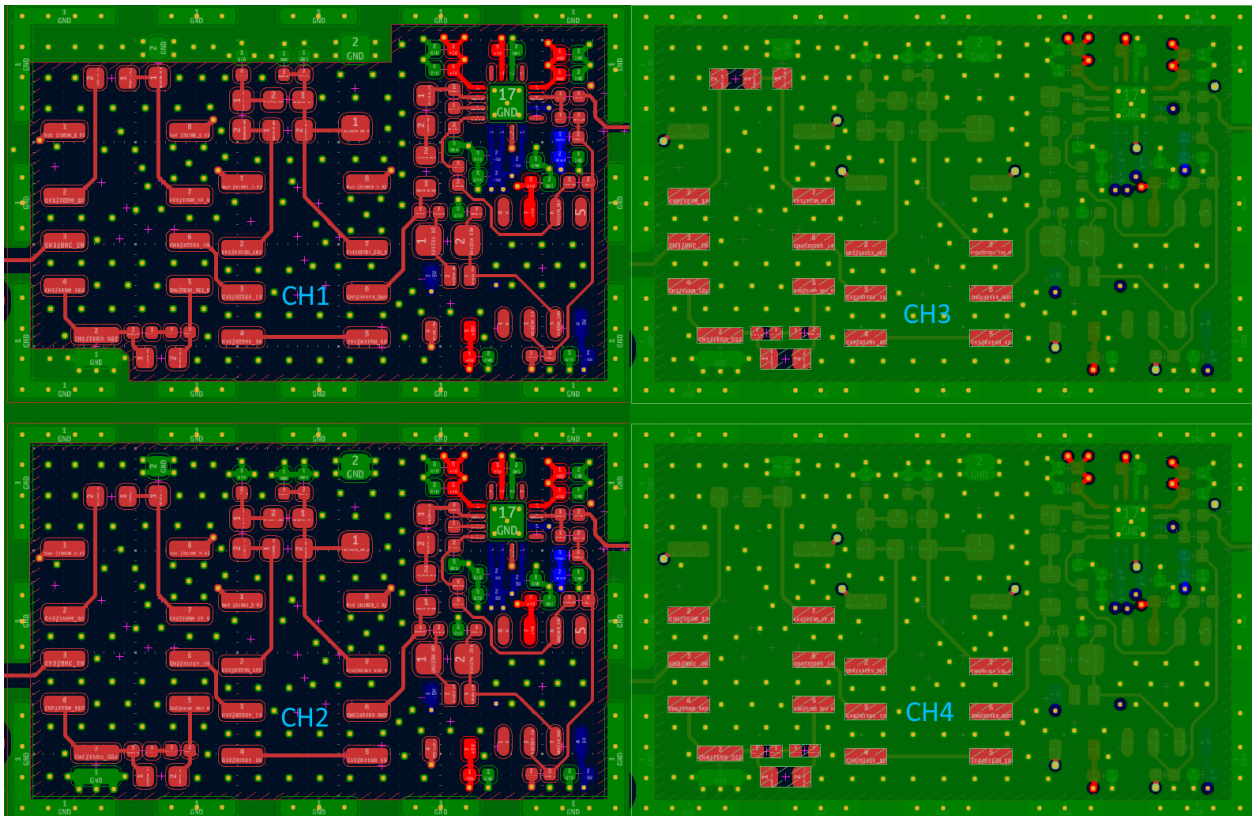
I didn't expect it to take that long, but then again this is the most effort I've ever put into a PCB design - it just had to be perfect!



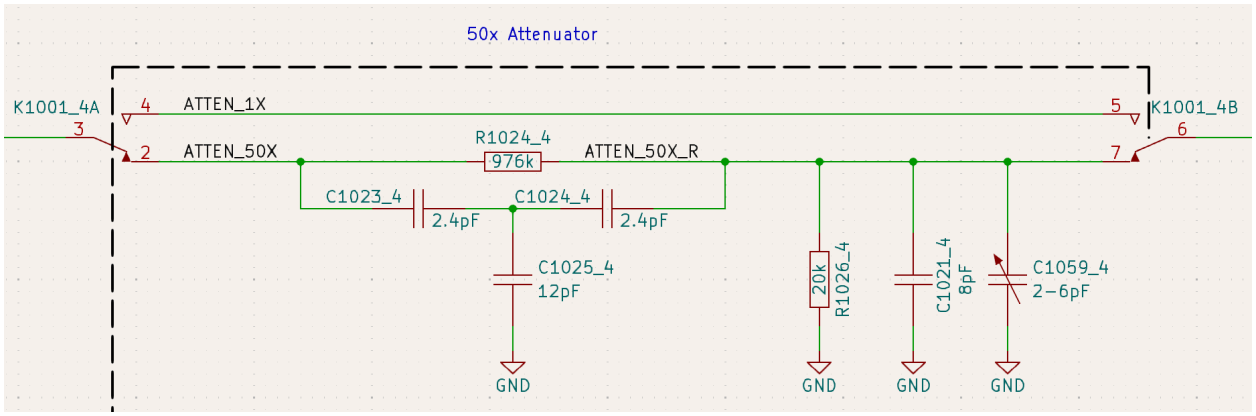
High effort silkscreen aside, I'm especially proud of fitting the ADC, Clock Generator, FPGA and all their power supplies under the heatsink. I added spring clips so the heatsink can function as a shield for the whole acquisition section as well. Here's some WIP progress pictures from when I first placed everything (left) and some point into the layout (right).



I also made the four front ends ever so slightly different from one another to test to see how the cutouts and grounding affect the elusive attenuator circuit. CH1 has a solid pour to all the components, while the other channels do not. CH3 and CH4 have progressively fewer ground plane cutouts than CH2. I've also via stitched the front end as I think that may have caused the wobbliness in the frequency response as dropping down a few layers causes the ground reference to change, and without vias nearby, the return current will have a hard time making it there.



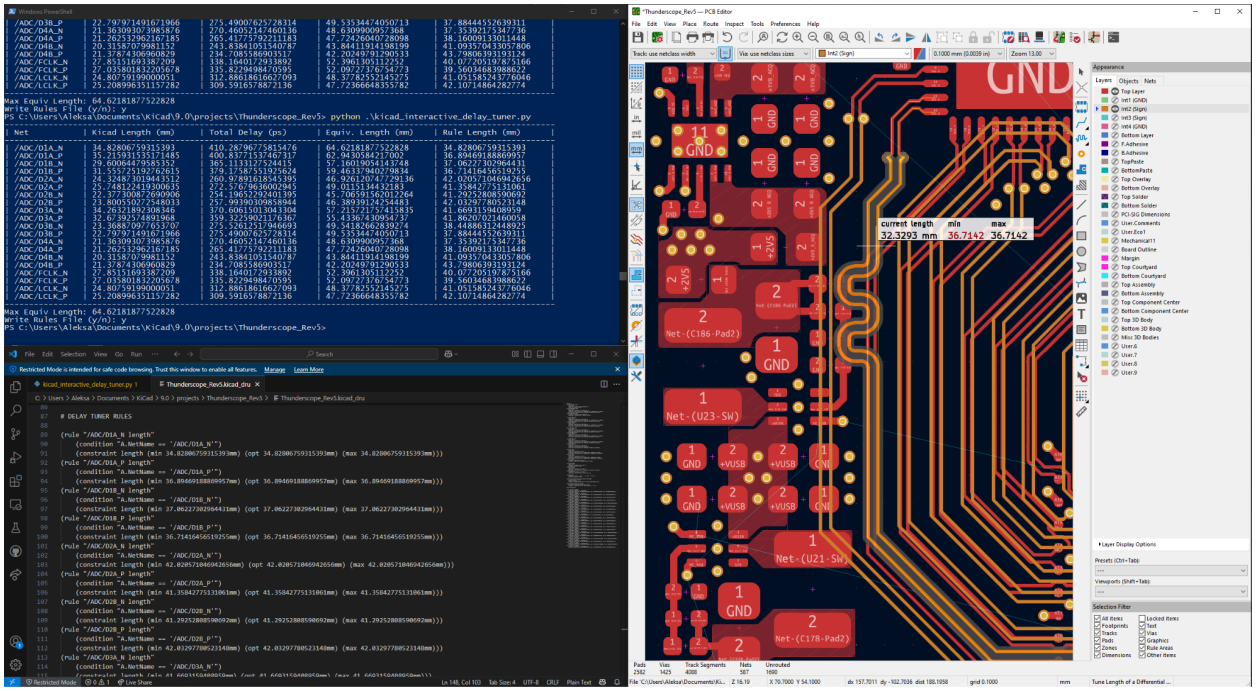
The other change in the front end is the (re)addition of a trim cap (C1059). Since the buffer's capacitance can vary from part to part, we want to trim it to a known level. This capacitance is about 2.4pF, and variation in it will be sub 1 pF. This wasn't much compared to the >100pF lower leg of the attenuator in previous designs, but with this new improved design we need to worry about it again. Trade-offs, trade-offs everywhere!



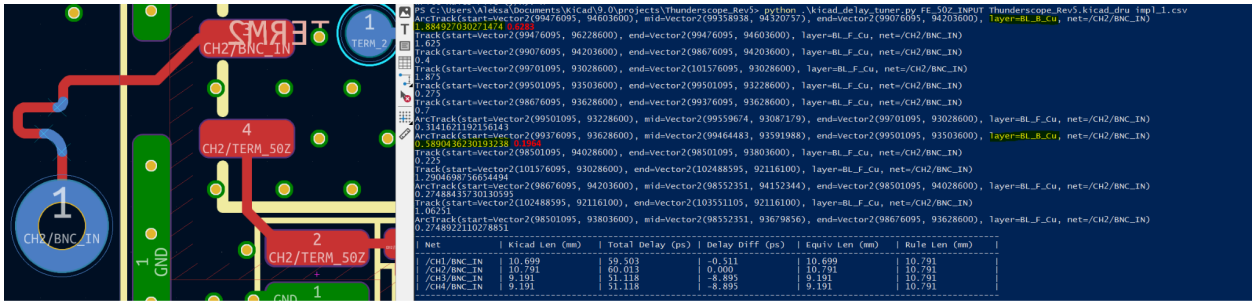
Teaching KiCad a New Trick - Matching Delays

As of time of writing, KiCad only understands the length of traces and pins. When length matching, it takes length as a single number added up across every layer. This leads to delay mismatches, as the signals on the inner layers are slower than the signals on the outer layers. When assigning pin lengths, you need to arbitrarily choose a layer to convert a delay value (given by the manufacturer), to a length. This also results in delay mismatches.

I wanted to do this right, just like Altium does, but I didn't want to have to calculate and add up all the delay values by hand in a spreadsheet. So I made a script to rewrite custom design rules to try to get KiCad's length matching to be delay matching (including pad delays).



It was only slightly off from KiCad's reported lengths, ok not bad, we just need consistency from trace to trace, not absolute accuracy. But then as soon as I added a curved tuning pattern it all fell apart.



I found out it was miscounting certain segments because of a small math error (normalizing the angle to [0,2*pi] when it should be [0,pi]) and got it working again! Below is the output of the script when tuning the skews on the PCIe lanes.

Net	Kicad Len (mm)	Total Delay (ps)	Delay Diff (ps)	Equiv Len (mm)	Rule Len (mm)
/FPGA/MGT_RX0_N	14.950	119.496	-6.633	21.486	16.143
/FPGA/MGT_RX0_P	15.989	126.129	0.000	22.679	15.989
/FPGA/MGT_RX1_N	18.156	139.948	-0.735	25.164	18.289
/FPGA/MGT_RX1_P	18.270	140.684	0.000	25.296	18.270
/FPGA/MGT_RX2_N	12.872	106.225	-6.560	19.100	14.051
/FPGA/MGT_RX2_P	13.898	112.785	0.000	20.280	13.898
/FPGA/MGT_RX3_N	26.076	190.492	-12.121	34.252	28.255
/FPGA/MGT_RX3_P	27.975	202.613	0.000	36.431	27.975
/FPGA/MGT_TX0_N	8.083	59.146	-5.678	10.635	9.104
/FPGA/MGT_TX0_P	9.104	64.824	0.000	11.656	9.104
/FPGA/MGT_TX1_N	8.249	60.067	-5.678	10.801	9.270
/FPGA/MGT_TX1_P	9.270	65.745	0.000	11.822	9.270
/FPGA/MGT_TX2_N	8.933	63.873	-5.177	11.485	9.864
/FPGA/MGT_TX2_P	9.864	69.050	0.000	12.416	9.864
/FPGA/MGT_TX3_N	9.494	66.990	-5.177	12.045	10.424
/FPGA/MGT_TX3_P	10.424	72.166	0.000	12.976	10.424
/MGT_CLK1_N	14.089	114.001	-4.300	20.498	14.862
/MGT_CLK1_P	14.763	118.301	0.000	21.271	14.763
/TS-PCIe Components/PCIe_PER0_N	27.124	150.852	0.000	27.124	27.124
/TS-PCIe Components/PCIe_PER0_P	27.124	150.852	0.000	27.124	27.124
/TS-PCIe Components/PCIe_PER1_N	25.882	143.941	0.000	25.882	25.882
/TS-PCIe Components/PCIe_PER1_P	25.882	143.941	-0.000	25.882	25.882
/TS-PCIe Components/PCIe_PER2_N	25.053	139.333	0.000	25.053	25.053
/TS-PCIe Components/PCIe_PER2_P	25.053	139.333	0.000	25.053	25.053
/TS-PCIe Components/PCIe_PER3_N	24.225	134.726	0.000	24.225	24.225
/TS-PCIe Components/PCIe_PER3_P	24.225	134.726	0.000	24.225	24.225
/TS-PCIe Components/PCIe_PET0_N	35.392	196.834	-0.000	35.392	35.392
/TS-PCIe Components/PCIe_PET0_P	35.392	196.834	0.000	35.392	35.392
/TS-PCIe Components/PCIe_PET1_N	32.750	182.138	0.000	32.750	32.750
/TS-PCIe Components/PCIe_PET1_P	32.750	182.138	-0.000	32.750	32.750
/TS-PCIe Components/PCIe_PET2_N	30.500	169.625	-0.000	30.500	30.500
/TS-PCIe Components/PCIe_PET2_P	30.500	169.625	0.000	30.500	30.500
/TS-PCIe Components/PCIe_PET3_N	28.257	157.151	-0.000	28.257	28.257
/TS-PCIe Components/PCIe_PET3_P	28.257	157.151	0.000	28.257	28.257
/TS-PCIe Components/PCIe_REFCLK_N	27.539	153.155	0.000	27.539	27.539
/TS-PCIe Components/PCIe_REFCLK_P	27.539	153.155	0.000	27.539	27.539
/TS-USB4 Components/M2_PER0_N	35.781	251.167	-5.851	45.162	36.833
/TS-USB4 Components/M2_PER0_P	36.732	257.018	0.000	46.214	36.732
/TS-USB4 Components/M2_PER1_N	29.848	213.307	-5.768	38.354	30.885
/TS-USB4 Components/M2_PER1_P	30.786	219.075	0.000	39.391	30.786
/TS-USB4 Components/M2_PER2_N	22.779	168.195	-5.862	30.243	23.833
/TS-USB4 Components/M2_PER2_P	23.732	174.057	0.000	31.297	23.732
/TS-USB4 Components/M2_PER3_N	16.790	129.984	-5.862	23.372	17.844
/TS-USB4 Components/M2_PER3_P	17.744	135.846	0.000	24.426	17.744
/TS-USB4 Components/M2_PET0_N	31.141	173.190	0.000	31.141	31.141
/TS-USB4 Components/M2_PET0_P	31.141	173.189	-0.000	31.141	31.141
/TS-USB4 Components/M2_PET1_N	23.902	132.929	0.000	23.902	23.902
/TS-USB4 Components/M2_PET1_P	23.902	132.928	-0.000	23.902	23.902
/TS-USB4 Components/M2_PET2_N	16.957	94.303	0.000	16.957	16.957
/TS-USB4 Components/M2_PET2_P	16.956	94.303	-0.000	16.956	16.957
/TS-USB4 Components/M2_PET3_N	8.466	47.086	-5.857	8.466	9.519
/TS-USB4 Components/M2_PET3_P	9.519	52.942	0.000	9.519	9.519
/TS-USB4 Components/M2_REFCLK_N	41.749	289.249	-5.851	52.009	42.801
/TS-USB4 Components/M2_REFCLK_P	42.700	295.100	0.000	53.061	42.700

The rewriting design rules bit doesn't work all that well given the slight discrepancy with the KiCad reported lengths and the whole delay to length conversion just assuming top layer for everything. However, if you just look at the delay deltas then it's pretty usable for tuning! In fact, I did all the delay matching on TS with this tool. If you want to try it yourself, I've put the script up in its own separate repo.

Next Steps, Accountability, and New Shipping Estimates

Now to address the elephant in the room, we won't be shipping on time. The new interposer design, switch to KiCad and some personal issues all contributed to this. I take full responsibility and am committed to getting this done as quickly as possible while still holding myself and the project to the highest standards. So first things first, what are the next steps?

Hand Build Rev 5 - Boards arrive at the end of April and I expect to get them built within a day or two of receiving them.

Test Rev 5 - This should take no longer than 2 weeks.

Once these are done, I can roll any minor changes into a Rev 5.1. If there are any major changes needed, however unlikely, I will repeat the above process with this new rev.

Next up,

Get Dev Edition PCBs Assembled - send the design to a CM and wait a month or so

Build Test Fixtures and Assembly Jigs - use the time the CM is working on the PCBAs

Test and Ship Dev Edition units - these should reach backers in July

A month after shipping Dev Edition units (to give time for any last bugs to be reported), we'll do the same process as above for the rest of the units. We can improve our fixtures and jigs while the boards are out for fab and assembly and should ship out in September.

To keep myself accountable, I will be using GitHub Issues to publicly track the tasks left before shipping, so check those out if you're ever wondering how things are going between updates. Or you can ask me directly through the project question form on CS, on Discord (bridged to #thunderscope:matrix.org on matrix or #thunderscope:libera.chat on IRC), or on Mastodon!

I will also be sending out another update right after we test Rev 5, just to confirm the timeline for you all. Looking forward to sharing the results of a whirlwind week of testing!

-Aleksa