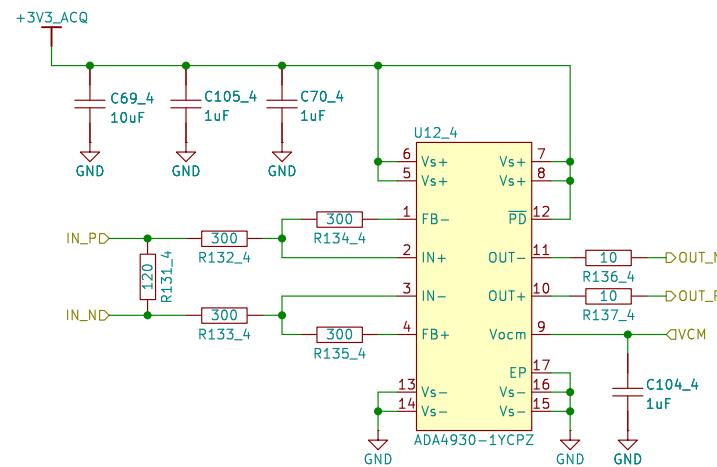


ADC Driver**EEVengers**

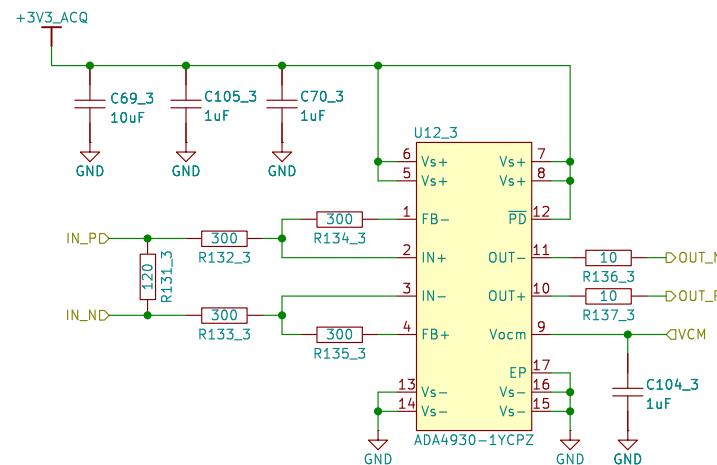
Sheet: /ADC Driver 4/
File: ADC_Driver.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 9.0.3

Drawn by: Aleksa Bjelogrlic

Rev: 5.3
Id: 3/20

ADC Driver**EEVengers**

Sheet: /ADC Driver 3/
File: ADC_Driver.kicad_sch

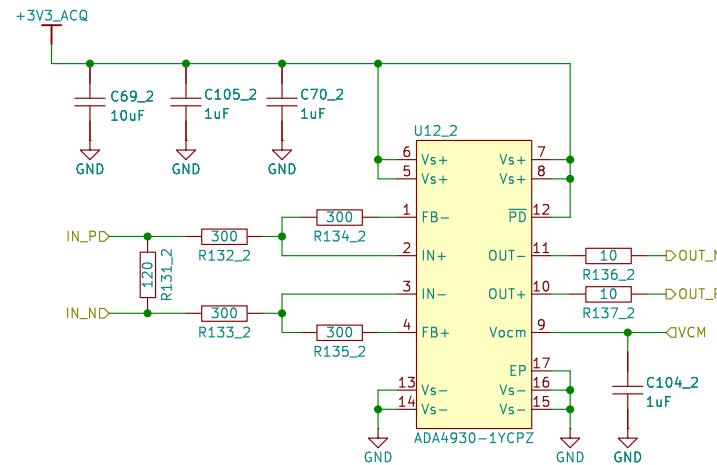
Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 9.0.3

Drawn by: Aleksa Bjelogrlic

Rev: 5.3
Id: 3/20

ADC Driver



EEVengers

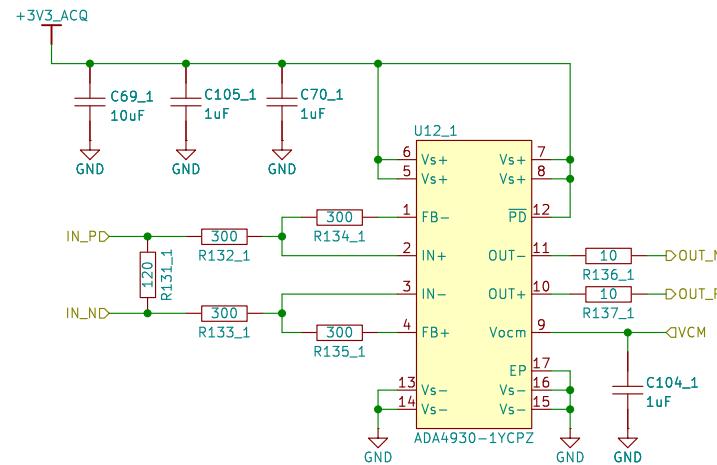
Sheet: /ADC Driver 2/
File: ADC_Driver.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 9.0.3

Drawn by: Aleksa Bjelogrlic

Rev: 5.3
Id: 3/20

ADC Driver**EEVengers**Sheet: /ADC Driver 1/
File: ADC_Driver.kicad_sch**Title: ThunderScope**Size: A4 Date:
KiCad E.D.A. 9.0.3

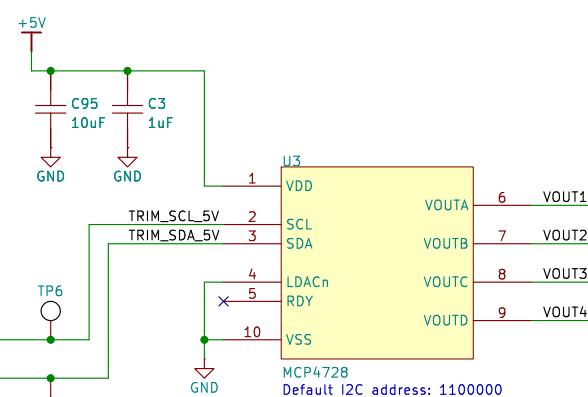
Drawn by: Aleksa Bjelogrlic

Rev: 5.3
Id: 3/20

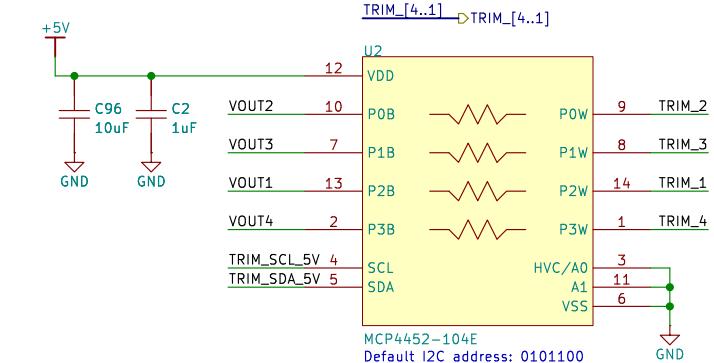
1 2 3 4 5 6

Offset Voltage Trim and User Offset Control

A

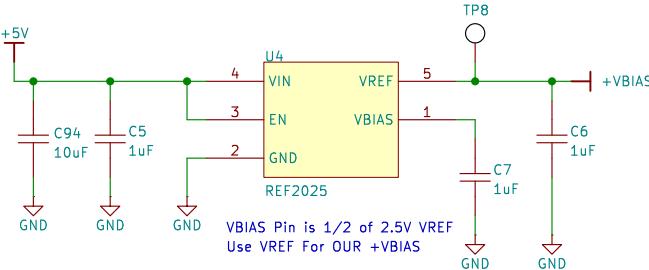


B

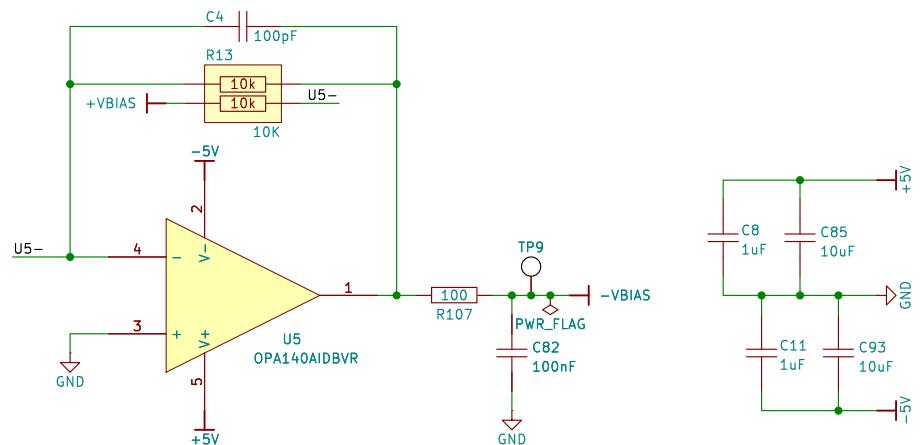


Bias Voltage Generation

C



D



EEVengers

Sheet: /Front End Trim and Bias/
File: FE.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 9.0.3

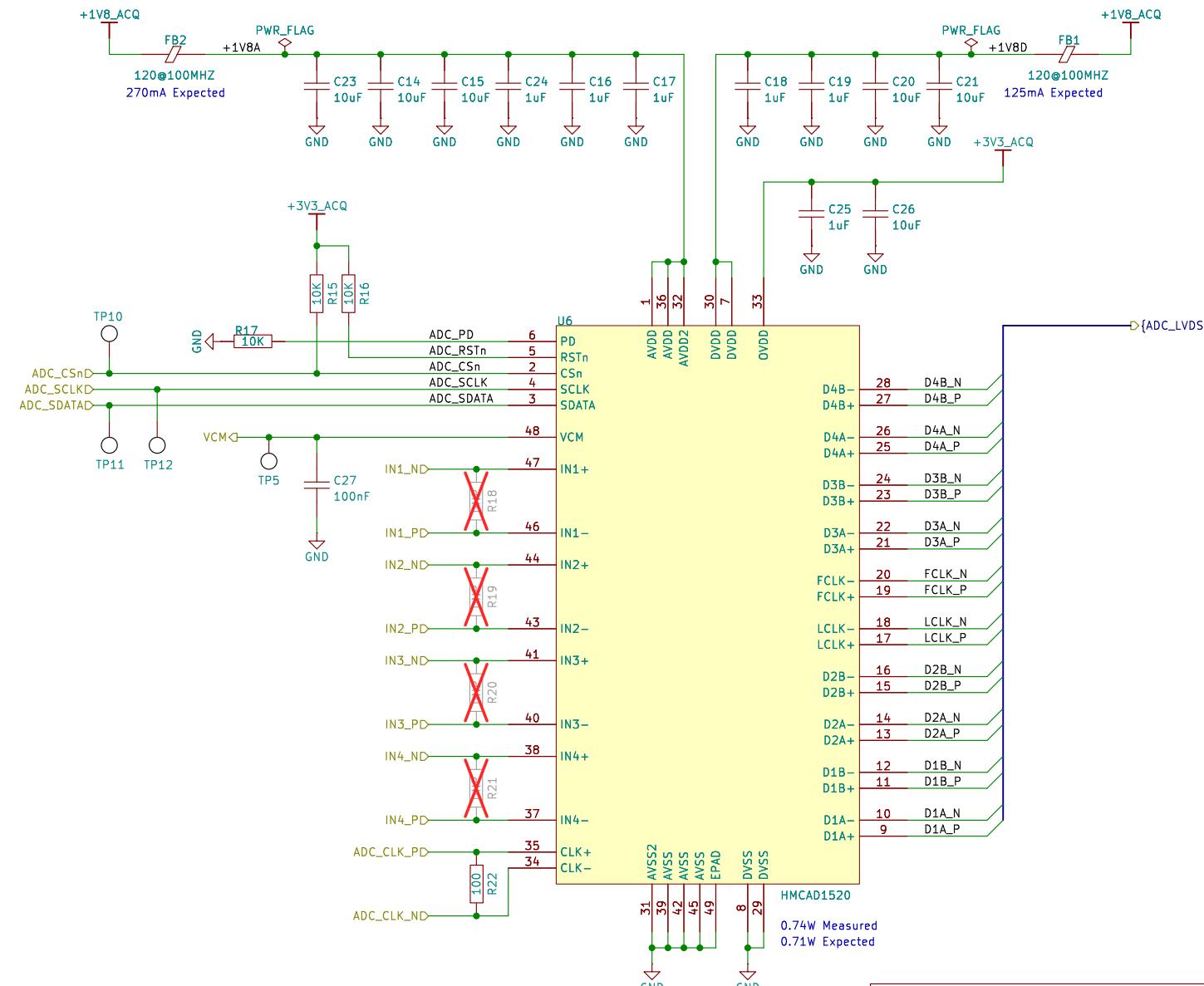
Drawn by: Aleksa Bjelogrlic

Rev: 5.3

Id: 4/20

1 2 3 4 5 6

1 2 3 4 5 6

ADC

EEVengers

Sheet: /ADC/
File: ADC.kicad_sch

Drawn by: Aleksa Bjelogrlic

Title: ThunderScope

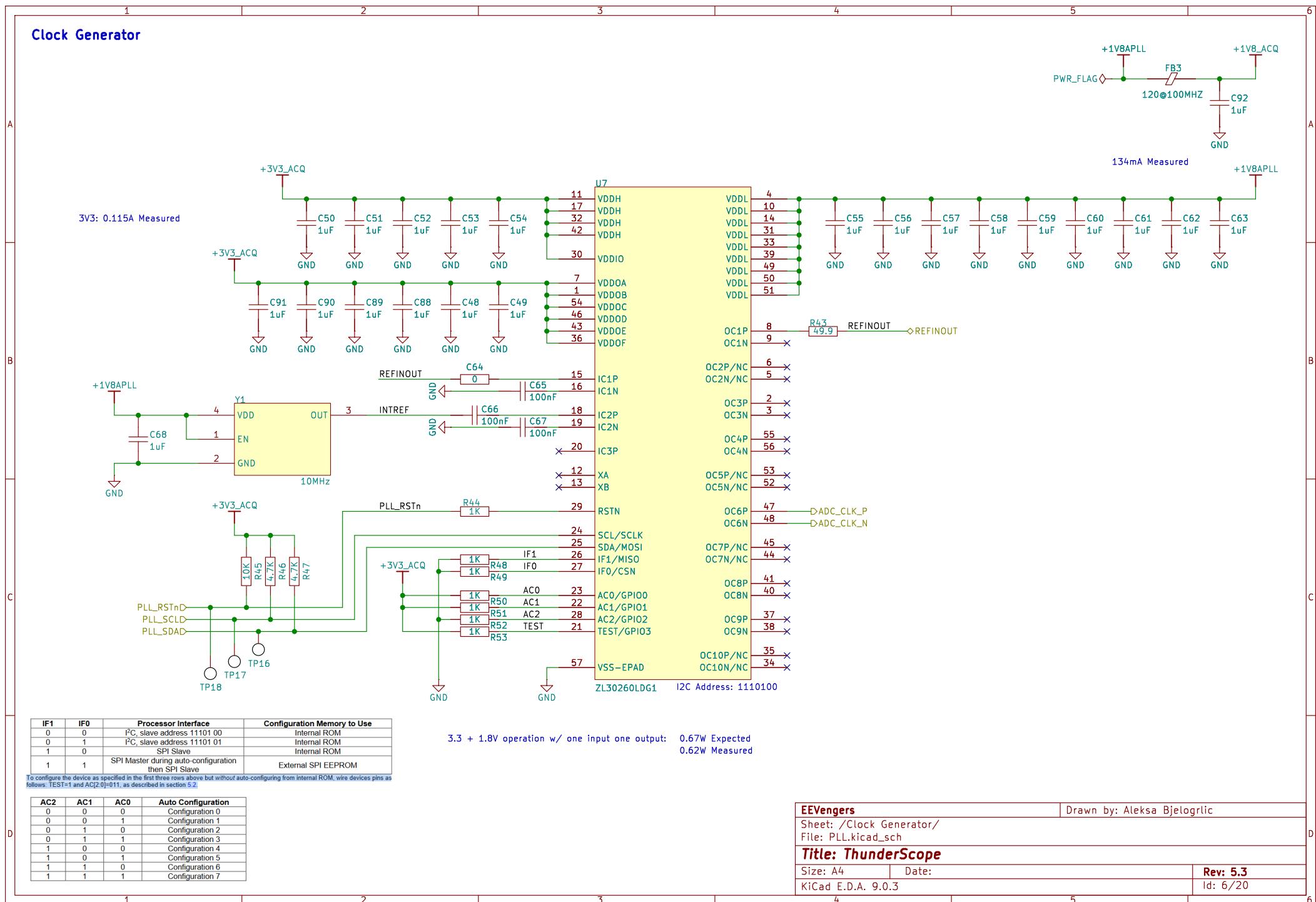
Size: A4 Date:

KiCad E.D.A. 9.0.3

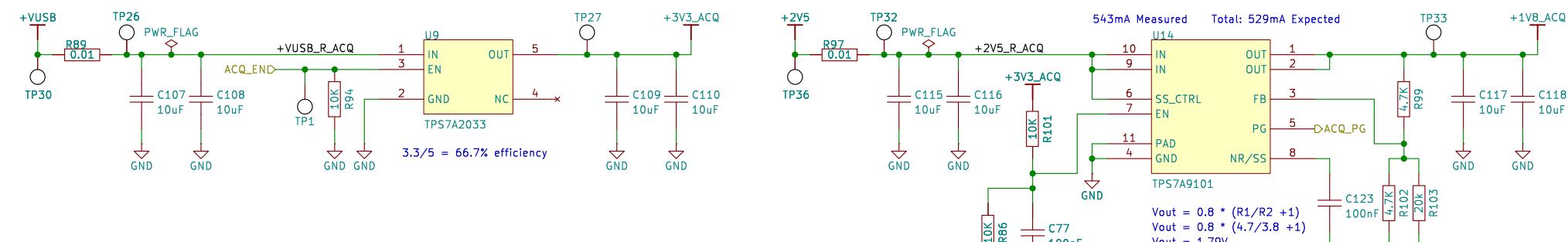
Rev: 5.3

Id: 5/20

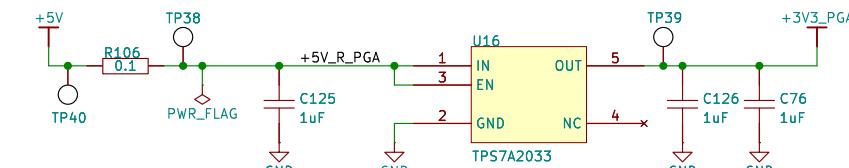
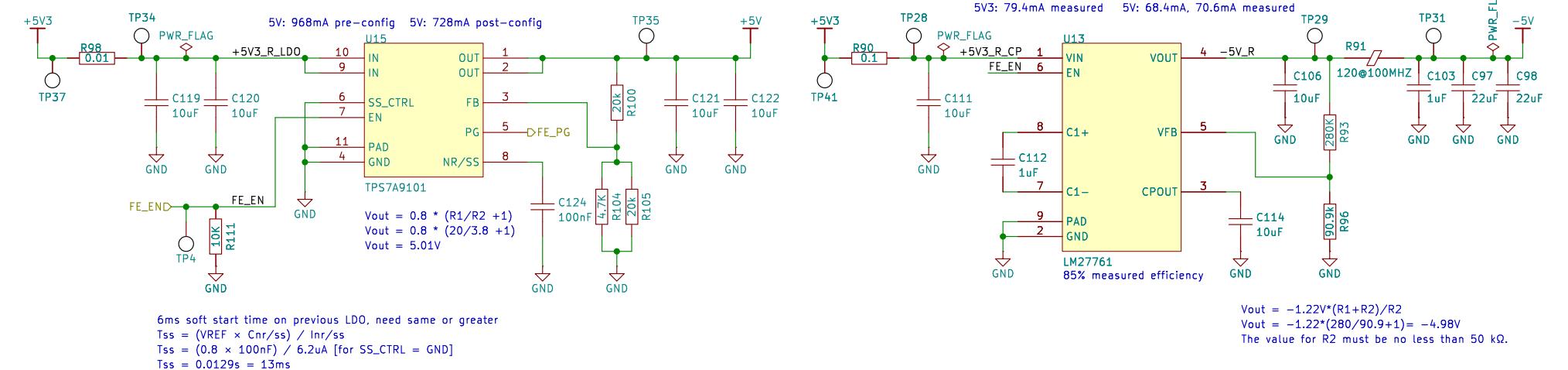
1 2 3 4 5 6



Acquisition Voltage Regulators



Front End Voltage Regulators



EEVengers

Sheet: /ACQ and FE Voltage Regs/
File: ACQ_FE_VREG.sch

Title: ThunderScope

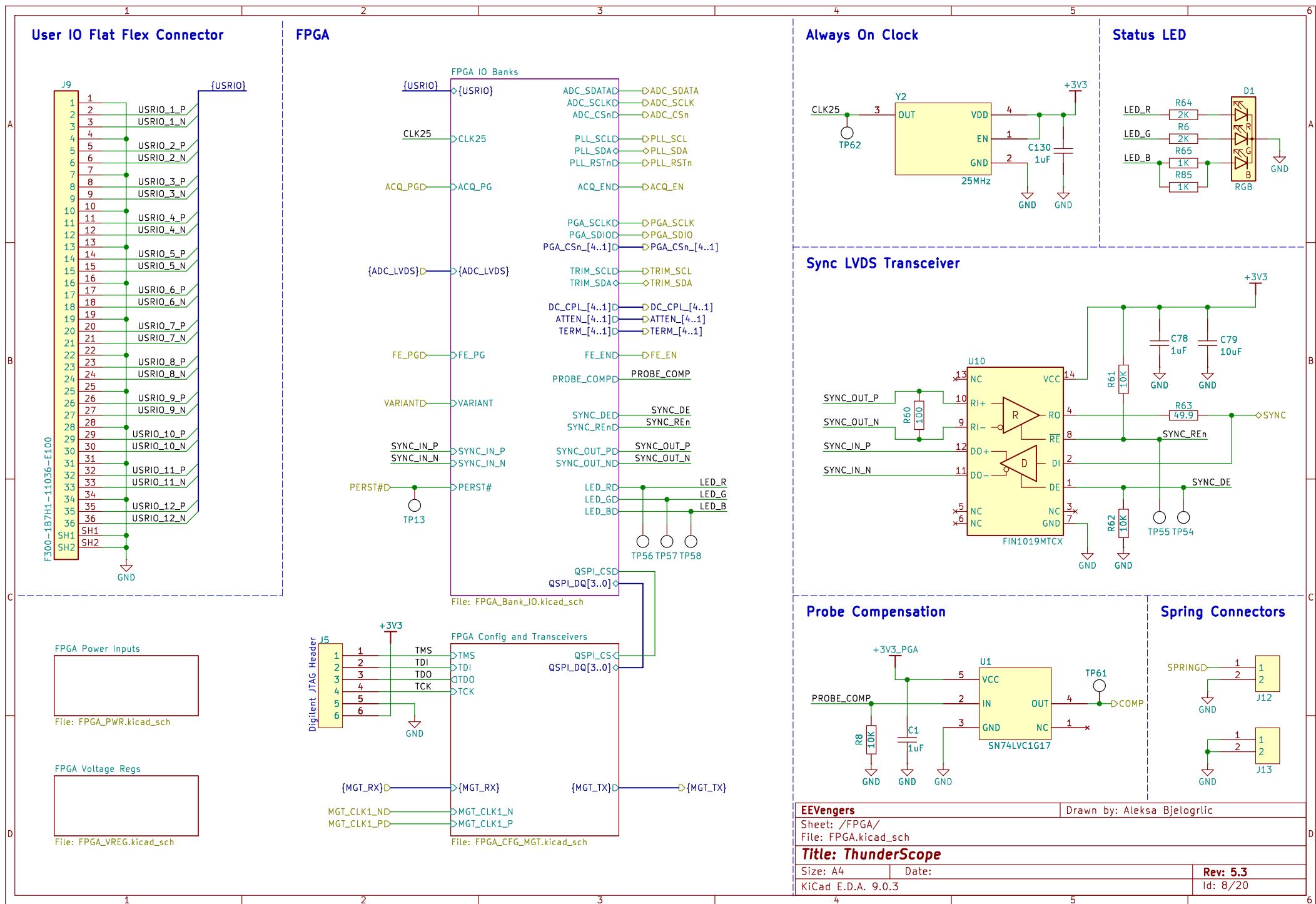
Size: A4 Date:

KiCad E.D.A. 9.0.3

Drawn by: Aleksa Bjelogrlic

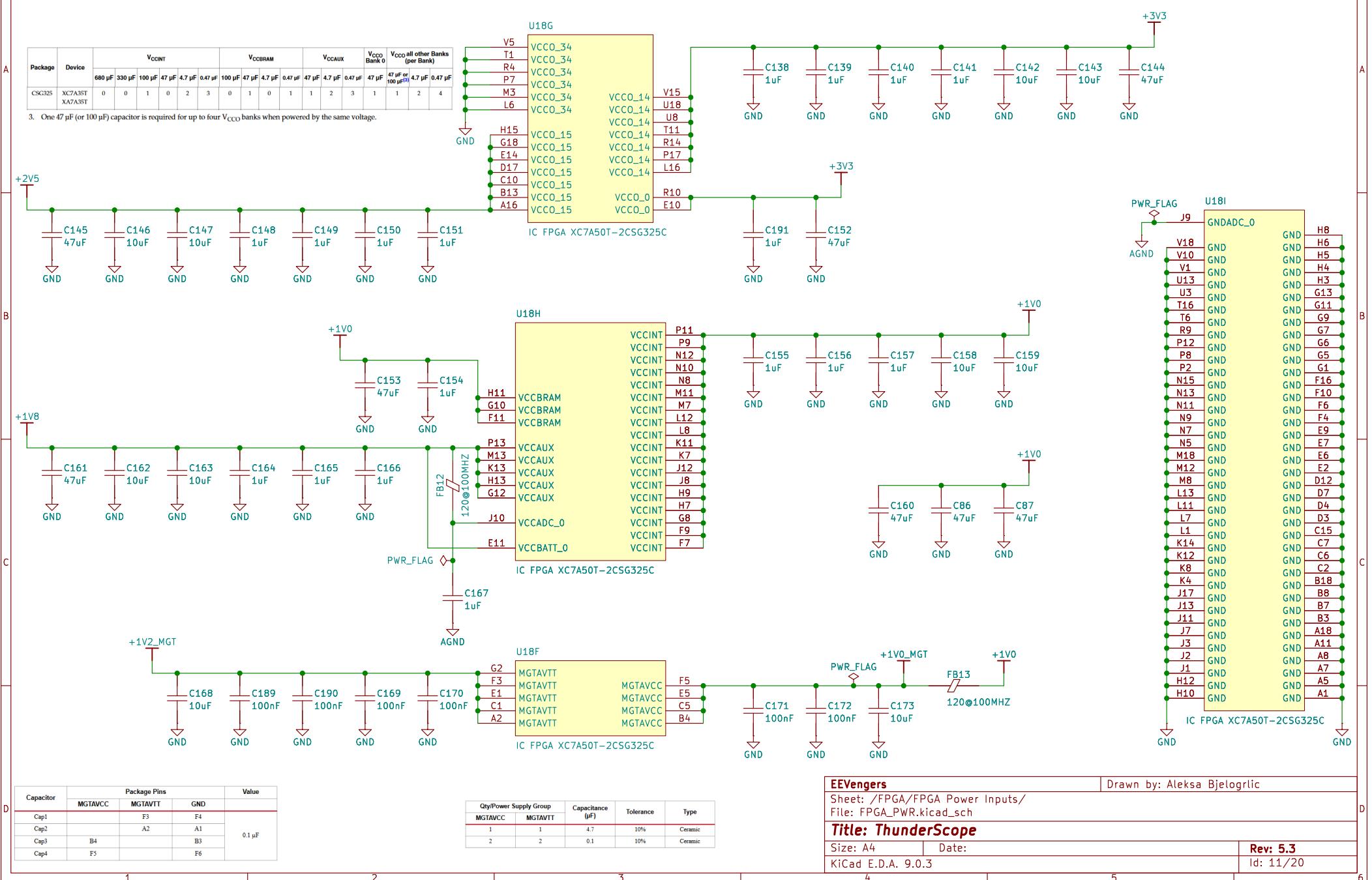
Rev: 5.3

Id: 7/20



1 2 3 4 5 6

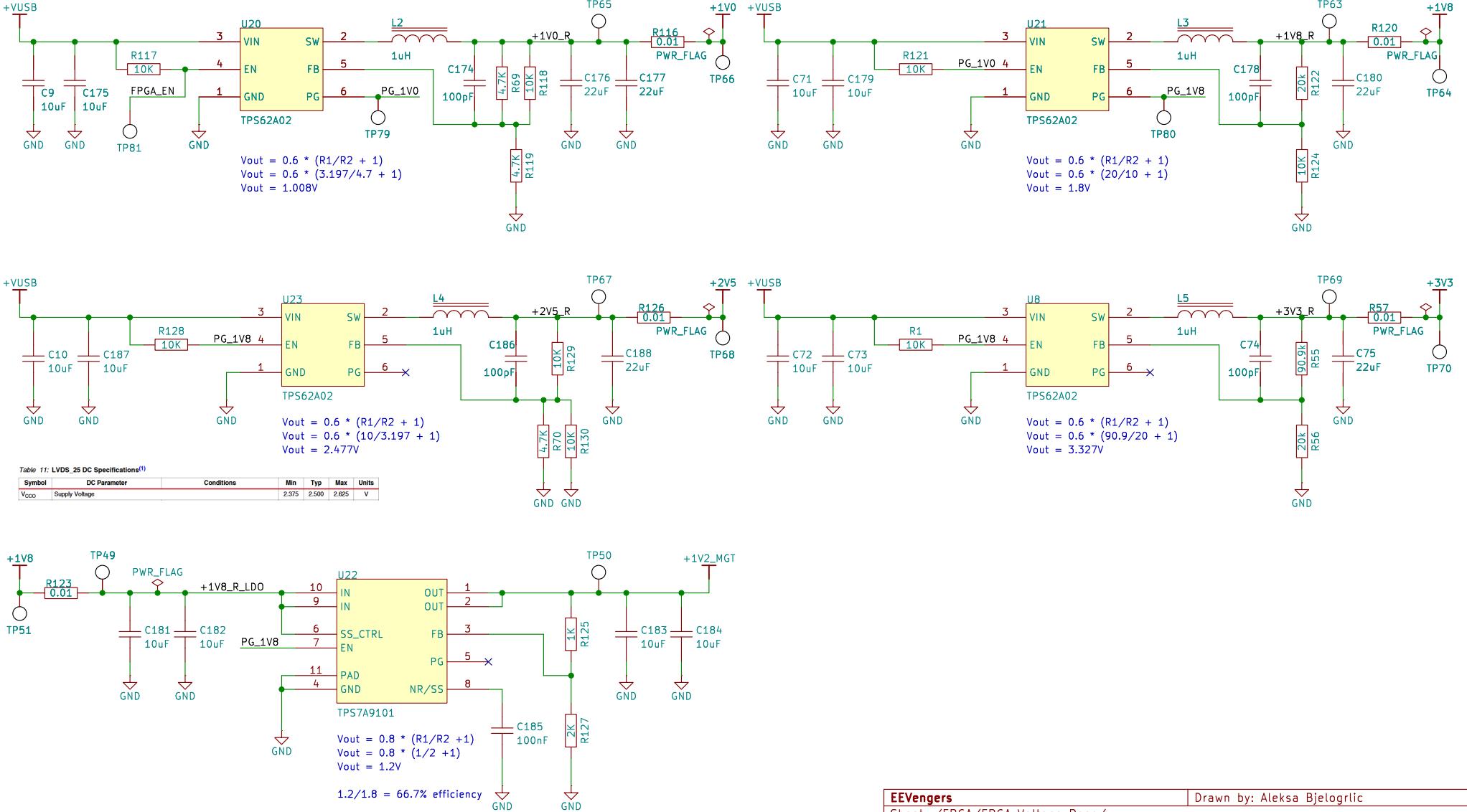
FPGA Power Inputs



1 2 3 4 5 6

FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V



EEVengers

Sheet: /FPGA/FPGA Voltage Regs/
File: FPGA_VREG.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 9.0.3

Drawn by: Aleksa Bjelogrlic

Rev: 5.3

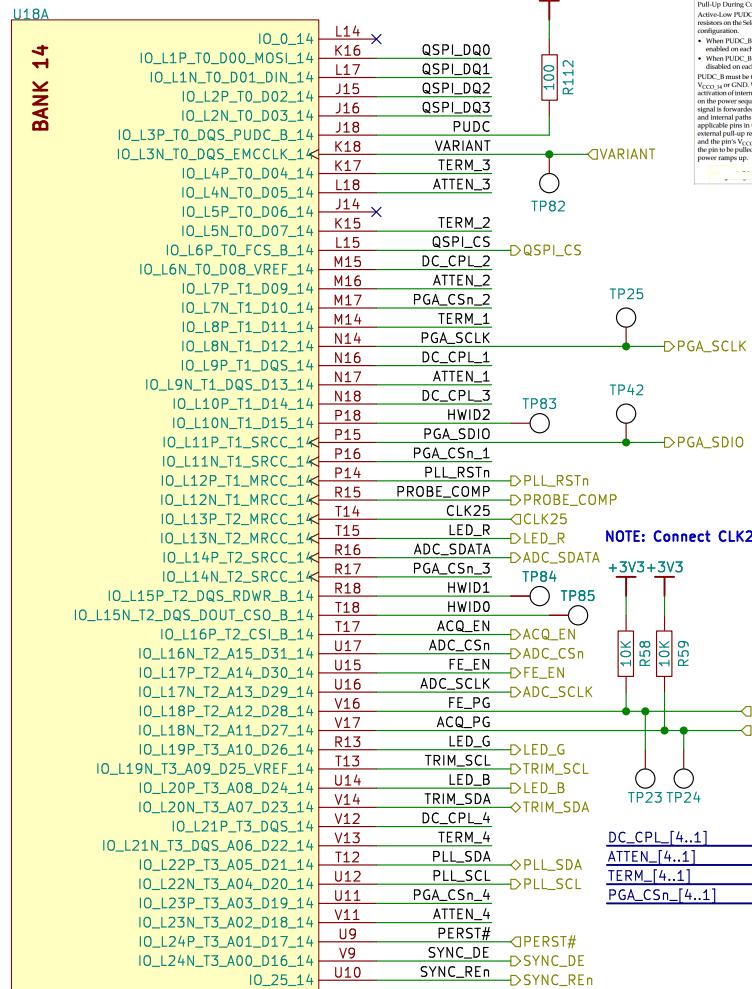
Id: 12/20

1 2 3 4 5 6

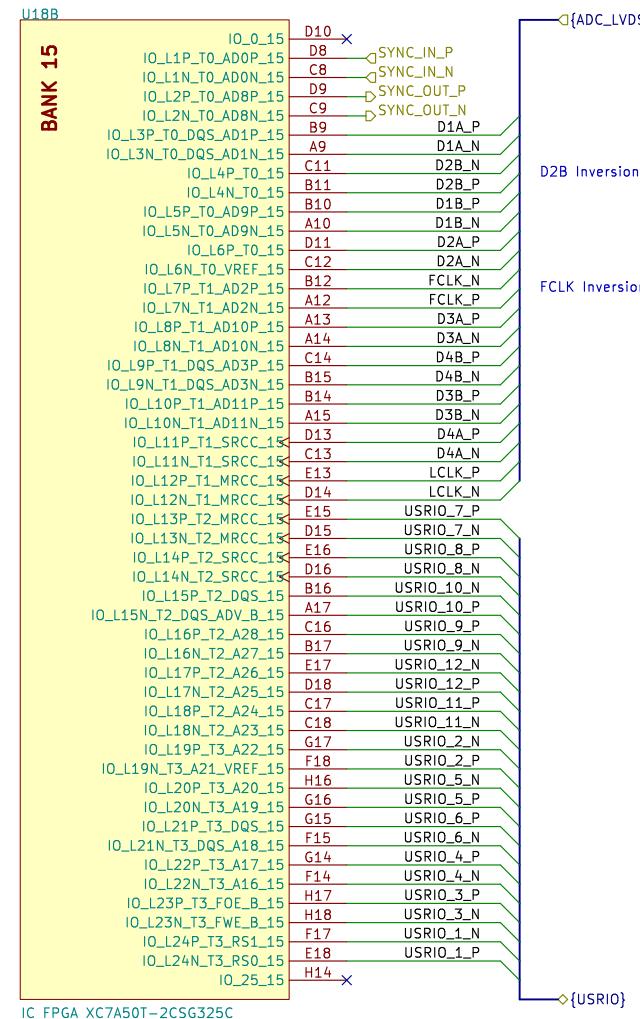
FPGA IO Banks

QSPI_DQ[3..0] → QSPI_DQ[3..0]

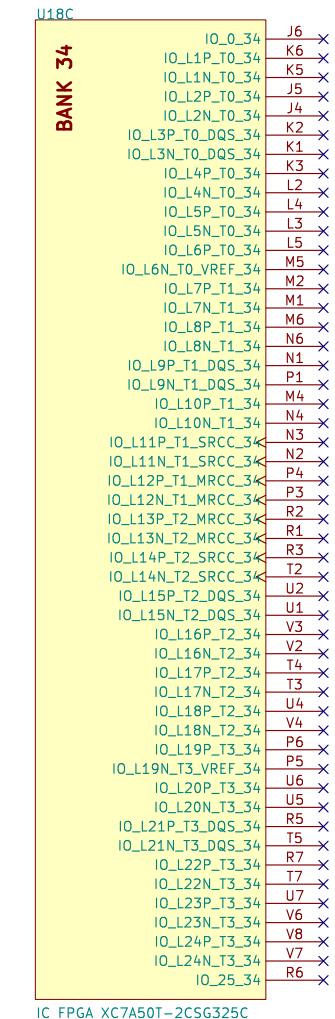
Full TP Coverage on Bank 14 Signals (except PUDC)



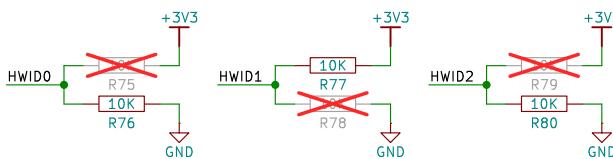
IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C

**EEVengers**

Sheet: /FPGA/FPGA IO Banks/
File: FPGA_Bank_IO.kicad_sch

Drawn by: Aleksa Bjelogrlic

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 9.0.3

Rev: 5.3

Id: 9/20

FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

Note: DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

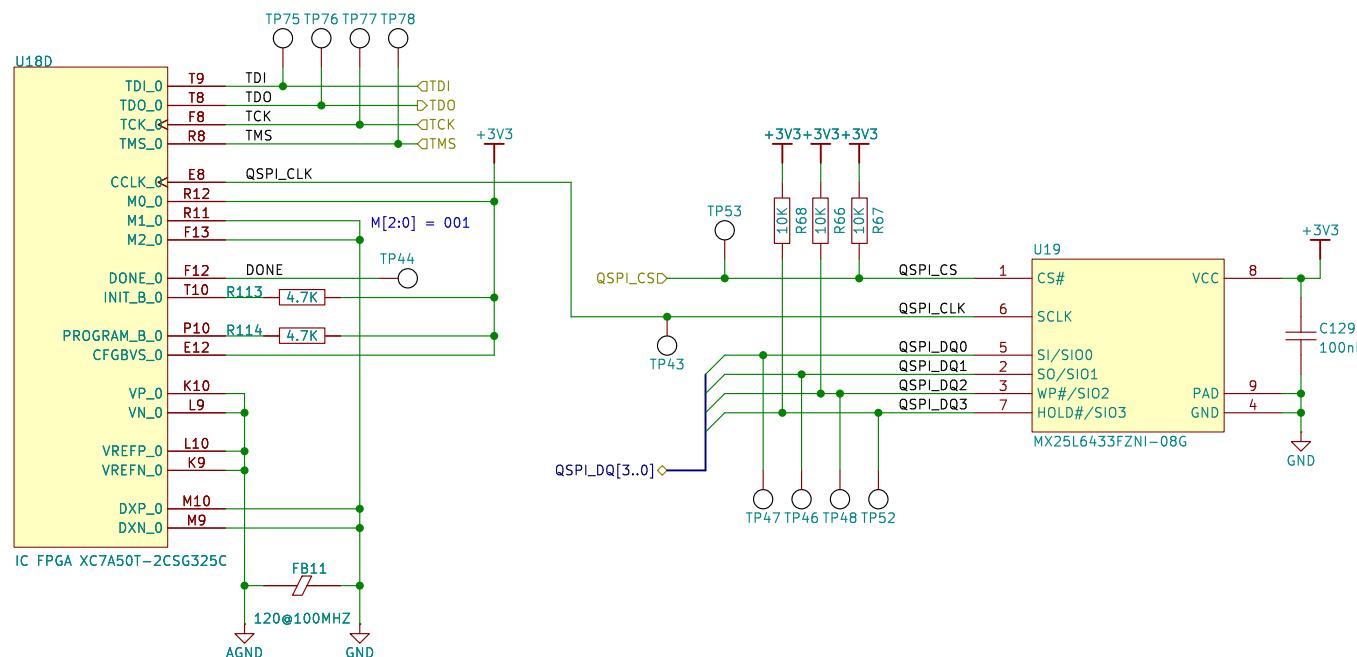
Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and

Table 2-1: 7 Series FPGA Configuration Modes				
Configuration Mode	M2[0]	Bus Width	CCLK Direction	
Master SPI	001	x1, x2, x4	Output	

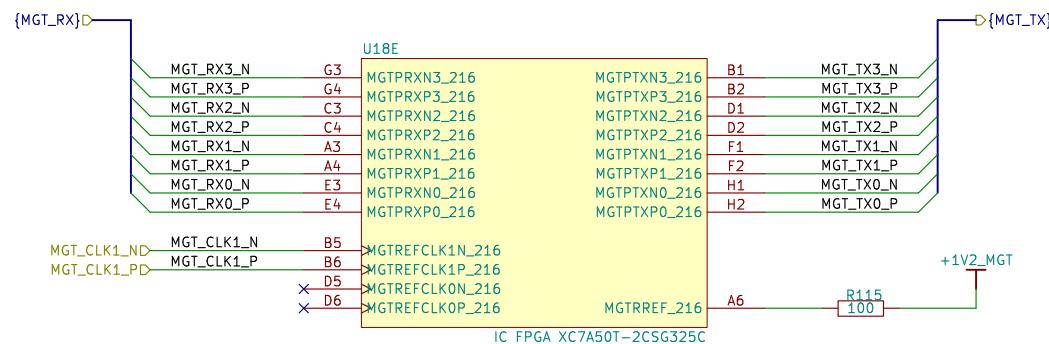
Table 2-2: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Banks Used	Configuration Interface I/O	HR Bank 0 V _{CCO}	HR Bank 14 V _{CCO}	HR Bank 15 V _{CCO}	CFGBVS
JTAG (only)	0	V _{PP}	3.3V	3.3V	Any	V _{CCO_0} , 0
		V _{REFP_0}	2.5V	2.5V	Any	V _{CCO_0} , 0
		V _{REFN_0}	1.8V	1.8V	Any	GND
		V _{REFP_0}	1.5V	1.5V	Any	GND
Serial SPI or SelectMAP	0, 14 ⁽¹⁾	V _{PP}	3.3V	3.3V	3.3V	V _{CCO_0} , 0
		V _{REFP_0}	2.5V	2.5V	2.5V	V _{CCO_0} , 0
		V _{REFN_0}	1.8V	1.8V	1.8V	GND
		V _{REFP_0}	1.5V	1.5V	1.5V	GND
		V _{PP}	3.3V	3.3V	3.3V	V _{CCO_0} , 0
		V _{REFP_0}	2.5V	2.5V	2.5V	V _{CCO_0} , 0
		V _{REFN_0}	1.8V	1.8V	1.8V	GND
		V _{PP}	3.3V	3.3V	3.3V	V _{CCO_0} , 0
		V _{REFP_0}	2.5V	2.5V	2.5V	V _{CCO_0} , 0
		V _{REFN_0}	1.8V	1.8V	1.8V	GND
BPI ⁽²⁾	0, 14, 15	V _{PP}	3.3V	3.3V	3.3V	V _{CCO_0} , 0
		V _{REFP_0}	2.5V	2.5V	2.5V	V _{CCO_0} , 0
		V _{REFN_0}	1.8V	1.8V	1.8V	GND
		V _{PP}	3.3V	3.3V	3.3V	V _{CCO_0} , 0
		V _{REFP_0}	2.5V	2.5V	2.5V	V _{CCO_0} , 0

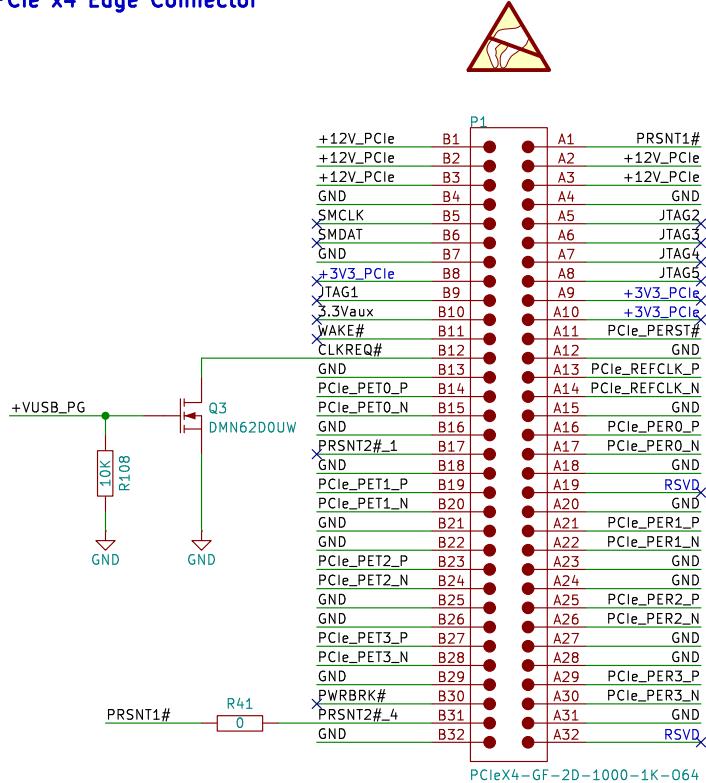
- Notes:
 1. RS1_0 for Multiboot or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.
 2. BPI mode is not available in the Spartan-7 family.



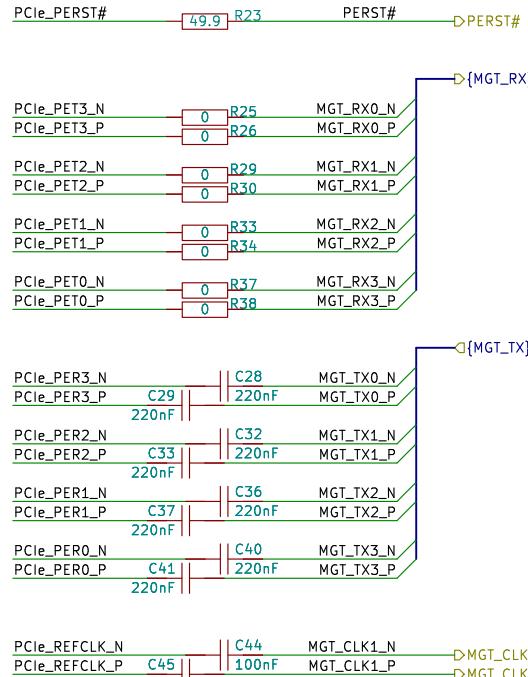
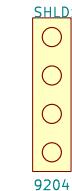
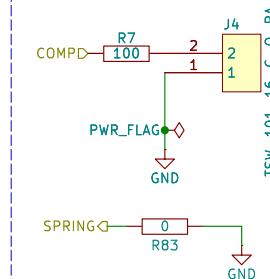
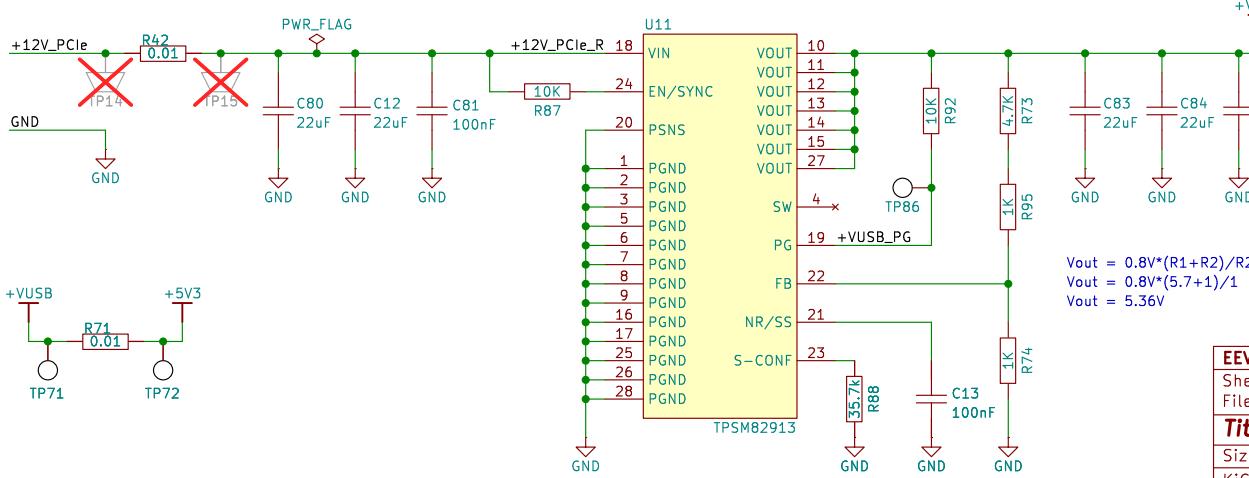
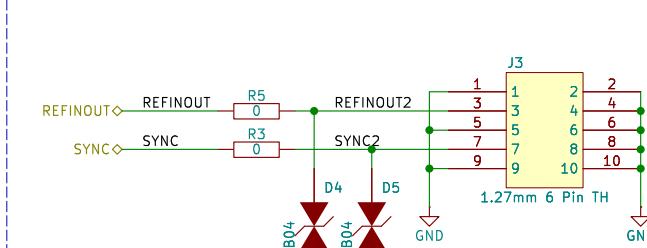
FPGA Transceivers



1 2 3 4 5 6

PCIe x4 Edge Connector

AC Couple PER Lines with 220nF
AC Couple REFCLK Lines with 100nF

**PCIe bracket****Variant Pin Strap****Probe Comp****5V3 Buck Converter****Refclock and Sync Header****EEVengers**

Sheet: /TS-PCIe Components/
File: CON_PCIe_X4.kicad_sch

Title: ThunderScope

Size: A4 Date:

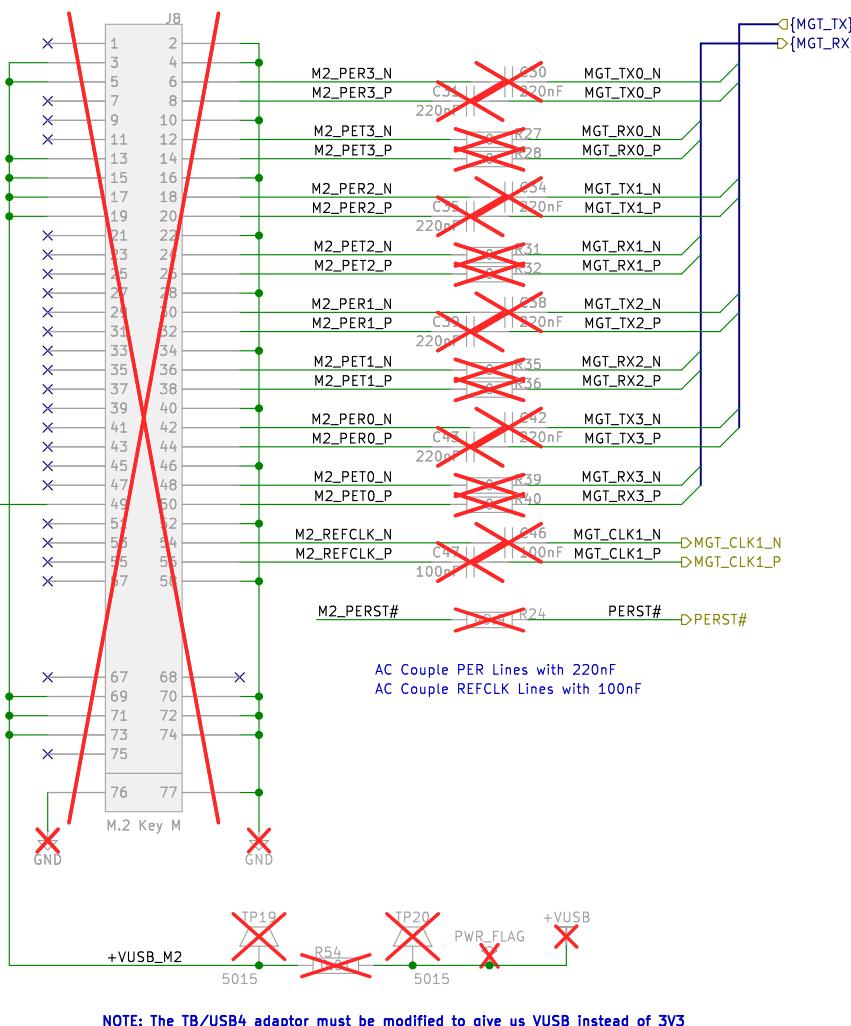
KiCad E.D.A. 9.0.3

Drawn by: Aleksa Bjelogrlic

Rev: 5.3

Id: 13/20

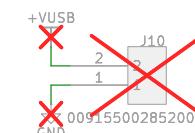
M.2 Key M Connector – Custom Pinout



Probe Comp

COMPD → R84 → D_{SPRING}

Fan Connector



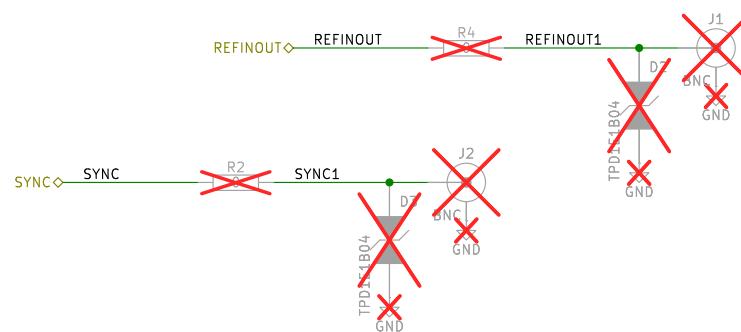
Ground Lug



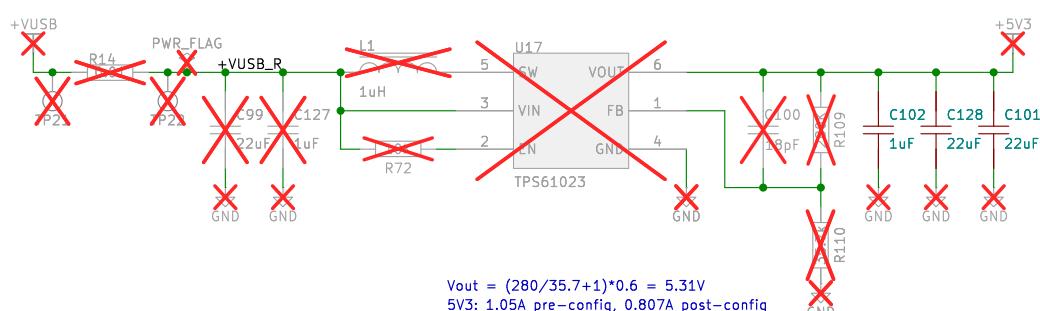
Variant Pin Strap



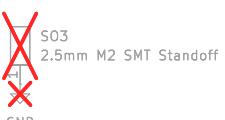
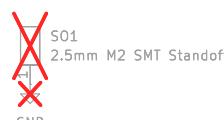
Refclock and Sync BNCs



5V3 Boost Converter



Interposer Standoffs



EEVengers	Drawn by: Aleksa Bjelogrlic
Sheet: /TS-USB4 Components/	
File: M2_KEY_M.kicad_sch	
Title: ThunderScope	
Size: A4	Date:
KiCad E.D.A. 9.0.3	Rev: 5.3
	Id: 14/20