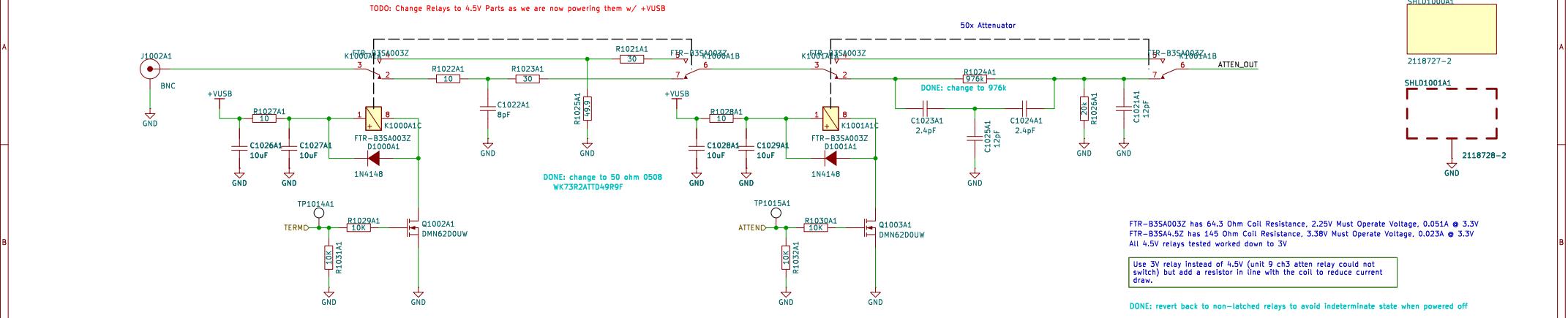
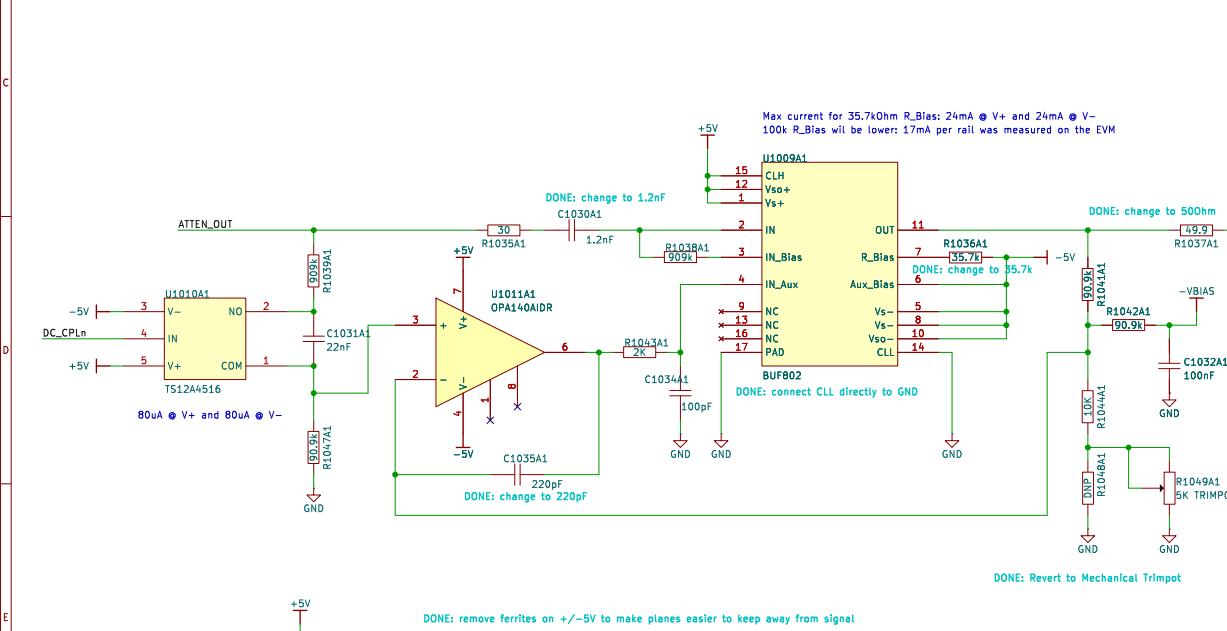


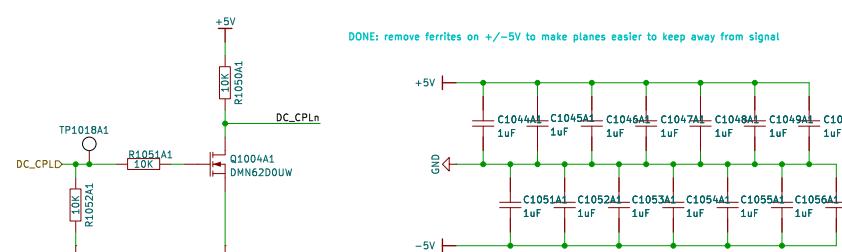
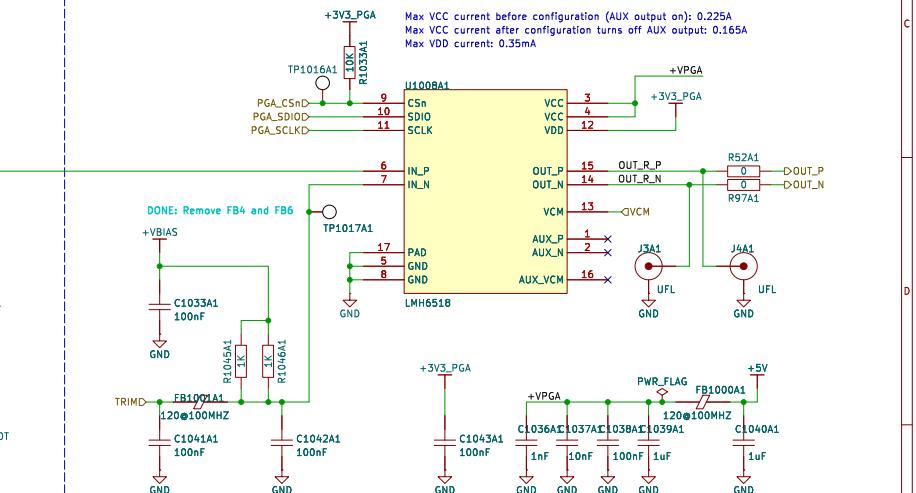
Termination and Attenuation



Input Buffer and AC/DC Coupling



Programmable Gain Amplifier



EEVengers

Sheet: /CH1/

File: FE_Channel.kicad_sch

Title: ThunderScope

Size: A3 Date:

KiCad E.D.A. 8.99.0-3402-gadd58faa30

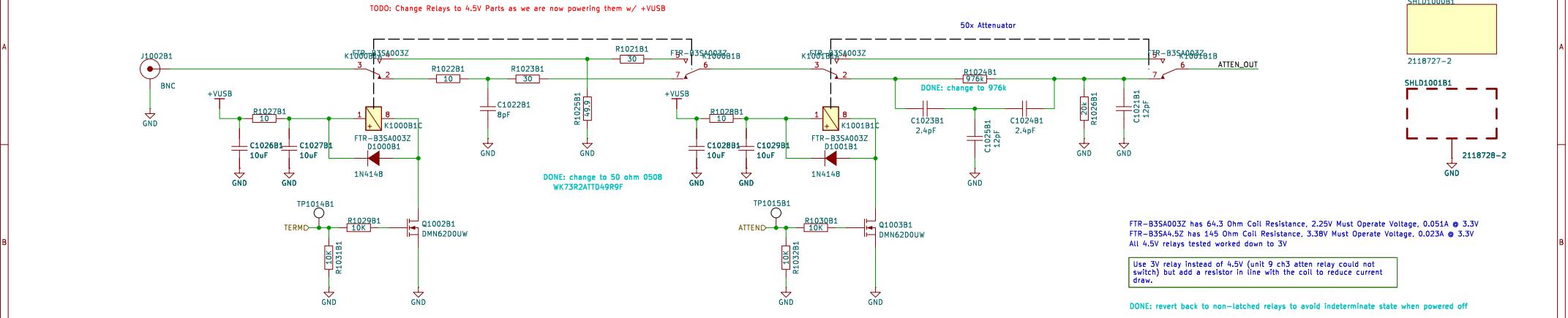


DONE: revert back to non-latched relays to avoid indeterminate state when powered off

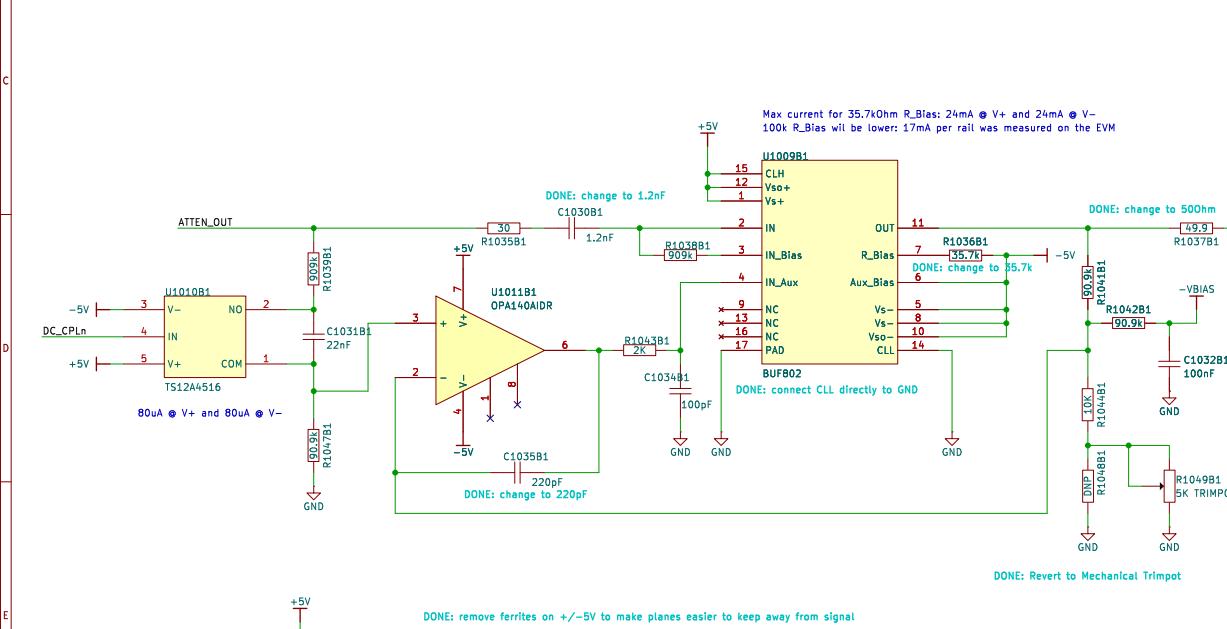
Rev: 5

Id: 2/18

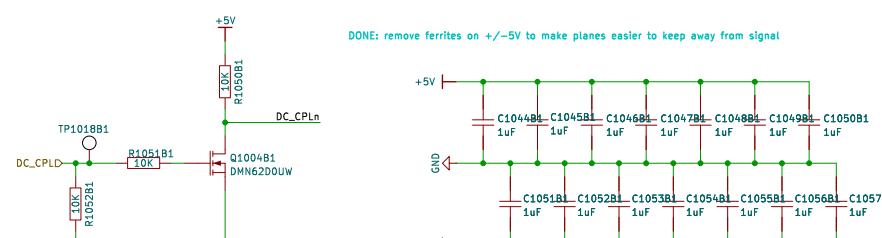
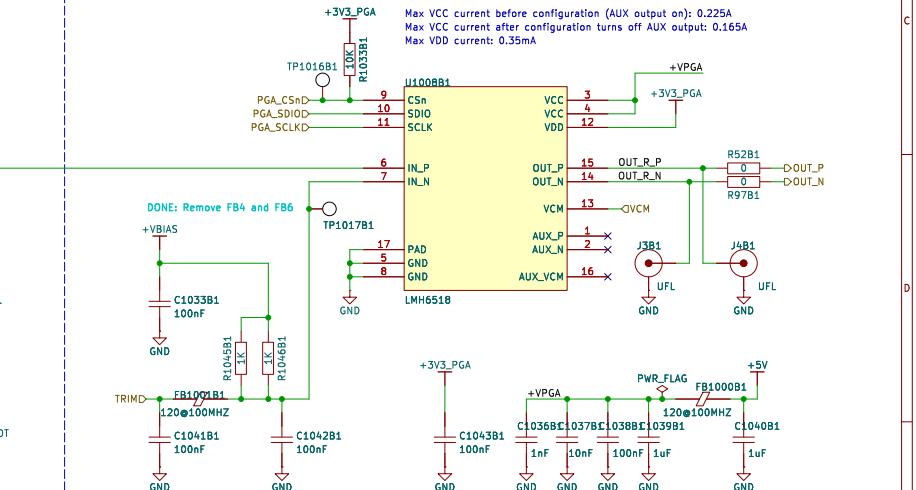
Termination and Attenuation



Input Buffer and AC/DC Coupling



Programmable Gain Amplifier



EEVengers

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File: FE_Channel.kicad_sch

Title: ThunderScope

Size: A3

Date: 8.99.0-3402-gadd58faa30

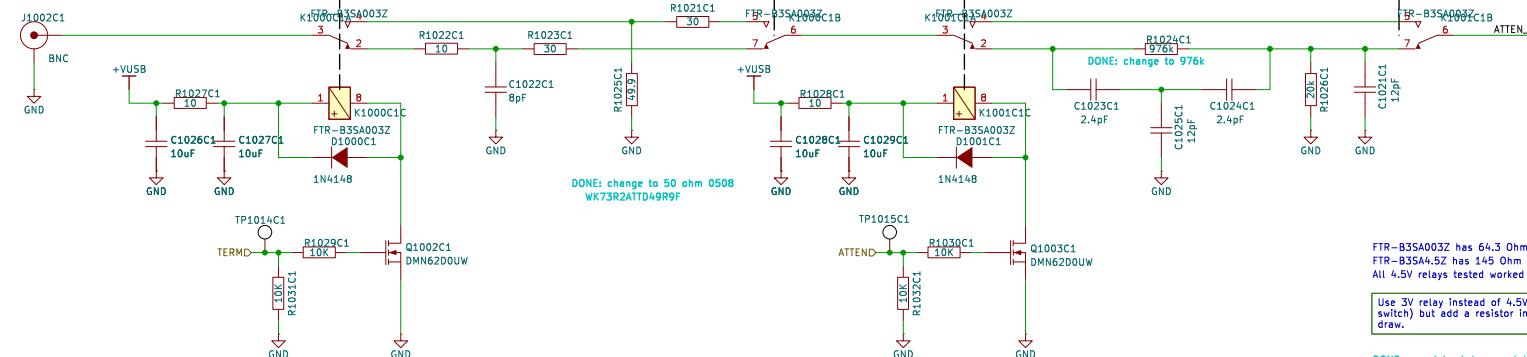
Rev: 5

KiCad E.D.A. 8.99.0-3402-gadd58faa30

Id: 2/18

Termination and Attenuation

TODO: Change Relays to 4.5V Parts as we are now powering them w/ +VUSB

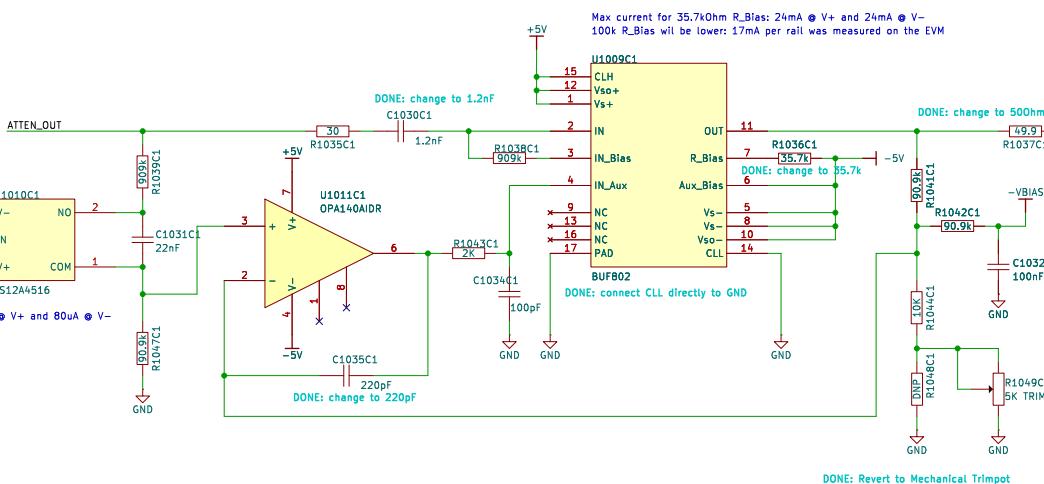


FTR-B35A003Z has 64.3 Ohm Coil Resistance, 2.25V Must Operate Voltage, 0.051A @ 3.3V
FTR-B35A4.5Z has 145 Ohm Coil Resistance, 3.38V Must Operate Voltage, 0.023A @ 3.3V
All 4.5V relays tested worked down to 3V

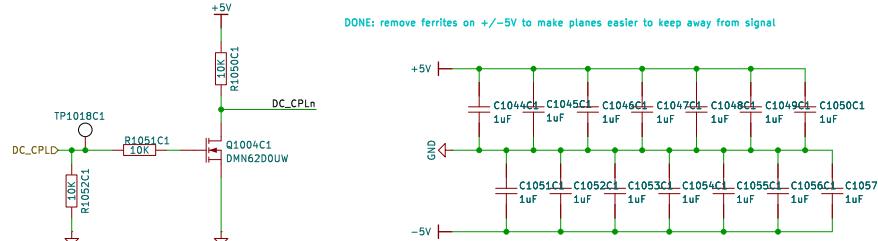
Use 3V relay instead of 4.5V (unit 9 ch3 aten relay could not switch) but add a resistor in line with the coil to reduce current draw.

DONE: revert back to non-latched relays to avoid indeterminate state when powered off

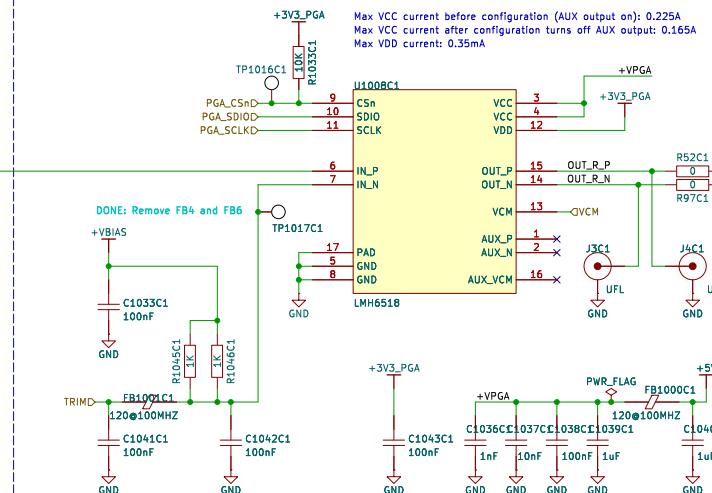
Input Buffer and AC/DC Coupling



DONE: Revert to Mechanical Trimpc



Programmable Gain Amplifier



FFVengers

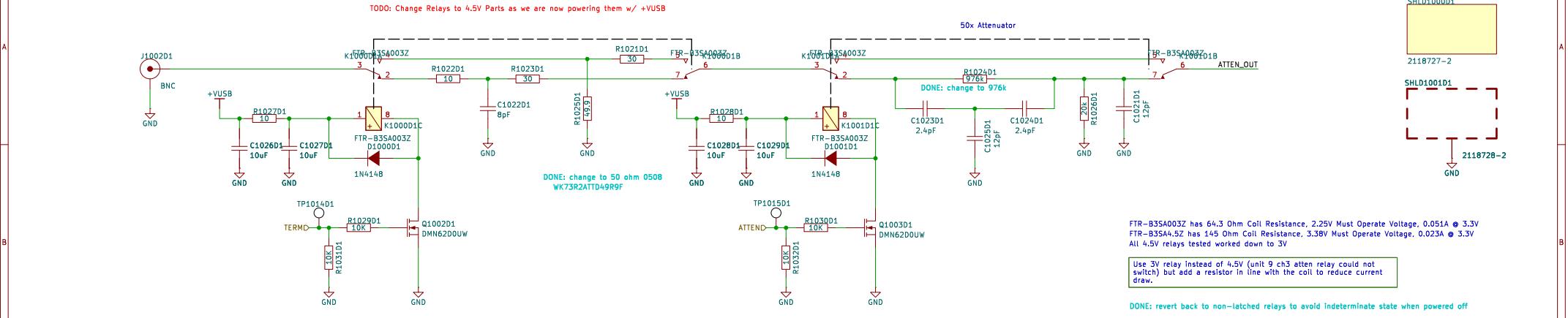
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File: FE_Channel.kicad_sch

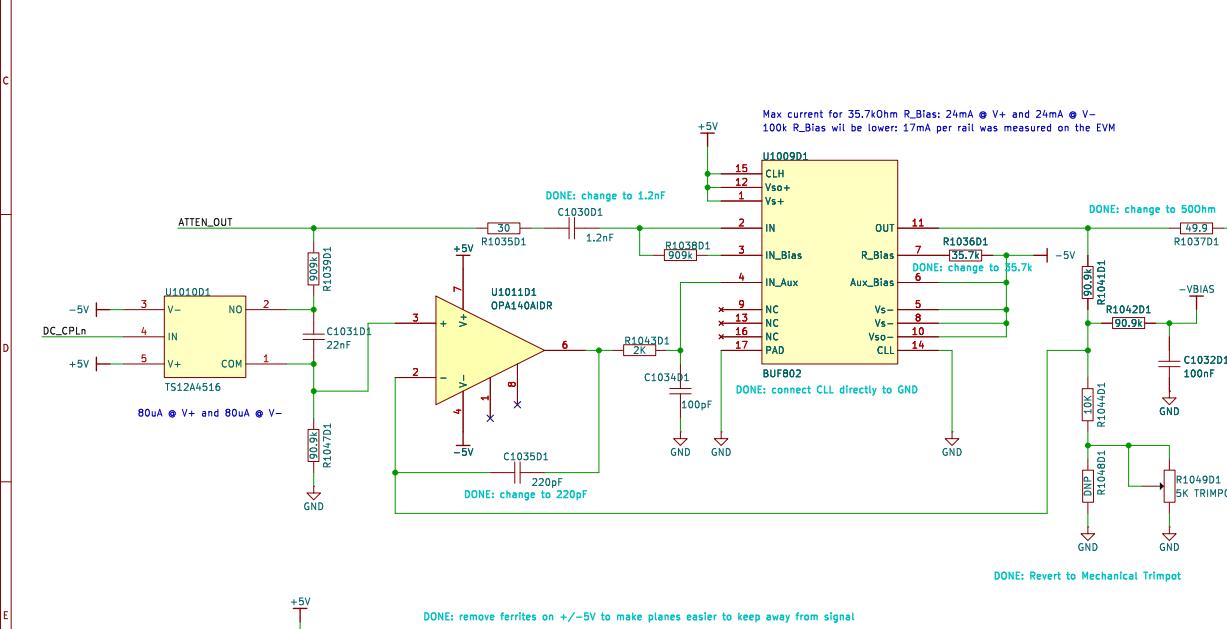
Title: ThunderScope

Re

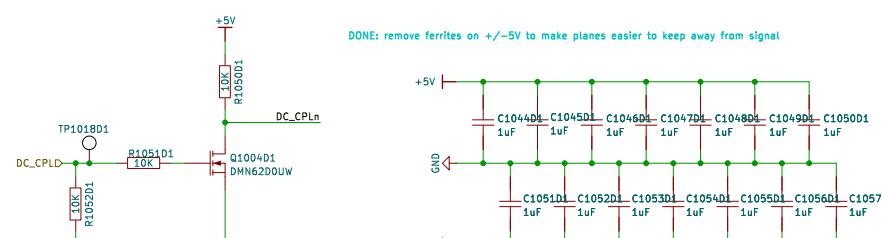
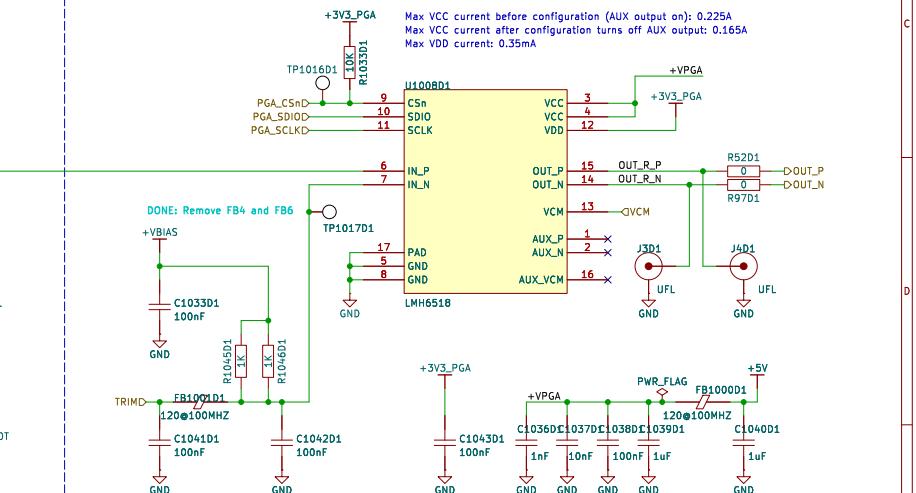
Termination and Attenuation



Input Buffer and AC/DC Coupling



Programmable Gain Amplifier



EEVengers

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Title: ThunderScope

Size: A3

Date:

KiCad E.D.A. 8.99.0-3402-gadd58faa30

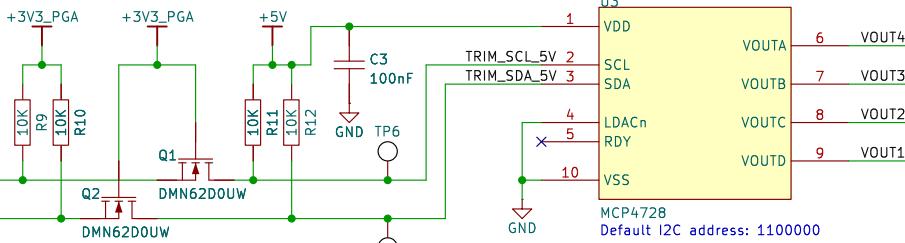
Rev: 5

Id: 2/18

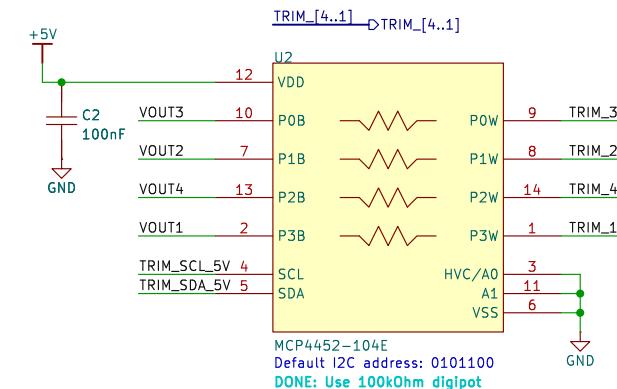
1 2 3 4 5 6

Offset Voltage Trim and User Offset Control

A

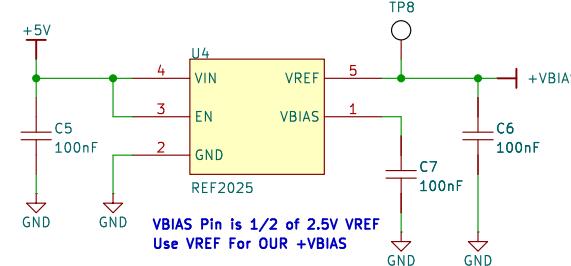


B



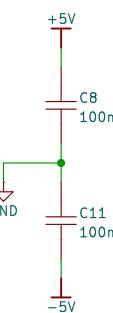
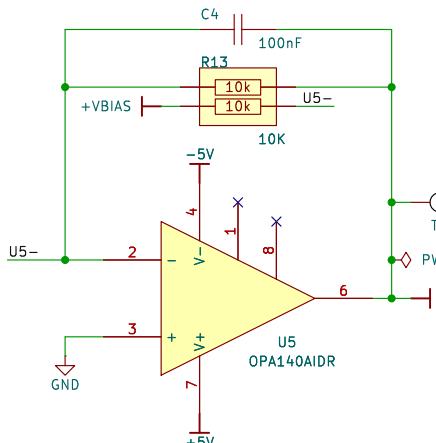
Bias Voltage Generation

C



D

Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140
-Max resistance is $(575/4 \parallel 10k) = 141.7 \text{ Ohm}$
-Worst case current is 17.64mA
-Use REF2025, has max current of 20mA
-Change U5 divider to matched resistor network
-ACASN1002S1002P1AT



EEVengers

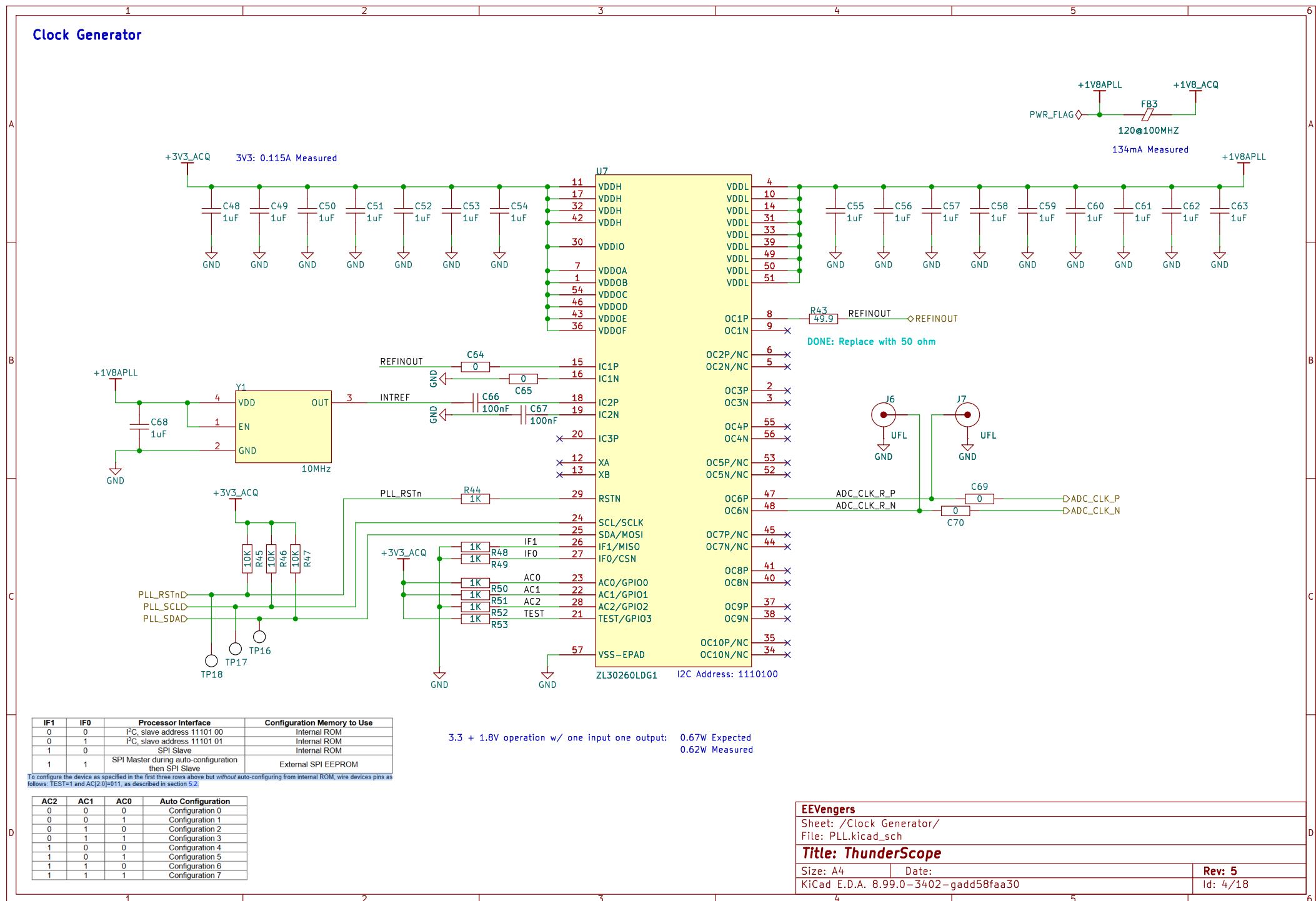
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File: FE.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

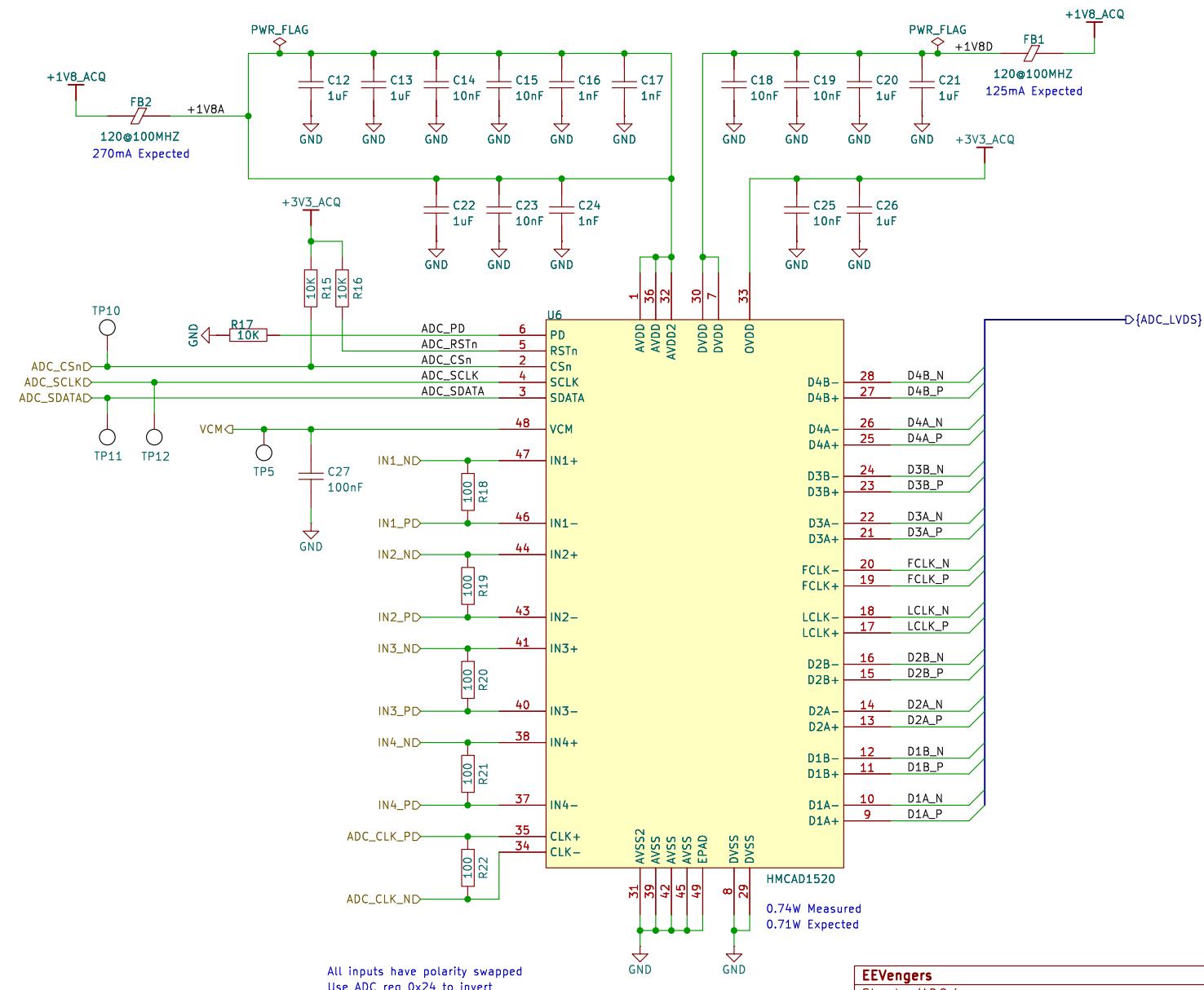
Rev: 5
Id: 3/18

1 2 3 4 5 6



1 2 3 4 5 6

ADC



EEVengers

Sheet: /ADC/
File: ADC.kicad_sch

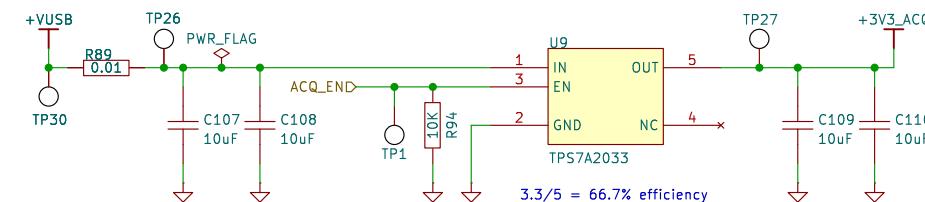
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Rev: 5
Id: 5/18

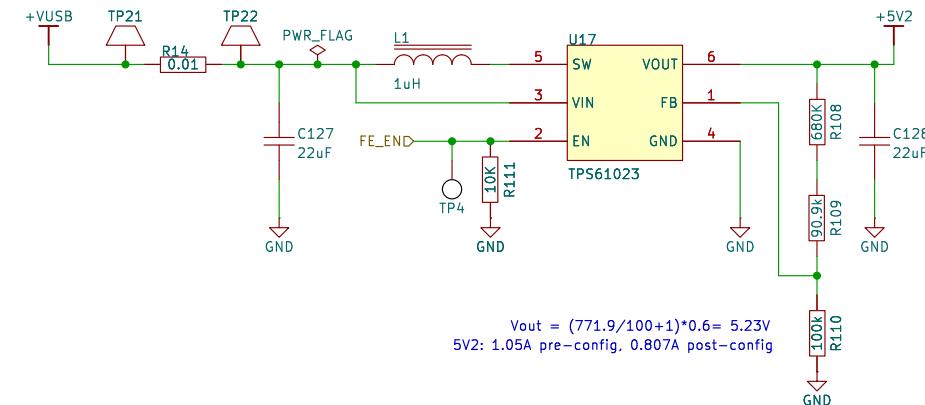
1 2 3 4 5 6

Acquisition Voltage Regulators



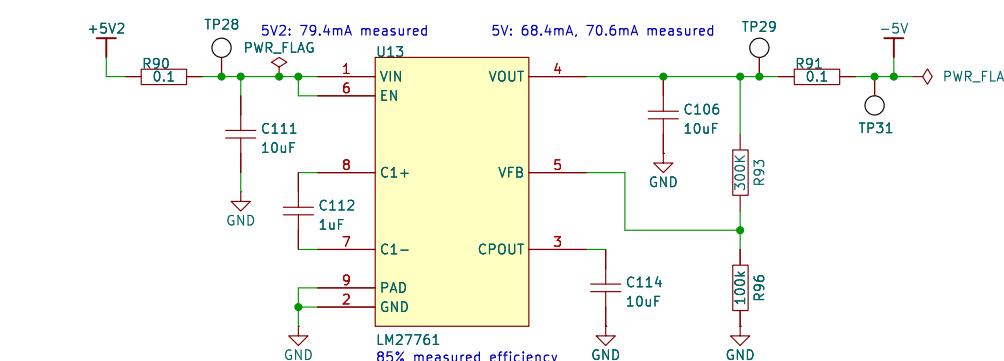
DONE: Hook up power good, pull up is in FPGA IO Banks

Front End Voltage Regulators



$$V_{out} = (771.9/100+1)*0.6 = 5.23V$$

5V2: 1.05A pre-config, 0.807A post-config



543mA Measured Total: 529mA Expected

$V_{out} = 0.8 * (R1/R2 + 1)$

$V_{out} = 0.8 * (4.7/3.8 + 1)$

$V_{out} = 1.79V$

$1.8/2.5 = 72\% \text{ efficiency}$

6ms soft start time on previous LDO, need same or greater

$T_{ss} = (V_{REF} \times C_{nr/ss}) / I_{nr/ss}$

$T_{ss} = (0.8 \times 100nF) / 6.2\mu A \text{ [for SS_CTRL = GND]}$

$T_{ss} = 0.0129s = 13ms$

DONE: Hook up power good, pull up is in FPGA IO Banks

5V: 968mA pre-config

5V: 728mA post-config

$V_{out} = 0.8 * (R1/R2 + 1)$

$V_{out} = 0.8 * (20/3.8 + 1)$

$V_{out} = 5.01V$

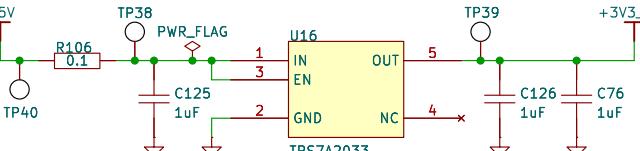
6ms soft start time on previous LDO, need same or greater

$T_{ss} = (V_{REF} \times C_{nr/ss}) / I_{nr/ss}$

$T_{ss} = (0.8 \times 100nF) / 6.2\mu A \text{ [for SS_CTRL = GND]}$

$T_{ss} = 0.0129s = 13ms$

DONE: Hook up power good, pull up is in FPGA IO Banks



EEVengers

Sheet: /ACQ and FE Voltage Regs/

File: ACQ_FE_VREG.kicad_sch

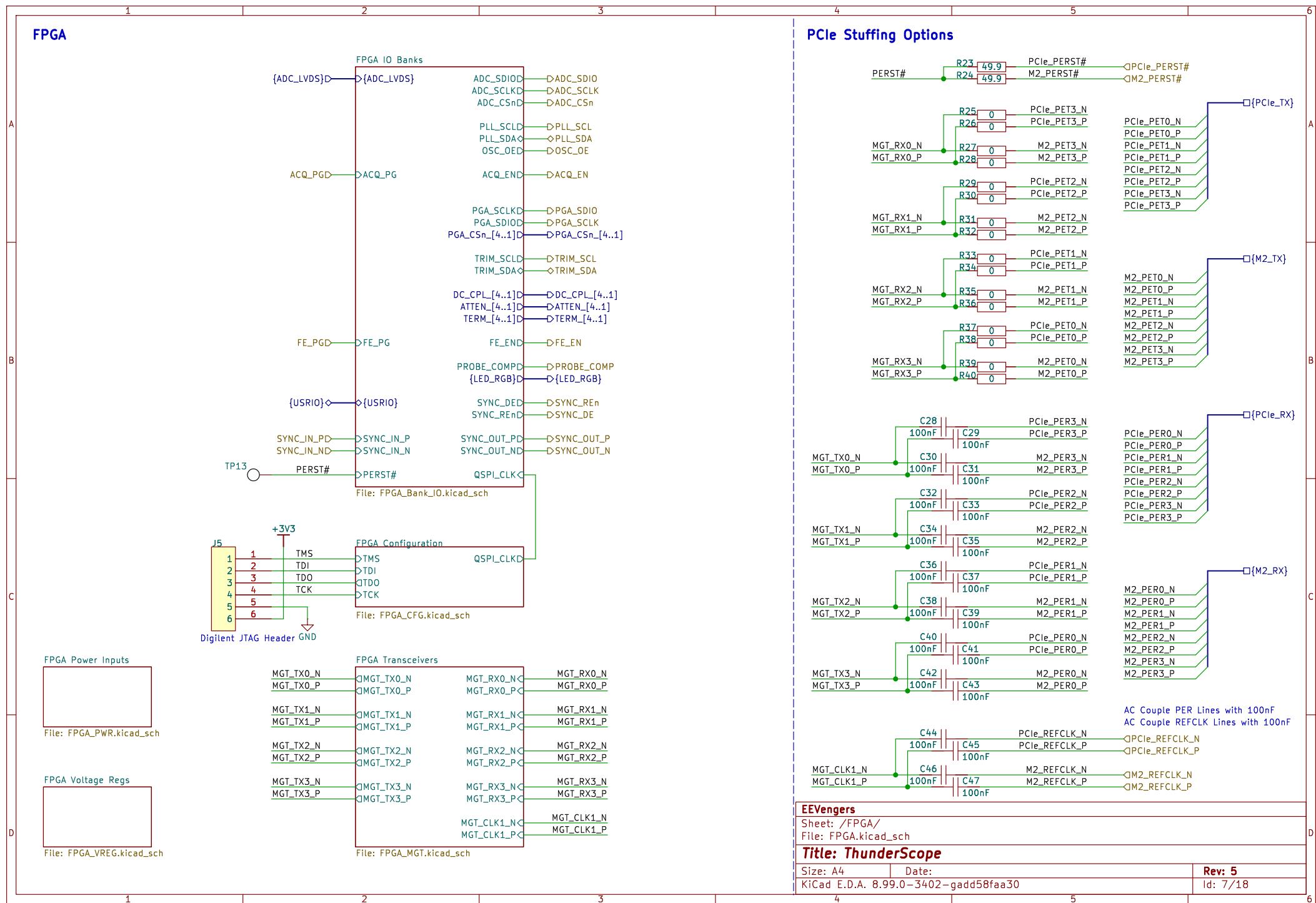
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Size: A4 Date:

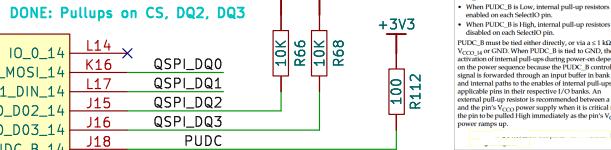
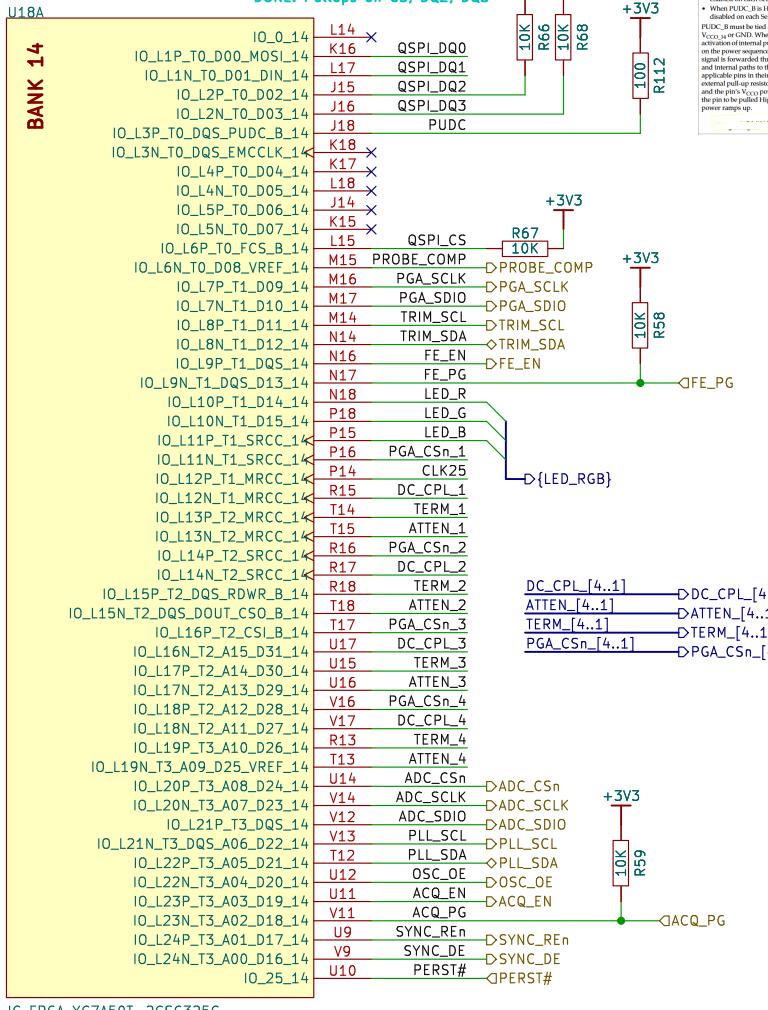
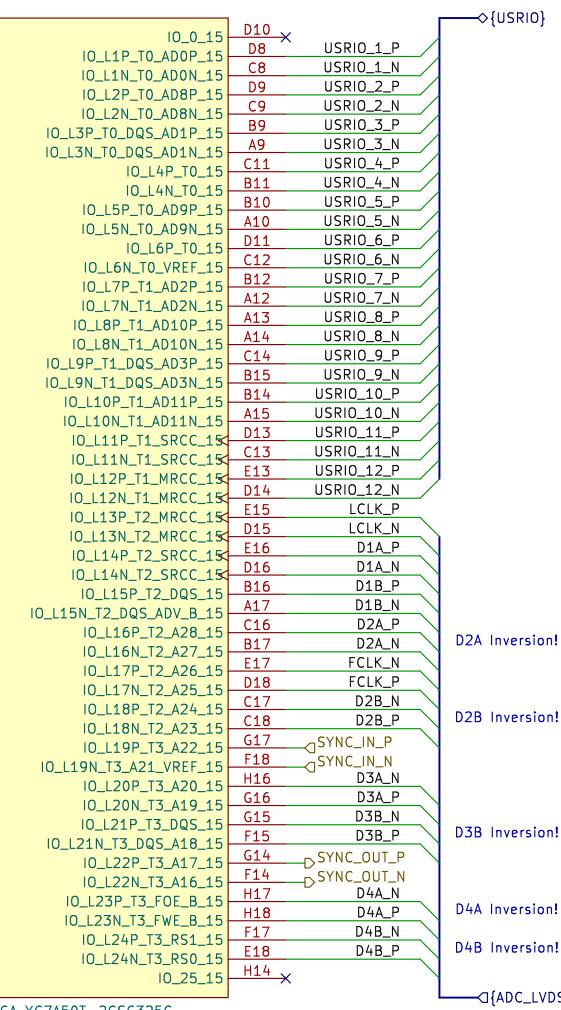
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Rev: 5

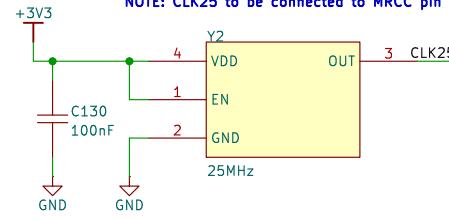
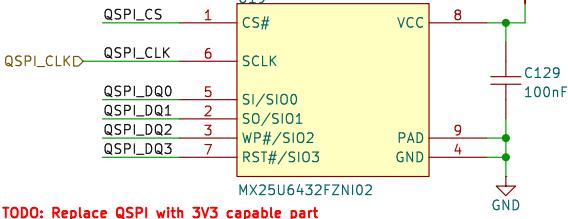
Id: 6/18



1 2 3 4 5 6

FPGA IO Banks**BANK 14****BANK 15**

IC FPGA XC7A50T-2CSG325C

D**5****6**

FPGA Configuration

A

B

2

D

Table 2-1: 7 Series FPGA Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

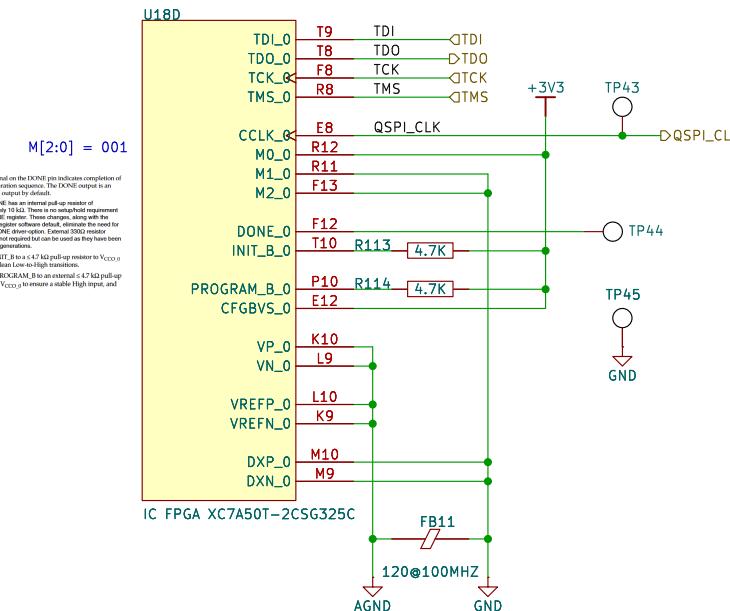


Table 2-6: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Banks Used	Configuration Interface IO Voltage	HR Bank 0 V _{CCO_0}	HR Bank 14 V _{CCO_14}	HR Bank 15 V _{CCO_15}	CFGWB
JTAG (only)	0	3.3V	3.3V	Any	Any	V _{CCCO}
		2.5V	2.5V	Any	Any	V _{CCCO}
		1.8V	1.8V	Any	Any	GND
		1.5V	1.5V	Any	Any	GND
Serial, SPI, or SelectMAP	0, 14 ⁽¹⁾	3.3V	3.3V	3.3V	Any	V _{CCCO}
		2.5V	2.5V	2.5V	Any	V _{CCCO}
		1.8V	1.8V	1.8V	Any	GND
		1.5V	1.5V	1.5V	Any	GND
BPI ⁽²⁾	0, 14, 15	3.3V	3.3V	3.3V	3.3V	V _{CCCO}
		2.5V	2.5V	2.5V	2.5V	V _{CCCO}
		1.8V	1.8V	1.8V	1.8V	GND
		1.5V	1.5V	1.5V	1.5V	GND

N

- RS[1:0] for MultiBoot or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.
- BPI mode is not available in the Spartan-7 family.

- RS[1:0] for MultiBoot or Fallback are in bank 15 supported in SPI mode.

FFVender

EEVBlog

Title: ThunderScope

KiCad E.D.A. 8.99.0-3402-qadd58faa30

Rev: 5
d: 9/18

FPGA Transceivers

A

A

B

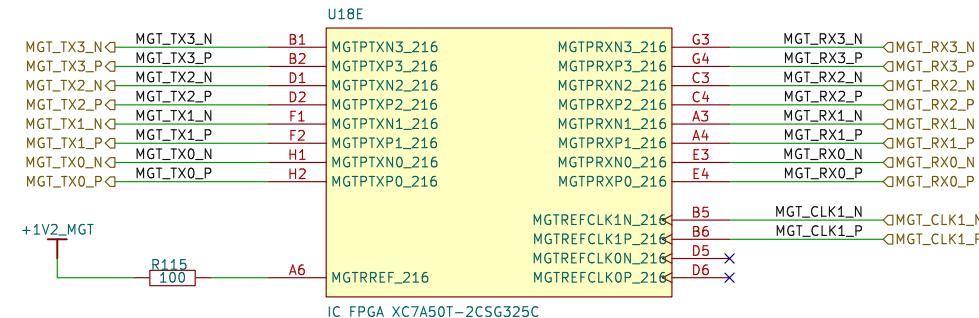
B

C

C

D

D

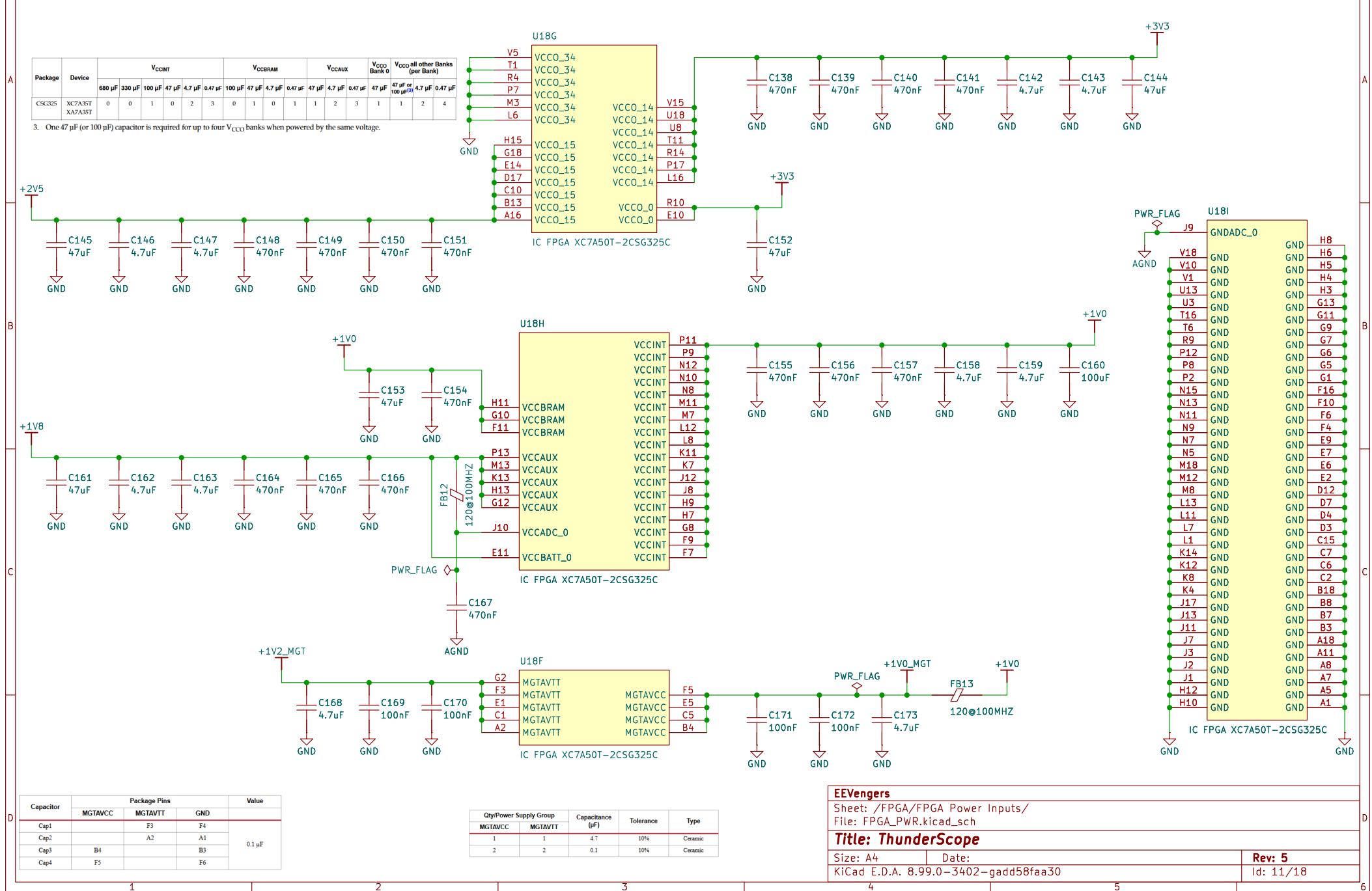
**EEVengers**

Sheet: /FPGA/FPGA Transceivers/
File: FPGA_MGT.kicad_sch

Title: ThunderScope

Size: A4	Date:	Rev: 5
KiCad E.D.A. 8.99.0-3402-gadd58faa30		Id: 10/18

FPGA Power Inputs



1

2

3

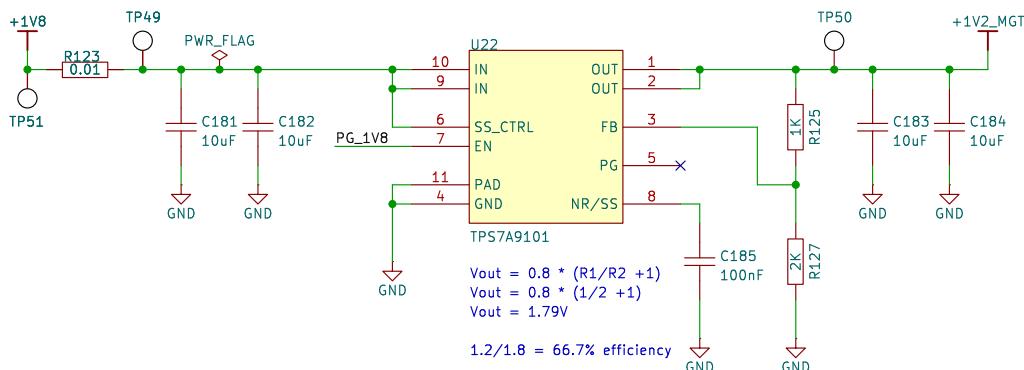
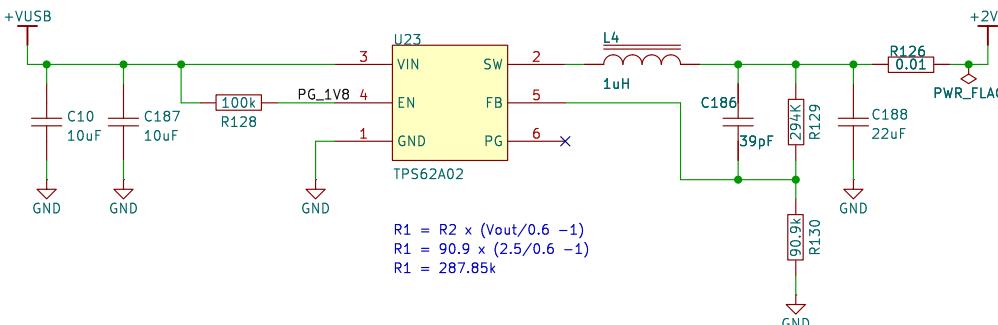
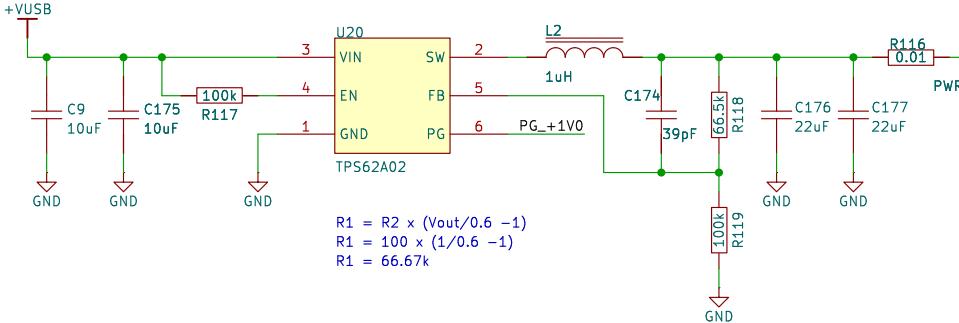
4

5

6

FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V



The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT
1V,1V,1.2V

1

2

3

4

5

6

EEVengers

Sheet: /FPGA/FPGA Voltage Regs/
File: FPGA_VREG.kicad_sch

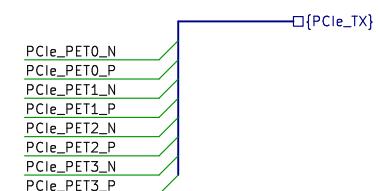
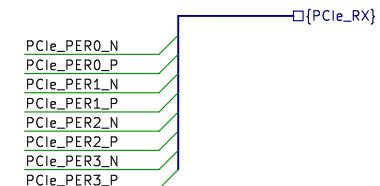
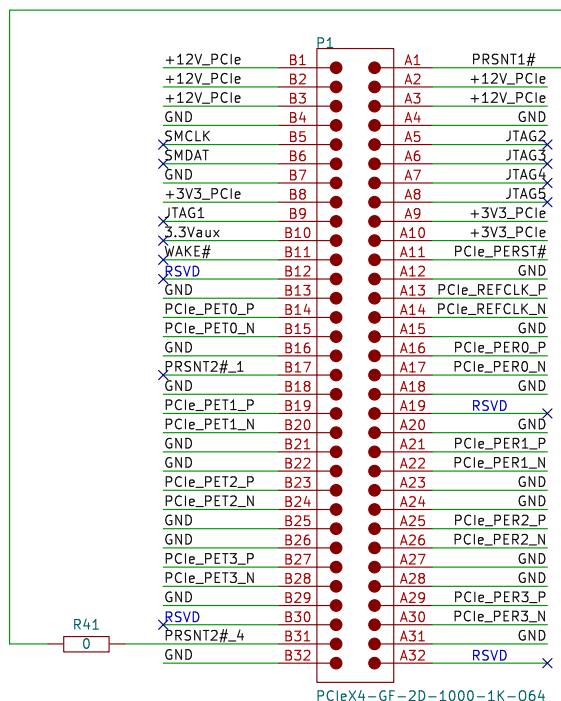
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Rev: 5 Id: 12/18

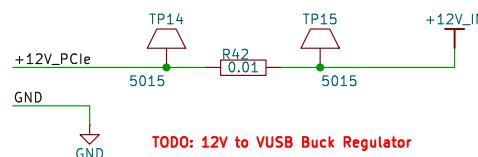
1 2 3 4 5 6

PCIe x4 Edge Connector

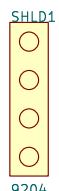


PCIe_REFCLK_P → PCIe_REFCLK_P
PCIe_REFCLK_N → PCIe_REFCLK_N

PCIe_PERST# → PCIe_PERST#



PCIe bracket



EEVengers

Sheet: /PCIe_x4/
File: CON_PCIe_X4.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Rev: 5
Id: 13/18

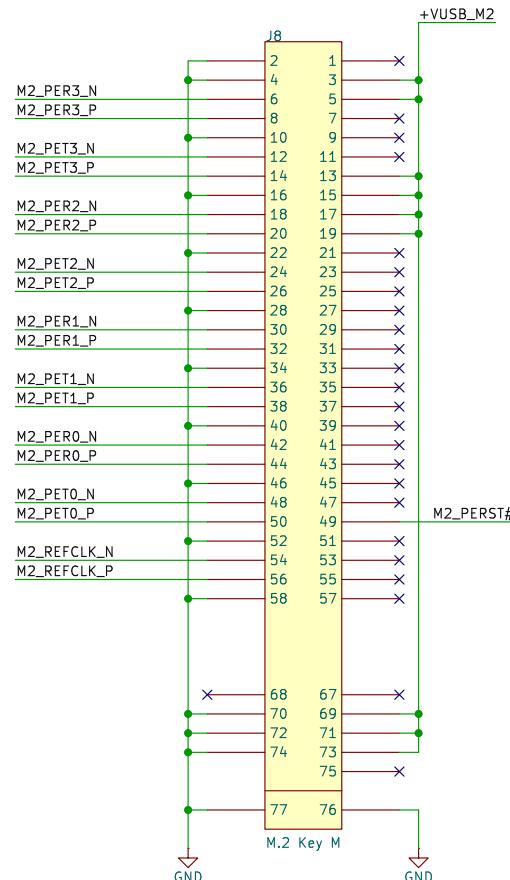
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1 2 3 4 5 6

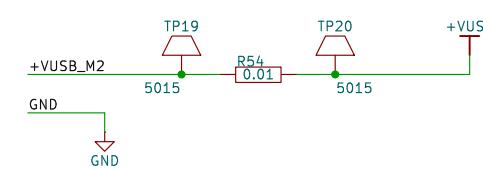
M.2 Key M Connector

A

Main Board
Custom Pinout



NOTE: The TB/USB4 adaptor must be modified to give us VUSB instead of 3V3



M2_RX

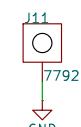
M2_TX

M2_REFCLK_P
M2_REFCLK_N

M2_PERST#

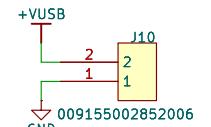
Ground Lug

Fan Connector



J11
7792

↓
GND



+VUSB
2
1
J10
009155002852006
GND

EEVengers

Sheet: /M.2_Key_M/
File: M2_KEY_M.kicad_sch

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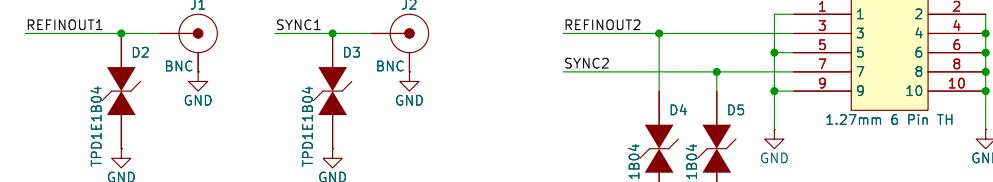
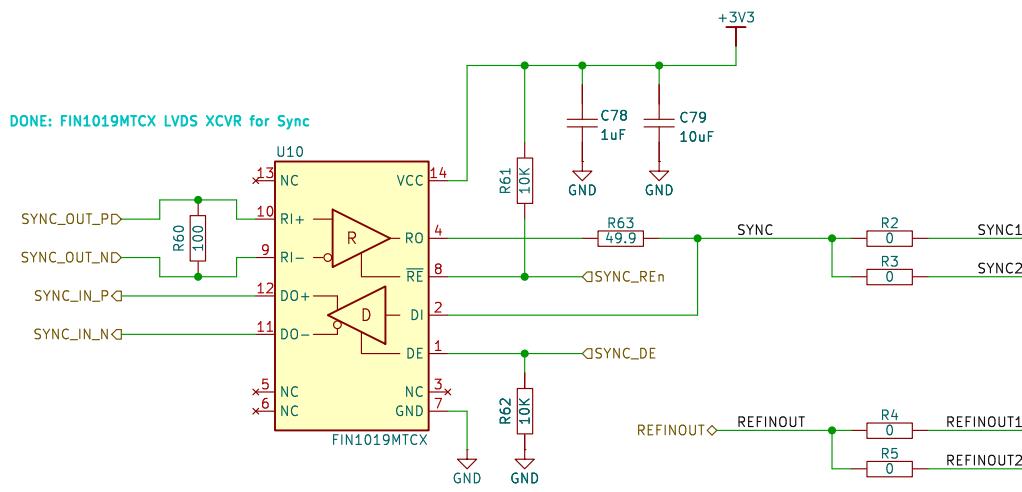
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Rev: 5
Id: 14/18

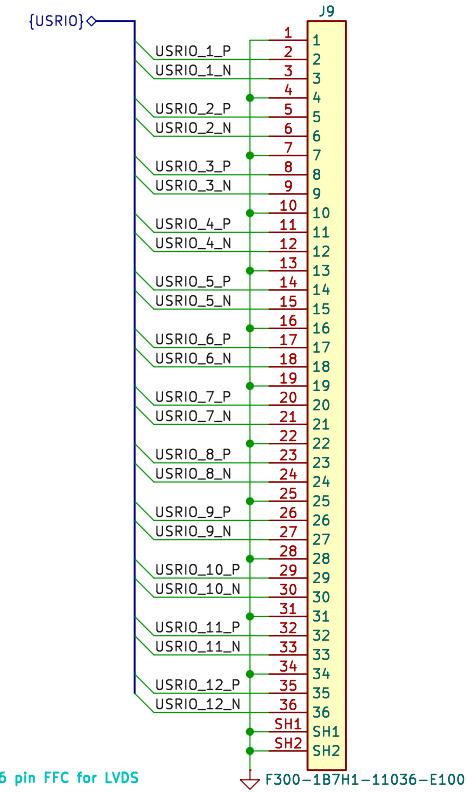
1 2 3 4 5 6

1 2 3 4 5 6

Reference Clock and Sync

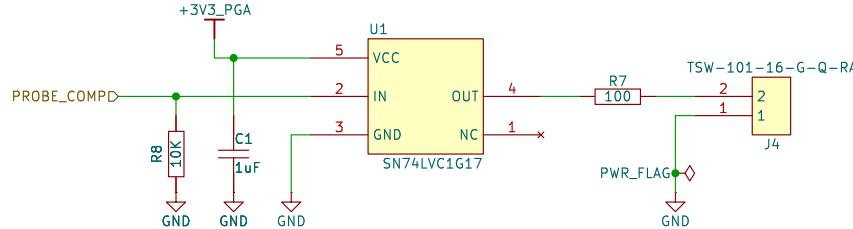


User IO Flat Flex Connector

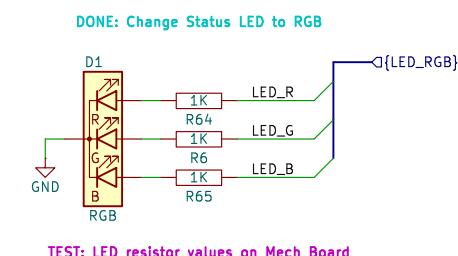


DONE: 36 pin FFC for LVDS

Probe Compensation



Status LED

**EEVengers**Sheet: /User IO/
File: User_Io.kicad_sch**Title: ThunderScope**Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30Rev: 5
Id: 15/18