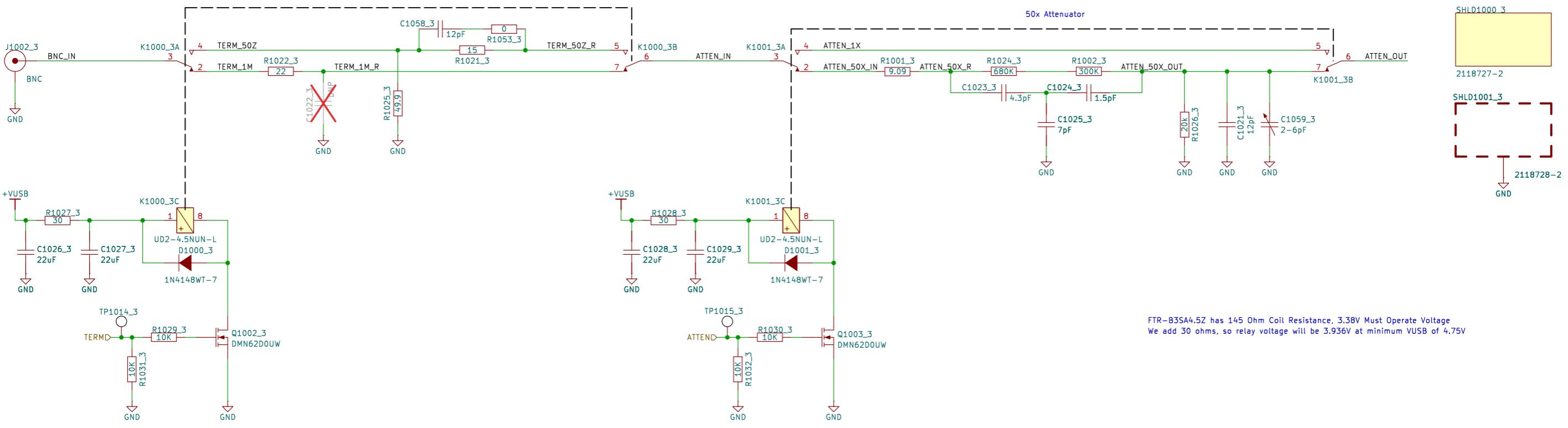


Termination and Attenuation



FTR-B3SA4.5Z has 145 Ohm Coil Resistance, 3.38V Must Operate Voltage
We add 30 ohms, so relay voltage will be 3.936V at minimum VUSB of 4.75V

Input Buffer and AC/DC Coupling

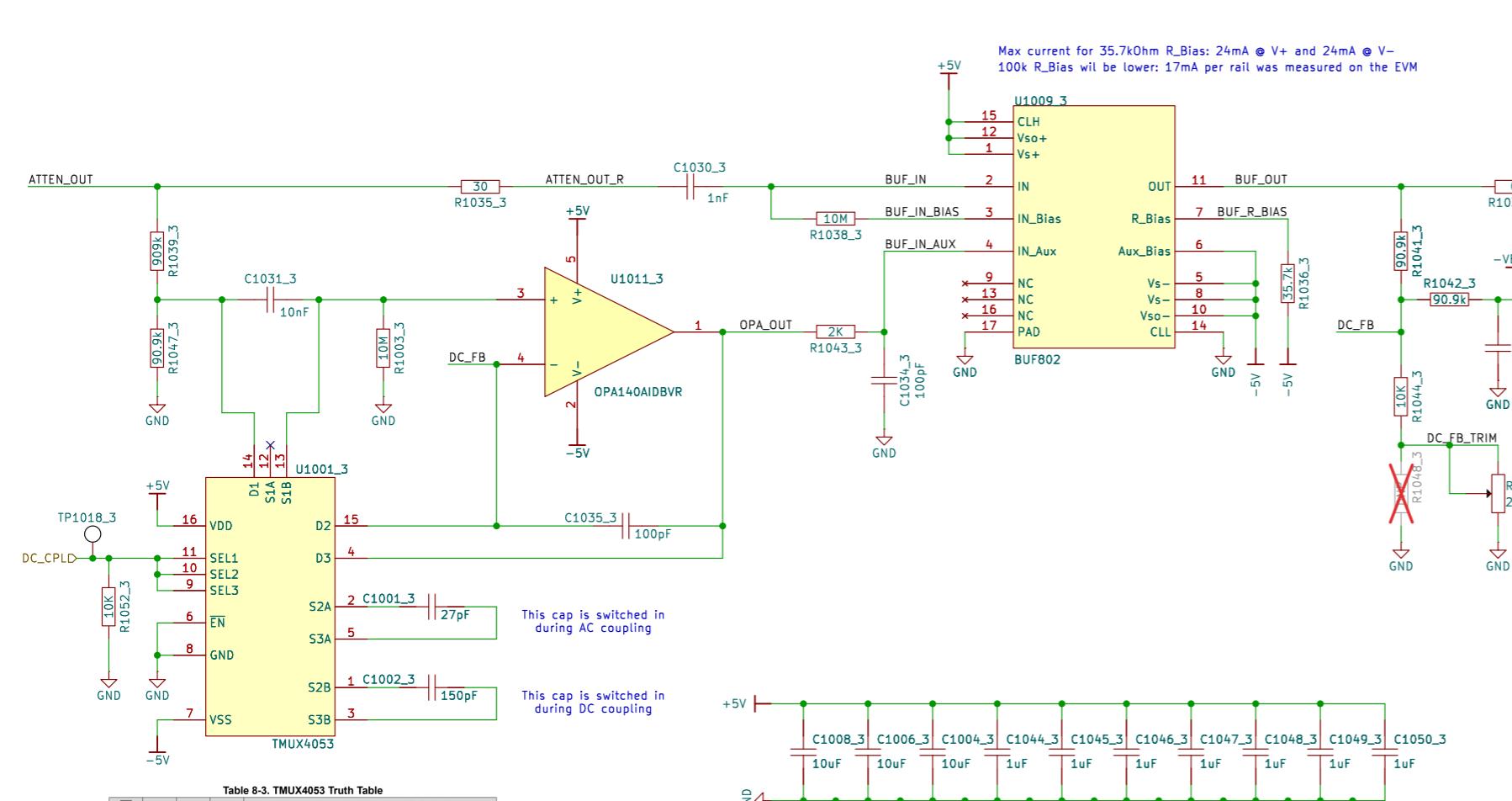
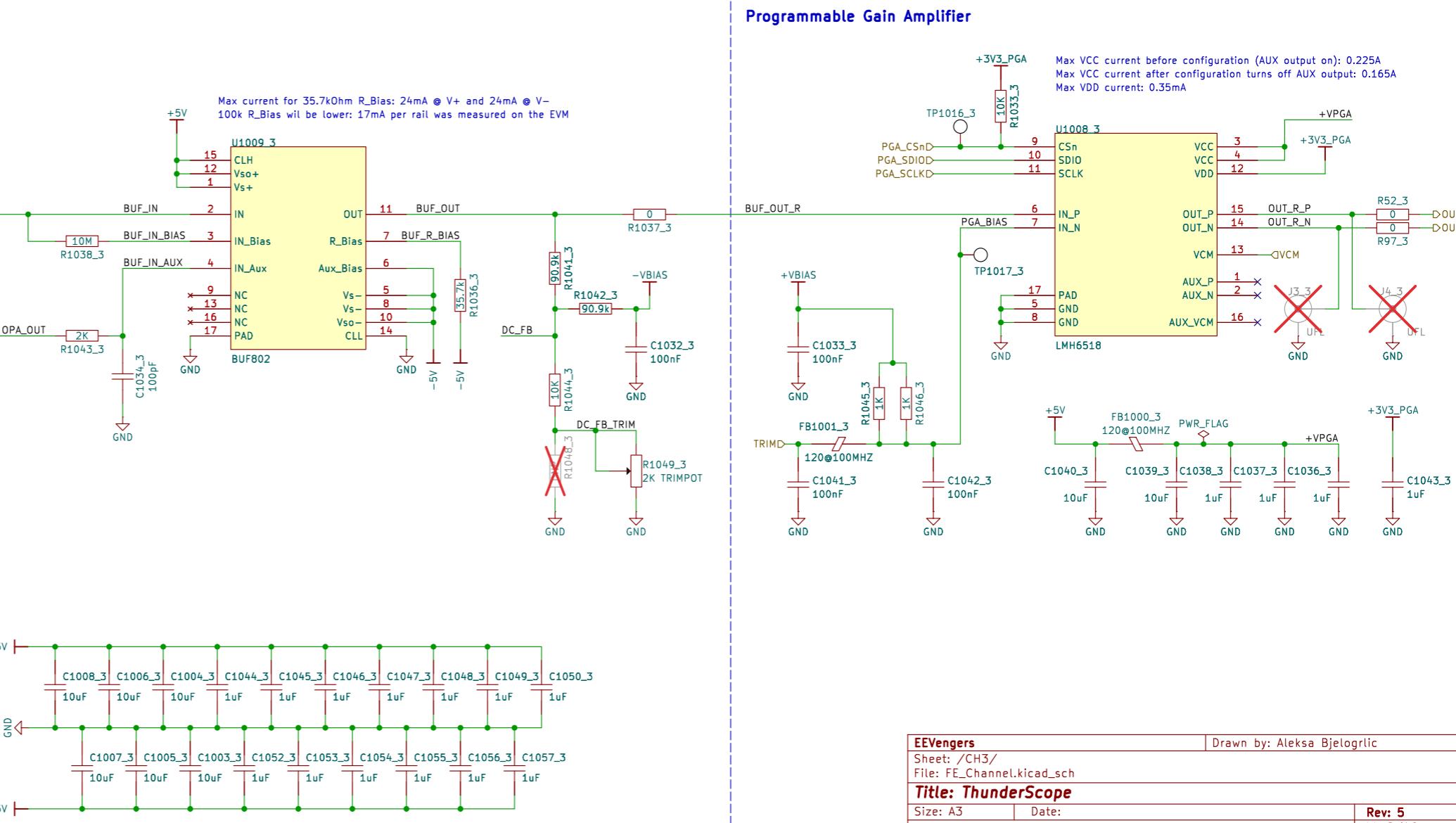
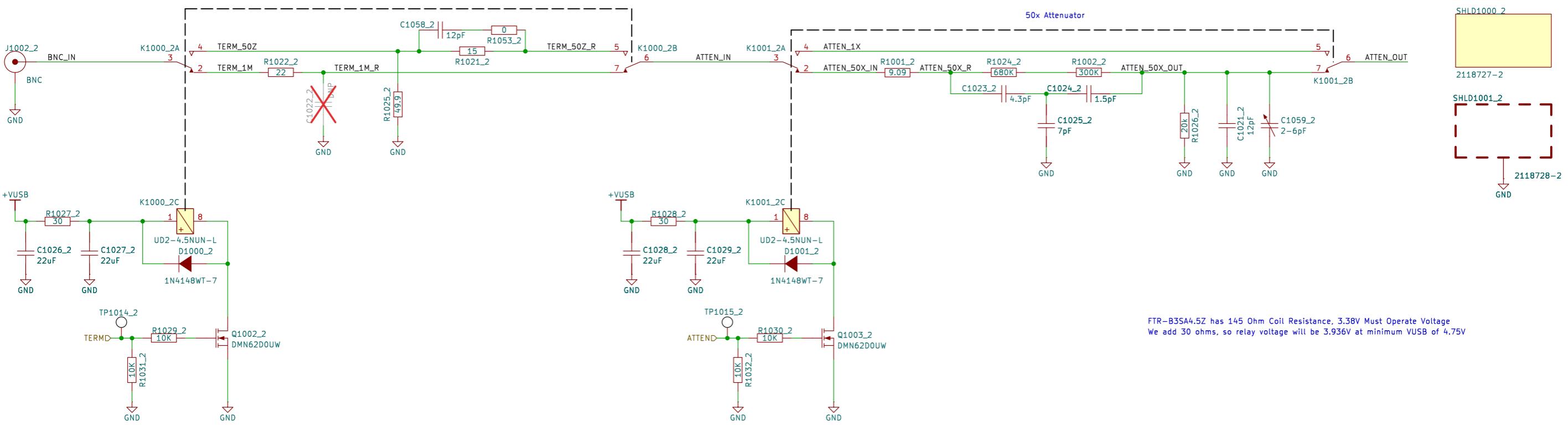


Table 8-3. TMUX4053 Truth Table				
EN	SEL1	SEL2	SEL3	Selected Signal Path Connected to Drain Pins
0	0	X	X	S1A to D1
0	1	X	X	S1B to D1
0	X	0	X	S2A to D2
0	X	1	X	S2B to D2
0	X	X	0	S3A to D3
0	X	X	1	S3B to D3
1	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	All inputs are unselected (Hi-Z)



EEVengers	
Sheet: /CH3/	
File: FE_Channel.kicad_sch	
Title: ThunderScope	
Size: A3	Date:

Termination and Attenuation



FTR-B3SA4.5Z has 145 Ohm Coil Resistance, 3.38V Must Operate Voltage
We add 30 ohms, so relay voltage will be 3.936V at minimum VUSB of 4.75V

Input Buffer and AC/DC Coupling

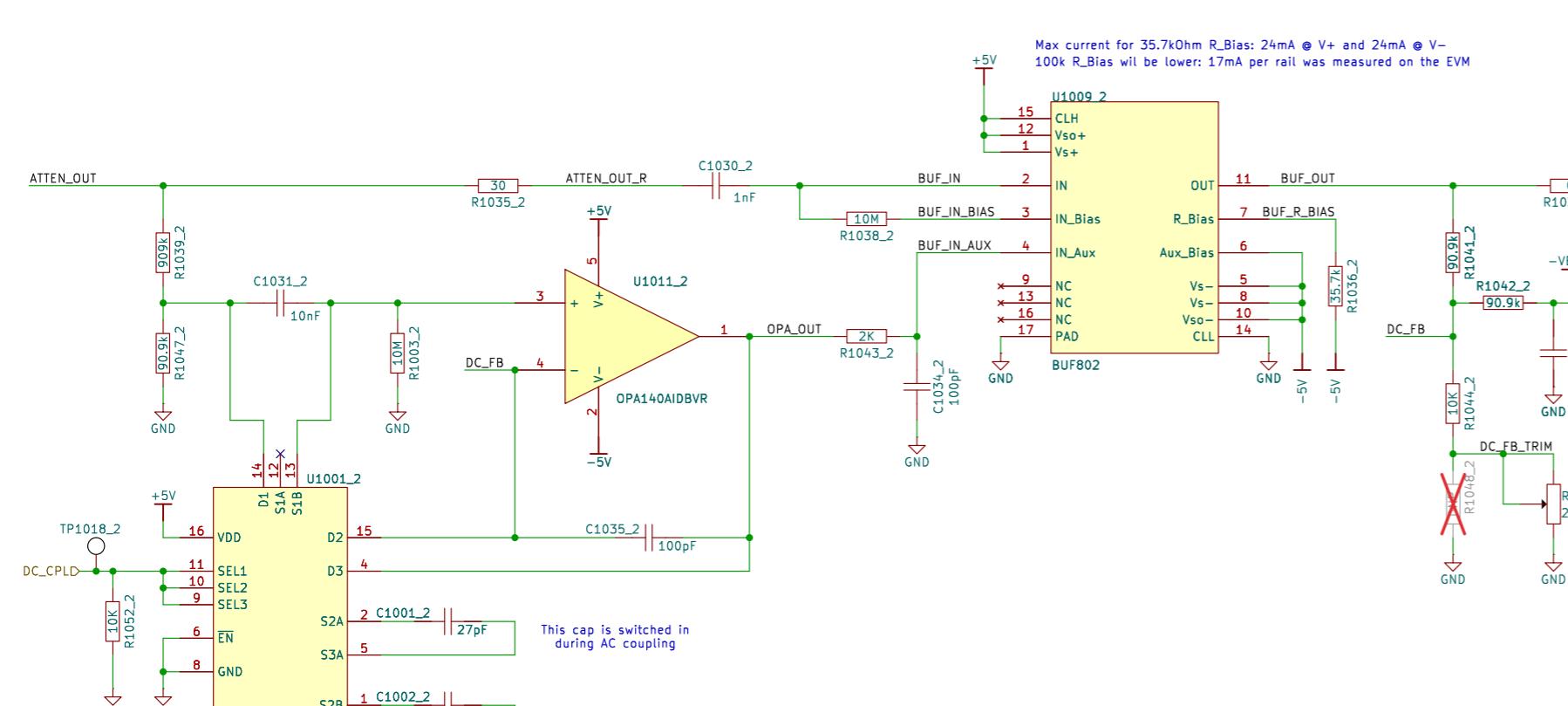
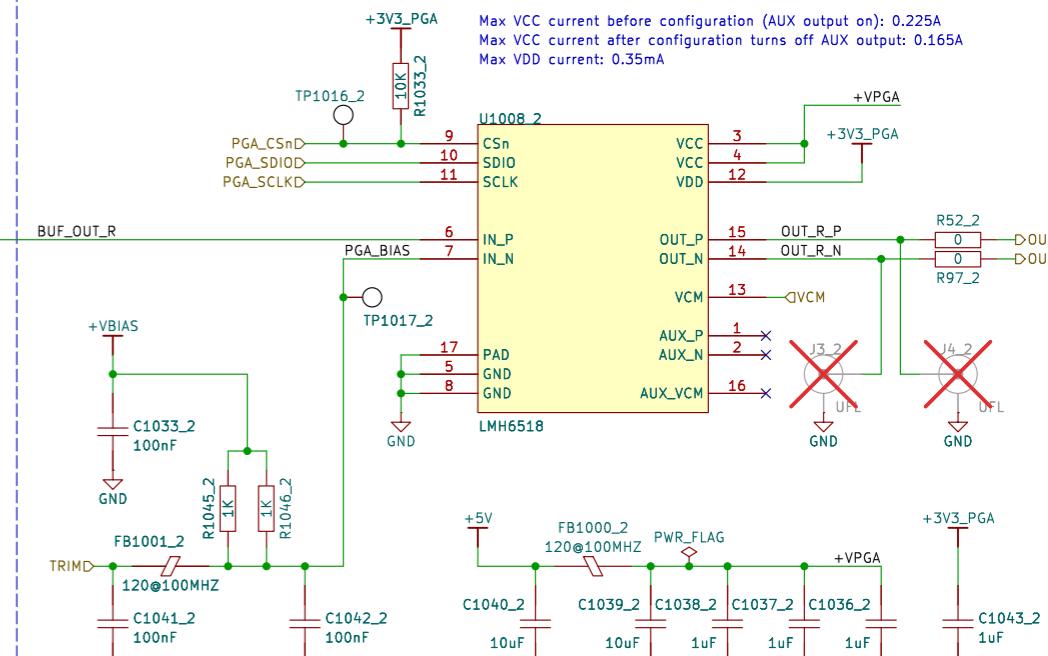


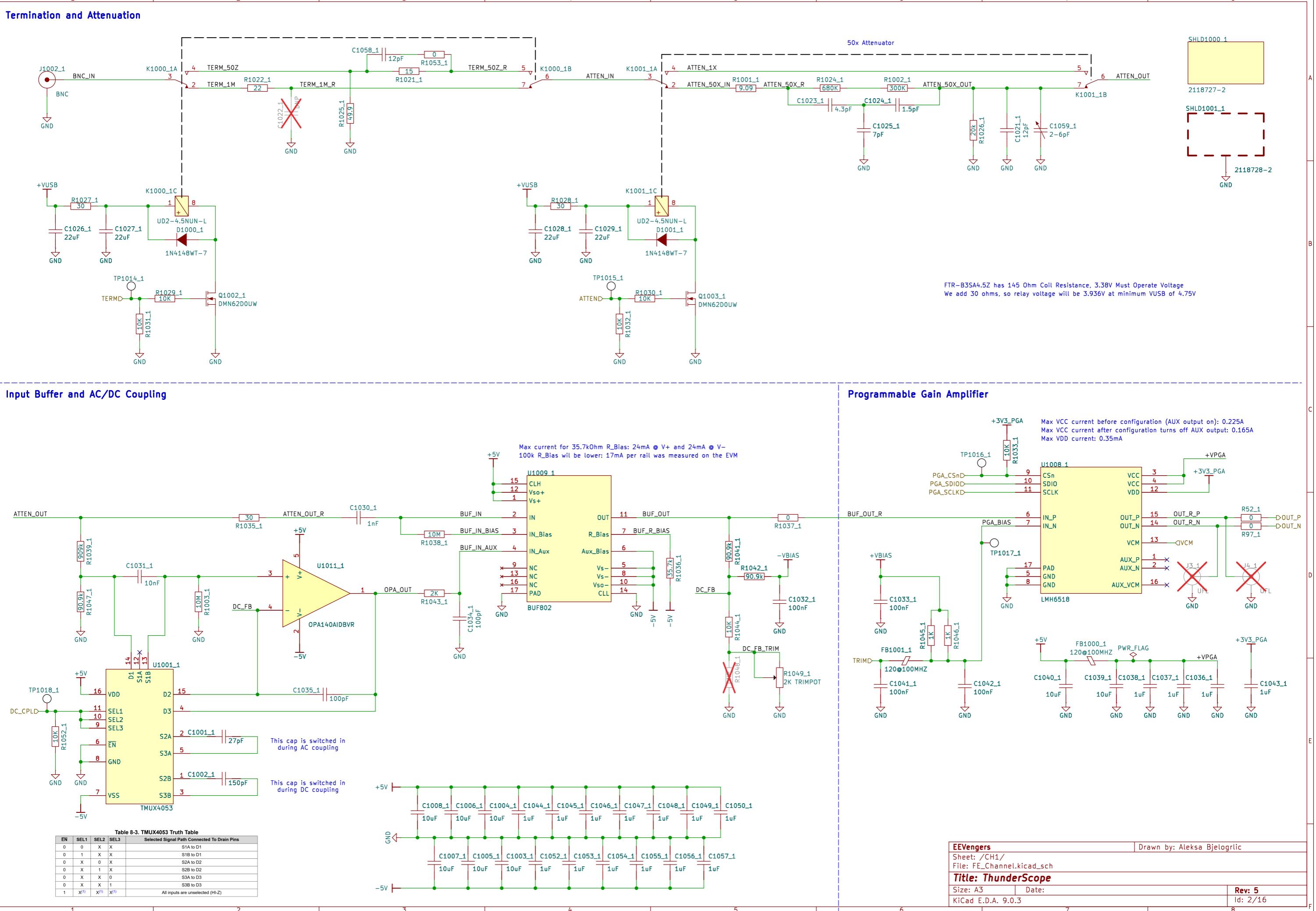
Table 8-3. TMUX4053 Truth Table

EN	SEL1	SEL2	SEL3	Selected Signal Path Connected To Drain Pins
0	0	X	X	S1A to D1
0	1	X	X	S1B to D1
0	X	0	X	S2A to D2
0	X	1	X	S2B to D2
0	X	X	0	S3A to D3
0	X	X	1	S3B to D3
1	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	All inputs are unselected (Hi-Z)

Programmable Gain Amplifier



EE Avengers	
Sheet: /CH2/	
File: FE_Channel.kicad_sch	
Title: ThunderScope	
Size: A3	Date:



1 2 3 4 5 6

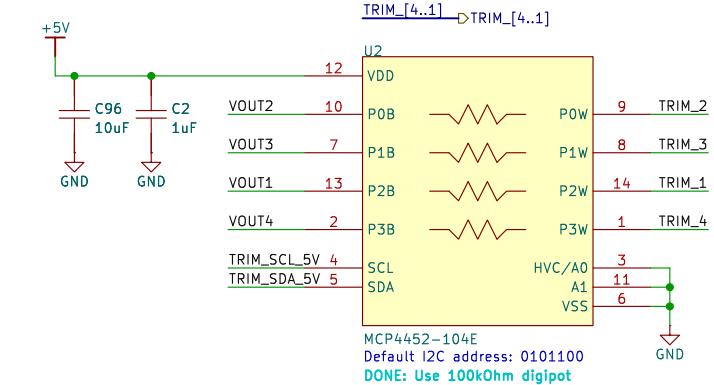
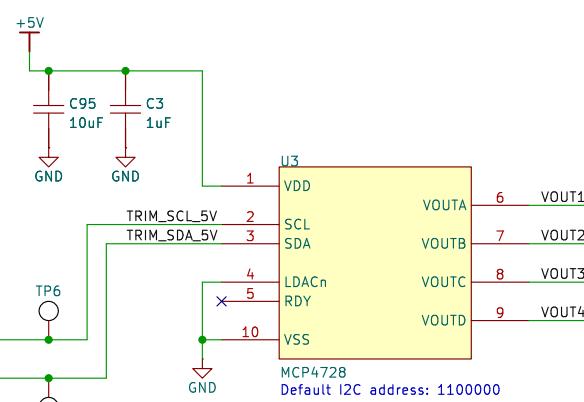
Offset Voltage Trim and User Offset Control

A

B

A

B



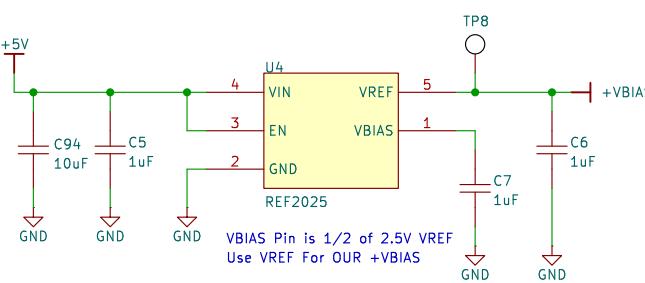
Bias Voltage Generation

C

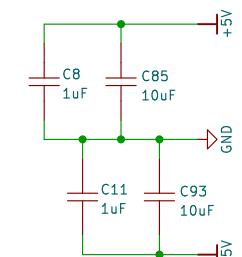
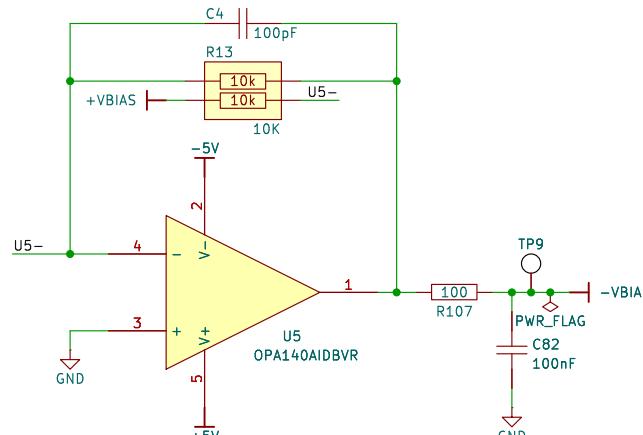
D

C

D



Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140
-Max resistance is $(575/4 // 10k) = 141.7 \text{ Ohm}$
-Worst case current is 17.64mA
-Use REF2025, has max current of 20mA
-Change U5 divider to matched resistor network
-ACASN1002S1002P1AT



EEVengers

Sheet: /Front End Trim and Bias/
File: FE.kicad_sch

Title: ThunderScope

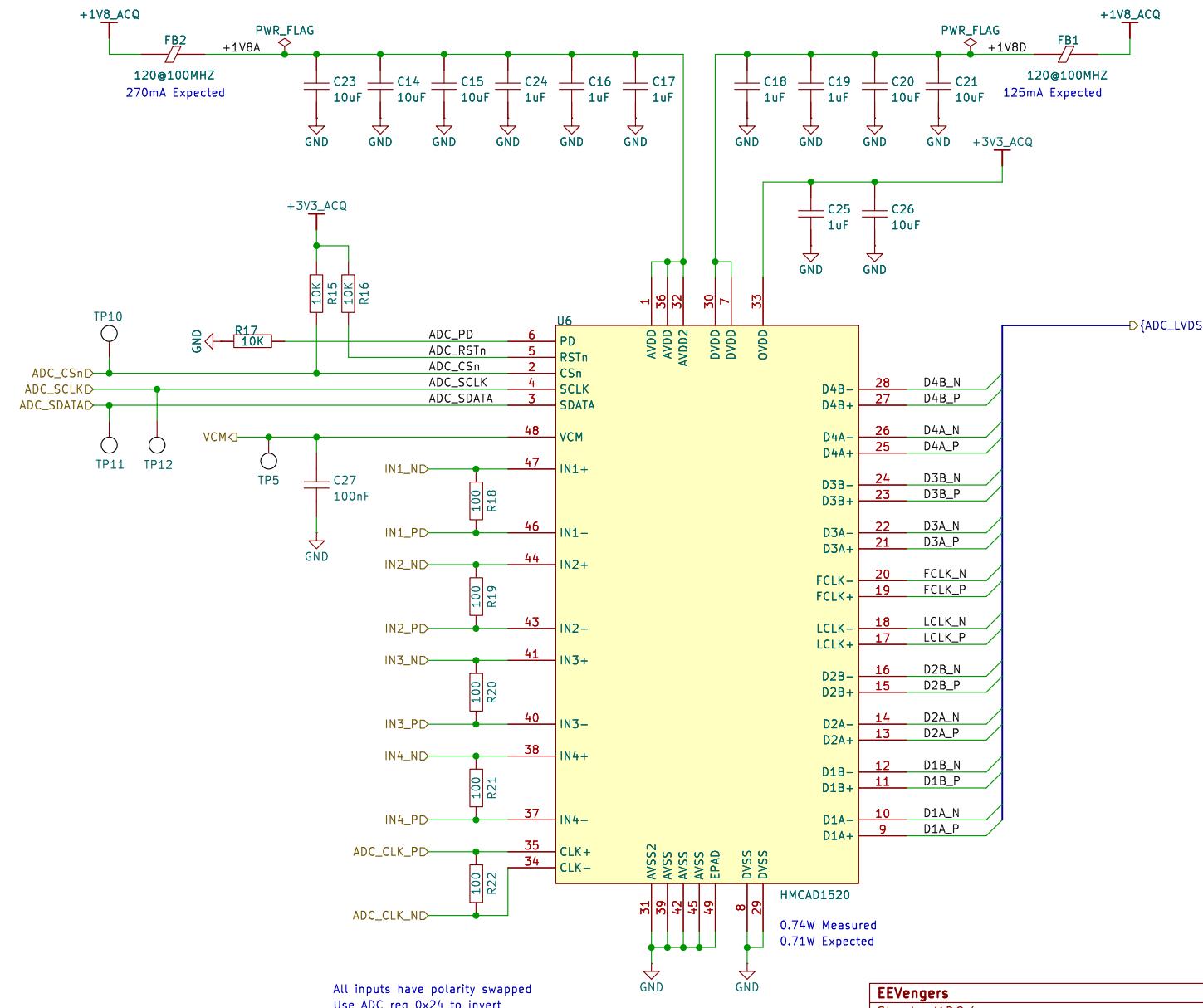
Size: A4 Date:
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Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 3/16

1 2 3 4 5 6

1 2 3 4 5 6

ADC

All inputs have polarity swapped
Use ADC reg 0x24 to invert

EEVengers

Drawn by: Aleksa Bjelogrlic

Sheet: /ADC/

File: ADC.kicad_sch

Title: ThunderScope

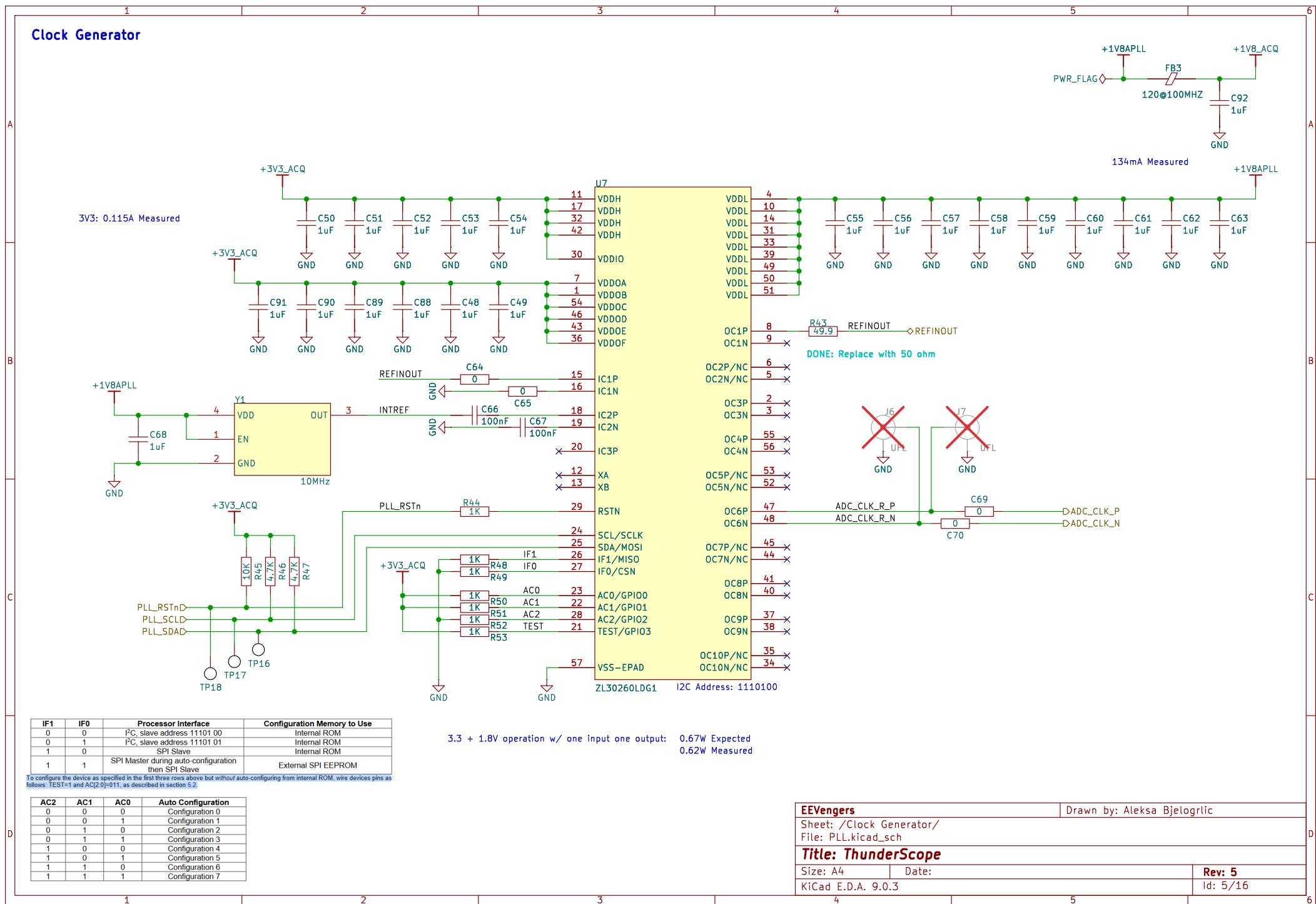
Size: A4 Date:

KiCad E.D.A. 9.0.3

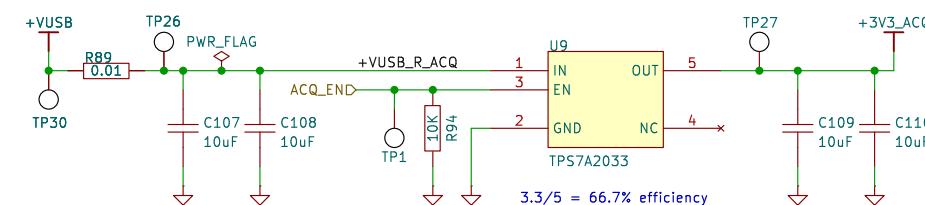
Rev: 5

Id: 4/16

1 2 3 4 5 6

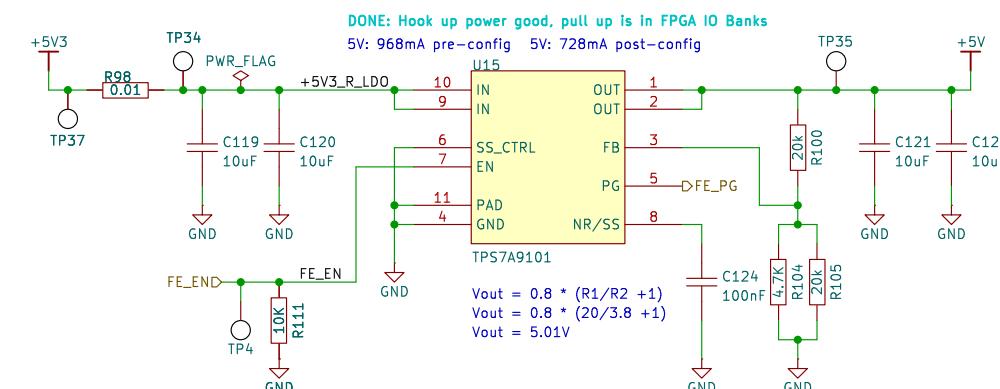


Acquisition Voltage Regulators



DONE: Hook up power good, pull up is in FPGA IO Banks

Front End Voltage Regulators



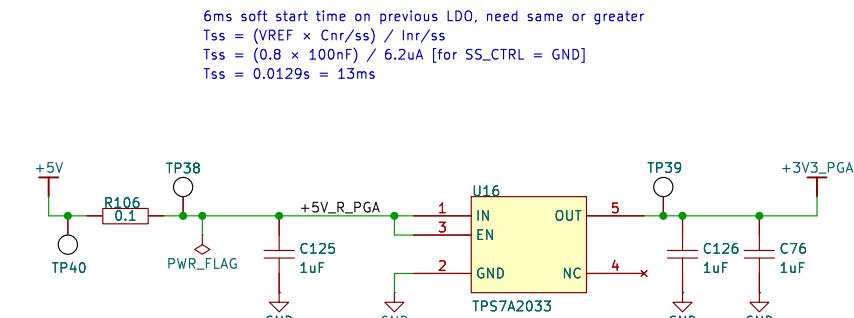
DONE: Hook up power good, pull up is in FPGA IO Banks

5V: 968mA pre-config 5V: 728mA post-config

$V_{out} = 0.8 * (R_1/R_2 + 1)$

$V_{out} = 0.8 * (20/3.8 + 1)$

$V_{out} = 5.01V$



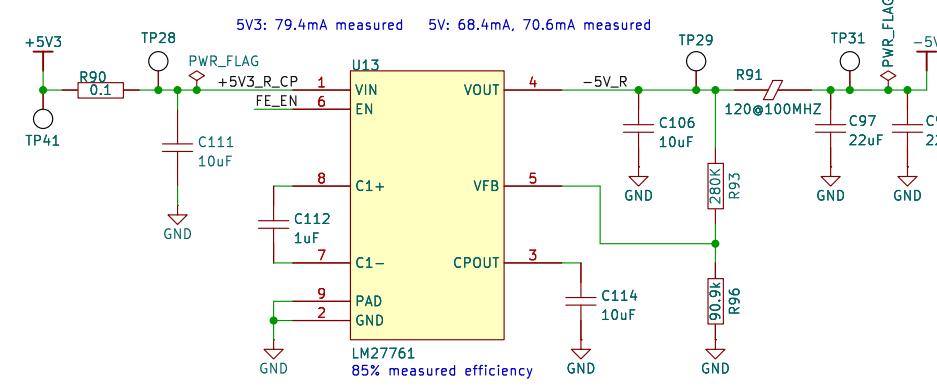
543mA Measured Total: 529mA Expected

$V_{out} = 0.8 * (R_1/R_2 + 1)$

$V_{out} = 0.8 * (4.7/3.8 + 1)$

$V_{out} = 1.79V$

$1.8/2.5 = 72\% \text{ efficiency}$



$V_{out} = -1.22V * (R_1 + R_2) / R_2$
 $V_{out} = -1.22 * (280/90.9 + 1) = -4.98V$
The value for R2 must be no less than 50 kΩ.

EEVengers

Sheet: /ACQ and FE Voltage Regs/
File: ACQ_FE_VREG.kicad_sch

Title: ThunderScope

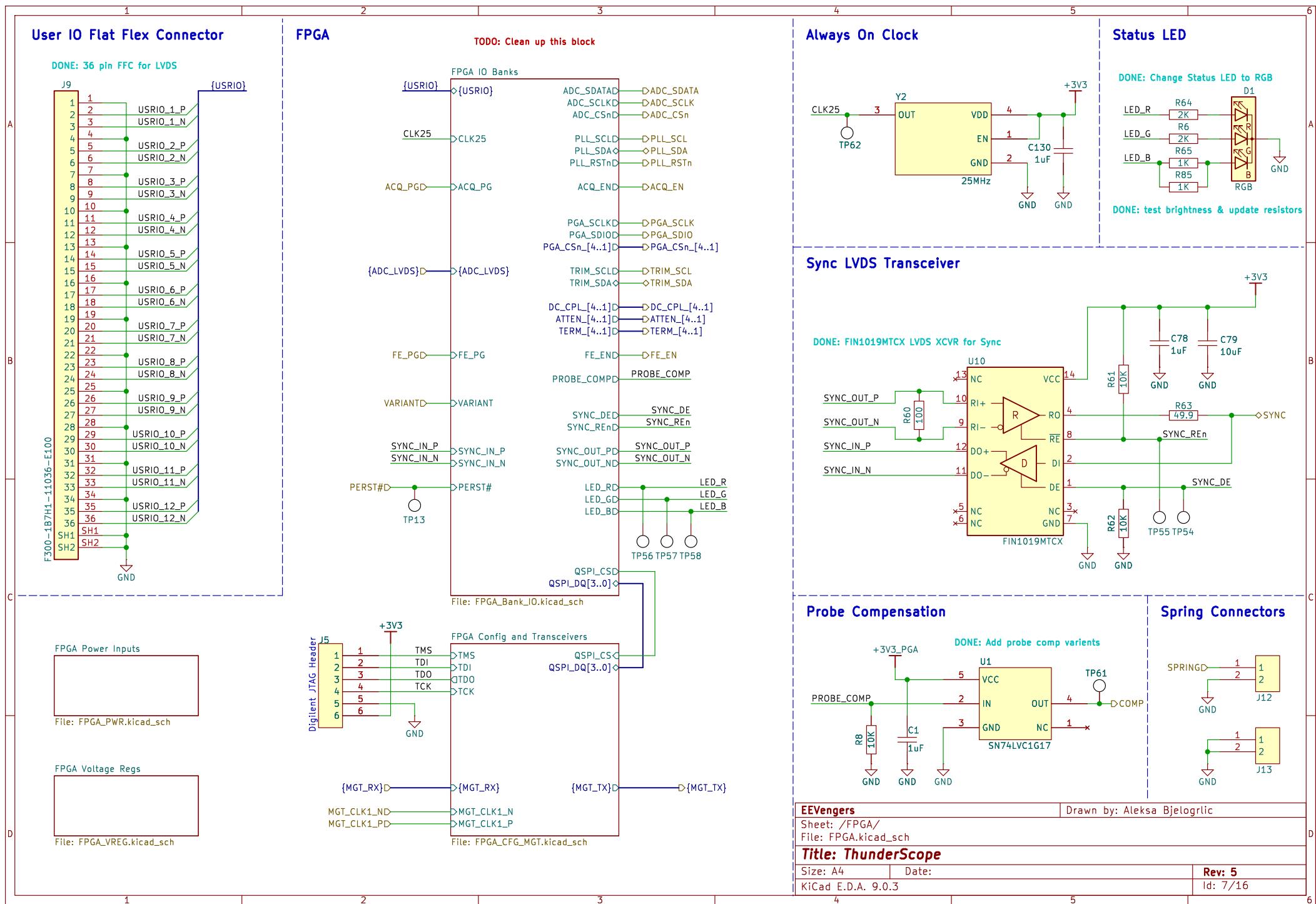
Size: A4 Date:

KiCad E.D.A. 9.0.3

Drawn by: Aleksa Bjelogrlic

Rev: 5

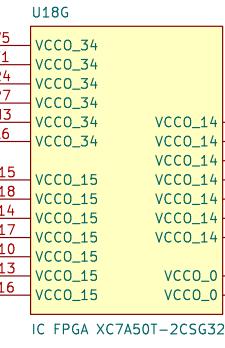
Id: 6/16



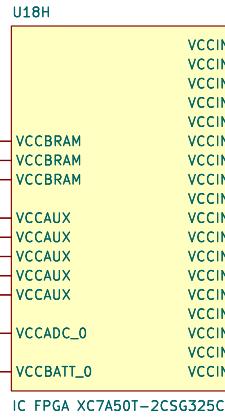
PAGE 1: FPGA Power Inputs

Package	Device	V _{CCINT}				V _{CCBRAM}				V _{CCAUX}				V _{CCO} Bank 0		V _{CCO} all other Banks (per Bank)	
		680 μ F	330 μ F	100 μ F	47 μ F	4.7 μ F	47 μ F	100 μ F	47 μ F	4.7 μ F	47 μ F	4.7 μ F	47 μ F	4.7 μ F	47 μ F	4.7 μ F	
CSG325	XC7A3ST XA7A3ST	0	0	1	0	2	3	0	1	0	1	2	3	1	1	2	4

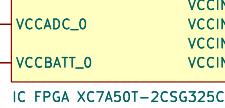
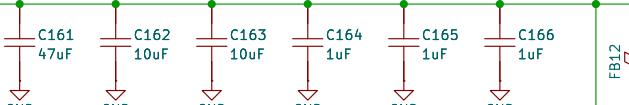
3. One 47 μ F (or 100 μ F) capacitor is required for up to four V_{CCO} banks when powered by the same voltage.



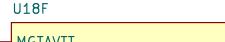
IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C

Capacitor	Package Pins			Value
	MGTAVCC	MGTAVTT	GND	
Cap1		F3	F4	
Cap2		A2	A1	
Cap3	B4		B3	0.1 μ F
Cap4	F5		F6	

Qty/Power Supply Group	MGTAVCC	MGTAVTT	Capacitance (μ F)	Tolerance	Type
					Ceramic
1	1	1	4.7	10%	Ceramic
2	2	2	0.1	10%	Ceramic

1 2 3 4 5 6

1 2 3 4 5 6

EEVengers

Sheet: /FPGA/FPGA Power Inputs/
File: FPGA_PWR.kicad_sch

Title: ThunderScope

Size: A4 Date:

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Rev: 5
Id: 10/16

1 2 3 4 5 6

1 2 3 4 5 6

1 2 3 4 5 6

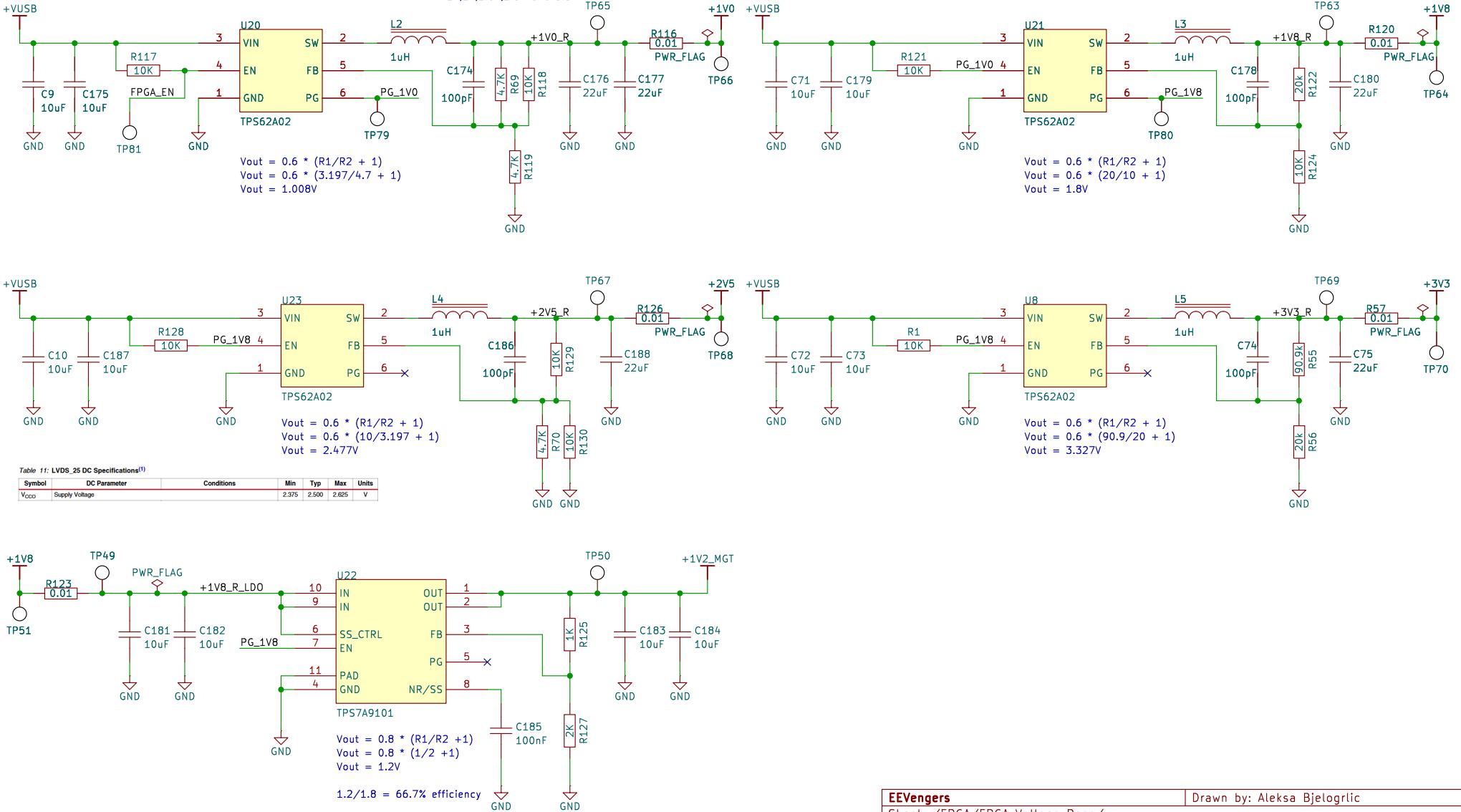
1 2 3 4 5 6

1 2 3 4 5 6

1 2 3 4 5 6

FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V



EEVengers

Sheet: /FPGA/FPGA Voltage Regs/
File: FPGA_VREG.kicad_sch

Title: ThunderScope

Size: A4 Date:

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Drawn by: Aleksa Bjelogrlic

Rev: 5

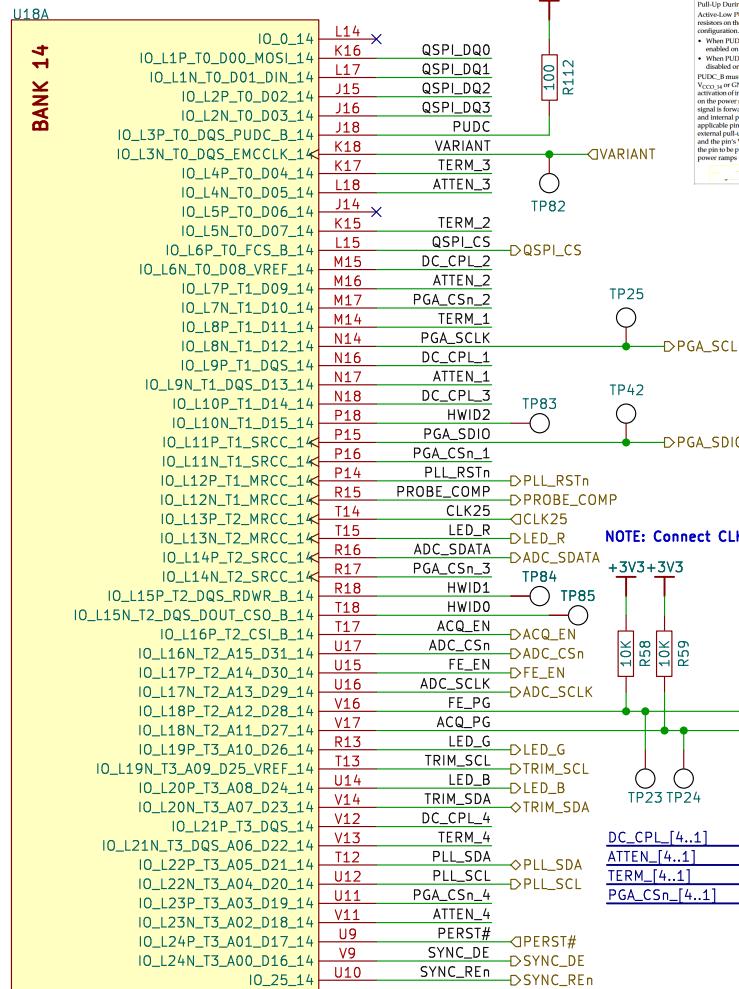
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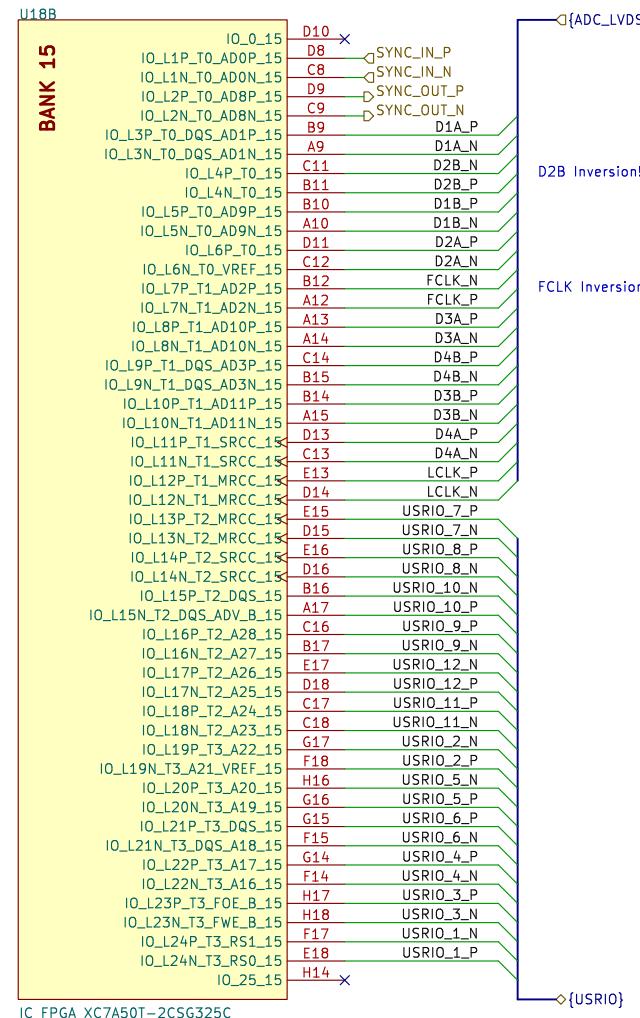
FPGA IO Banks

QSPI_DQ[3..0] — QSPI_DQ[3..0]

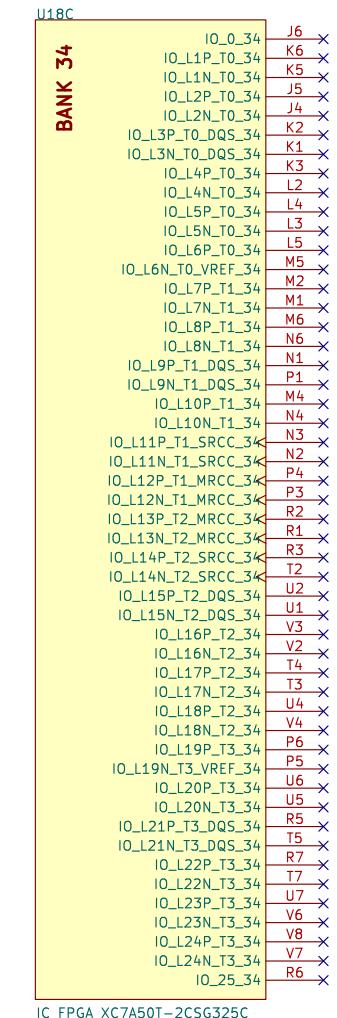
Full TP Coverage on Bank 14 Signals (except PUDC)



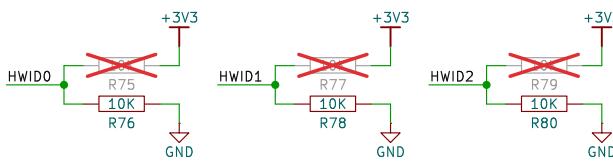
IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C

**EEVengers**

Sheet: /FPGA/FPGA IO Banks/
File: FPGA_Bank_IO.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 9.0.3

Drawn by: Aleksa Bjelogrlic

Rev: 5

Id: 8/16

FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

Note: DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and

Table 2-1: 7 Series FPGA Configuration Modes			
Configuration Mode	M2[0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

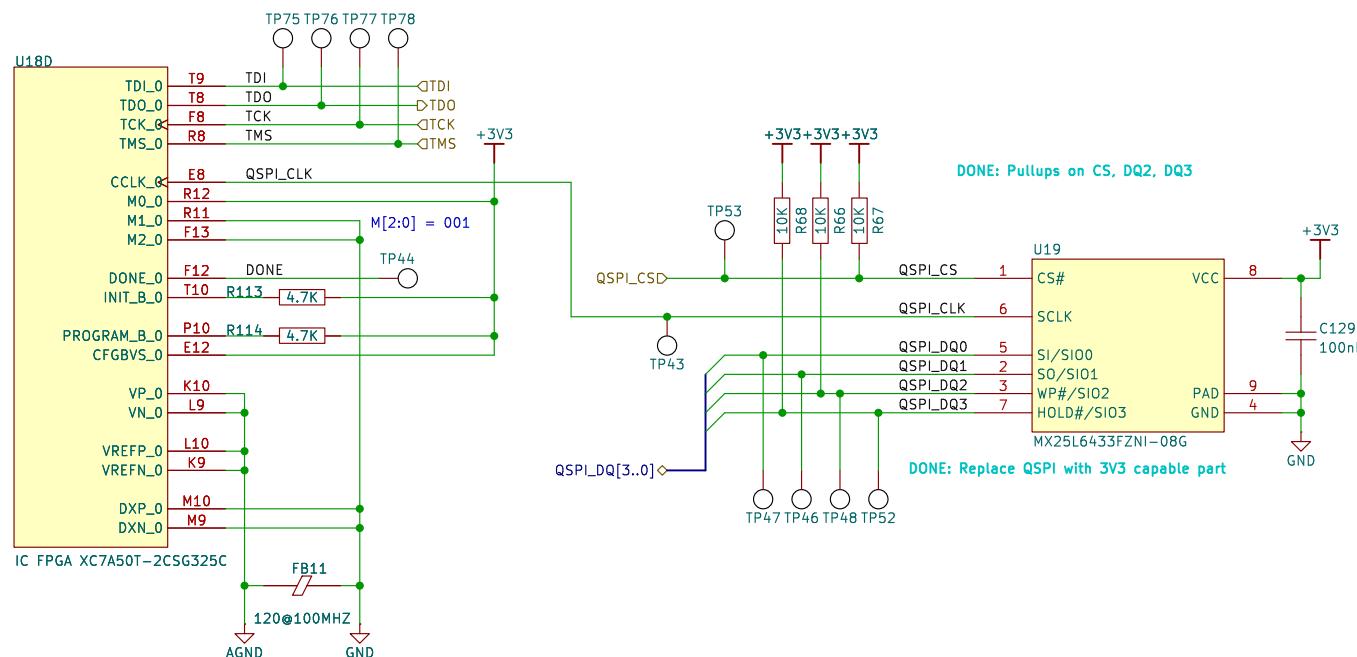
Table 2-2: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Bank Used	Configuration Interface I/O	HR Bank 0 V _{CCO} 4	HR Bank 14 V _{CCO} 14	HR Bank 15 V _{CCO} 15	CFGBVS
JTAG (only)	0	VREFP_0	3.3V	3.3V	Any	VCCO_0
		VREFN_0	2.5V	2.5V	Any	VCCO_0
		VREFP_0	1.8V	1.8V	Any	GND
		VREFN_0	1.5V	1.5V	Any	GND
Serial SPI or SelectMAP	0, 14 ⁽¹⁾	DXP_0	3.3V	3.3V	3.3V	VCCO_0
		DXN_0	2.5V	2.5V	2.5V	VCCO_0
		VREFP_0	1.8V	1.8V	1.8V	GND
		VREFN_0	1.5V	1.5V	1.5V	GND
BPI ⁽²⁾	0, 14, 15	VREFP_0	3.3V	3.3V	3.3V	VCCO_0
		VREFN_0	2.5V	2.5V	2.5V	VCCO_0
		VREFP_0	1.8V	1.8V	1.8V	GND
		VREFN_0	1.5V	1.5V	1.5V	GND

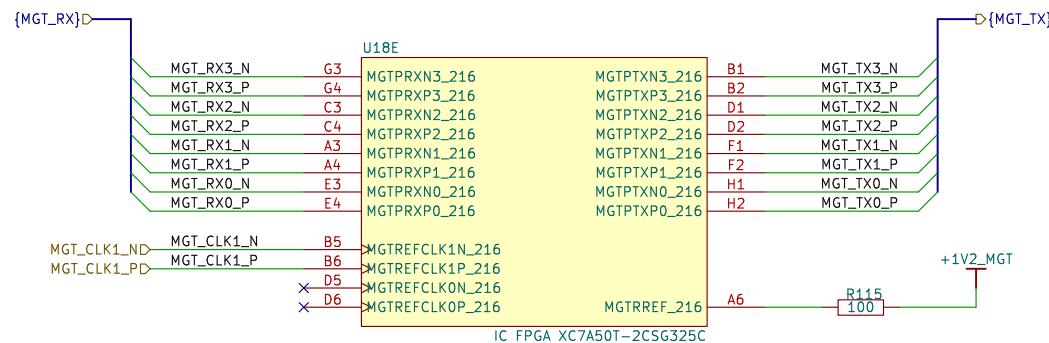
Notes:

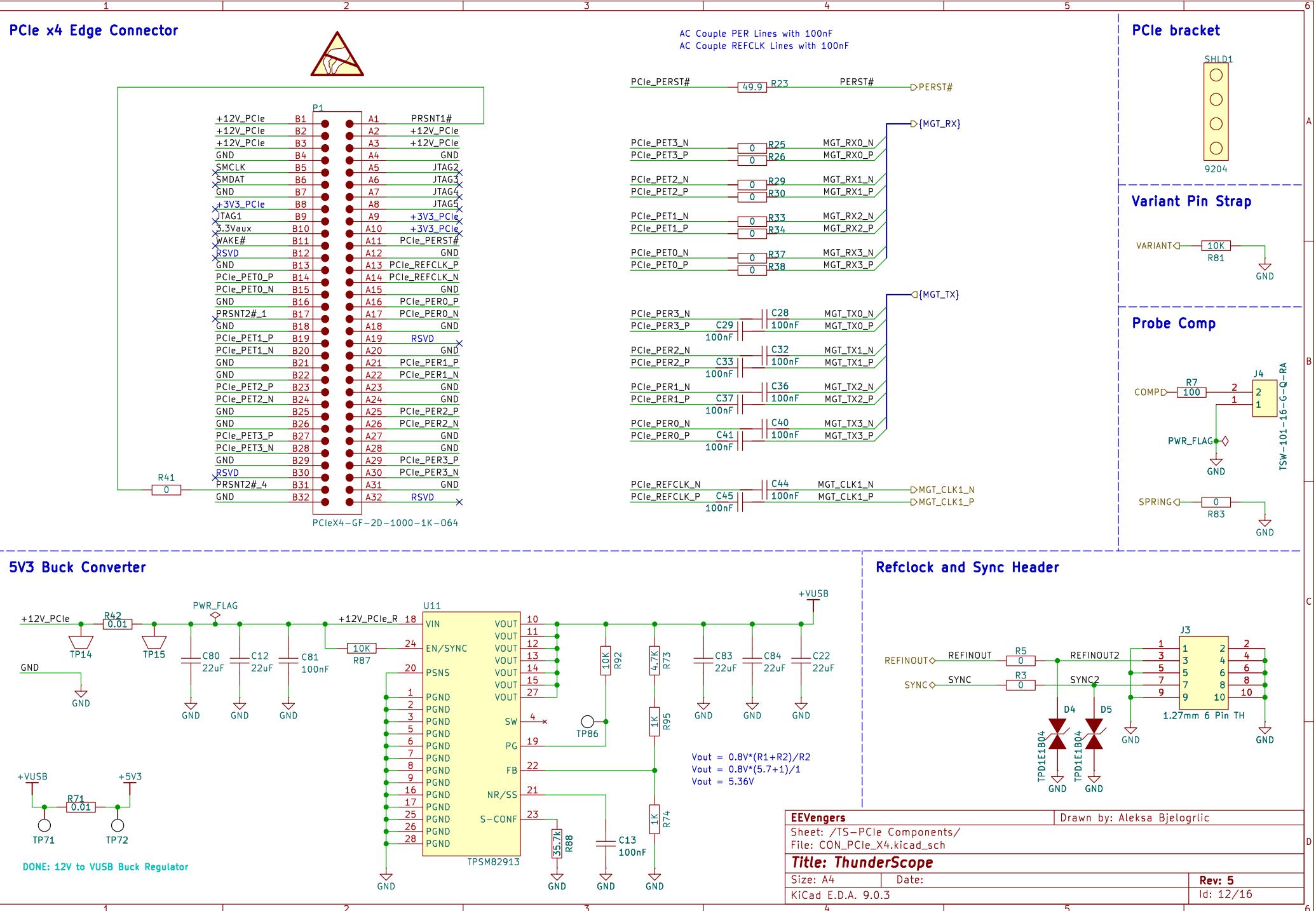
1. RS1 of Multifuse or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.

2. BPI mode is not available in the Spartan-7 family.

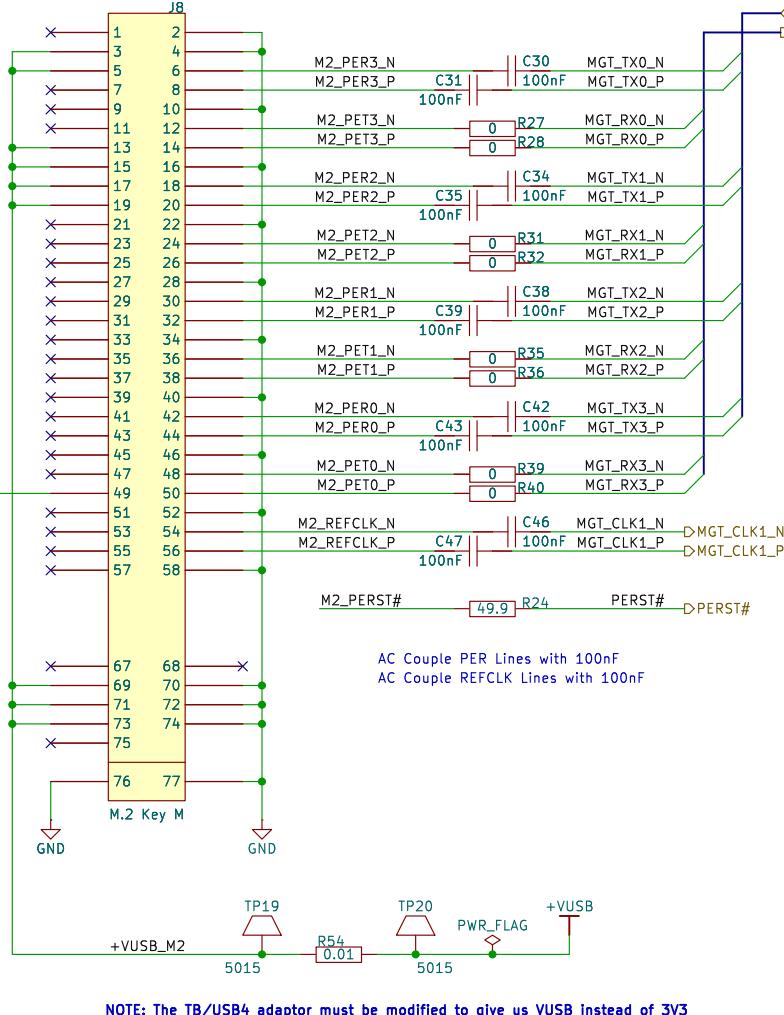


FPGA Transceivers

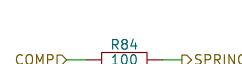




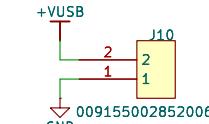
M.2 Key M Connector – Custom Pinout



Probe Comp



Fan Connector



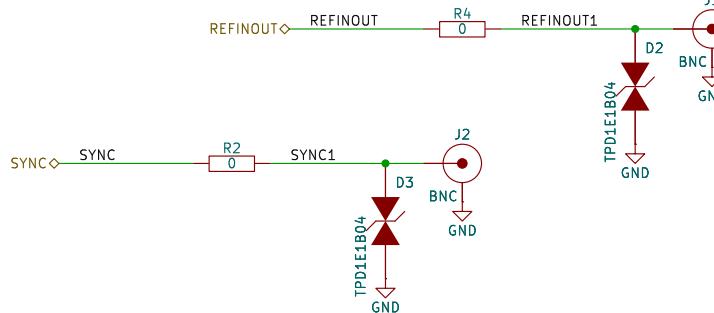
Ground Lug



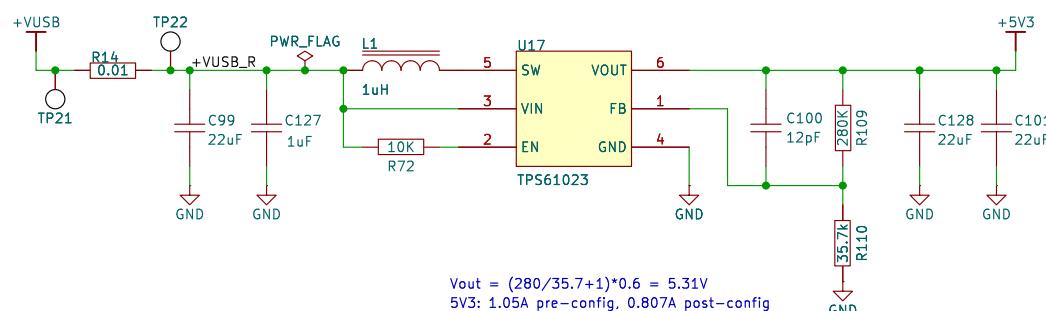
Variant Pin Strap



Refclock and Sync BNCs



5V3 Boost Converter



Interposer Standoffs



EEVengers

Sheet: /TS-USB4 Components/
File: M2_KEY_M.kicad_sch

Title: ThunderScope

Size: A4 Date:

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