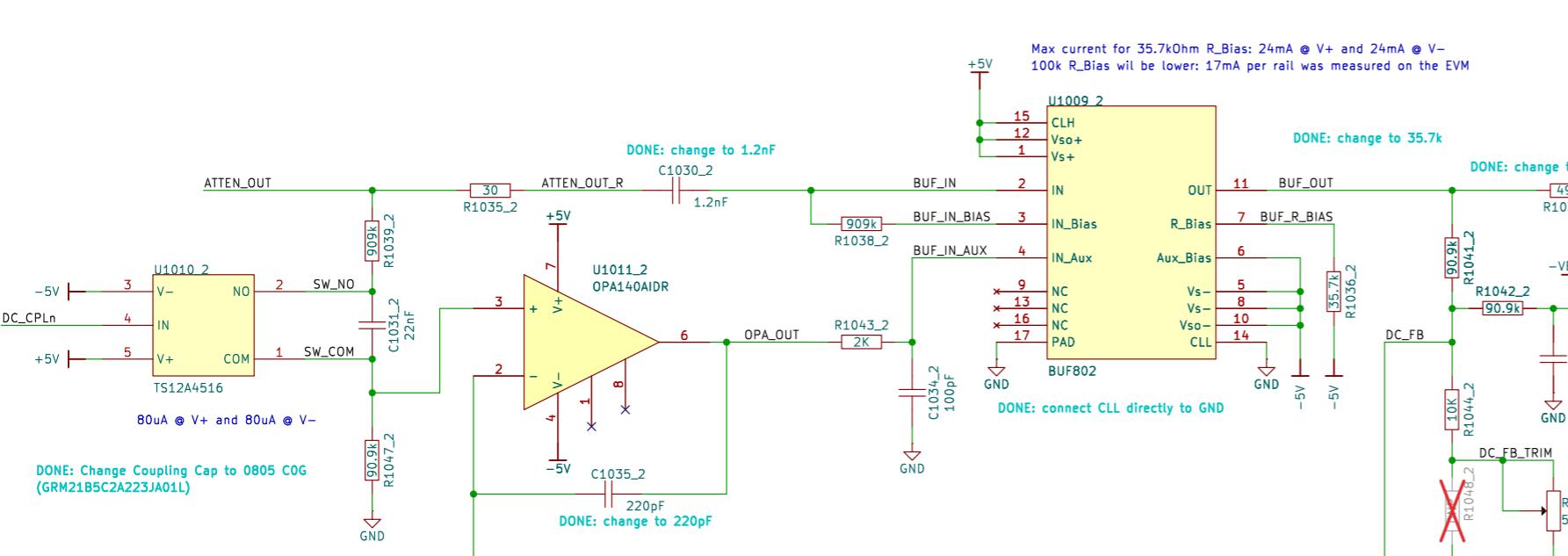
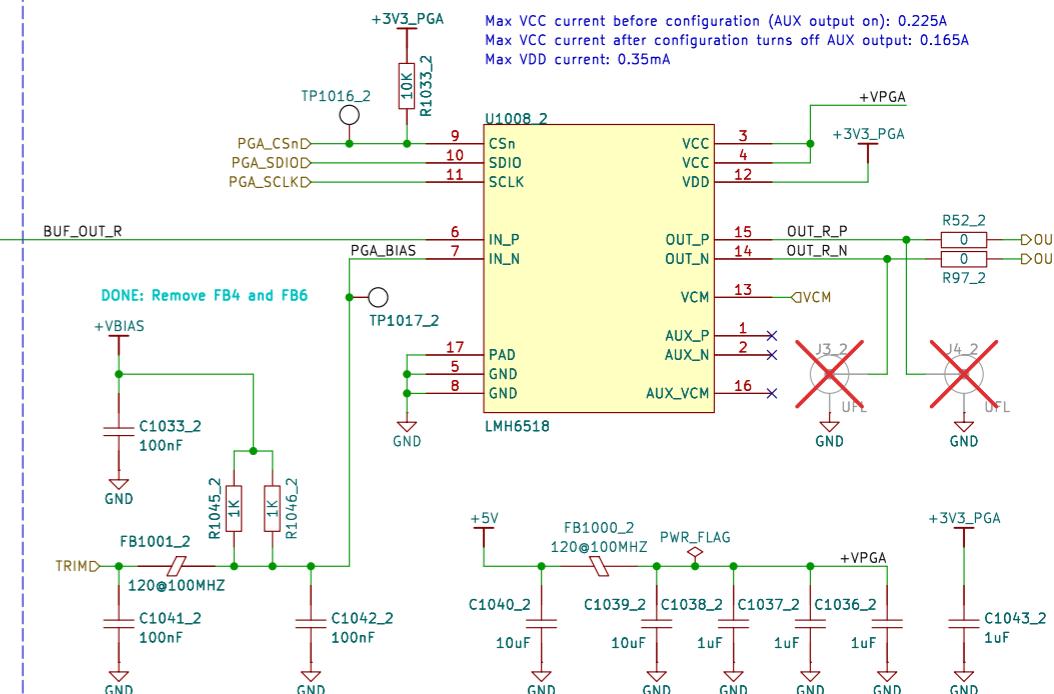


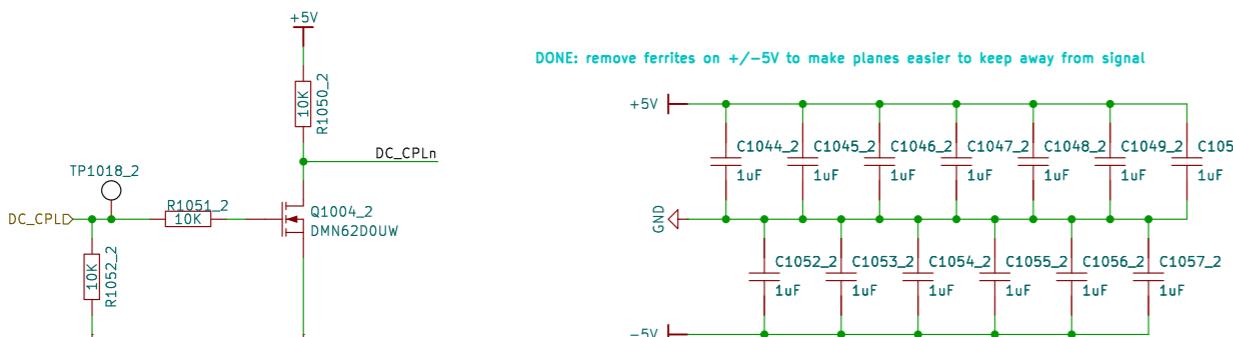
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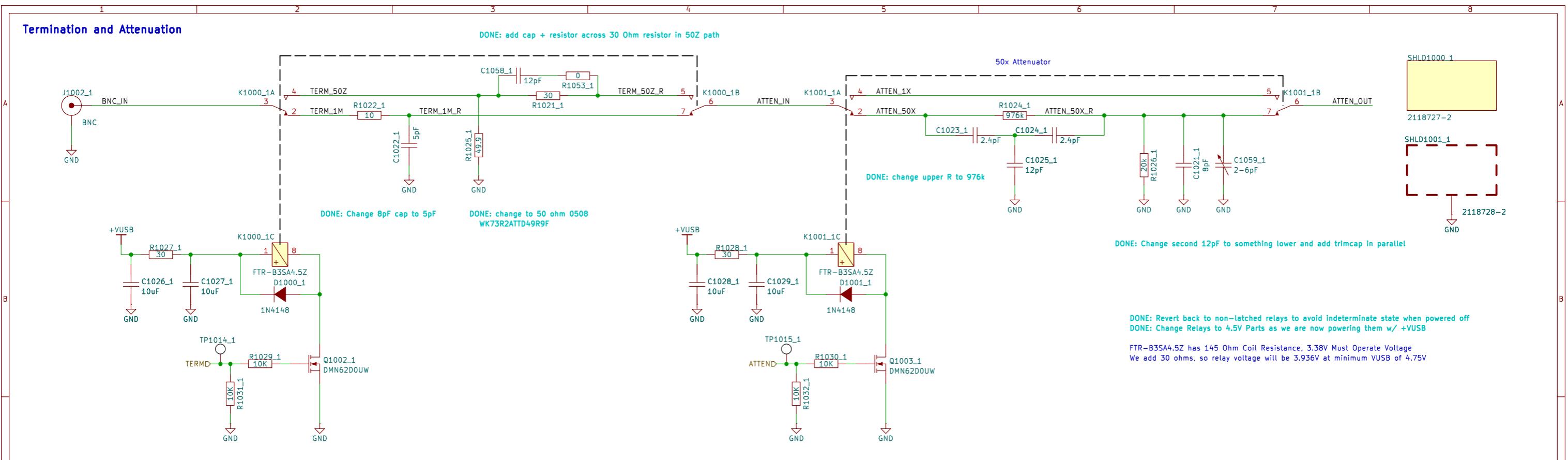


## Programmable Gain Amplifier

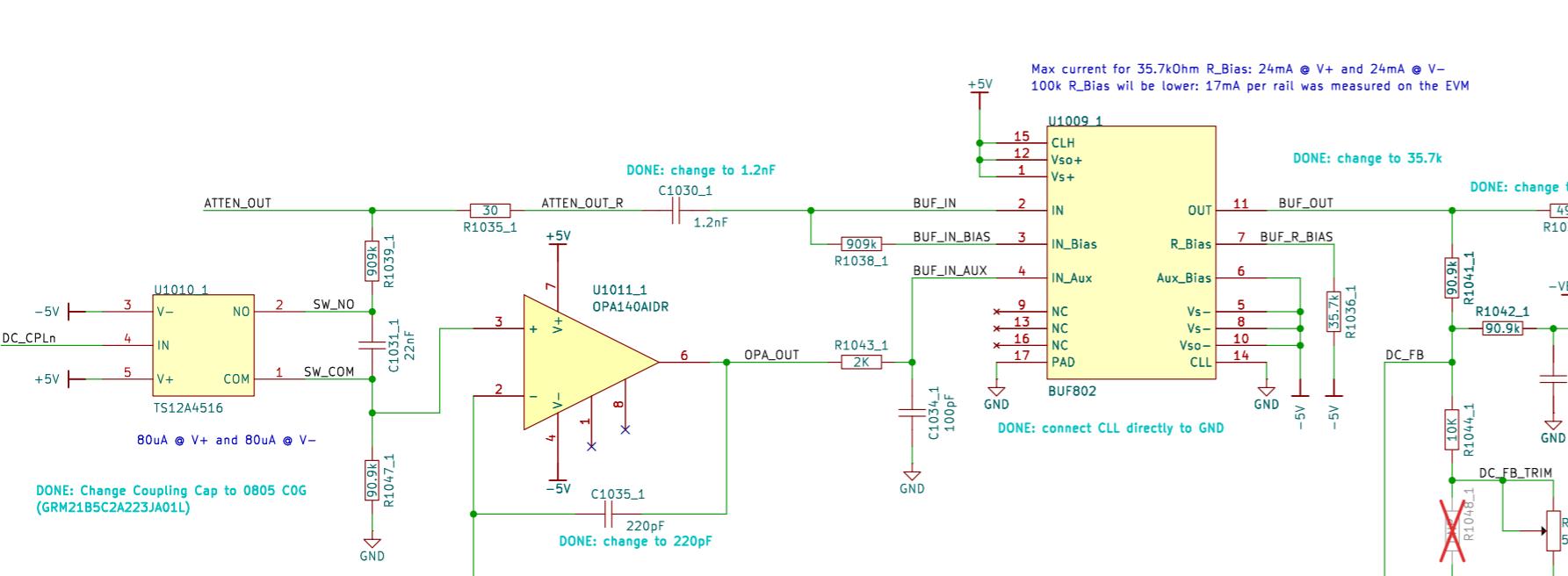


DONE: Revert to Mechanical Trimpot

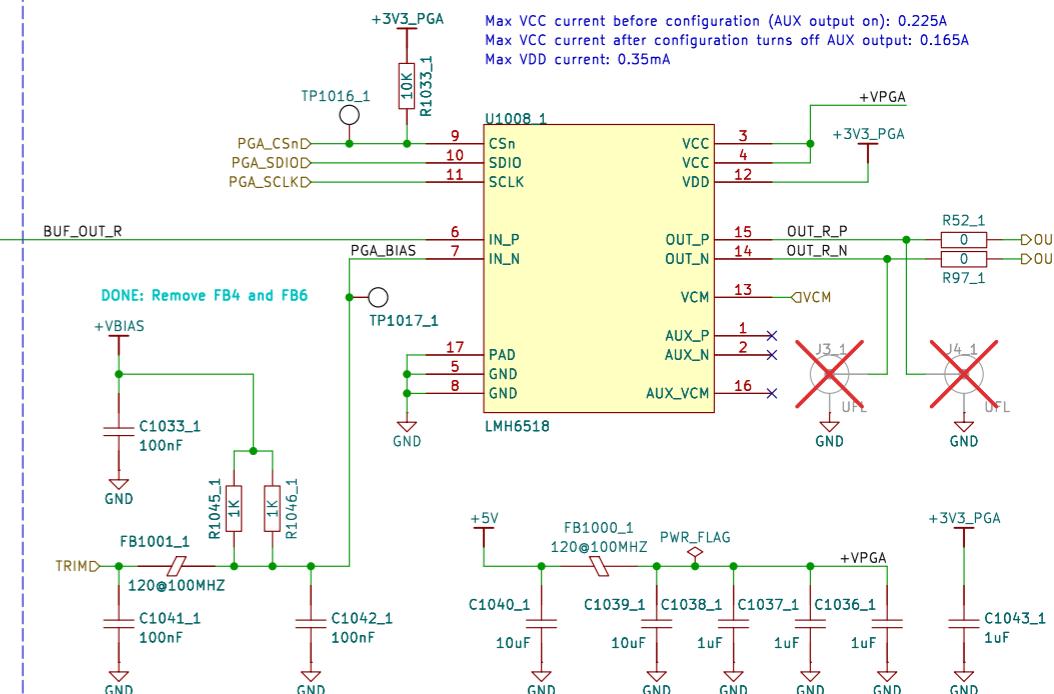




## Input Buffer and AC/DC Coupling



## Programmable Gain Amplifier



EEVengers

| Drawn by: Aleksa Bielogrlic

Sheet: /CH1/

Brown, S.J., Krebs, D.J. 2009. *Ecological Methods*. Springer, New York.

File: FE\_Channel.kicad\_sch

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**Title: ThunderScope**

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Size: A3 Date:

Rev: 1

KiCad E.D.A. 9.0.0

2 : D1

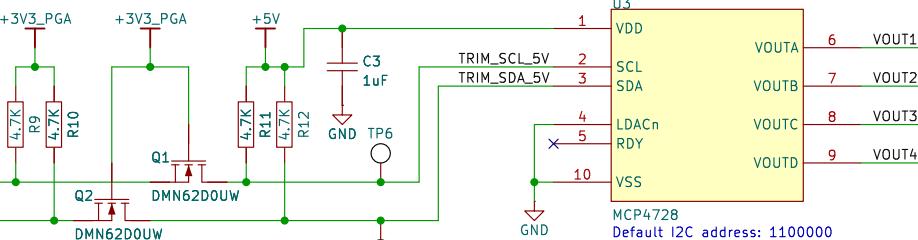
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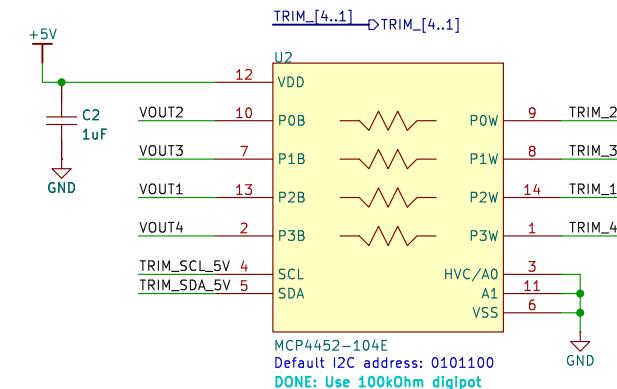
1 2 3 4 5 6

## Offset Voltage Trim and User Offset Control

A

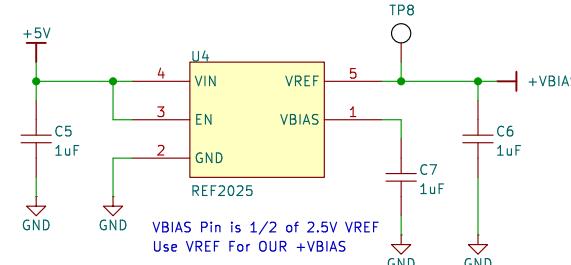


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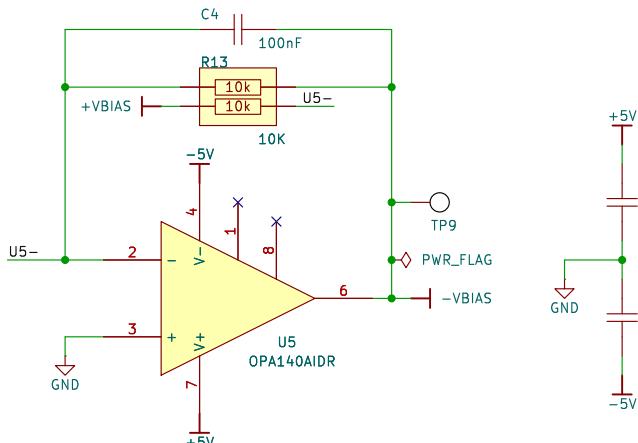
## Bias Voltage Generation

C



D

Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140  
-Max resistance is  $(575/4 // 10k) = 141.7 \text{ Ohm}$   
-Worst case current is  $17.64\text{mA}$   
-Use REF2025, has max current of  $20\text{mA}$   
-Change U5 divider to matched resistor network  
-ACASN1002S1002P1AT



EEVengers

Sheet: /Front End Trim and Bias/  
File: FE.kicad\_sch

Title: ThunderScope

Size: A4 Date:

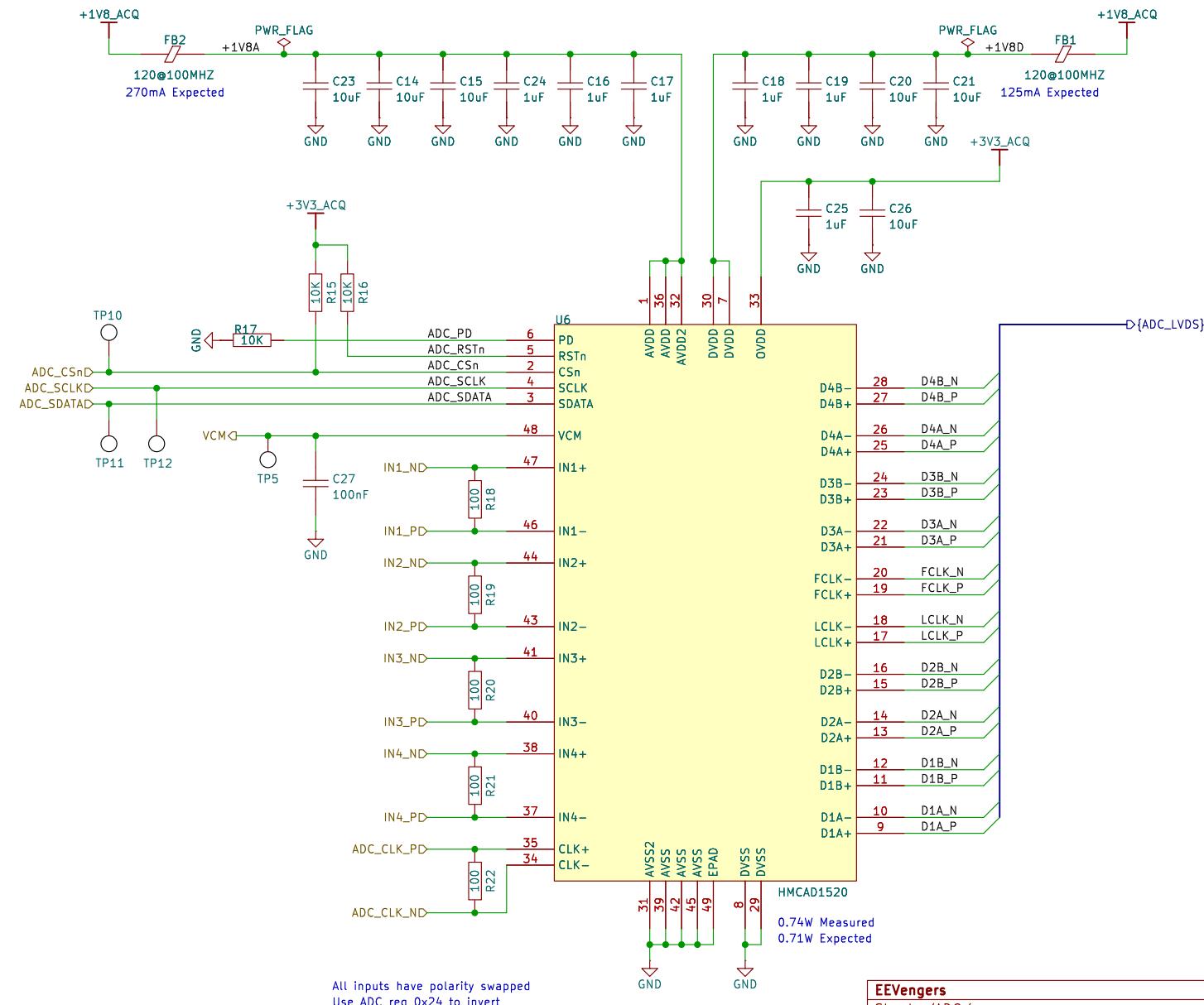
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Drawn by: Aleksa Bjelogrlic

Rev: 5  
Id: 3/16

1 2 3 4 5 6

1 2 3 4 5 6

**ADC**

EEVengers

Drawn by: Aleksa Bjelogrlic

Sheet: /ADC/

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**Title: ThunderScope**

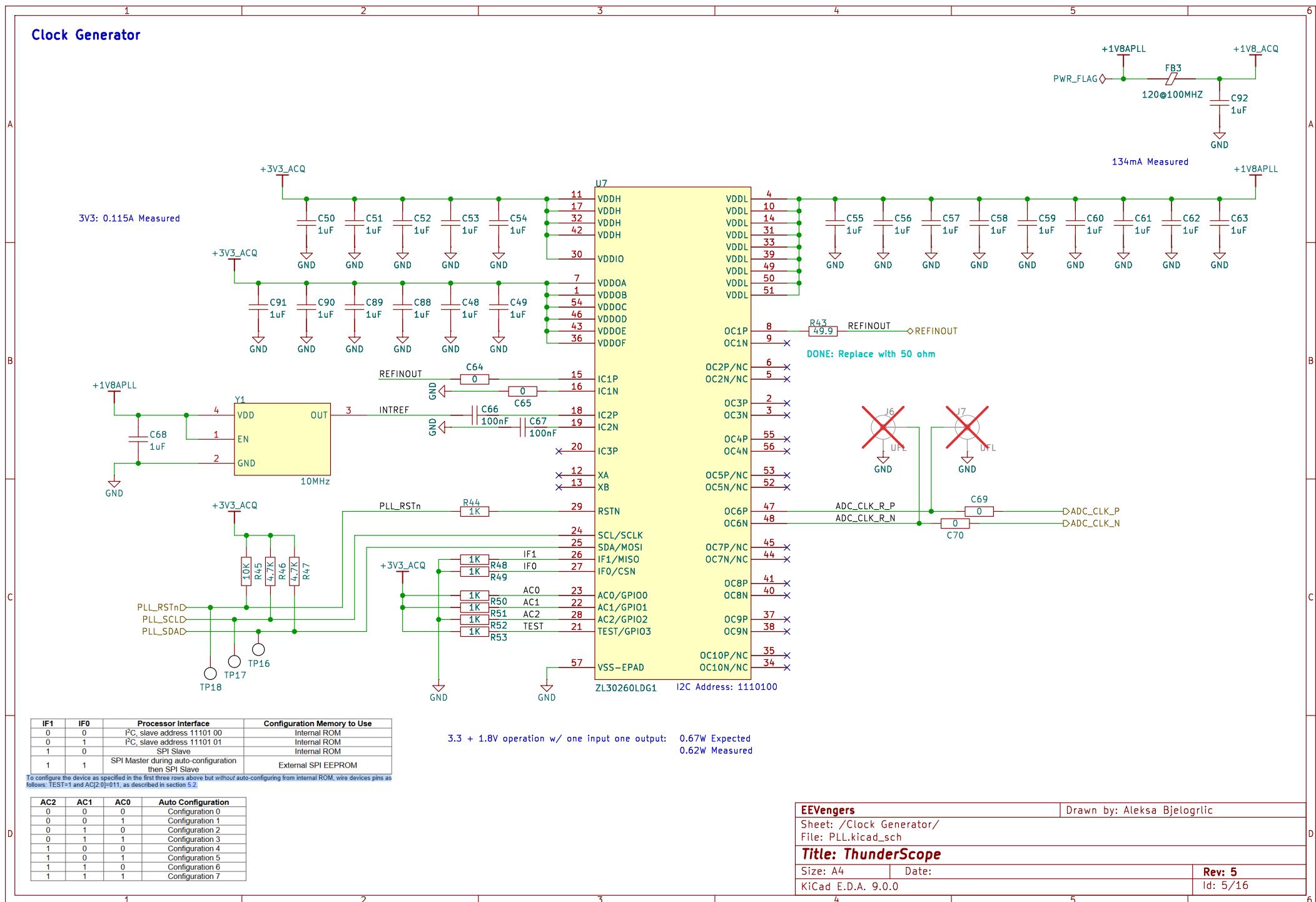
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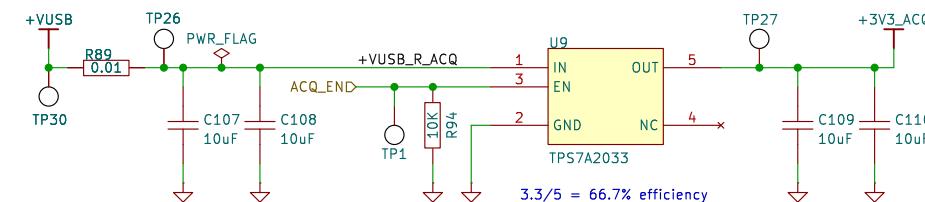
Rev: 5

Id: 4/16

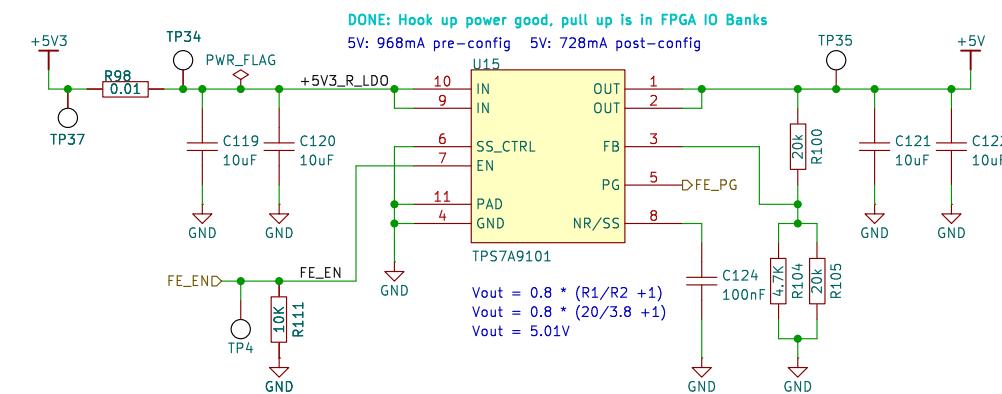
1 2 3 4 5 6



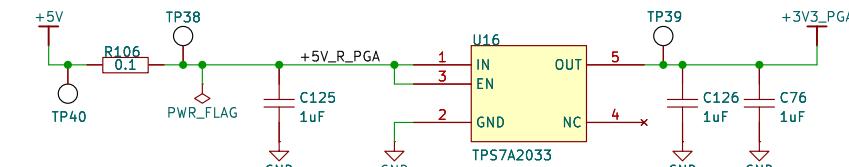
## Acquisition Voltage Regulators



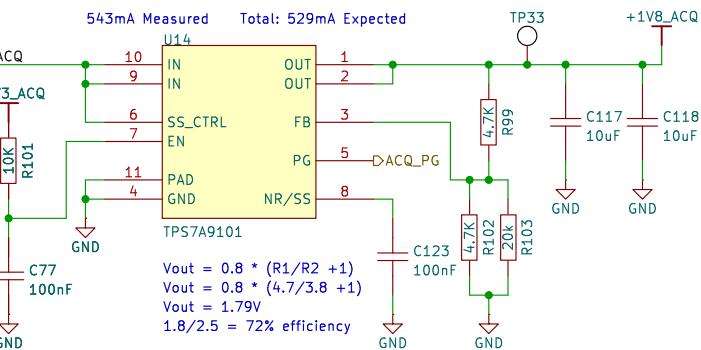
## Front End Voltage Regulators



6ms soft start time on previous LDO, need same or greater  
 $T_{ss} = (V_{REF} \times C_{nr/ss}) / I_{nr/ss}$   
 $T_{ss} = (0.8 \times 100nF) / 6.2\mu A$  [for SS\_CTRL = GND]  
 $T_{ss} = 0.0129s = 13ms$

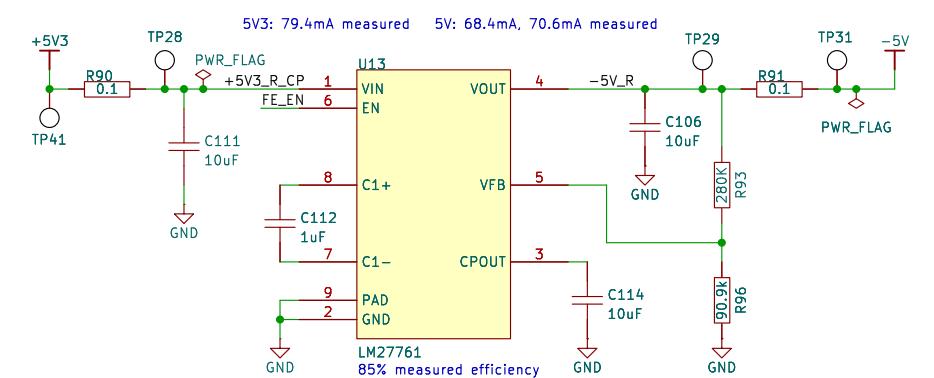


DONE: Hook up power good, pull up is in FPGA IO Banks



54.3mA Measured Total: 529mA Expected

Vout = 0.8 \* (R1/R2 + 1)  
 $V_{out} = 0.8 * (4.7/3.8 + 1)$   
 $V_{out} = 1.79V$   
 $1.8/2.5 = 72\% \text{ efficiency}$



Vout =  $-1.22V(R_1+R_2)/R_2$   
 $V_{out} = -1.22 \times (280/90.9+1) = -4.98V$   
 The value for R2 must be no less than 50 kΩ.

EEVengers

Sheet: /ACQ and FE Voltage Regs/  
 File: ACQ\_FE\_VREG.kicad\_sch

Title: ThunderScope

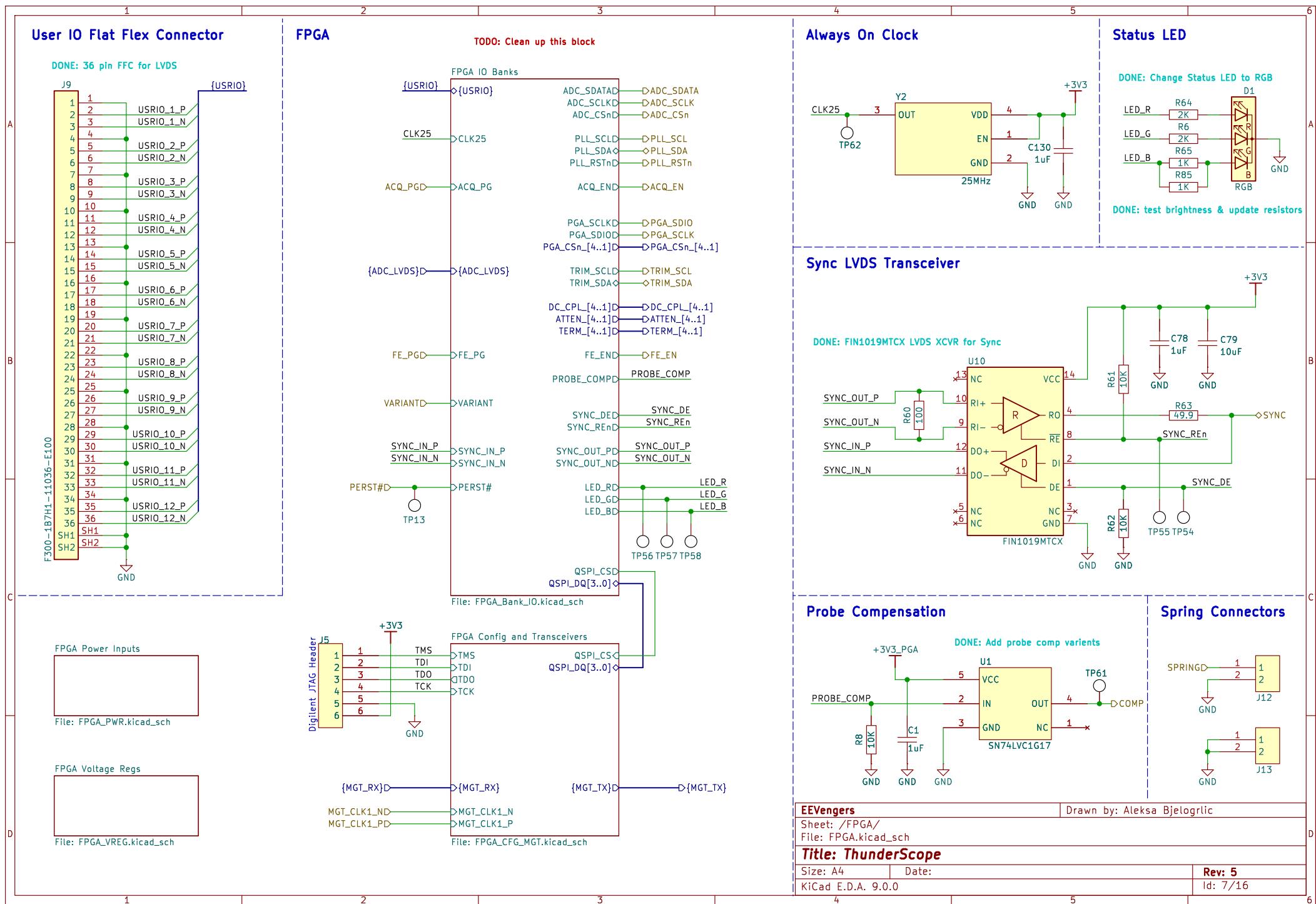
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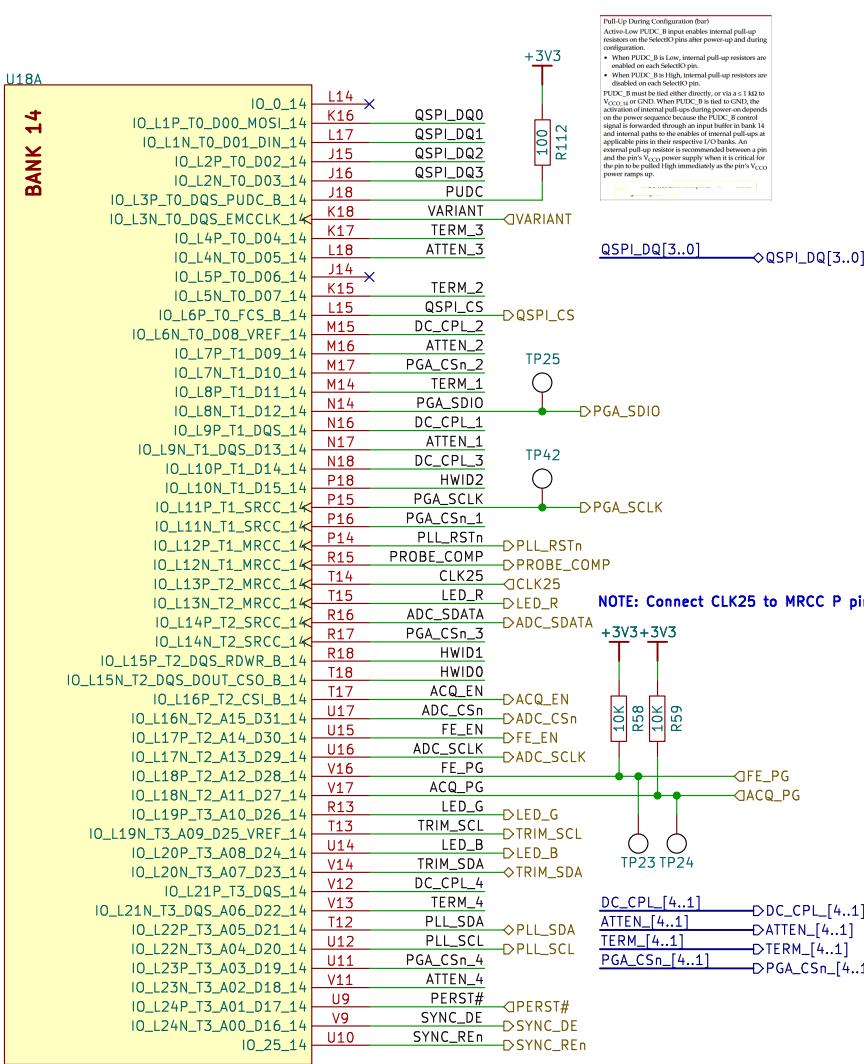
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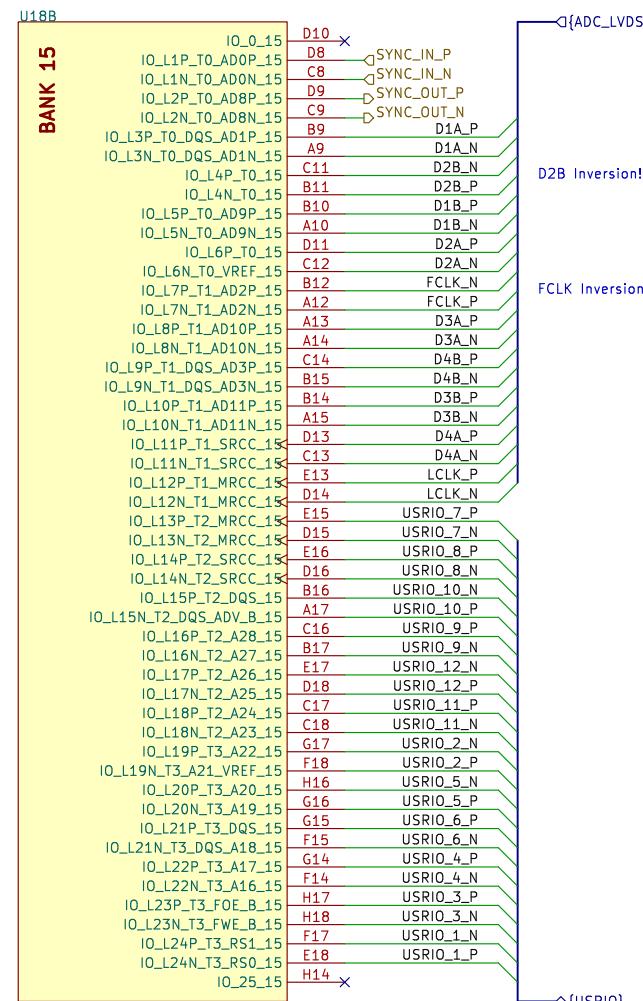


**FPGA IO Banks**

A



B



C



## FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

**Note:** DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

Connect INIT\_B to a ≤ 4.7 kΩ pull-up resistor to V<sub>CCO\_0</sub> to ensure clean Low-to-High transitions.

Connect PROGRAM\_B to an external ≤ 4.7 kΩ pull-up resistor to V<sub>CCO\_0</sub> to ensure a stable High input, and

Table 2-1: 7 Series FPGA Configuration Modes			
Configuration Mode	M2[0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

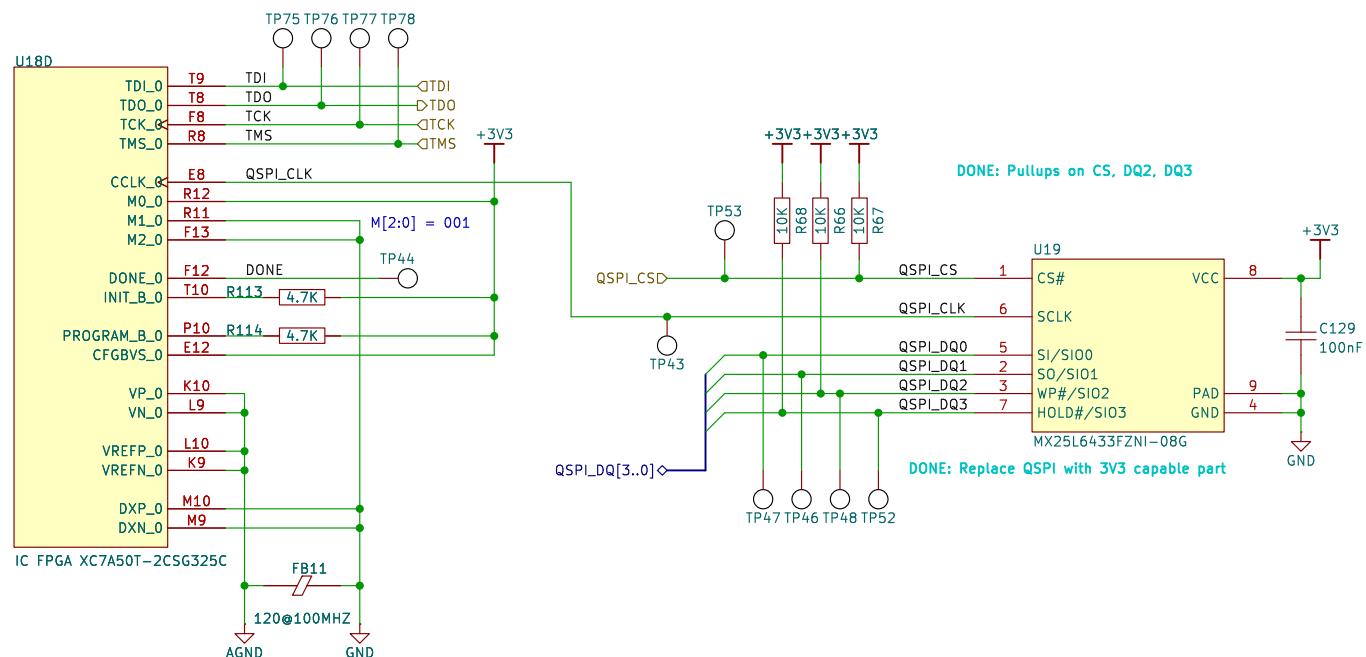
Table 2-2: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Bank Used	Configuration Interface I/O	HR Bank 0 V <sub>CCO</sub> 4	HR Bank 14 V <sub>CCO</sub> 14	HR Bank 15 V <sub>CCO</sub> 15	CFGBVS
JTAG (only)	0	VREFP_0	3.3V	3.3V	Any	VCCO_0
		VREFN_0	2.5V	2.5V	Any	VCCO_0
		VREFP_0	1.8V	1.8V	Any	GND
		VREFN_0	1.5V	1.5V	Any	GND
Serial SPI or SelectMAP	0, 14 <sup>(1)</sup>	DXP_0	3.3V	3.3V	3.3V	VCCO_0
		DXN_0	2.5V	2.5V	2.5V	VCCO_0
		VREFP_0	1.8V	1.8V	1.8V	GND
		VREFN_0	1.5V	1.5V	1.5V	GND
BPI <sup>(2)</sup>	0, 14, 15	VREFP_0	3.3V	3.3V	3.3V	VCCO_0
		VREFN_0	2.5V	2.5V	2.5V	VCCO_0
		VREFP_0	1.8V	1.8V	1.8V	GND
		VREFN_0	1.5V	1.5V	1.5V	GND

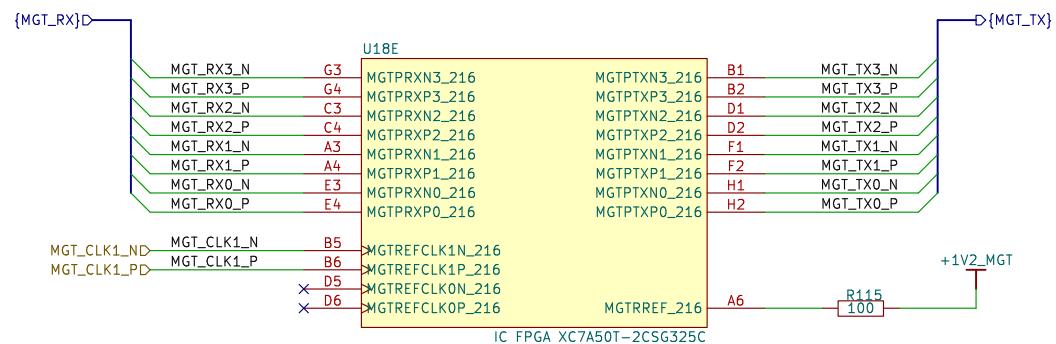
Notes:

1. RS1 of Multiflash or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.

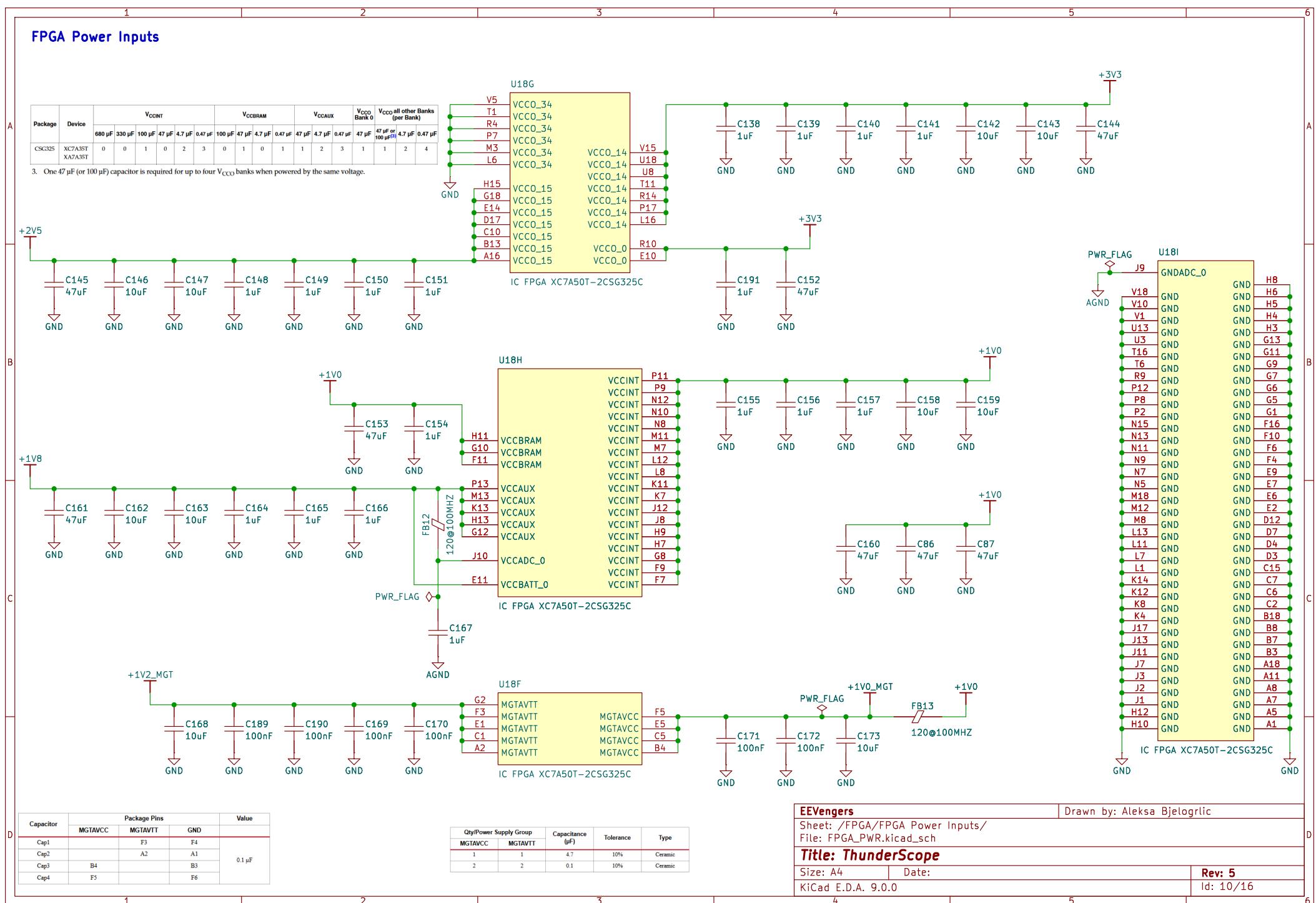
2. BPI mode is not available in the Spartan-7 family.



## FPGA Transceivers



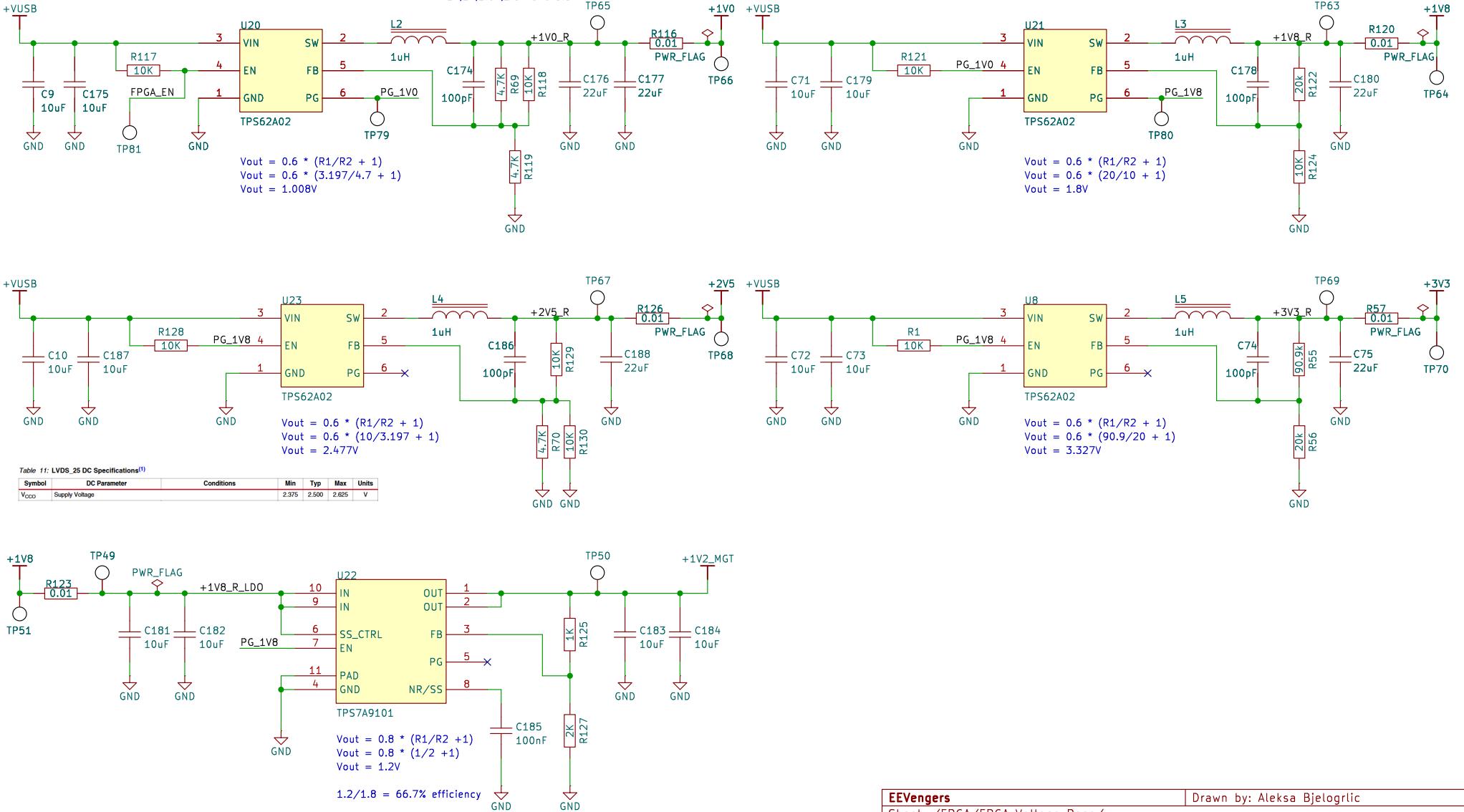
## PAGE 1: FPGA Power Inputs



1 2 3 4 5 6

## FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO  
1V,1V,1.8V,2.5V and 3.3V



The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT  
1V,1V,1.2V

### EEVengers

Sheet: /FPGA/FPGA Voltage Regs/  
File: FPGA\_VREG.kicad\_sch

### Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 9.0.0

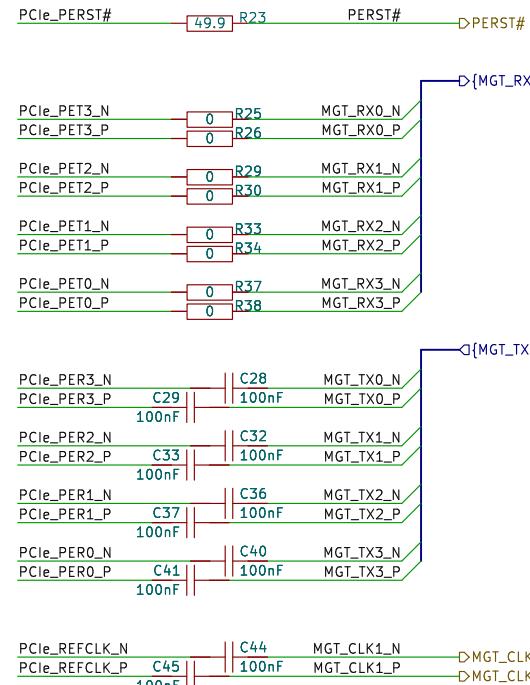
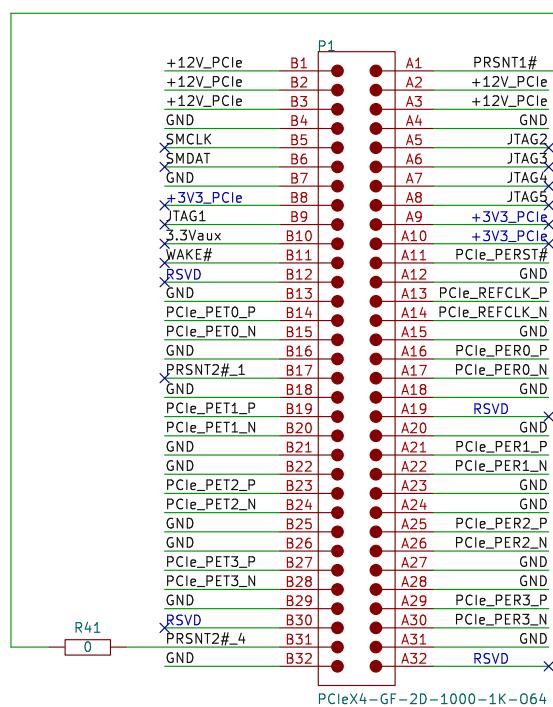
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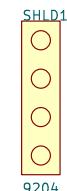
1 2 3 4 5 6

1 2 3 4 5 6

### PCIe x4 Edge Connector



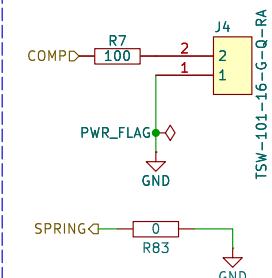
### PCIe bracket



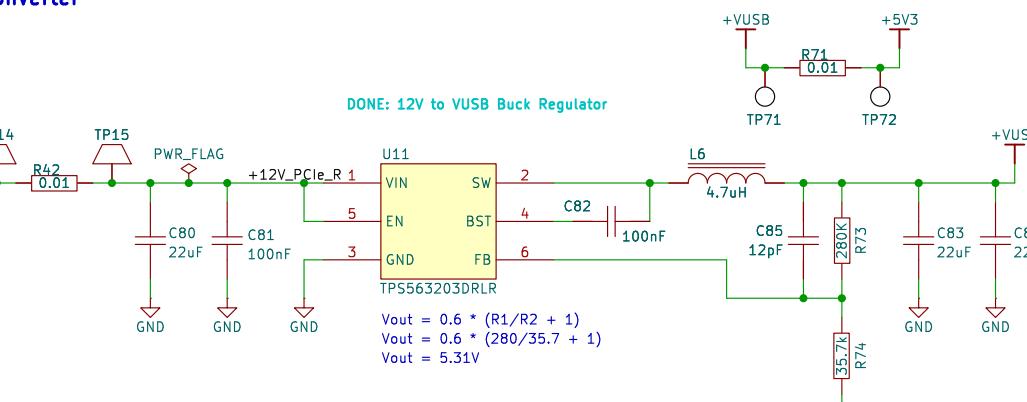
### Variant Pin Strap



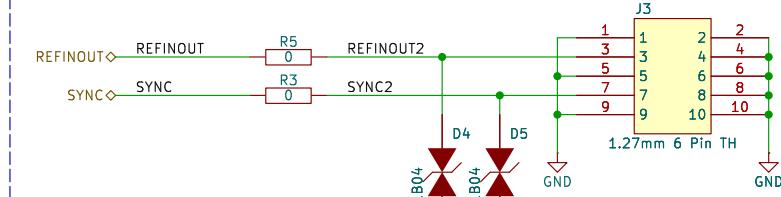
### Probe Comp



### 5V3 Buck Converter



### Refclock and Sync Header



EEVengers

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File: CON\_PCIe\_X4.kicad\_sch

Title: ThunderScope

Size: A4 Date:

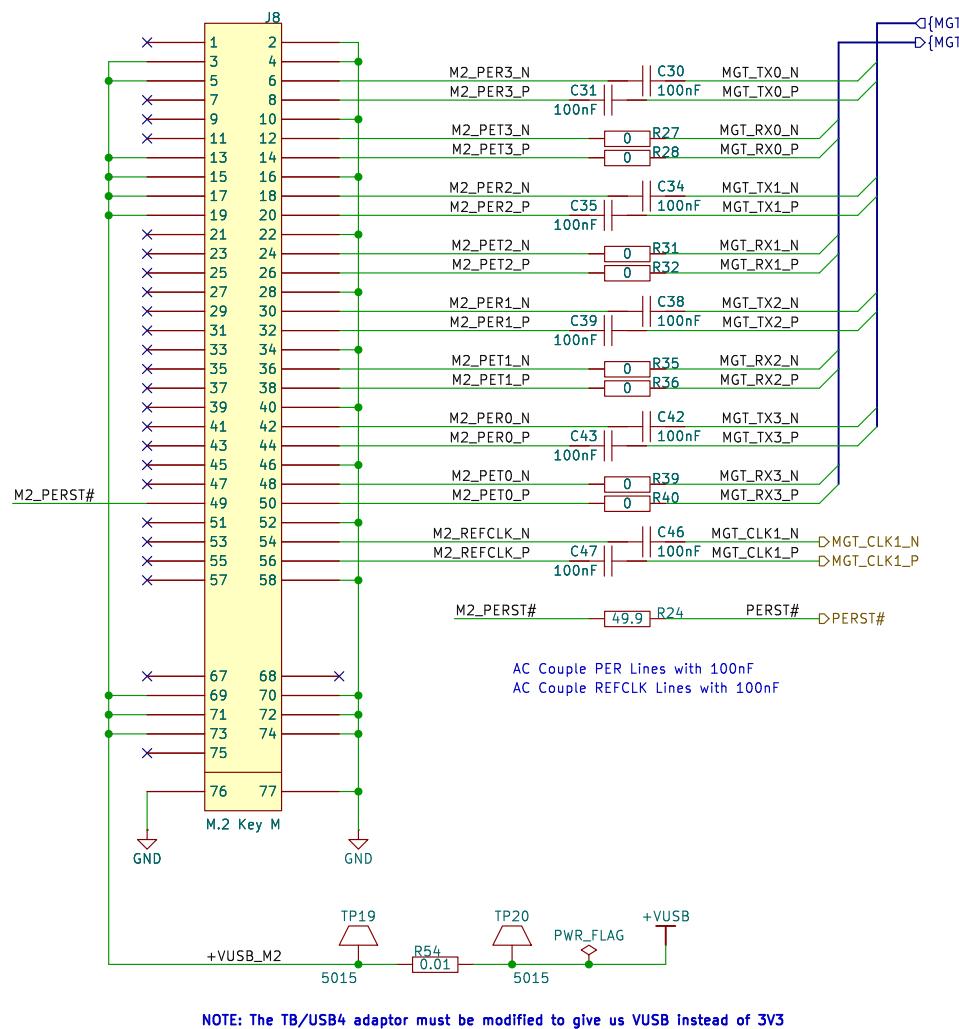
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## M.2 Key M Connector – Custom Pinout



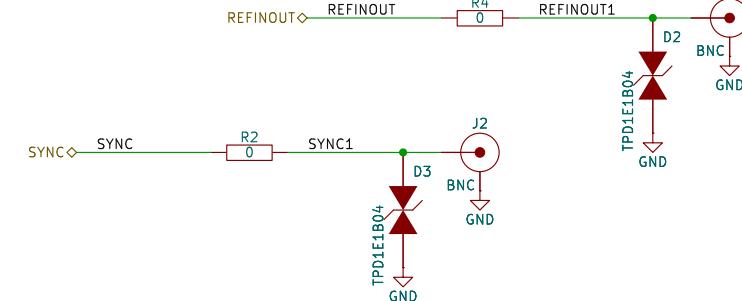
## Interposer Standoffs



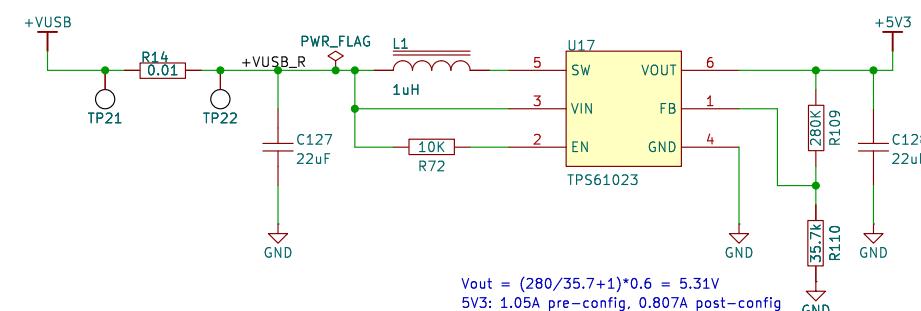
## Probe Comp

COMPD → R84 100 → SPRING

## Refclock and Sync BNCs



## 5V3 Boost Converter



EEVengers

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Title: ThunderScope

Size: A4 Date:

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Rev: 5  
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