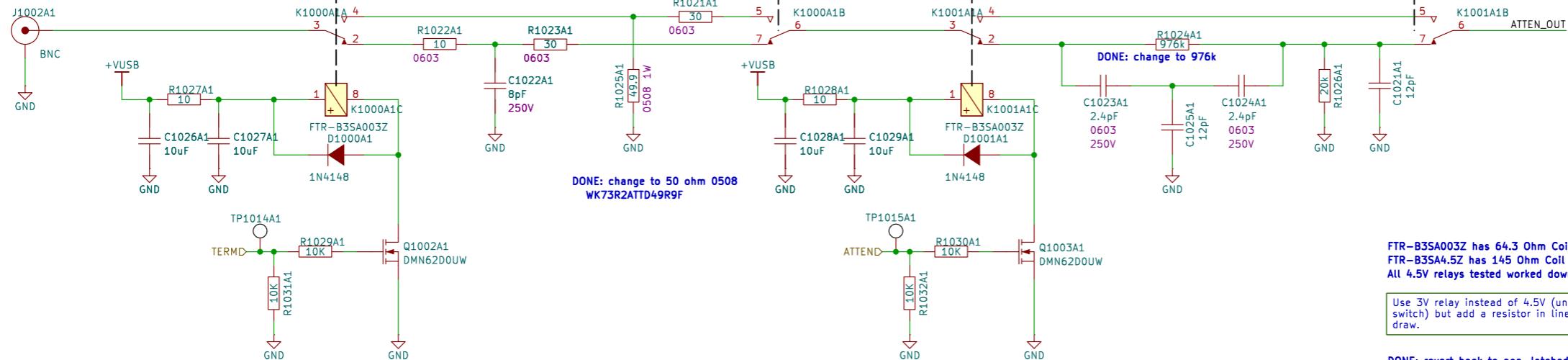


## Termination and Attenuation

**TODO:** Change Relays to 4.5V Parts as we are now powering them w/ +VUS



FTR-B35A003Z has 64.3 Ohm Coil Resistance, 2.25V Must Operate Voltage, 0.051A @ 3.3V  
FTR-B35A4.5Z has 145 Ohm Coil Resistance, 3.38V Must Operate Voltage, 0.023A @ 3.3V  
All 4.5V relays tested worked down to 3V

Use 3V relay instead of 4.5V (unit 9 ch3 atten relay could not switch) but add a resistor in line with the coil to reduce current draw.

DONE: revert back to non-latched relays to avoid indeterminate state when powered off

## Input Buffer and AC/DC Coupling

Max current for 35.7kOhm R\_Bias: 24mA @ V+ and 24mA @ V-  
100k R\_Bias will be lower: 17mA per rail was measured on the EV

DONE: change to 500hm

~~5.7k~~ → ~~range to 35.7k~~ -5V A1

R1042A1

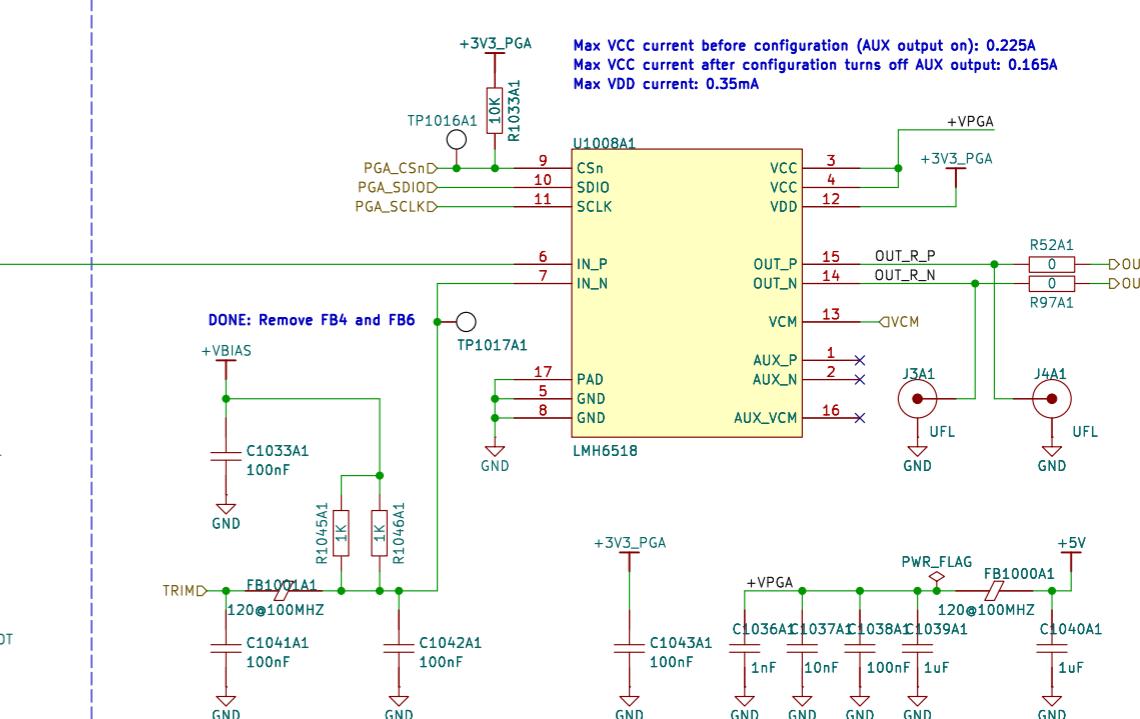
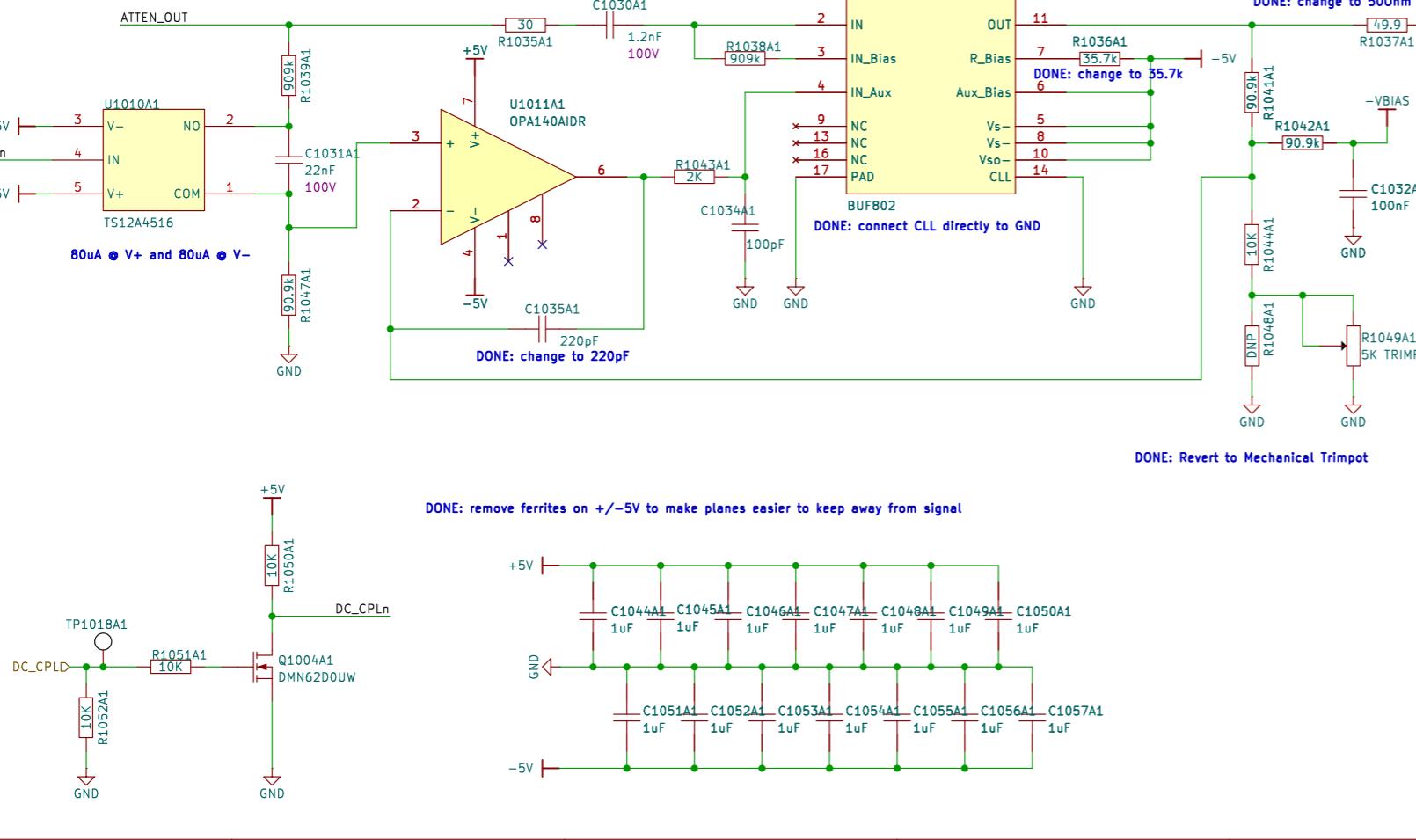
C1032A  
100nF

G2D

R1049A1

## Programmable Gain Amplifier

+3V3_PGA	Max VCC current before configuration (AUX output on): 0.225A Max VCC current after configuration turns off AUX output: 0.165A Max VDD current: 0.35mA
----------	---



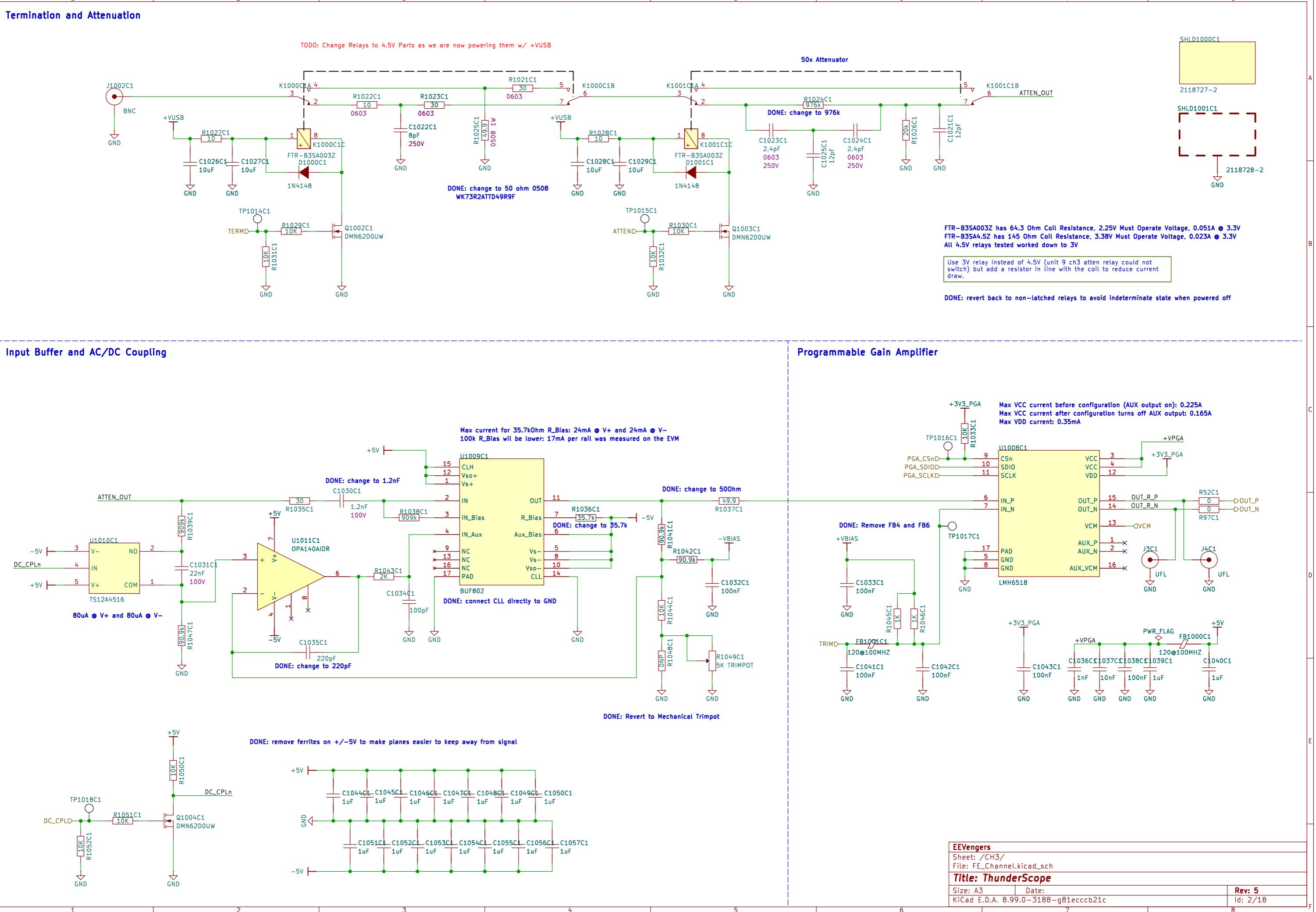
EEVengers  
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File: EE\_Channel\_Kiosk.sch

**Title:** ThunderScope

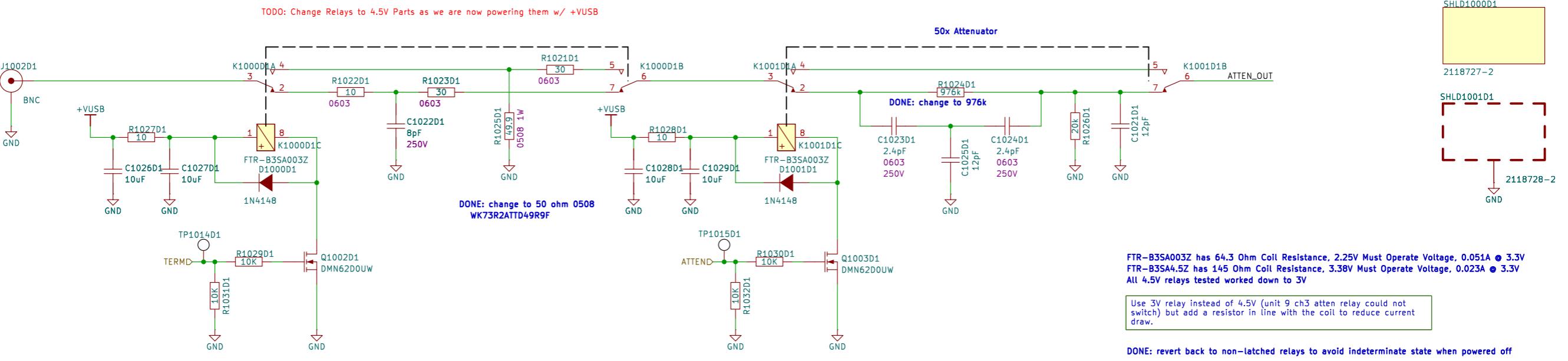
KiCad E.D.A. 8.99.0-3188-g81ecccb21c 7

Id: 2/18

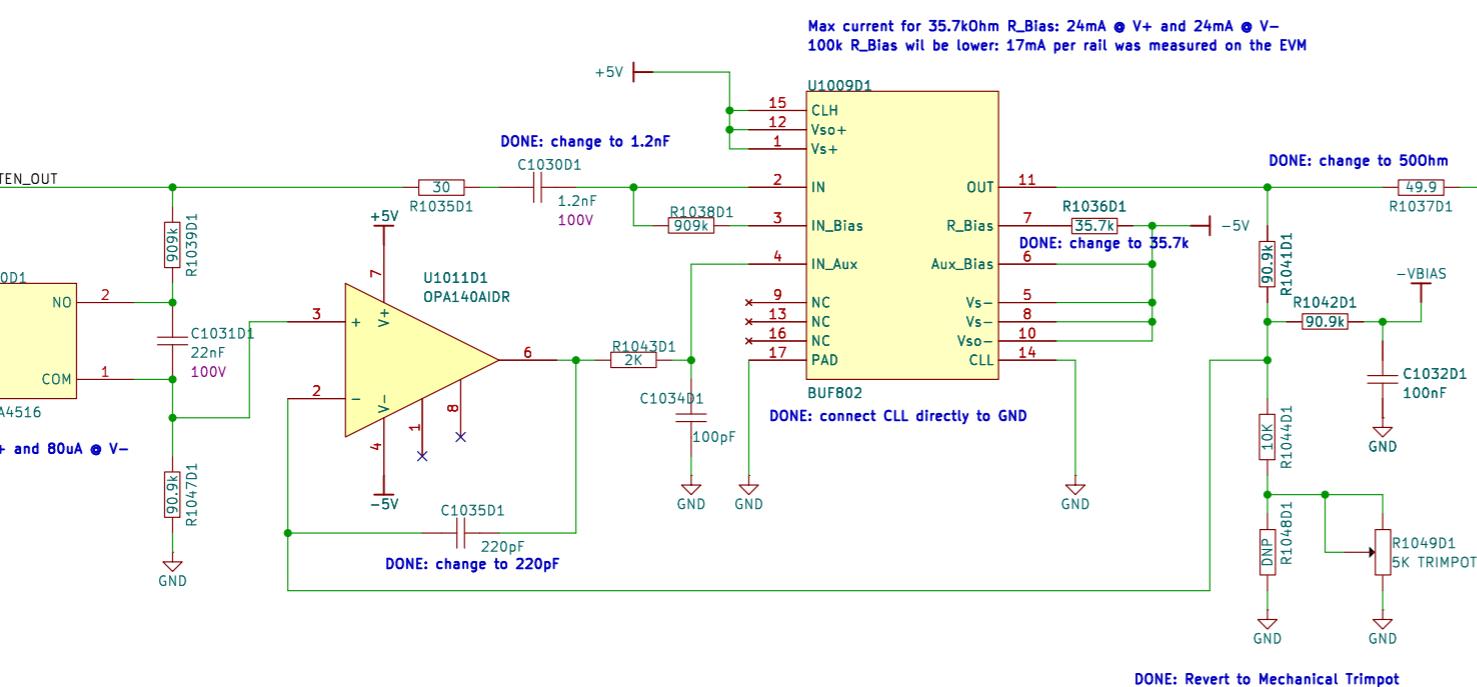




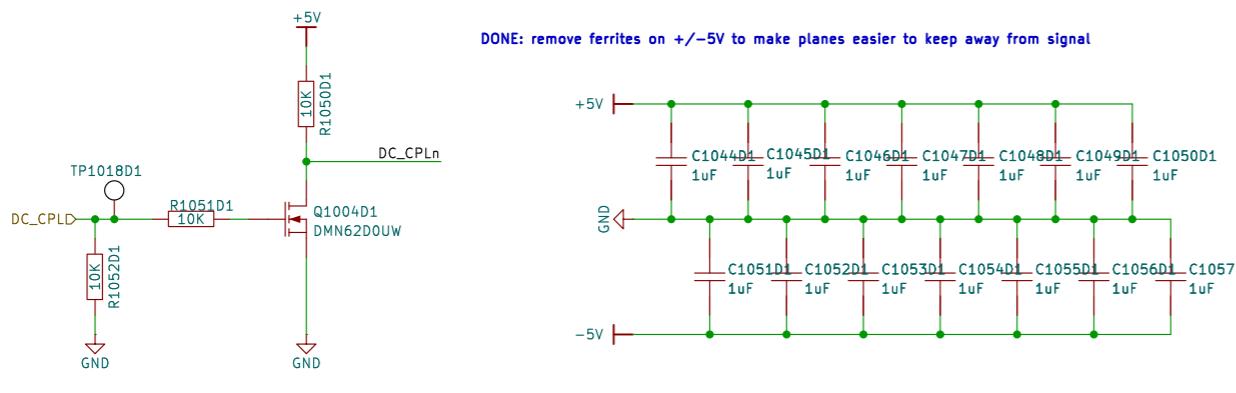
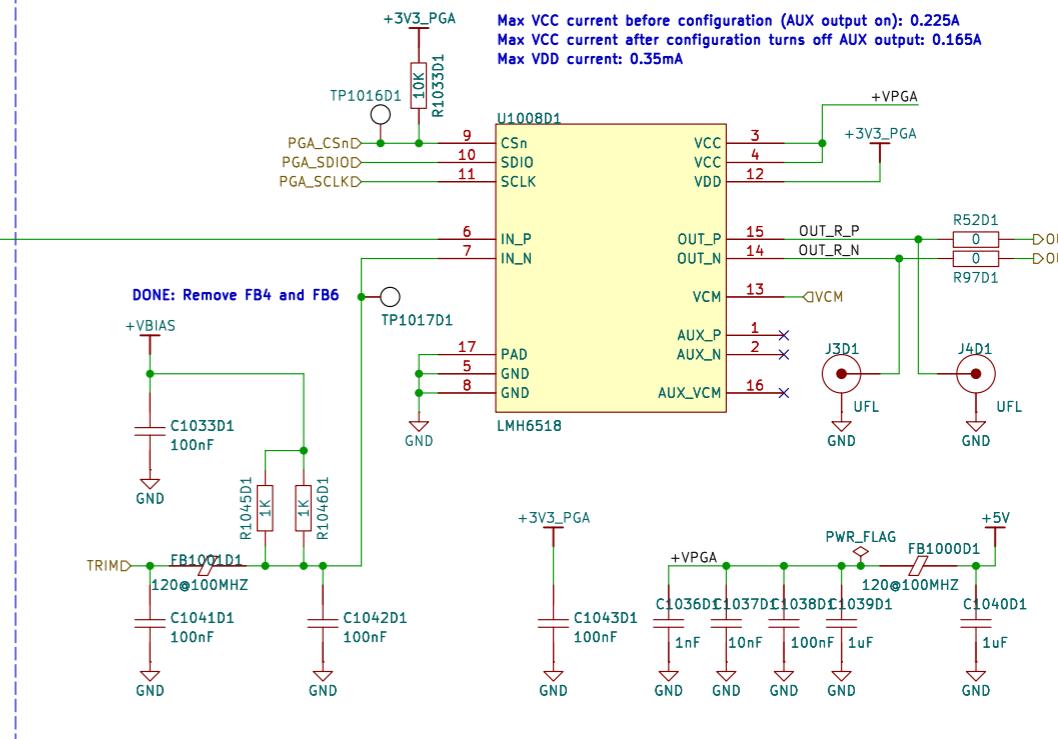
## Termination and Attenuation



## Input Buffer and AC/DC Coupling



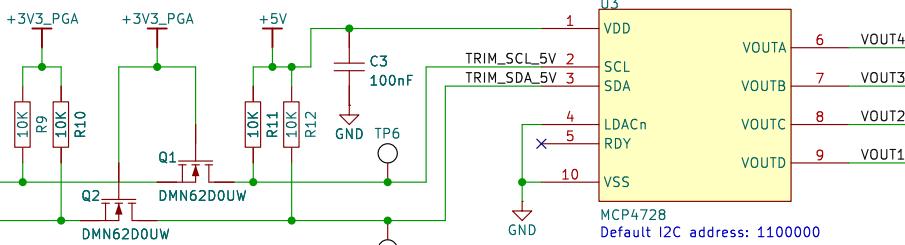
## Programmable Gain Amplifier



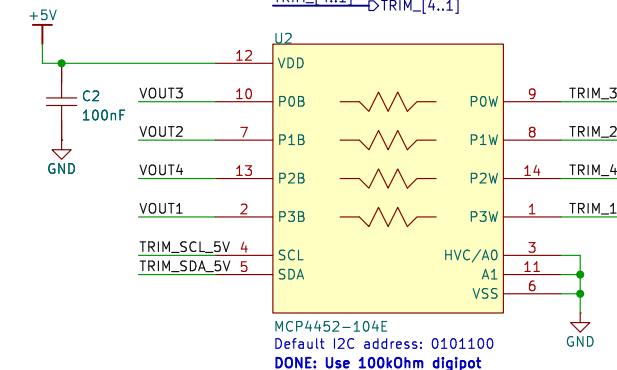
1 2 3 4 5 6

## Offset Voltage Trim and User Offset Control

A



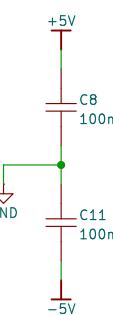
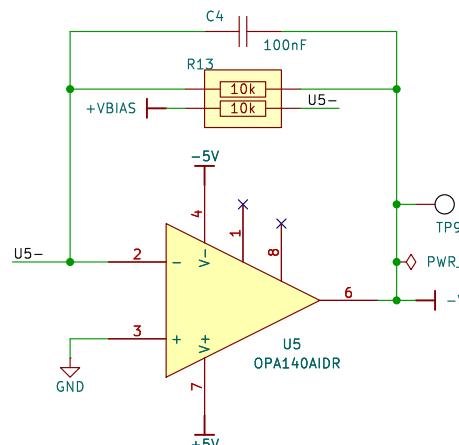
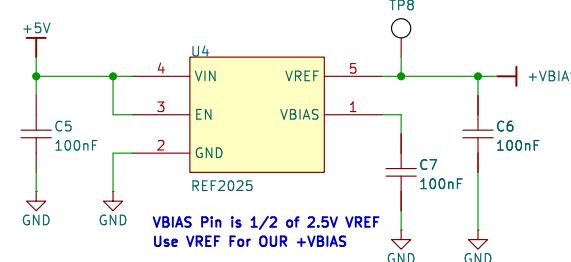
TRIM\_[4..1] → DTRIM\_[4..1]



B

## Bias Voltage Generation

C



Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140  
 -Max resistance is  $(575/4 // 10k) = 141.7 \text{ Ohm}$   
 -Worst case current is 17.64mA  
 -Use REF2025, has max current of 20mA  
 -Change U5 divider to matched resistor network  
 -ACASN1002S1002P1AT

## EEVengers

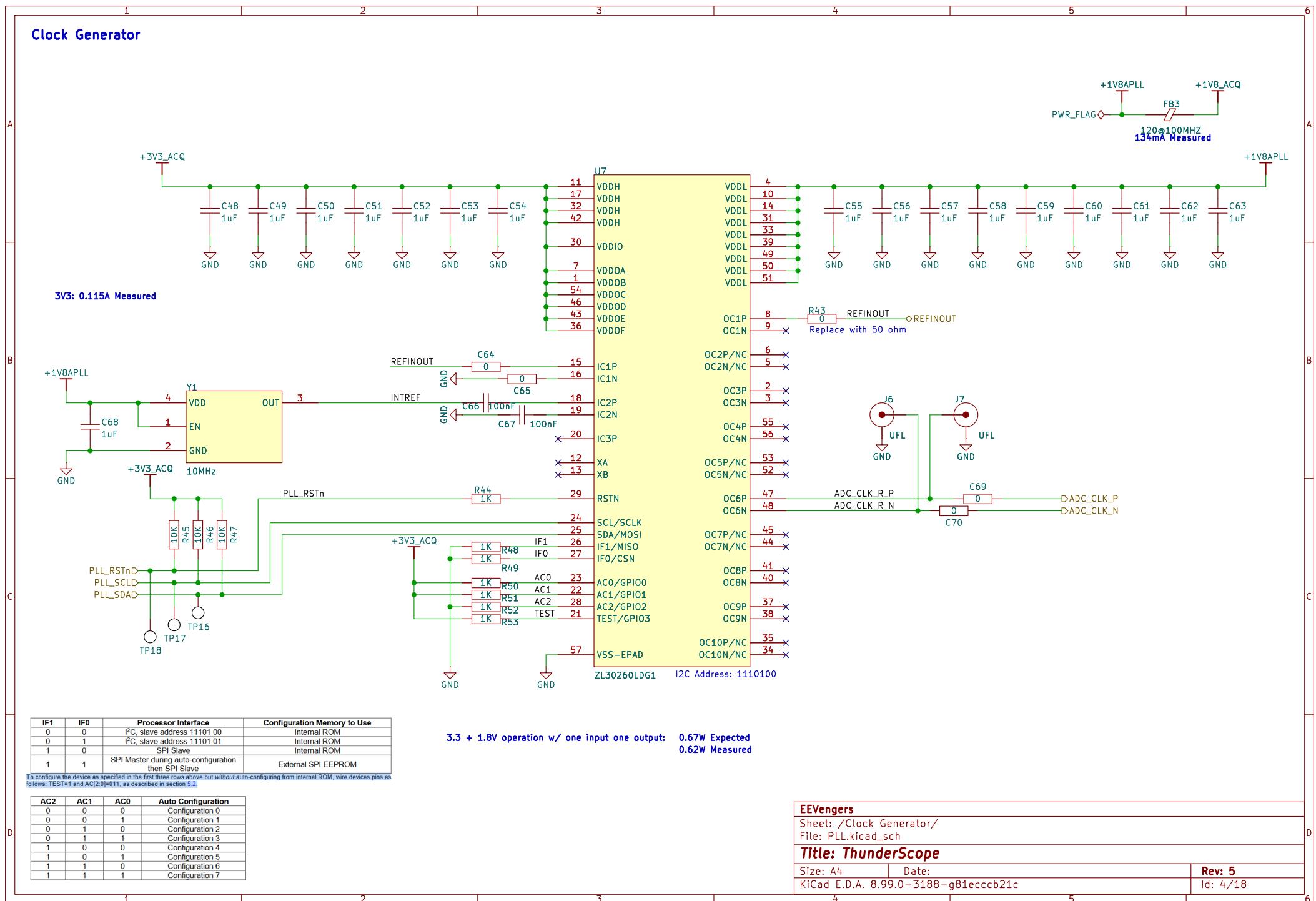
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Title: ThunderScope

Size: A4 Date:  
 KiCad E.D.A. 8.99.0-3188-g81ecccb21c

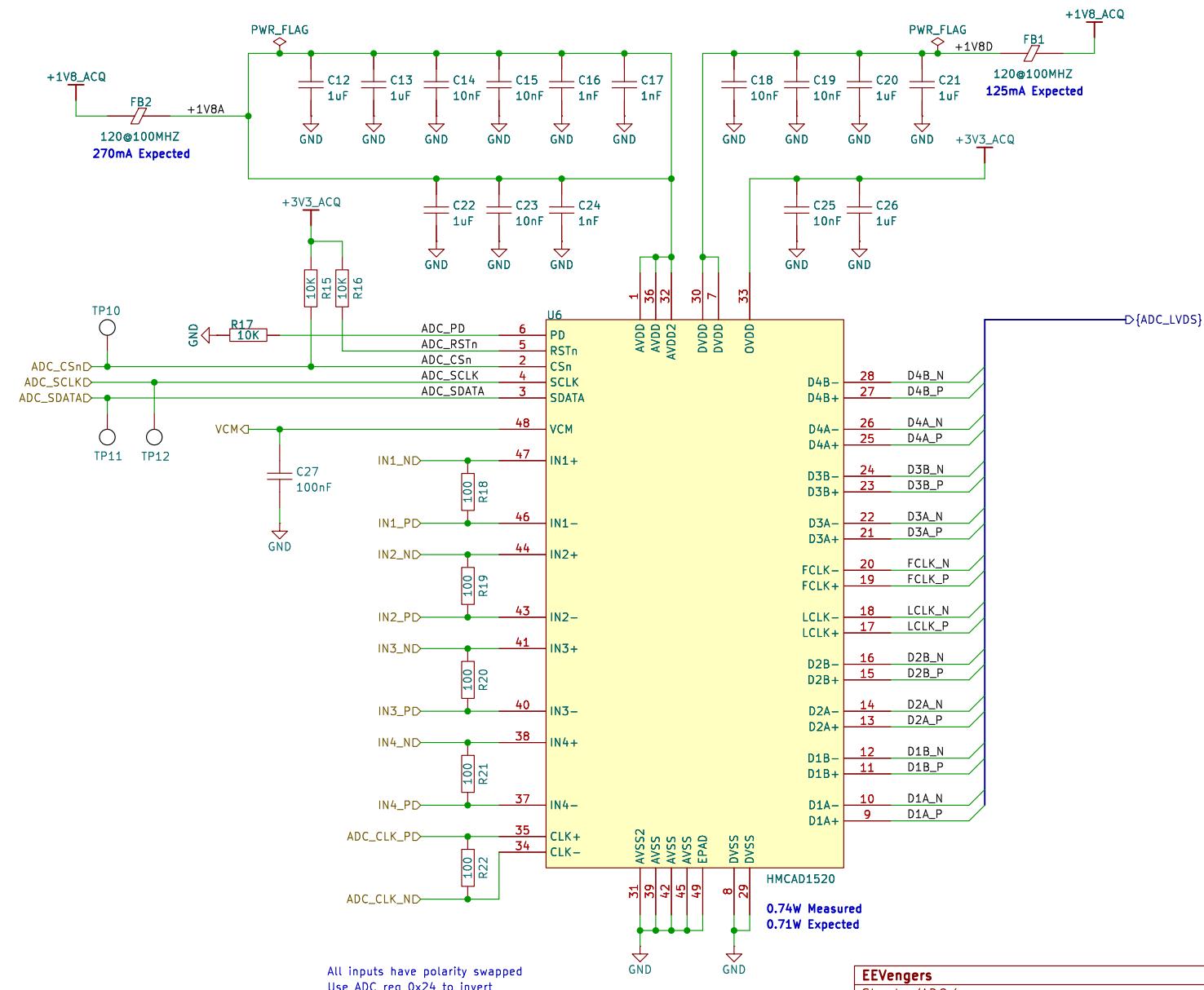
Rev: 5 Id: 3/18

1 2 3 4 5 6



1 2 3 4 5 6

## ADC



EEVengers

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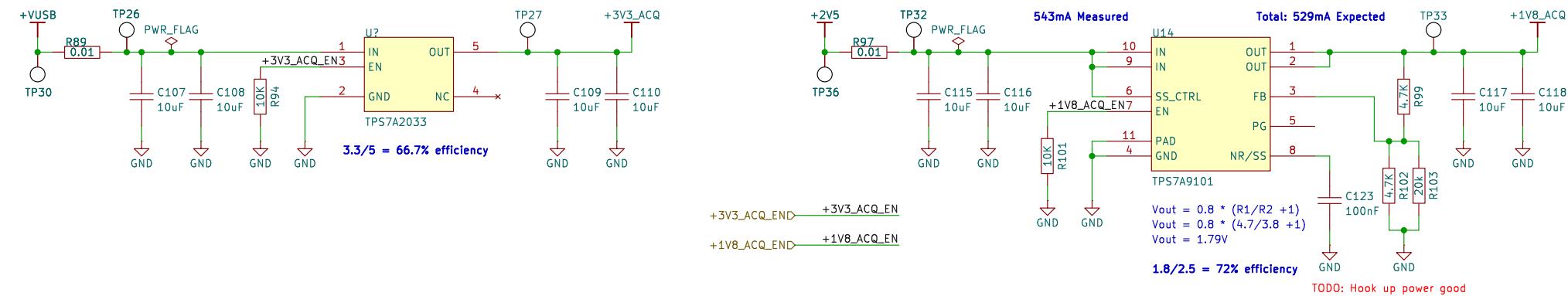
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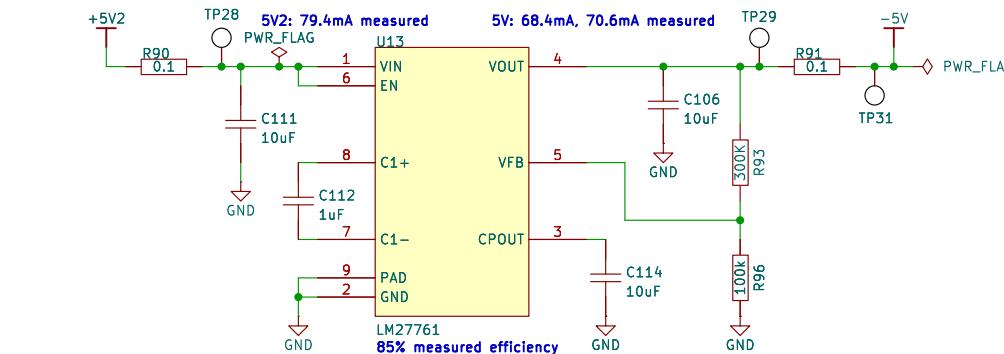
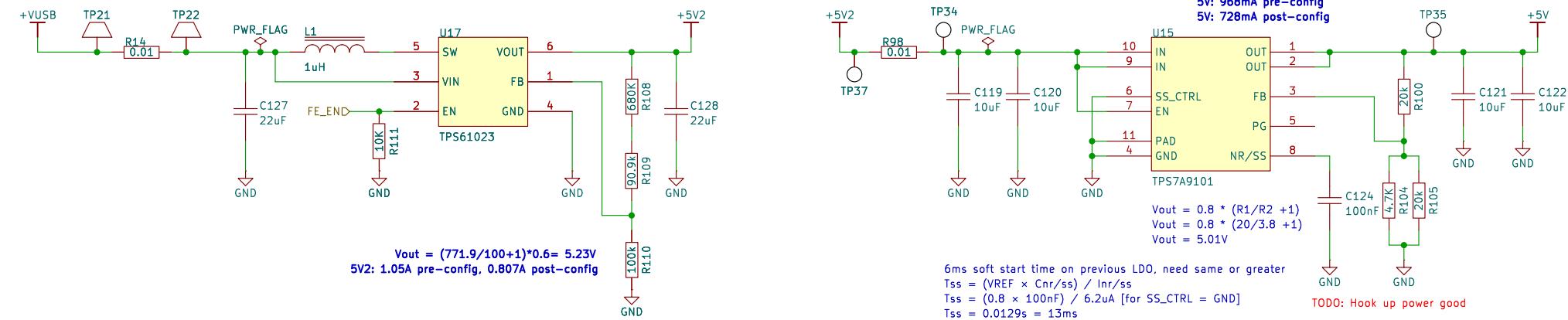
Rev: 5  
Id: 5/18

1 2 3 4 5 6

## Acquisition Voltage Rails



## Front End Voltage Rails



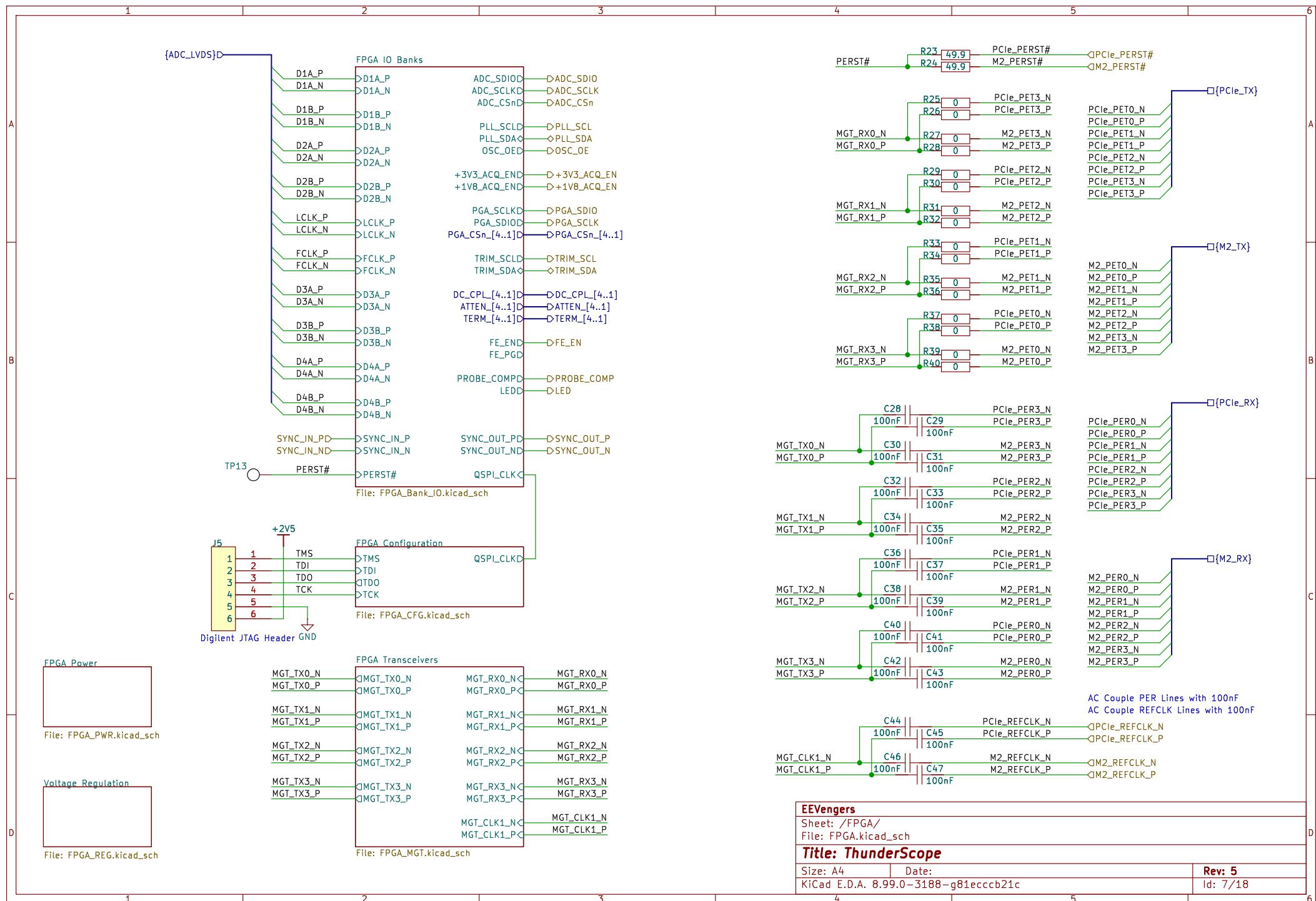
## EEVengers

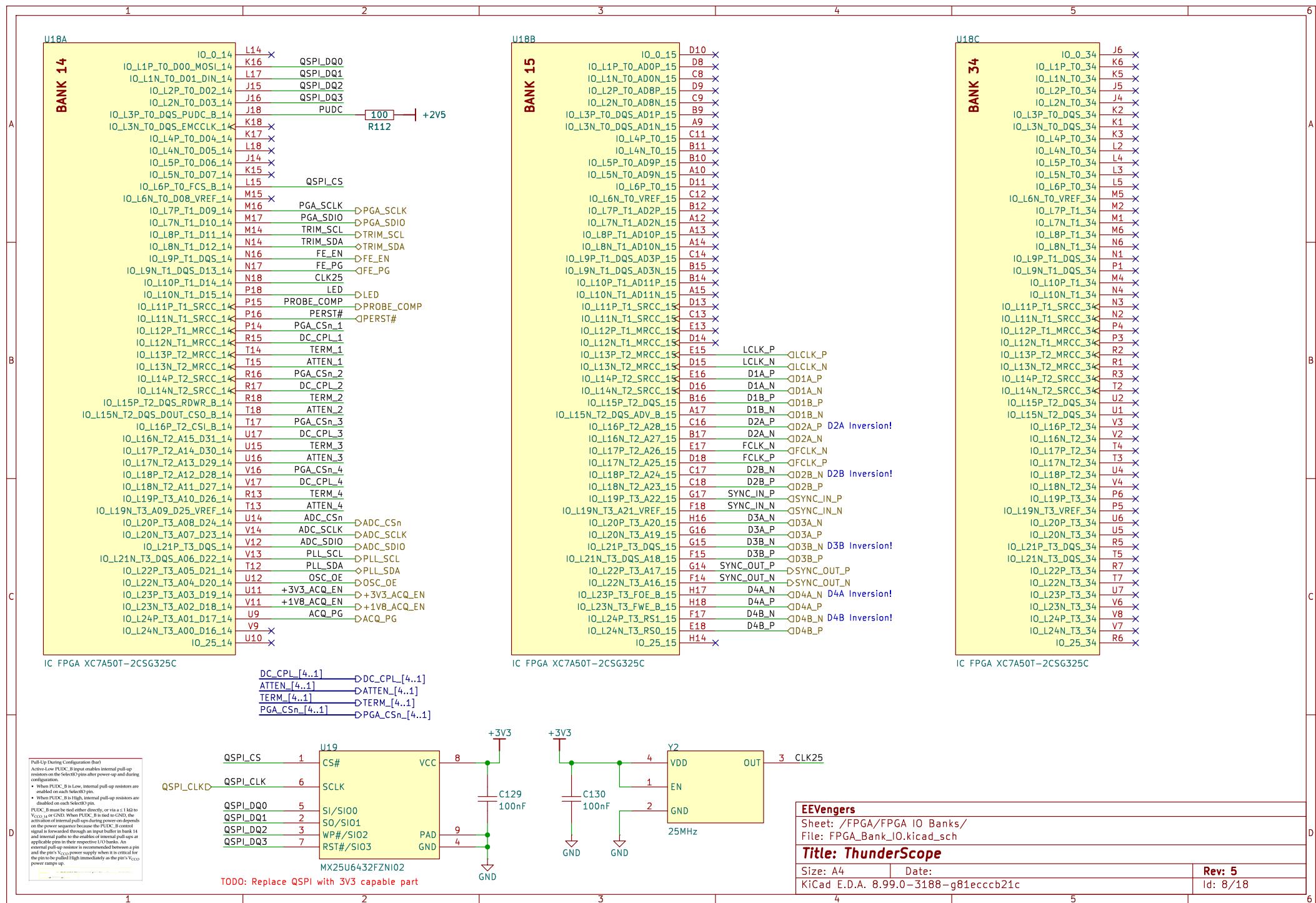
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File: PWR.kicad\_sch

**Title: ThunderScope**

Size: A4 Date:  
KiCad E.D.A. 8.99.0-3188-g81ecccb21c

Rev: 5  
Id: 6/18





A

A

B

B

C

C

D

D

Table 2-1: 7 Series FPGA Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

M[2:0] = 001

A high signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.  
After DONE goes high, there is a setup/hold requirement of approximately 10 kΩ. There is no setup/hold requirement for the TDI, TDO, TCK, and TMS pins. After the Done[6:0] register software default, eliminate the need for the TDI, TDO, TCK, and TMS pull-up resistors. These circuits are not required but can be used as they have been previously shown.

Connect INIT\_B to a 47 kΩ pull-up resistor to VCCO\_0 to ensure clean Low-to-High transitions.

Connect PROGRAM\_B to an external < 47 kΩ pull-up resistor to VCCO\_0 to generate a stable High input, and

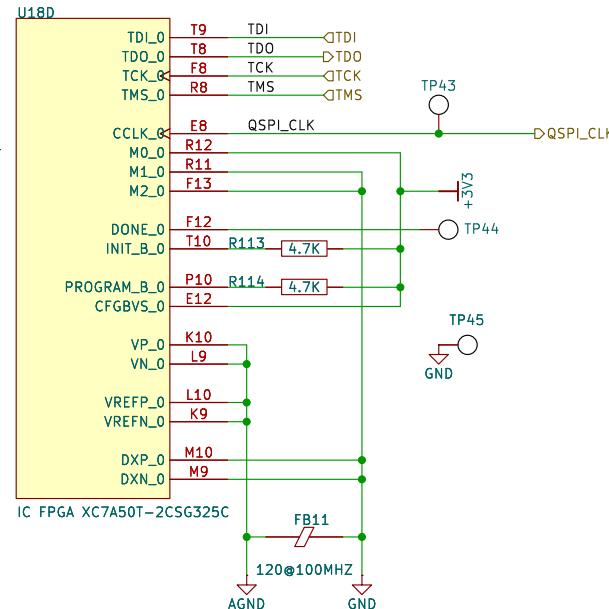


Table 2-6: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Banks Used	Configuration Interface I/O Voltage	HR Bank 0 V <sub>CCO_0</sub>	HR Bank 14 V <sub>CCO_14</sub>	HR Bank 15 V <sub>CCO_15</sub>	CFGBVS
JTAG (only)	0	3.3V	3.3V	Any	Any	VCCO_0
		2.5V	2.5V	Any	Any	VCCO_0
		1.8V	1.8V	Any	Any	GND
		1.5V	1.5V	Any	Any	GND
		3.3V	3.3V	3.3V	Any	VCCO_0
Serial SPI or SelectMAP	0, 14 <sup>(1)</sup>	2.5V	2.5V	2.5V	Any	VCCO_0
		1.8V	1.8V	1.8V	Any	GND
		1.5V	1.5V	1.5V	Any	GND
		3.3V	3.3V	3.3V	3.3V	VCCO_0
		2.5V	2.5V	2.5V	2.5V	VCCO_0
BPI <sup>(2)</sup>	0, 14, 15	1.8V	1.8V	1.8V	1.8V	GND
		1.5V	1.5V	1.5V	1.5V	GND
		3.3V	3.3V	3.3V	3.3V	VCCO_0
		2.5V	2.5V	2.5V	2.5V	VCCO_0
		1.8V	1.8V	1.8V	1.8V	GND

## Notes:

- RS[1:0] for MultiBoot or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.
- BPI mode is not available in the Spartan-7 family.

## EEVengers

Sheet: /FPGA/FPGA Configuration/  
File: FPGA\_CFG.kicad\_sch

## Title: ThunderScope

Size: A4 Date:  
KiCad E.D.A. 8.99.0-3188-g81ecccb21c

Rev: 5  
Id: 9/18

A

A

B

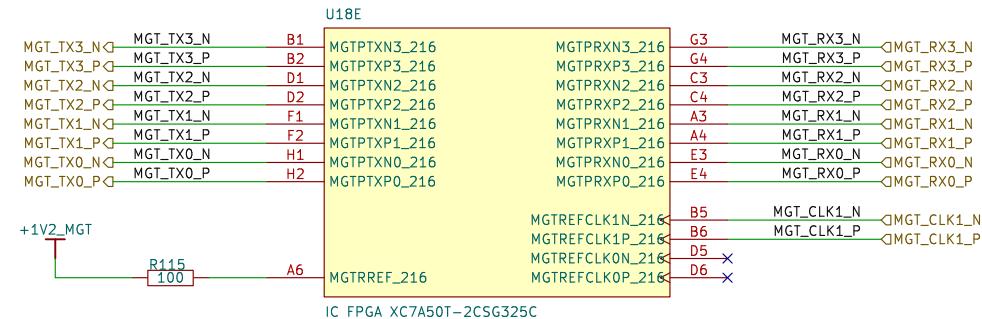
B

C

C

D

D

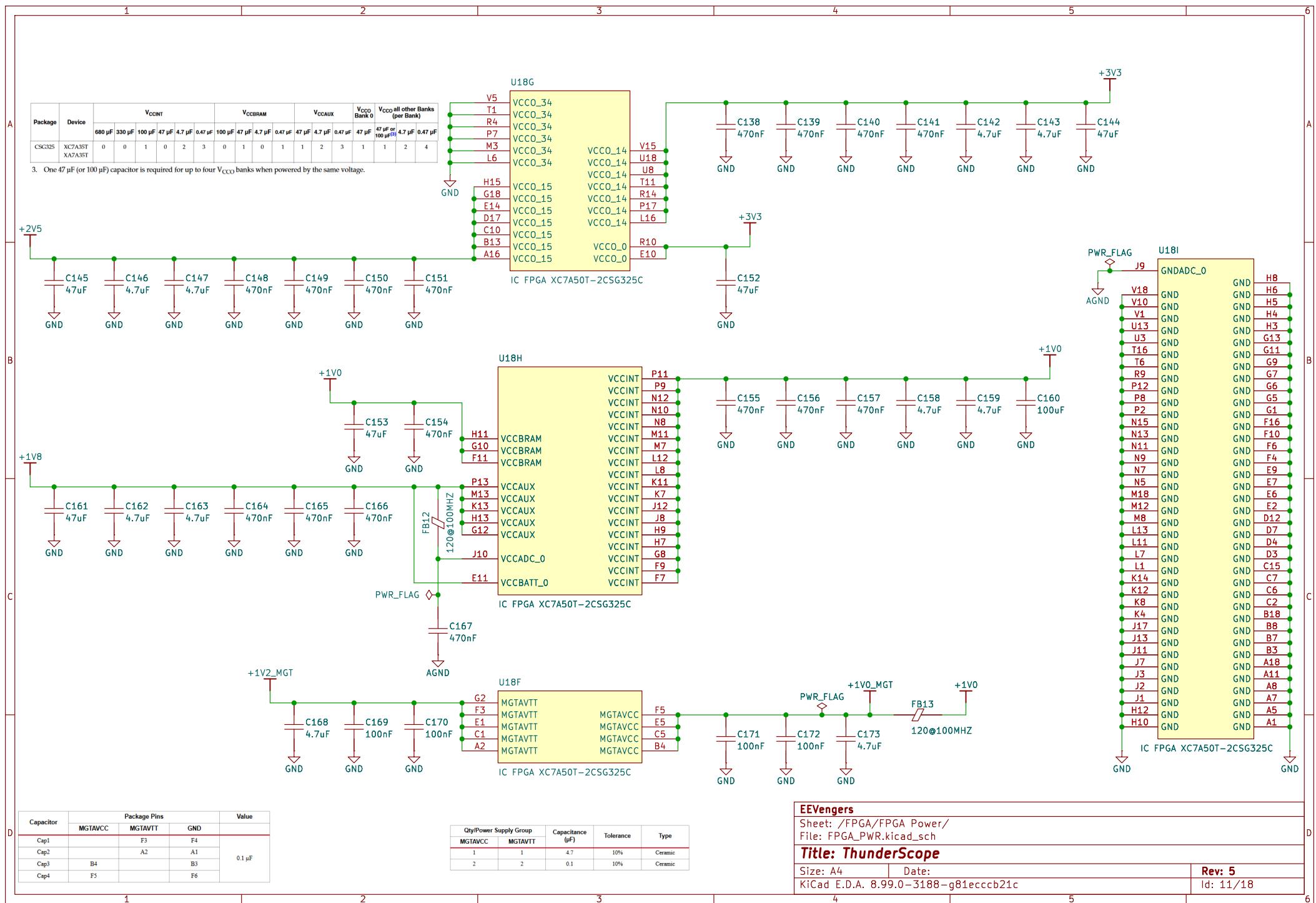
**EEVengers**

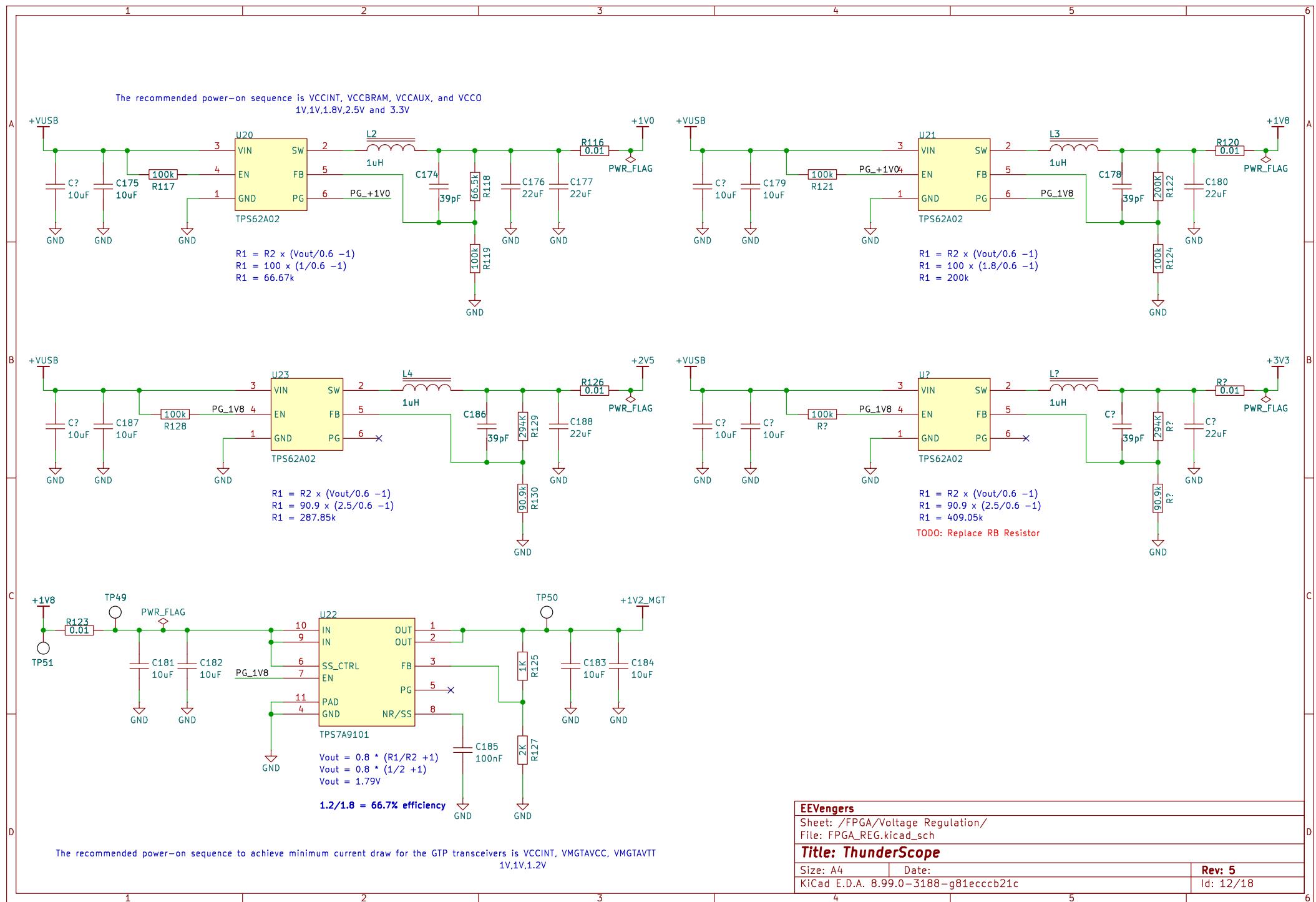
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**Title: ThunderScope**

Size: A4 Date:  
KiCad E.D.A. 8.99.0-3188-g81ecccb21c

Rev: 5  
Id: 10/18

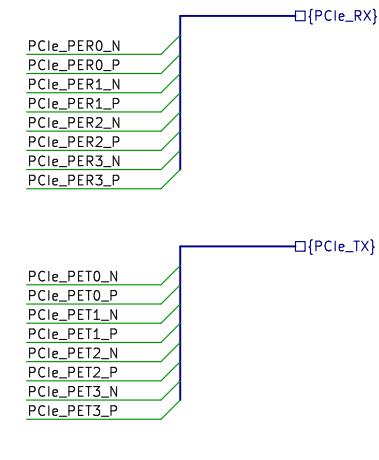
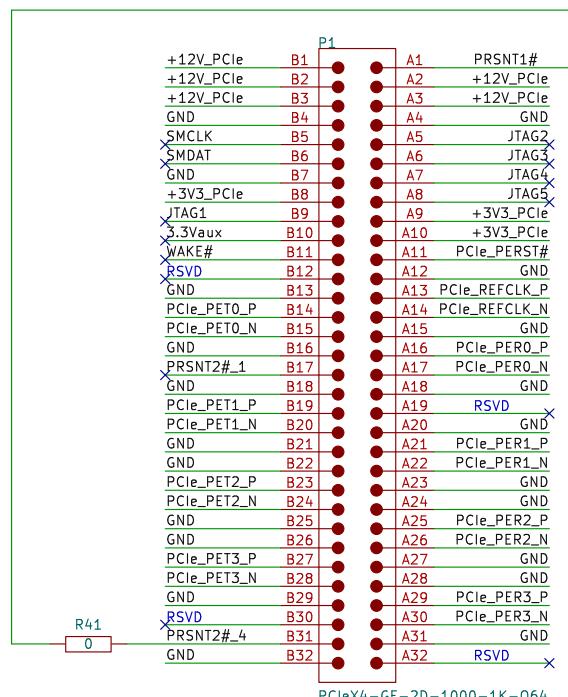




1 2 3 4 5 6

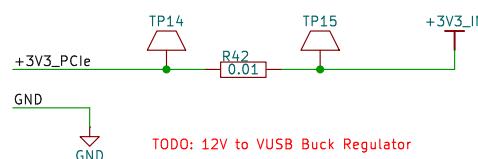
## PCIe x4 Edge Connector

A



PCIe\_REFCLK\_P → PCIe\_REFCLK\_P  
PCIe\_REFCLK\_N → PCIe\_REFCLK\_N

PCIe\_PERST# → PCIe\_PERST#



EEVengers

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File: CON\_PClie\_X4.kicad\_sch

Title: ThunderScope

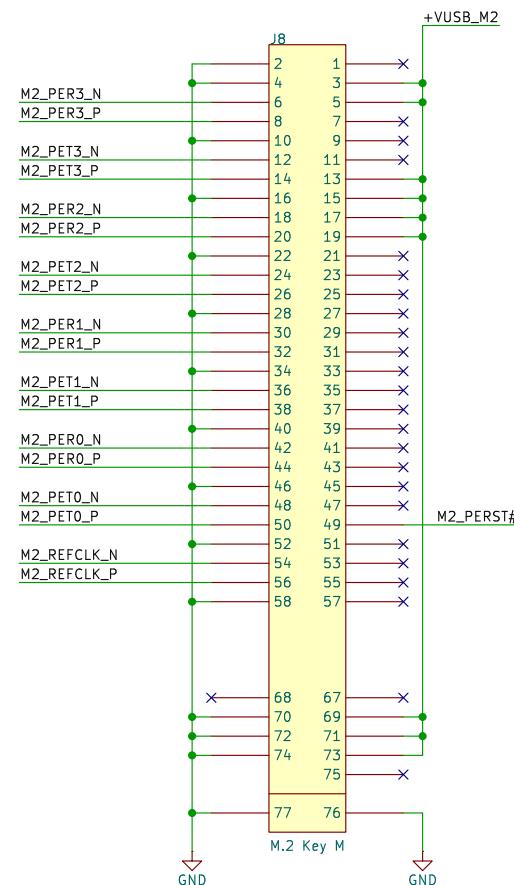
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Rev: 5  
Id: 13/18

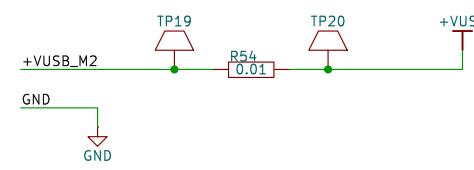
1 2 3 4 5 6

**M.2 Key M Connector**

A

**Main Board  
Custom Pinout**

Note that the TB/USB4 adaptor must be modified to give us VUSB instead of 3V3

**EEVengers**

Sheet: /M.2\_Key\_M/  
File: M2\_KEY\_M.kicad\_sch

**Title: ThunderScope**

Size: A4 Date:  
KiCad E.D.A. 8.99.0-3188-g81eccb21c

Rev: 5  
Id: 14/18

1 2 3 4 5 6

A

A

B

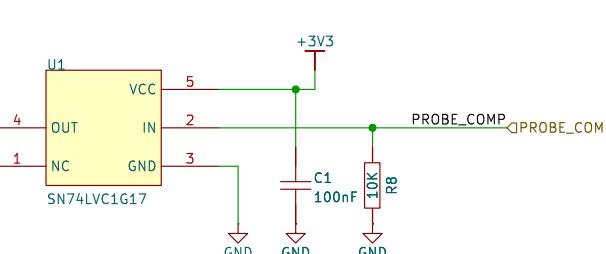
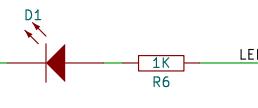
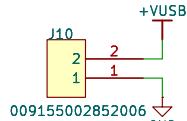
B

C

C

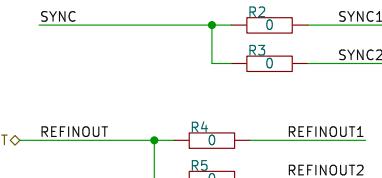
D

D

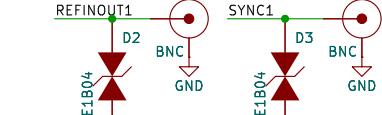
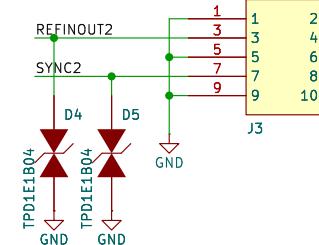


SYNC\_IN\_P  
SYNC\_IN\_N

SYNC\_OUT\_P  
SYNC\_OUT\_N



#### Connectors for multi-scope connection



EEVengers

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File: User\_I0.kicad\_sch

Title: ThunderScope

Size: A4 Date:  
KiCad E.D.A. 8.99.0-3188-g81ecccb21c

Rev: 5  
Id: 15/18

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