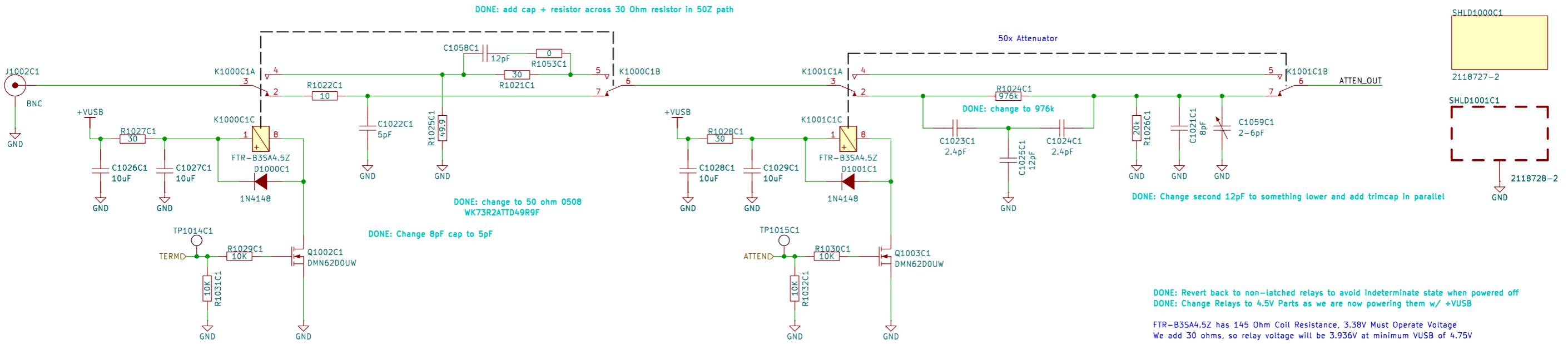
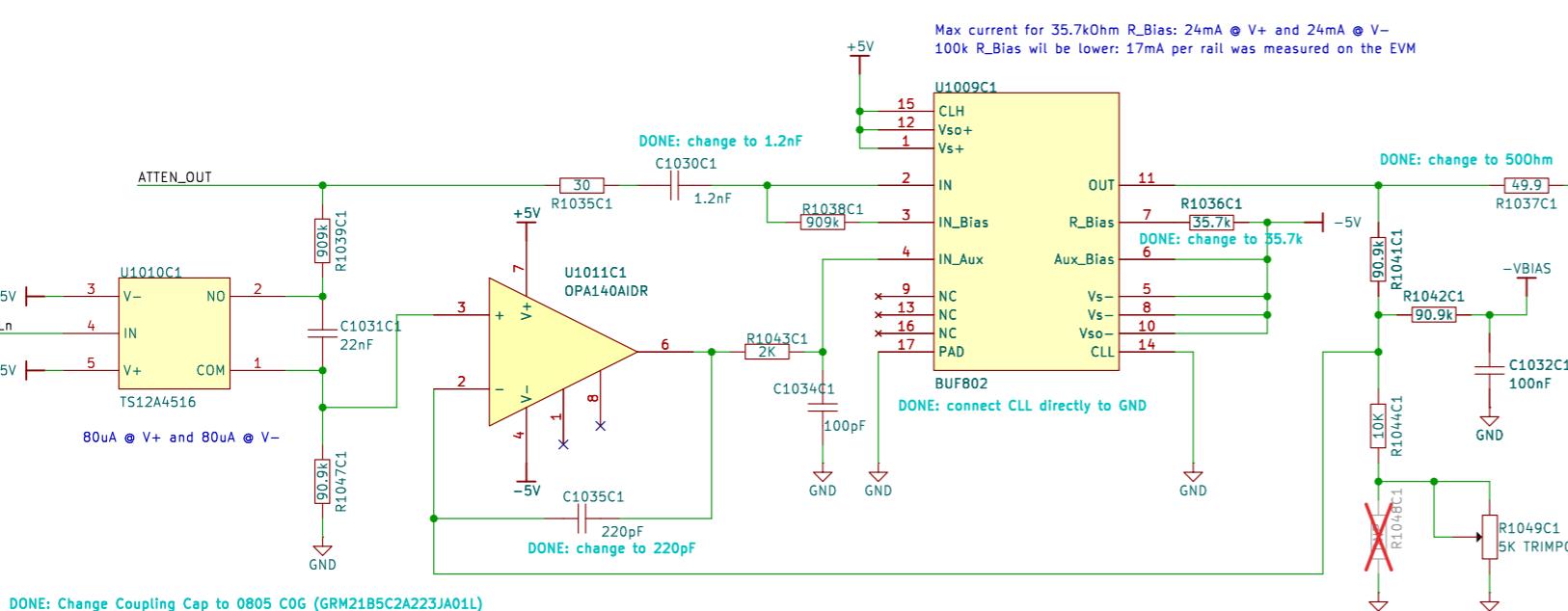


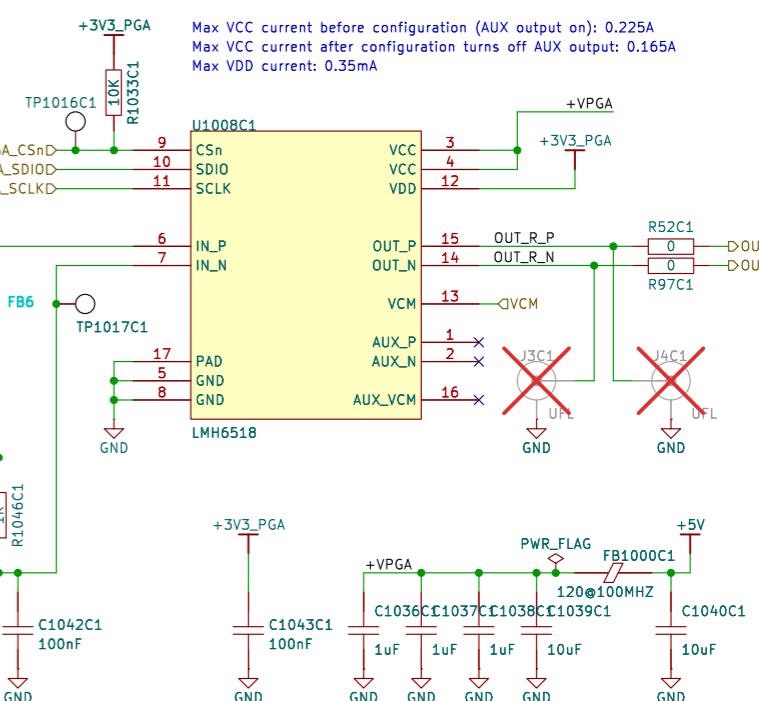
Termination and Attenuation



Input Buffer and AC/DC Coupling

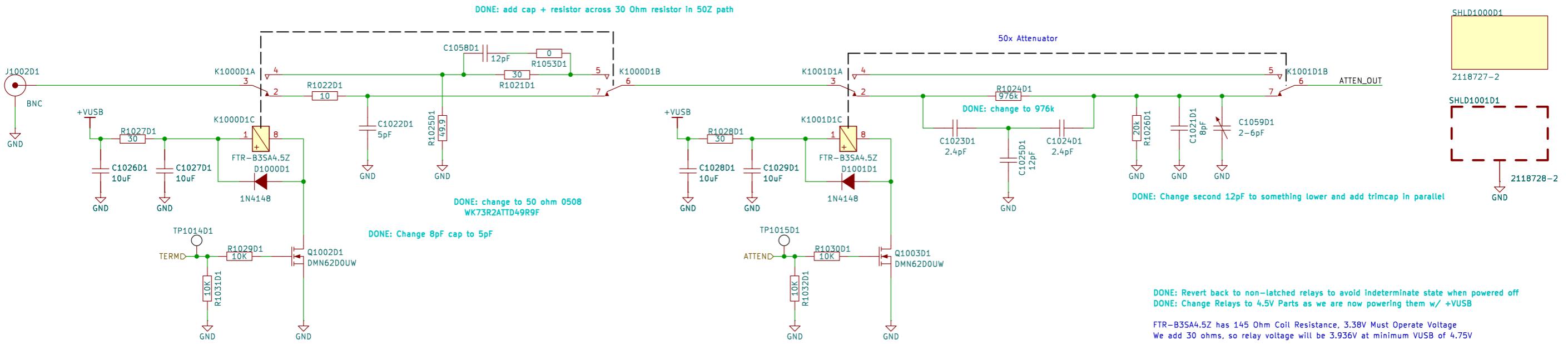


Programmable Gain Amplifier

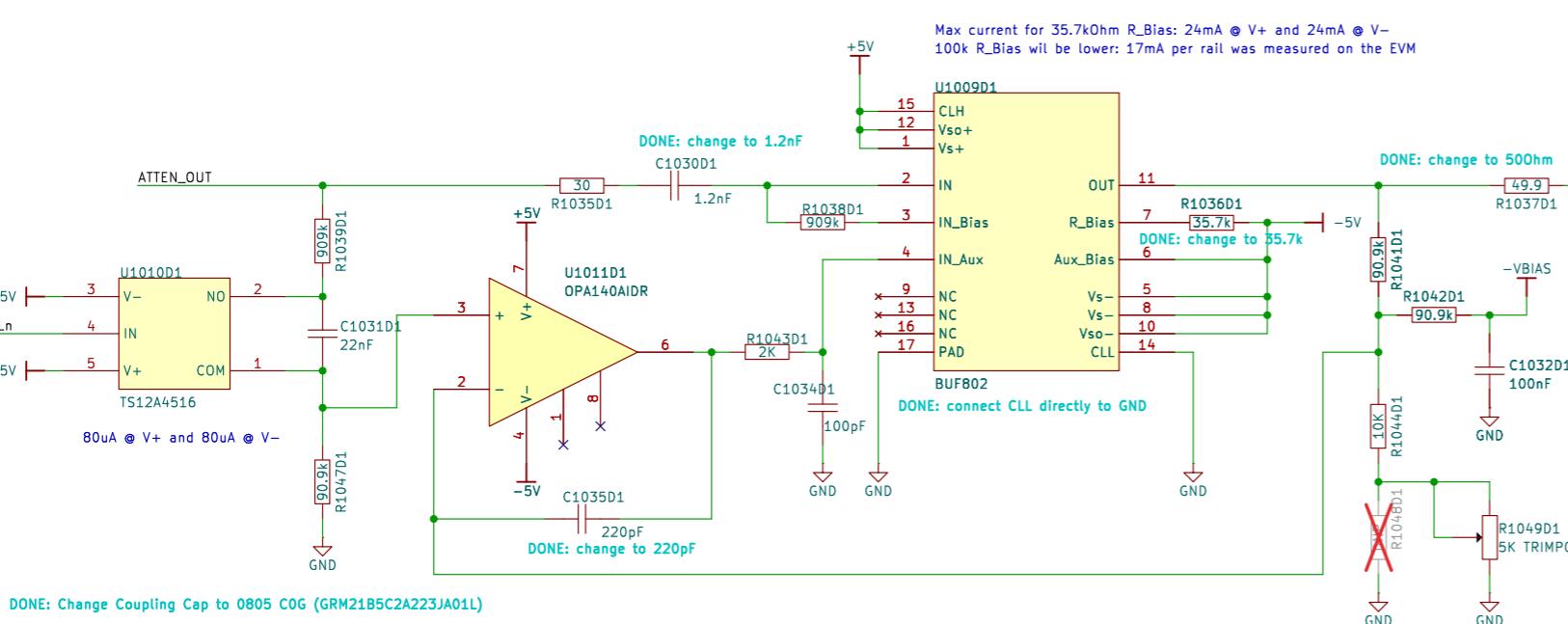


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Title: ThunderScope
Size: A3 Date:
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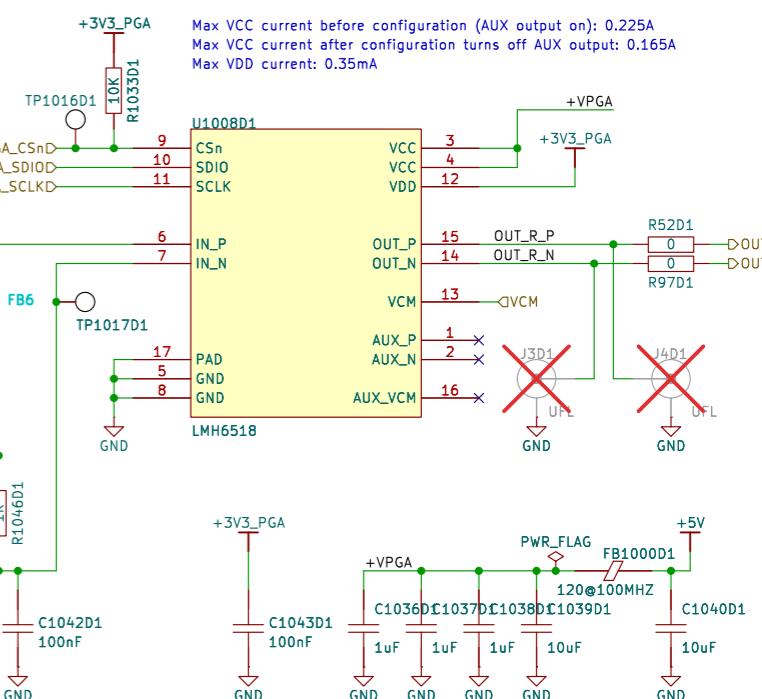
Termination and Attenuation



Input Buffer and AC/DC Coupling



Programmable Gain Amplifier



DONE: Change Coupling Cap to 0805 COG (GRM21B5C2A223JA0)

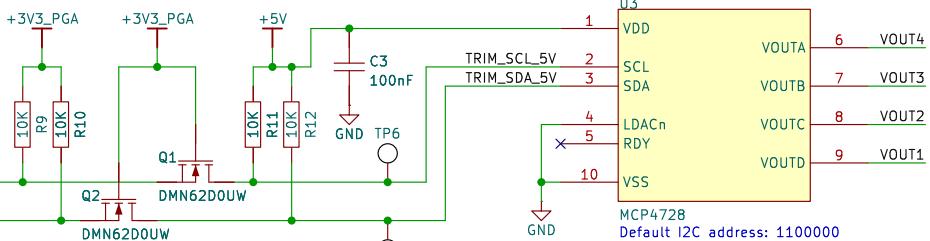
DONE: Revert to Mechanical Trimpo

DONE: remove ferrites on +/-5V to make planes easier to keep away from sig

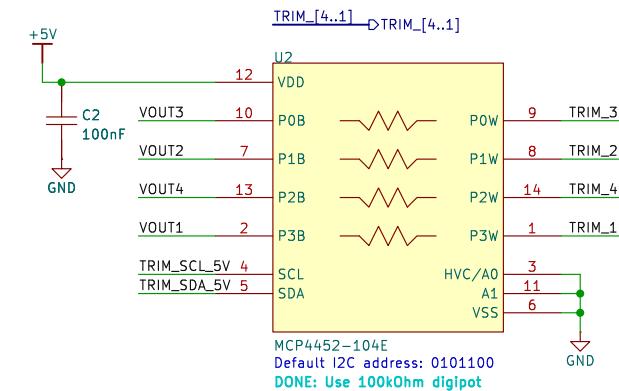
1 2 3 4 5 6

Offset Voltage Trim and User Offset Control

A

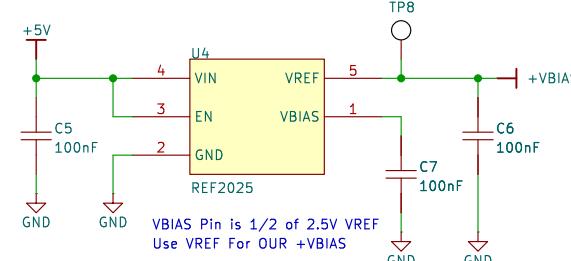


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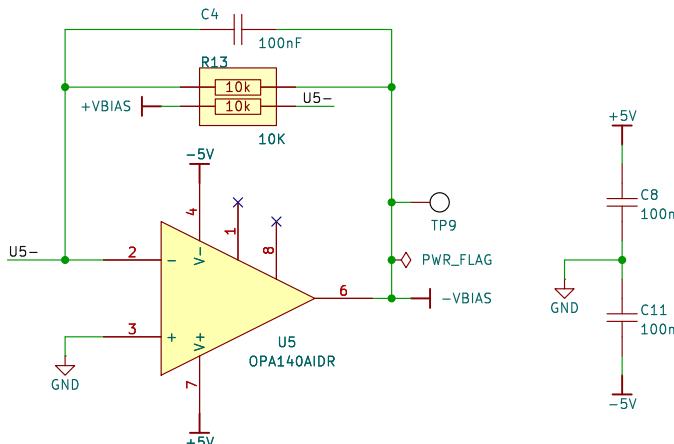
Bias Voltage Generation

C



D

Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140
-Max resistance is $(575/4 // 10k) = 141.7 \text{ Ohm}$
-Worst case current is 17.64mA
-Use REF2025, has max current of 20mA
-Change U5 divider to matched resistor network
-ACASN1002S1002P1AT



EEVengers

Sheet: /Front End Trim and Bias/
File: FE.kicad_sch

Title: ThunderScope

Size: A4 Date:

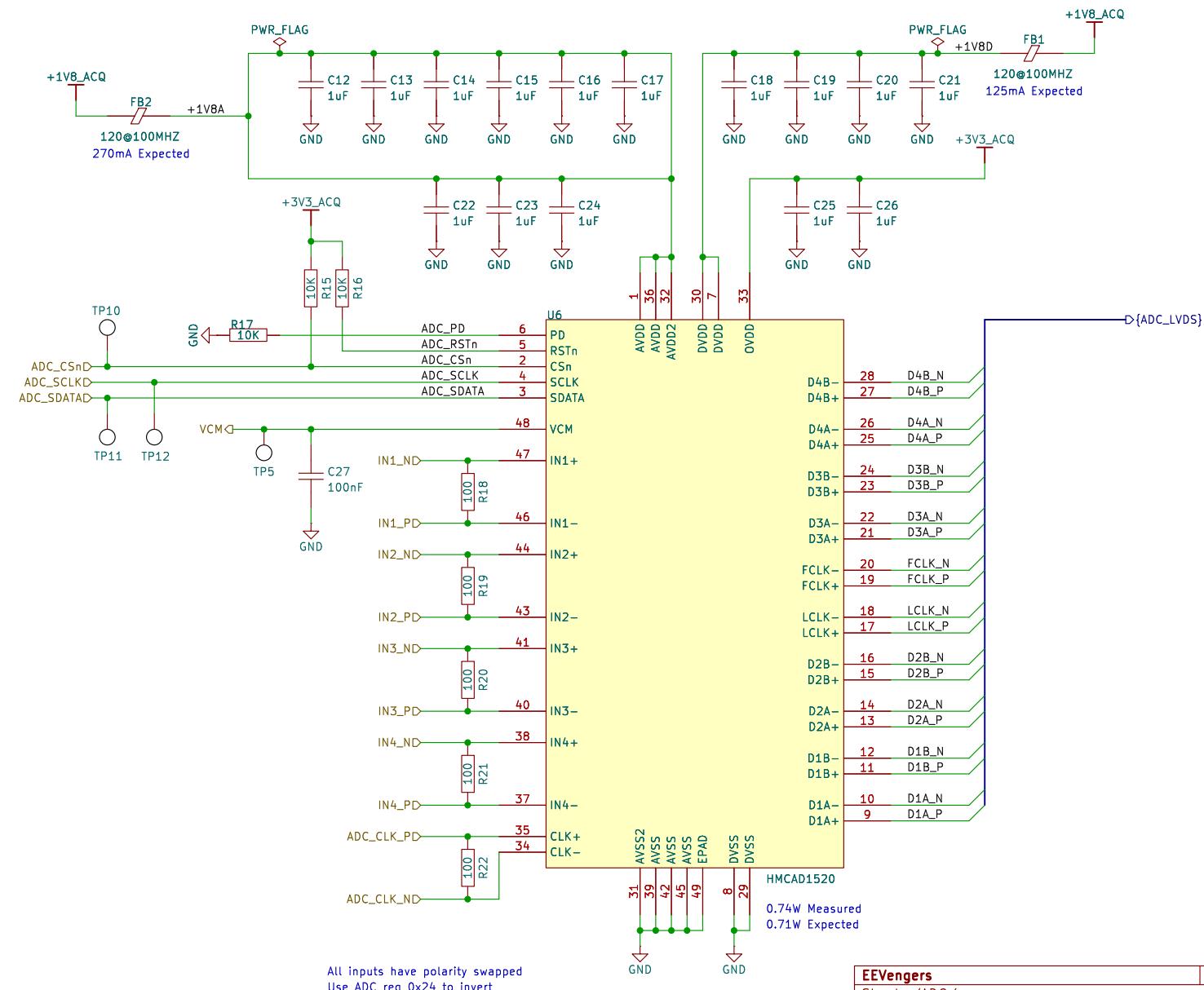
KiCad E.D.A. 9.0.0

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 3/16

1 2 3 4 5 6

1 2 3 4 5 6

ADC

EEVengers

Drawn by: Aleksa Bjelogrlic

Sheet: /ADC/

File: ADC.kicad_sch

Title: ThunderScope

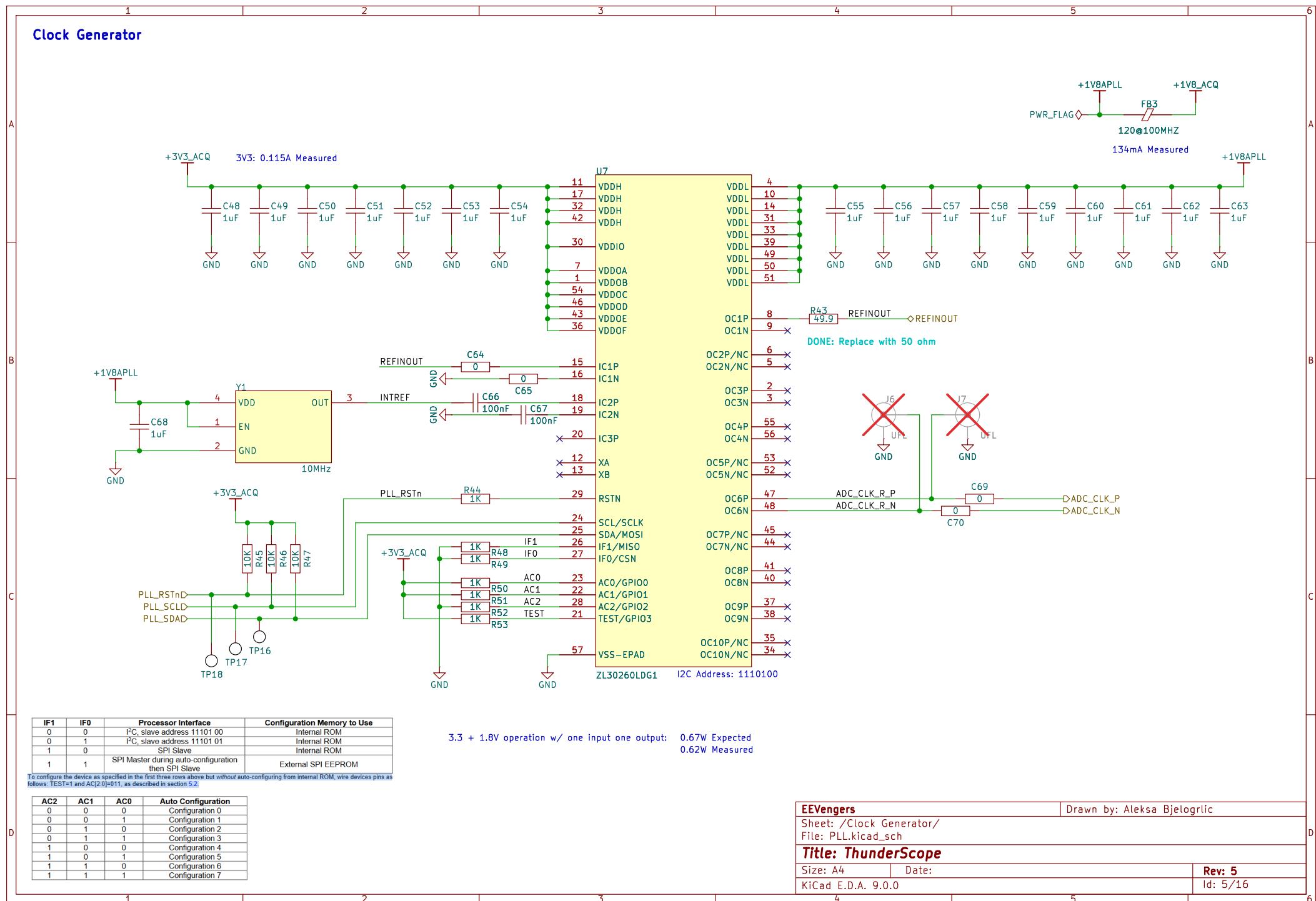
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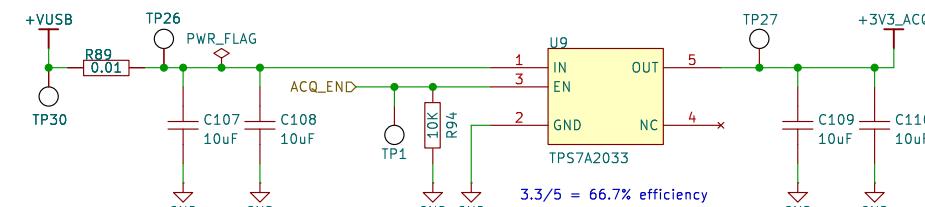
Rev: 5

Id: 4/16

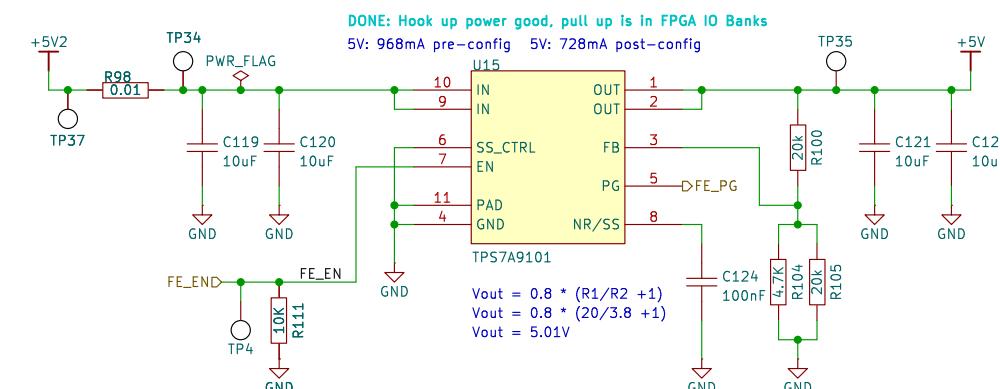
1 2 3 4 5 6



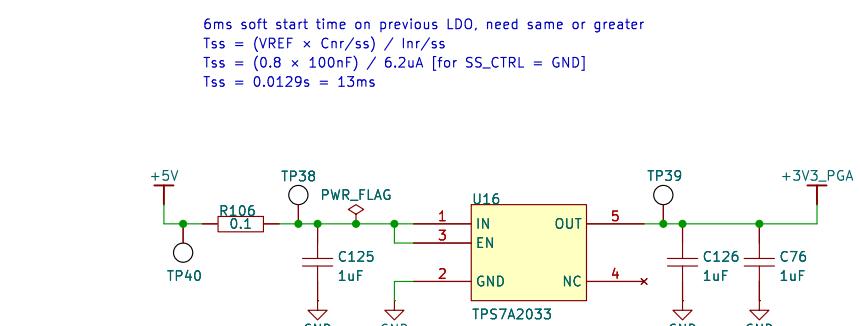
Acquisition Voltage Regulators



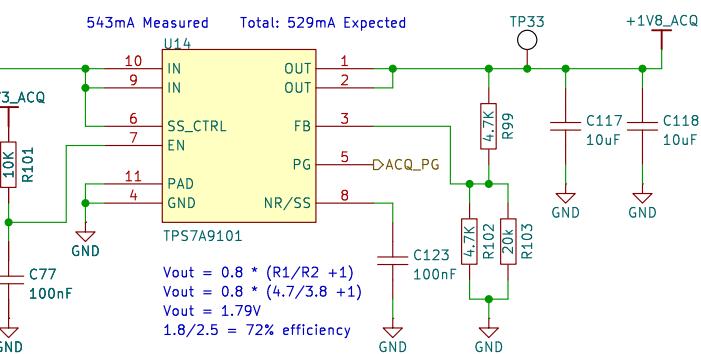
Front End Voltage Regulators



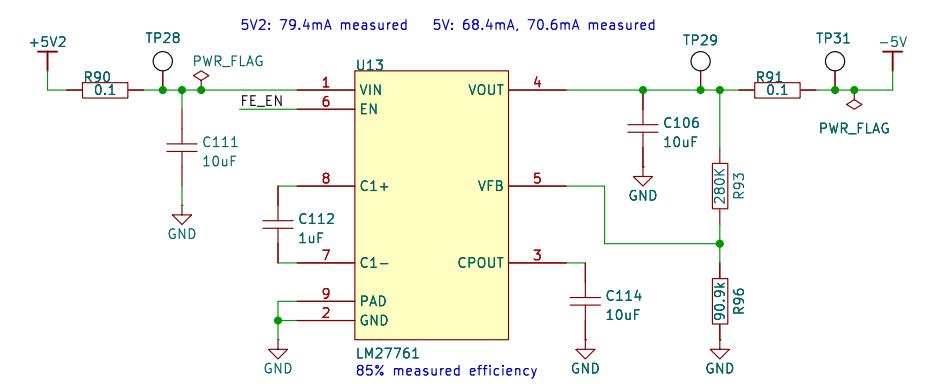
6ms soft start time on previous LDO, need same or greater
 $T_{ss} = (V_{REF} \times C_{nr/ss}) / I_{nr/ss}$
 $T_{ss} = (0.8 \times 100nF) / 6.2\mu A$ [for SS_CTRL = GND]
 $T_{ss} = 0.0129s = 13ms$



DONE: Hook up power good, pull up is in FPGA IO Banks



54.3mA Measured Total: 529mA Expected
 $V_{out} = 0.8 * (R1/R2 + 1)$
 $V_{out} = 0.8 * (4.7/3.8 + 1)$
 $V_{out} = 1.79V$
 $1.8/2.5 = 72\% \text{ efficiency}$



5V: 79.4mA measured 5V: 68.4mA, 70.6mA measured
 $V_{out} = -1.22V * (R1+R2)/R2$
 $V_{out} = -1.22 * (280/90.9+1) = -4.98V$
The value for R2 must be no less than 50 kΩ.

EEVengers

Sheet: /ACQ and FE Voltage Regs/
File: ACQ_FE_VREG.kicad_sch

Title: ThunderScope

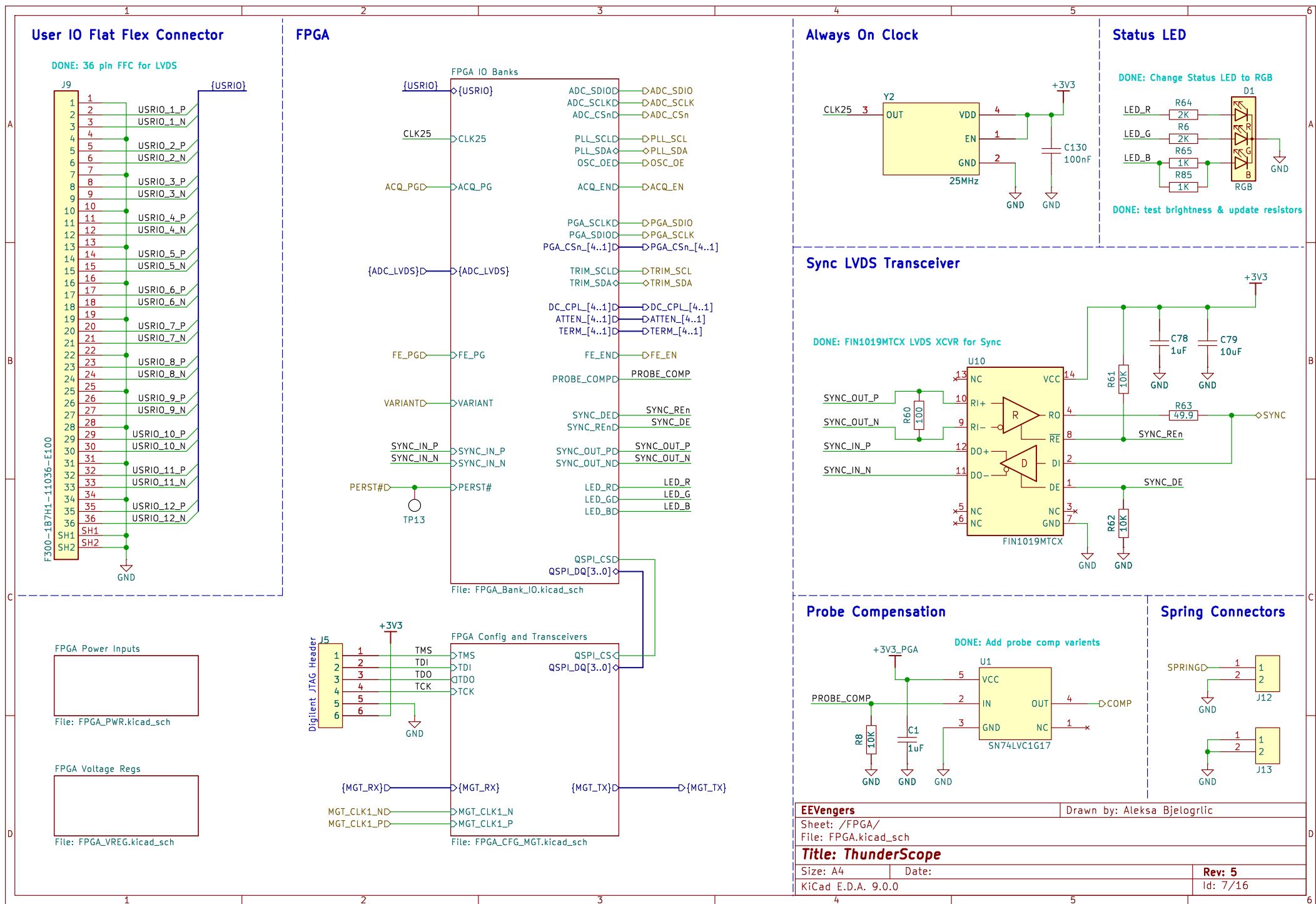
Size: A4

Drawn by: Aleksa Bjelogrlic

Rev: 5

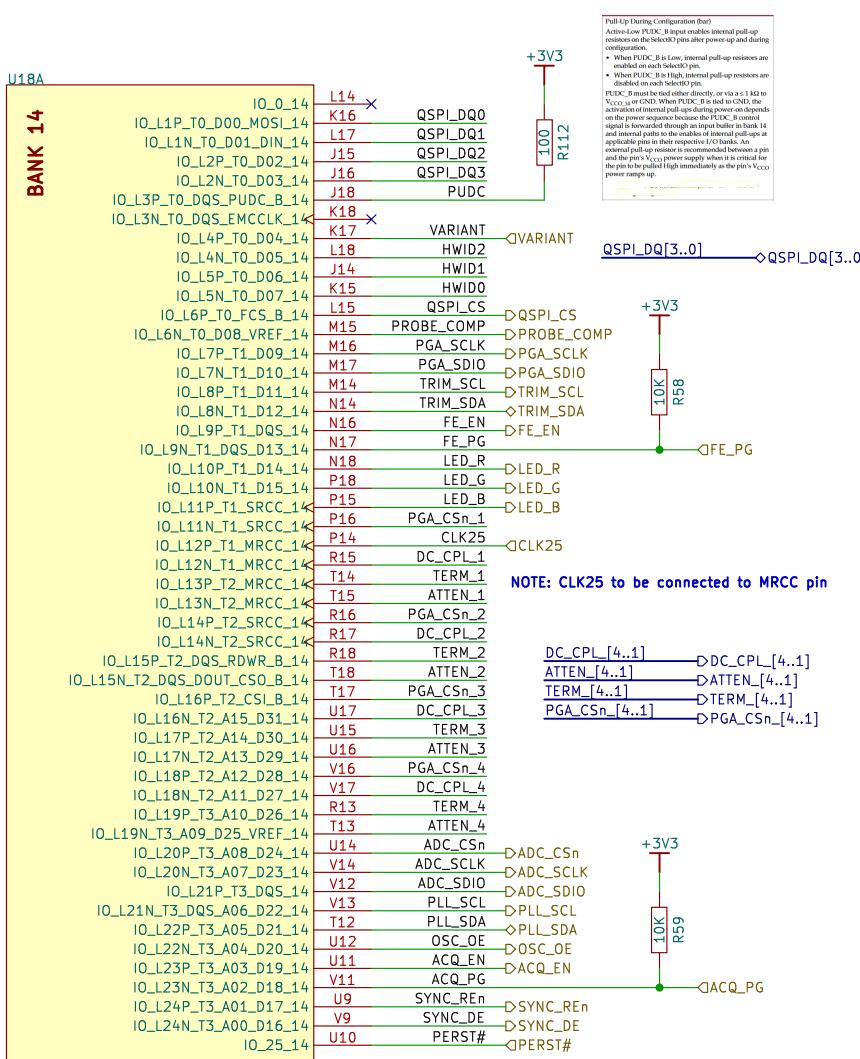
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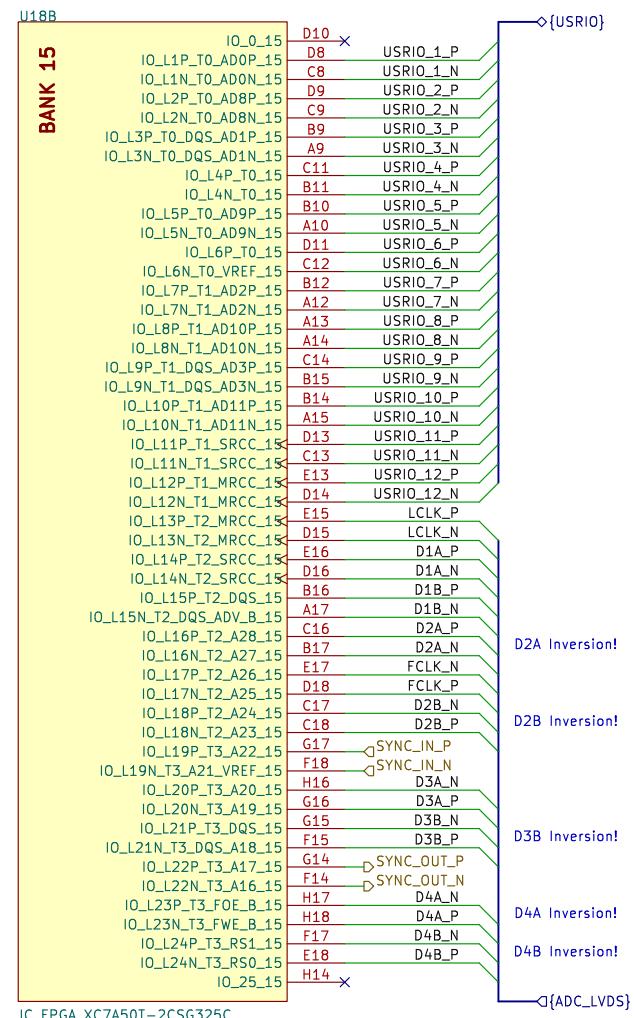


FPGA IO Banks

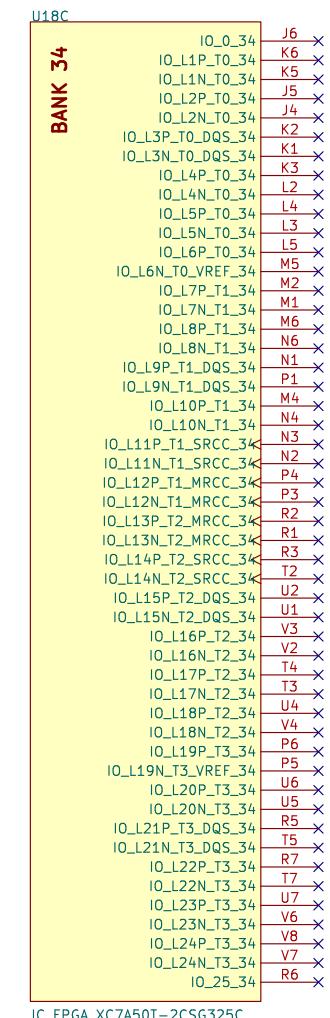
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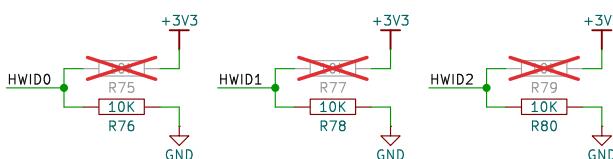
B



C



D

**EEVengers**

Sheet: /FPGA/FPGA IO Banks/
File: FPGA_Bank_IO.kicad_sch

Drawn by: Aleksa Bjelogrlic

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 9.0.0

Rev: 5

Id: 8/16

FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

Note: DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

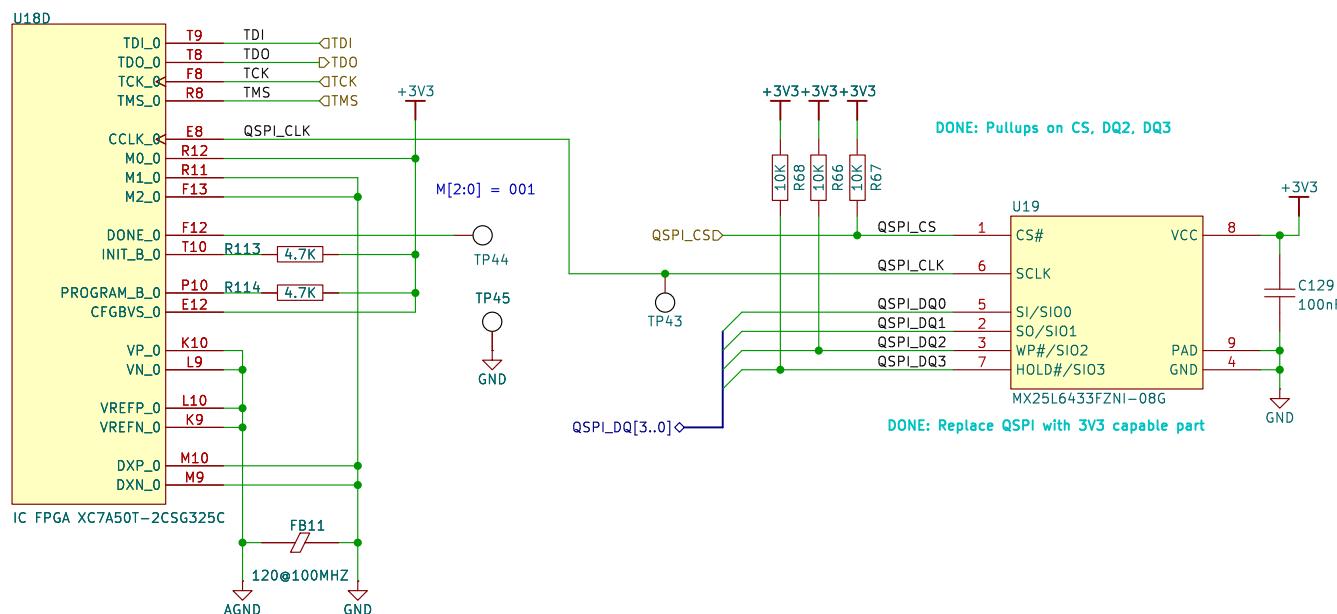
Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and

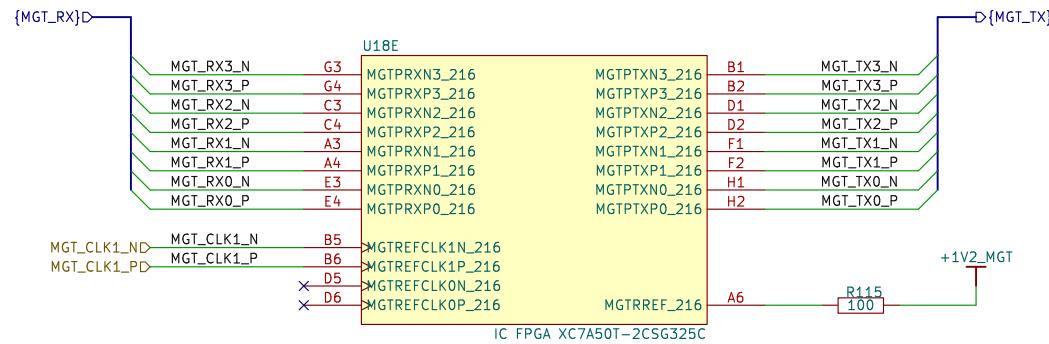
Table 2-1: 7 Series FPGA Configuration Modes				
Configuration Mode	M2[0]	Bus Width	CCLK Direction	
Master SPI	001	x1, x2, x4	Output	

Table 2-2: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

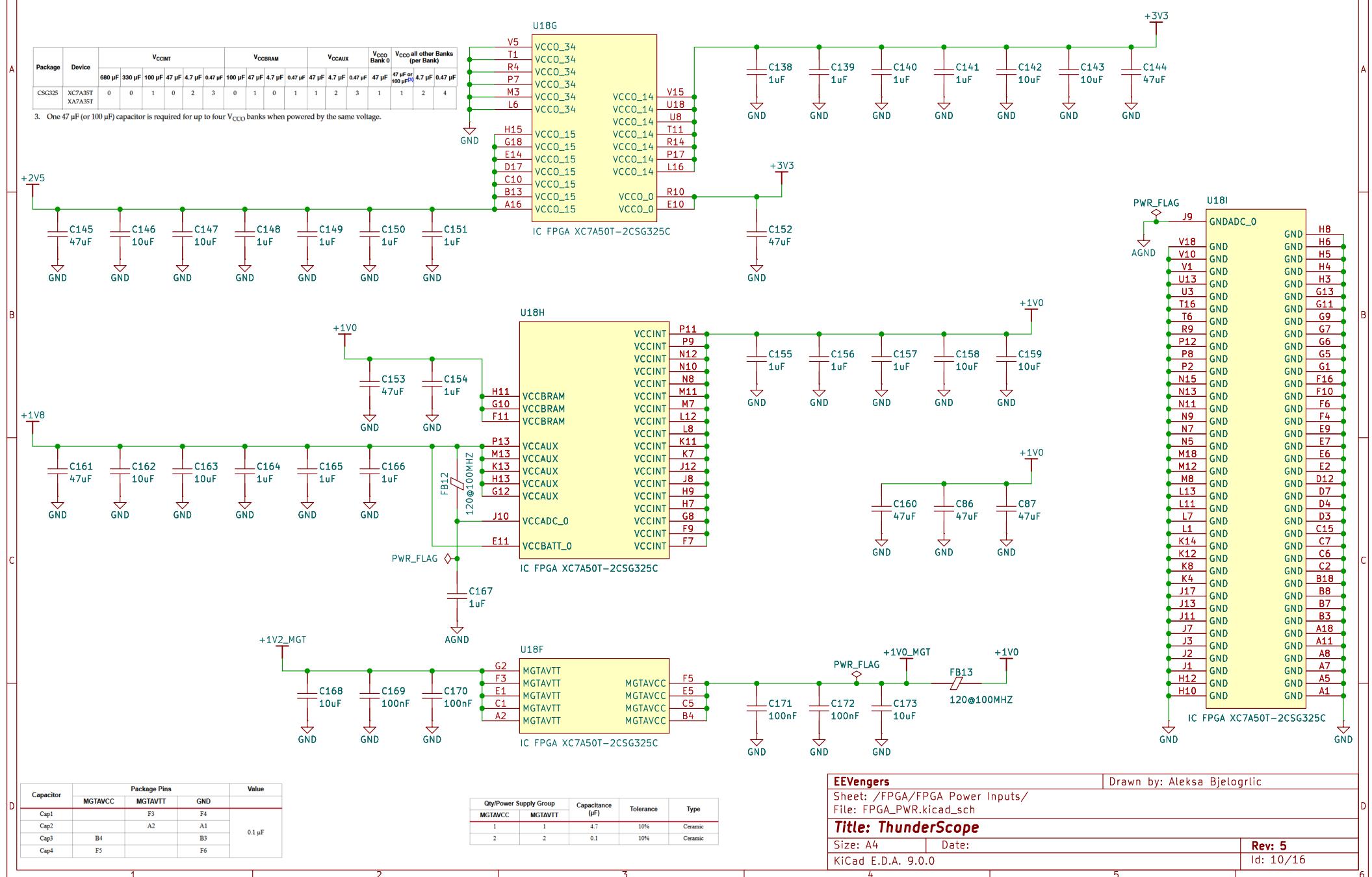
Configuration Mode	Bank Used	Configuration Interface I/O	HR Bank 0 V _{CCO} 0	HR Bank 14 V _{CCO} 14	HR Bank 15 V _{CCO} 15	CFGBVS	
JTAG (only)	0	VREFP_0	2.5V	2.5V	Any	VCCO_0	
		VREFN_0	1.8V	1.8V	Any	GND	
		DXP_0	2.5V	2.5V	2.5V	VCCO_0	
		DXN_0	1.8V	1.8V	1.8V	GND	
Serial SPI or SelectMAP	0, 14 ⁽¹⁾	VREFP_0	3.3V	3.3V	3.3V	VCCO_0	
		VREFN_0	2.5V	2.5V	2.5V	VCCO_0	
		DXP_0	2.5V	2.5V	2.5V	VCCO_0	
		DXN_0	1.8V	1.8V	1.8V	GND	
		BPI ⁽²⁾	3.3V	3.3V	3.3V	VCCO_0	
BPI ⁽²⁾	0, 14, 15	VREFP_0	2.5V	2.5V	2.5V	VCCO_0	
		VREFN_0	1.8V	1.8V	1.8V	GND	
		DXP_0	3.3V	3.3V	3.3V	VCCO_0	
		DXN_0	2.5V	2.5V	2.5V	VCCO_0	
		BPI ⁽²⁾	1.8V	1.8V	1.8V	GND	
Notes:							
1. RS232 for Multiflash or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.							
2. BPI mode is not available in the Spartan-7 family.							



FPGA Transceivers



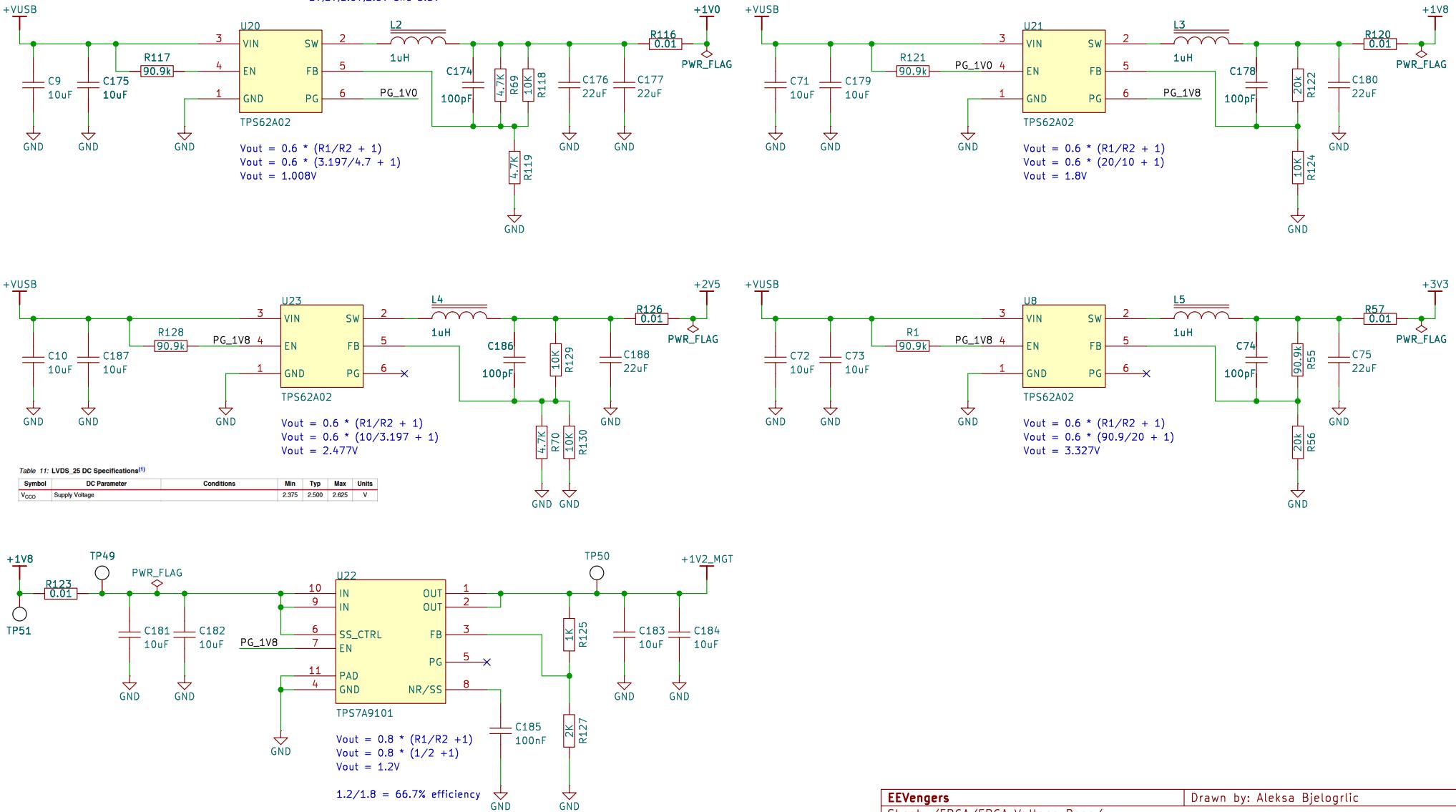
PAGE 1: FPGA Power Inputs



1 2 3 4 5 6

FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V



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Sheet: /FPGA/FPGA Voltage Regs/
File: FPGA_VREG.kicad_sch

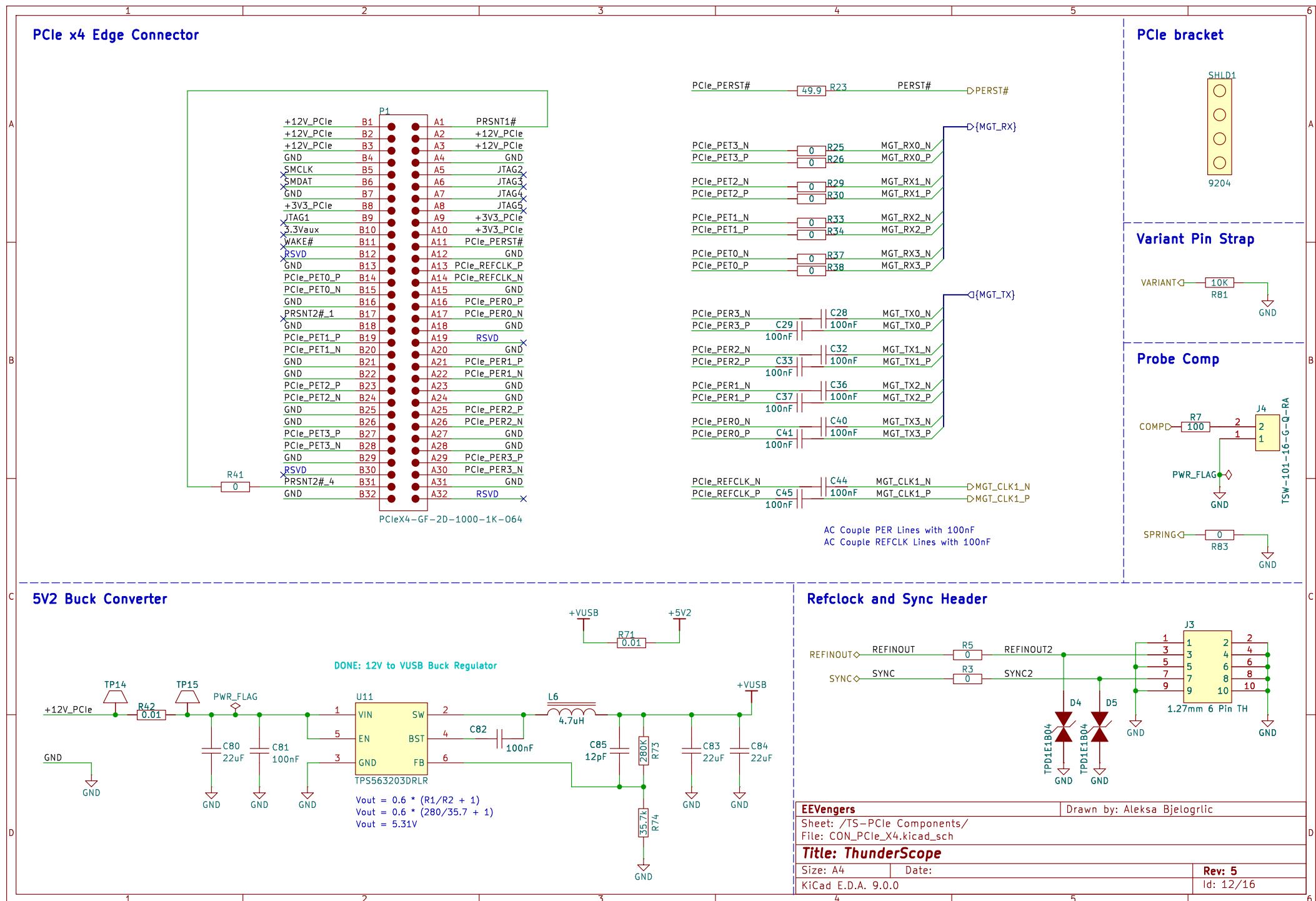
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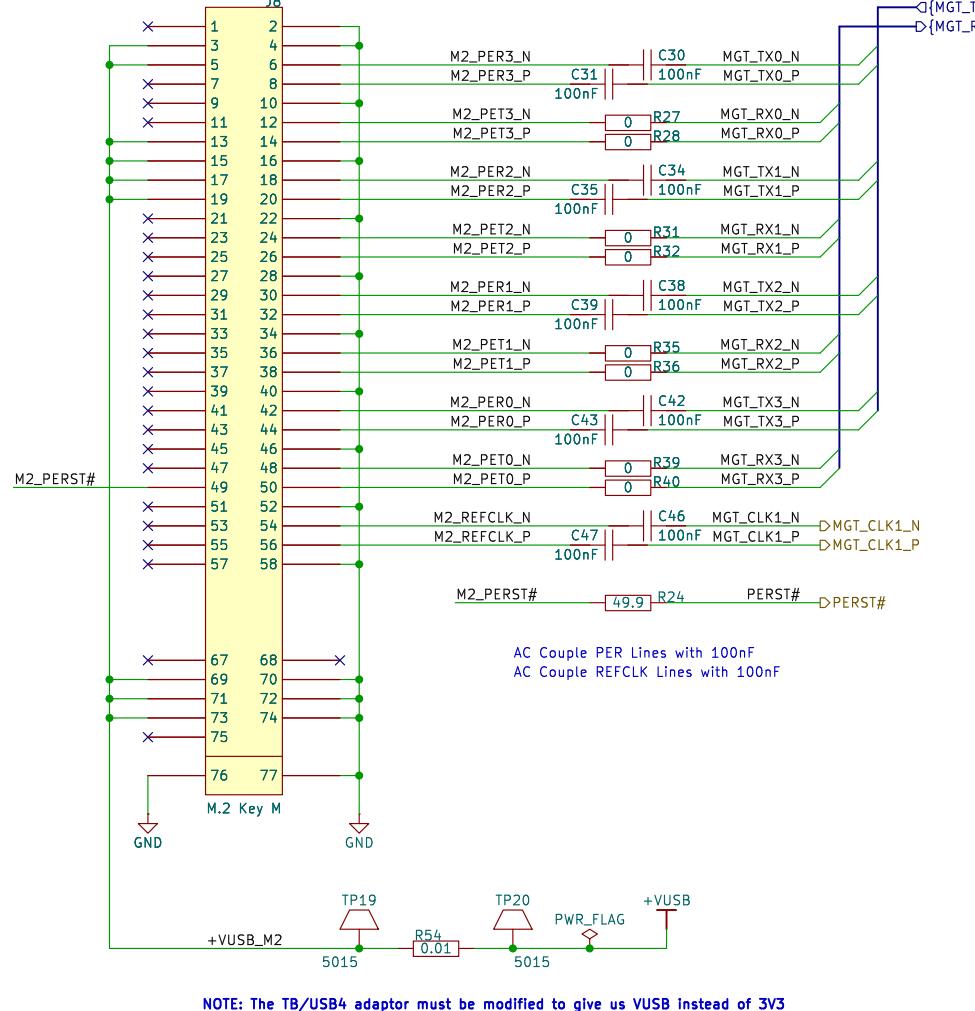
Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 11/16

1 2 3 4 5 6



M.2 Key M Connector – Custom Pinout

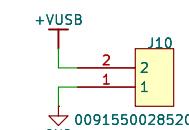


Probe Comp

COMPD → R84 → SPRING



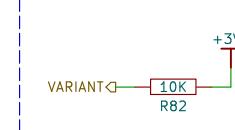
Fan Connector



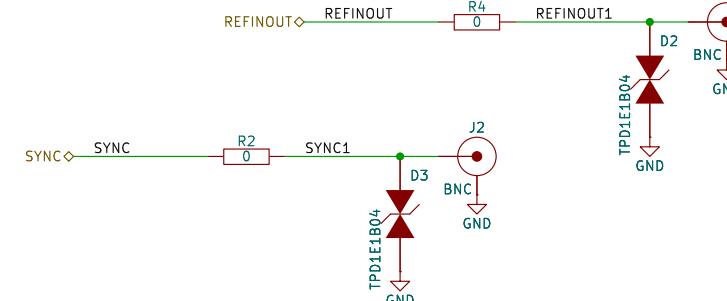
Ground Lug



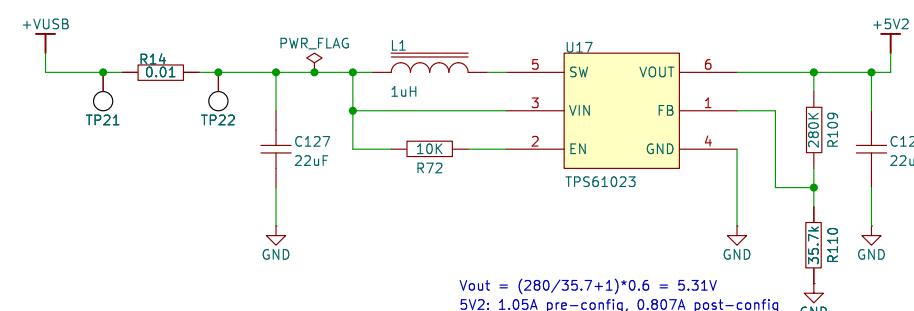
Variant Pin Strap



Refclock and Sync BNCs



5V2 Boost Converter



EEVengers

Sheet: /TS-USB4 Components/
File: M2_KEY_M.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 9.0.0

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Rev: 5
Id: 13/16