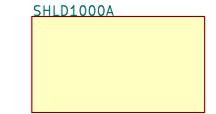
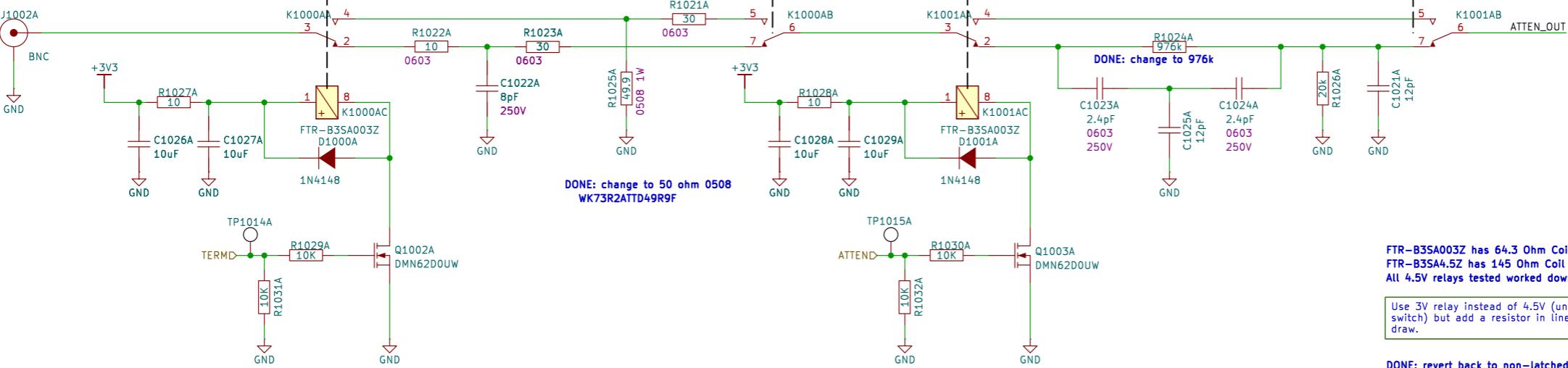
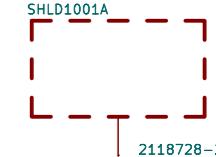


Termination and Attenuation



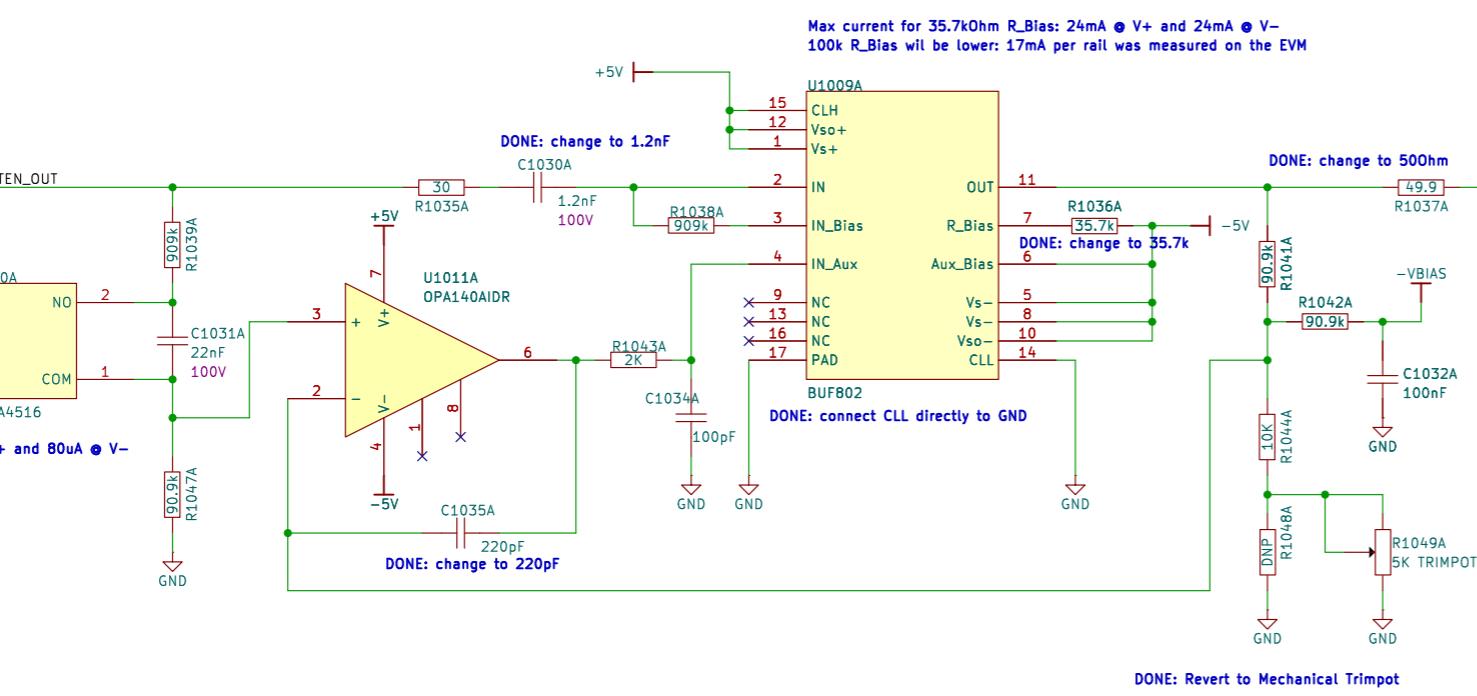
2118727-2



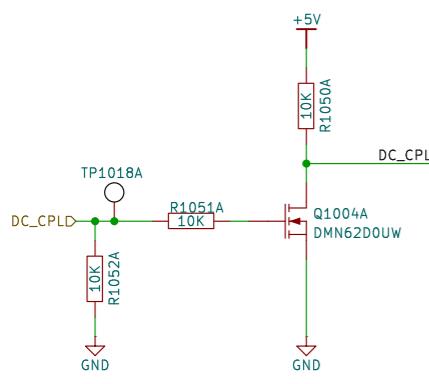
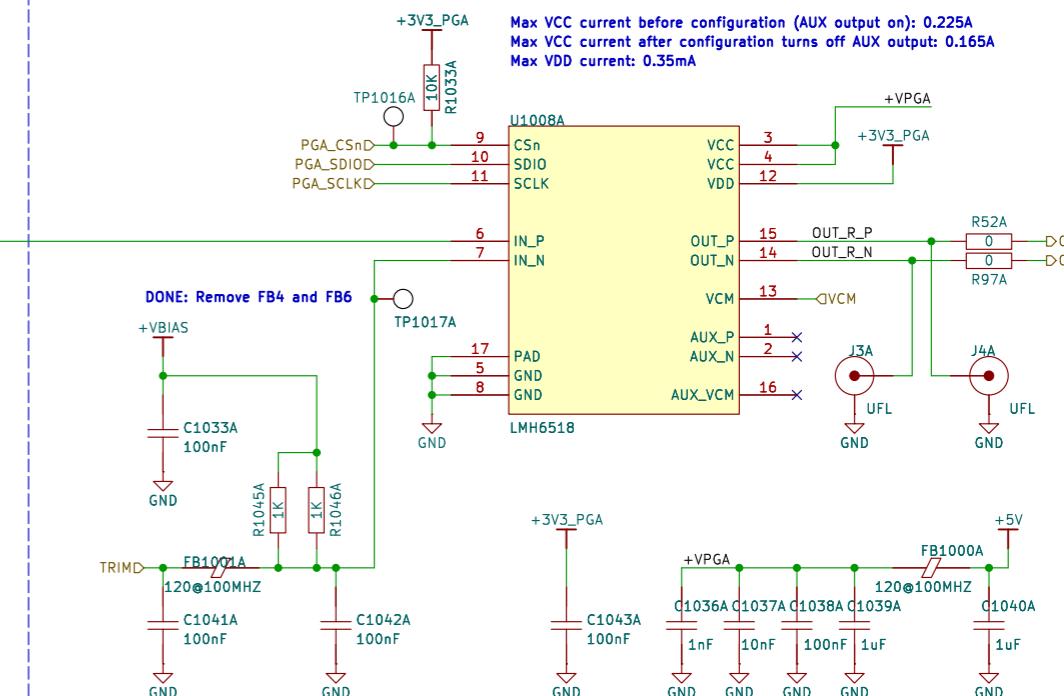
2118728-2

GND

Input Buffer and AC/DC Coupling

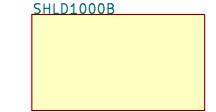
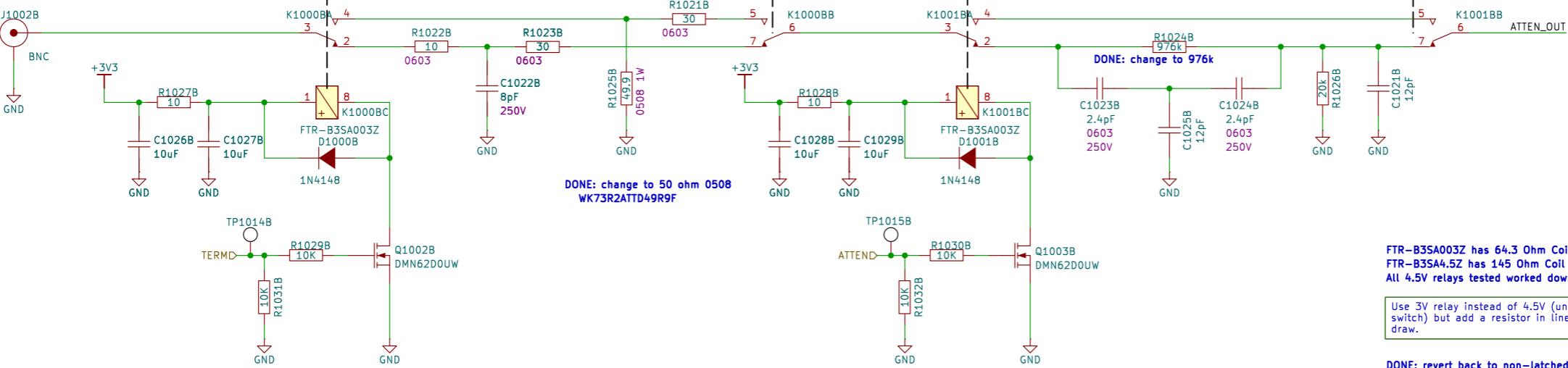


Programmable Gain Amplifier

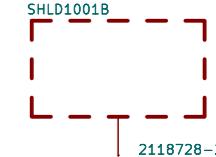


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Title: ThunderScope
Size: A3 Date:
KiCad E.D.A. 8.99.0-3188-g81ecccb21c Rev: 5
Id: 2/17

Termination and Attenuation



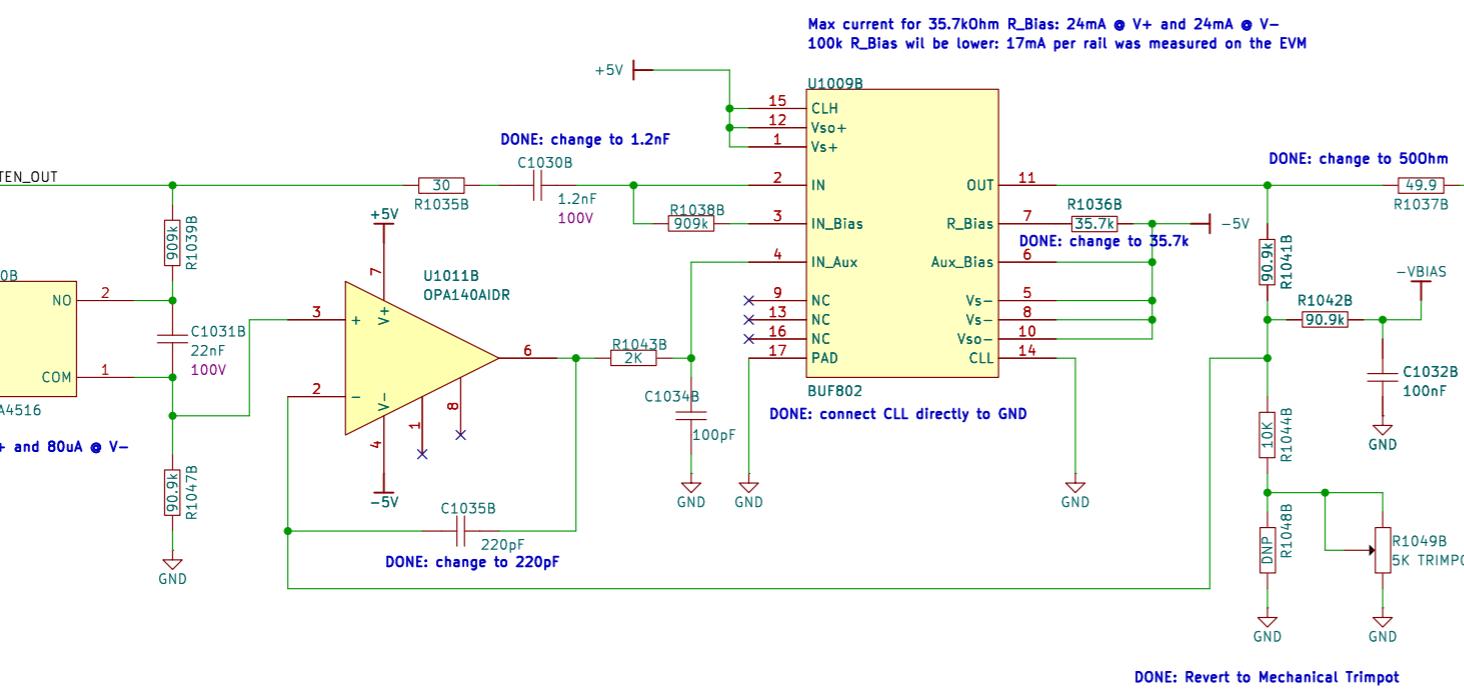
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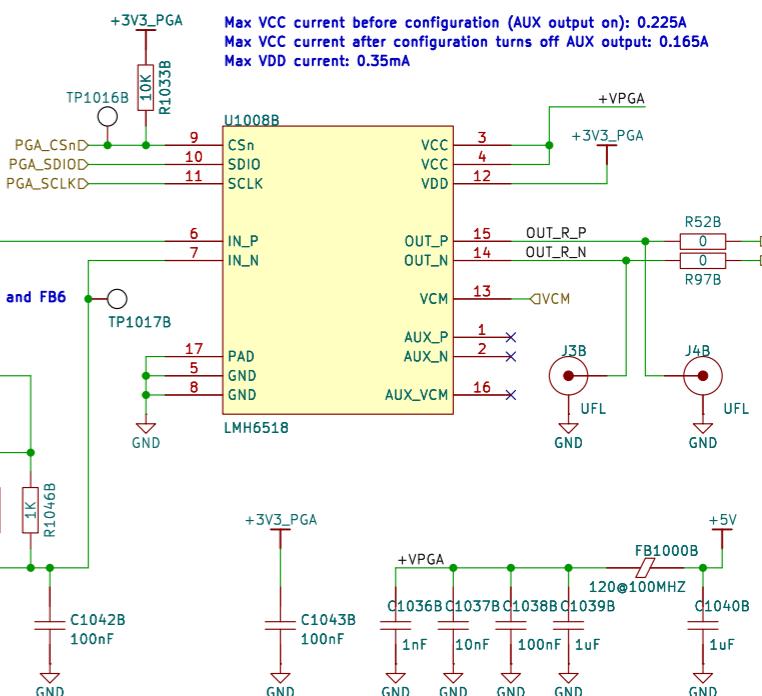
2118728-2

GND

Input Buffer and AC/DC Coupling



Programmable Gain Amplifier



EEVengers

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Title: ThunderScope

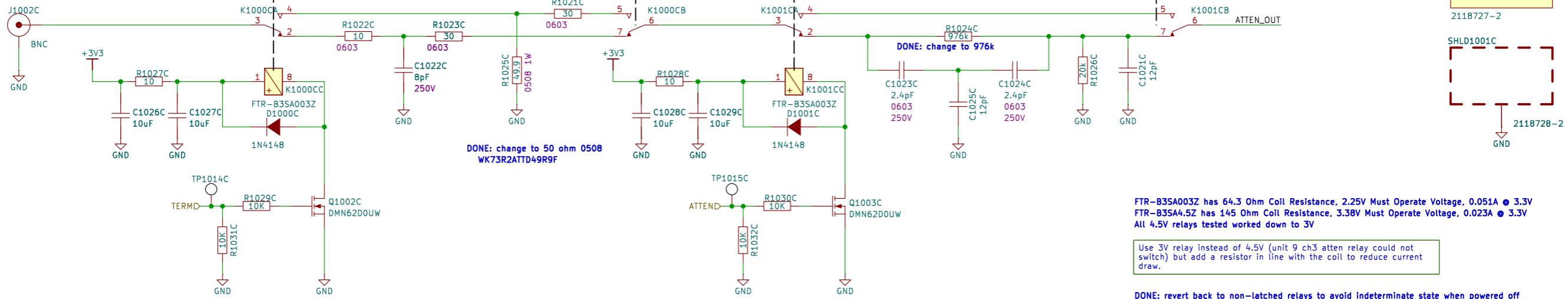
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KiCad E.D.A. 8.99.0-3188-g81ecccb21c

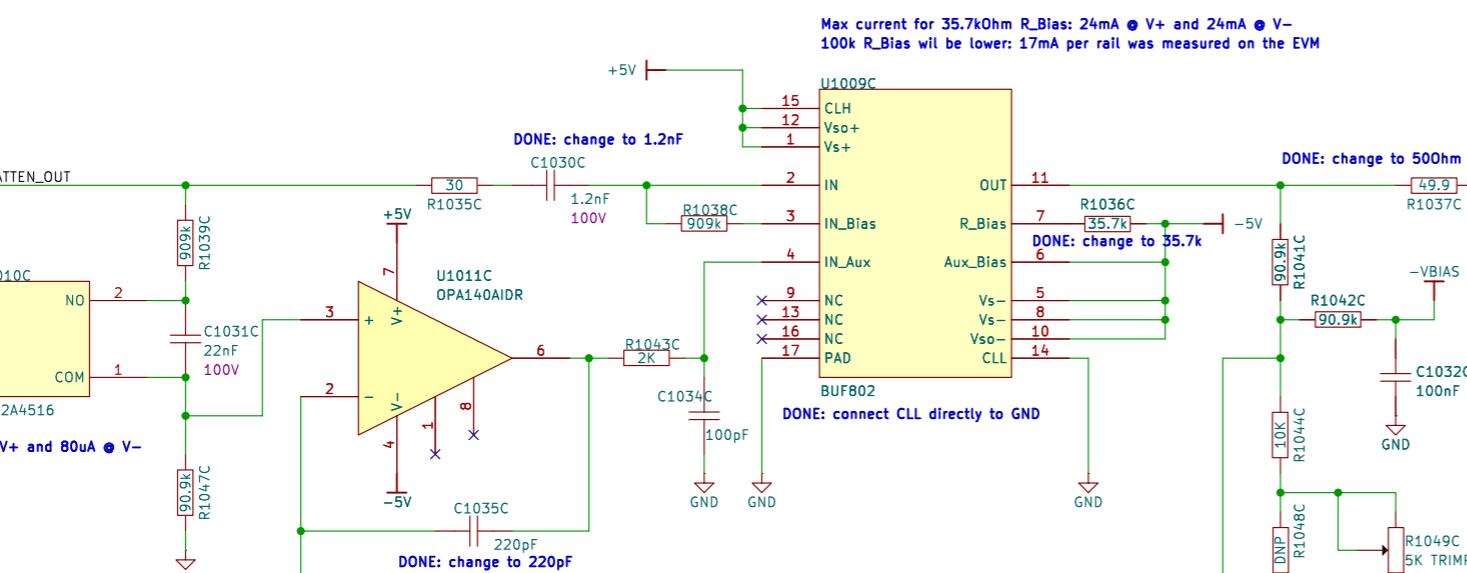
Rev: 5

Id: 2/17

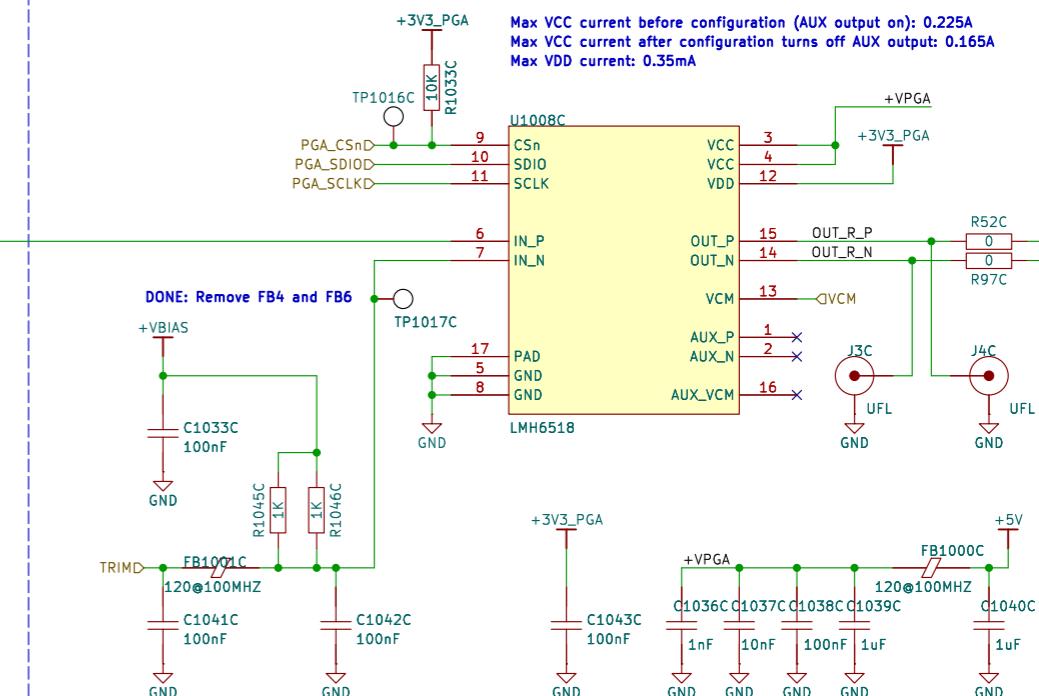
Termination and Attenuation



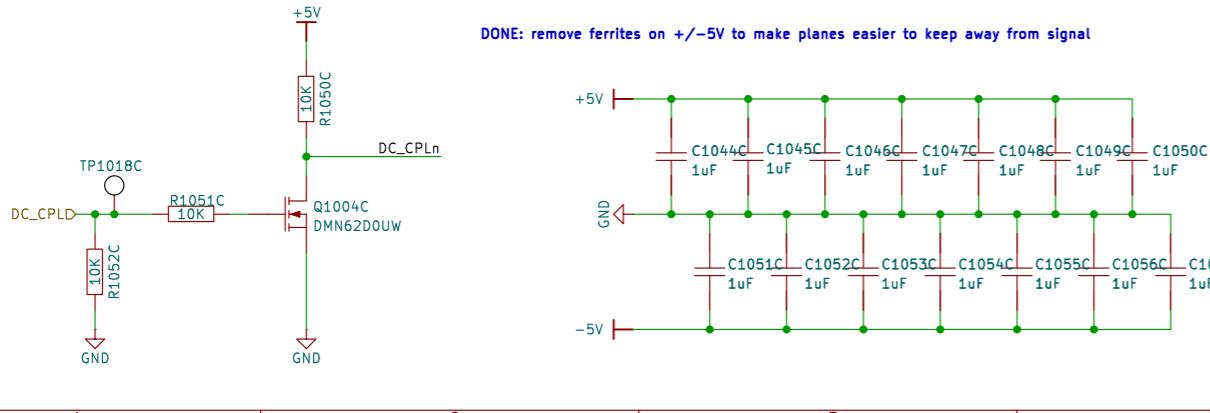
Input Buffer and AC/DC Coupling



Programmable Gain Amplifier

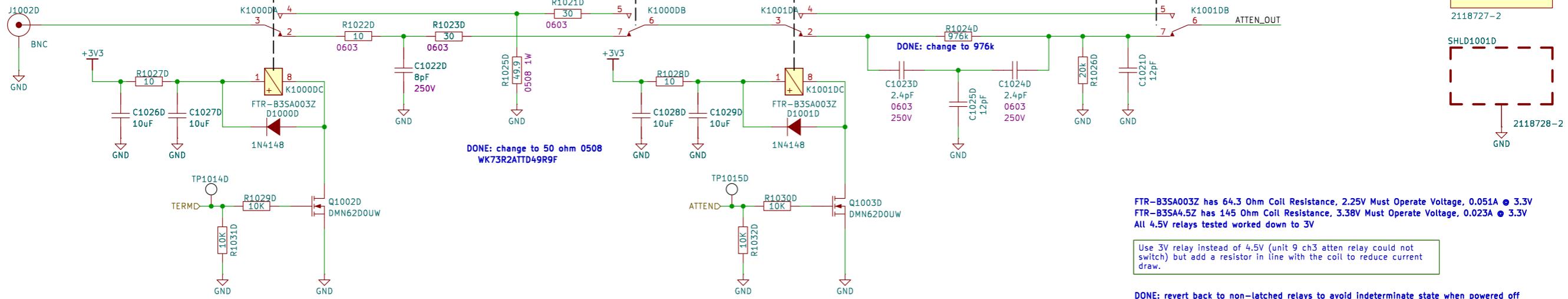


DONE: Revert to Mechanical Trim

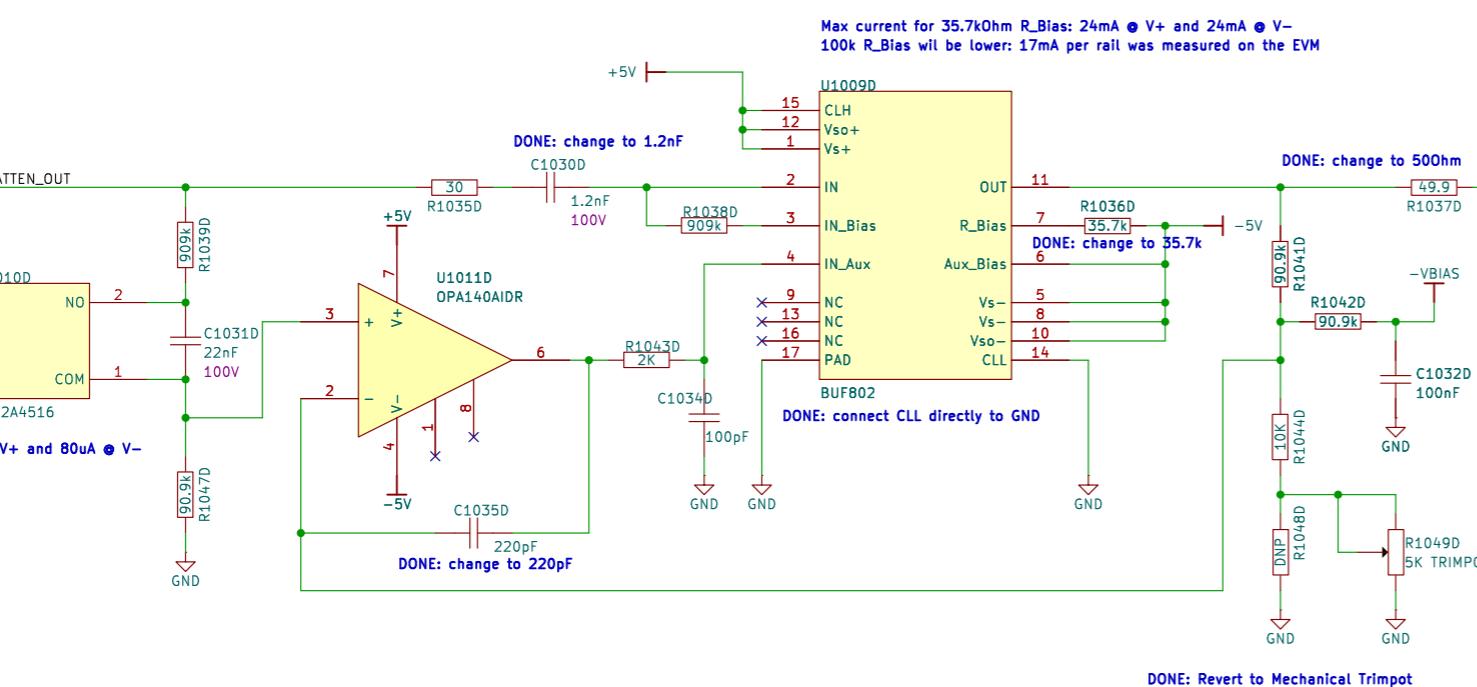


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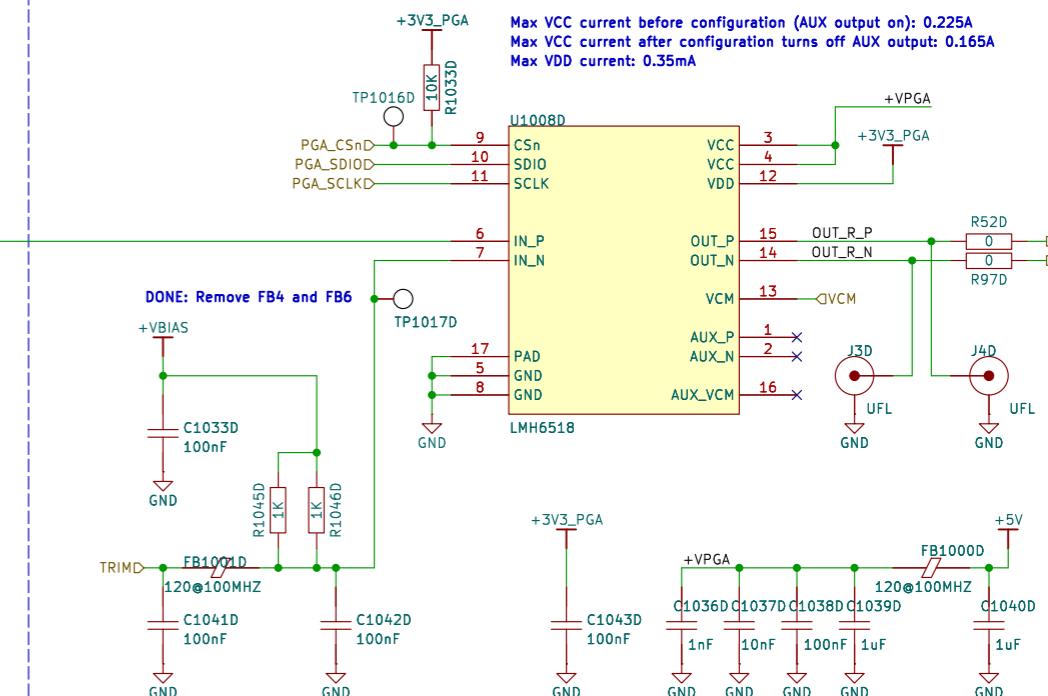
Termination and Attenuation



Input Buffer and AC/DC Coupling



Programmable Gain Amplifier

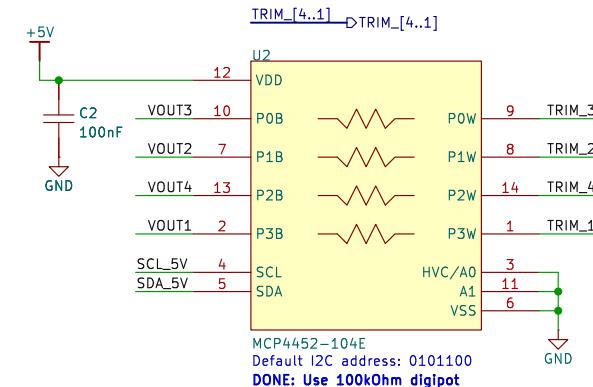
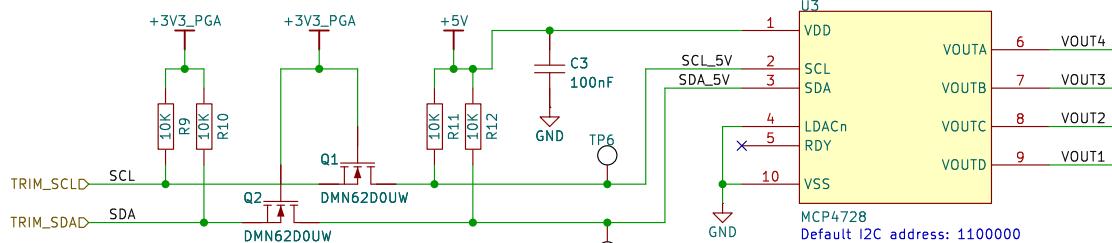


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Title: ThunderScope	
Size: A3	Date:

1 2 3 4 5 6

Offset Voltage Trim and User Offset Control

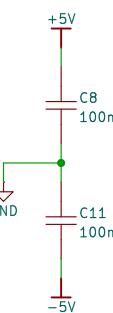
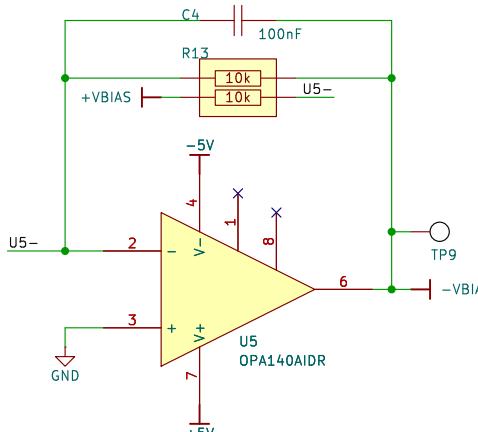
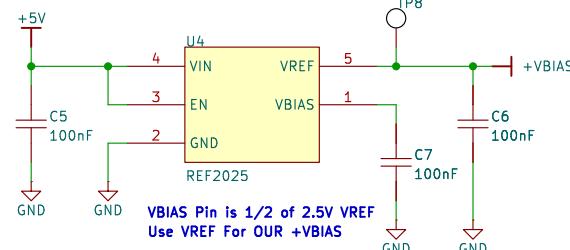
A



B

Bias Voltage Generation

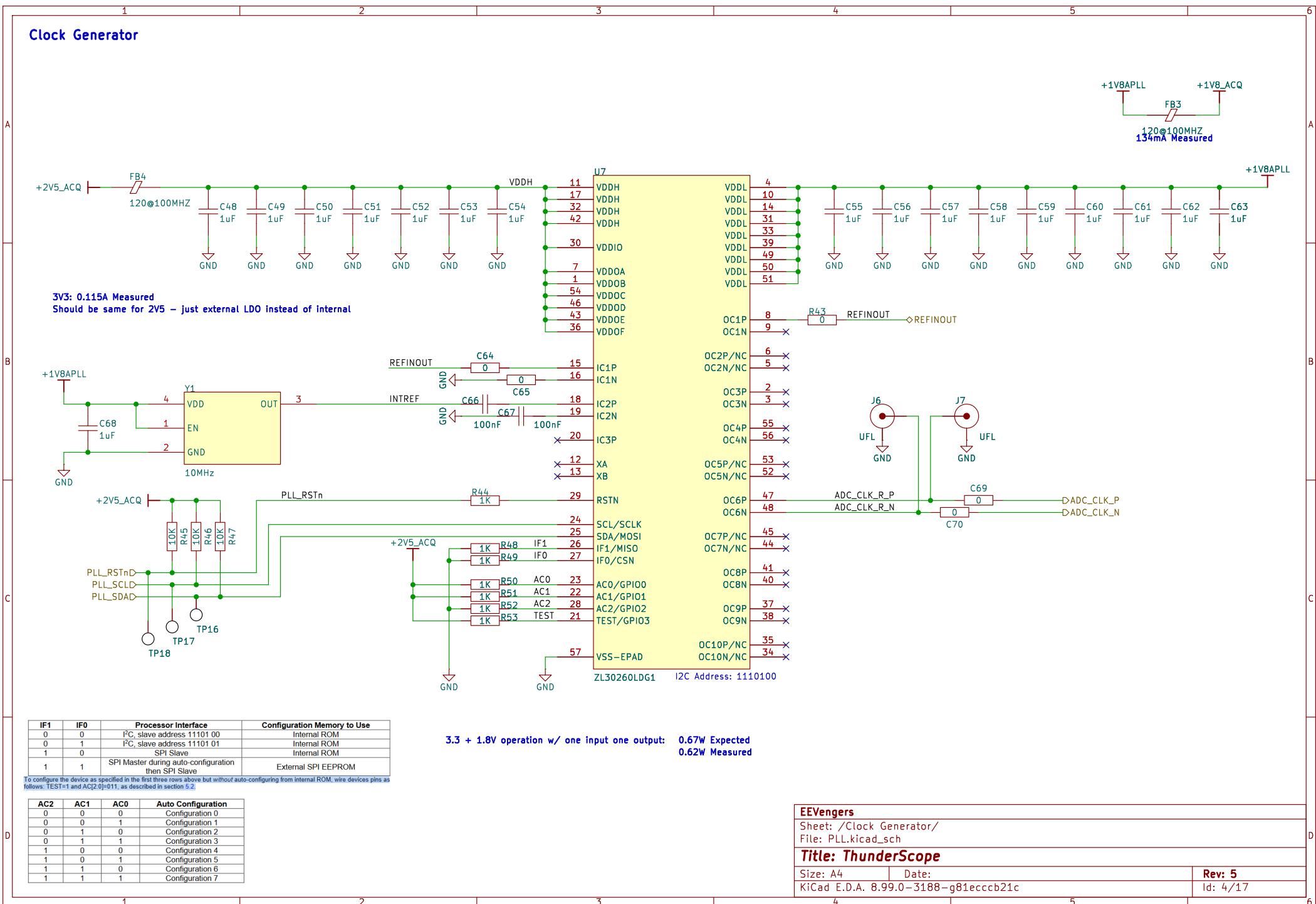
C



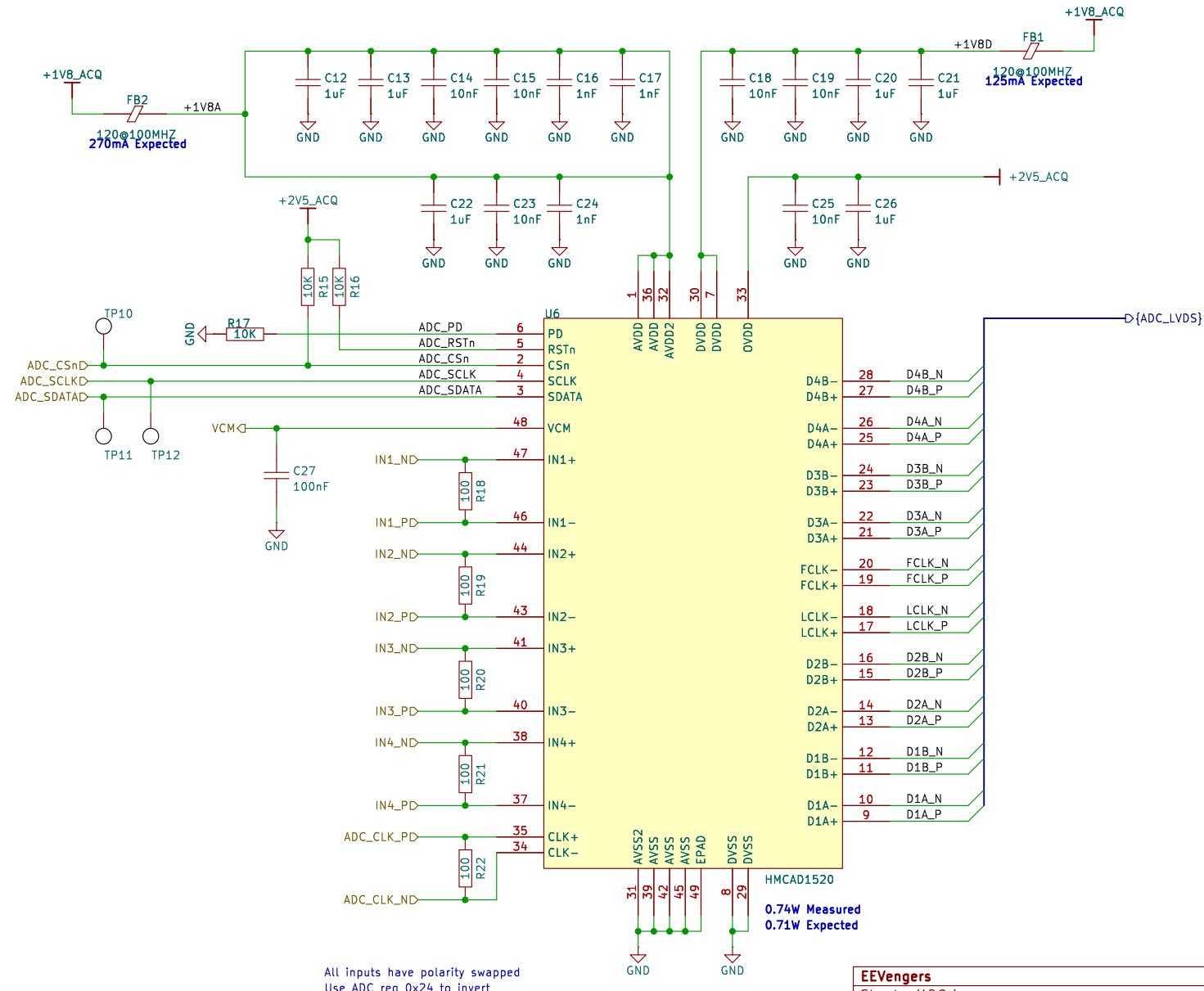
Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140
-Max resistance is $(575/4 // 10k) = 141.7 \text{ Ohm}$
-Worst case current is 17.64mA
-Use REF2025, has max current of 20mA
-Change U5 divider to matched resistor network
-ACASN1002S1002P1AT

EEVengers
Sheet: /Front End Trim and Bias/
File: FE.kicad_sch
Title: ThunderScope
Size: A4 Date:
KiCad E.D.A. 8.99.0-3188-g81ecccb21c
Rev: 5 Id: 3/17

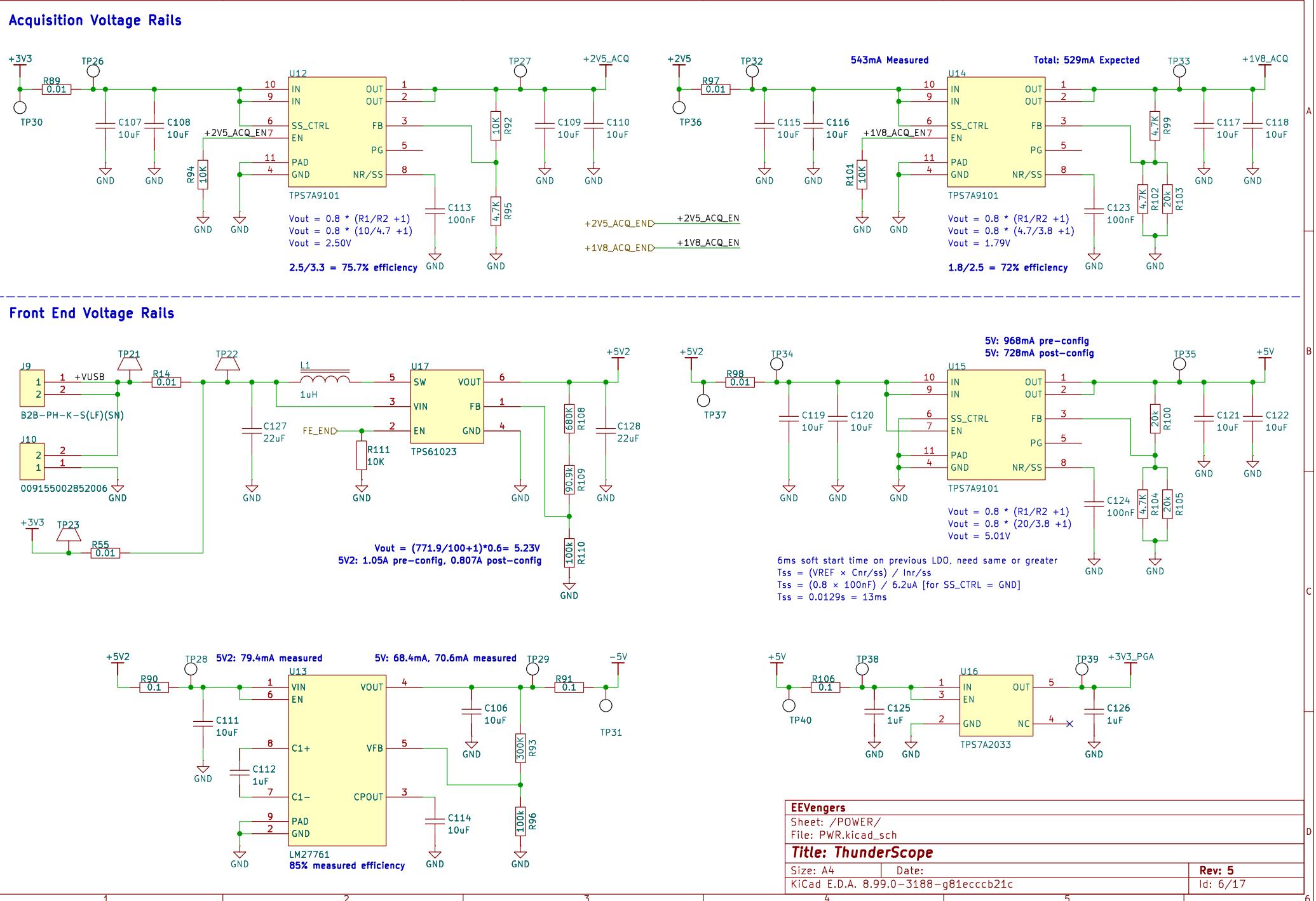
1 2 3 4 5 6

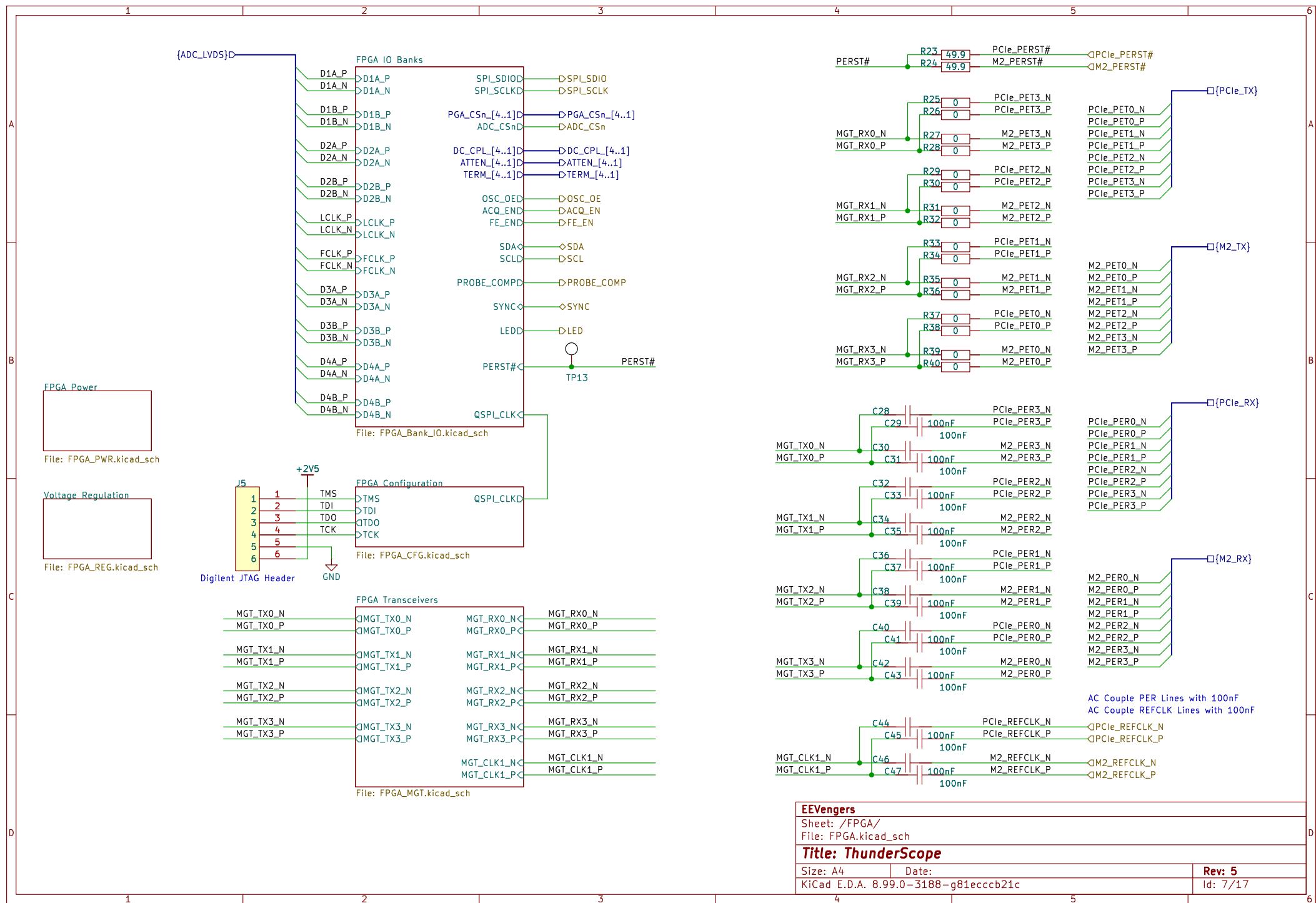


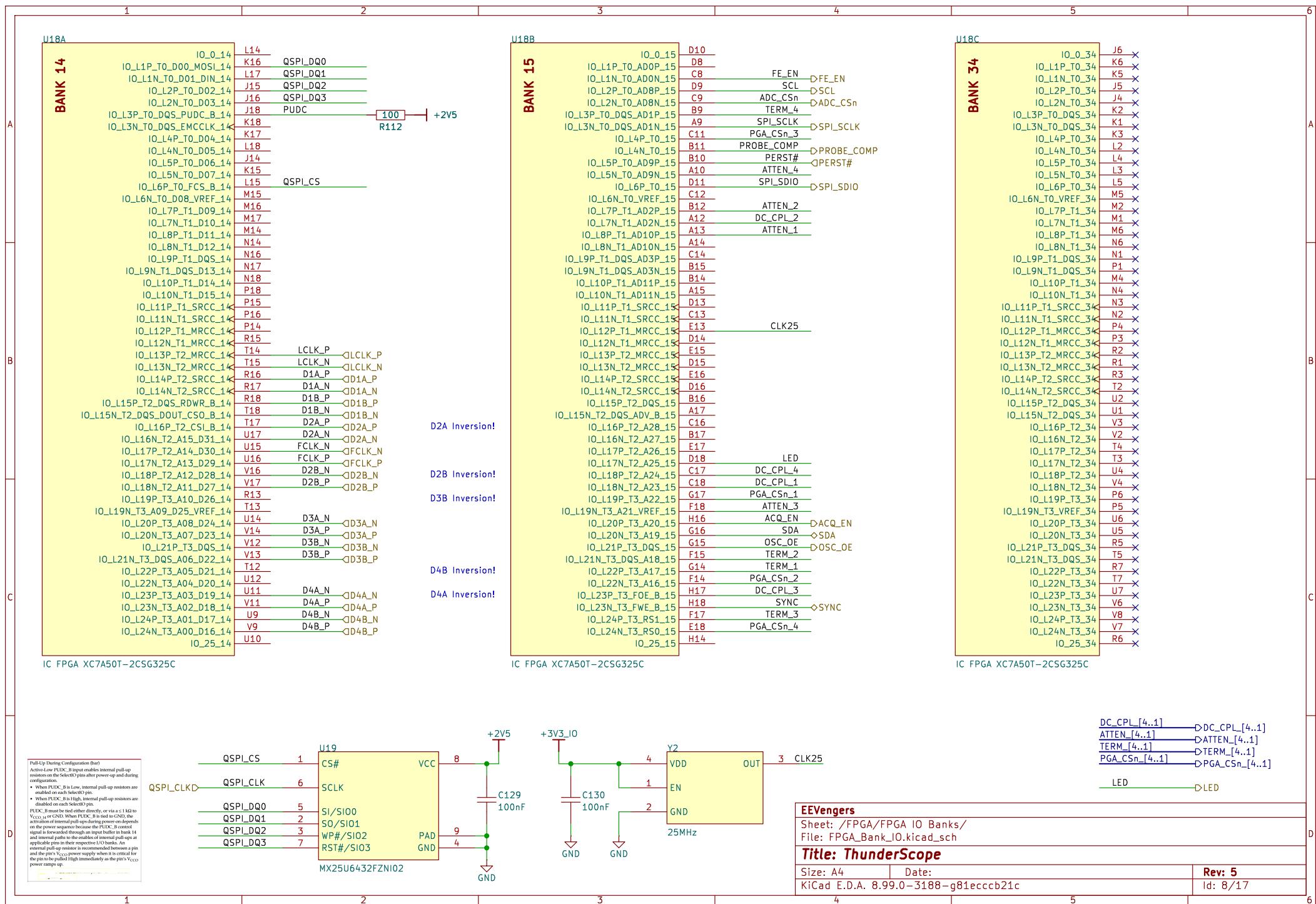
1 2 3 4 5 6

ADC**EEVengers**Sheet: /ADC/
File: ADC.kicad_sch**Title: ThunderScope**Size: A4 Date:
KiCad E.D.A. 8.99.0-3188-g81ecccb21cRev: 5
Id: 5/17

1 2 3 4 5 6







A

A

B

B

C

C

D

D

Table 2-1: 7 Series FPGA Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

M[2:0] = 001

A high signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.
Master DONE has a minimum pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE pin. If you are using the Done[6:0] register software default, eliminate the need for the DONE pin pull-up resistor. The internal pull-up circuits are not required but can be used as they have been previously described.

Connect INIT_B to a 47 kΩ pull-up resistor to VCCO_0 to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external < 47 kΩ pull-up resistor to VCCO_0 to generate a stable High input, and

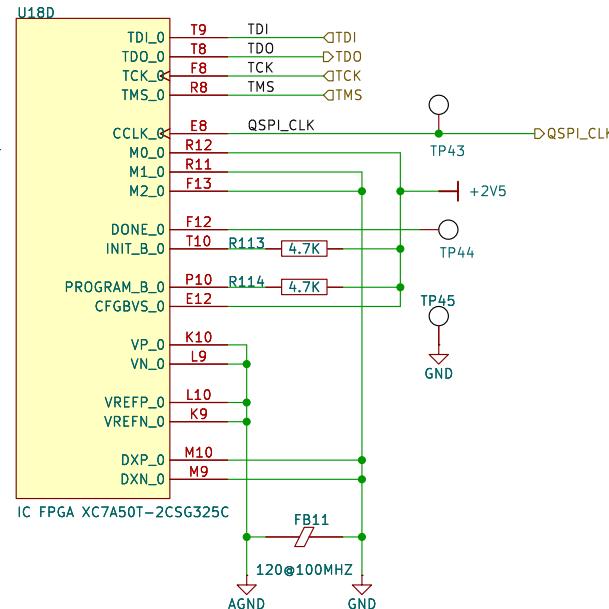


Table 2-6: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Banks Used	Configuration Interface I/O Voltage	HR Bank 0 V _{CCO_0}	HR Bank 14 V _{CCO_14}	HR Bank 15 V _{CCO_15}	CFGBVS
JTAG (only)	0	3.3V	3.3V	Any	Any	VCCO_0
		2.5V	2.5V	Any	Any	VCCO_0
		1.8V	1.8V	Any	Any	GND
		1.5V	1.5V	Any	Any	GND
Serial, SPI or SelectMAP	0, 14 ⁽¹⁾	3.3V	3.3V	3.3V	Any	VCCO_0
		2.5V	2.5V	2.5V	Any	VCCO_0
		1.8V	1.8V	1.8V	Any	GND
		1.5V	1.5V	1.5V	Any	GND
BPI ⁽²⁾	0, 14, 15	3.3V	3.3V	3.3V	3.3V	VCCO_0
		2.5V	2.5V	2.5V	2.5V	VCCO_0
		1.8V	1.8V	1.8V	1.8V	GND
		1.5V	1.5V	1.5V	1.5V	GND

Notes:

1. RS1:0 for MultiBoot or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.

2. BPI mode is not available in the Spartan-7 family.

EEVengers

Sheet: /FPGA/FPGA Configuration/

File: FPGA_CFG.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 8.99.0-3188-g81ecccb21c

Rev: 5

Id: 9/17

A

A

B

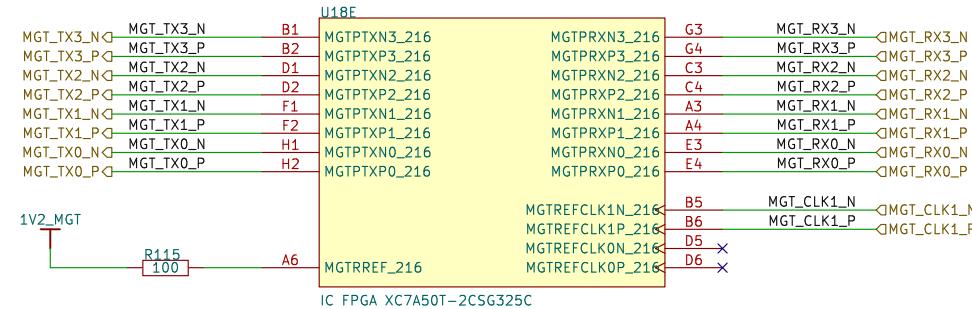
B

C

C

D

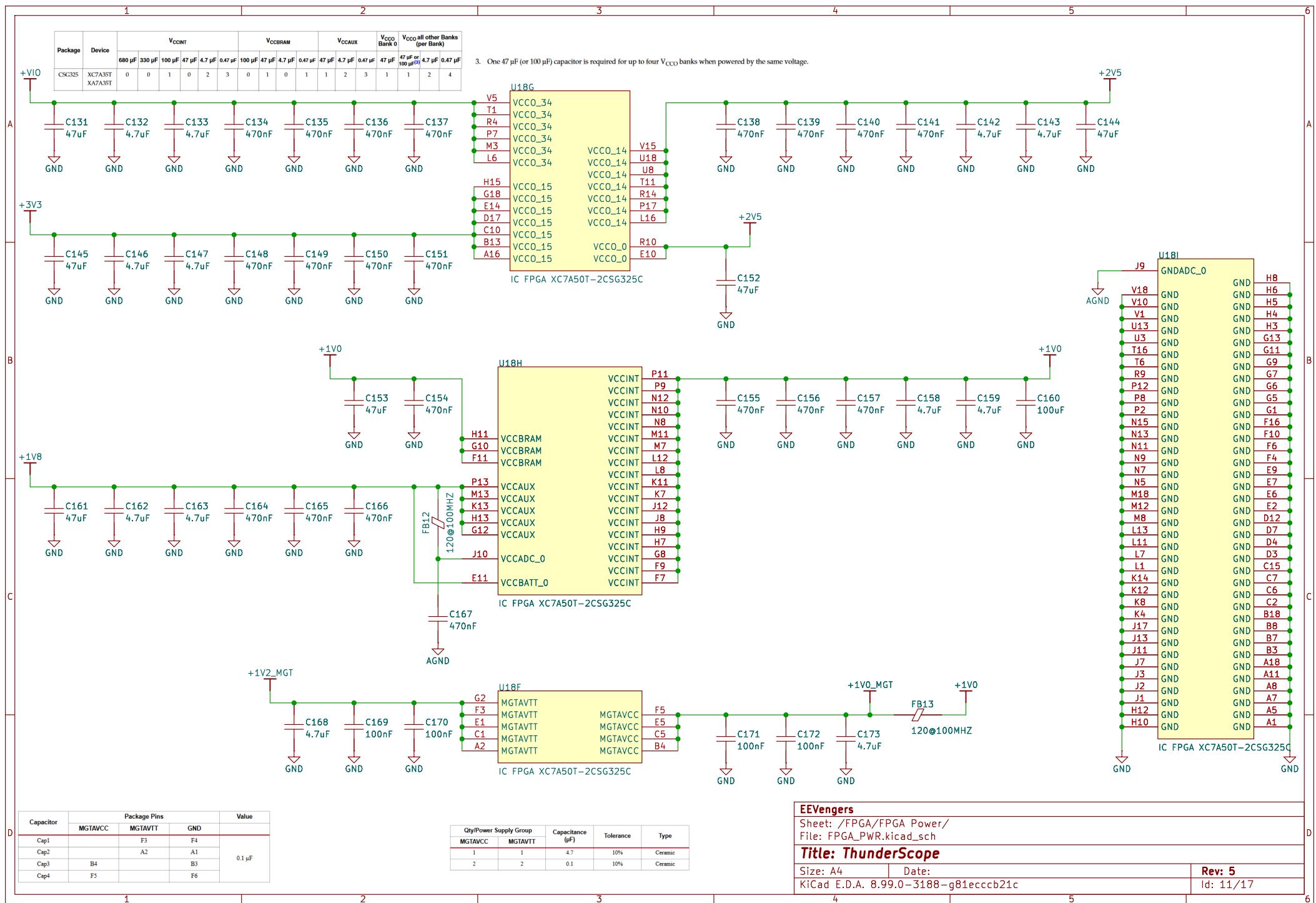
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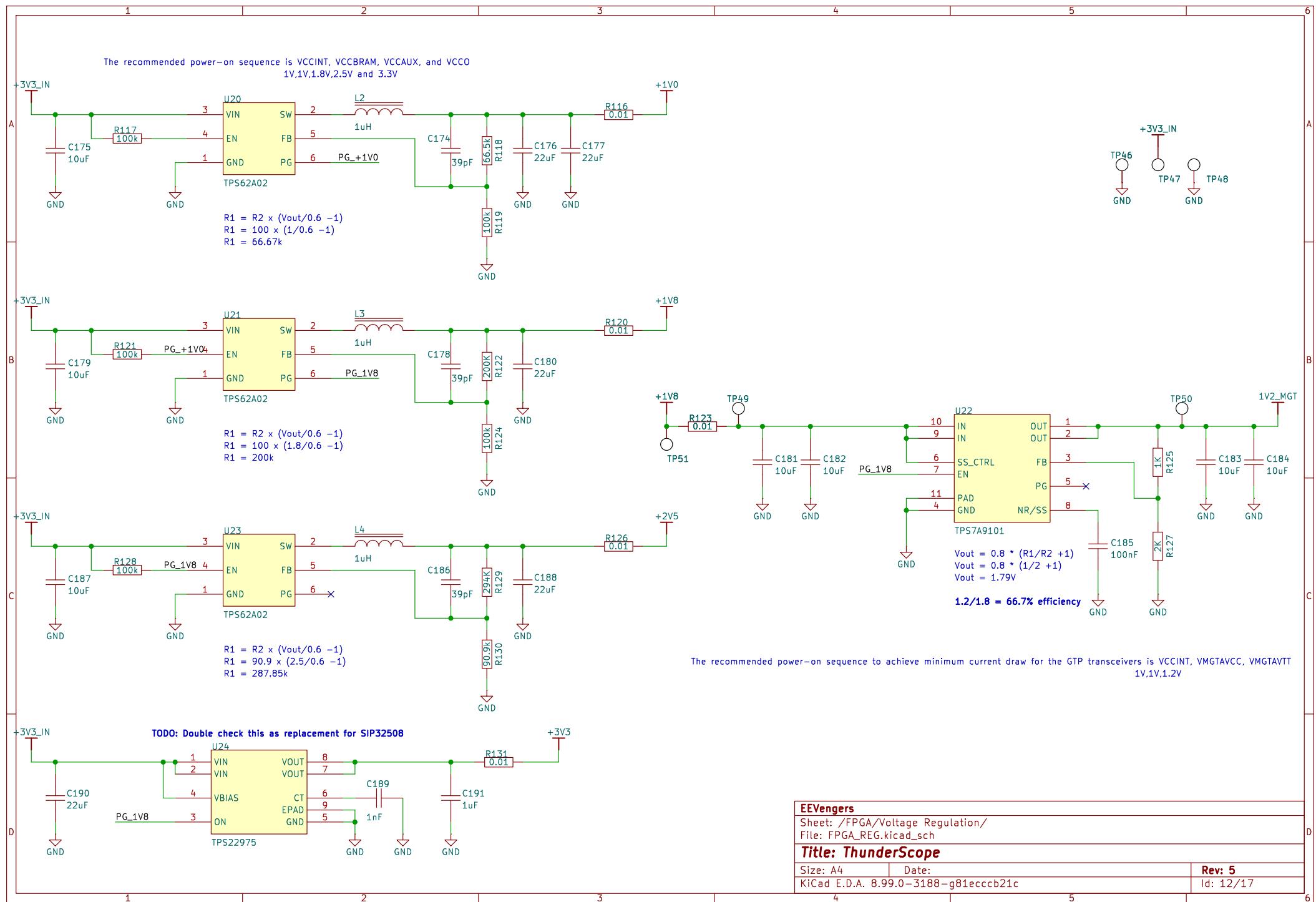
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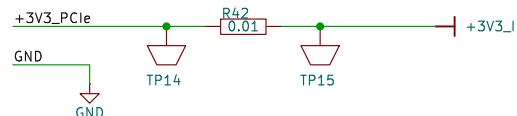
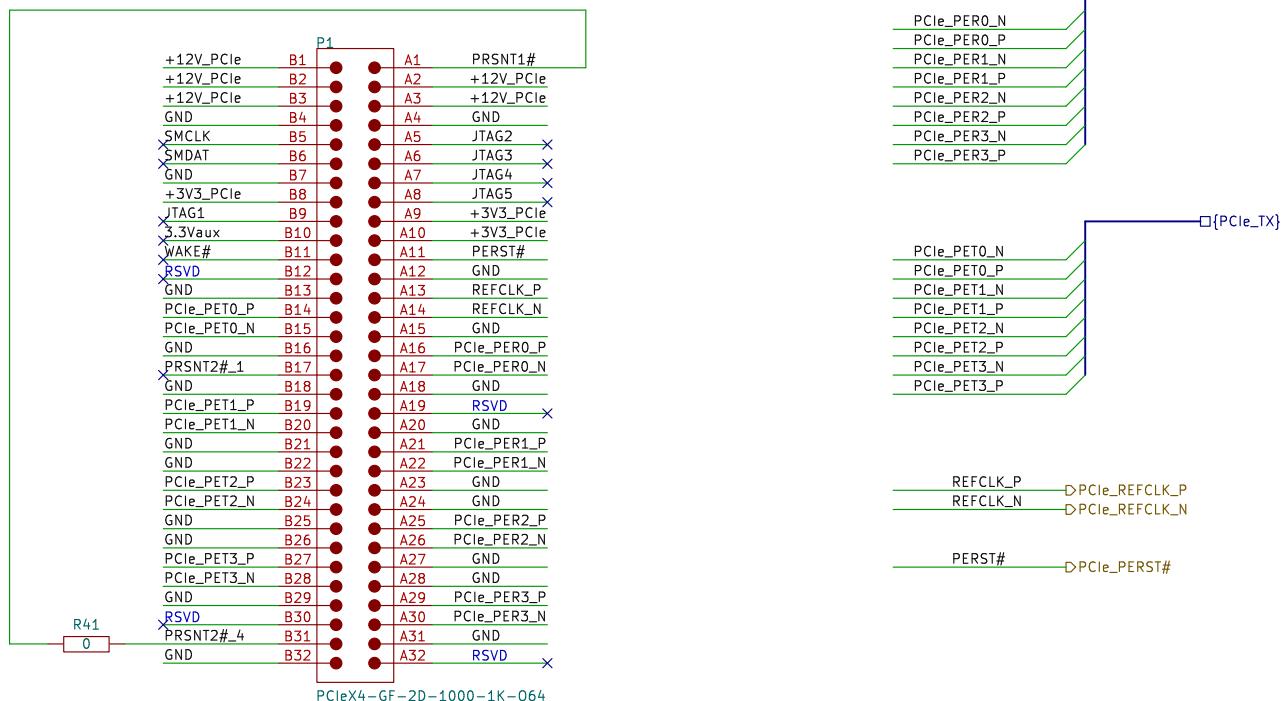
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File: FPGA_MGT.kicad_sch

Title: ThunderScope

Size: A4	Date:	Rev: 5
KiCad E.D.A. 8.99.0-3188-g81ecccb21c		Id: 10/17





PCIe x4 Edge Connector

- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

EEVengers

Sheet: /PCIe_x4/
File: CON_PCIe_X4.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0-3188-g81ecccb21c

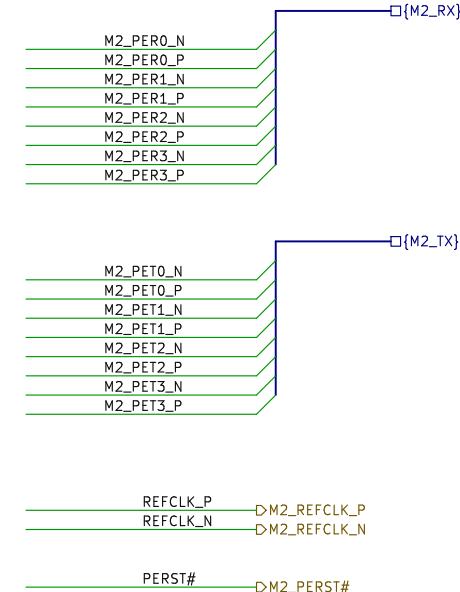
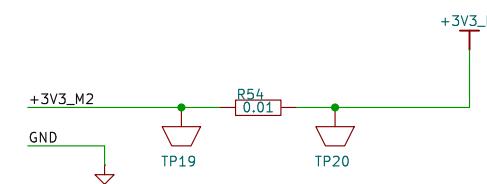
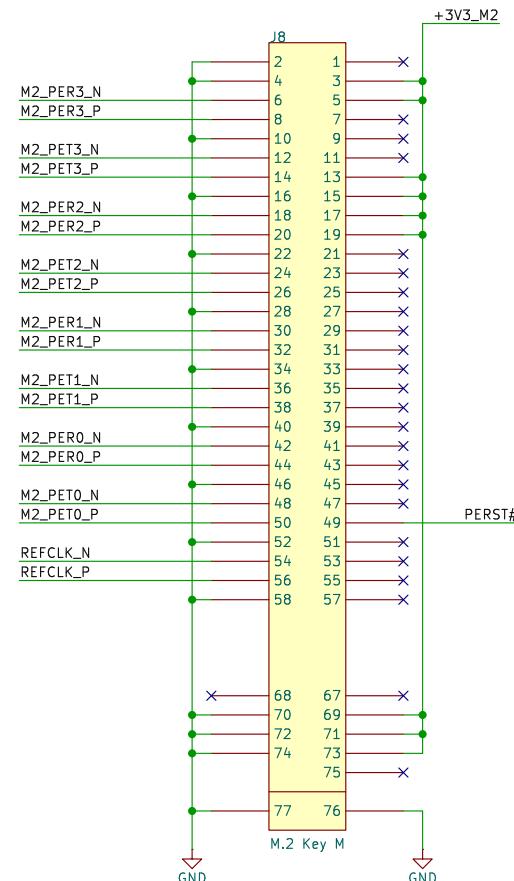
Rev: 5
Id: 13/17

1 2 3 4 5 6

M.2 Key M Connector

A

Main Board
Custom Pinout



EEVengers

Sheet: /M.2_Key_M/
File: M2_KEY_M.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0-3188-g81ecccb21c

Rev: 5
Id: 14/17

1 2 3 4 5 6