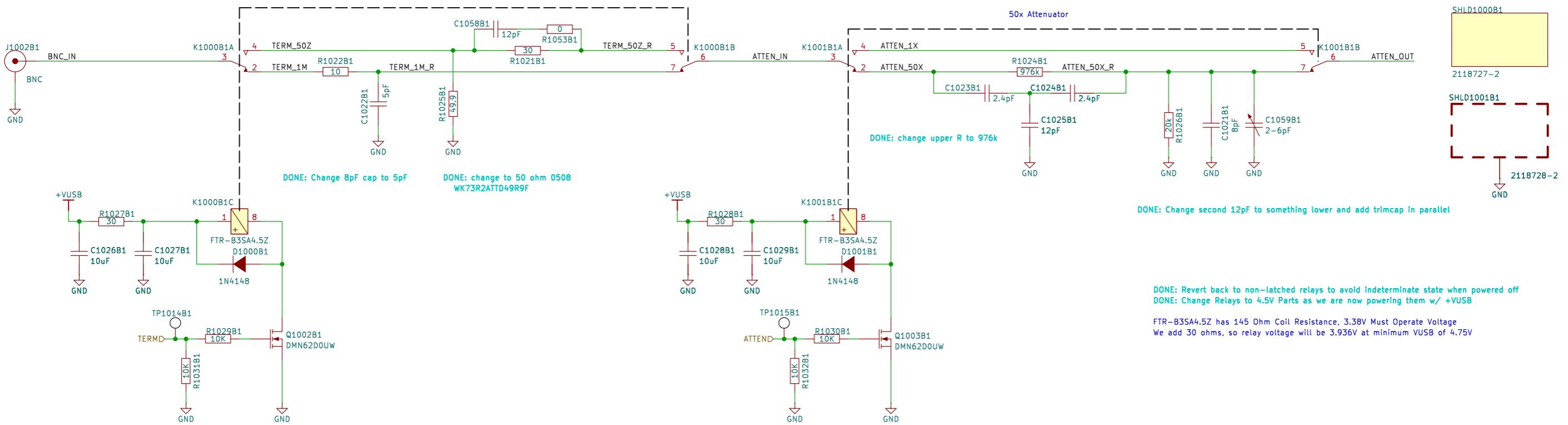


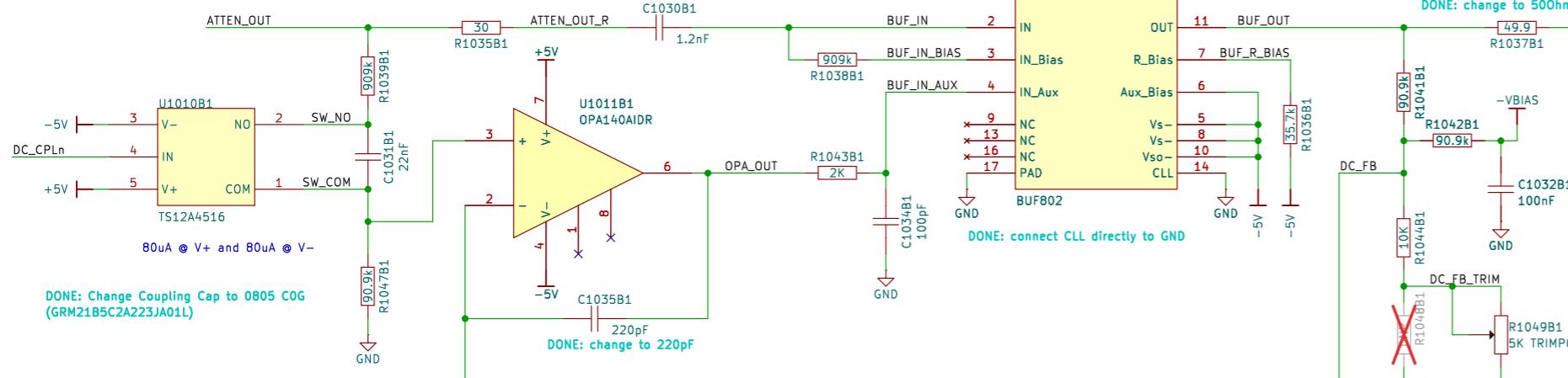
Termination and Attenuation

DONE: add cap + resistor across 30 Ohm resistor in 50Z path



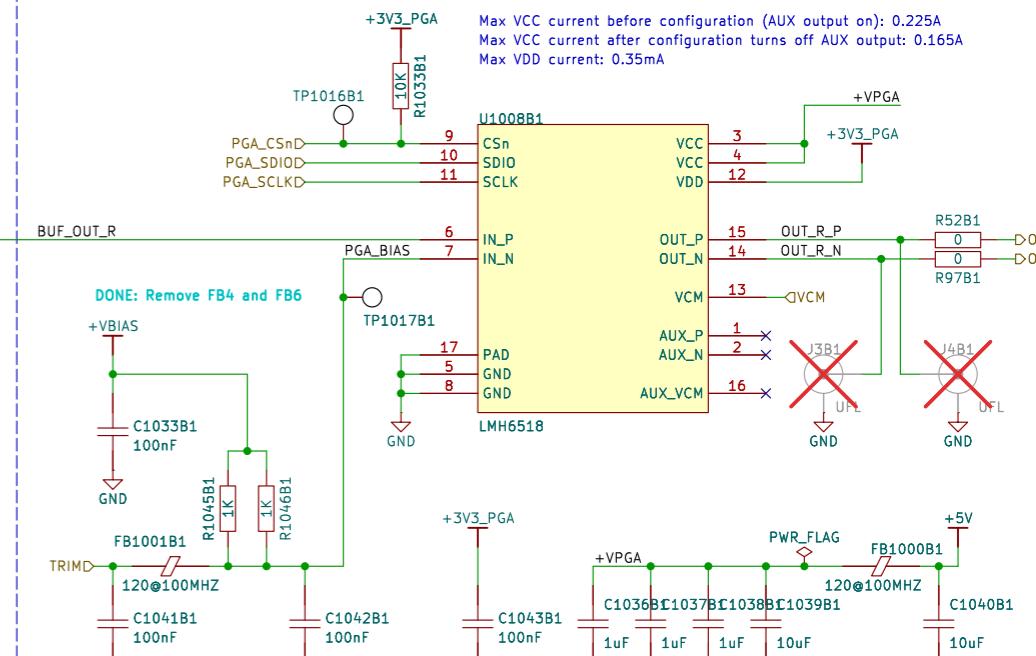
Input Buffer and AC/DC Coupling

Max current for 35.7kOhm R_Bias: 24mA @ V+ and 24mA @ V-
100k R_Bias will be lower; 17mA per rail was measured on the EVB



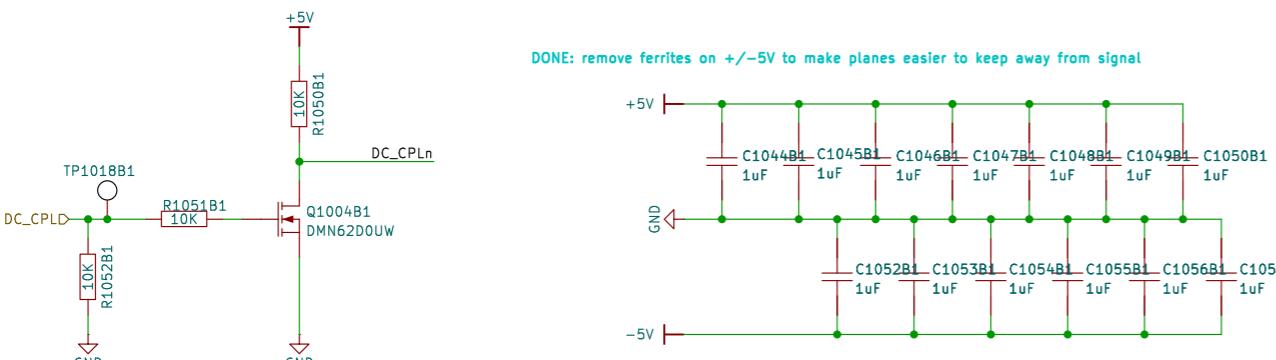
Programmable Gain Amplifier

Max VCC current before configuration (AUX output on): 0.225A
Max VCC current after configuration turns off AUX output: 0.165A
Max VDD current: 0.35mA

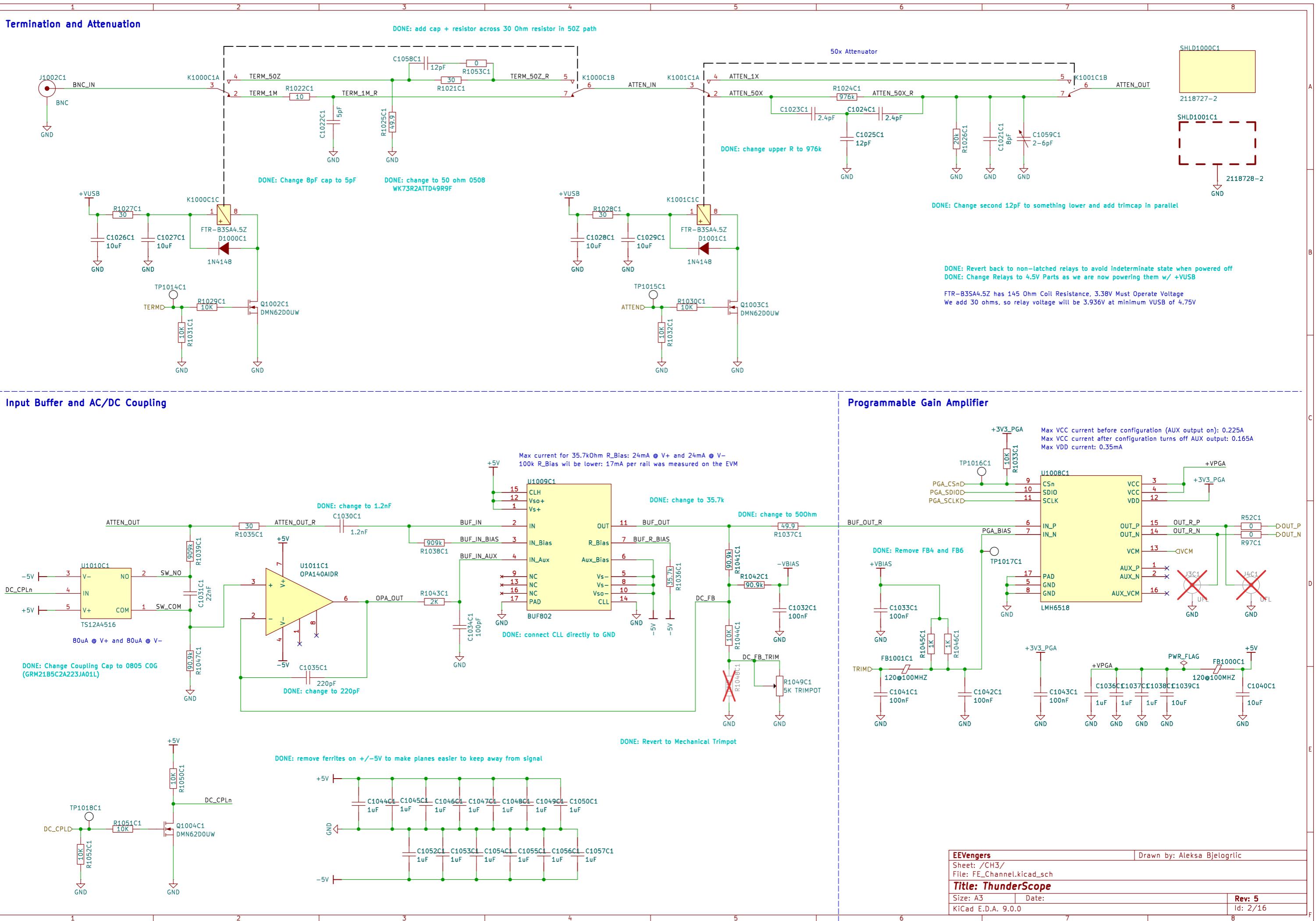


DONE: Revert to Mechanical Trimpot

DONE: remove ferrites on $\pm 5V$ to make planes easier to keep away from signal lines.

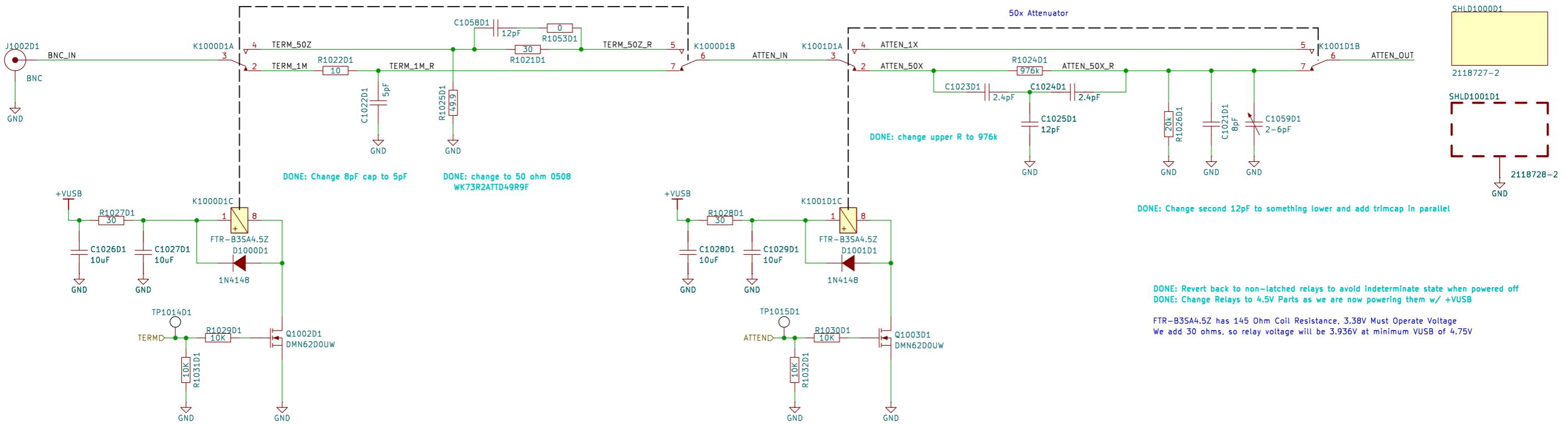


EEVengers	Drawn by: Aleksa Bjelogrlic
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Title: ThunderScope	
Size: A3	Date:
KiCad E.D.A. 9.0.0	Rev: 5 Id: 2/16



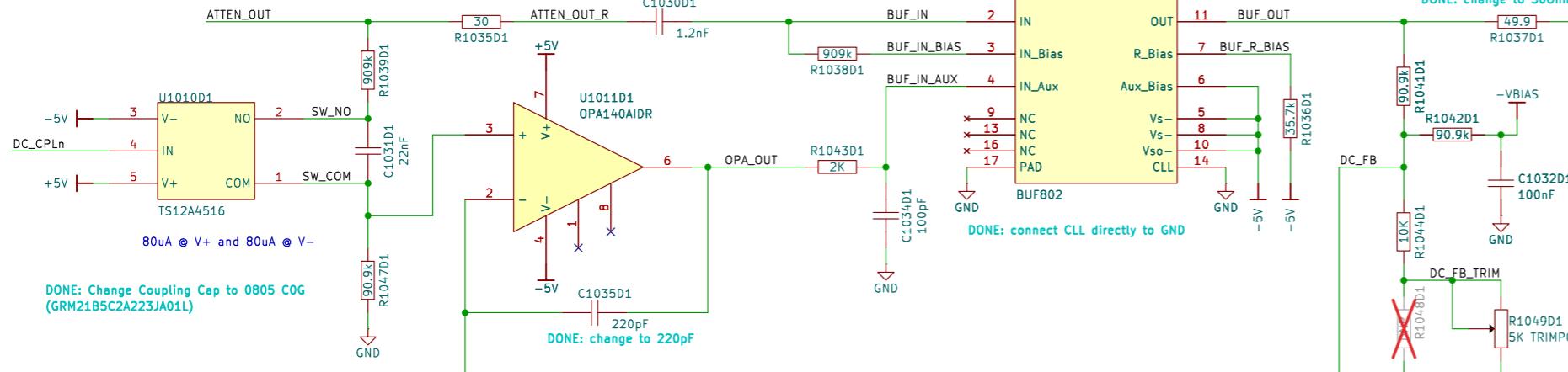
Termination and Attenuation

DONE: add cap + resistor across 30 Ohm resistor in 50Z path



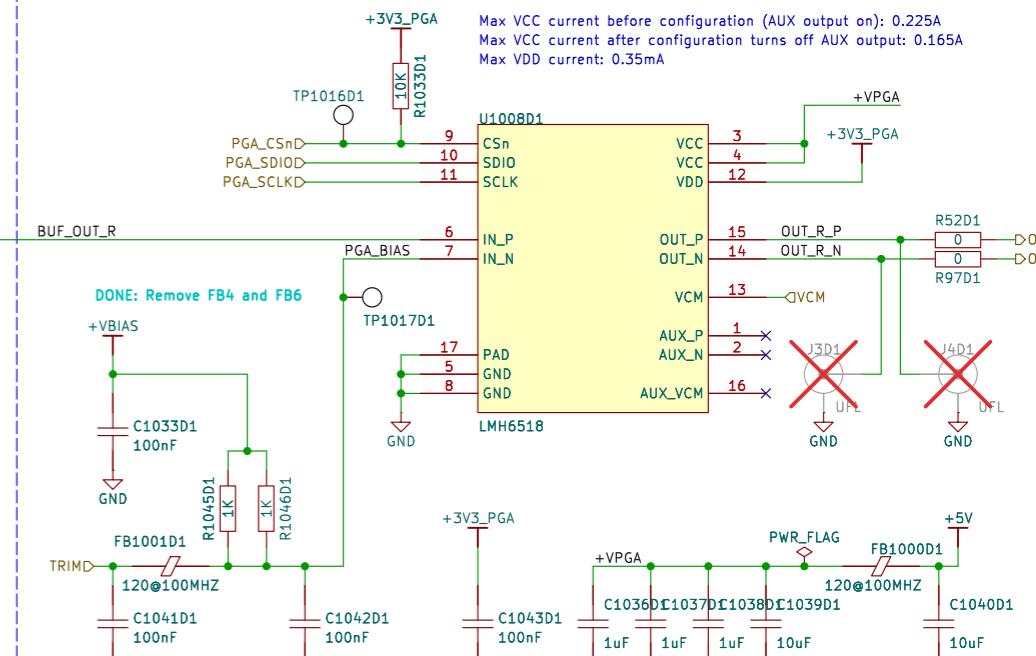
Input Buffer and AC/DC Coupling

Max current for 35.7kOhm R_Bias: 24mA @ V+ and 24mA @ V-
100k R_Bias will be lower: 17mA per rail was measured on the EV



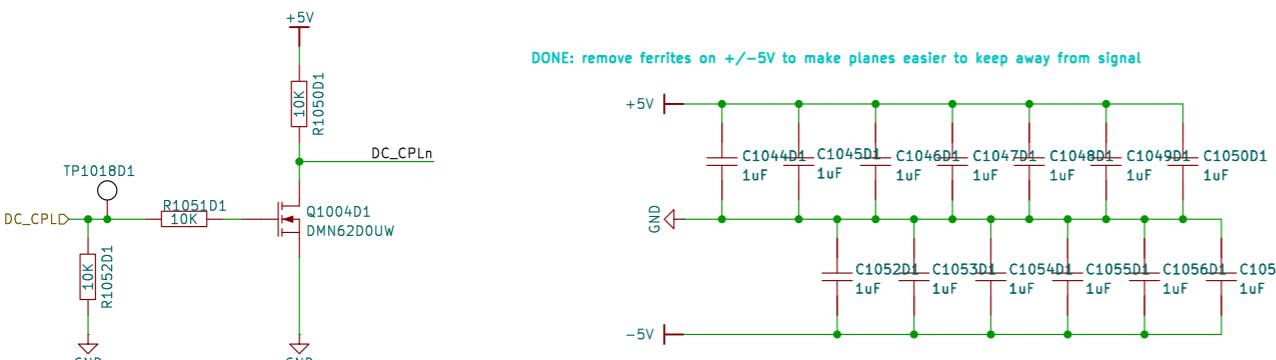
Programmable Gain Amplifier

Max VCC current before configuration (AUX output on): 0.225A
Max VCC current after configuration turns off AUX output: 0.165A
Max VDD current: 0.35mA



DONE: Revert to Mechanical Trimpot

DONE: remove ferrites on +/-5V to make planes easier to keep away from sign



EEVengers

Sheet: /CH4/

File: FE_Channel.kicad_sch

Title: ThunderScope

| Drawn by: Aleksa Bielogarlic

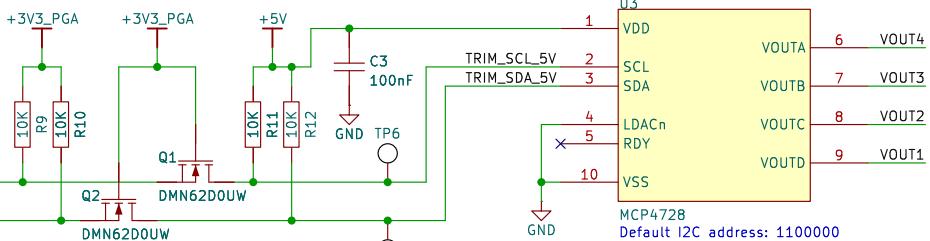
Drawn by: Aleksa Djelic

Digitized by srujanika@gmail.com

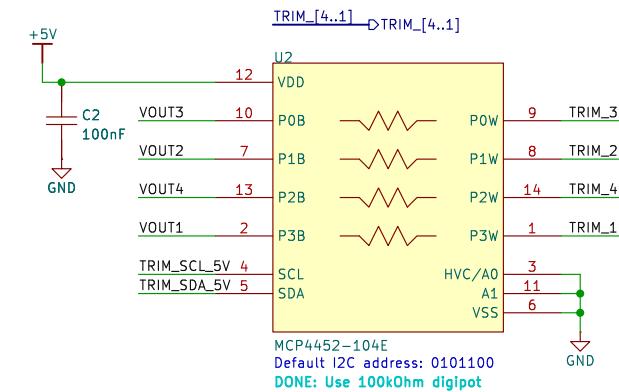
1 2 3 4 5 6

Offset Voltage Trim and User Offset Control

A

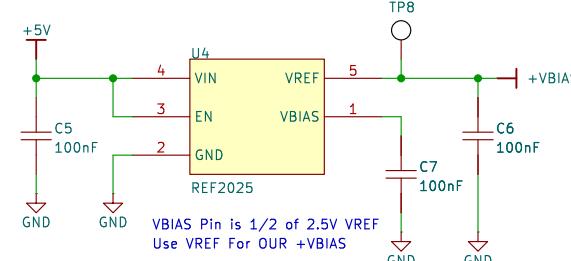


B



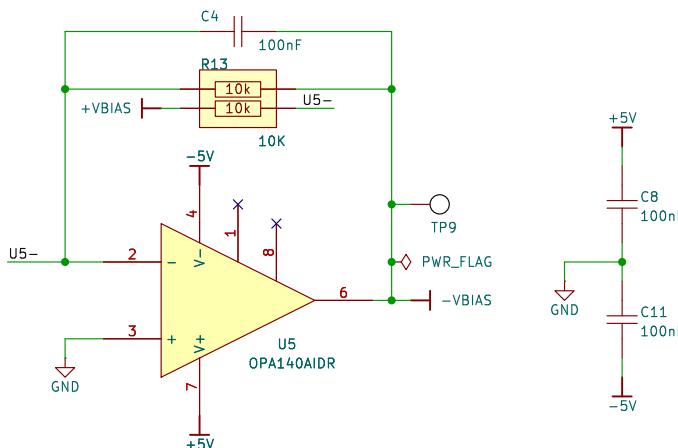
Bias Voltage Generation

C



D

Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140
 -Max resistance is $(575/4 // 10k) = 141.7 \text{ Ohm}$
 -Worst case current is 17.64mA
 -Use REF2025, has max current of 20mA
 -Change U5 divider to matched resistor network
 -ACASN1002S1002P1AT



EEVengers

Sheet: /Front End Trim and Bias/
 File: FE.kicad_sch

Title: ThunderScope

Size: A4 Date:

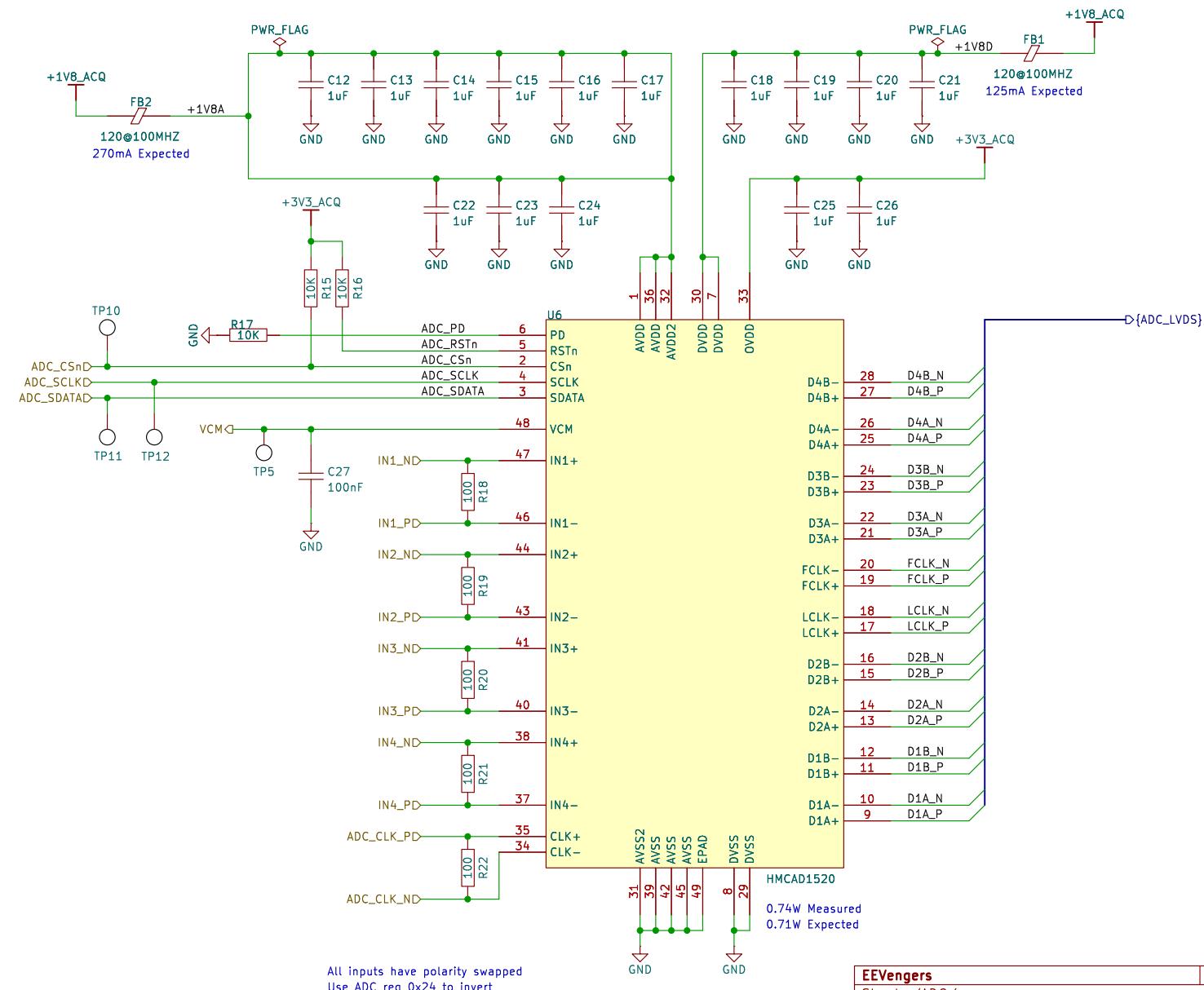
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 Id: 3/16

1 2 3 4 5 6

1 2 3 4 5 6

ADC

EEVengers

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Sheet: /ADC/
File: ADC.kicad_sch**Title: ThunderScope**

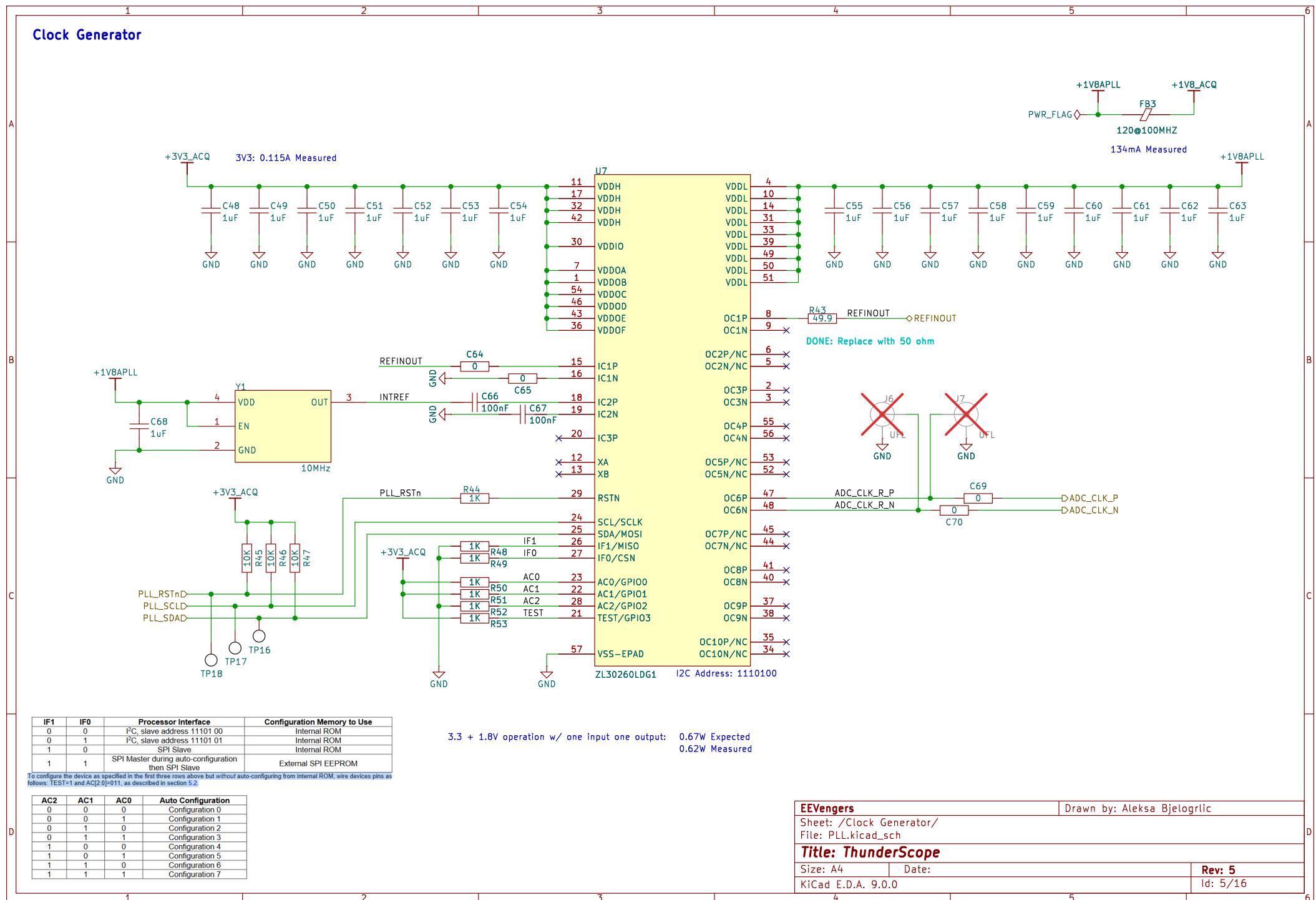
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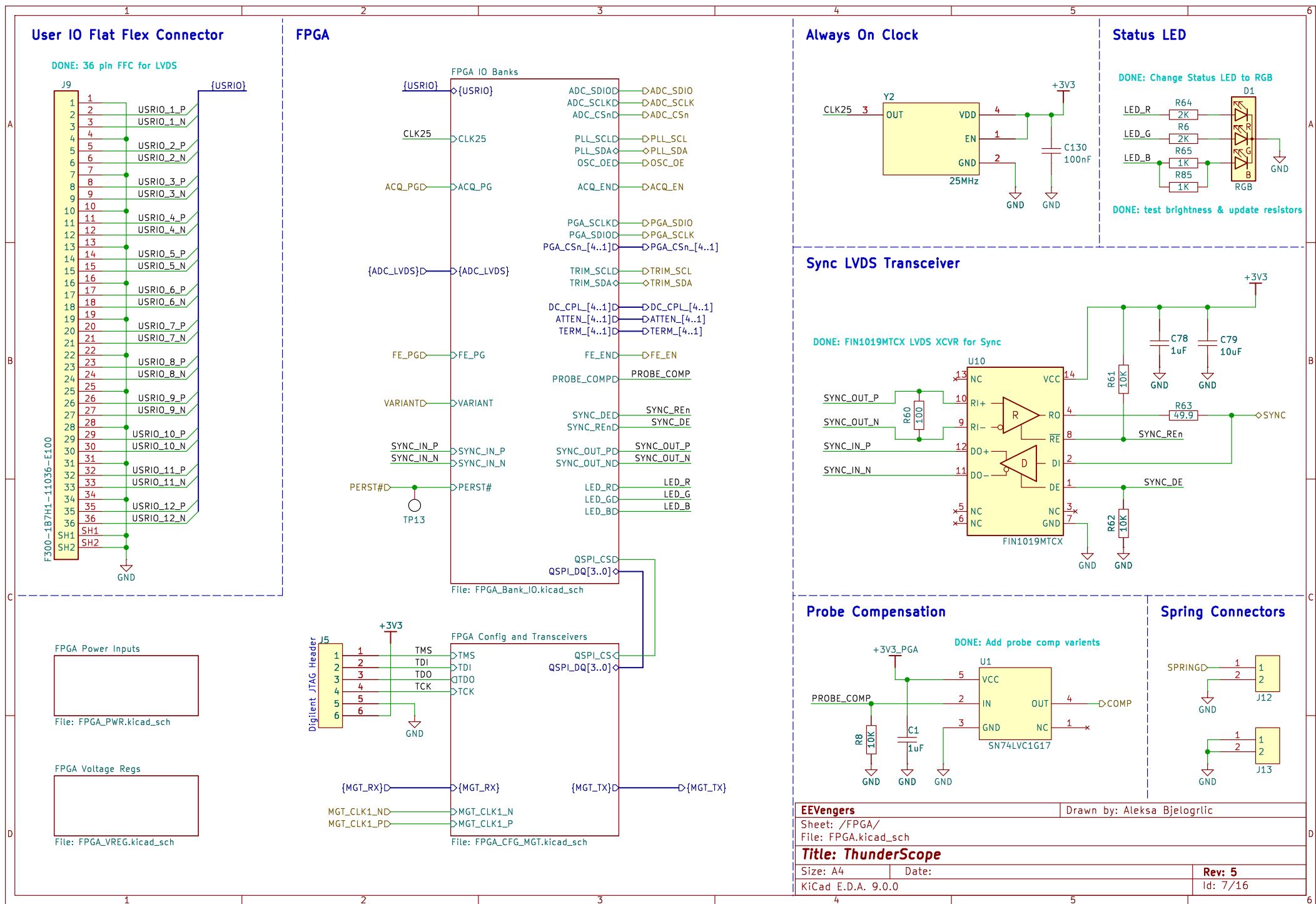
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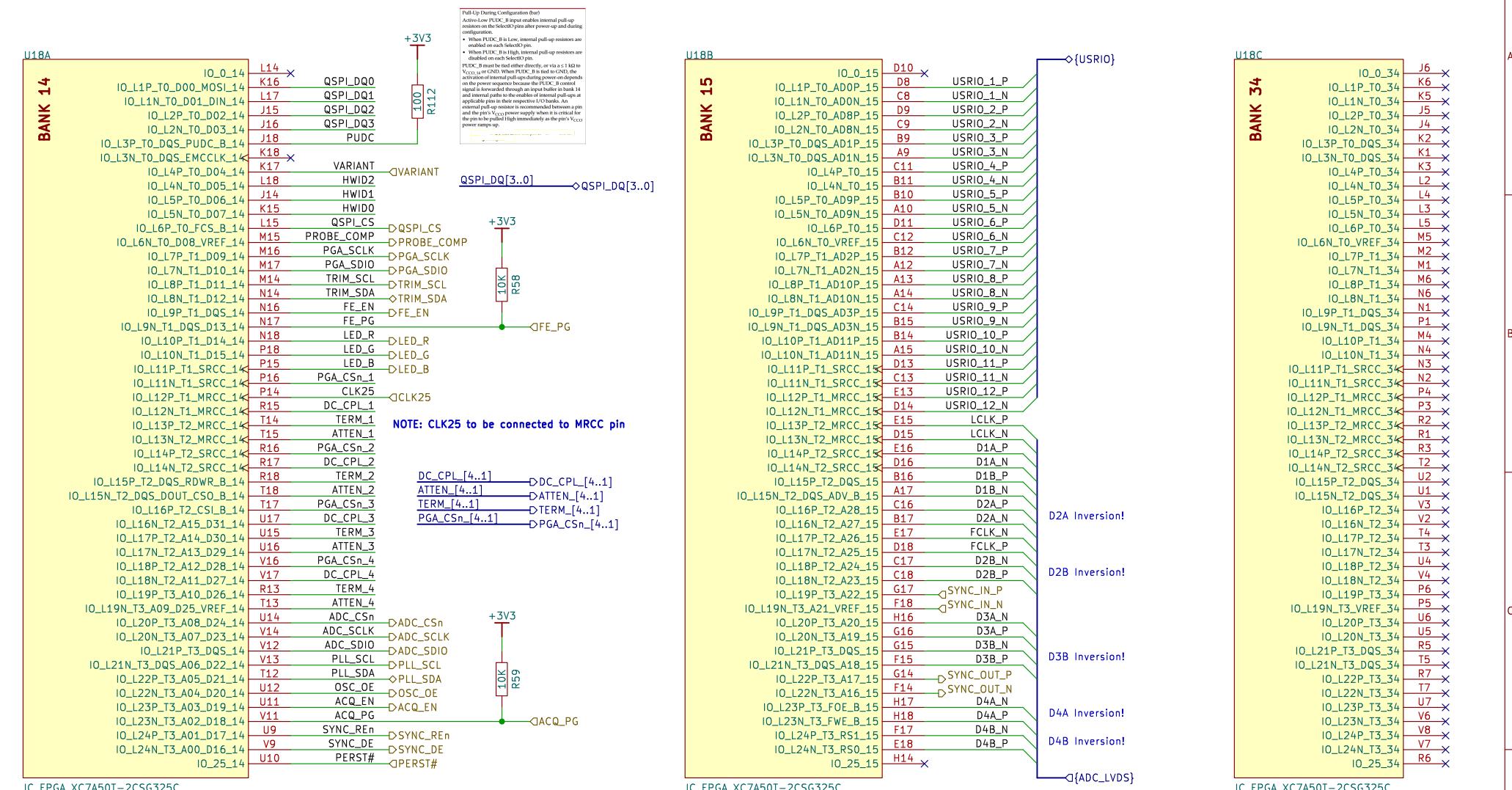
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1 2 3 4 5 6





FPGA IO Banks



EEVengers

Sheet: /FPGA/FPGA IO Banks/
File: FPGA_Bank_IO.kicad_sch

Drawn by: Aleksa Bjelogrlic

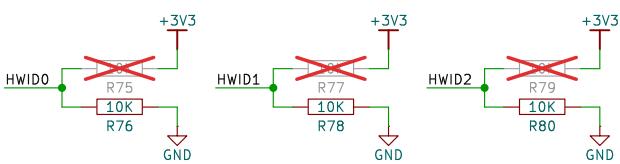
Title: ThunderScope

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Rev: 5

Id: 8/16



FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

Note: DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

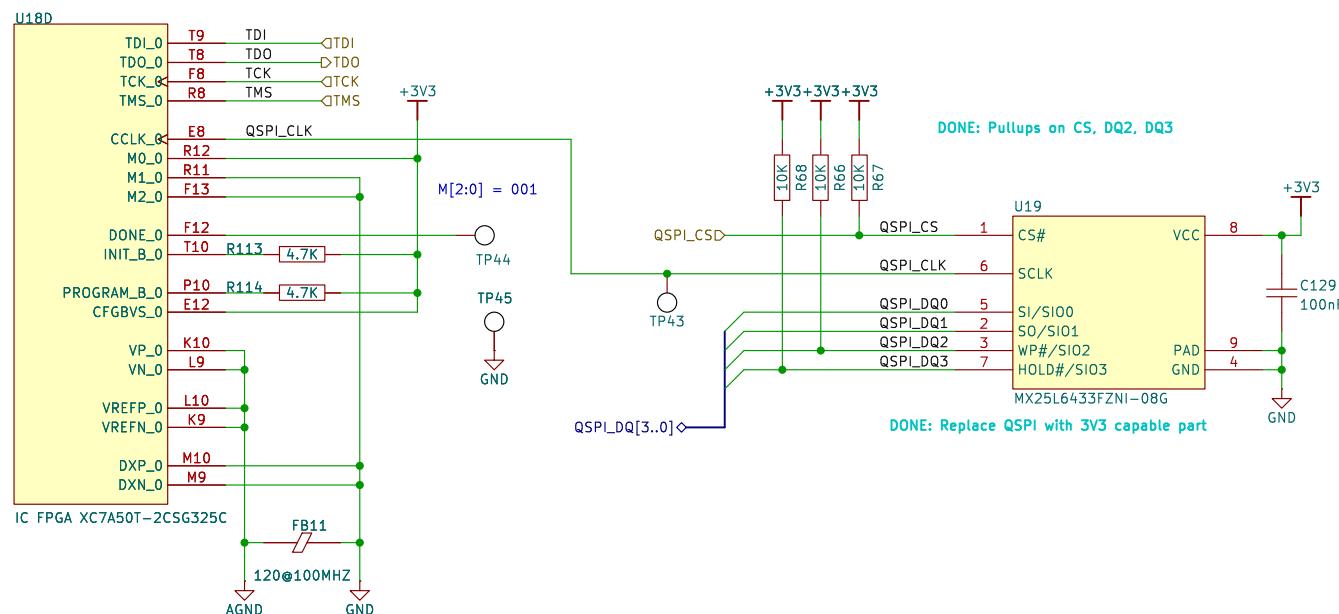
Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and

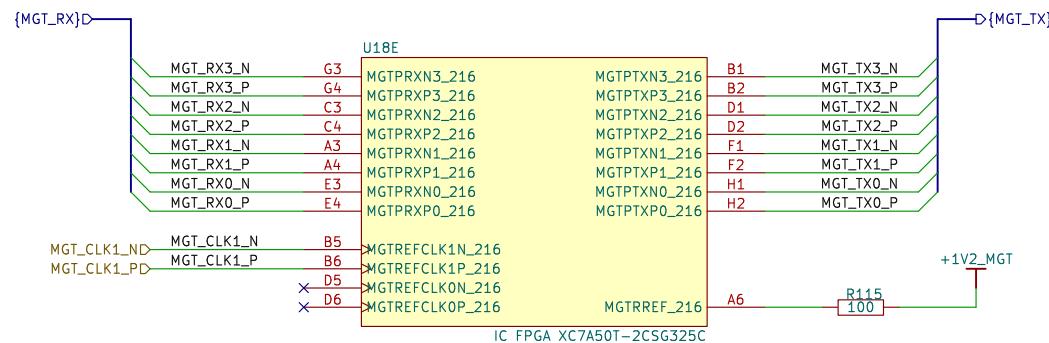
Table 2-1: 7 Series FPGA Configuration Modes				
Configuration Mode	M2[0]	Bus Width	CCLK Direction	
Master SPI	001	x1, x2, x4	Output	

Table 2-2: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Bank Used	Configuration Interface I/O	HR Bank 0 V _{CCO} 0	HR Bank 14 V _{CCO} 14	HR Bank 15 V _{CCO} 15	CFGBVS	
JTAG (only)	0	VREFP_0	2.5V	2.5V	Any	VCCO_0	
		VREFN_0	1.8V	1.8V	Any	GND	
		DXP_0	2.5V	2.5V	2.5V	VCCO_0	
		DXN_0	1.8V	1.8V	1.8V	GND	
Serial SPI or SelectMAP	0, 14 ⁽¹⁾	VREFP_0	3.3V	3.3V	3.3V	VCCO_0	
		VREFN_0	2.5V	2.5V	2.5V	VCCO_0	
		DXP_0	2.5V	2.5V	2.5V	VCCO_0	
		DXN_0	1.8V	1.8V	1.8V	GND	
		BPI ⁽²⁾	3.3V	3.3V	3.3V	VCCO_0	
BPI ⁽²⁾	0, 14, 15	VREFP_0	2.5V	2.5V	2.5V	VCCO_0	
		VREFN_0	1.8V	1.8V	1.8V	GND	
		DXP_0	3.3V	3.3V	3.3V	VCCO_0	
		DXN_0	2.5V	2.5V	2.5V	VCCO_0	
		BPI ⁽²⁾	1.8V	1.8V	1.8V	GND	
Notes:							
1. RS232 for Multiflash or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.							
2. BPI mode is not available in the Spartan-7 family.							



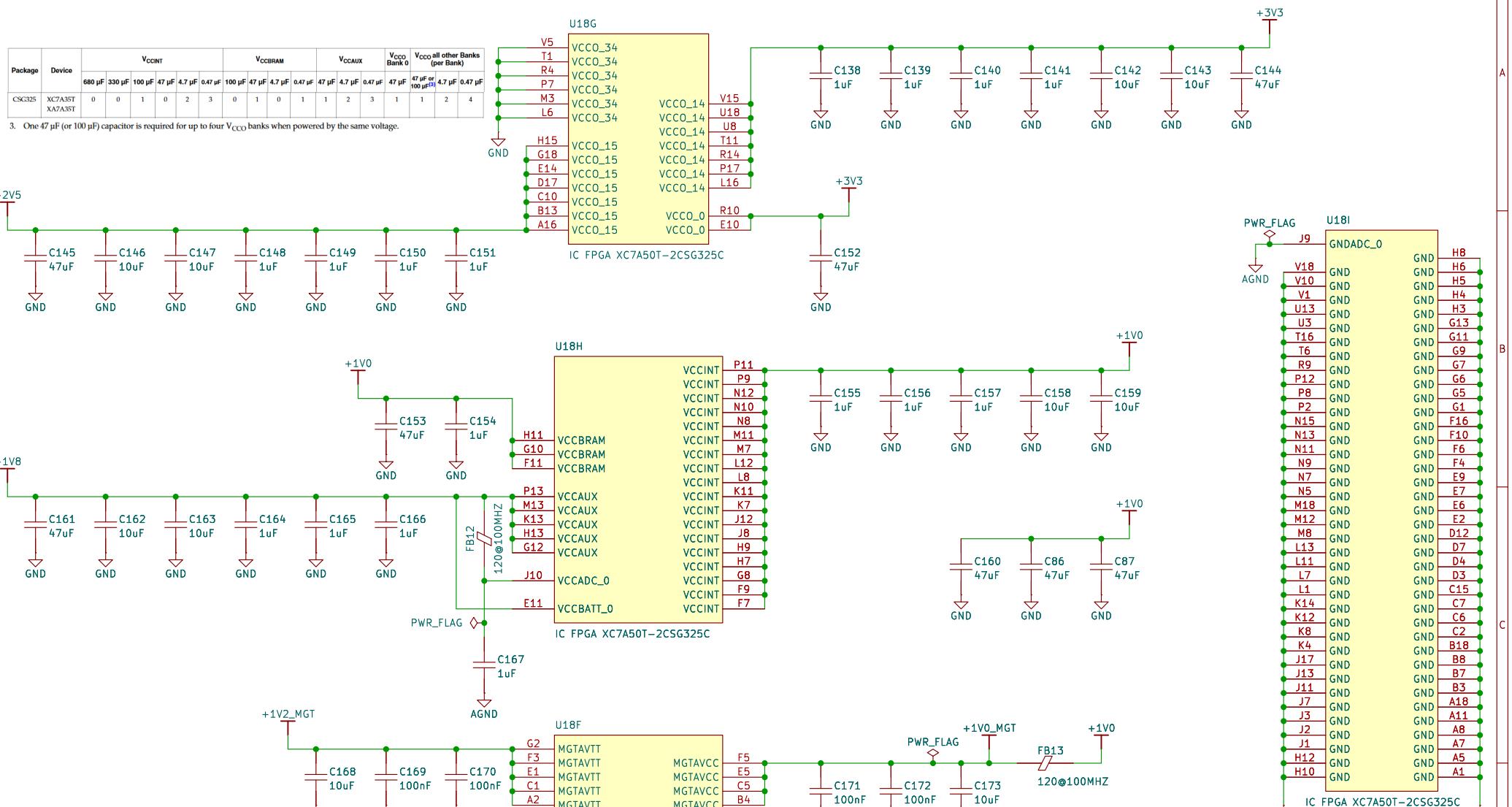
FPGA Transceivers



FPGA Power Inputs

Package	Device	V _{CCINT}				V _{CCBRAM}				V _{CCAUX}				V _{CCO} Bank 0	V _{CCO} all other Banks (per Bank)			
		680 µF	330 µF	100 µF	47 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF			
CSC325	XC7A35T XA7A35T	0	0	1	0	2	3	0	1	0	1	1	2	3	1	1	2	4

One 47 μ F (or 100 μ F) capacitor is required for up to four V_{CCO} banks when powered by the same voltage.



Capacitor	Package Pins			Value
	MGTAVCC	MGTAVTT	GND	
Cap1		F3	F4	
Cap2		A2	A1	
Cap3	B4		B3	
Cap4	F5		F6	
				0.1 μ F

Qty/Power Supply Group		Capacitance (μ F)	Tolerance	Type
MGTAVCC	MGTAVTT			
1	1	4.7	10%	Ceramic
2	2	0.1	10%	Ceramic

FFVenners

Sheet: /FPGA/FPGA Power Inputs,
File: FPGA_PWR.kicad_sch

Title: ThunderScope

Size: A4 Date:

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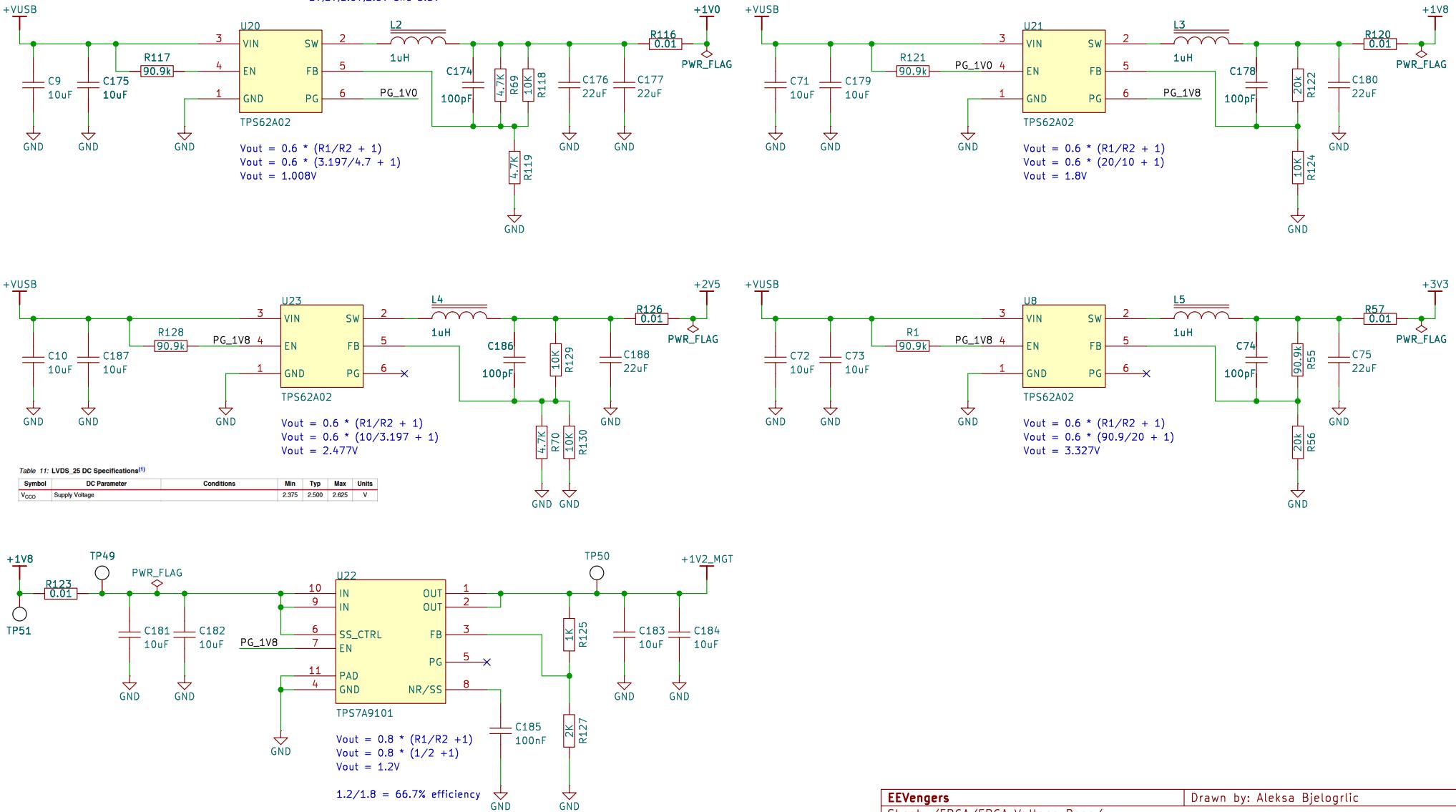
10 of 10

Rev: 5

1 2 3 4 5 6

FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V



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Sheet: /FPGA/FPGA Voltage Regs/
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Title: ThunderScope

Size: A4 Date:

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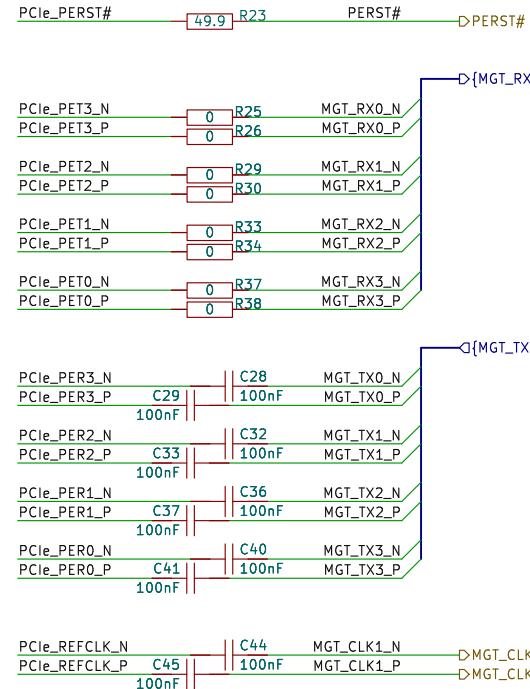
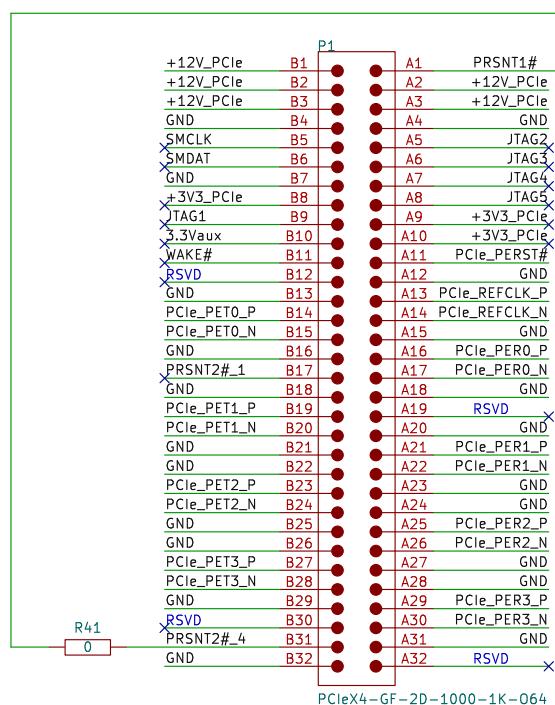
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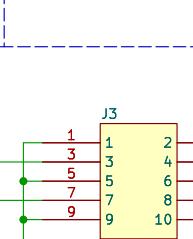
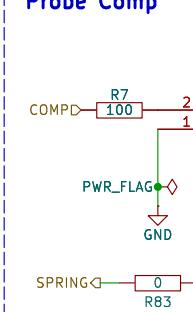
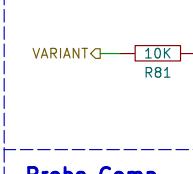
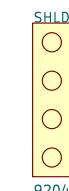
1 2 3 4 5 6

1 2 3 4 5 6

PCIe x4 Edge Connector



PCIe bracket



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Size: A4 Date:

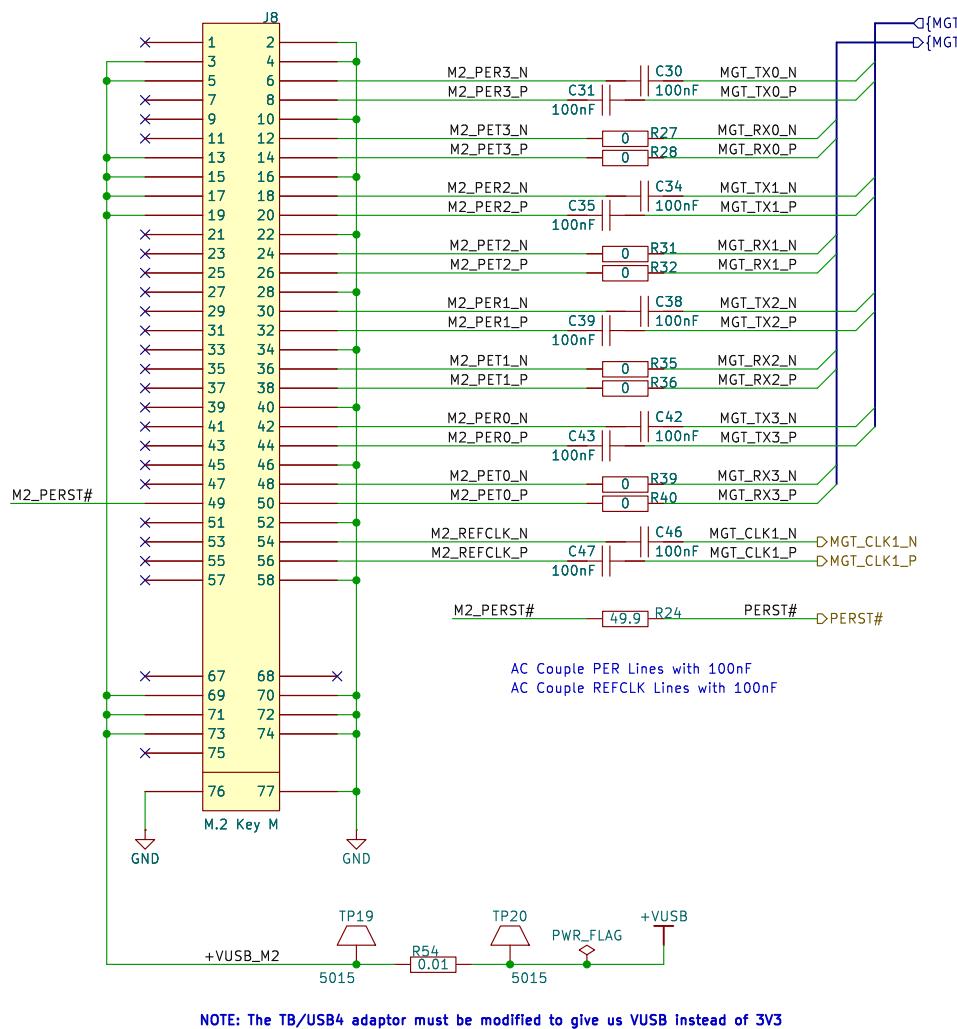
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Rev: 5

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M.2 Key M Connector – Custom Pinout



Probe Comp

COMPD → R84 → SPRING

Fan Connector

+VUSB → R84 → J10 → SPRING → GND
009155002852006

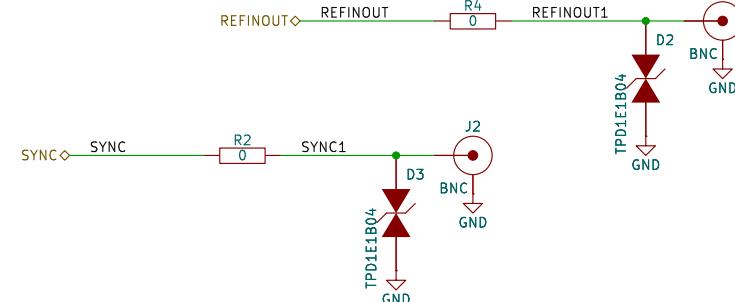
Ground Lug

J11 → 7793 → GND

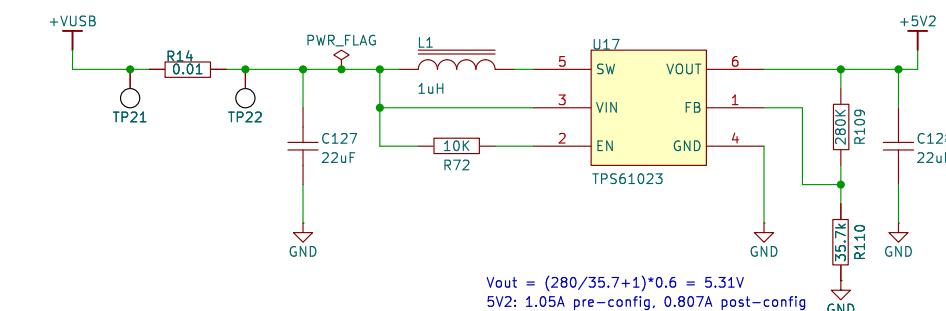
Variant Pin Strap

VARIANT → R82 → +3V3

Refclock and Sync BNCs



5V2 Boost Converter



Interposer Standoffs



EEVengers

Sheet: /TS-USB4 Components/
File: M2_KEY_M.kicad_sch

Title: ThunderScope

Size: A4 Date:

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Rev: 5

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