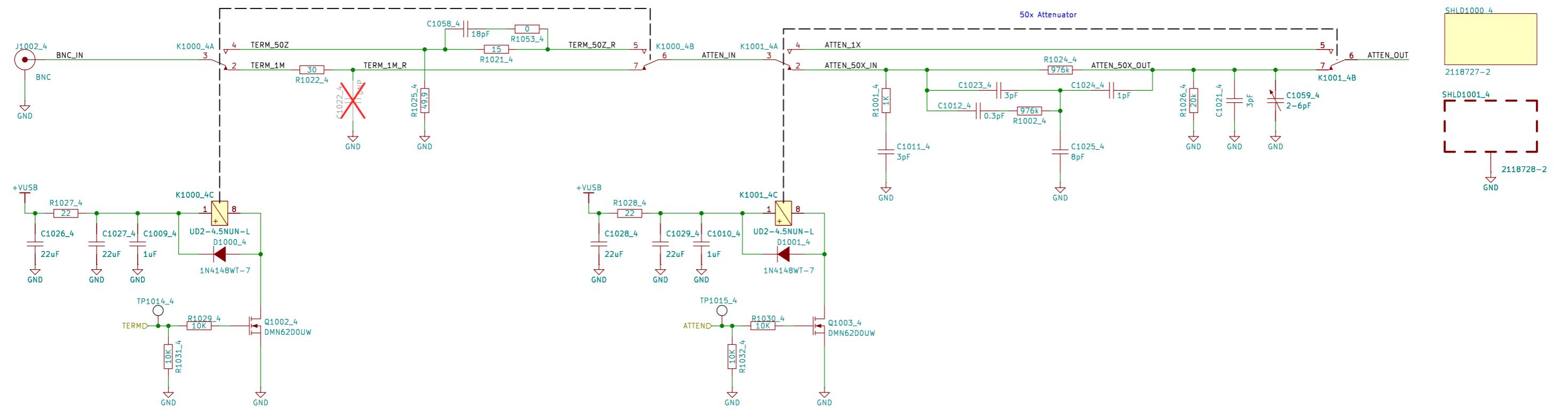


Termination and Attenuation



Input Buffer and AC/DC Coupling

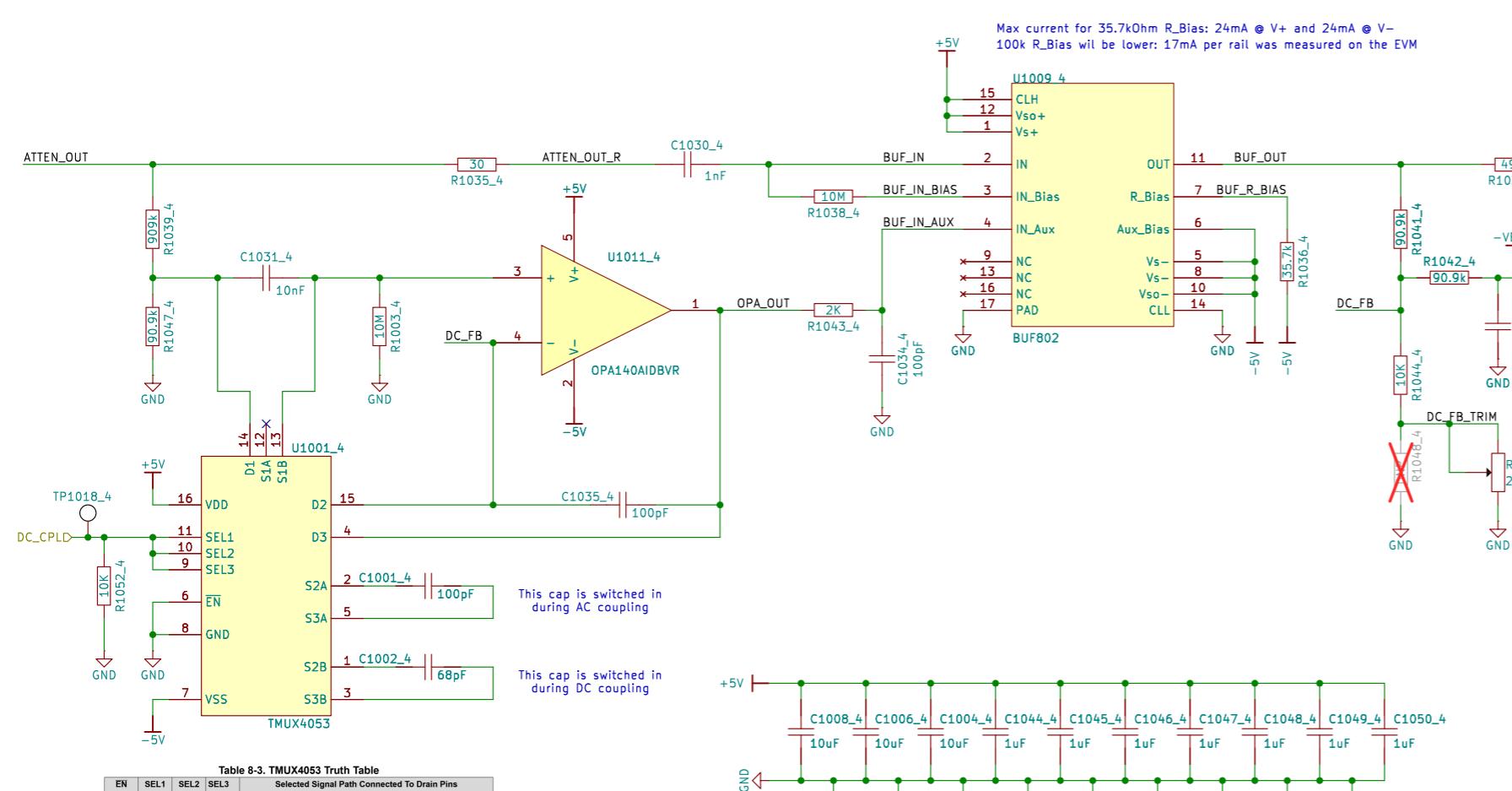
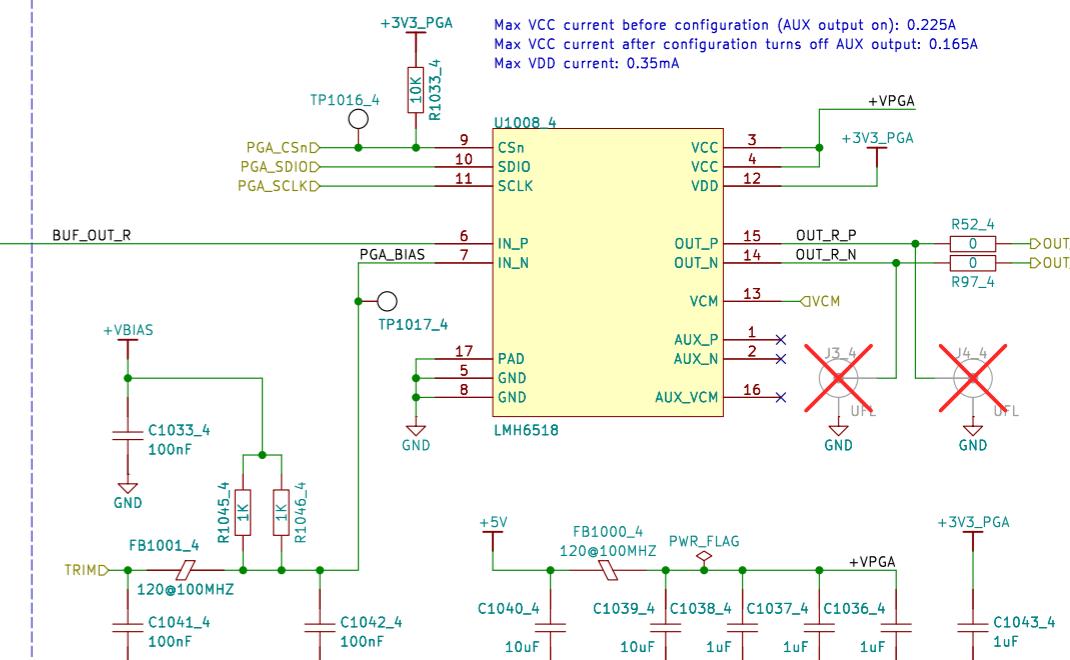
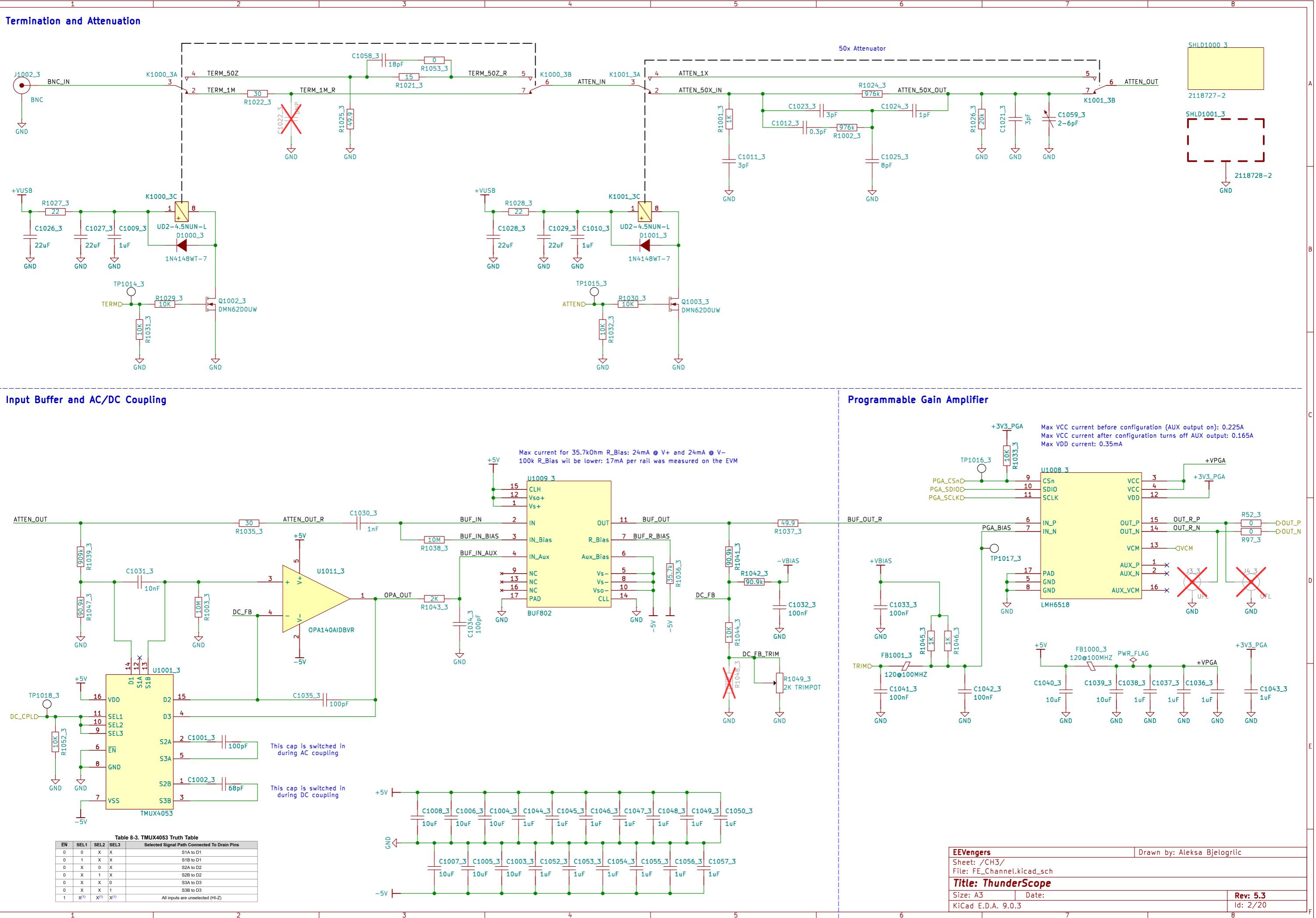
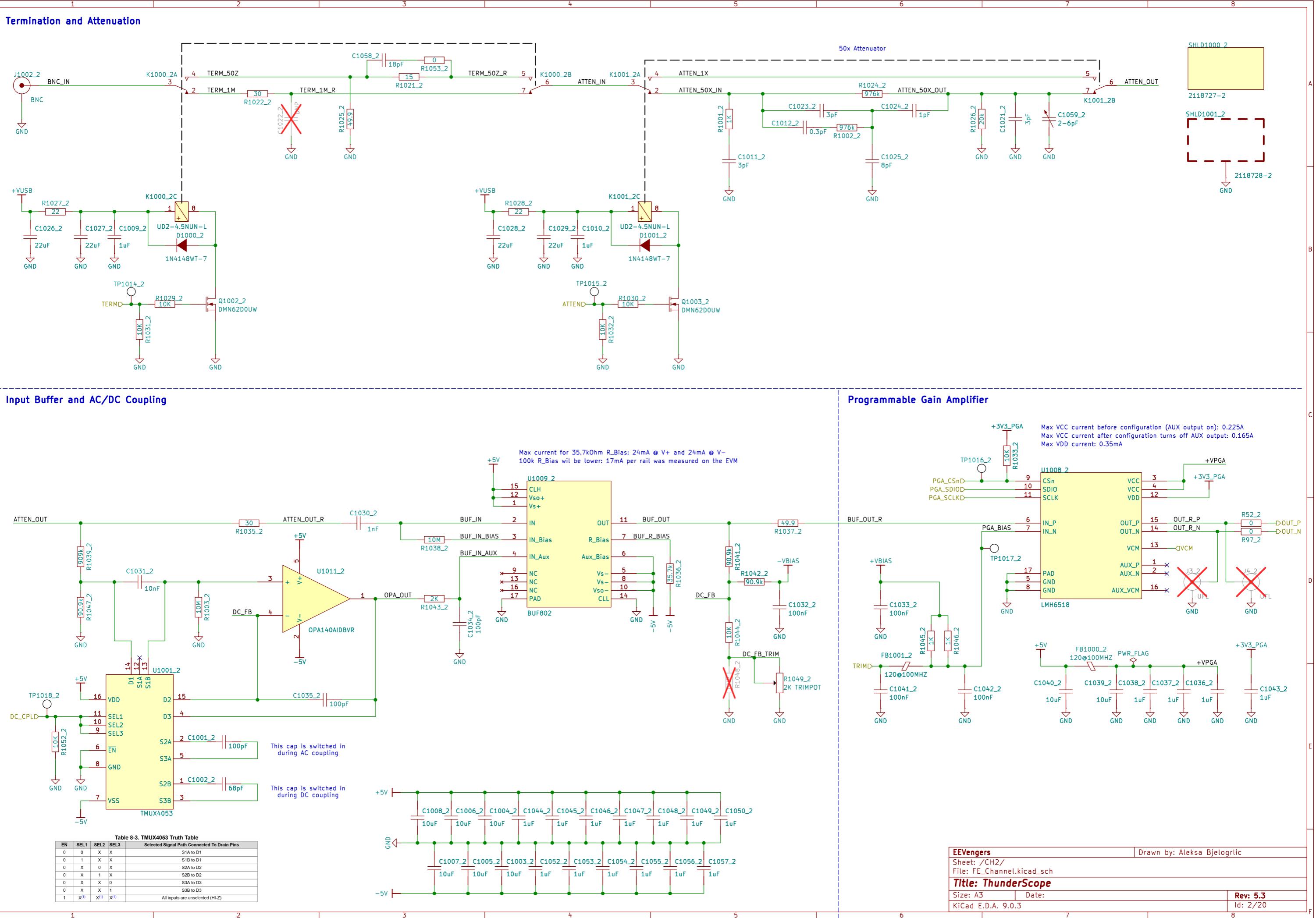


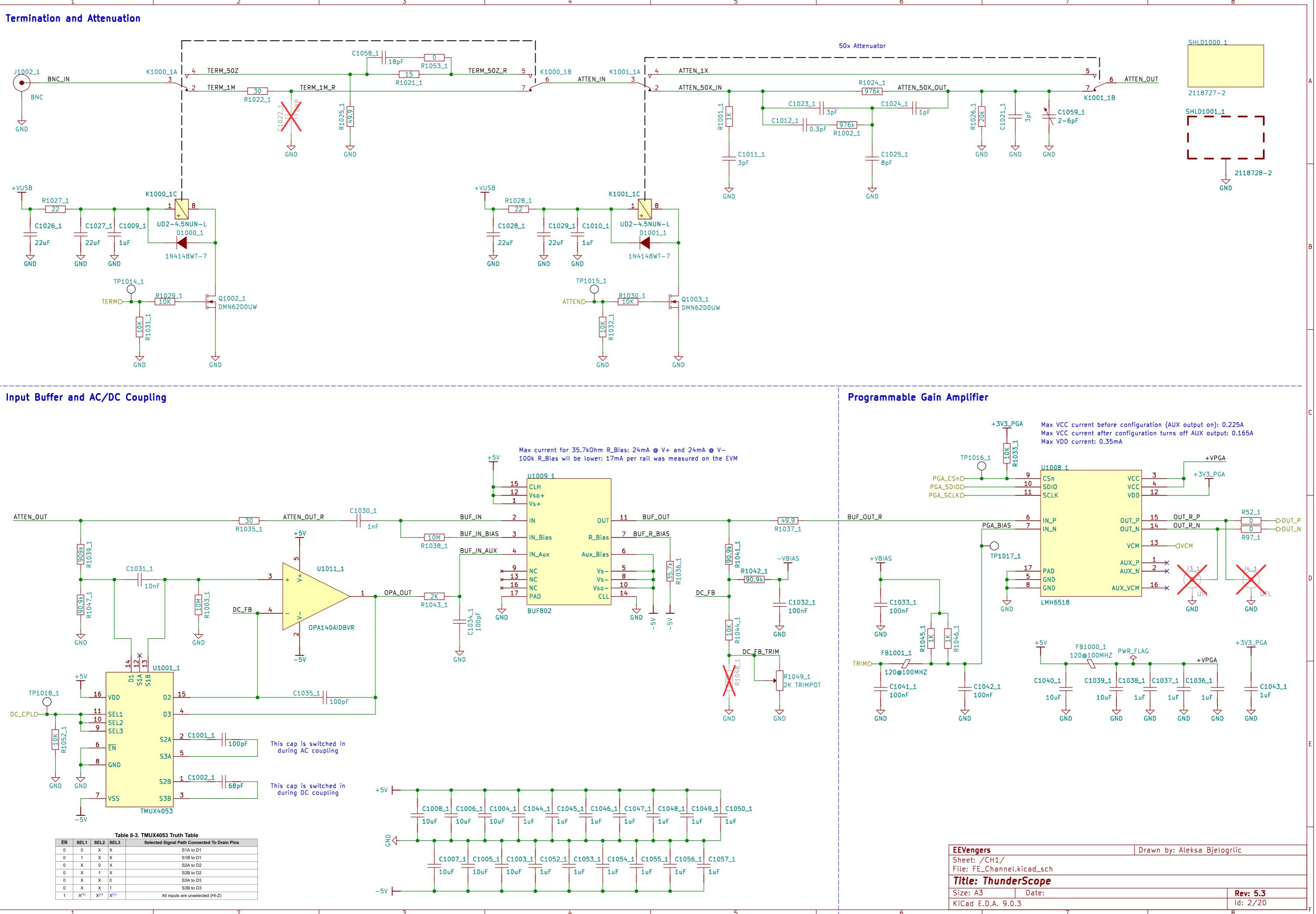
Table 8-3. TMUX4053 Truth Table				
EN	SEL1	SEL2	SEL3	Selected Signal Path Connected To Drain Pins
0	0	X	X	S1A to D1
0	1	X	X	S1B to D1
0	X	0	X	S2A to D2
0	X	1	X	S2B to D2
0	X	X	0	S3A to D3
0	X	X	1	S3B to D3
1	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	All inputs are unselected (Hi-Z)

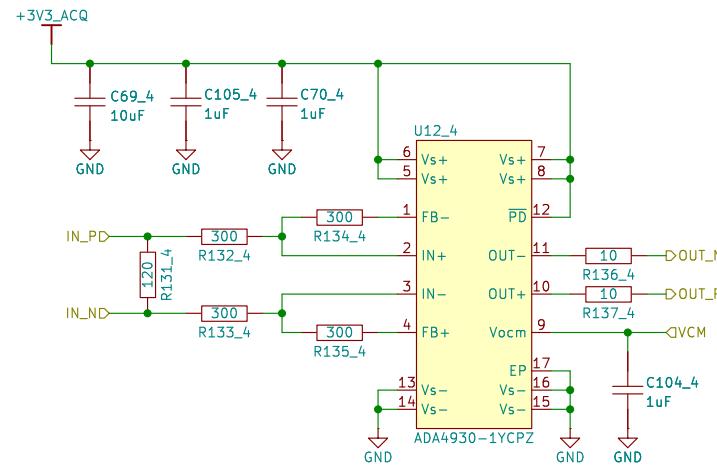


H4/
channel.kicad_sch
thunderScope
Date:
A 0.3







ADC Driver**EEVengers**

Sheet: /ADC Driver 4/
File: ADC_Driver.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 9.0.3

Drawn by: Aleksa Bjelogrlic

Rev: 5.3
Id: 3/20

ADC Driver

A

B

C

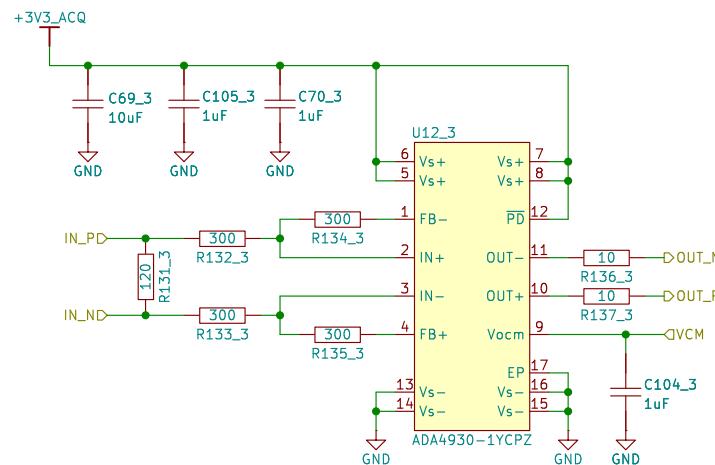
D

A

B

C

D



EEVengers	Drawn by: Aleksa Bjelogrlic
Sheet: /ADC Driver 3/ File: ADC_Driver.kicad_sch	D
Title: ThunderScope	
Size: A4	Date:
KiCad E.D.A. 9.0.3	Rev: 5.3 Id: 3/20

ADC Driver

A

A

B

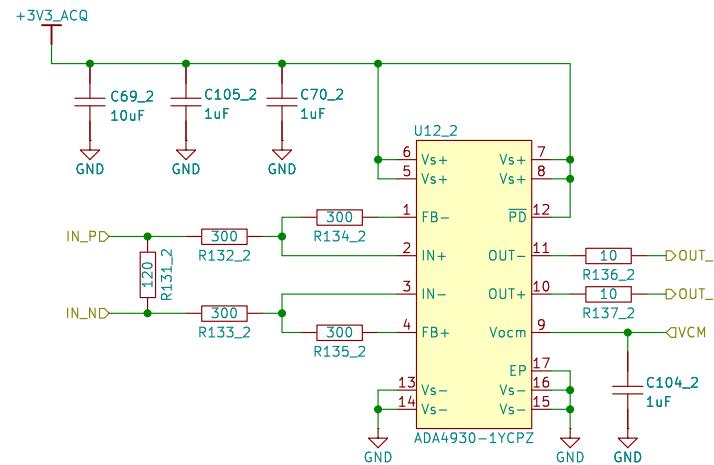
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C

C

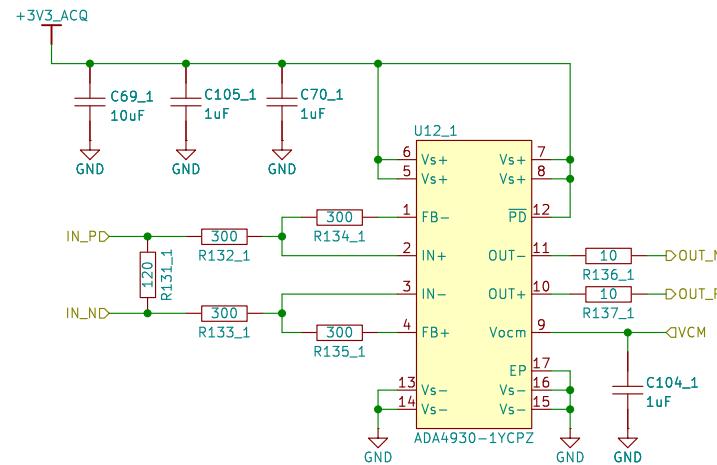
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D

**EEVengers**

Drawn by: Aleksa Bjelogrlic

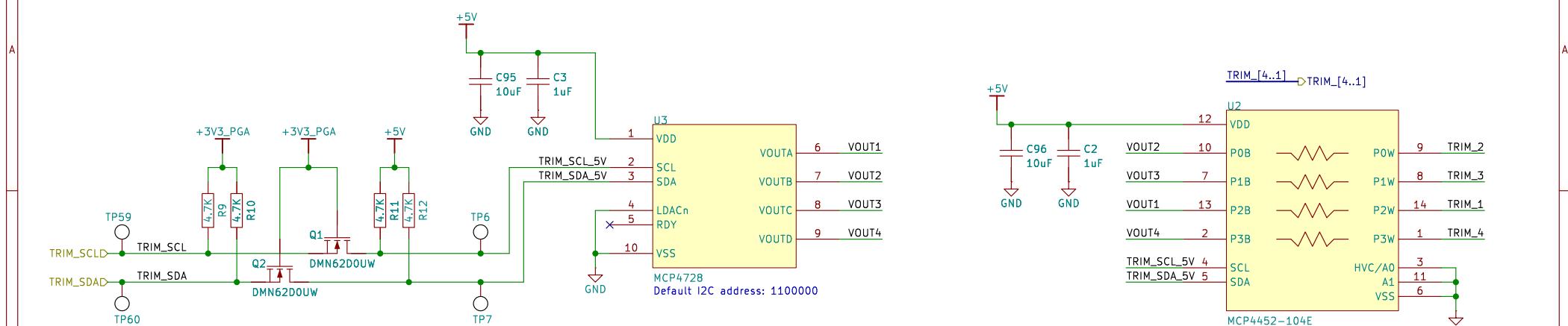
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File: ADC_Driver.kicad_sch**Title: ThunderScope**Size: A4 Date:
KiCad E.D.A. 9.0.3Rev: 5.3
Id: 3/20

ADC Driver**EEVengers**Sheet: /ADC Driver 1/
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KiCad E.D.A. 9.0.3

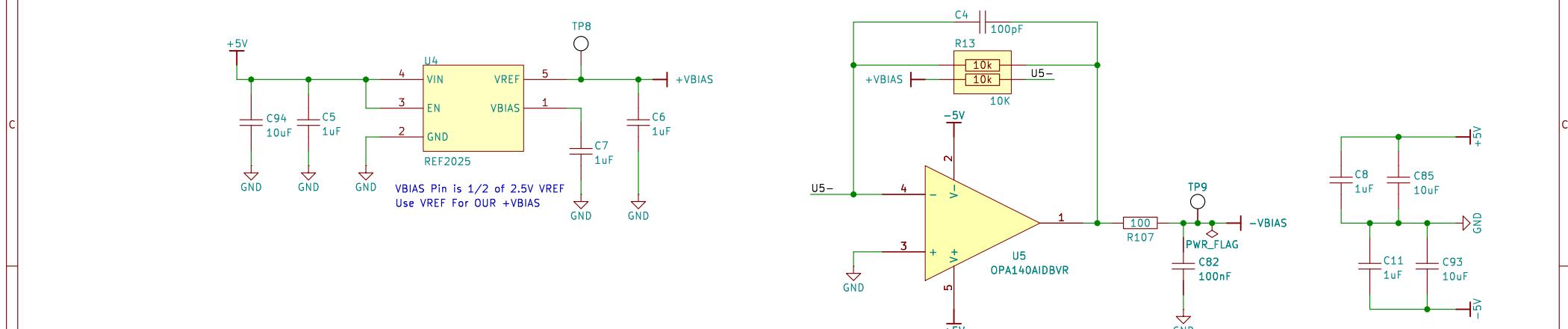
Drawn by: Aleksa Bjelogrlic

Rev: 5.3
Id: 3/20

Offset Voltage Trim and User Offset Control



Bias Voltage Generation



FFVenner

Sheet: /Front End Trim and Bias/
File: FE.kicad_sch

Title: ThunderScope

Size: A4

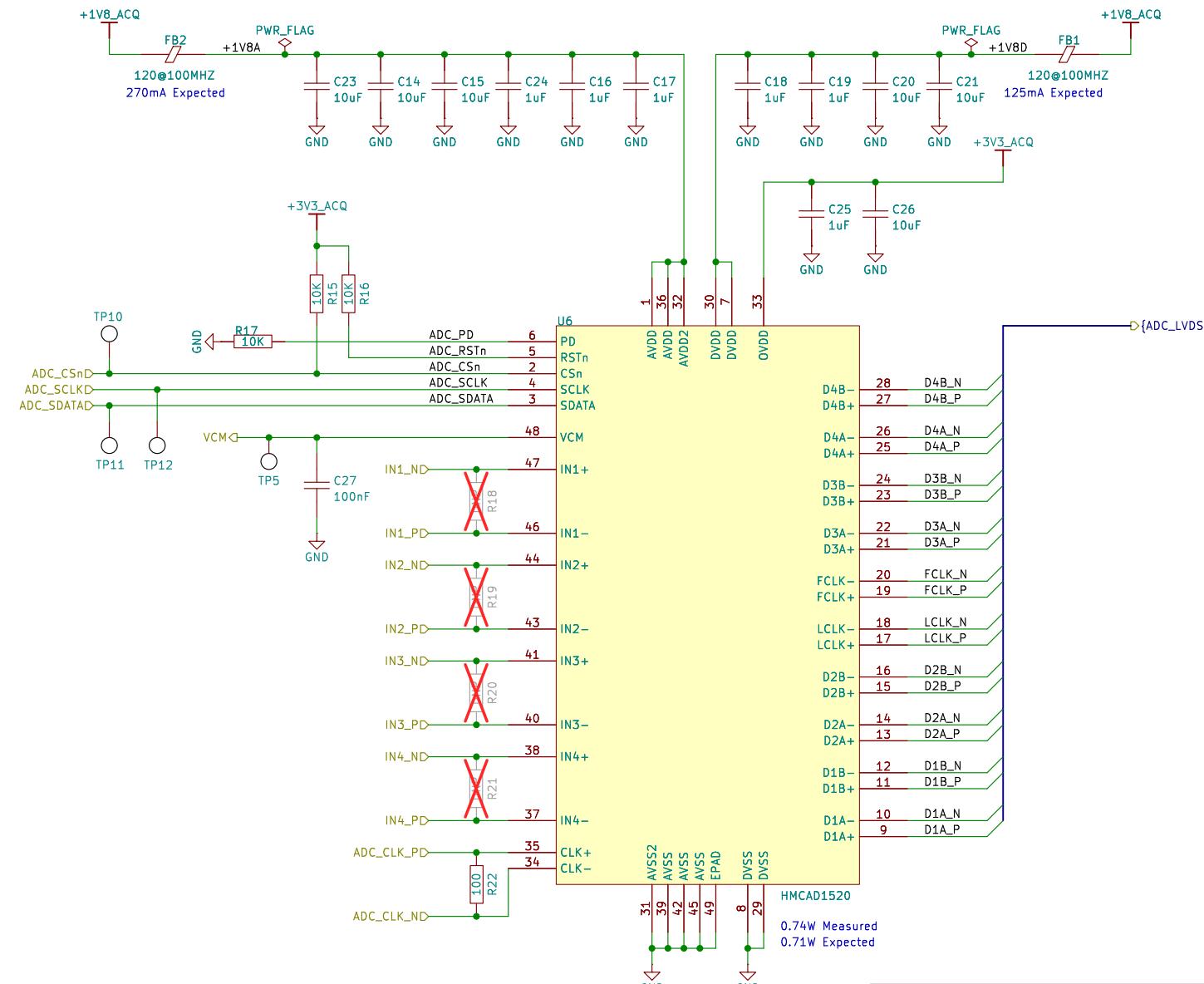
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Rev: 5.3

d: 4/20

1 2 3 4 5 6

ADC

EEVengers

Sheet: /ADC/
File: ADC.kicad_sch

Drawn by: Aleksa Bjelogrlic

Title: ThunderScope

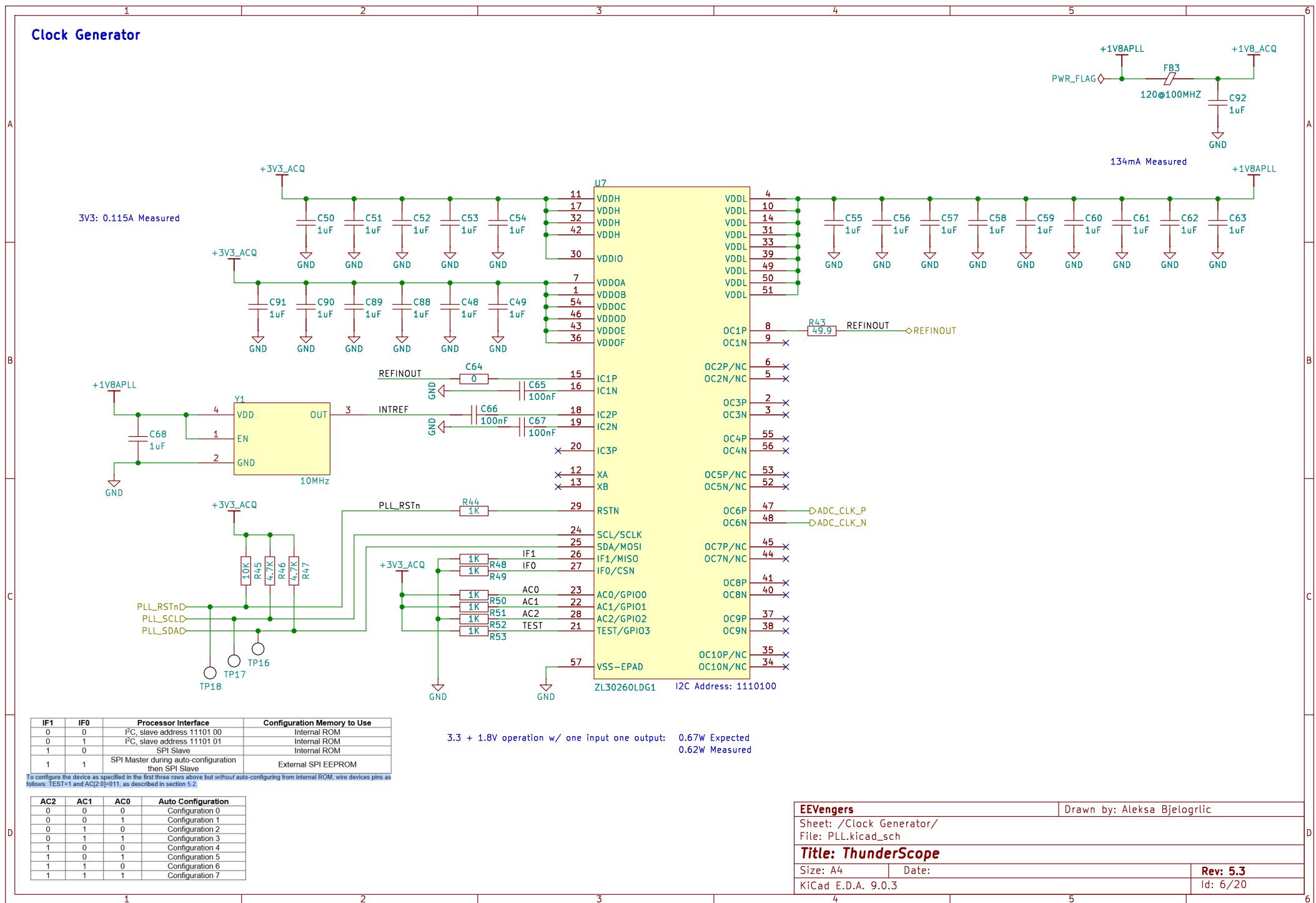
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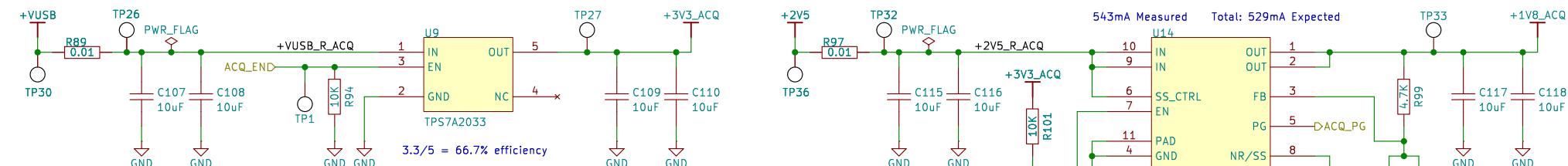
Rev: 5.3

Id: 5/20

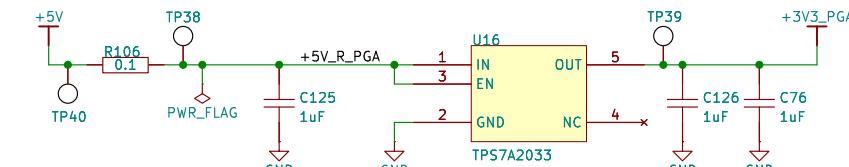
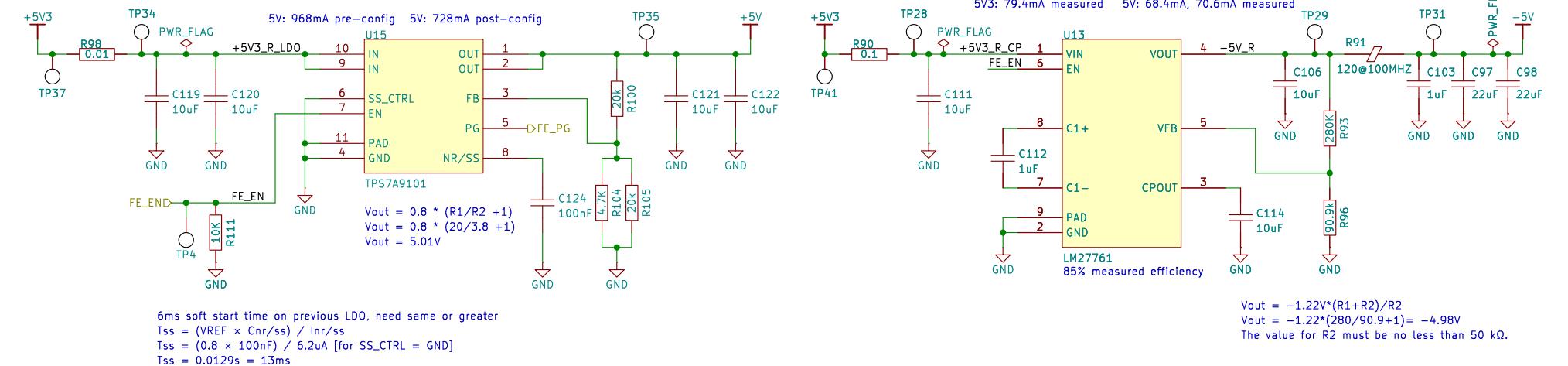
1 2 3 4 5 6



Acquisition Voltage Regulators



Front End Voltage Regulators



EEVblog

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Title: ThunderScope

Size: A4

KiCad E.D.A. 9.0.3

4

Drawn by Alaska Biographics

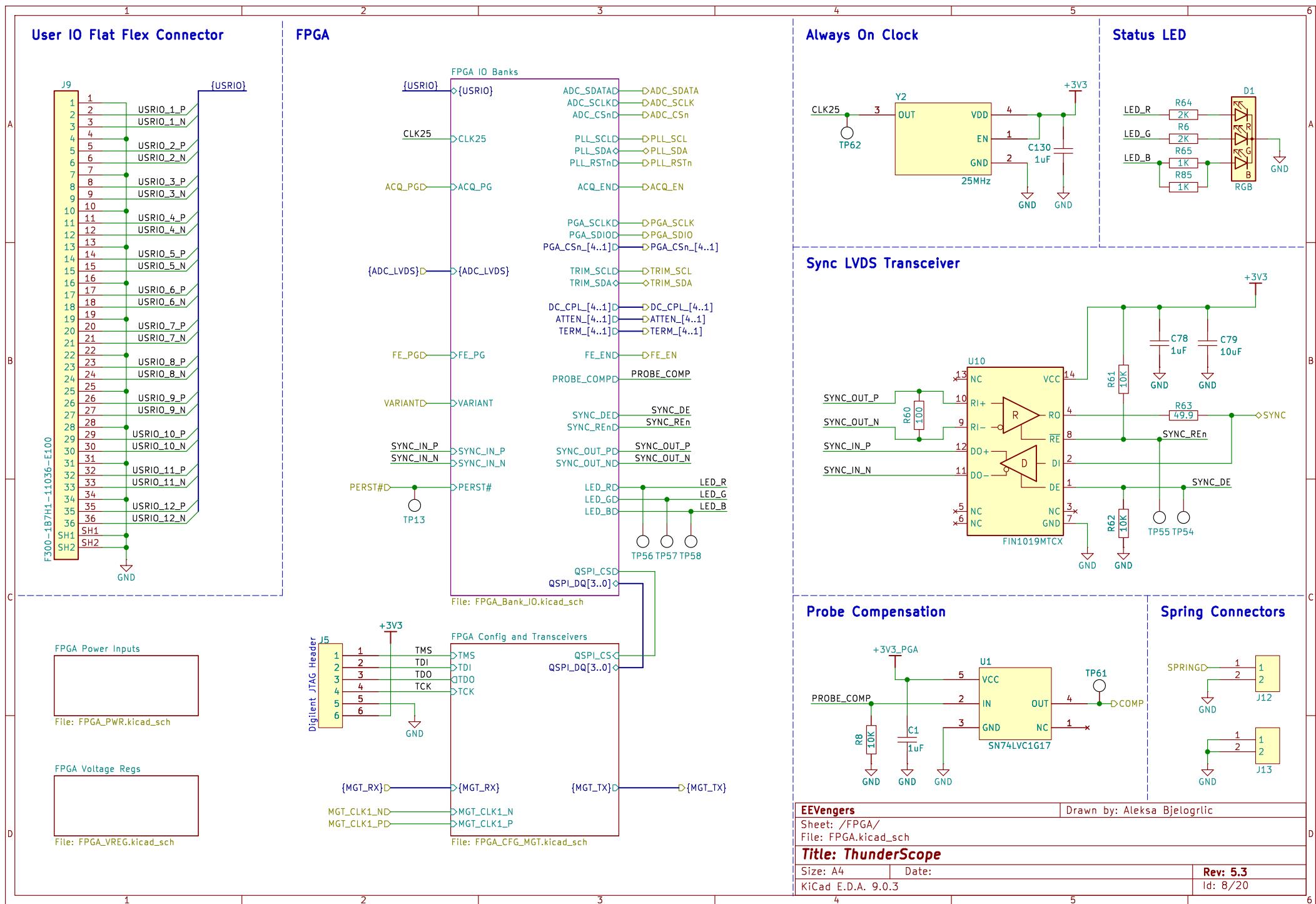
Drawn by: Aleksa Bjelogrlic

1

1

10

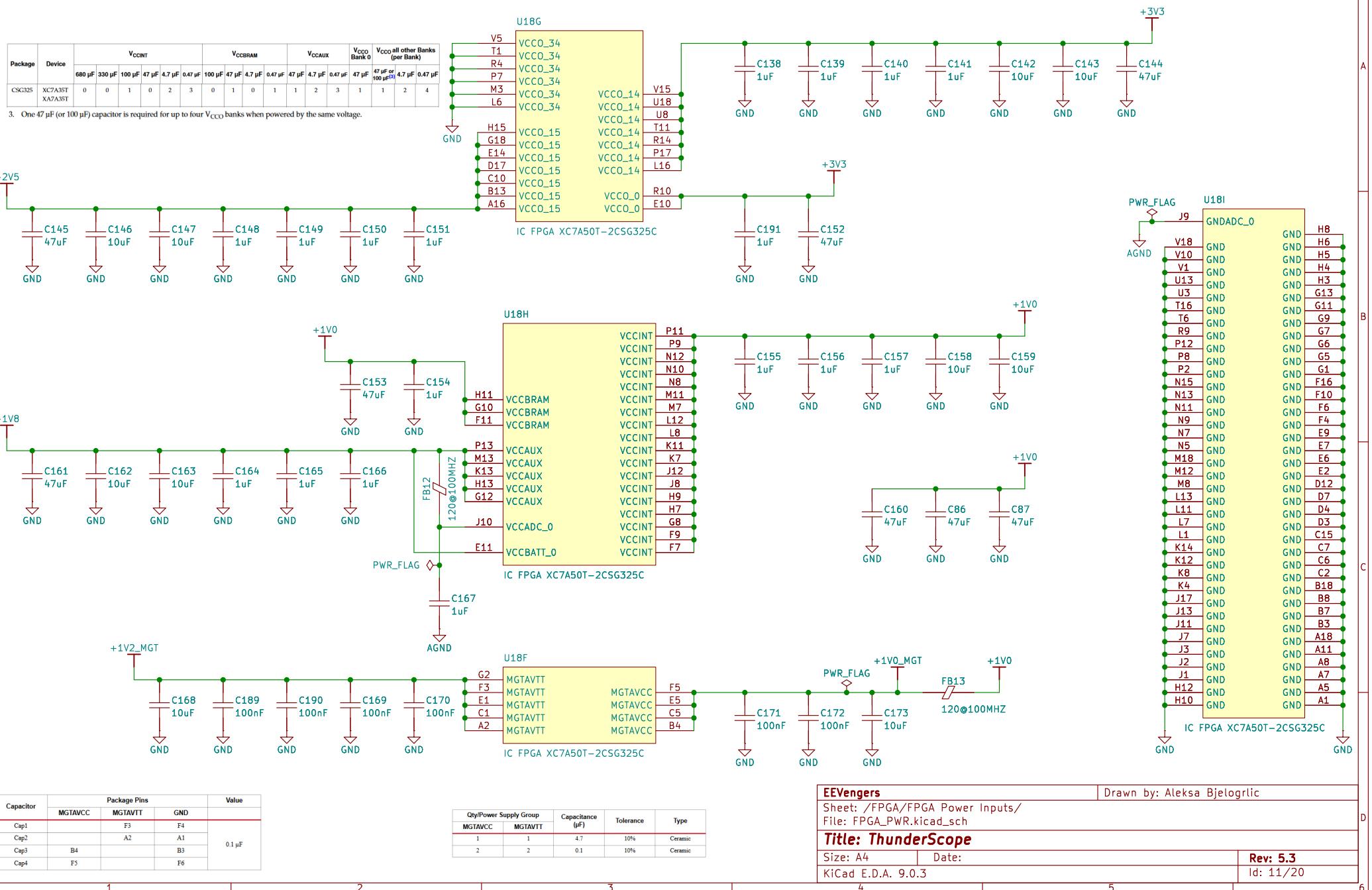
5



FPGA Power Inputs

Package	Device	V _{CCINT}				V _{CCBRAM}				V _{CCAUX}				V _{CCO} Bank 0	V _{CCO} all other Banks (per Bank)			
		680 µF	330 µF	100 µF	47 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF			
CSC325	XC7A35T XA7A35T	0	0	1	0	2	3	0	1	0	1	1	2	3	1	1	2	4

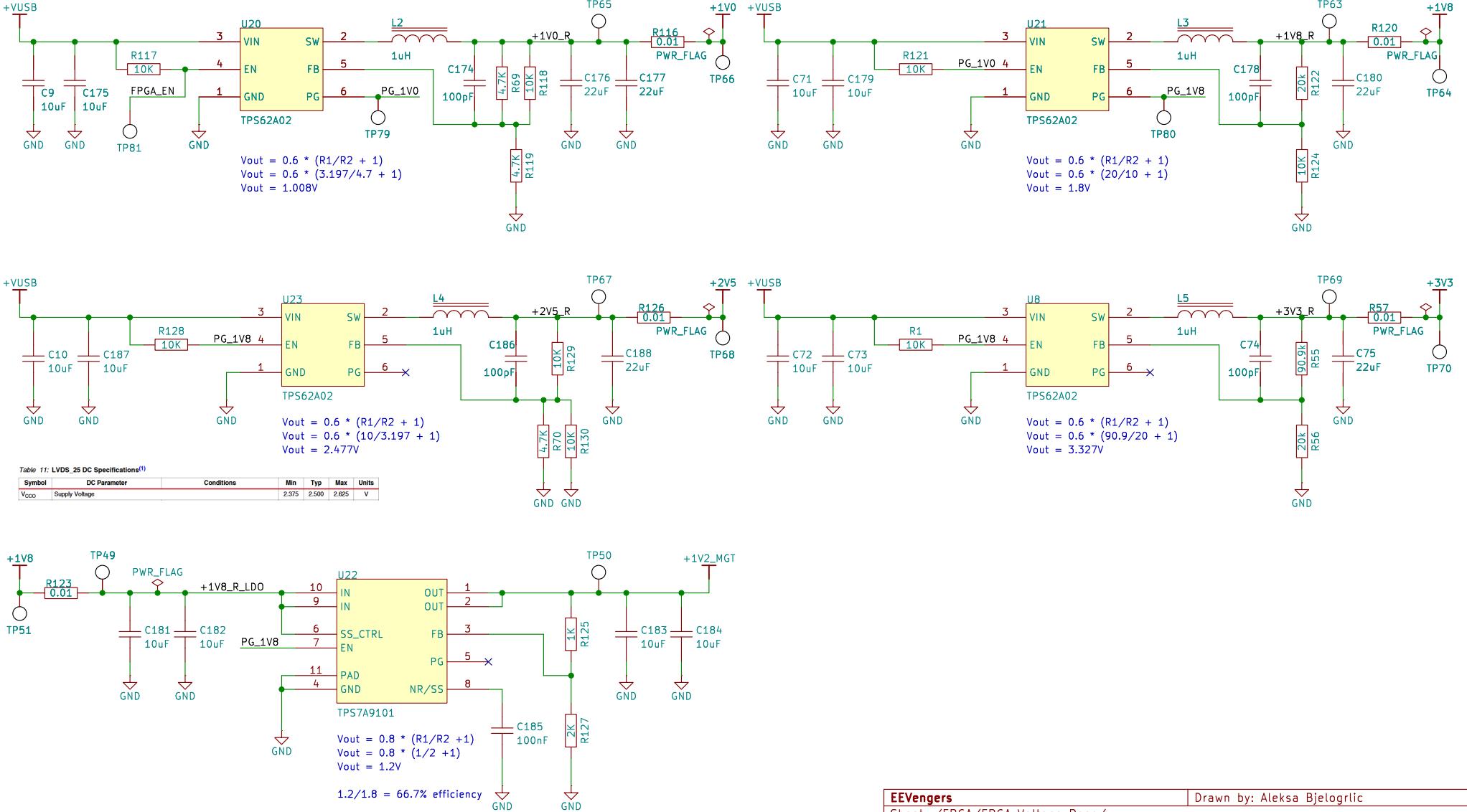
3. One 47 μ F (or 100 μ F) capacitor is required for up to four V_{CC0} banks when powered by the same voltage.



1 2 3 4 5 6

FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V



The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT
1V,1V,1.2V

EEVengers

Sheet: /FPGA/FPGA Voltage Regs/
File: FPGA_VREG.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 9.0.3

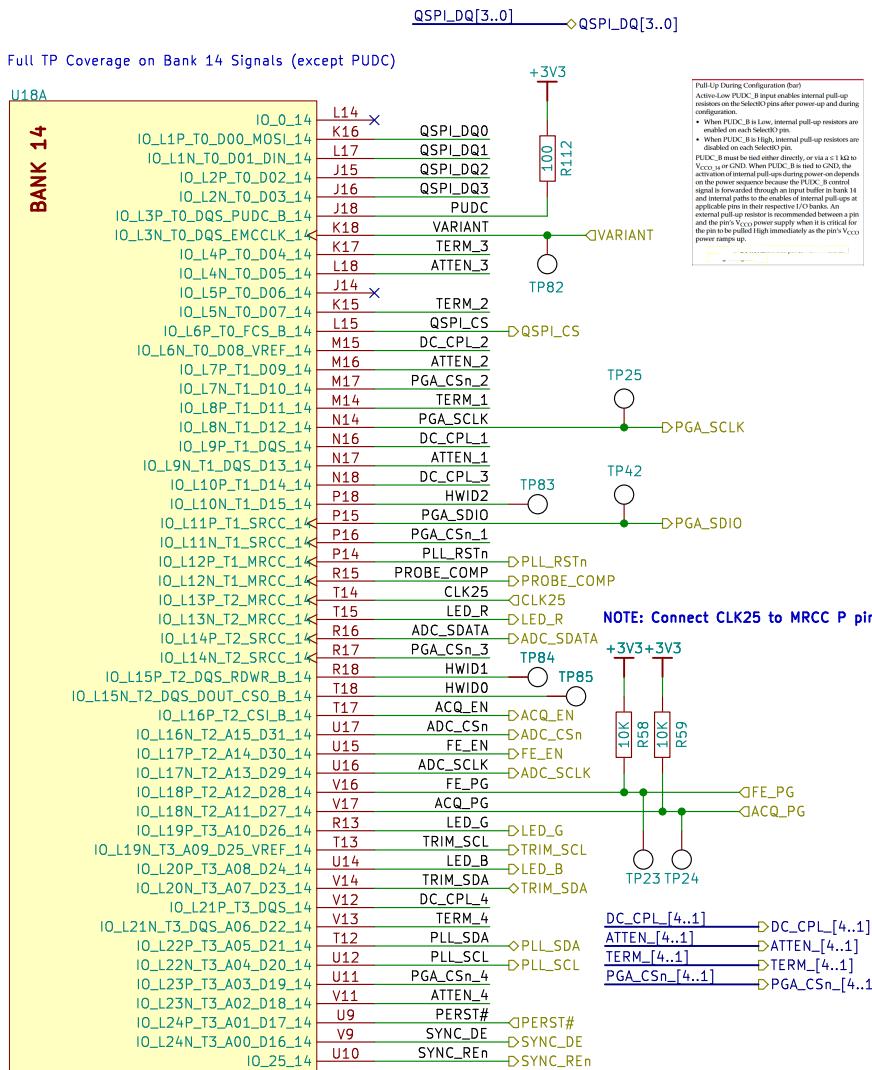
Drawn by: Aleksa Bjelogrlic

Rev: 5.3

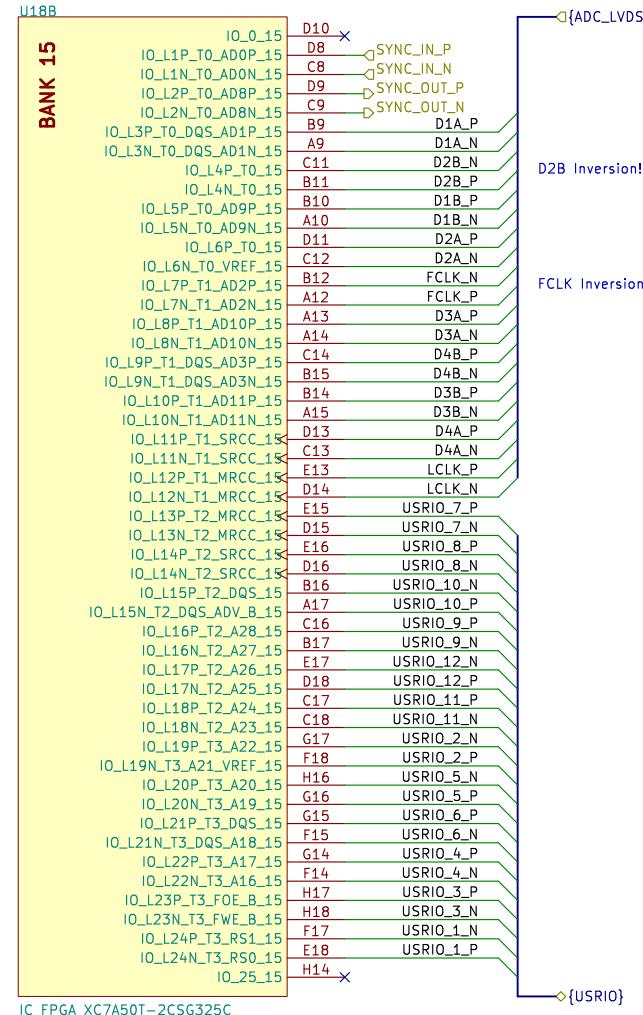
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1 2 3 4 5 6

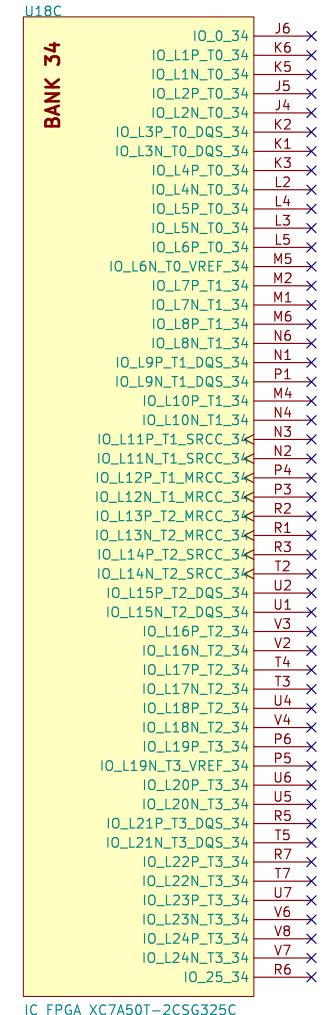
FPGA IO Banks



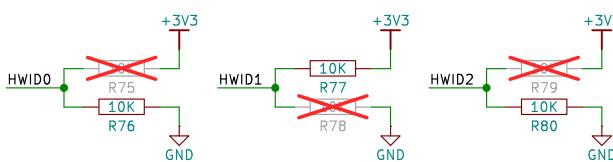
IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C



EEV

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Sheet: /EPGA/EPGA IO E

File: FPGA_Bank_I0.kicad

Title: Thunder

Size: A4 Date:

Page 1

Rev. 5.3

FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

Note: DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and

Table 2-1: 7 Series FPGA Configuration Modes				
Configuration Mode	M2[0]	Bus Width	CCLK Direction	
Master SPI	001	x1, x2, x4	Output	

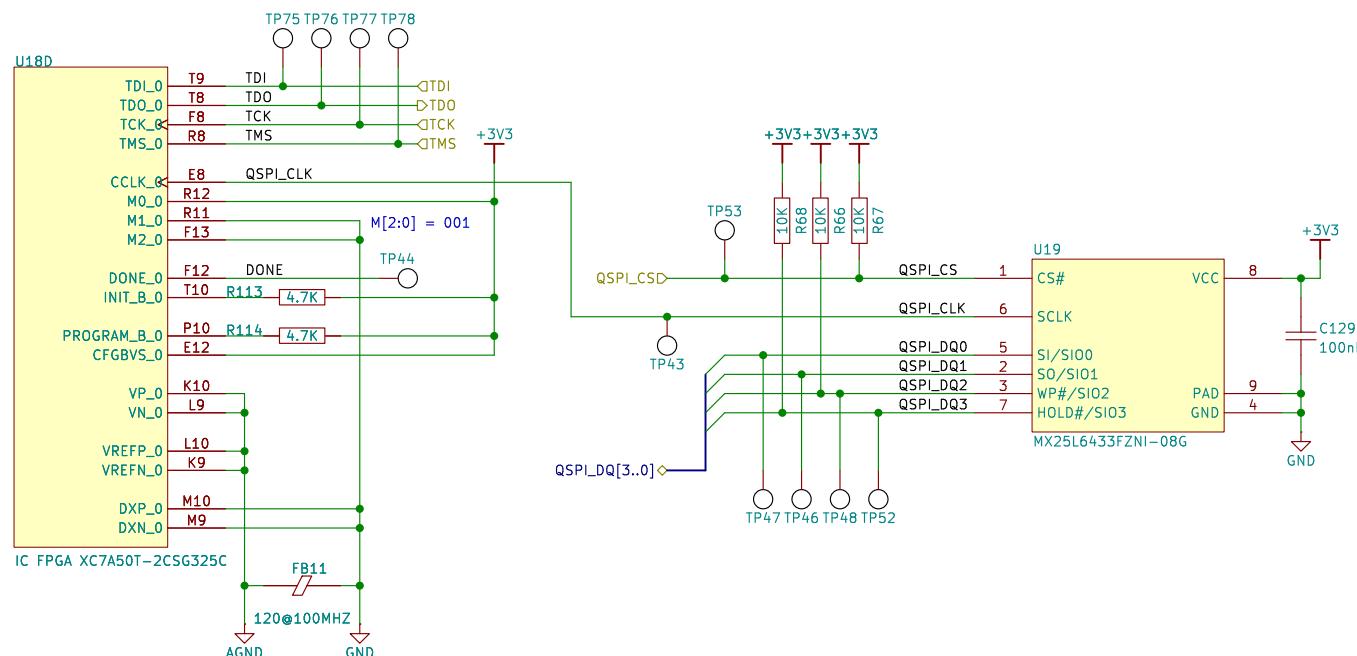
Table 2-2: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Banks Used	Configuration Interface I/O	HR Bank 0 V _{CCO}	HR Bank 14 V _{CCO}	HR Bank 15 V _{CCO}	CFGBVS
JTAG (only)	0	V _{PP}	3.3V	3.3V	Any	V _{CCO_0} , 0
		V _{REFP_0}	2.5V	2.5V	Any	V _{CCO_0} , 0
		V _{REFN_0}	1.8V	1.8V	Any	GND
		V _{PP}	3.3V	3.3V	Any	V _{CCO_0} , 0
Serial SPI or SelectMAP	0, 14 ⁽¹⁾	V _{PP}	2.5V	2.5V	2.5V	V _{CCO_0} , 0
		V _{REFP_0}	1.8V	1.8V	1.8V	GND
		V _{REFN_0}	1.8V	1.8V	1.8V	GND
		V _{PP}	3.3V	3.3V	3.3V	V _{CCO_0} , 0
BPI ⁽²⁾	0, 14, 15	V _{PP}	2.5V	2.5V	2.5V	V _{CCO_0} , 0
		V _{REFP_0}	1.8V	1.8V	1.8V	GND
		V _{REFN_0}	1.8V	1.8V	1.8V	GND
		V _{PP}	3.3V	3.3V	3.3V	GND

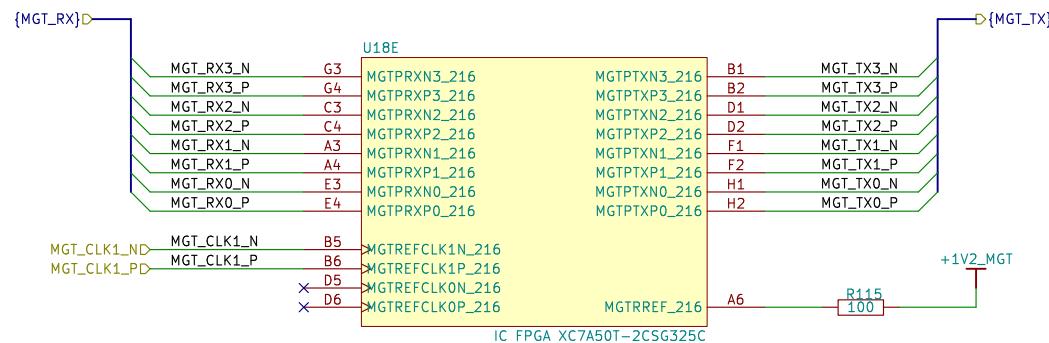
Notes:

1. RS1_0 for Multiflash or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.

2. BPI mode is not available in the Spartan-7 family.



FPGA Transceivers



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Sheet: /FPGA/FPGA Config and Transceivers/
File: FPGA_CFG_MGT.kicad_sch

Title: ThunderScope

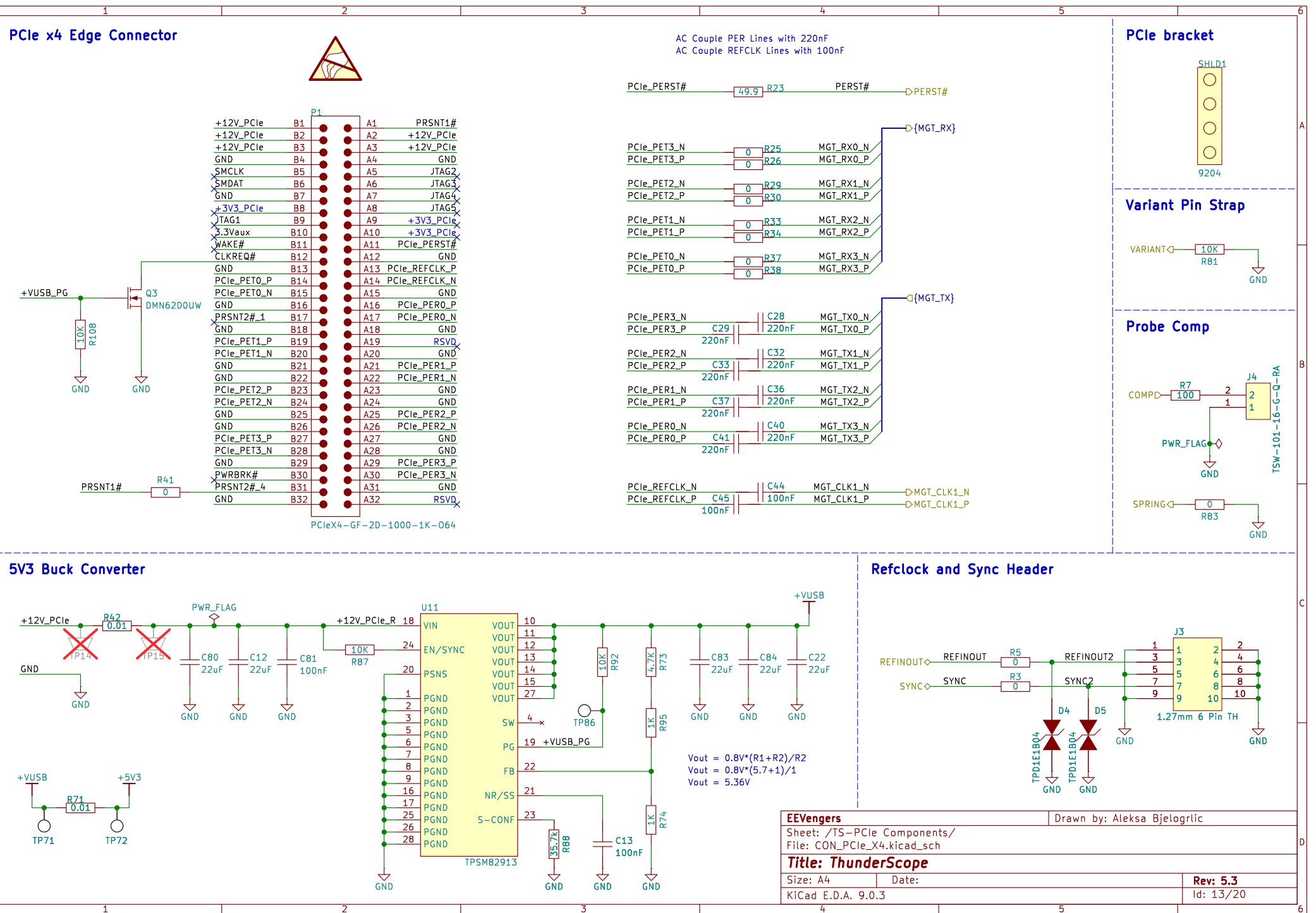
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KiCad E.D.A. 9.0.3

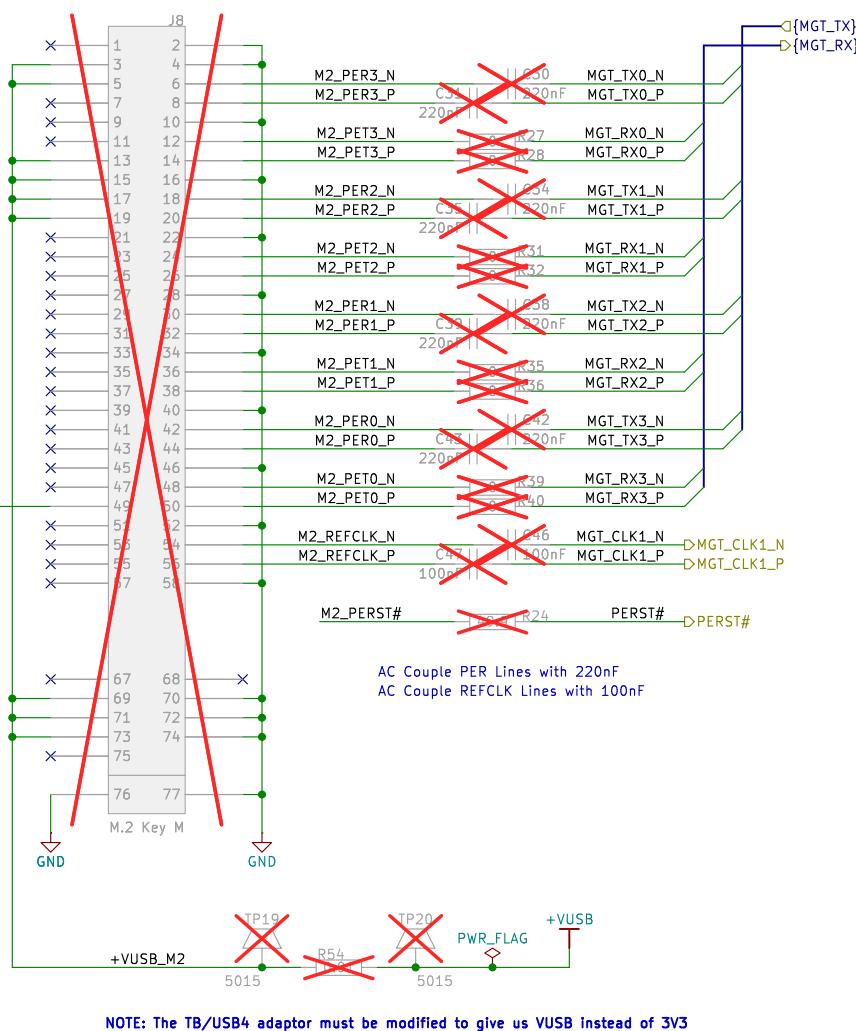
Drawn by: Aleksa Bjelogrlic

Rev: 5.3

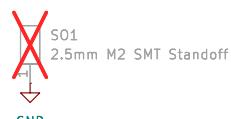
Id: 10/20



M.2 Key M Connector – Custom Pinout



Interposer Standoffs



Probe Comp

COMPD → R84 → D_{SPRING}

Fan Connector

+VUSB → J10 → GND
 00915500285200b

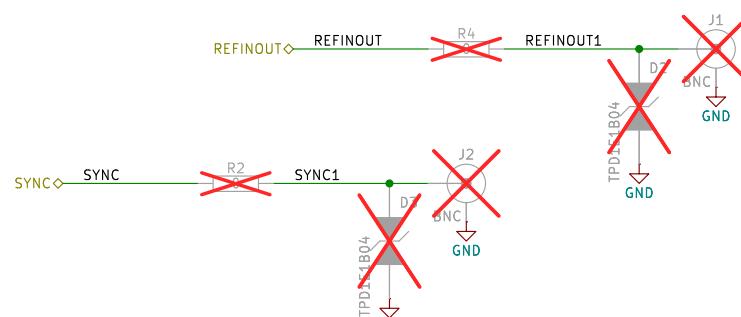
Ground Lug

J11 → GND
 77 → GND

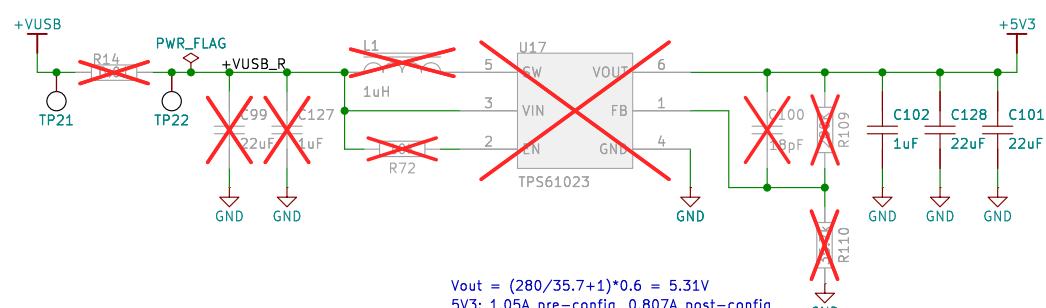
Variant Pin Strap

VARIANT → R82 → +3V3

Refclock and Sync BNCs



5V3 Boost Converter



EEVengers

Sheet: /TS-USB4 Components/
 File: M2_KEY_M.kicad_sch

Title: ThunderScope

Size: A4 Date:

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Drawn by: Aleksa Bjelogrlic

Rev: 5.3

Id: 14/20