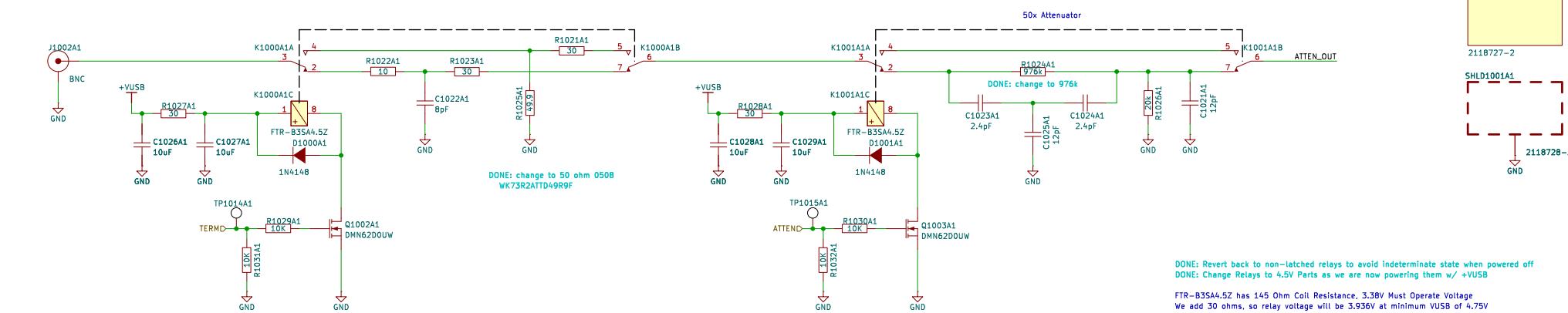
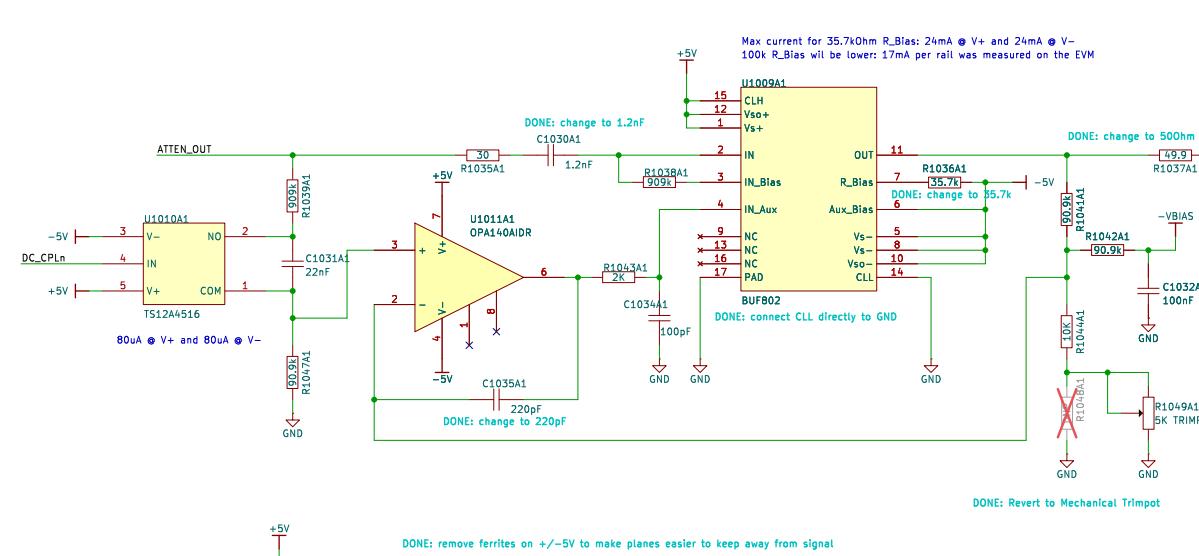


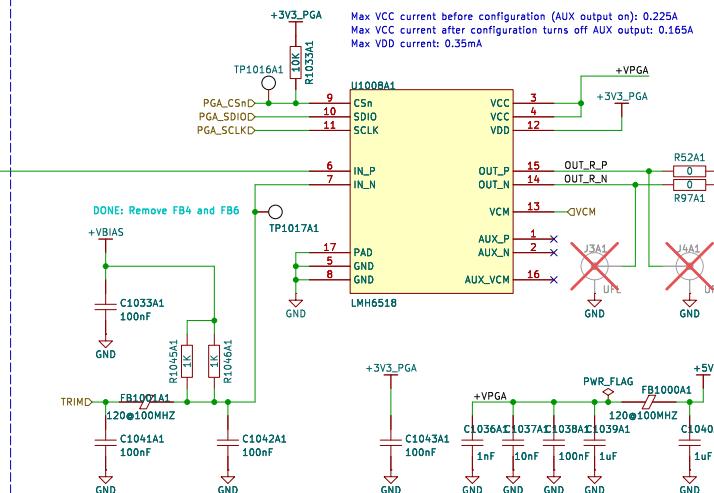
Termination and Attenuation



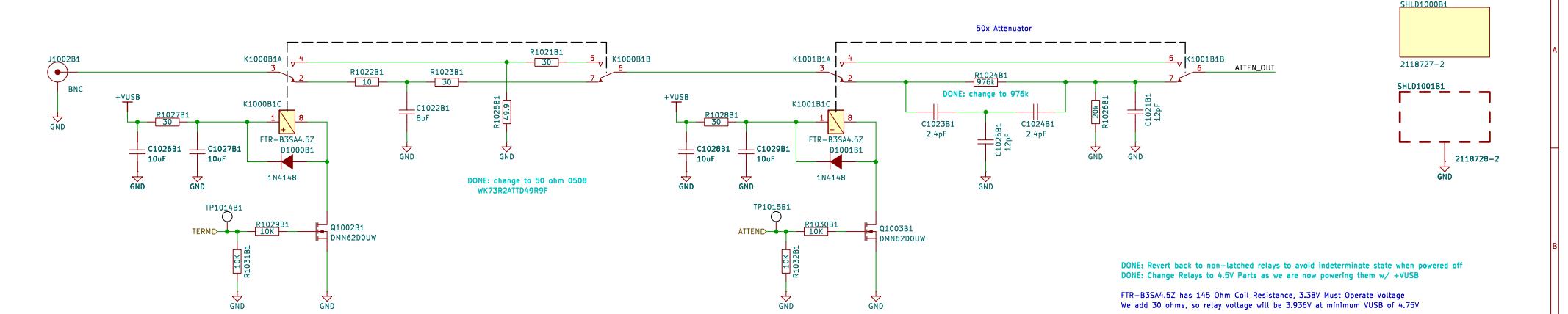
Input Buffer and AC/DC Coupling



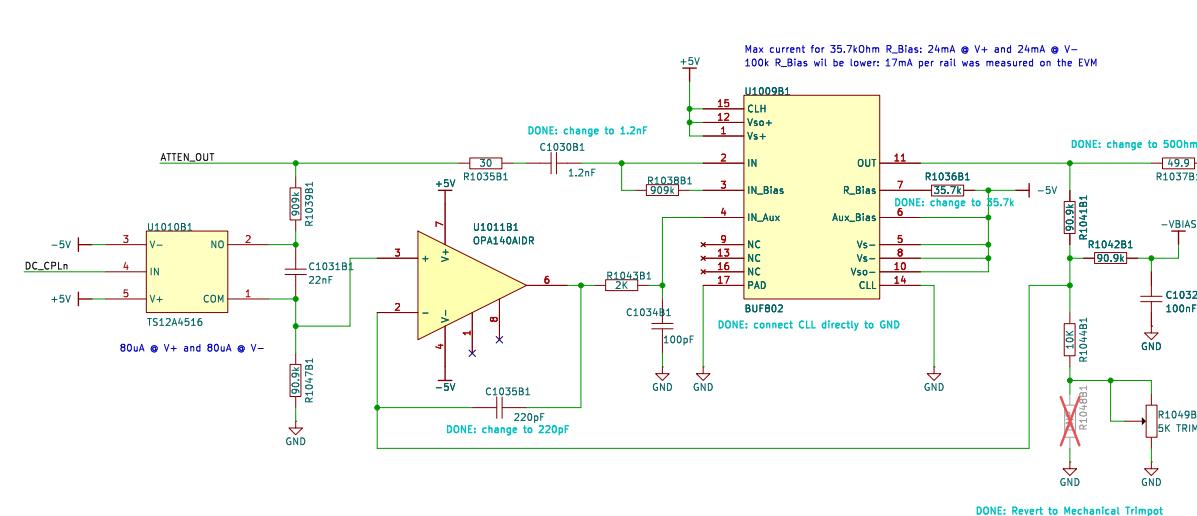
Programmable Gain Amplifier



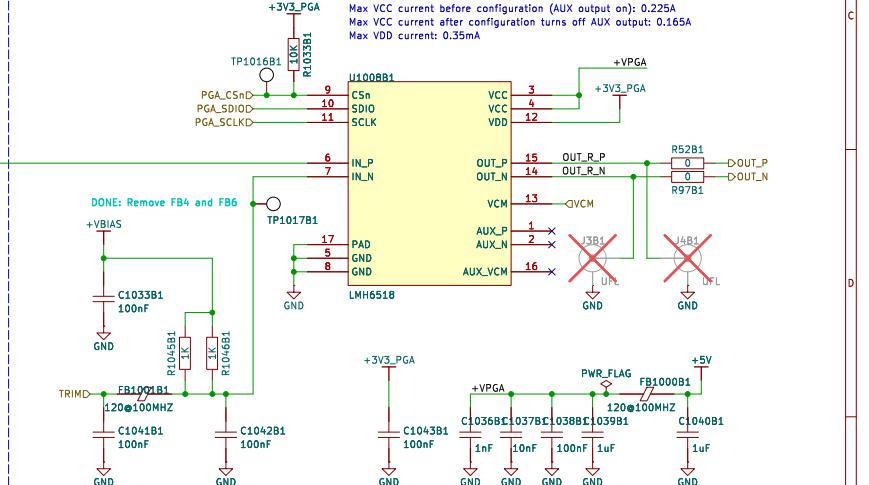
Termination and Attenuation



Input Buffer and AC/DC Coupling

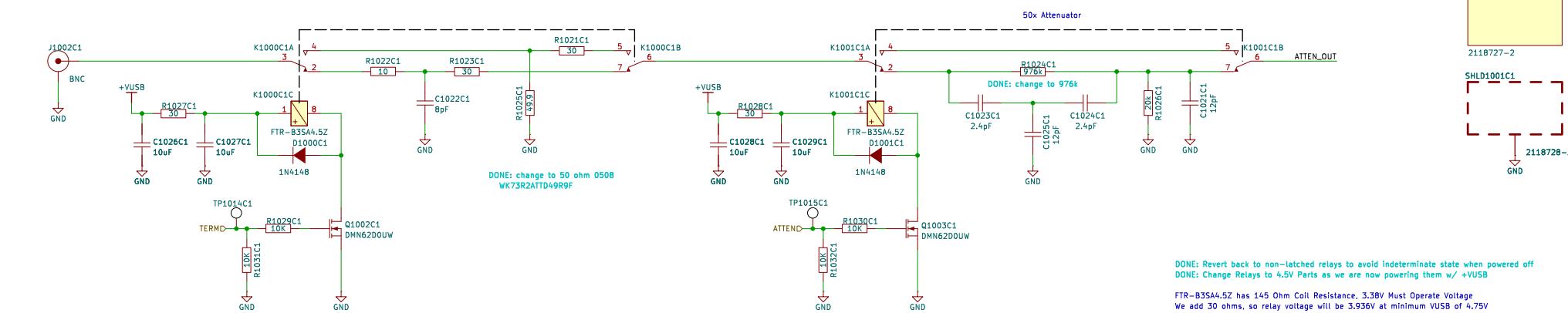


Programmable Gain Amplifier

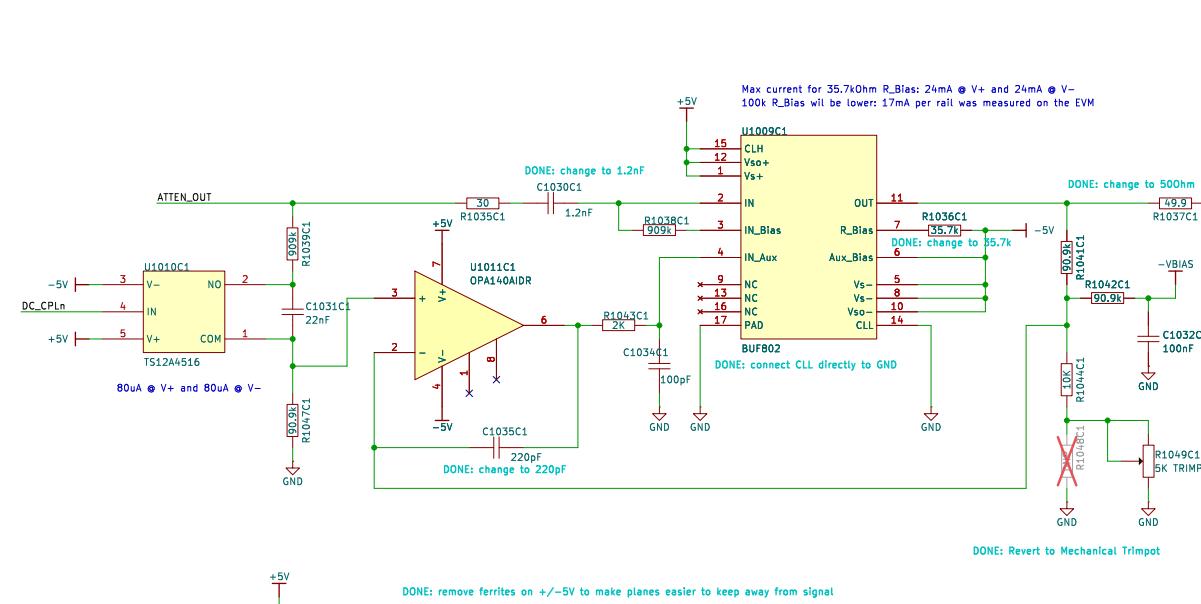


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KICad E.D.A. 8.99.0-3402-gadd58fa30	Id:

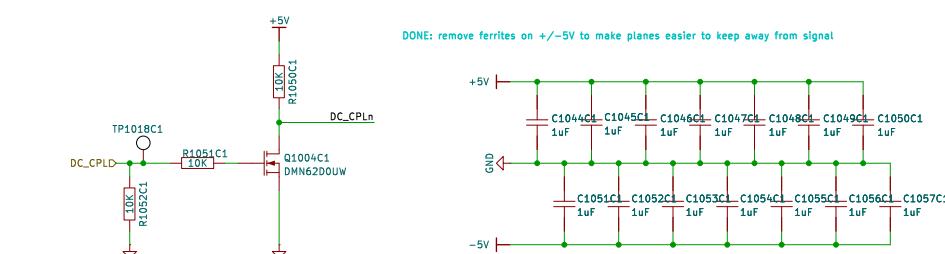
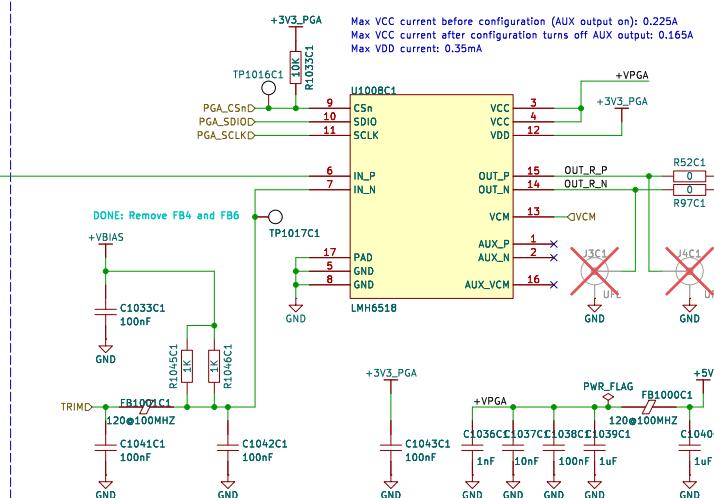
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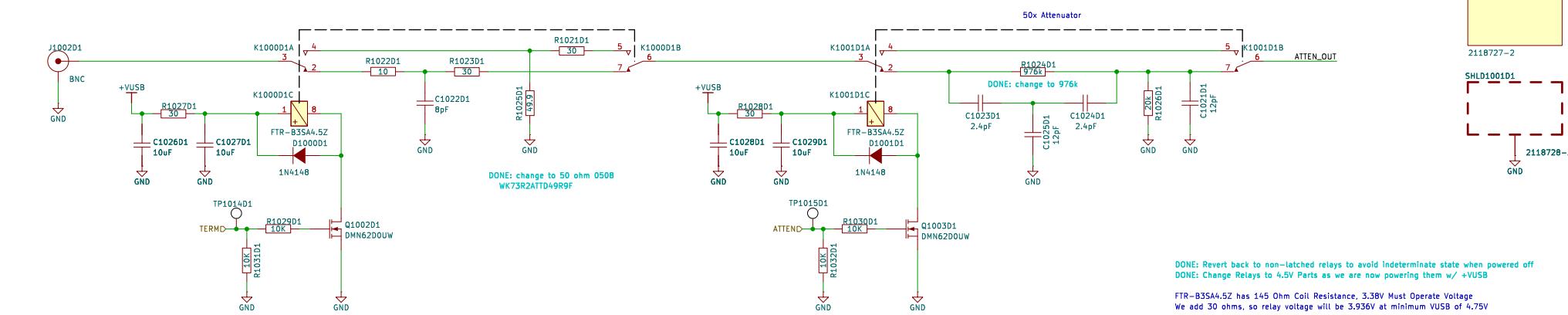
Input Buffer and AC/DC Coupling



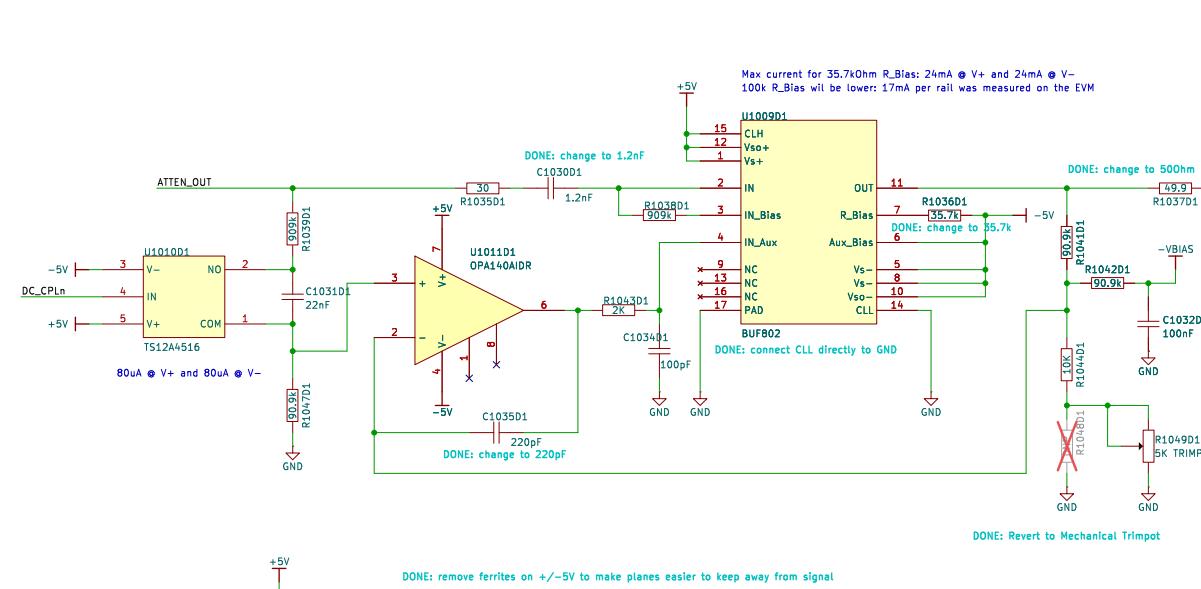
Programmable Gain Amplifier



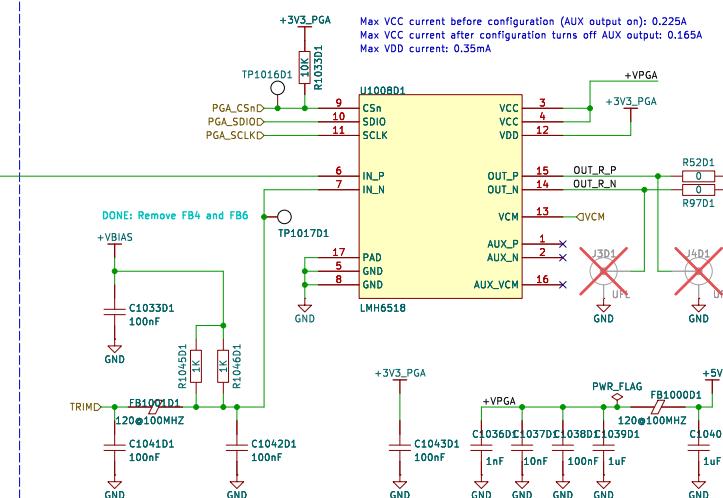
Termination and Attenuation



Input Buffer and AC/DC Coupling



Programmable Gain Amplifier

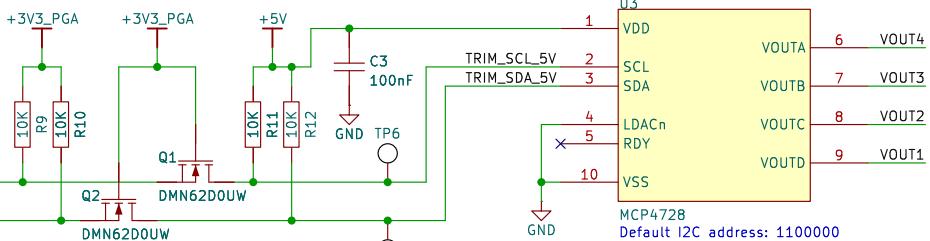


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Sheet: /CH4/	
File: FE_Channel.kicad_sch	
Title: ThunderScope	
Size: A3	Date: Rev: 5
KiCad E.D.A. 8.99.0 -3402-gadd58faa30	Id: 2/16

1 2 3 4 5 6

Offset Voltage Trim and User Offset Control

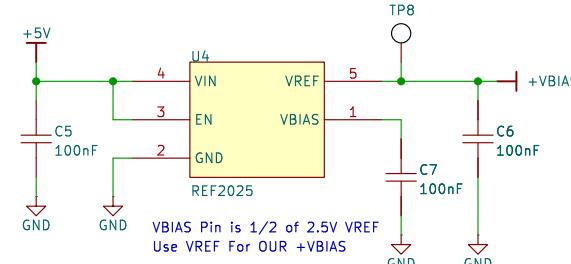
A



B

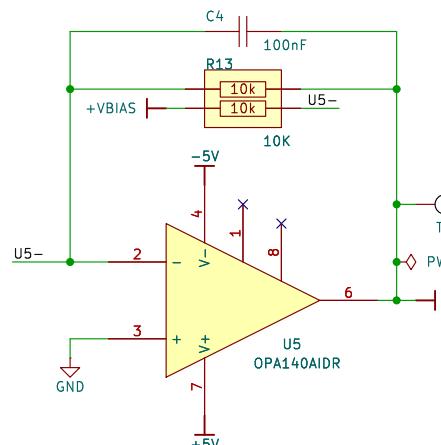
Bias Voltage Generation

C



D

Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140
-Max resistance is $(575/4 // 10k) = 141.7 \text{ Ohm}$
-Worst case current is 17.64mA
-Use REF2025, has max current of 20mA
-Change U5 divider to matched resistor network
-ACASN1002S1002P1AT



EEVengers

Sheet: /Front End Trim and Bias/
File: FE.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 3/16

1

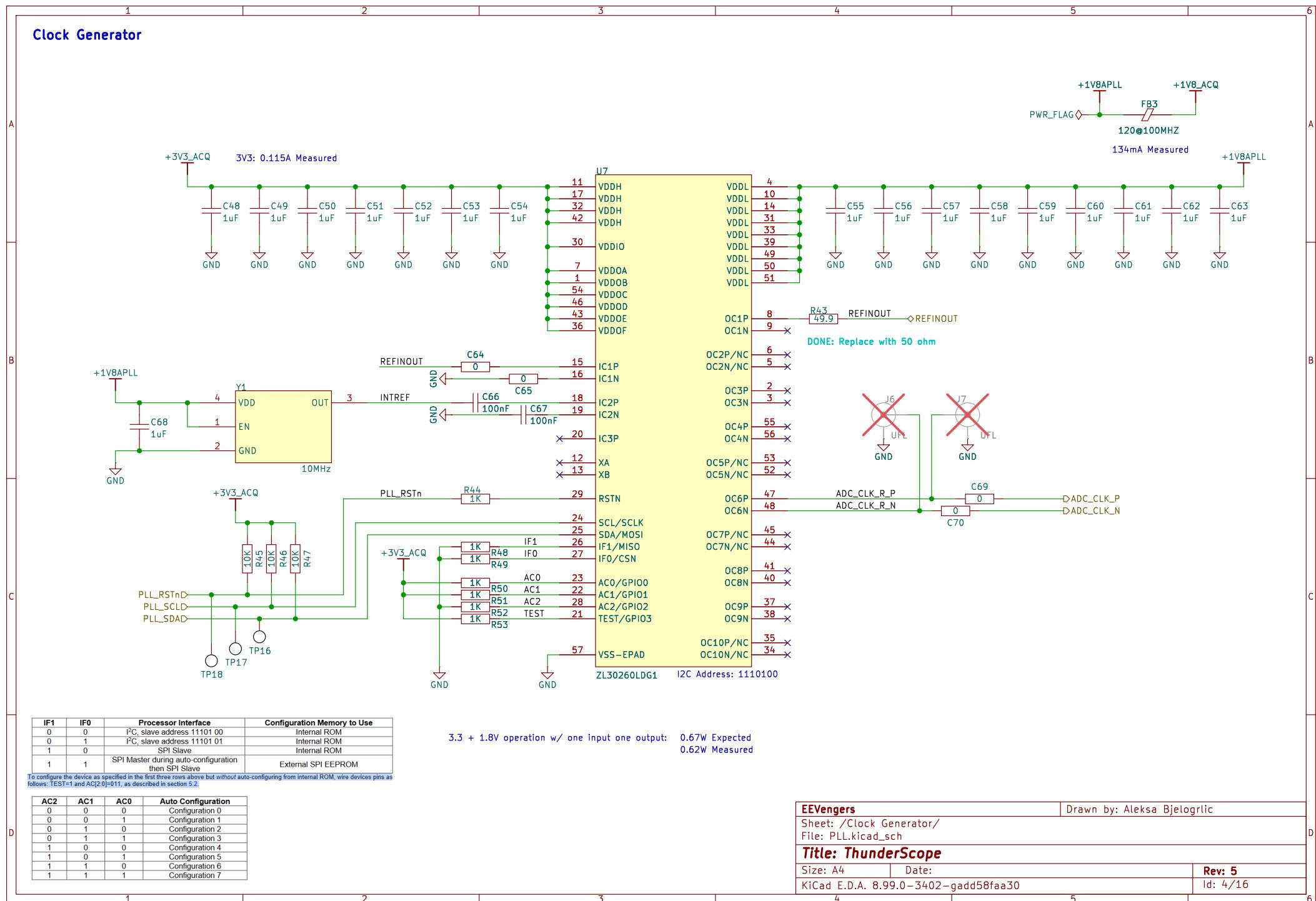
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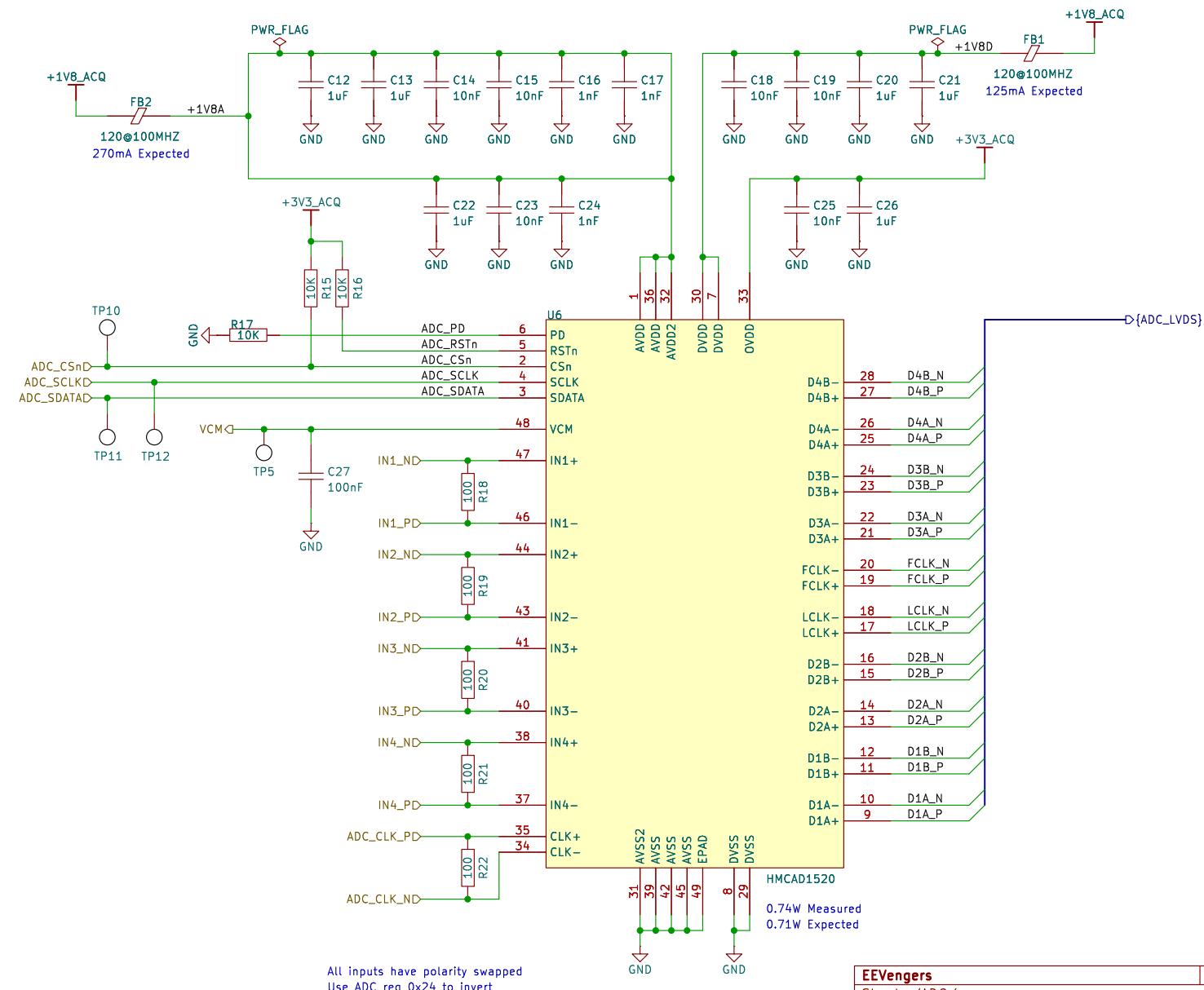
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6



1 2 3 4 5 6

ADC



EEVengers

Drawn by: Aleksa Bjelogrlic

Sheet: /ADC/

File: ADC.kicad_sch

Title: ThunderScope

Size: A4 Date:

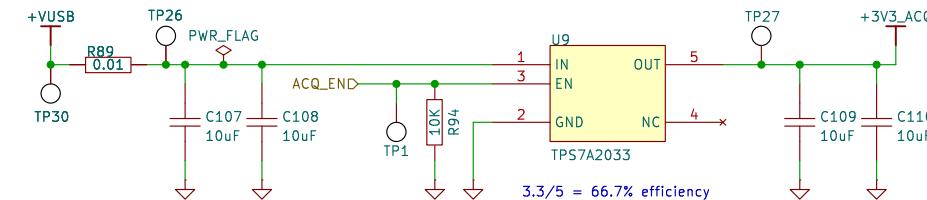
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Rev: 5

Id: 5/16

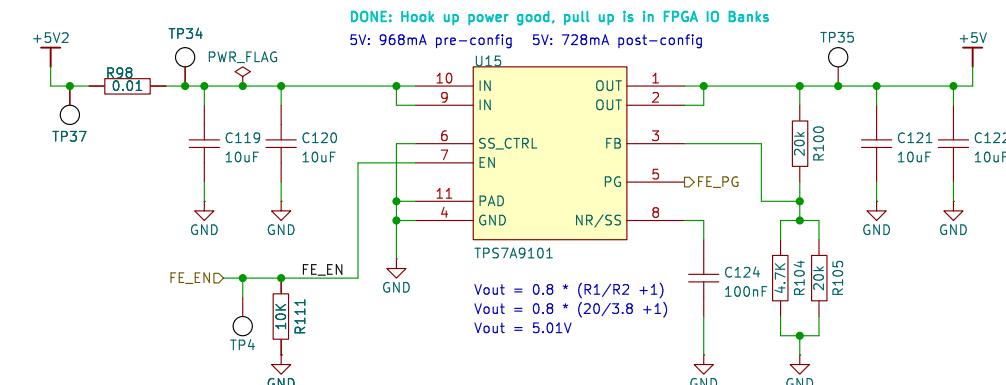
1 2 3 4 5 6

Acquisition Voltage Regulators

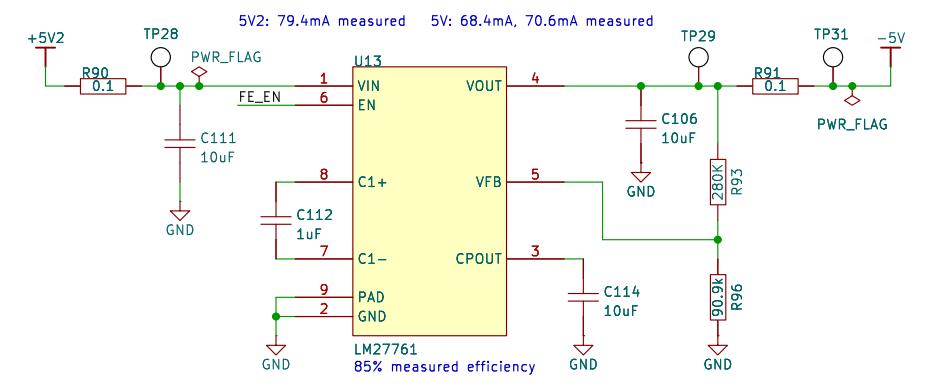
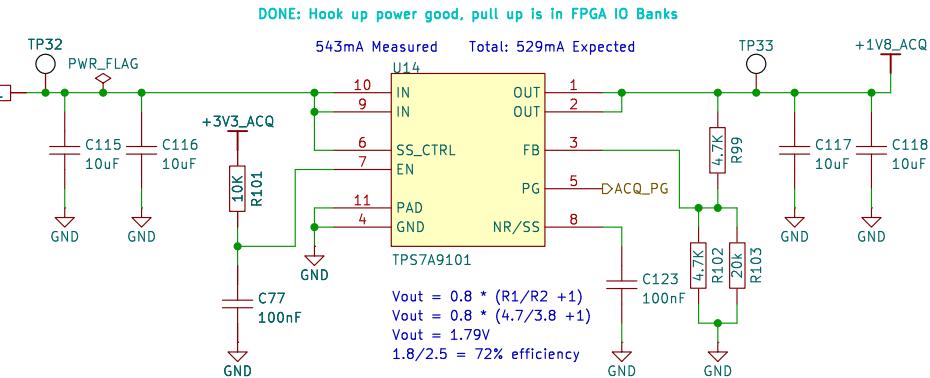
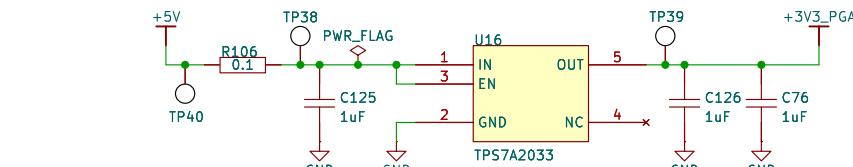


DONE: Hook up power good, pull up is in FPGA IO Banks

Front End Voltage Regulators



6ms soft start time on previous LDO, need same or greater
 $T_{ss} = (V_{REF} \times C_{nr/ss}) / I_{nr/ss}$
 $T_{ss} = (0.8 \times 100nF) / 6.2\mu A$ [for SS_CTRL = GND]
 $T_{ss} = 0.0129s = 13ms$



EEVengers

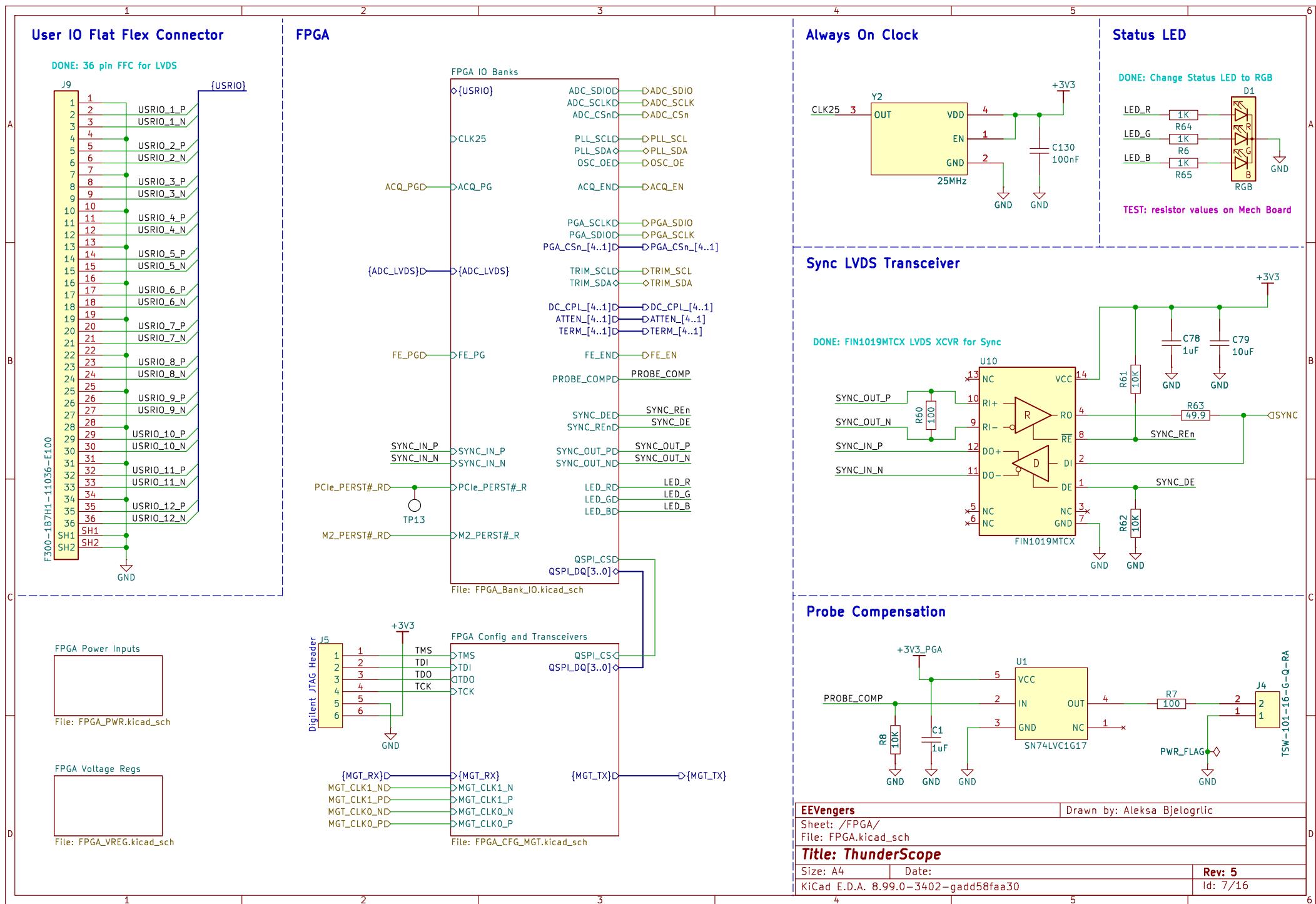
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Title: ThunderScope

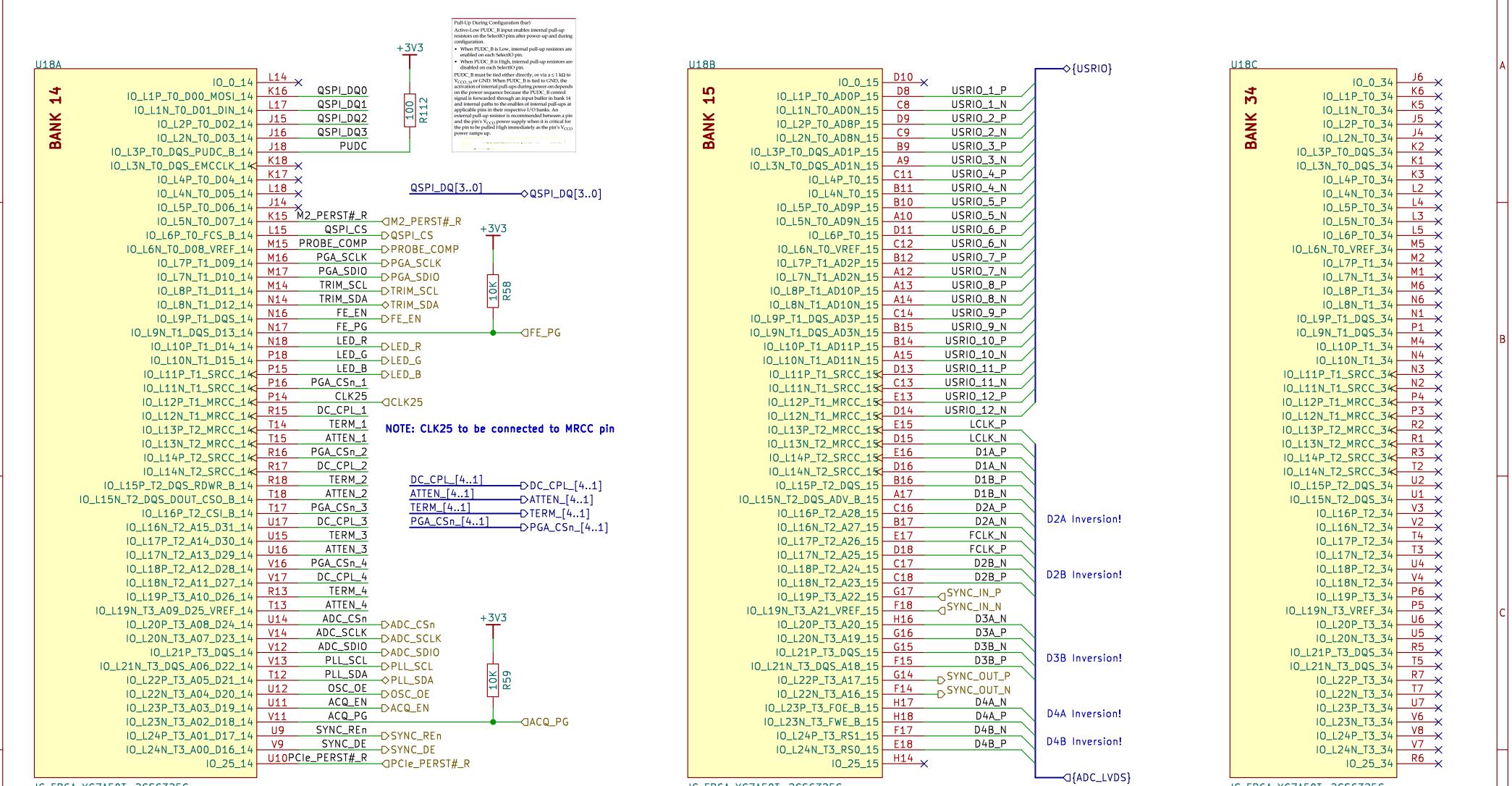
Size: A4 Date:
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Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 6/16



FPGA IO Banks



IC FPGA XC7A50T-2CSG325C

IC FPGA XC7A50T-2CSG325C

1 2 3 4 5 6

EEVengers

Sheet: /FPGA/FPGA IO Banks/
File: FPGA_Bank_IO.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 8/16

1 2 3 4 5 6

FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

Note: DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

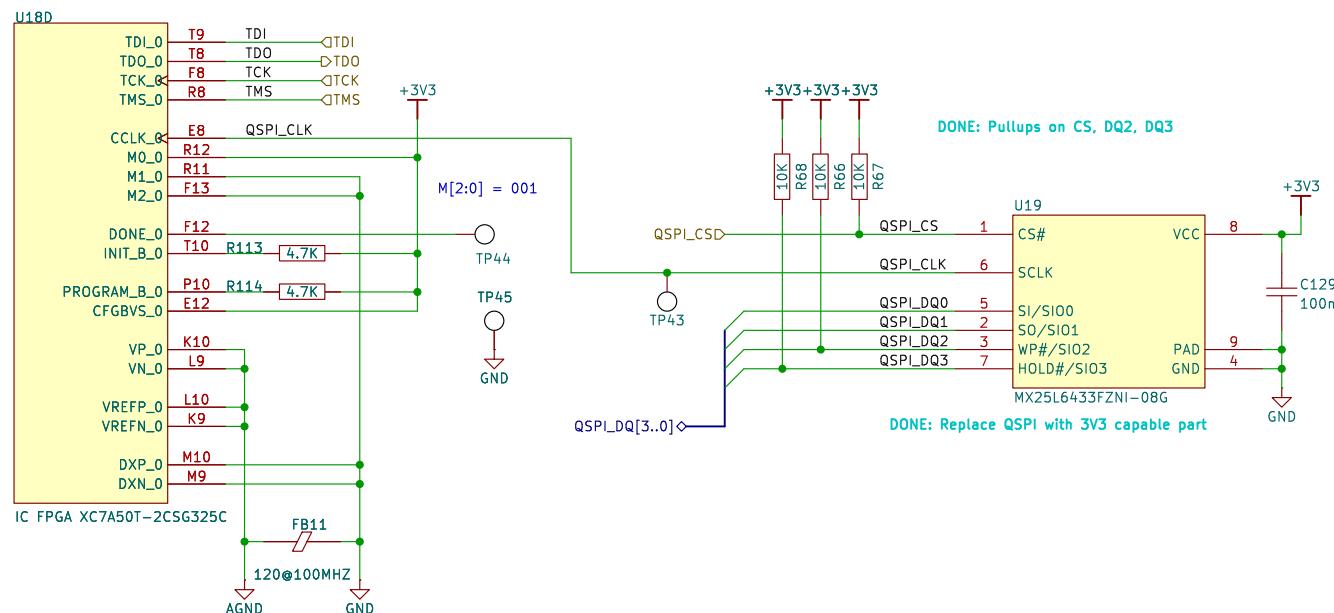
Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and

Table 2-1: 7 Series FPGA Configuration Modes				
Configuration Mode	M2[0]	Bus Width	CCLK Direction	
Master SPI	001	x1, x2, x4	Output	

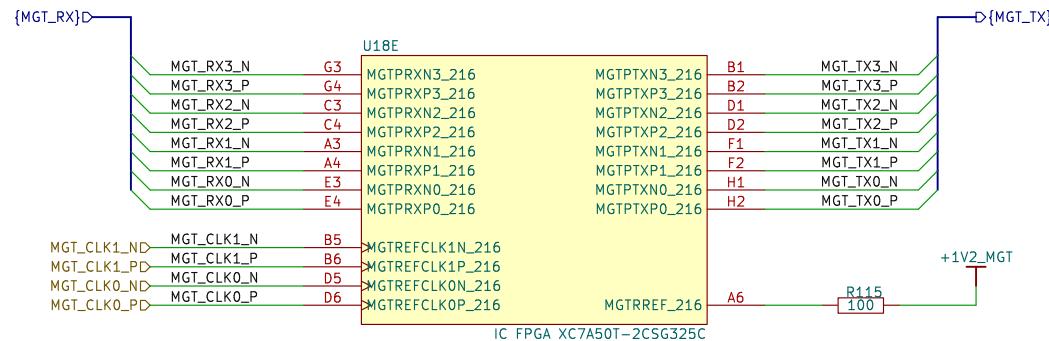
Table 2-6: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Bank Used	Configuration Interface I/O	HR Bank 0 V _{CCO} 0	HR Bank 14 V _{CCO} 14	HR Bank 15 V _{CCO} 15	CFGBVS
JTAG (only)	0	VREFP_0	2.5V	2.5V	Analog	VCCO_0
		VREFN_0	1.8V	1.8V	Analog	GND
		DXP_0	2.5V	2.5V	2.5V	VCCO_0
		DXN_0	1.8V	1.8V	1.8V	GND
Serial SPI or SelectMAP	0, 14 ⁽¹⁾	VREFP_0	3.3V	3.3V	3.3V	VCCO_0
		VREFN_0	2.5V	2.5V	2.5V	VCCO_0
		DXP_0	1.8V	1.8V	1.8V	GND
		DXN_0	1.8V	1.8V	1.8V	GND
		BPI ⁽²⁾	1.8V	1.8V	1.8V	1.8V
BPI ⁽²⁾	0, 14, 15	VREFP_0	3.3V	3.3V	3.3V	VCCO_0
		VREFN_0	2.5V	2.5V	2.5V	VCCO_0

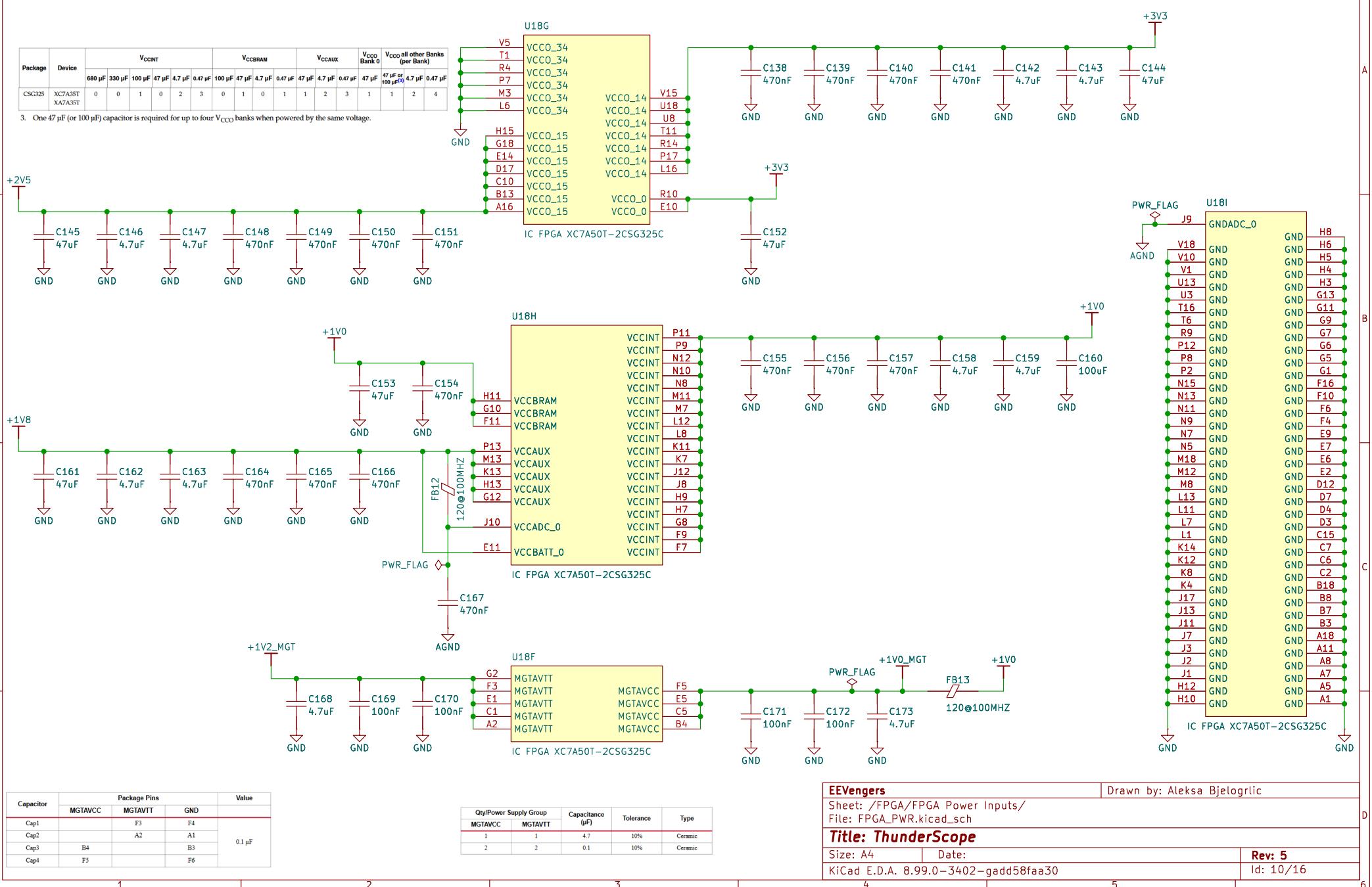
Notes:
1. RS1-0 for Multiboot or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.
2. BPI mode is not available in the Spartan-7 family.



FPGA Transceivers

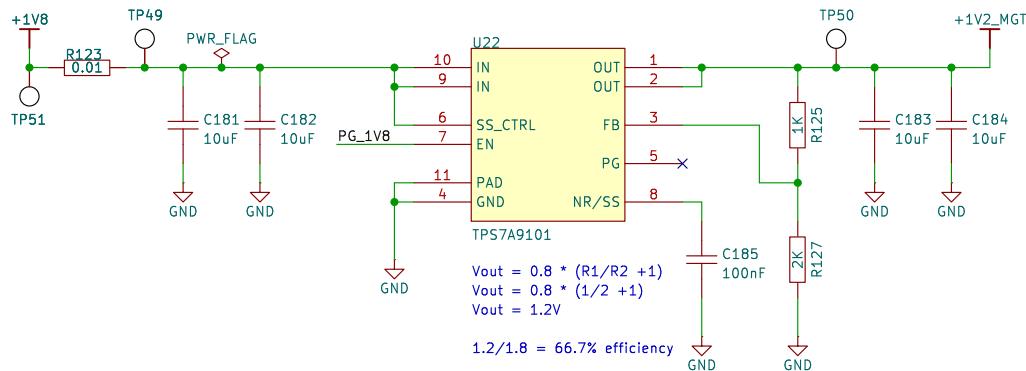
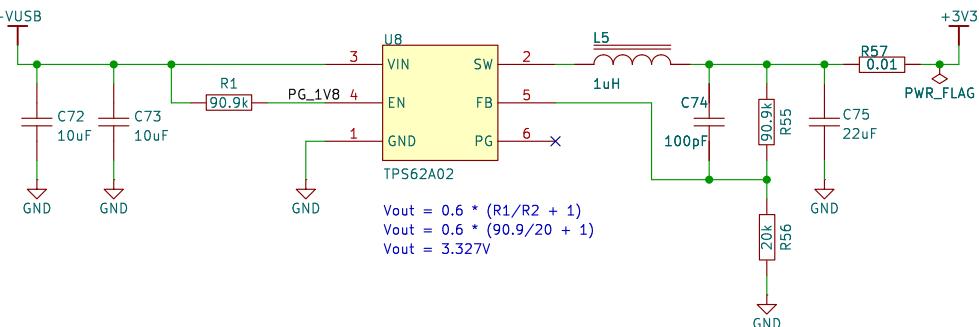
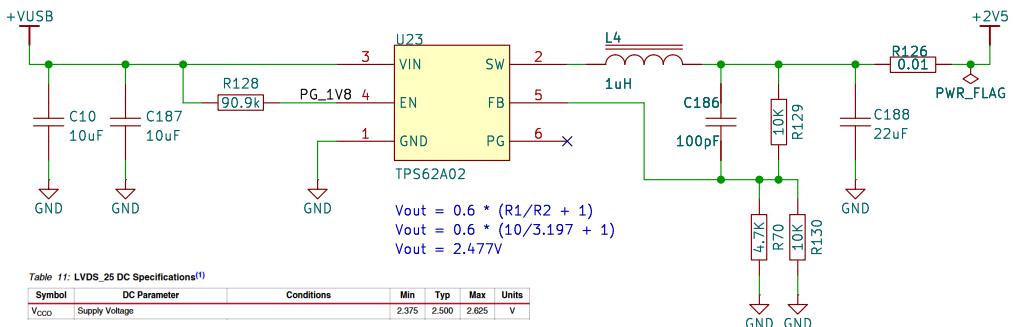
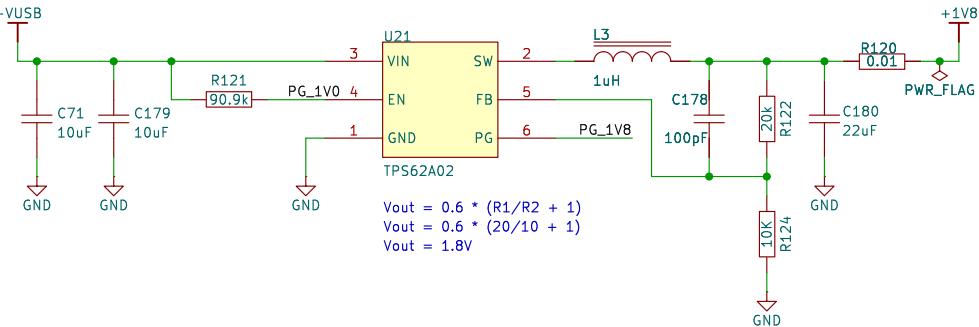
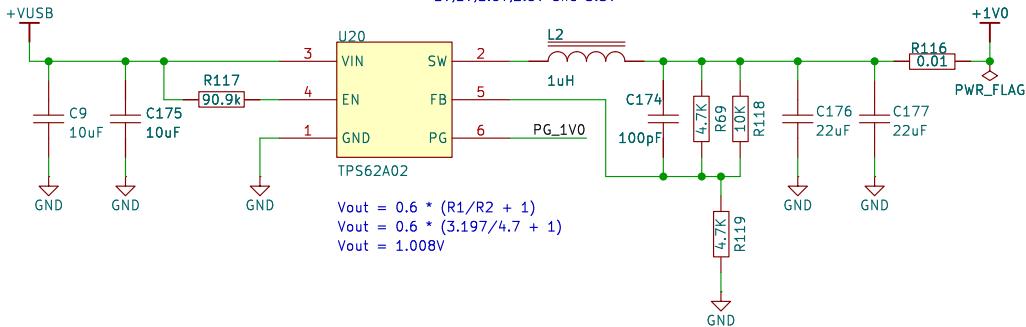


PAGE 1: FPGA Power Inputs



FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V

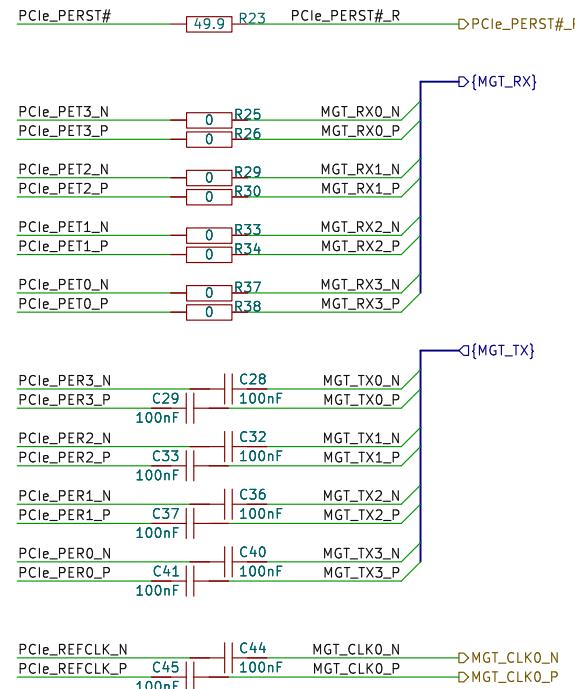
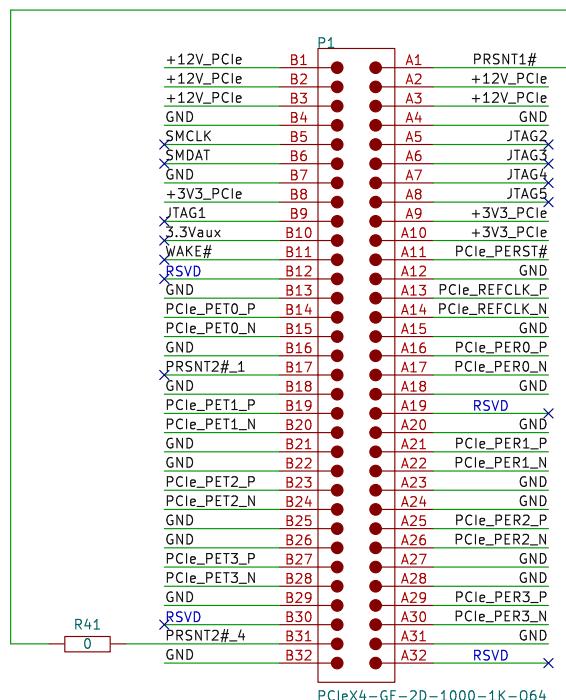


The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT
1V1V1.2V

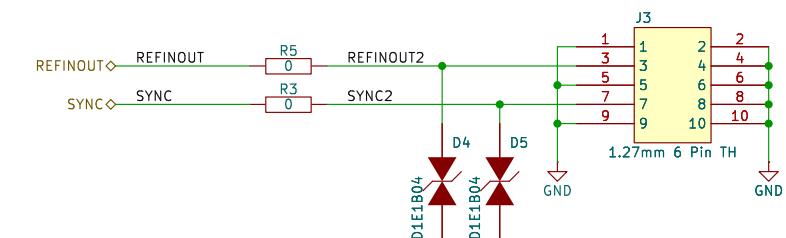
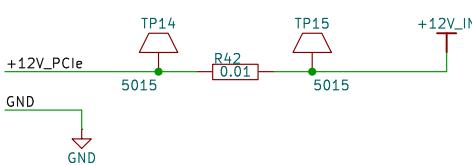
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Title: ThunderScope	
Size: A4	Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30	Rev: 5 Id: 11/16

1 2 3 4 5 6

PCIe x4 Edge Connector



TODO: 12V to VUSB Buck Regulator



EEVengers

Sheet: /PCIe_x4/
File: CON_PCIe_X4.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 12/16

1 2 3 4 5 6

1

2

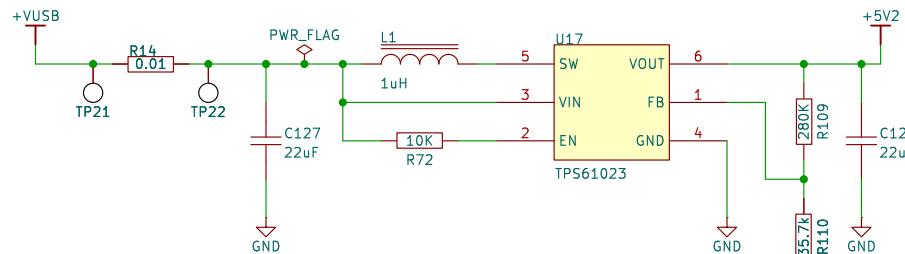
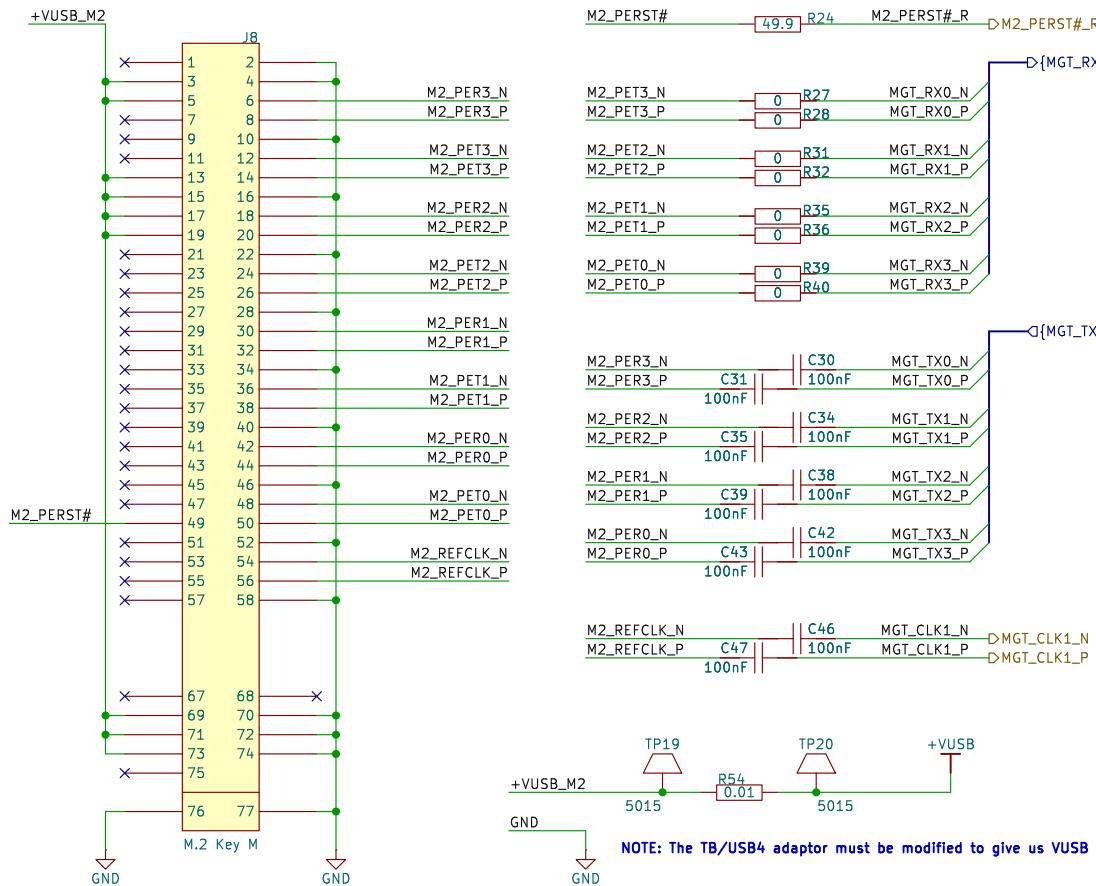
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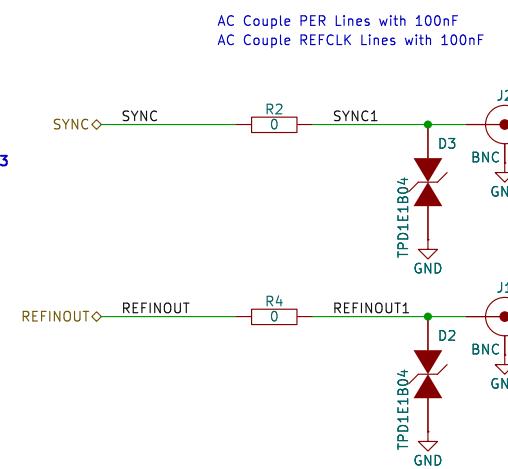
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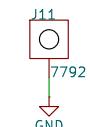
M.2 Key M Connector – Custom Pinout



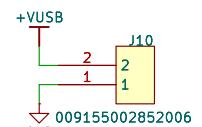
AC Couple PER Lines with 100nF
AC Couple REFCLK Lines with 100nF



Ground Lug



Fan Connector



EEVengers

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Sheet: /M.2_Key_M/

File: M2_KEY_M.kicad_sch

Title: ThunderScope

Size: A4 Date:

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Rev: 5

Id: 13/16