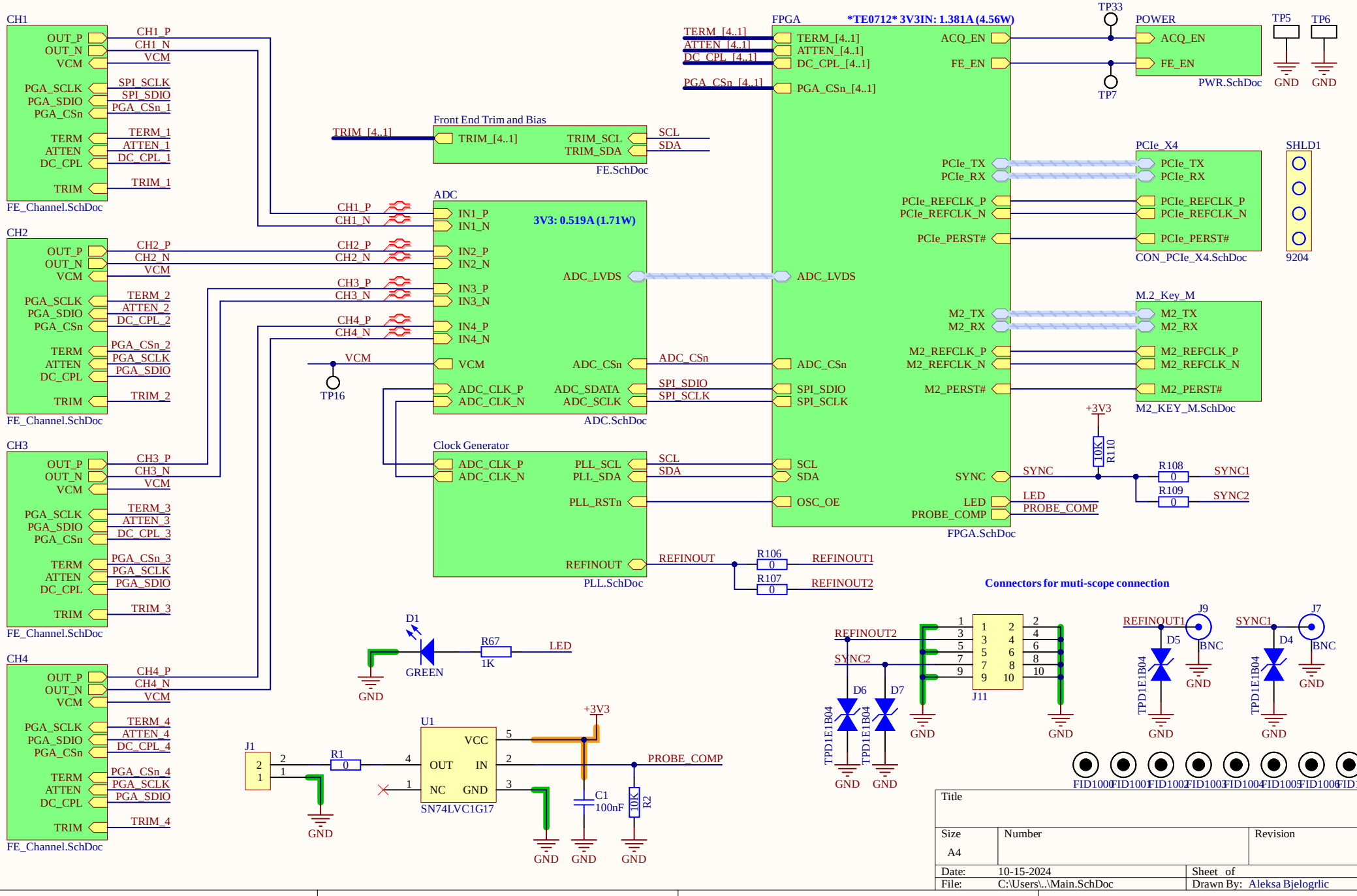
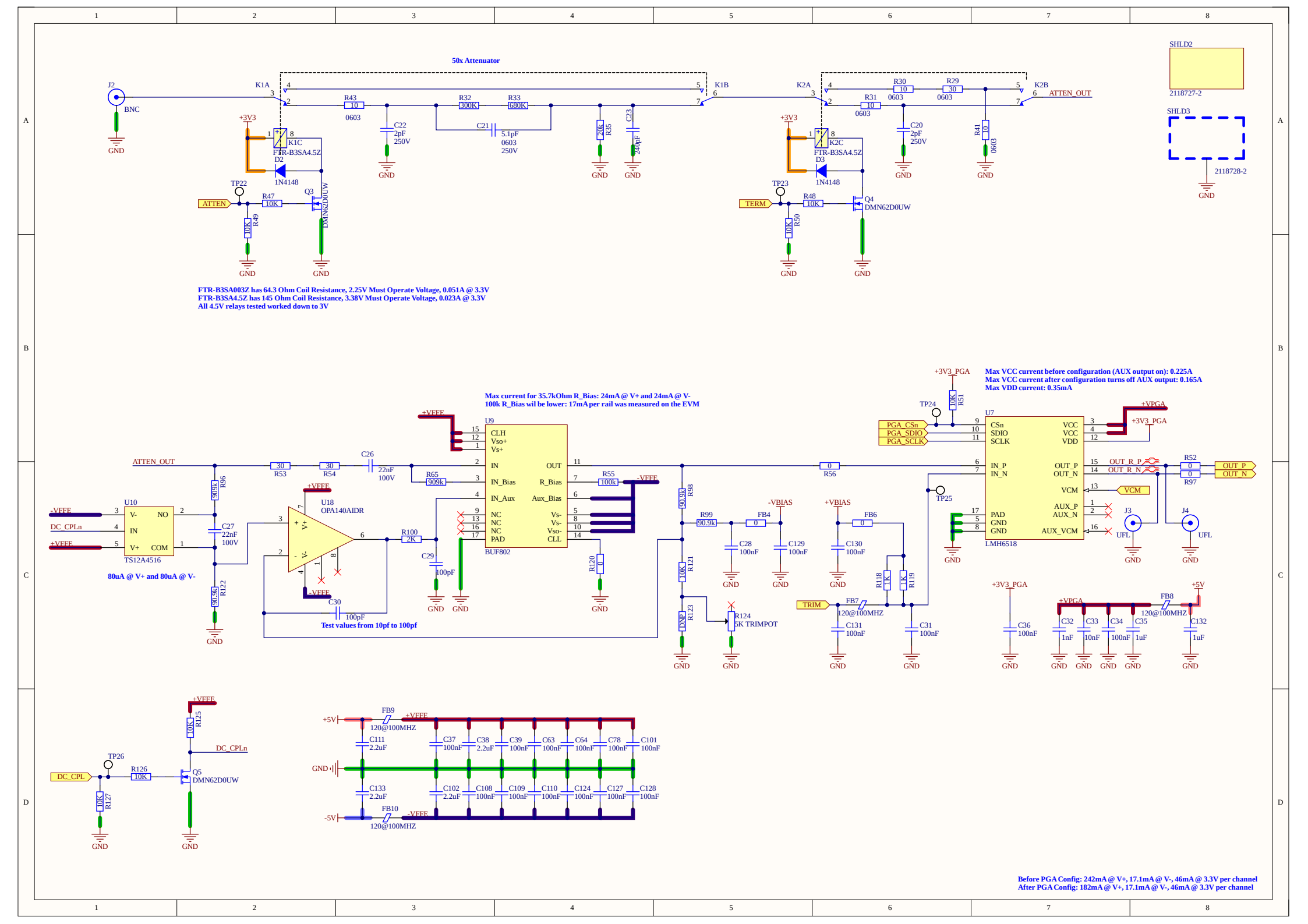
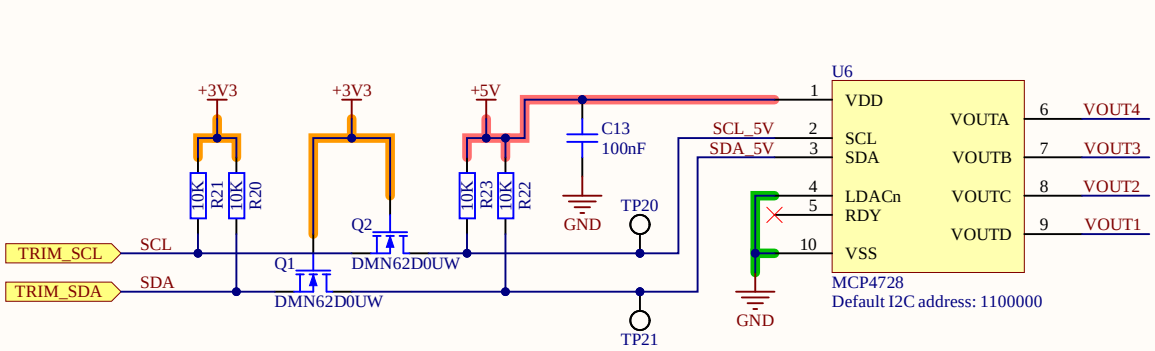
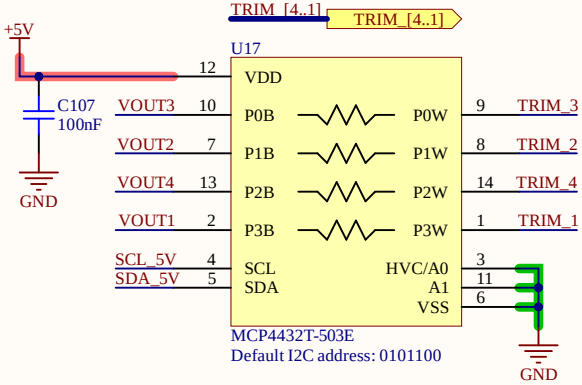
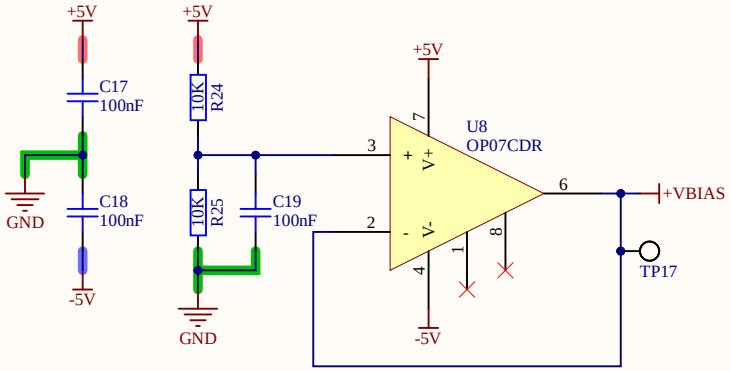
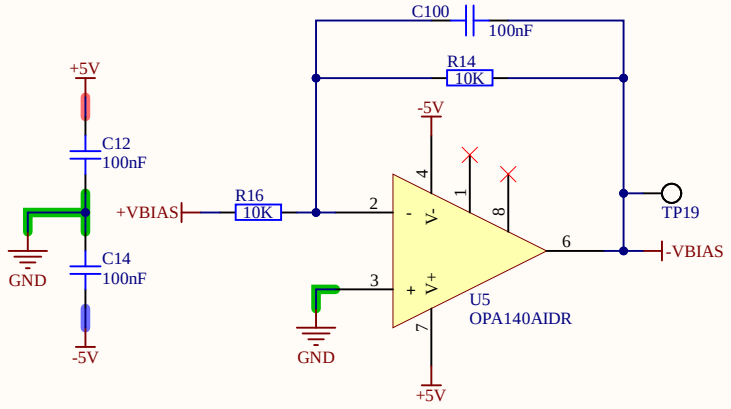

CH1
FE_Channel.SchDoc
CH2
FE_Channel.SchDoc
CH3
FE_Channel.SchDoc
CH4
FE_Channel.SchDoc
Front End Trim and Bias
FE.SchDoc
ADC
3V3: 0.519A (1.71W)
ADC.SchDoc
Clock Generator
PLL.SchDoc
FPGA
TE0712 3V3IN: 1.381A (4.56W)
FPGA.SchDoc
POWER
PWR.SchDoc
PCIe_X4
CON_PCIe_X4.SchDoc
SHLD1
9204
M.2_Key_M
M2_KEY_M.SchDoc
Connectors for muti-scope connection
SN74LVC1G17
Title
Size
A4
Number
Revision
Date: 10-15-2024
File: C:\Users\..\Main.SchDoc
Sheet of
Drawn By: Aleksa Bjelogrlic


50x Attenuator
J2
BNC
GND
K1A
K1B
K2A
K2B
ATTEN_OUT
R43
10
0603
C22
2pF
250V
R32
300K
R33
680K
C21
5.1pF
0603
250V
20K
R35
C23
240pF
+3V3
K1C
FTR-B3SA4.5Z
D2
1N4148
TP22
ATTEN
R47
10K
Q3
DMN62D0UW
10K
R49
R30
10
0603
R29
30
0603
R31
10
0603
C20
2pF
250V
R41
10
0603
K2C
FTR-B3SA4.5Z
D3
1N4148
TP23
TERM
R48
10K
Q4
DMN62D0UW
10K
R50
SHLD2
2118727-2
SHLD3
2118728-2
FTR-B3SA003Z has 64.3 Ohm Coil Resistance, 2.25V Must Operate Voltage, 0.051A @ 3.3V
FTR-B3SA4.5Z has 145 Ohm Coil Resistance, 3.38V Must Operate Voltage, 0.023A @ 3.3V
All 4.5V relays tested worked down to 3V
Max current for 35.7kOhm R_Bias: 24mA @ V+ and 24mA @ V-
100k R_Bias wil be lower: 17mA per rail was measured on the EVM
+VEFE
-VEFE
U9
BUF802
CLH
Vso+
Vs+
IN
IN_Bias
IN_Aux
NC
NC
NC
PAD
OUT
R_Bias
Aux_Bias
Vs-
Vs-
Vso-
CLL
ATTEN_OUT
R53
30
R54
30
C26
22nF
100V
R65
909k
R55
100k
R56
0
U10
TS12A4516
V-
NO
IN
V+
COM
DC_CPLn
+VEFE
-VEFE
R96
909k
C27
22nF
100V
R122
90.9k
80uA @ V+ and 80uA @ V-
U18
OPA140AIDR
R100
2K
C29
100pF
C30
100pF
Test values from 10pf to 100pf
R98
90.9k
R99
90.9k
FB4
0
C28
100nF
C129
100nF
-VBIAS
+VBIAS
FB6
0
C130
100nF
C131
100nF
R118
1K
R119
1K
TRIM
FB7
120@100MHZ
C31
100nF
R121
10K
DNP
R123
R124
5K TRIMPOT
R120
0
+3V3_PGA
TP24
R51
10K
PGA_CSn
PGA_SDIO
PGA_SCLK
U7
LMH6518
CSn
SDIO
SCLK
IN_P
IN_N
PAD
GND
VCC
VCC
VDD
OUT_P
OUT_N
VCM
AUX_P
AUX_N
AUX_VCM
+VPGA
+3V3_PGA
OUT_R_P
OUT_R_N
R52
0
R97
0
OUT_P
OUT_N
VCM
TP25
J3
J4
UFL
Max VCC current before configuration (AUX output on): 0.225A
Max VCC current after configuration turns off AUX output: 0.165A
Max VDD current: 0.35mA
+3V3_PGA
C36
100nF
+VPGA
C32
1nF
C33
10nF
C34
100nF
C35
1uF
FB8
120@100MHZ
+5V
C132
1uF
TP26
DC_CPL
R126
10K
Q5
DMN62D0UW
DC_CPLn
R125
10K
R127
10K
+5V
-5V
FB9
FB10
120@100MHZ
C111
2.2uF
C133
2.2uF
C37
100nF
C38
2.2uF
C39
100nF
C63
100nF
C64
100nF
C78
100nF
C101
100nF
C102
2.2uF
C108
100nF
C109
100nF
C110
100nF
C124
100nF
C127
100nF
C128
100nF
Before PGA Config: 242mA @ V+, 17.1mA @ V-, 46mA @ 3.3V per channel
After PGA Config: 182mA @ V+, 17.1mA @ V-, 46mA @ 3.3V per channel







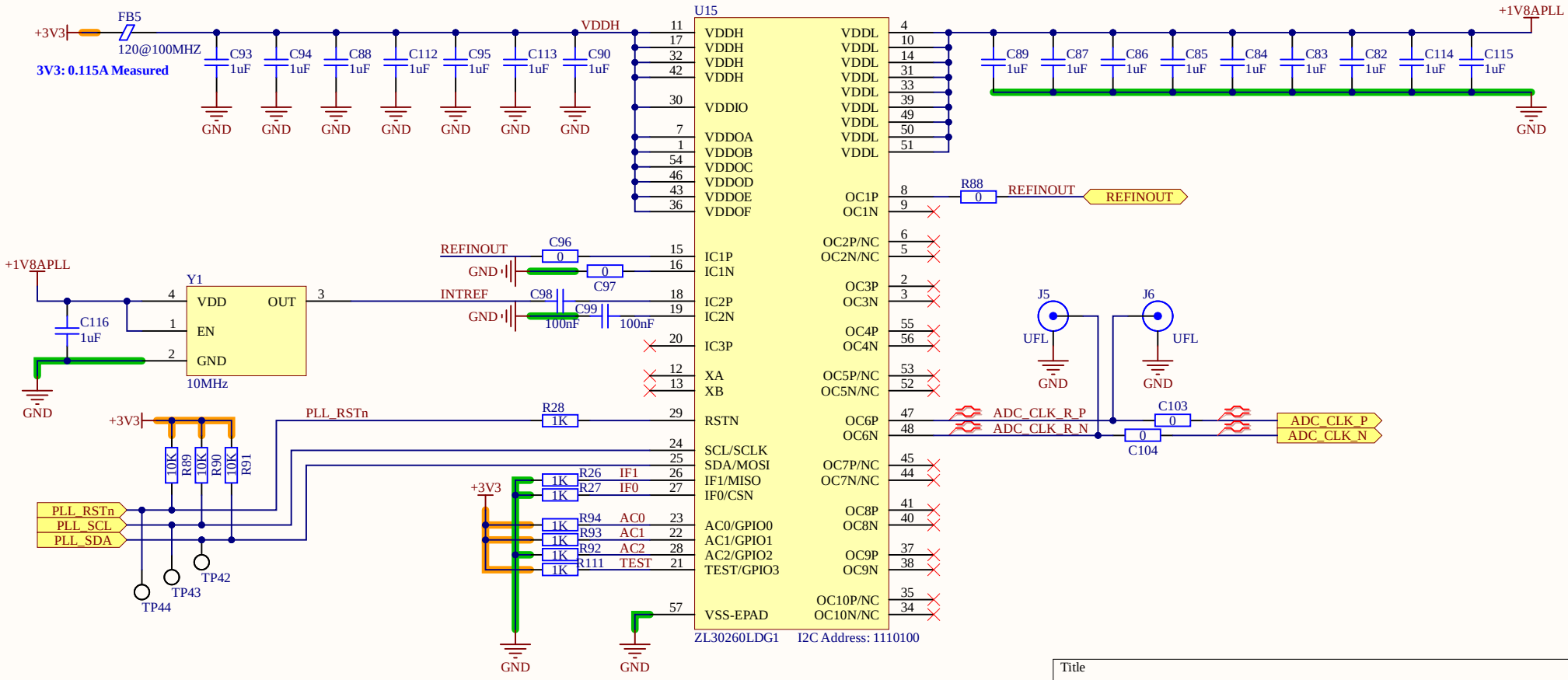


Title		
Size: A4	Number	Revision
Date: 10-15-2024		Sheet of
File: C:\Users\..\FE.SchDoc		Drawn By: Aleksa Bjelogrlic

IF1	IF0	Processor Interface	Configuration Memory to Use
0	0	I²C, slave address 11101 00	Internal ROM
0	1	I²C, slave address 11101 01	Internal ROM
1	0	SPI Slave	Internal ROM
1	1	SPI Master during auto-configuration then SPI Slave	External SPI EEPROM

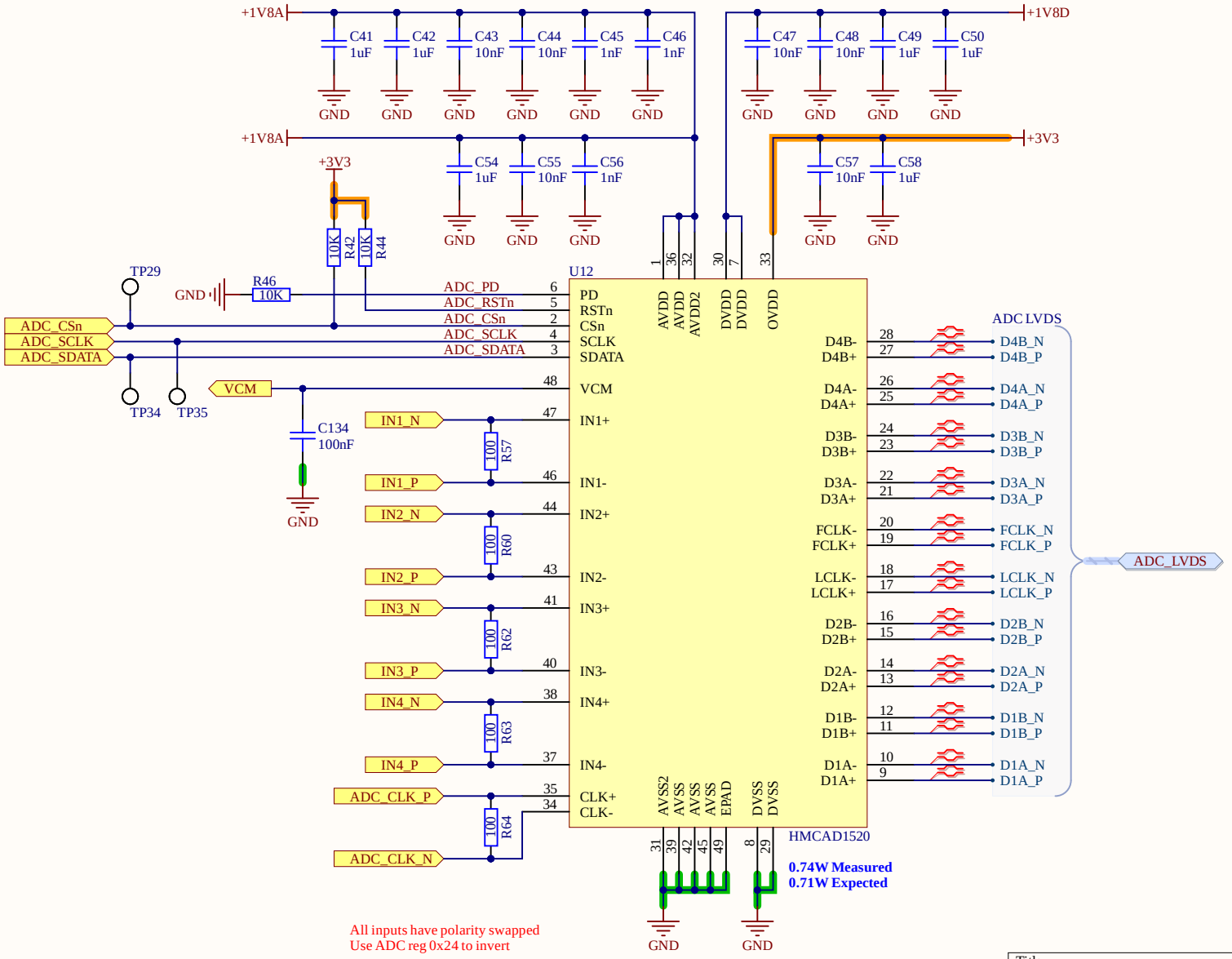
To configure the device as specified in the first three rows above but *without* auto-configuring from internal ROM, wire devices pins as follows: TEST=1 and AC[2:0]=011, as described in section 5.2.

AC2	AC1	AC0	Auto Configuration
0	0	0	Configuration 0
0	0	1	Configuration 1
0	1	0	Configuration 2
0	1	1	Configuration 3
1	0	0	Configuration 4
1	0	1	Configuration 5
1	1	0	Configuration 6
1	1	1	Configuration 7

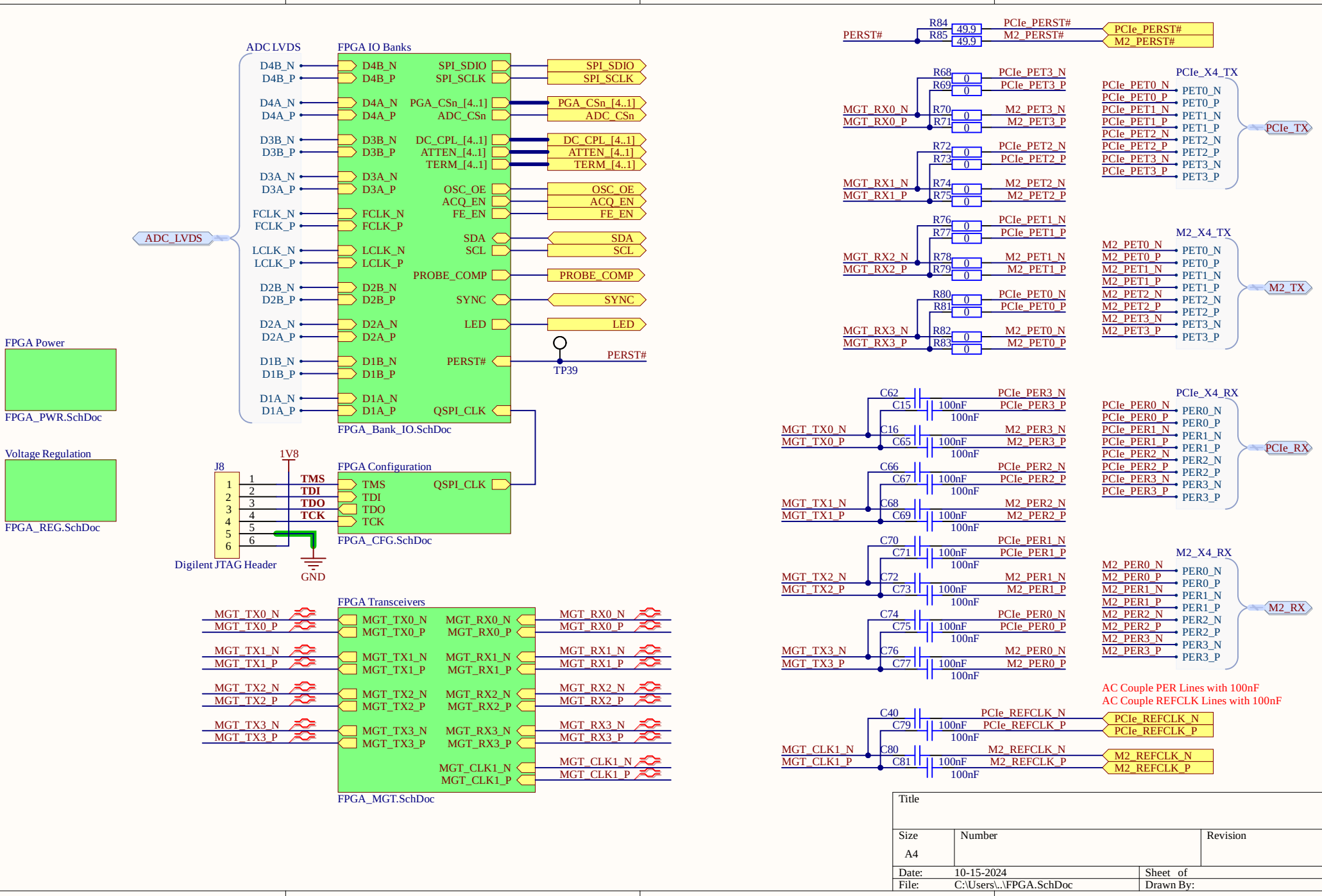


3.3 + 1.8V operation w/ one input one output: 0.67W Expected
0.62W Measured

Title		
Size A4	Number	Revision
Date: 10-15-2024		Sheet of
File: C:\Users\..\PLL.SchDoc		Drawn By:



Title		
Size: A4	Number: ADC.SchDoc	Revision: 1
Date: 10-15-2024		Sheet of
File: C:\Users\..\ADC.SchDoc		Drawn By: Aleksa Bjelogrlic


ADC LVDS
FPGA IO Banks
ADC_LVDS
D4B_N
D4B_P
D4A_N
D4A_P
D3B_N
D3B_P
D3A_N
D3A_P
FCLK_N
FCLK_P
LCLK_N
LCLK_P
D2B_N
D2B_P
D2A_N
D2A_P
D1B_N
D1B_P
D1A_N
D1A_P
SPI_SDIO
SPI_SCLK
PGA_CSn_[4..1]
ADC_CSn
DC_CPL_[4..1]
ATTEN_[4..1]
TERM_[4..1]
OSC_OE
ACQ_EN
FE_EN
SDA
SCL
PROBE_COMP
SYNC
LED
PERST#
QSPI_CLK
TP39
FPGA_Bank_IO.SchDoc
FPGA Power
FPGA_PWR.SchDoc
Voltage Regulation
FPGA_REG.SchDoc
J8
1V8
TMS
TDI
TDO
TCK
Digilent JTAG Header
GND
FPGA Configuration
FPGA_CFG.SchDoc
FPGA Transceivers
MGT_TX0_N
MGT_TX0_P
MGT_TX1_N
MGT_TX1_P
MGT_TX2_N
MGT_TX2_P
MGT_TX3_N
MGT_TX3_P
MGT_RX0_N
MGT_RX0_P
MGT_RX1_N
MGT_RX1_P
MGT_RX2_N
MGT_RX2_P
MGT_RX3_N
MGT_RX3_P
MGT_CLK1_N
MGT_CLK1_P
FPGA_MGT.SchDoc
PERST#
R84
R85
49.9
PCIe_PERST#
M2_PERST#
PCIe_X4_TX
PCIe_TX
M2_X4_TX
M2_TX
PCIe_X4_RX
PCIe_RX
M2_X4_RX
M2_RX
R68
R69
R70
R71
R72
R73
R74
R75
R76
R77
R78
R79
R80
R81
R82
R83
PCIe_PET3_N
PCIe_PET3_P
M2_PET3_N
M2_PET3_P
PCIe_PET2_N
PCIe_PET2_P
M2_PET2_N
M2_PET2_P
PCIe_PET1_N
PCIe_PET1_P
M2_PET1_N
M2_PET1_P
PCIe_PET0_N
PCIe_PET0_P
M2_PET0_N
M2_PET0_P
C62
C15
C16
C65
C66
C67
C68
C69
C70
C71
C72
C73
C74
C75
C76
C77
100nF
PCIe_PER3_N
PCIe_PER3_P
M2_PER3_N
M2_PER3_P
PCIe_PER2_N
PCIe_PER2_P
M2_PER2_N
M2_PER2_P
PCIe_PER1_N
PCIe_PER1_P
M2_PER1_N
M2_PER1_P
PCIe_PER0_N
PCIe_PER0_P
M2_PER0_N
M2_PER0_P
AC Couple PER Lines with 100nF
AC Couple REFCLK Lines with 100nF
C40
C79
C80
C81
PCIe_REFCLK_N
PCIe_REFCLK_P
M2_REFCLK_N
M2_REFCLK_P
Title
Size
A4
Number
Revision
Date:
10-15-2024
Sheet of
File:
C:\Users\..\FPGA.SchDoc
Drawn By:

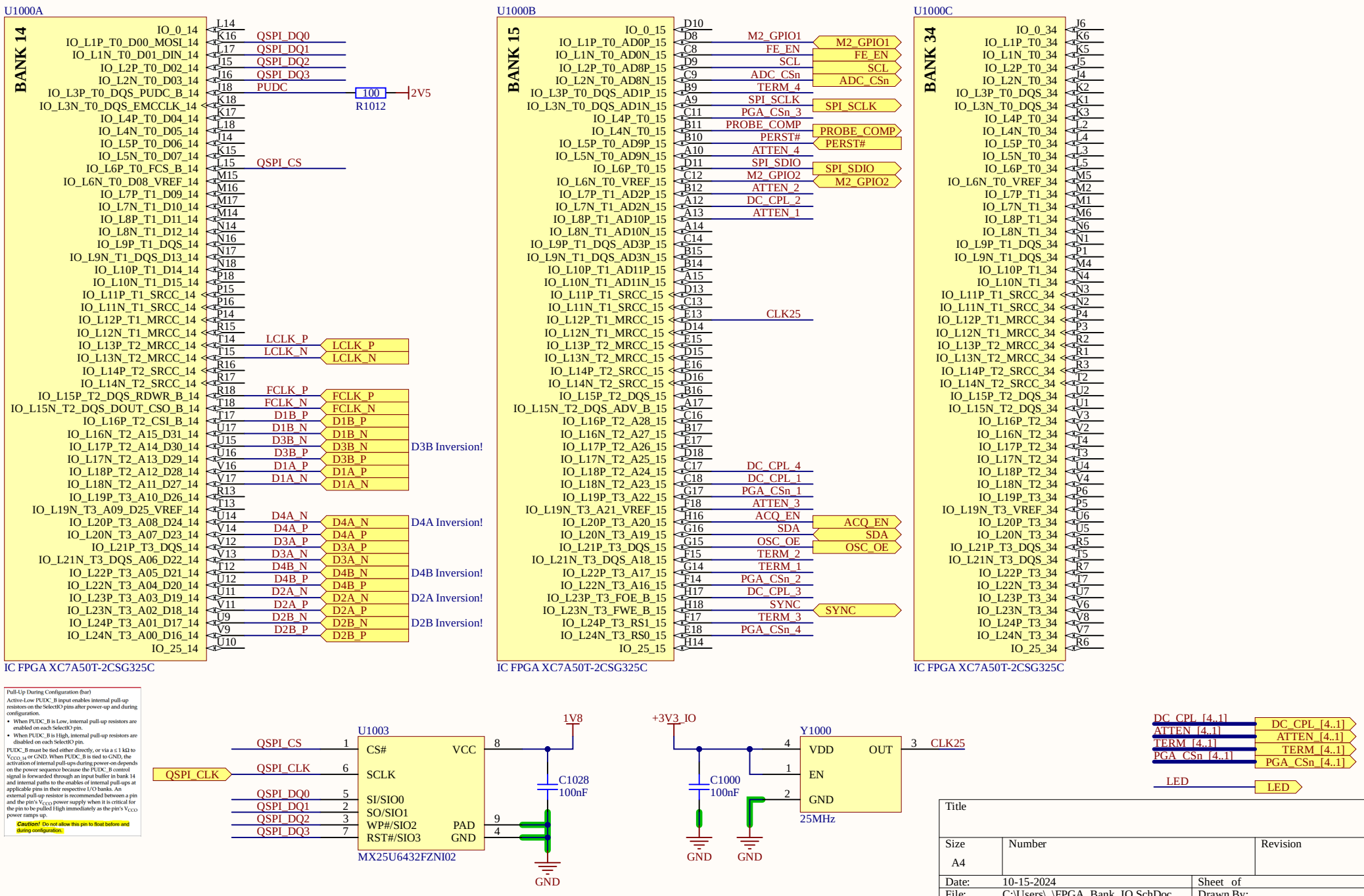

U1000A
BANK 14
IO_0_14
IO_L1P_T0_D00_MOSI_14
IO_L1N_T0_D01_DIN_14
IO_L2P_T0_D02_14
IO_L2N_T0_D03_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L4P_T0_D04_14
IO_L4N_T0_D05_14
IO_L5P_T0_D06_14
IO_L5N_T0_D07_14
IO_L6P_T0_FCS_B_14
IO_L6N_T0_D08_VREF_14
IO_L7P_T1_D09_14
IO_L7N_T1_D10_14
IO_L8P_T1_D11_14
IO_L8N_T1_D12_14
IO_L9P_T1_DQS_14
IO_L9N_T1_DQS_D13_14
IO_L10P_T1_D14_14
IO_L10N_T1_D15_14
IO_L11P_T1_SRCC_14
IO_L11N_T1_SRCC_14
IO_L12P_T1_MRCC_14
IO_L12N_T1_MRCC_14
IO_L13P_T2_MRCC_14
IO_L13N_T2_MRCC_14
IO_L14P_T2_SRCC_14
IO_L14N_T2_SRCC_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L16P_T2_CSI_B_14
IO_L16N_T2_A15_D31_14
IO_L17P_T2_A14_D30_14
IO_L17N_T2_A13_D29_14
IO_L18P_T2_A12_D28_14
IO_L18N_T2_A11_D27_14
IO_L19P_T3_A10_D26_14
IO_L19N_T3_A09_D25_VREF_14
IO_L20P_T3_A08_D24_14
IO_L20N_T3_A07_D23_14
IO_L21P_T3_DQS_14
IO_L21N_T3_DQS_A06_D22_14
IO_L22P_T3_A05_D21_14
IO_L22N_T3_A04_D20_14
IO_L23P_T3_A03_D19_14
IO_L23N_T3_A02_D18_14
IO_L24P_T3_A01_D17_14
IO_L24N_T3_A00_D16_14
IO_25_14
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
PUDC
100
R1012
2V5
QSPI_CS
LCLK_P
LCLK_N
FCLK_P
FCLK_N
D1B_P
D1B_N
D3B_N
D3B_P
D1A_P
D1A_N
D3B Inversion!
D4A_N
D4A_P
D3A_P
D3A_N
D4B_N
D4B_P
D2A_N
D2A_P
D2B_N
D2B_P
D4A Inversion!
D4B Inversion!
D2A Inversion!
D2B Inversion!
IC FPGA XC7A50T-2CSG325C
U1000B
BANK 15
IO_0_15
IO_L1P_T0_AD0P_15
IO_L1N_T0_AD0N_15
IO_L2P_T0_AD8P_15
IO_L2N_T0_AD8N_15
IO_L3P_T0_DQS_AD1P_15
IO_L3N_T0_DQS_AD1N_15
IO_L4P_T0_15
IO_L4N_T0_15
IO_L5P_T0_AD9P_15
IO_L5N_T0_AD9N_15
IO_L6P_T0_15
IO_L6N_T0_VREF_15
IO_L7P_T1_AD2P_15
IO_L7N_T1_AD2N_15
IO_L8P_T1_AD10P_15
IO_L8N_T1_AD10N_15
IO_L9P_T1_DQS_AD3P_15
IO_L9N_T1_DQS_AD3N_15
IO_L10P_T1_AD11P_15
IO_L10N_T1_AD11N_15
IO_L11P_T1_SRCC_15
IO_L11N_T1_SRCC_15
IO_L12P_T1_MRCC_15
IO_L12N_T1_MRCC_15
IO_L13P_T2_MRCC_15
IO_L13N_T2_MRCC_15
IO_L14P_T2_SRCC_15
IO_L14N_T2_SRCC_15
IO_L15P_T2_DQS_15
IO_L15N_T2_DQS_ADV_B_15
IO_L16P_T2_A28_15
IO_L16N_T2_A27_15
IO_L17P_T2_A26_15
IO_L17N_T2_A25_15
IO_L18P_T2_A24_15
IO_L18N_T2_A23_15
IO_L19P_T3_A22_15
IO_L19N_T3_A21_VREF_15
IO_L20P_T3_A20_15
IO_L20N_T3_A19_15
IO_L21P_T3_DQS_15
IO_L21N_T3_DQS_A18_15
IO_L22P_T3_A17_15
IO_L22N_T3_A16_15
IO_L23P_T3_FOE_B_15
IO_L23N_T3_FWE_B_15
IO_L24P_T3_RS1_15
IO_L24N_T3_RS0_15
IO_25_15
M2_GPIO1
FE_EN
SCL
ADC_CSn
TERM_4
SPI_SCLK
PGA_CSn_3
PROBE_COMP
PERST#
ATTEN_4
SPI_SDIO
M2_GPIO2
ATTEN_2
DC_CPL_2
ATTEN_1
CLK25
DC_CPL_4
DC_CPL_1
PGA_CSn_1
ATTEN_3
ACQ_EN
SDA
OSC_OE
TERM_2
TERM_1
PGA_CSn_2
DC_CPL_3
SYNC
TERM_3
PGA_CSn_4
IC FPGA XC7A50T-2CSG325C
U1000C
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
IC FPGA XC7A50T-2CSG325C
Pull-Up During Configuration (bar)
Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration.
When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin.
When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin.
PUDC_B must be tied either directly, or via a ≤ 1 kΩ to VCCO_14 or GND. When PUDC_B is tied to GND, the activation of internal pull-ups during power-on depends on the power sequence because the PUDC_B control signal is forwarded through an input buffer in bank 14 and internal paths to the enables of internal pull-ups at applicable pins in their respective I/O banks. An external pull-up resistor is recommended between a pin and the pin's VCCO power supply when it is critical for the pin to be pulled High immediately as the pin's VCCO power ramps up.
Caution! Do not allow this pin to float before and during configuration.
U1003
QSPI_CS
QSPI_CLK
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
CS#
SCLK
SI/SIO0
SO/SIO1
WP#/SIO2
RST#/SIO3
VCC
PAD
GND
MX25U6432FZNI02
1V8
C1028
100nF
GND
+3V3_IO
Y1000
VDD
EN
GND
OUT
CLK25
25MHz
C1000
100nF
GND
GND
DC_CPL_[4..1]
ATTEN_[4..1]
TERM_[4..1]
PGA_CSn_[4..1]
LED
Title
Size
A4
Number
Revision
Date:
10-15-2024
Sheet of
File:
C:\Users\..\FPGA_Bank_IO.SchDoc
Drawn By:

Table 2-1: **7 Series FPGA Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

M[2:0] = 001

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

Note: DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and

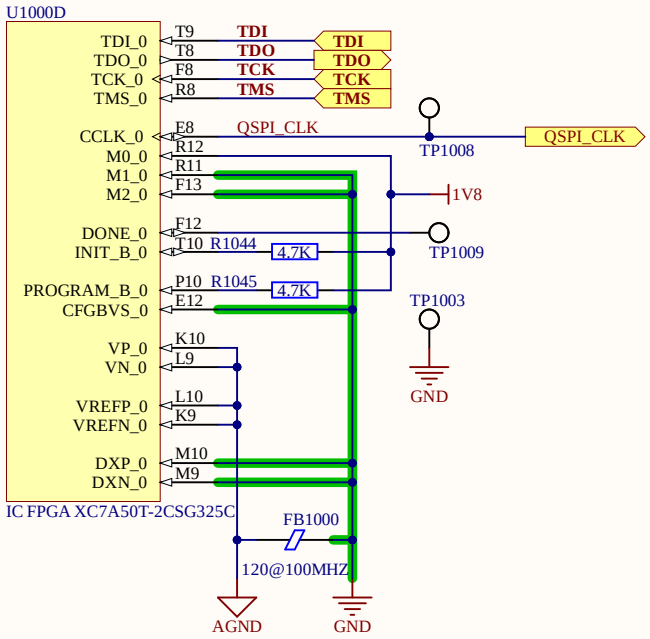


Table 2-6: **Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection**

Configuration Mode	Banks Used	Configuration Interface I/O Voltage	HR Bank 0 V_{CCO_0}	HR Bank 14 V_{CCO_14}	HR Bank 15 V_{CCO_15}	CFGBVS
JTAG (only)	0	3.3V	3.3V	Any	Any	VCCO_0
		2.5V	2.5V	Any	Any	VCCO_0
		1.8V	1.8V	Any	Any	GND
		1.5V	1.5V	Any	Any	GND
Serial, SPI, or SelectMAP	0, 14(1)	3.3V	3.3V	3.3V	Any	VCCO_0
		2.5V	2.5V	2.5V	Any	VCCO_0
		1.8V	1.8V	1.8V	Any	GND
		1.5V	1.5V	1.5V	Any	GND
BPI(2)	0, 14, 15	3.3V	3.3V	3.3V	3.3V	VCCO_0
		2.5V	2.5V	2.5V	2.5V	VCCO_0
		1.8V	1.8V	1.8V	1.8V	GND
		1.5V	1.5V	1.5V	1.5V	GND

Notes:
1. RS[1:0] for MultiBoot or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.
2. BPI mode is not available in the Spartan-7 family.

Title		
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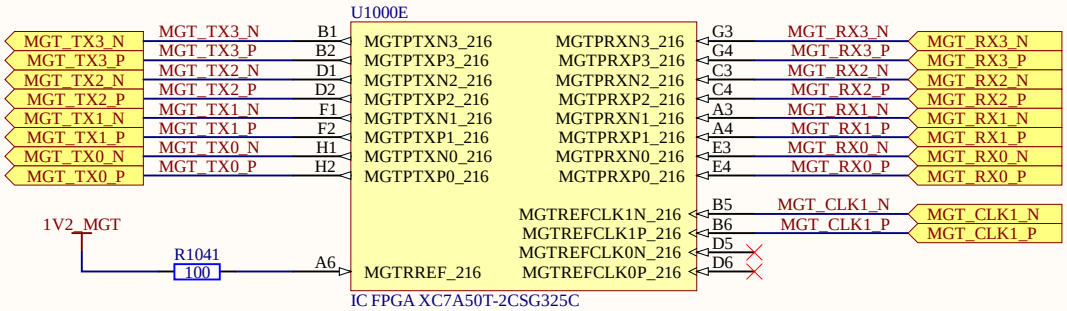

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Package	Device	V_{CCINT}						V_{CCBRAM}				V_{CCAUX}			V_{CCO} Bank 0	V_{CCO} all other Banks (per Bank)		
		680 µF	330 µF	100 µF	47 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF	47 µF or 100 µF[3]	4.7 µF	0.47 µF
CSG325	XC7A35T XA7A35T	0	0	1	0	2	3	0	1	0	1	1	2	3	1	1	2	4

3. One 47 µF (or 100 µF) capacitor is required for up to four V_{CCO} banks when powered by the same voltage.

+3V3_IO

U1000G

C1029 47uF, C1030 4.7uF, C1031 4.7uF, C1032 470nF, C1033 470nF, C1034 470nF, C1035 470nF

V5, T1, R4, P7, M3, L6 — VCCO_34

H15, G18, E14, D17, C10 — VCCO_15

B13, A16 — VCCO_15

V15, U18, U8, T11, R14, P17, L16 — VCCO_14

R10, E10 — VCCO_0

1V35

C1036 470nF, C1037 470nF, C1038 470nF, C1039 470nF, C1040 4.7uF, C1041 4.7uF

1V35

C1042 47uF, C1043 4.7uF, C1044 4.7uF, C1045 470nF, C1046 470nF, C1047 470nF, C1048 470nF

1V8

C1049 47uF

IC FPGA XC7A50T-2CSG325C

U1000H

1V0

C1050 47uF, C1051 470nF

H11, G10, F11 — VCCBRAM

P11, P9, N12, N10, N8, M11, M7, L12, L8, K11, K7, J12, J8, H9, H7, G8, F9, F7 — VCCINT

C1052 470nF, C1053 470nF, C1054 470nF, C1055 4.7uF, C1056 4.7uF, C1057 100uF

1V0

1V8

C1058 47uF, C1059 4.7uF, C1060 4.7uF, C1061 470nF, C1062 470nF, C1063 470nF

P13, M13, K13, H13, G12 — VCCAUX

FB1001 120@100MHZ

J10 — VCCADC_0

E11 — VCCBATT_0

C1064 470nF

AGND

IC FPGA XC7A50T-2CSG325C

U1000I

J9 — GNDADC_0

AGND

V18, V10, V1, U13, U3, T16, T6, R9, P12, P8, P2, N15, N13, N11, N9, N7, N5, M18, M12, M8, L13, L11, L7, L1, K14, K12, K8, K4, J17, J13, J11, J7, J3, J2, J1, H12, H10 — GND

H8, H6, H5, H4, H3, G13, G11, G9, G7, G6, G5, G1, F16, F10, F6, F4, E9, E7, E6, E2, D12, D7, D4, D3, C15, C7, C6, C2, B18, B8, B7, B3, A18, A11, A8, A7, A5, A1 — GND

IC FPGA XC7A50T-2CSG325C

1V2_MGT

U1000F

C1065 4.7uF, C1066 100nF, C1067 100nF

G2, F3, E1, C1, A2 — MGTAVTT

F5, E5, C5, B4 — MGTAVCC

C1068 100nF, C1069 100nF, C1070 4.7uF

1V0_MGT

FB1002 120@100MHZ

1V0

IC FPGA XC7A50T-2CSG325C

Qty/Power Supply Group		Capacitance (µF)	Tolerance	Type
MGTAVCC	MGTAVTT			
1	1	4.7	10%	Ceramic
2	2	0.1	10%	Ceramic

Capacitor	Package Pins			Value
	MGTAVCC	MGTAVTT	GND	
Cap1		F3	F4	0.1 µF
Cap2		A2	A1	
Cap3	B4		B3	
Cap4	F5		F6	

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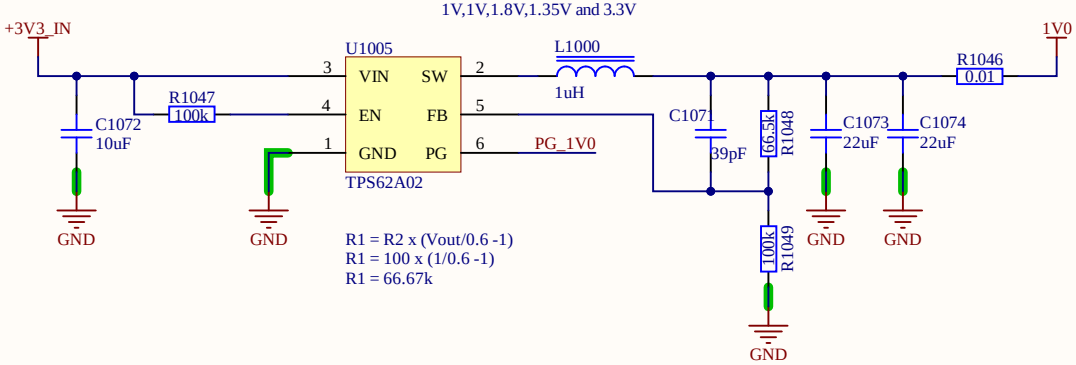
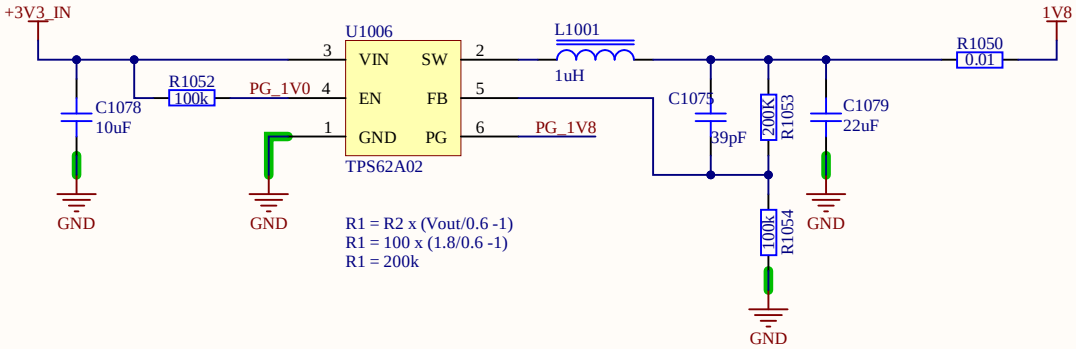
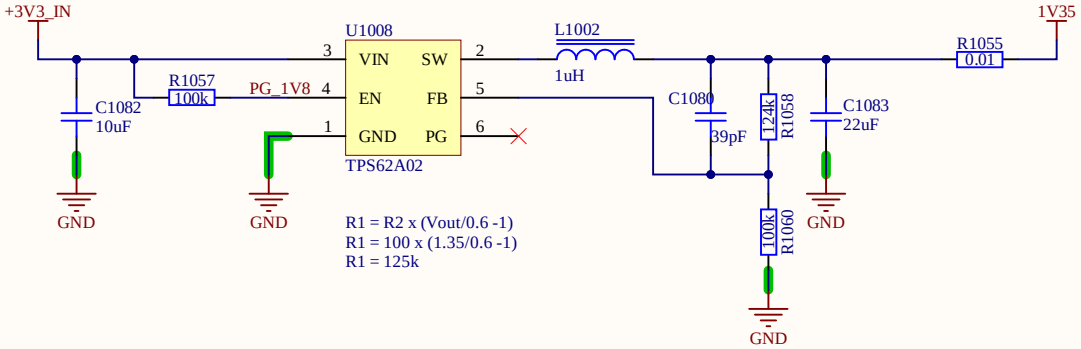
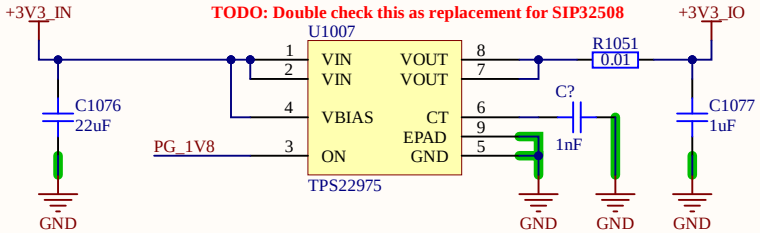
The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,1.35V and 3.3V



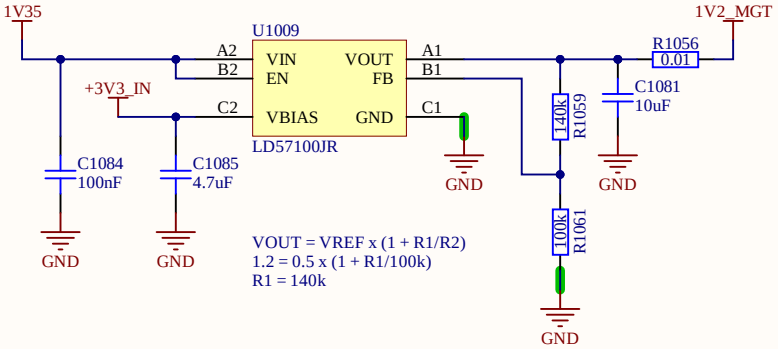




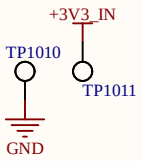
3V3: 0.927A (3.06W) for 3V relays

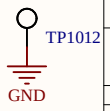


3V3: 0.703A (2.32W) for 4.5V relays



The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT
1V,1V,1.2V





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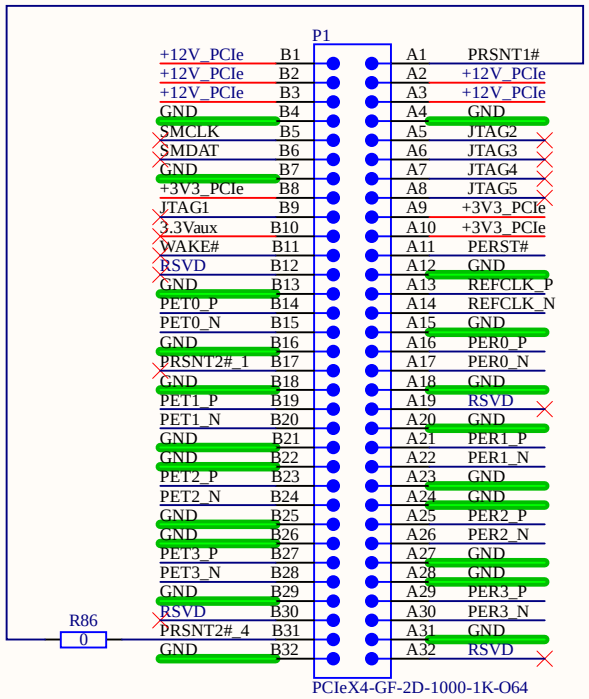
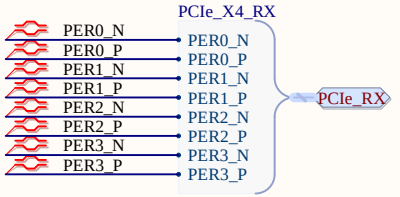
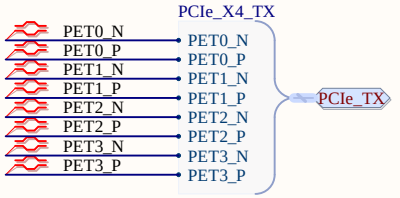
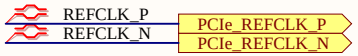
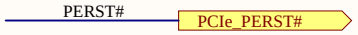
- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

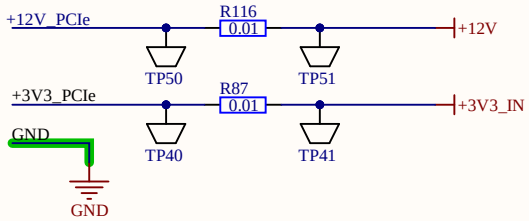












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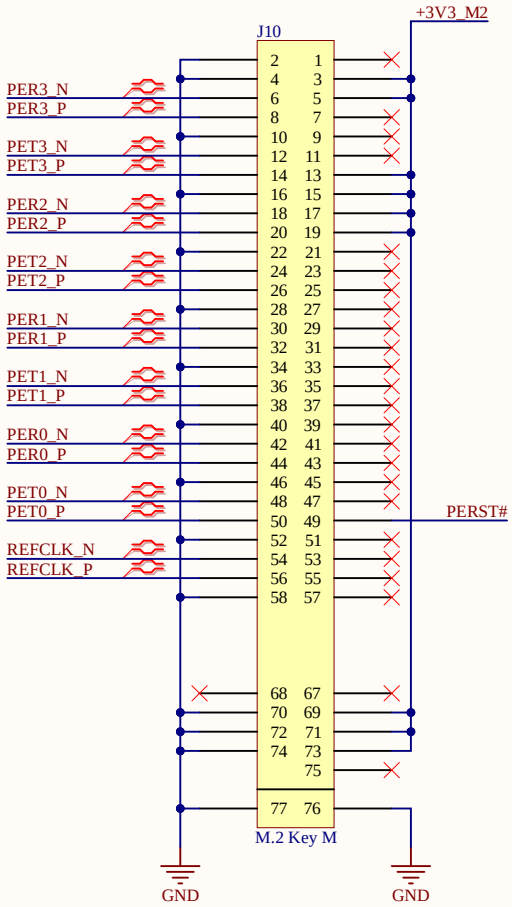
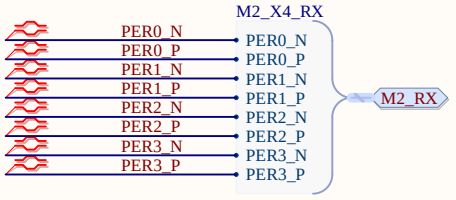
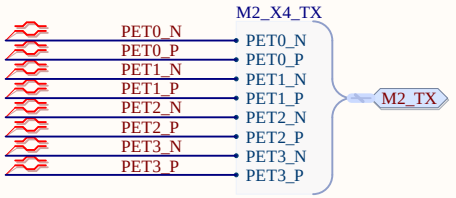
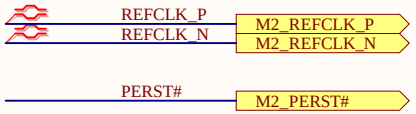
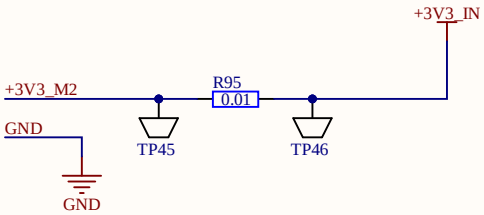
Main Board
Custom Pinout











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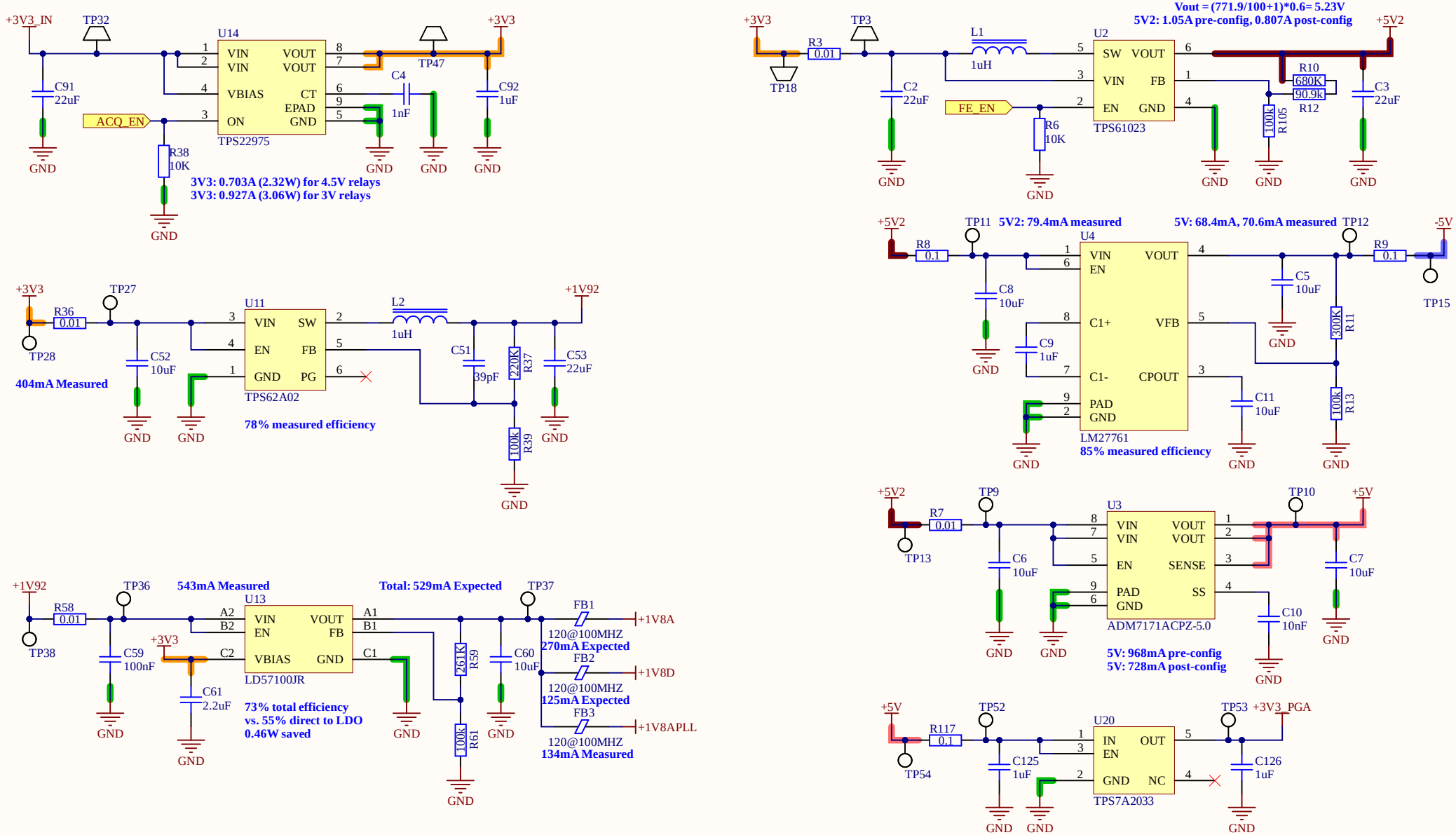
+3V3_IN
TP32
U14
VIN
VIN
VBIAS
ON
VOUT
VOUT
CT
EPAD
GND
TPS22975
TP47
+3V3
C91
22uF
C4
1nF
C92
1uF
ACQ_EN
R38
10K
GND
3V3: 0.703A (2.32W) for 4.5V relays
3V3: 0.927A (3.06W) for 3V relays
+3V3
TP27
R36
0.01
TP28
U11
VIN
EN
GND
SW
FB
PG
TPS62A02
L2
1uH
C52
10uF
C51
39pF
220K
R37
100k
R39
C53
22uF
+1V92
404mA Measured
78% measured efficiency
+1V92
TP36
543mA Measured
Total: 529mA Expected
TP37
R58
0.01
TP38
U13
VIN
EN
VBIAS
VOUT
FB
GND
LD57100JR
C59
100nF
C61
2.2uF
C60
10uF
261K
R59
100K
R61
FB1
120@100MHZ
270mA Expected
+1V8A
FB2
120@100MHZ
125mA Expected
+1V8D
FB3
120@100MHZ
134mA Measured
+1V8APLL
73% total efficiency
vs. 55% direct to LDO
0.46W saved
5V2: 1.05A (5.46W) pre-config, 0.807A (4.20W) post-config
3V3: 0.184A (0.61W) for 4.5V relays
3V3: 0.408A (1.35W) for 3V relays
0.74W saved
Vout = (771.9/100+1)*0.6= 5.23V
5V2: 1.05A pre-config, 0.807A post-config
+3V3
TP3
R3
0.01
TP18
L1
1uH
U2
SW
VIN
EN
VOUT
FB
GND
TPS61023
+5V2
C2
22uF
FE_EN
R6
10K
R10
680K
90.9k
R12
100k
R105
C3
22uF
+5V2
TP11
5V2: 79.4mA measured
5V: 68.4mA, 70.6mA measured
TP12
-5V
R8
0.1
U4
VIN
EN
C1+
C1-
PAD
GND
VOUT
VFB
CPOUT
LM27761
C8
10uF
C9
1uF
C5
10uF
C11
10uF
R9
0.1
TP15
300K
R11
100k
R13
85% measured efficiency
+5V2
TP9
R7
0.01
TP13
U3
VIN
VIN
EN
PAD
GND
VOUT
VOUT
SENSE
SS
ADM7171ACPZ-5.0
TP10
+5V
C6
10uF
C7
10uF
C10
10nF
5V: 968mA pre-config
5V: 728mA post-config
+5V
TP52
R117
0.1
TP54
U20
IN
EN
GND
OUT
NC
TPS7A2033
TP53
+3V3_PGA
C125
1uF
C126
1uF
GND
Title
Size
A4
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Revision
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