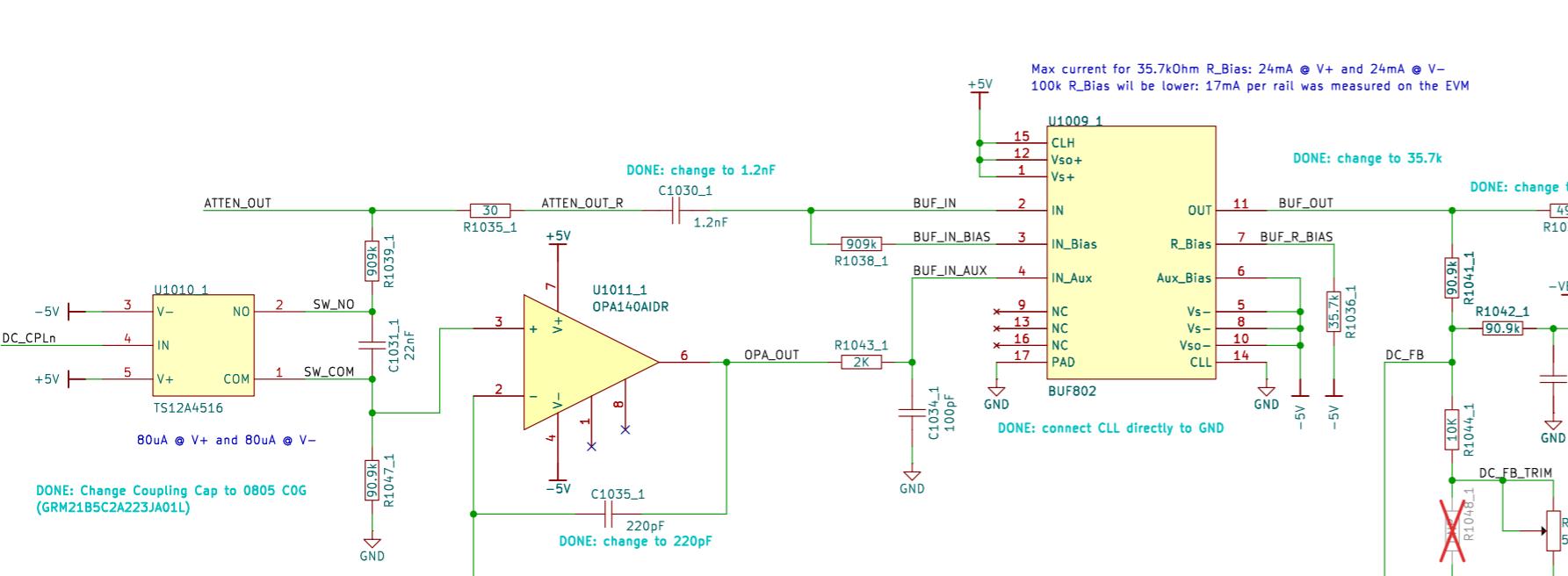
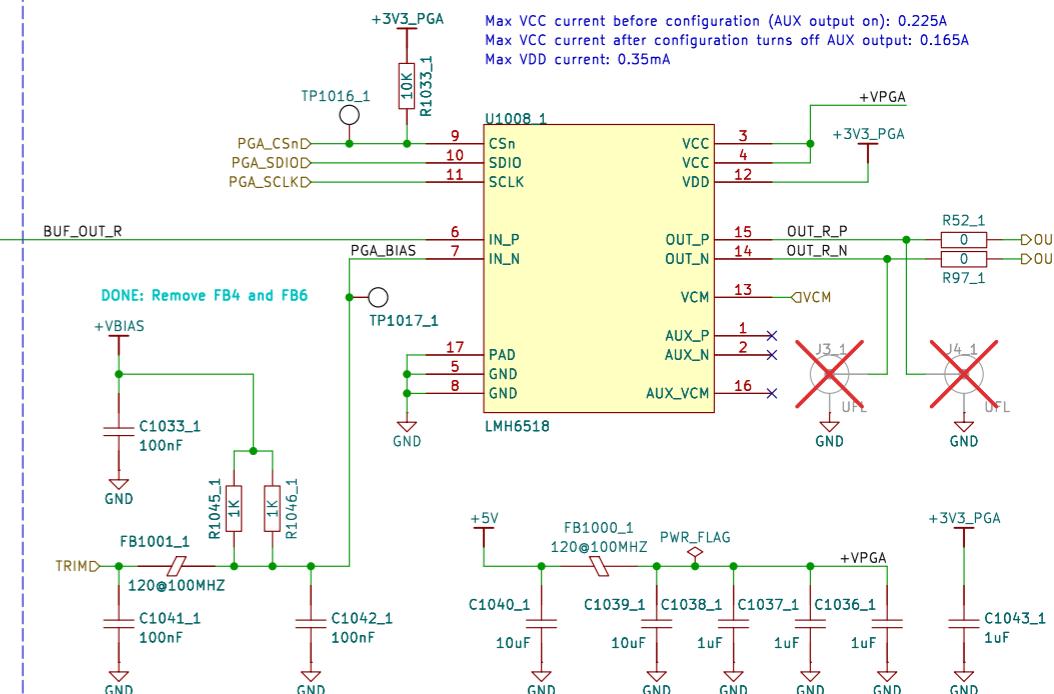


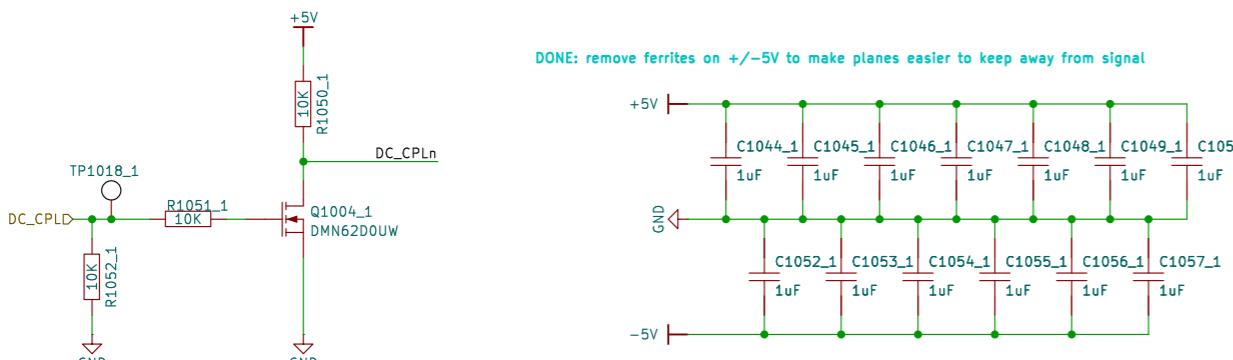
Input Buffer and AC/DC Coupling



Programmable Gain Amplifier



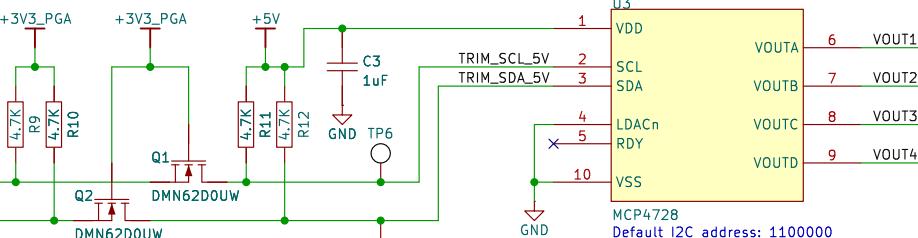
DONE: Revert to Mechanical Trimpot



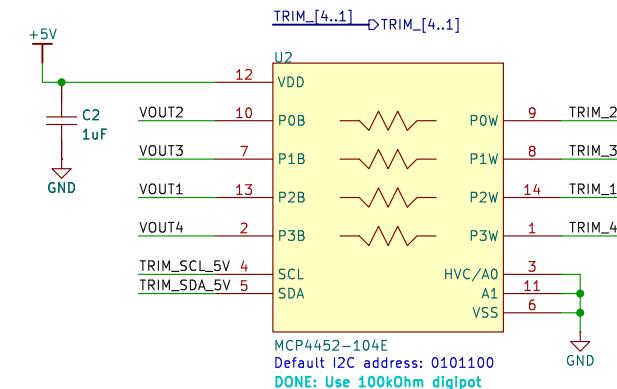
1 2 3 4 5 6

Offset Voltage Trim and User Offset Control

A

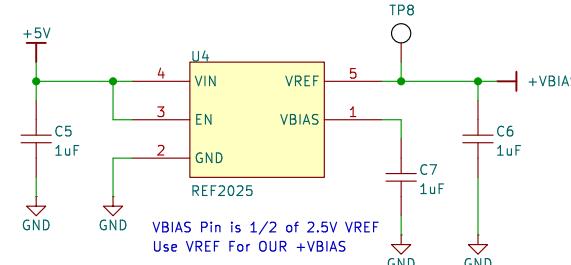


B



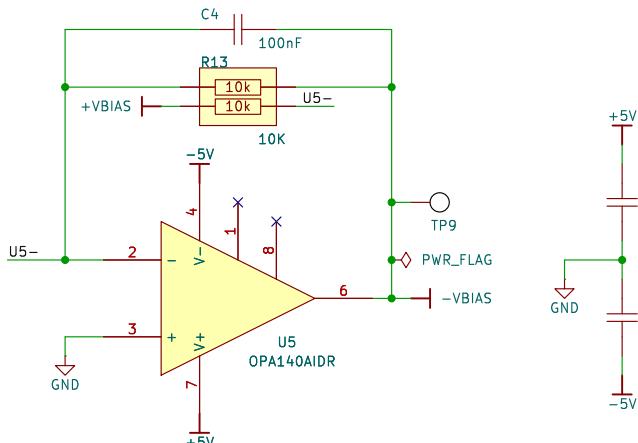
Bias Voltage Generation

C



D

Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140
-Max resistance is $(575/4 // 10k) = 141.7 \text{ Ohm}$
-Worst case current is 17.64mA
-Use REF2025, has max current of 20mA
-Change U5 divider to matched resistor network
-ACASN1002S1002P1AT



EEVengers

Sheet: /Front End Trim and Bias/
File: FE.kicad_sch

Title: ThunderScope

Size: A4 Date:

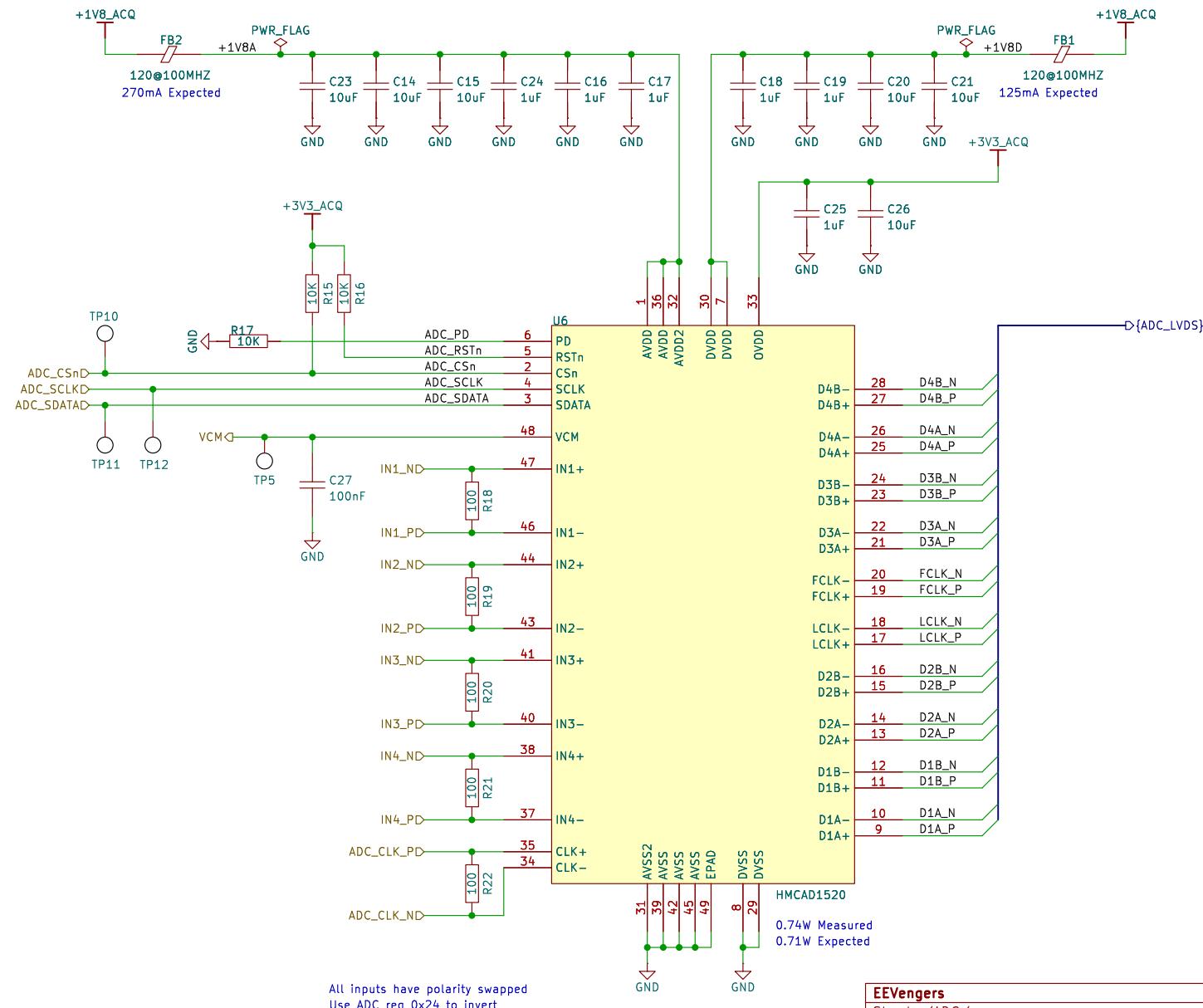
KiCad E.D.A. 9.0.0

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 3/16

1 2 3 4 5 6

1 2 3 4 5 6

ADC

EEVengers

Sheet: /ADC/
File: ADC.kicad_sch

Drawn by: Aleksa Bjelogrlic

Title: ThunderScope

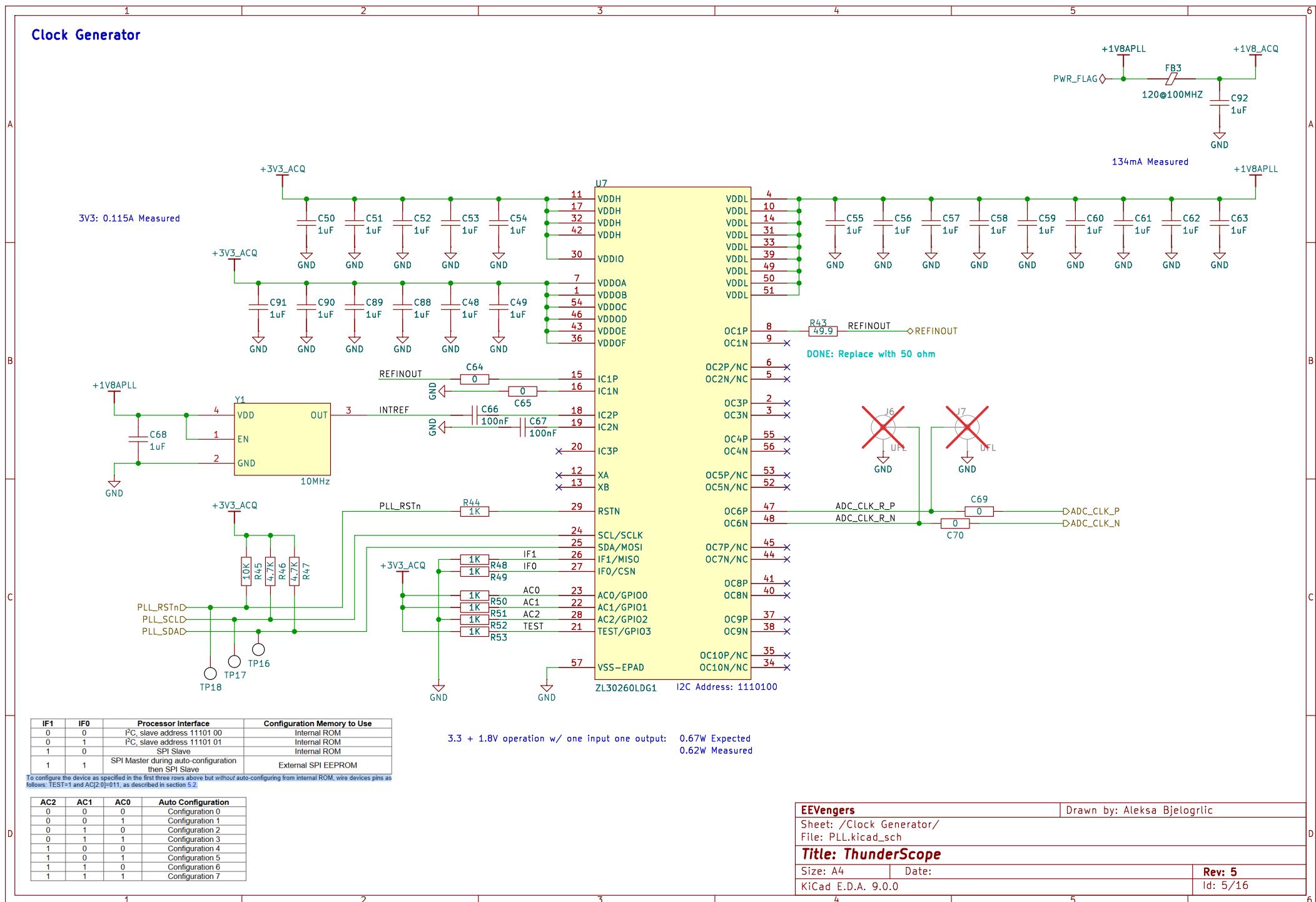
Size: A4 Date:

KiCad E.D.A. 9.0.0

Rev: 5

Id: 4/16

1 2 3 4 5 6



Processor Interface	Configuration Memory to Use
0 0	I ² C, slave address 1110100
0 1	I ² C, slave address 1110101
1 0	SPI Slave
1 1	SPI Master during auto-configuration then SPI Slave
	External SPI EEPROM

To configure the device as specified in the first three rows above but without auto-configuring from internal ROM, wire devices pins as follows: TEST=1 and AC[2:0]=011, as described in section 5.2.

AC2	AC1	AC0	Auto Configuration
0	0	0	Configuration 0
0	0	1	Configuration 1
0	1	0	Configuration 2
0	1	1	Configuration 3
1	0	0	Configuration 4
1	0	1	Configuration 5
1	1	0	Configuration 6
1	1	1	Configuration 7

3.3 + 1.8V operation w/ one input one output: 0.67W Expected
0.62W Measured

EEVengers

Sheet: /Clock Generator/
File: PLL.kicad_sch

Title: ThunderScope

Size: A4 Date:

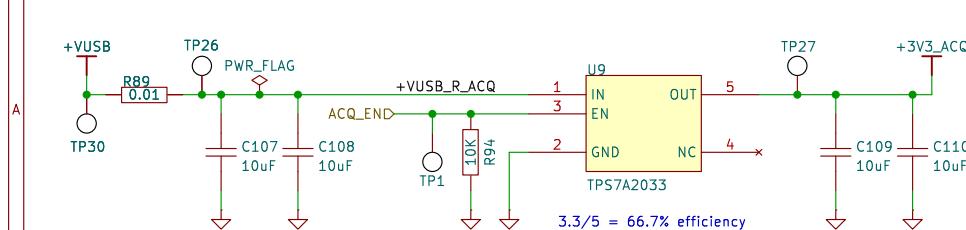
KiCad E.D.A. 9.0.0

Drawn by: Aleksa Bjelogrlic

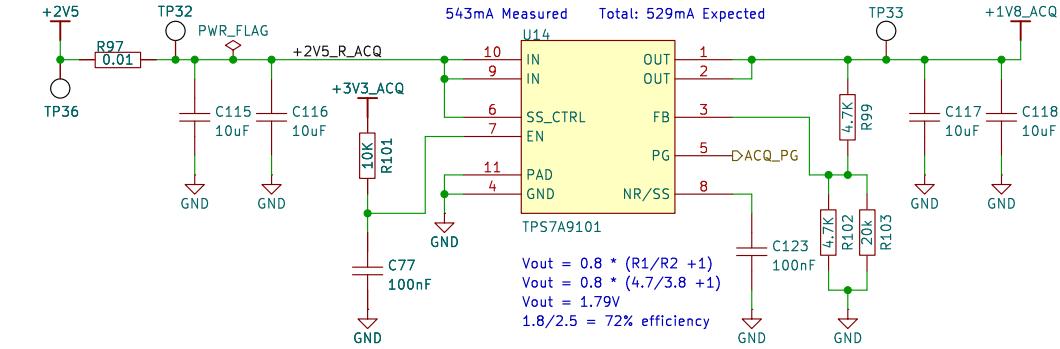
Rev: 5

Id: 5/16

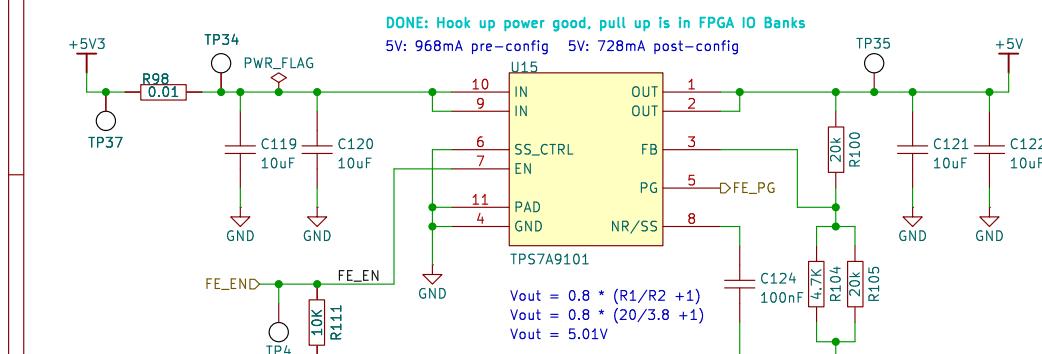
Acquisition Voltage Regulators



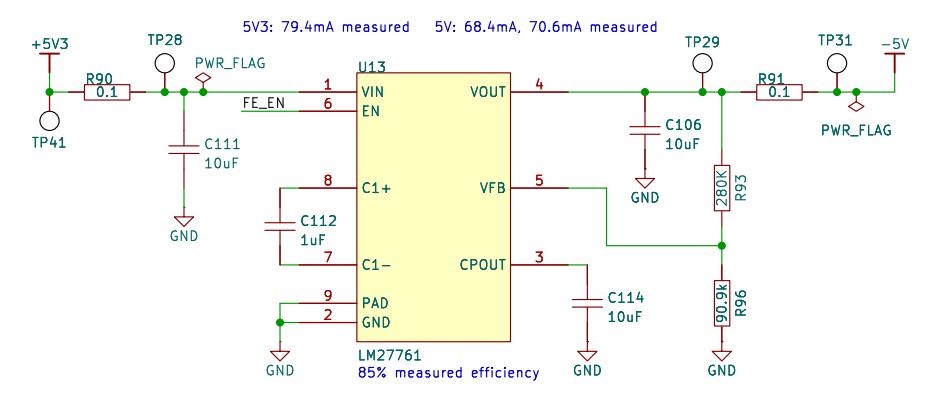
DONE: Hook up power good, pull up is in FPGA IO Banks



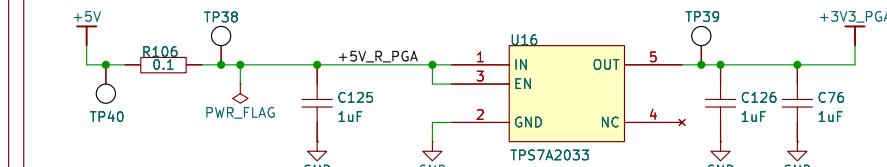
Front End Voltage Regulators



6ms soft start time on previous LDO, need same or greater
 $T_{ss} = (V_{REF} \times C_{nr/ss}) / I_{nr/ss}$
 $T_{ss} = (0.8 \times 100nF) / 6.2\mu A$ [for SS_CTRL = GND]
 $T_{ss} = 0.0129s = 13ms$



$V_{out} = -1.22V(R_1+R_2)/R_2$
 $V_{out} = -1.22 \times (280/90.9+1) = -4.98V$
The value for R2 must be no less than 50 kΩ.



EEVengers

Sheet: /ACQ and FE Voltage Regs/
File: ACQ_FE_VREG.kicad_sch

Title: ThunderScope

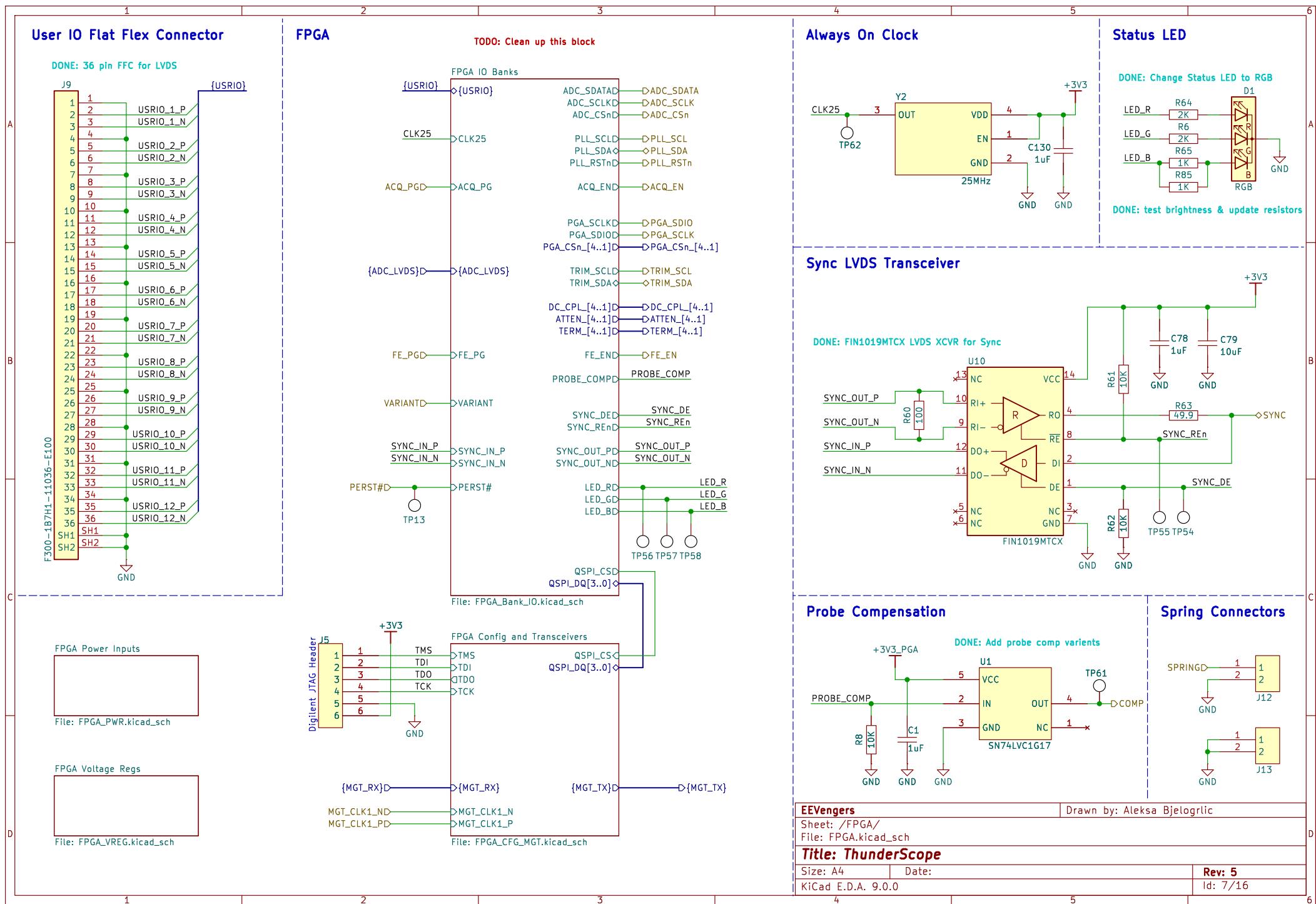
Size: A4 Date:

KiCad E.D.A. 9.0.0

Drawn by: Aleksa Bjelogrlic

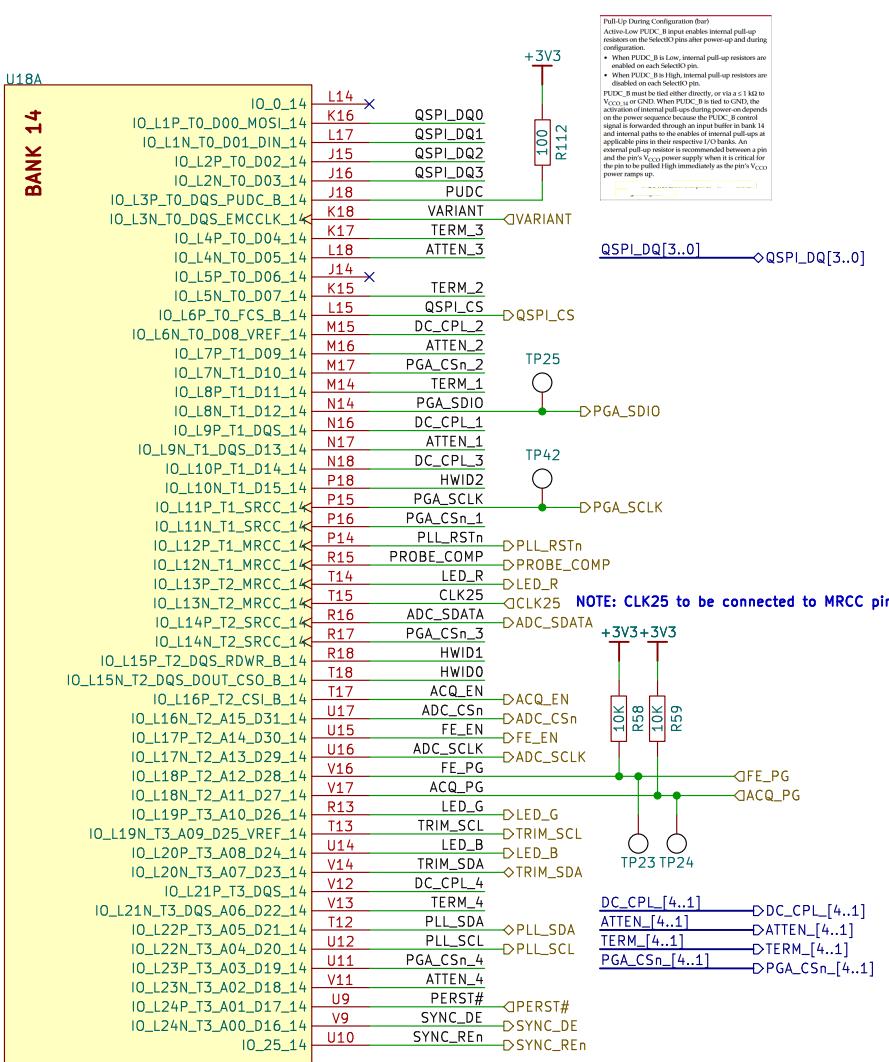
Rev: 5

Id: 6/16



FPGA IO Banks

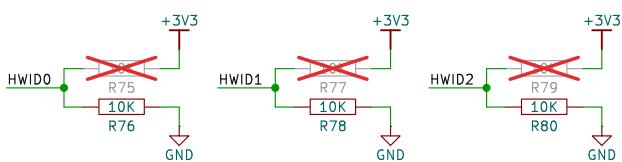
A



B

C

D

**EEVengers**

Sheet: /FPGA/FPGA IO Banks/
File: FPGA_Bank_IO.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 9.0.0

Drawn by: Aleksa Bjelogrlic

Rev: 5

Id: 8/16

FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

Note: DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and

Table 2-1: 7 Series FPGA Configuration Modes				
Configuration Mode	M2[0]	Bus Width	CCLK Direction	
Master SPI	001	x1, x2, x4	Output	

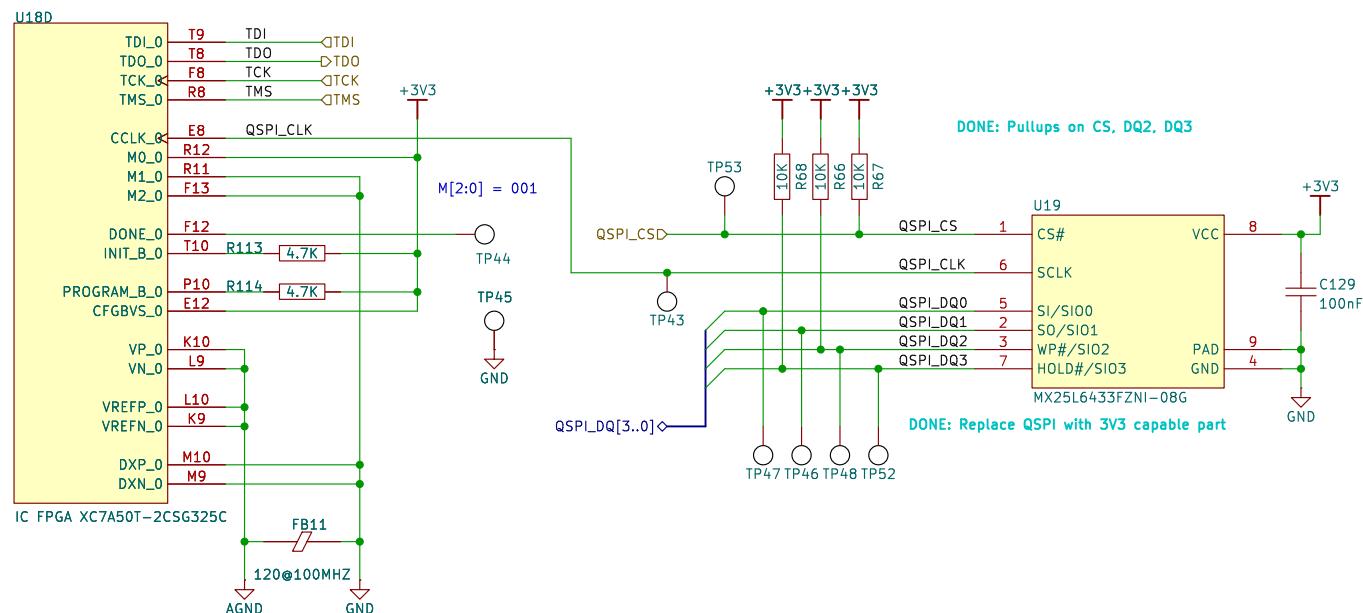
Table 2-2: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Bank Used	Configuration Interface I/O	HR Bank 0 V _{CCO} 0	HR Bank 14 V _{CCO} 14	HR Bank 15 V _{CCO} 15	CFGBVS
JTAG (only)	0	VREFP_0	3.3V	3.3V	Any	VCCO_0
		VREFN_0	2.5V	2.5V	Any	VCCO_0
		VREFP_0	1.8V	1.8V	Any	GND
		VREFN_0	1.5V	1.5V	Any	GND
Serial SPI or SelectMAP	0, 14 ⁽¹⁾	DXP_0	3.3V	3.3V	3.3V	VCCO_0
		DXP_0	2.5V	2.5V	2.5V	VCCO_0
		DXN_0	1.8V	1.8V	1.8V	GND
		DXN_0	1.5V	1.5V	1.5V	GND
BPI ⁽²⁾	0, 14, 15	VREFP_0	3.3V	3.3V	3.3V	VCCO_0
		VREFN_0	2.5V	2.5V	2.5V	VCCO_0
		VREFP_0	1.8V	1.8V	1.8V	GND
		VREFN_0	1.5V	1.5V	1.5V	GND

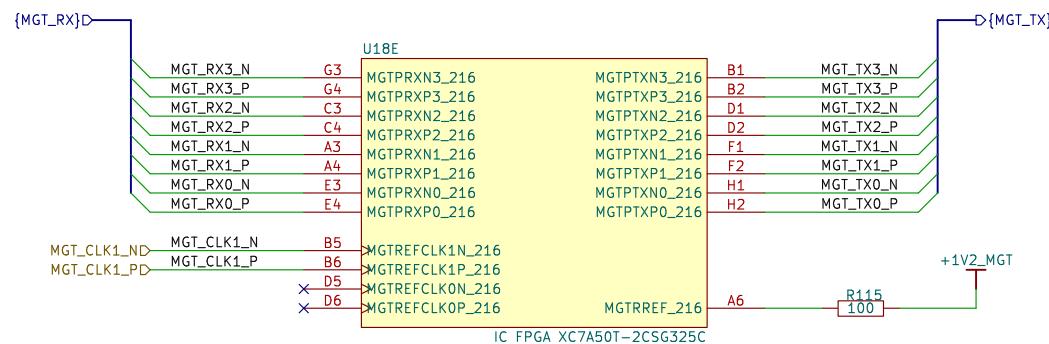
Notes:

1. RS1 of Multiflash or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.

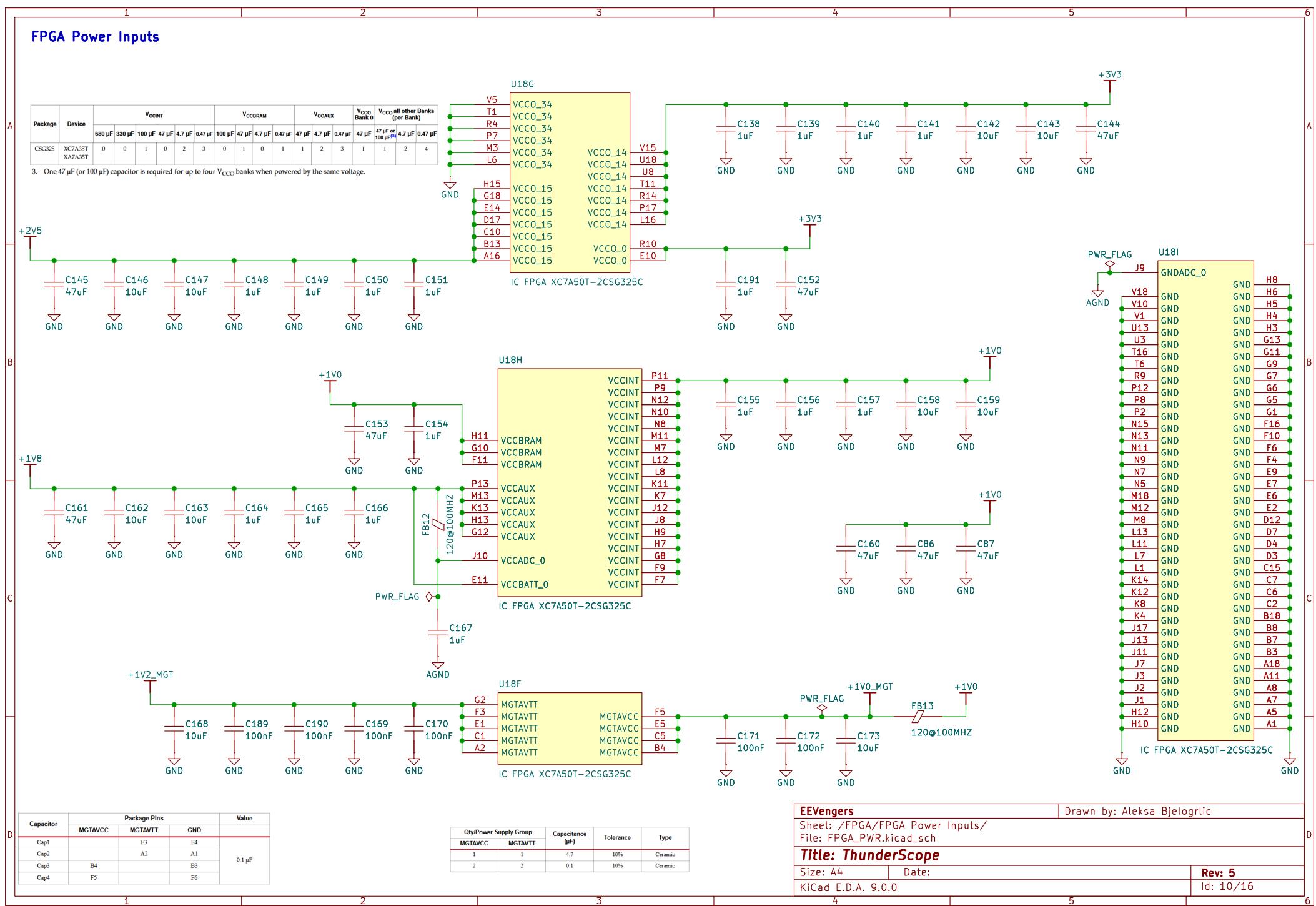
2. BPI mode is not available in the Spartan-7 family.



FPGA Transceivers



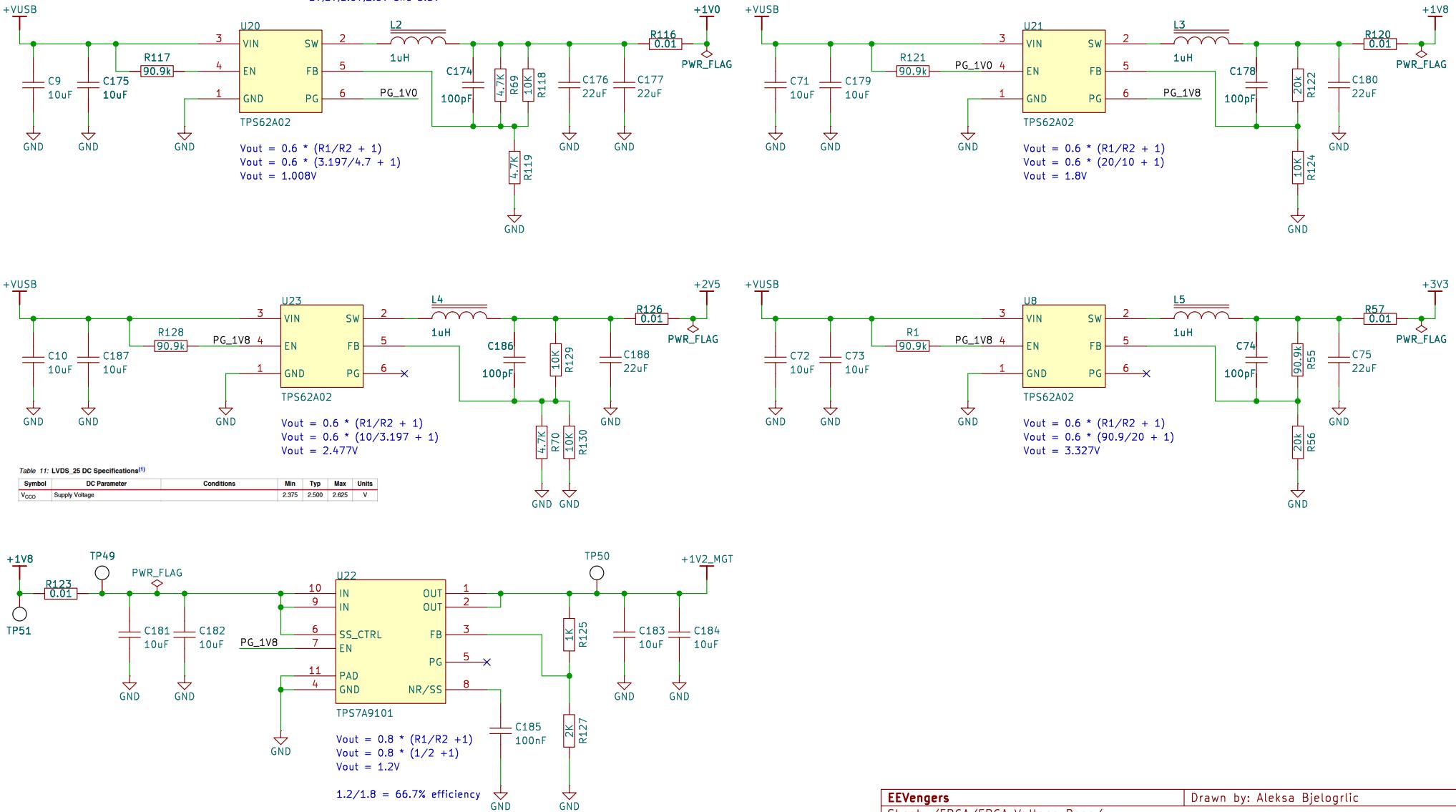
PAGE 1: FPGA Power Inputs



1 2 3 4 5 6

FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V



EEVengers

Sheet: /FPGA/FPGA Voltage Regs/
File: FPGA_VREG.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 9.0.0

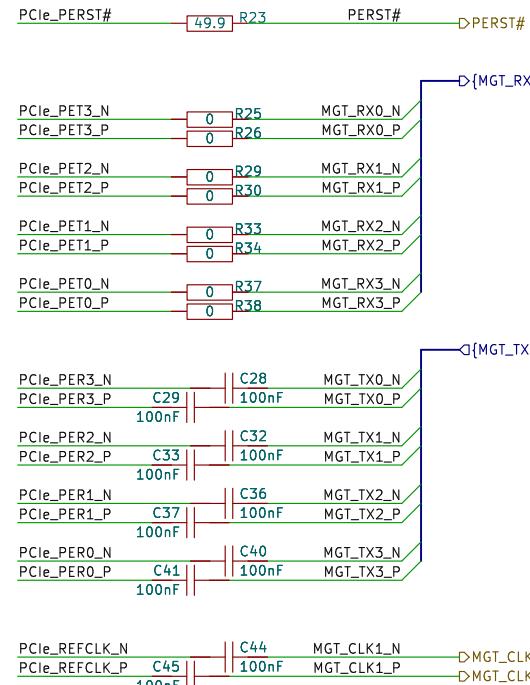
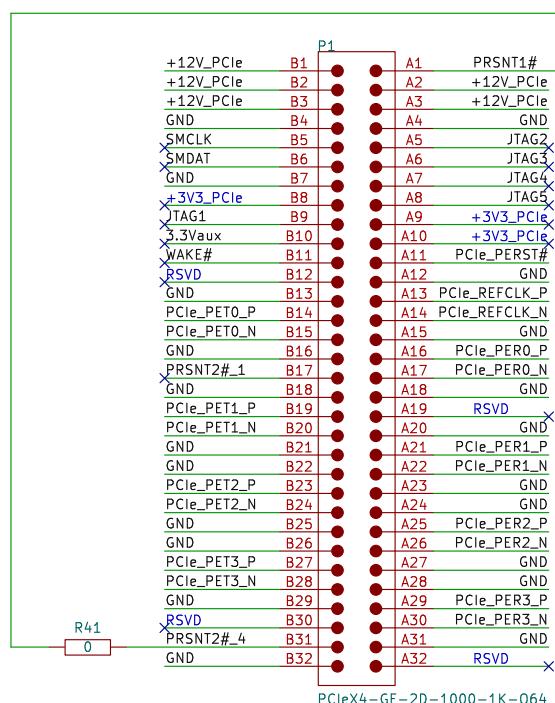
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Rev: 5
Id: 11/16

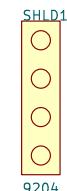
1 2 3 4 5 6

1 2 3 4 5 6

PCIe x4 Edge Connector



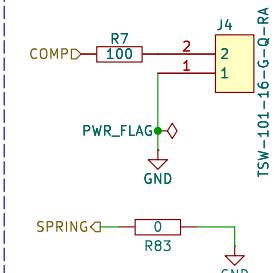
PCIe bracket



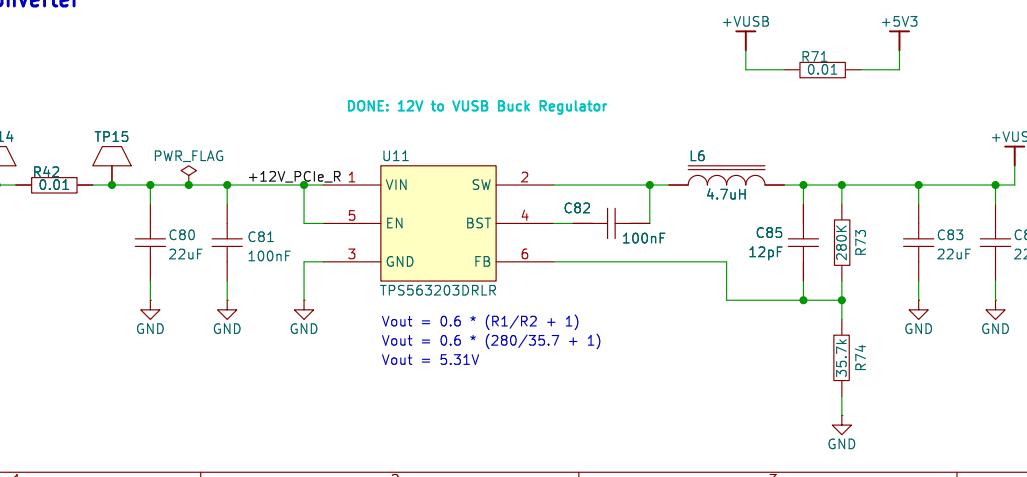
Variant Pin Strap



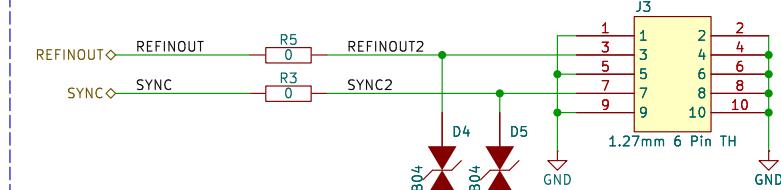
Probe Comp



5V3 Buck Converter



Refclock and Sync Header



EEVengers

Sheet: /TS-PCIe Components/
File: CON_PCIe_X4.kicad_sch

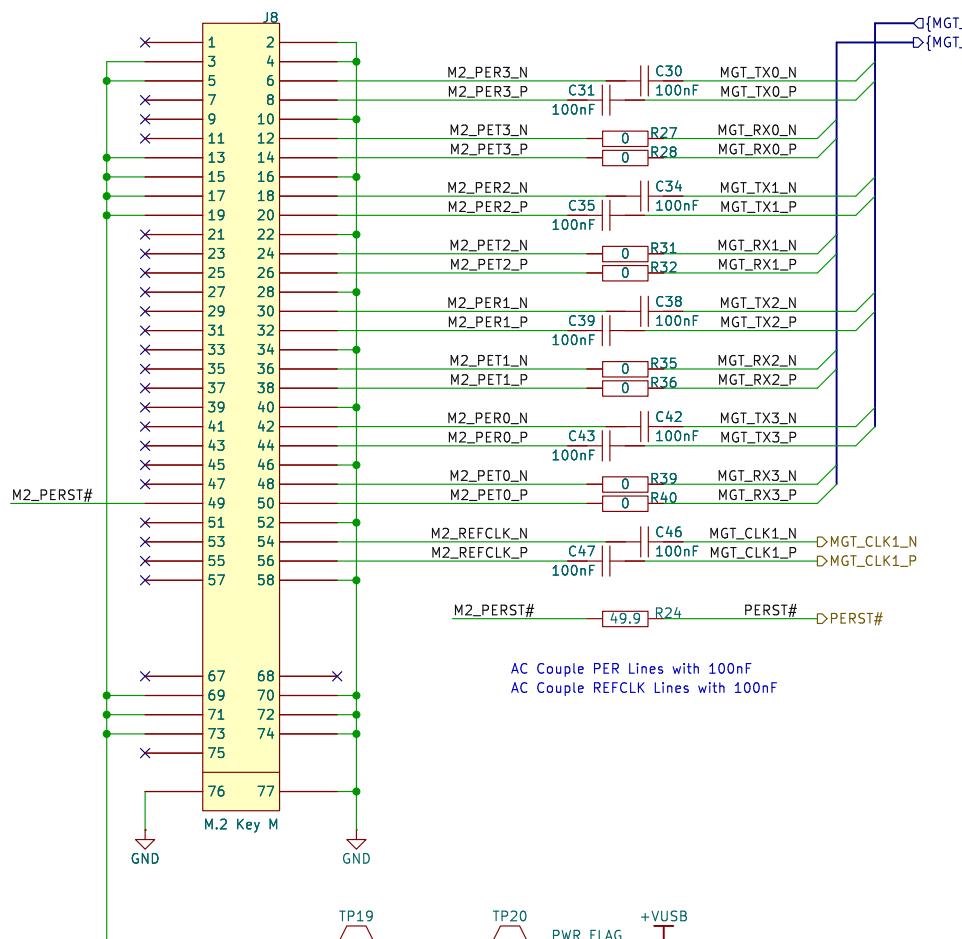
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Size: A4 Date:
KiCad E.D.A. 9.0.0

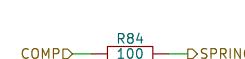
Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 12/16

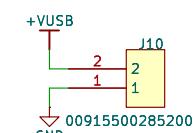
M.2 Key M Connector – Custom Pinout



Probe Comp



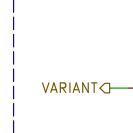
Fan Connector



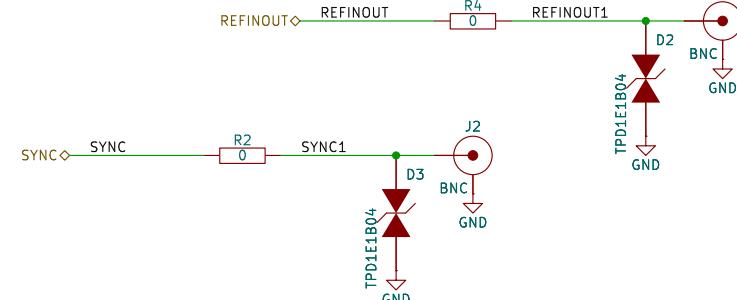
Ground Lug



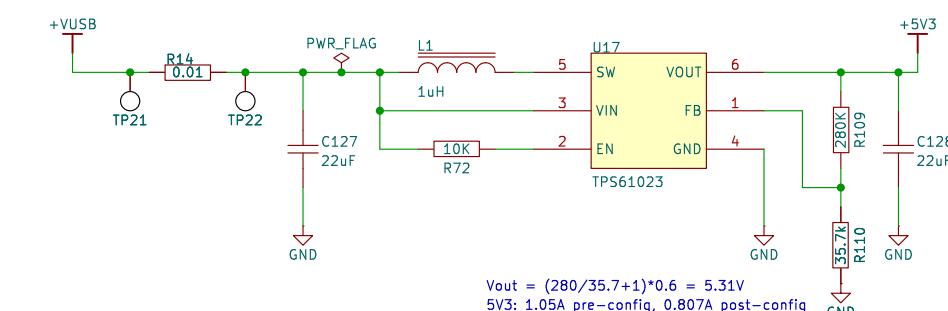
Variant Pin Strap



Refclock and Sync BNCs



5V3 Boost Converter



Interposer Standoffs



EEVengers

Sheet: /TS-USB4 Components/
File: M2_KEY_M.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 9.0.0

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 13/16