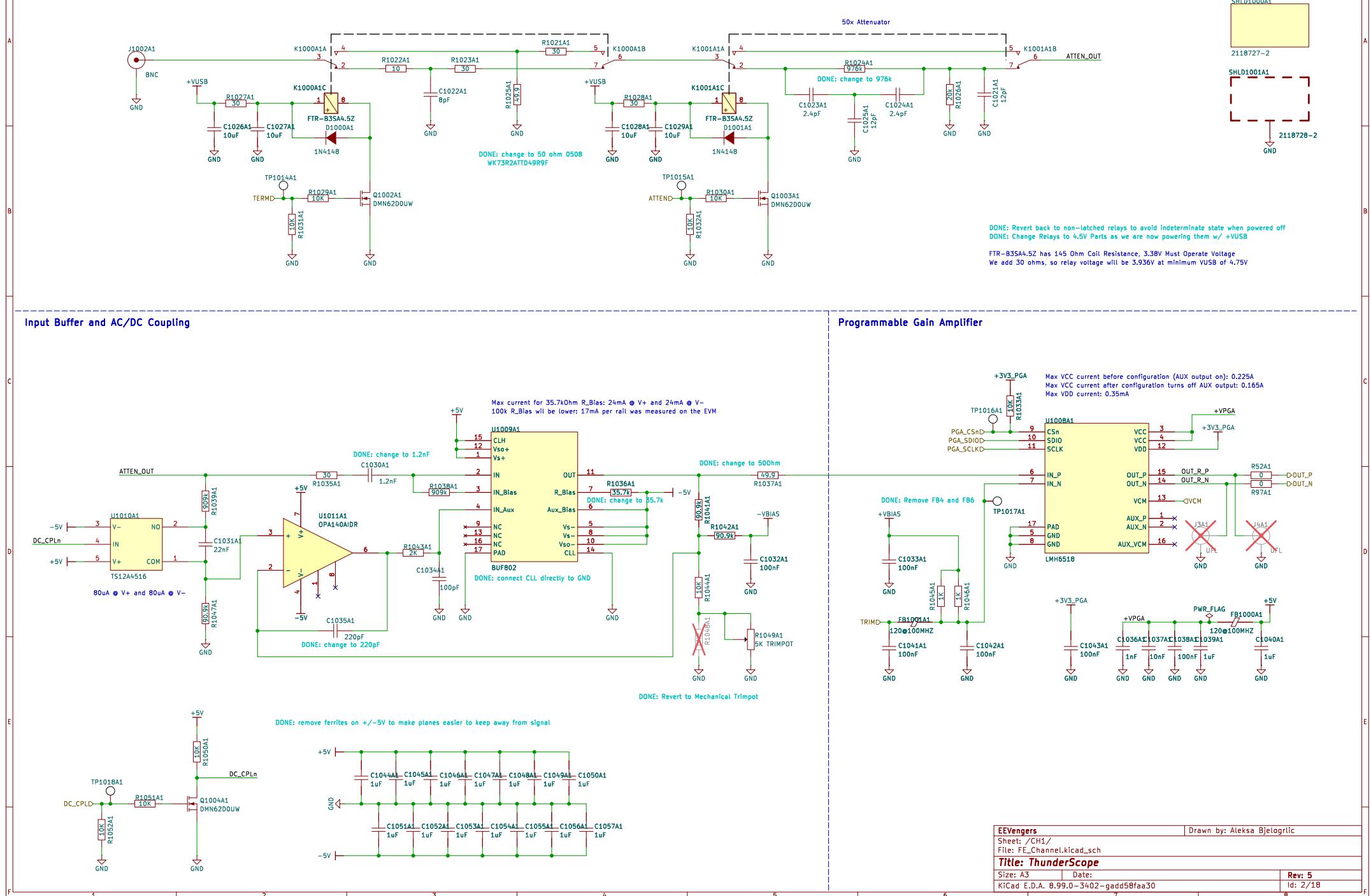
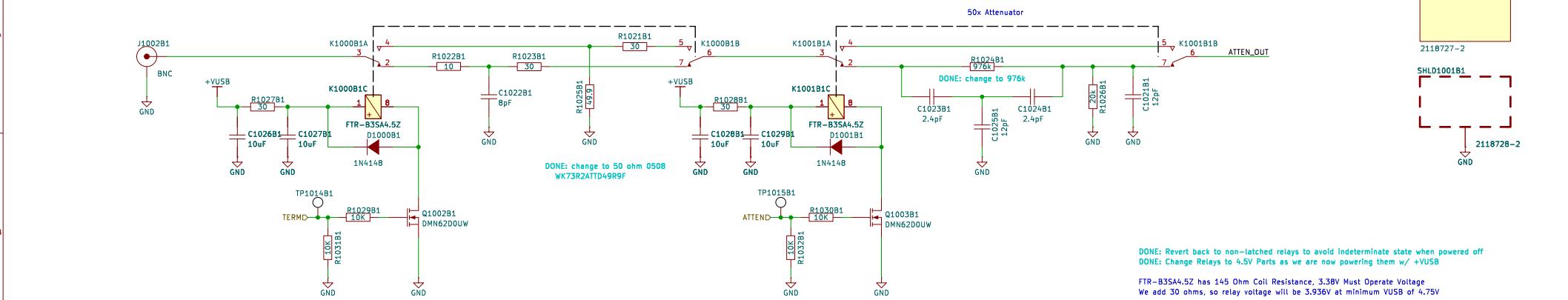


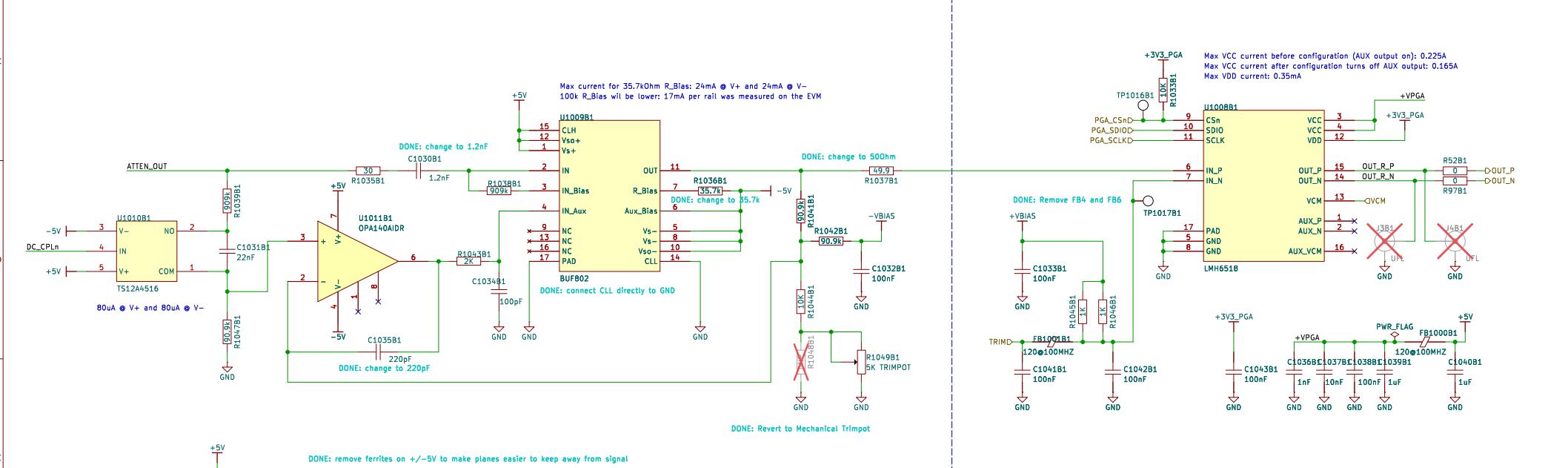
Termination and Attenuation



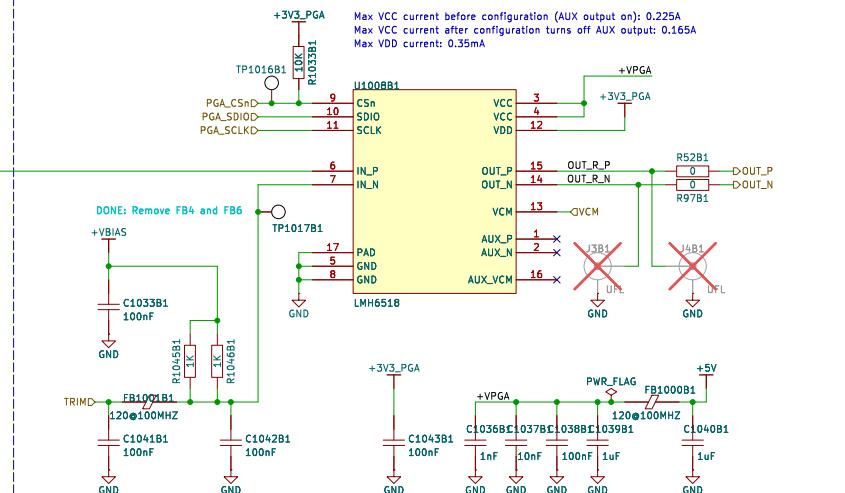
Termination and Attenuation



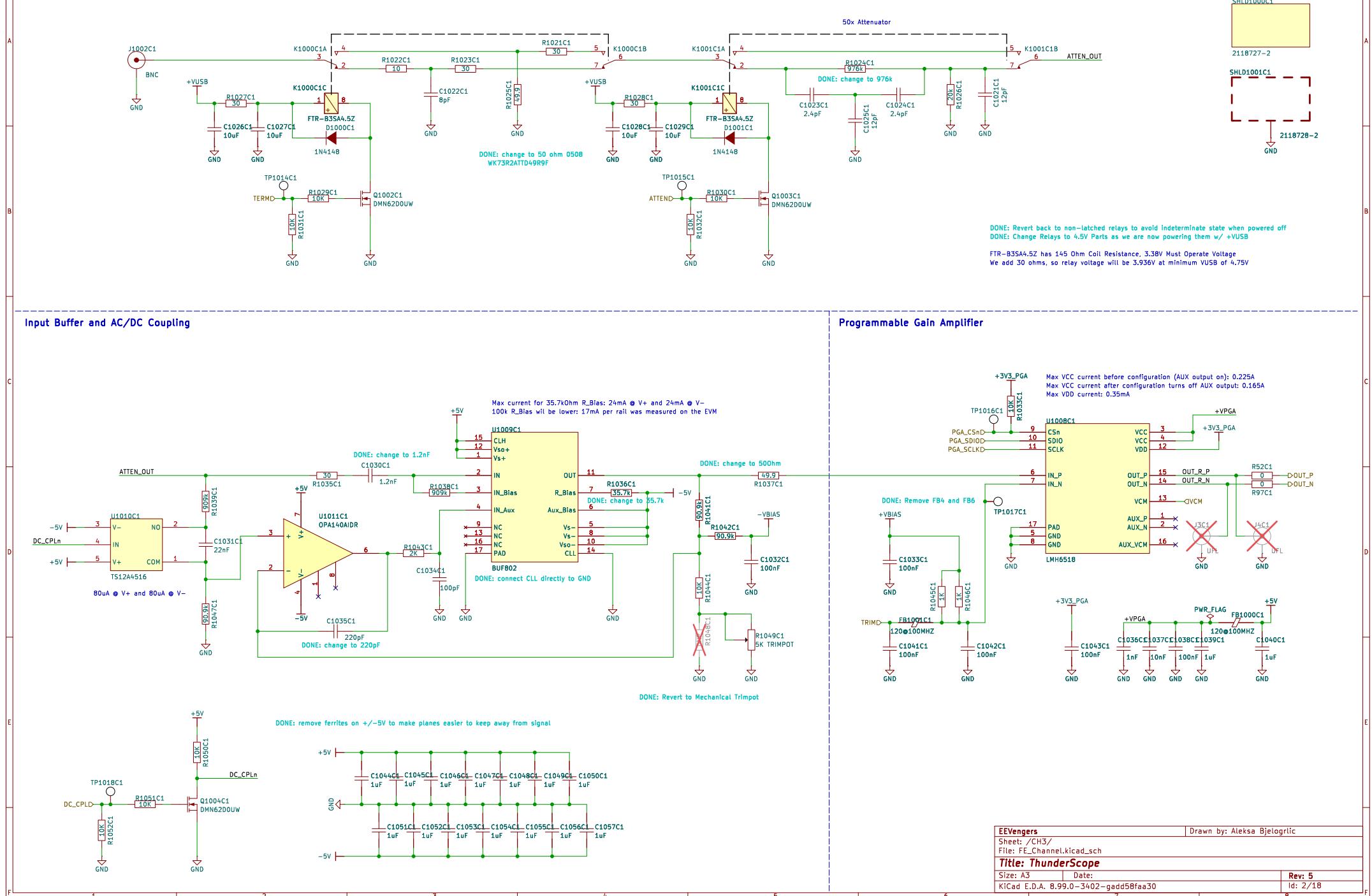
Input Buffer and AC/DC Coupling



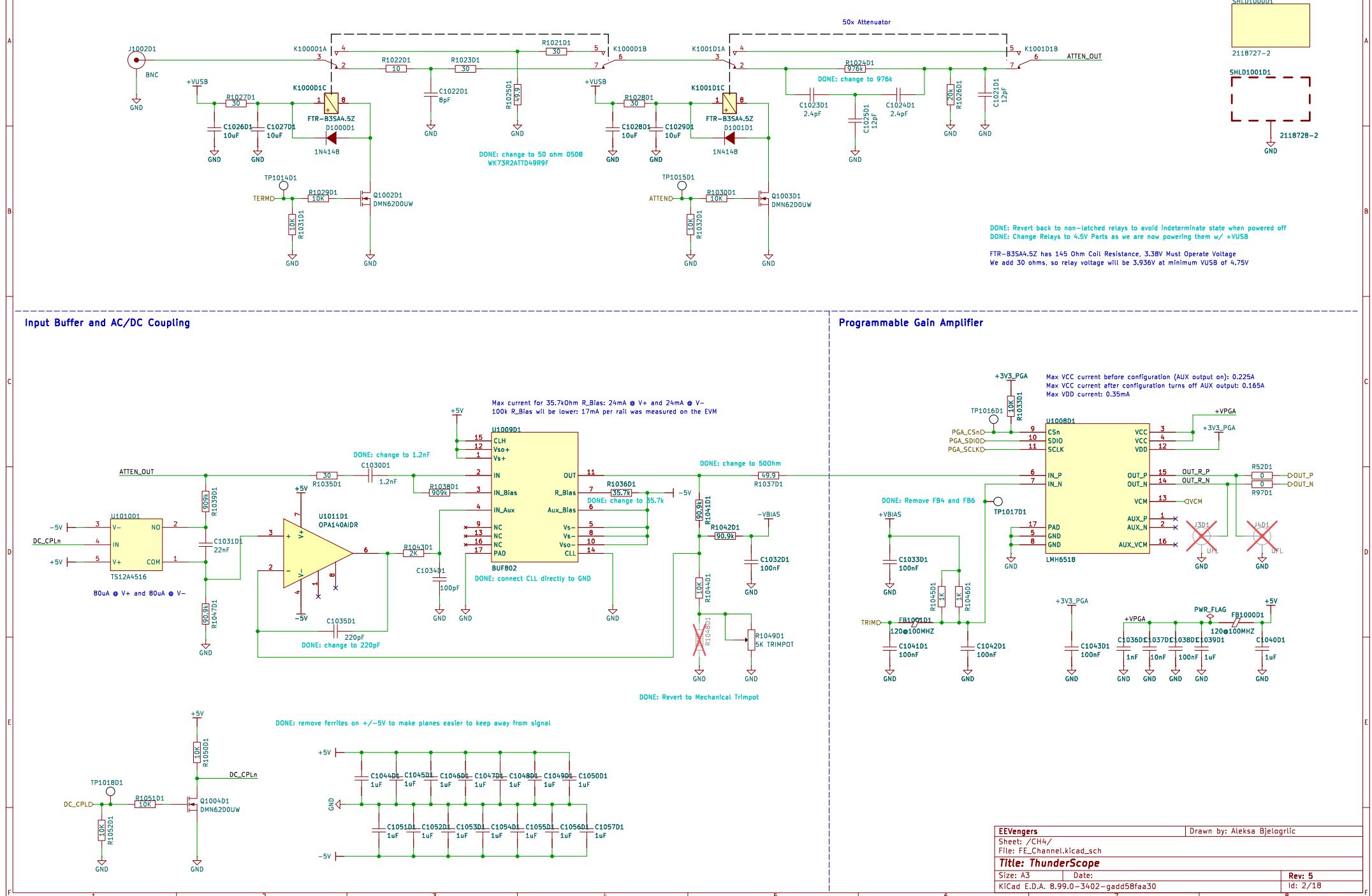
Programmable Gain Amplifier



Termination and Attenuation



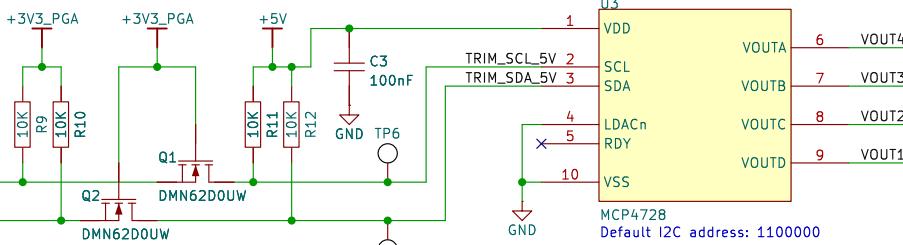
Termination and Attenuation



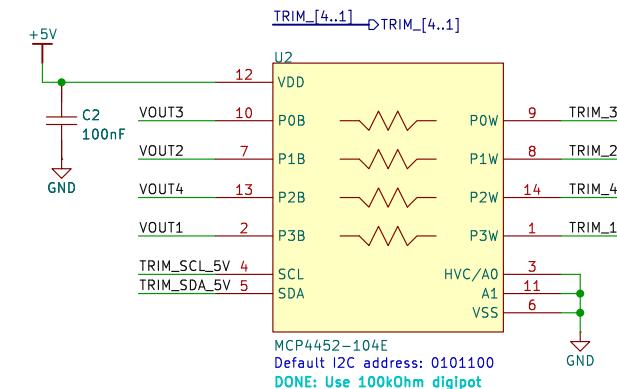
1 2 3 4 5 6

Offset Voltage Trim and User Offset Control

A

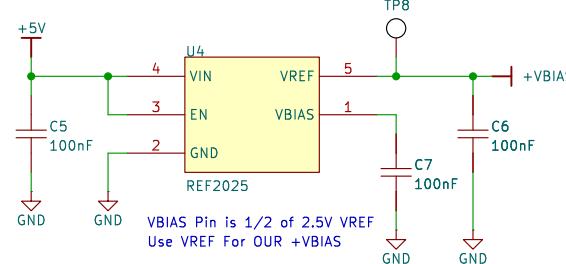


B



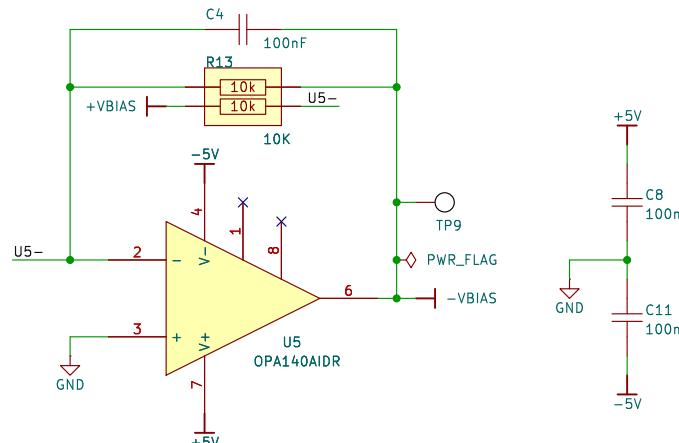
Bias Voltage Generation

C



D

Use 2.5V VREF Instead of U8 opamp, change remaining opamps to opa140
-Max resistance is $(575/4 // 10k) = 141.7 \text{ Ohm}$
-Worst case current is 17.64mA
-Use REF2025, has max current of 20mA
-Change U5 divider to matched resistor network
-ACASN1002S1002P1AT



EEVengers

Sheet: /Front End Trim and Bias/
File: FE.kicad_sch

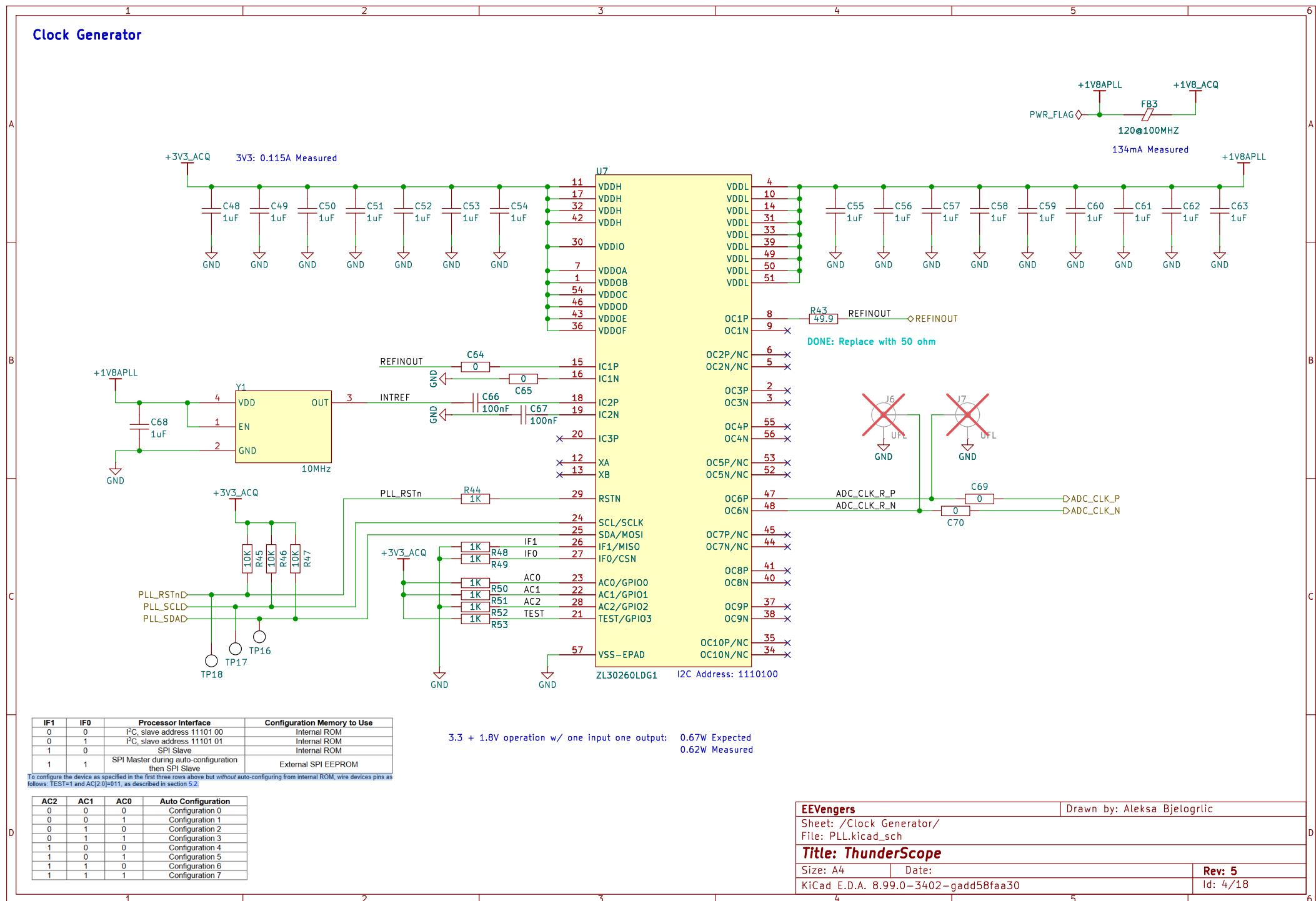
Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

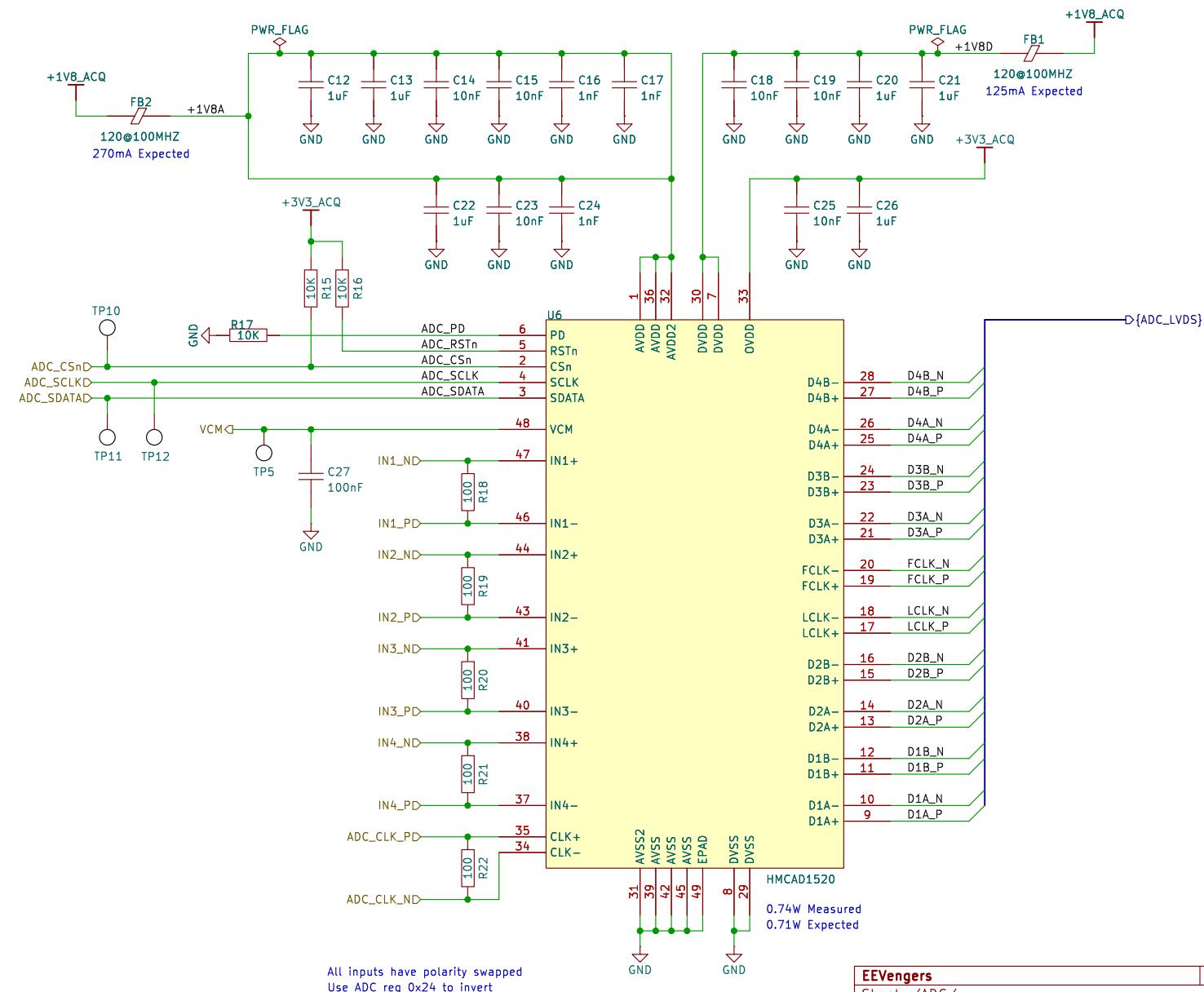
Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 3/18

1 2 3 4 5 6



1 2 3 4 5 6

ADC**EEVengers**

Drawn by: Aleksa Bjelogrlic

Sheet: /ADC/
File: ADC.kicad_sch**Title: ThunderScope**

Size: A4 Date:

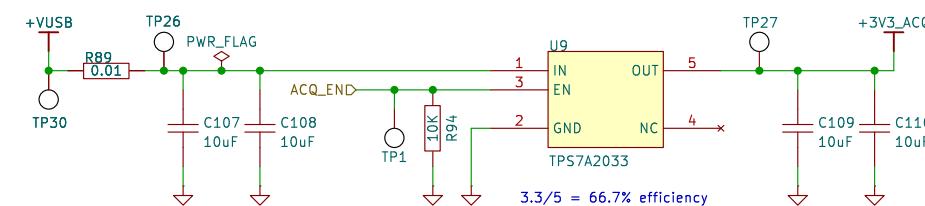
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Rev: 5

Id: 5/18

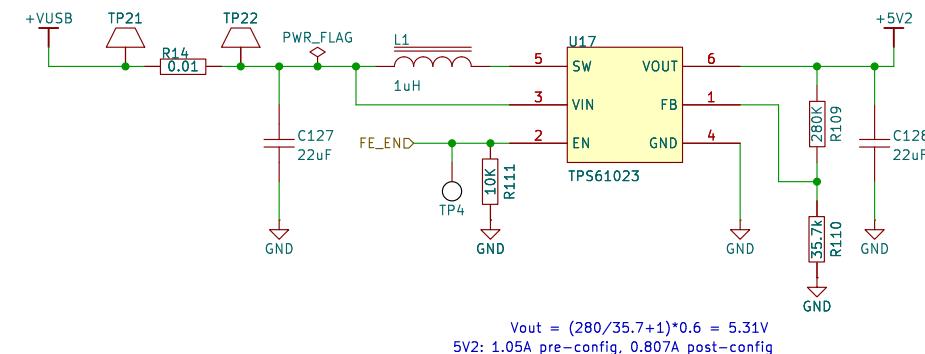
1 2 3 4 5 6

Acquisition Voltage Regulators



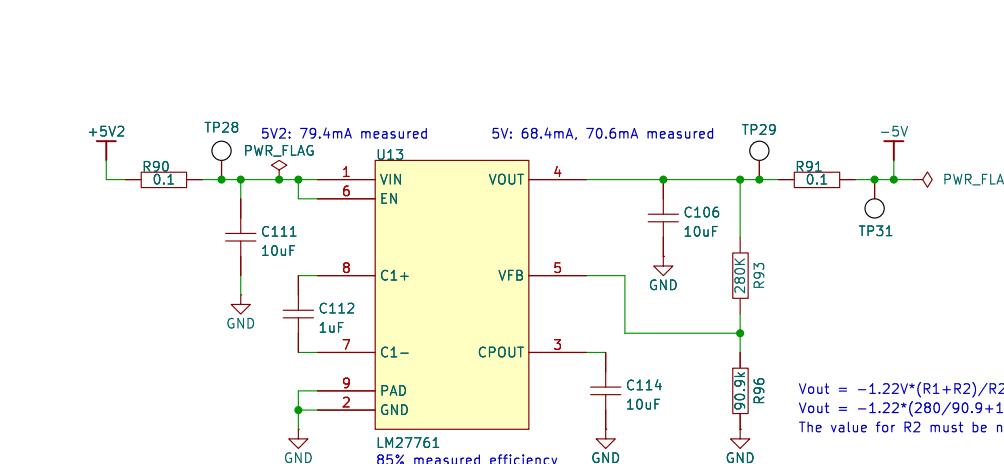
DONE: Hook up power good, pull up is in FPGA IO Banks

Front End Voltage Regulators



$$V_{out} = (280/35.7+1)*0.6 = 5.31V$$

5V2: 1.05A pre-config, 0.807A post-config



$$V_{out} = -1.22V*(R1+R2)/R2$$

$$V_{out} = -1.22*(280/90.9+1) = -4.98V$$

The value for R2 must be no less than 50 kΩ.

1 2 3

4 5 6

EEVengers Drawn by: Aleksa Bjelogrlic

Sheet: /ACQ and FE Voltage Regs/

File: ACQ_FE_VREG.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 8.99.0-3402-gadd58faa30

Rev: 5

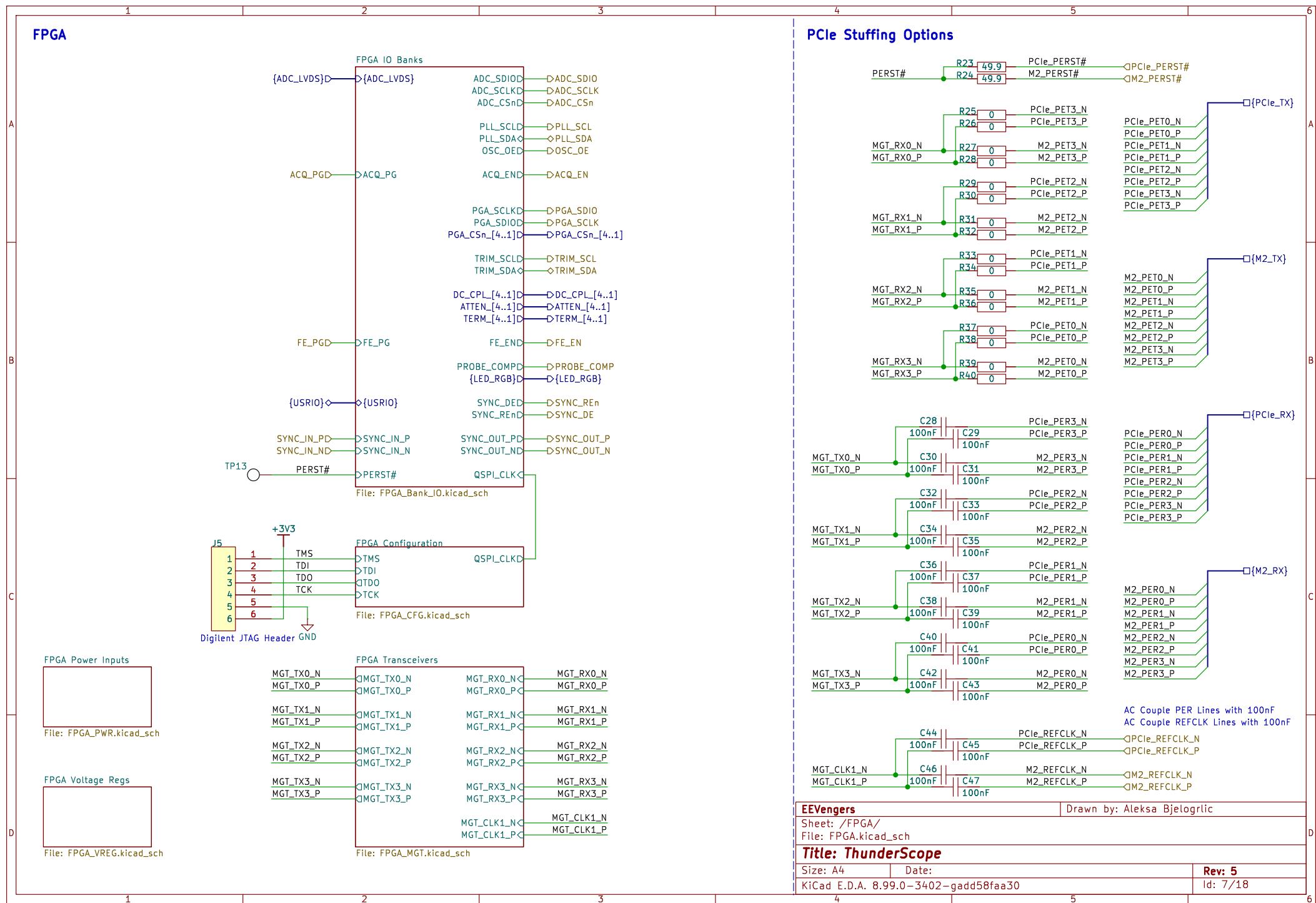
Id: 6/18

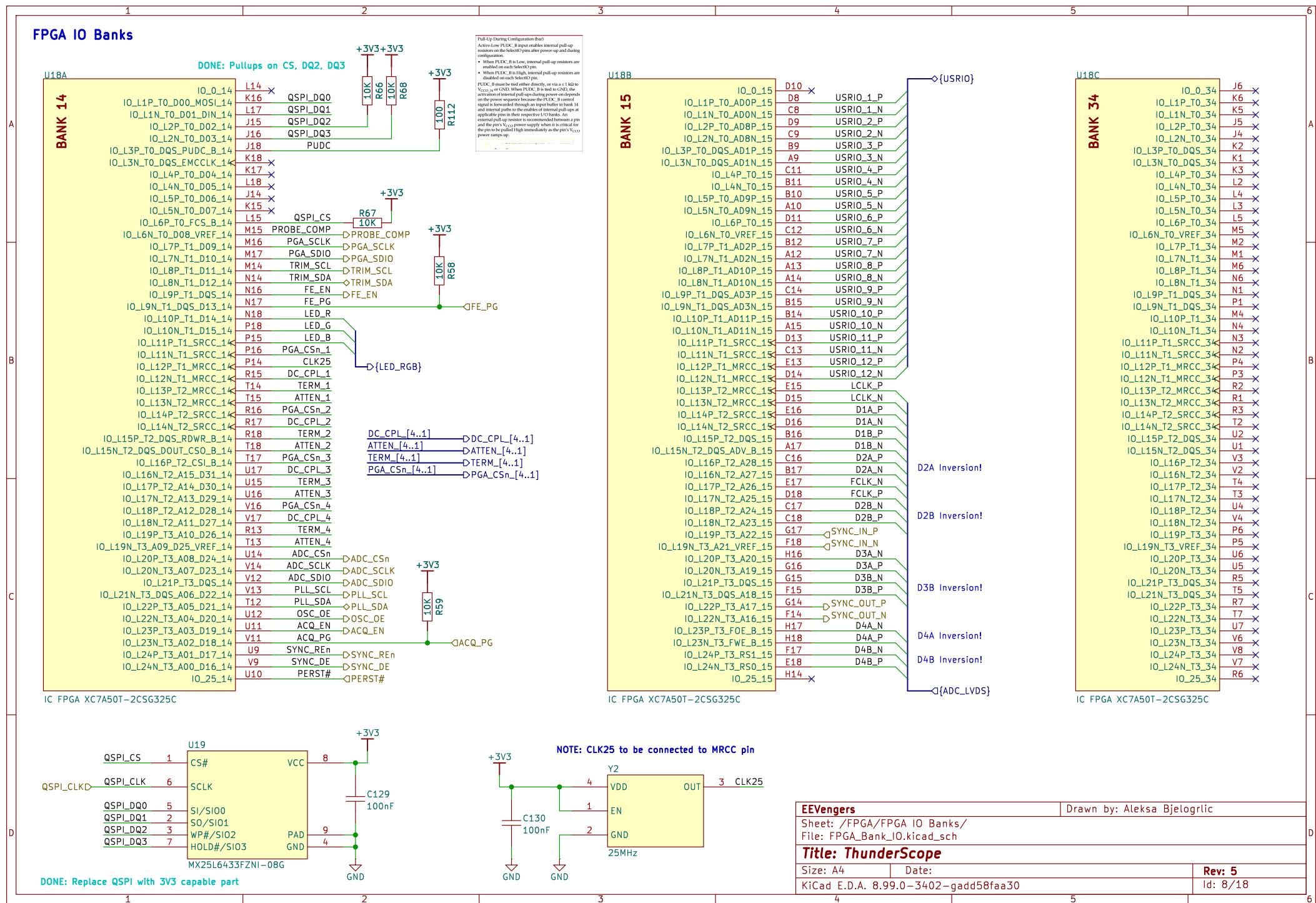
1 2 3

4 5 6

1 2 3

4 5 6





FPGA Configuration

A

B

C

D

A

B

C

D

Table 2-1: 7 Series FPGA Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

M[2:0] = 001

A high signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.
Active DONE is a high signal with a pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE pin. If the user does not require the DONE pin, software default, eliminate the need for the DONE pin by connecting it to ground. Three pull-down circuits are not required but can be used as they have been previously shown.

Connect INIT_B to a 47 kΩ pull-up resistor to VCCO_0 to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external < 47 kΩ pull-up resistor to VCCO_0 to generate a stable High input, and

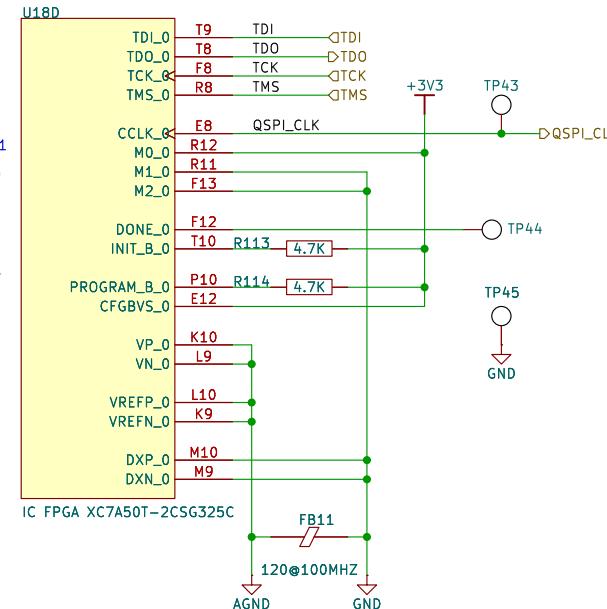


Table 2-6: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Voltages, and CFGBVS Connection

Configuration Mode	Banks Used	Configuration Interface I/O Voltage	HR Bank 0 V _{CCO_0}	HR Bank 14 V _{CCO_14}	HR Bank 15 V _{CCO_15}	CFGBVS
JTAG (only)	0	3.3V	3.3V	Any	Any	VCCO_0
		2.5V	2.5V	Any	Any	VCCO_0
		1.8V	1.8V	Any	Any	GND
		1.5V	1.5V	Any	Any	GND
		3.3V	3.3V	3.3V	Any	VCCO_0
Serial SPI or SelectMAP	0, 14 ⁽¹⁾	3.3V	3.3V	2.5V	Any	VCCO_0
		2.5V	2.5V	2.5V	Any	VCCO_0
		1.8V	1.8V	1.8V	Any	GND
		1.5V	1.5V	1.5V	Any	GND
		3.3V	3.3V	3.3V	3.3V	VCCO_0
BPI ⁽²⁾	0, 14, 15	2.5V	2.5V	2.5V	2.5V	VCCO_0
		1.8V	1.8V	1.8V	1.8V	GND
		1.5V	1.5V	1.5V	1.5V	GND
		3.3V	3.3V	3.3V	3.3V	VCCO_0
		2.5V	2.5V	2.5V	2.5V	VCCO_0

Notes:

1. RS[1:0] for MultiBoot or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SPI mode.
2. BPI mode is not available in the Spartan-7 family.

EEVengers

Sheet: /FPGA/FPGA Configuration/
File: FPGA_CFG.kicad_sch

Title: ThunderScope

Size: A4 Date:

KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 9/18

FPGA Transceivers

A

A

B

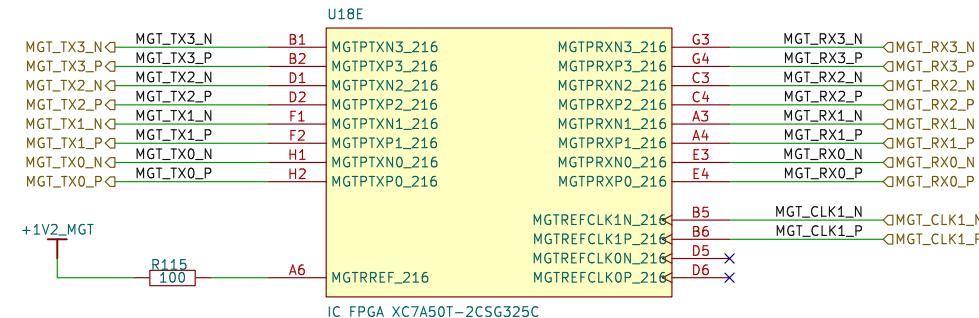
B

C

C

D

D

**EEVengers**

Sheet: /FPGA/FPGA Transceivers/
File: FPGA_MGT.kicad_sch

Title: ThunderScope

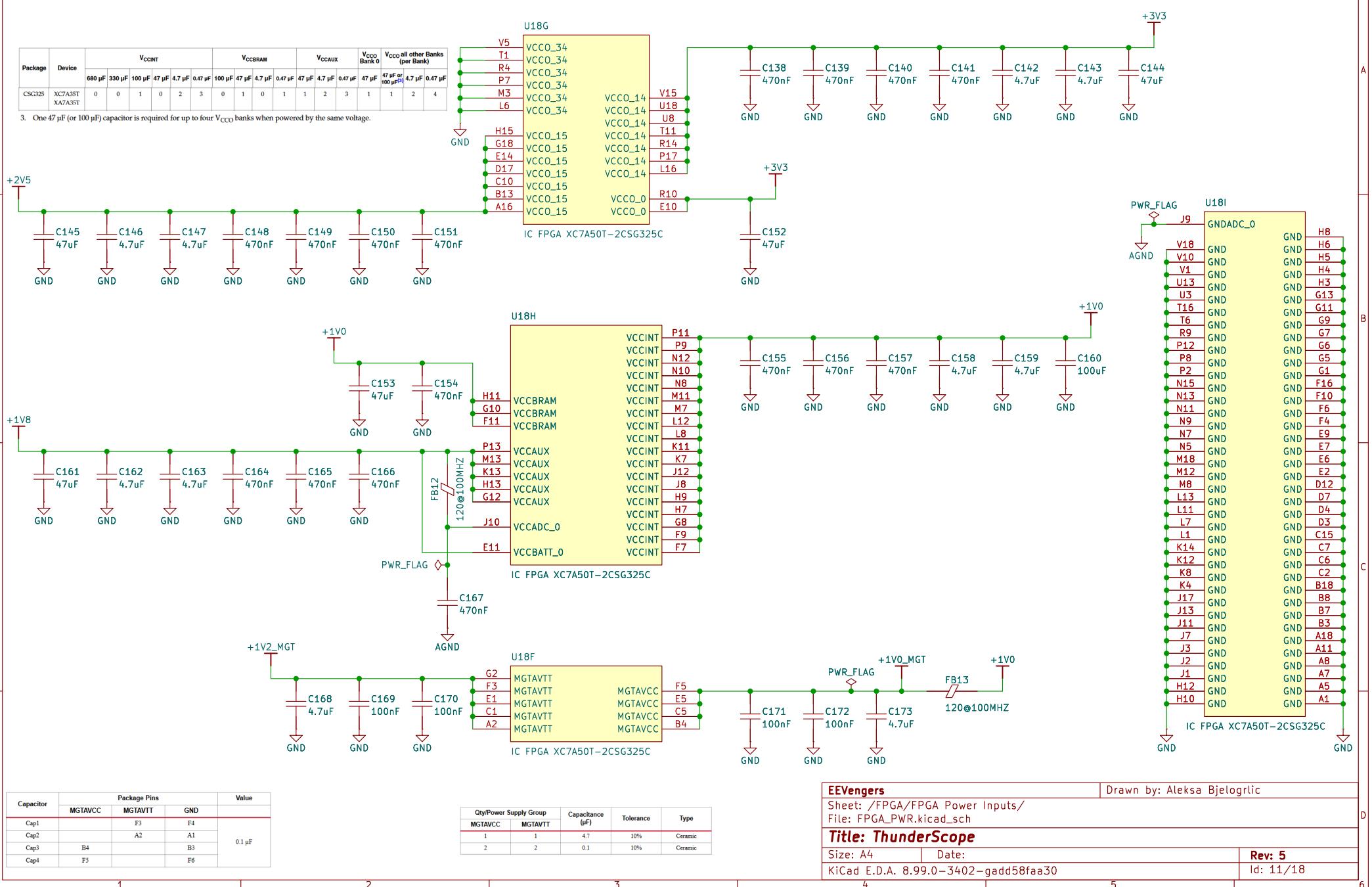
Size: A4 Date:

KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 10/18

PAGE 1: FPGA Power Inputs



1

2

3

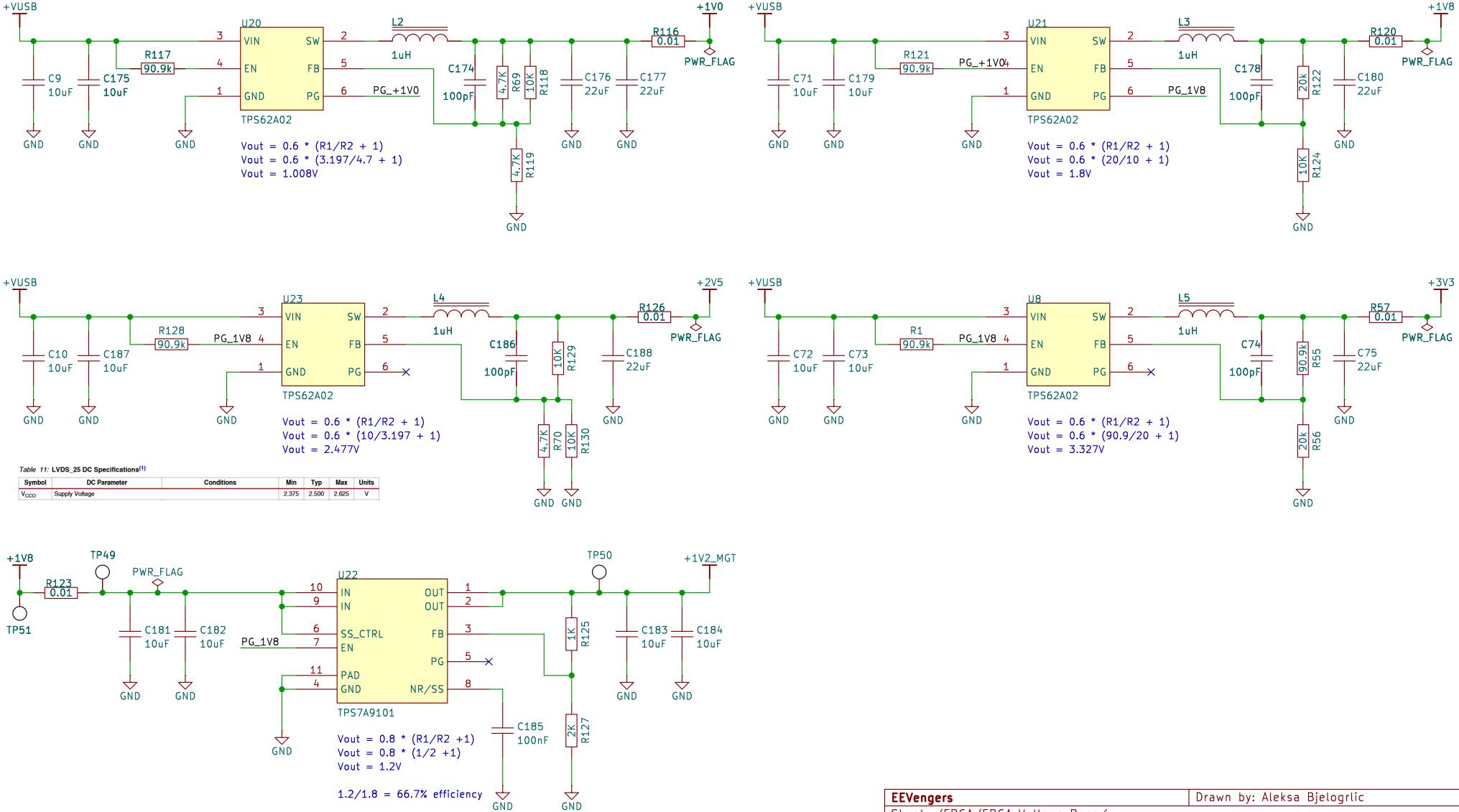
4

5

6

FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V



EEVengers

Sheet: /FPGA/FPGA Voltage Regs/
File: FPGA_VREG.kicad_sch

Title: ThunderScope

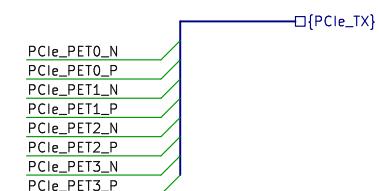
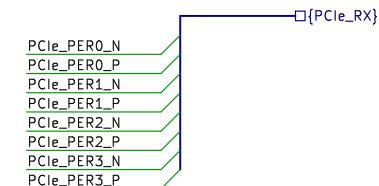
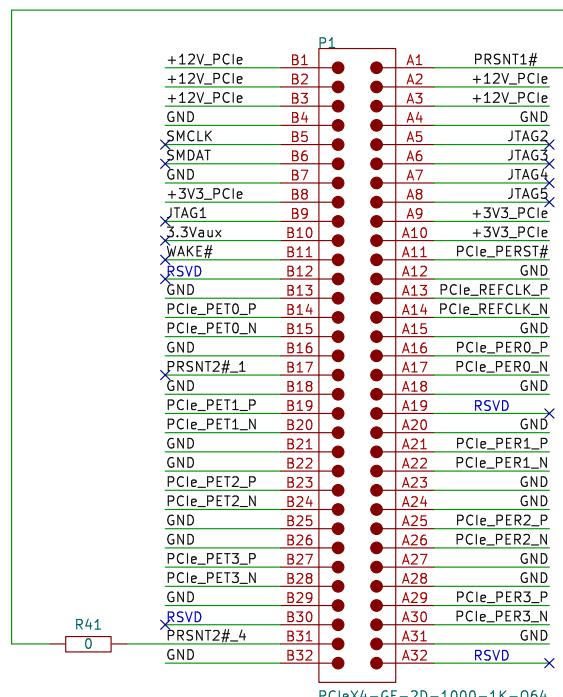
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Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 12/18

1 2 3 4 5 6

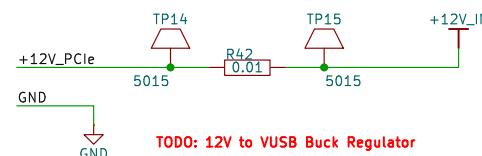
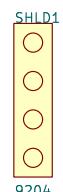
PCIe x4 Edge Connector



PCIe_REFCLK_P → PCIe_REFCLK_P
PCIe_REFCLK_N → PCIe_REFCLK_N

PCIe_PERST# → PCIe_PERST#

PCIe bracket



EEVengers

Sheet: /PCIe_x4/
File: CON_PCIe_X4.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

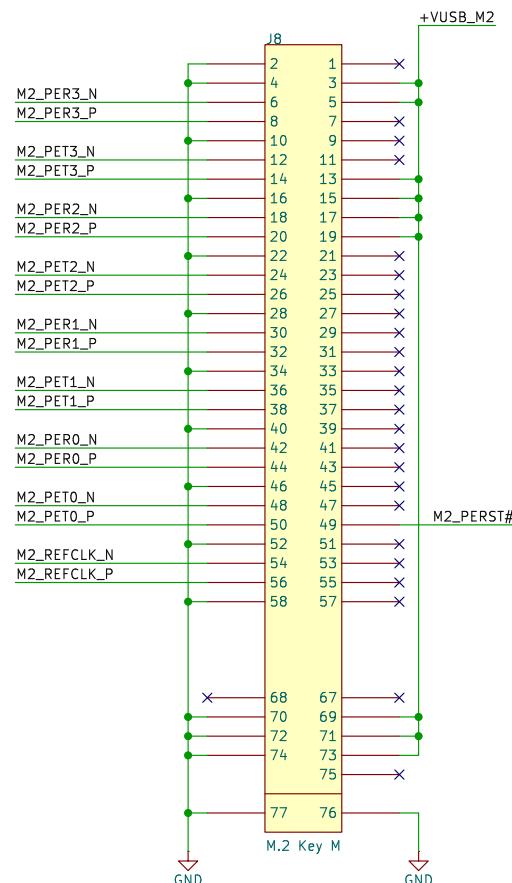
Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 13/18

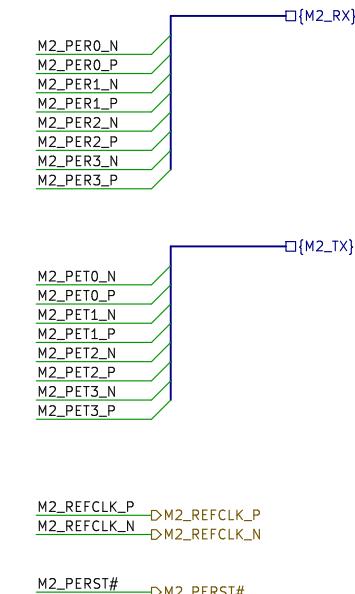
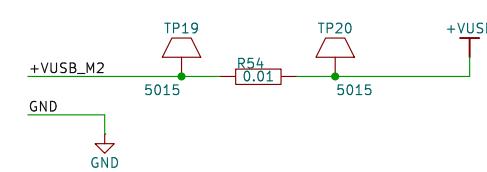
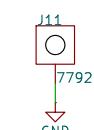
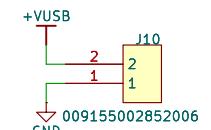
1 2 3 4 5 6

M.2 Key M Connector

A

**Main Board
Custom Pinout**

NOTE: The TB/USB4 adaptor must be modified to give us VUSB instead of 3V3

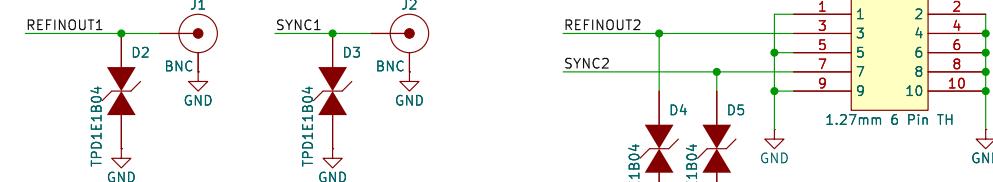
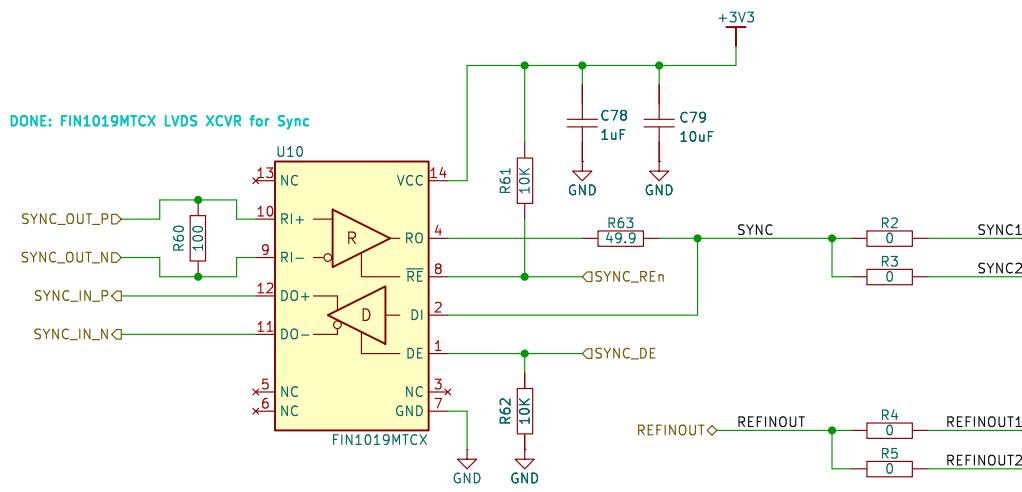
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File: M2_KEY_M.kicad_sch**Title: ThunderScope**Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

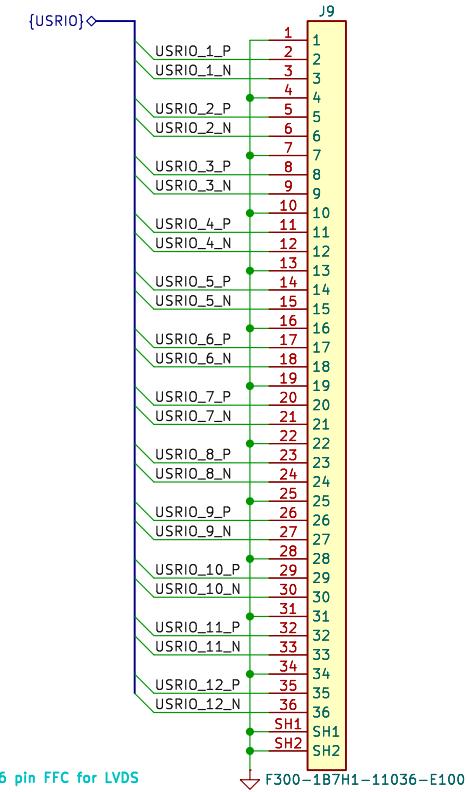
Rev: 5
Id: 14/18

1 2 3 4 5 6

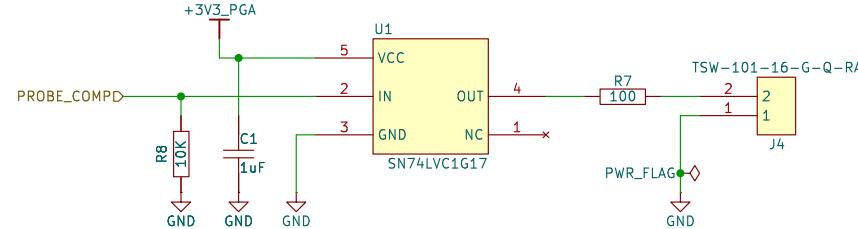
Reference Clock and Sync



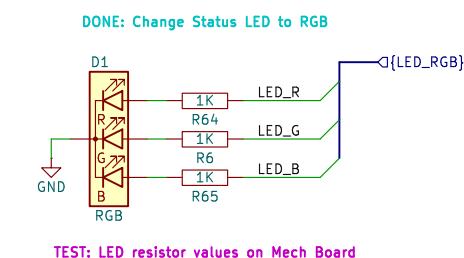
User IO Flat Flex Connector



Probe Compensation



Status LED



EEVengers

Sheet: /User IO/
File: User_I0.kicad_sch**Title: ThunderScope**Size: A4 Date:
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Rev: 5
Id: 15/18