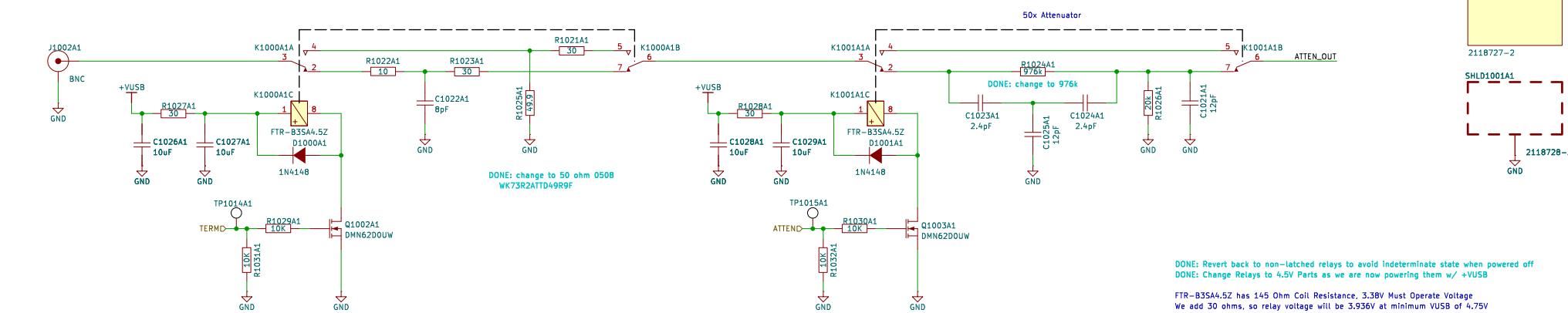
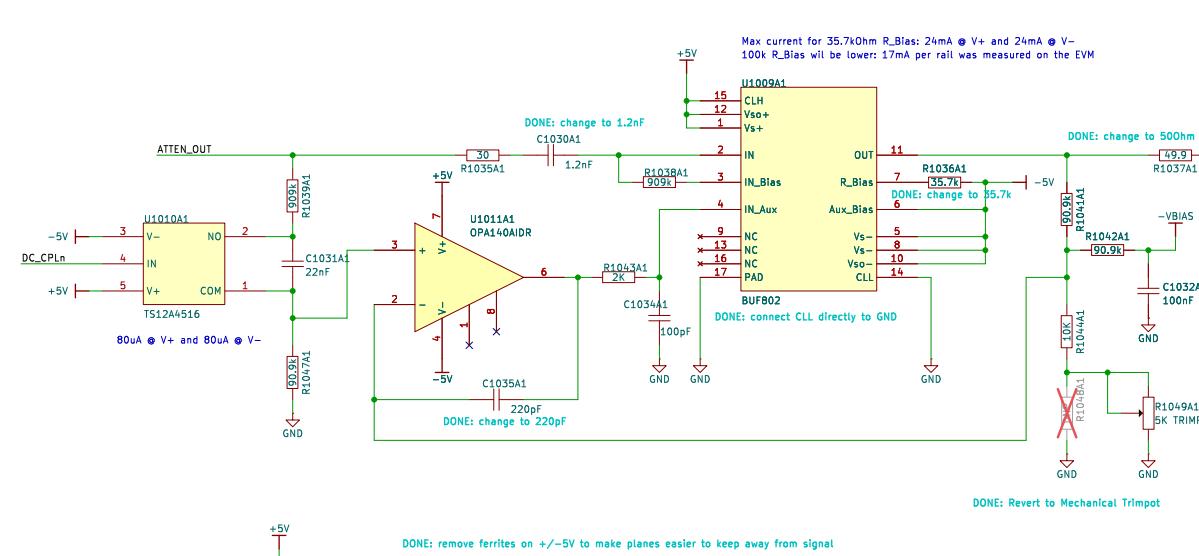


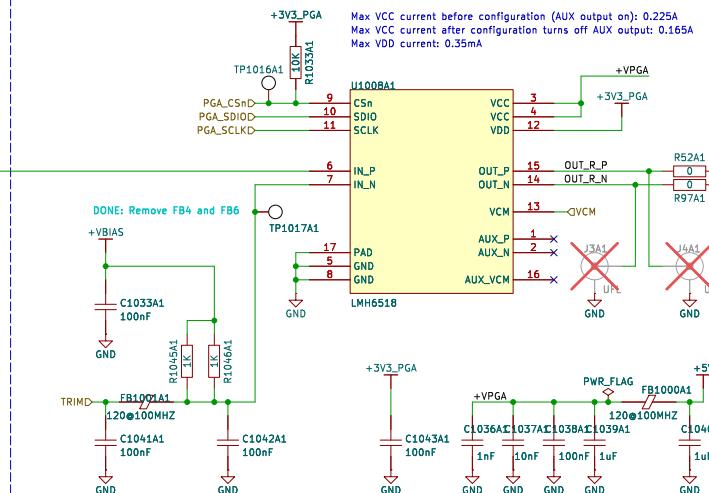
Termination and Attenuation



Input Buffer and AC/DC Coupling

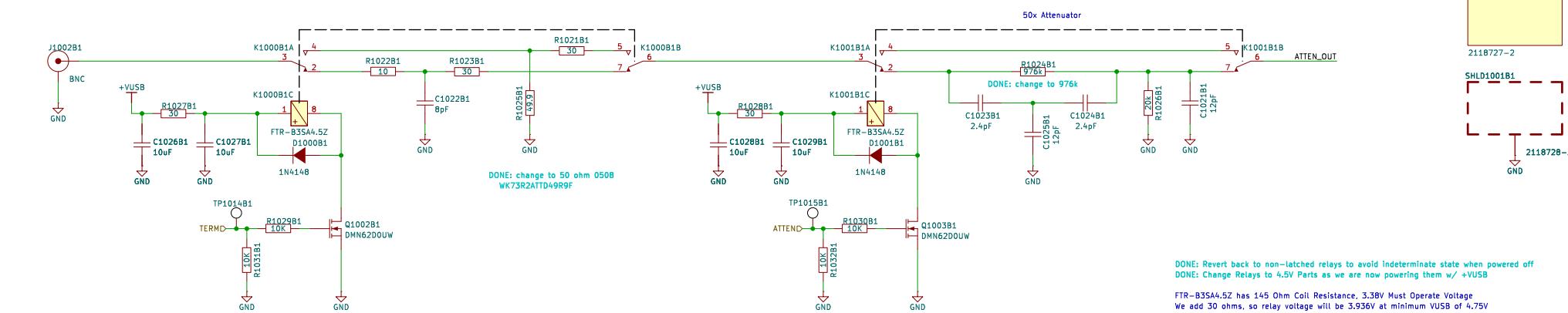


Programmable Gain Amplifier

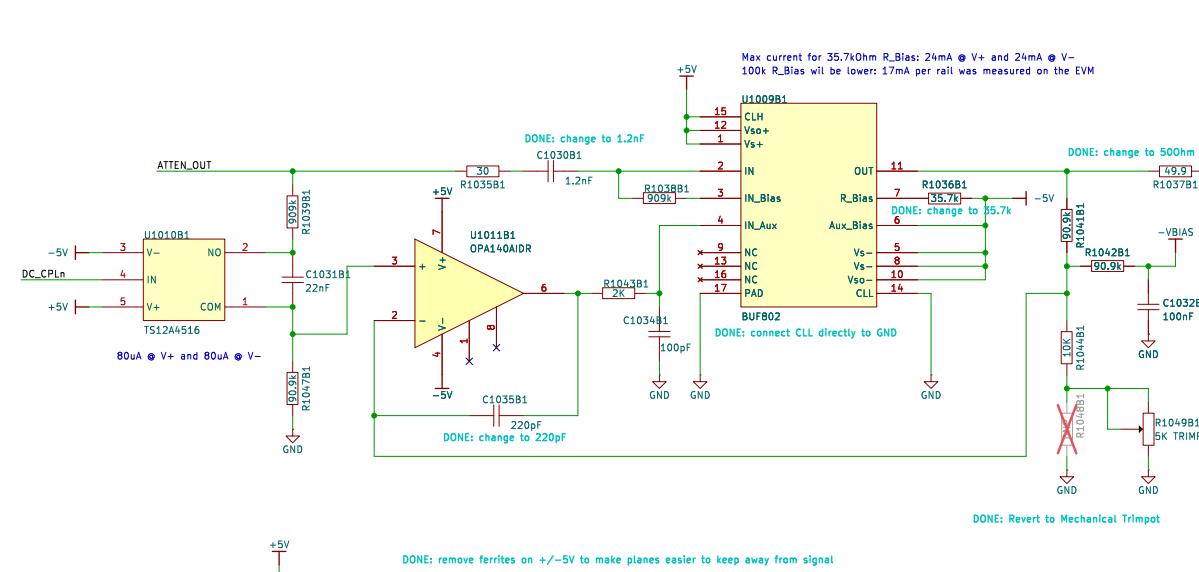


EEVengers		Drawn by: Aleksa Bjelogrlic	
Sheet: /CH1/			
File: FE_Channel.kicad_sch			
Title: ThunderScope			
Size: A3	Date:	Rev: 5	
KiCad E.D.A. 8.99.0-3402-gadd58faa30		Id: 2/16	

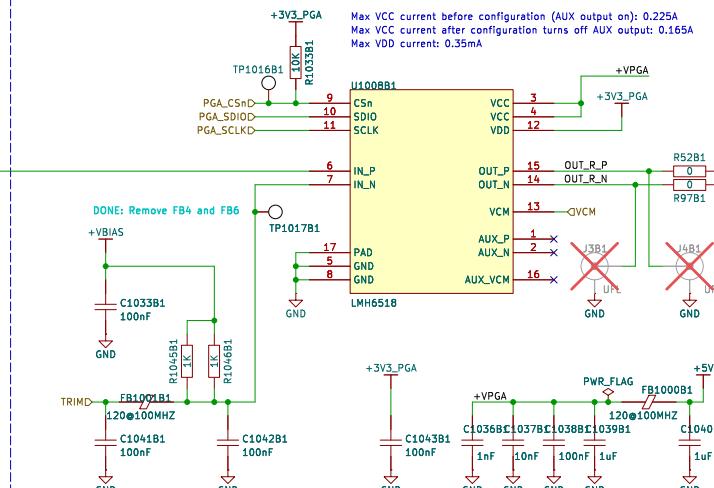
Termination and Attenuation



Input Buffer and AC/DC Coupling

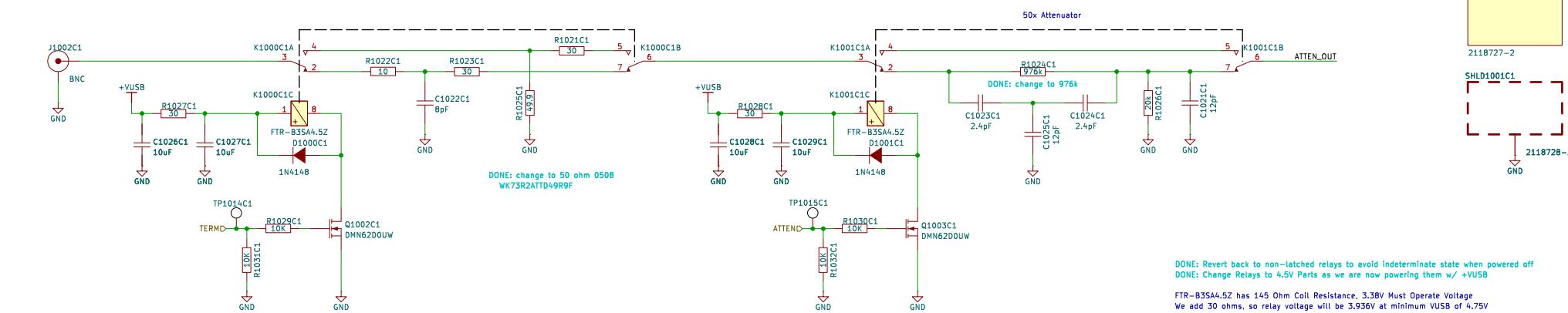


Programmable Gain Amplifier

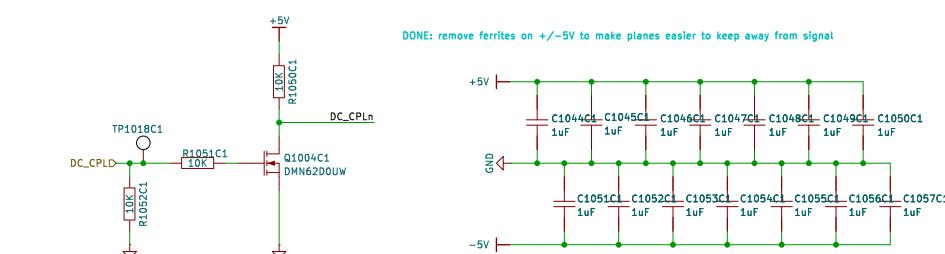
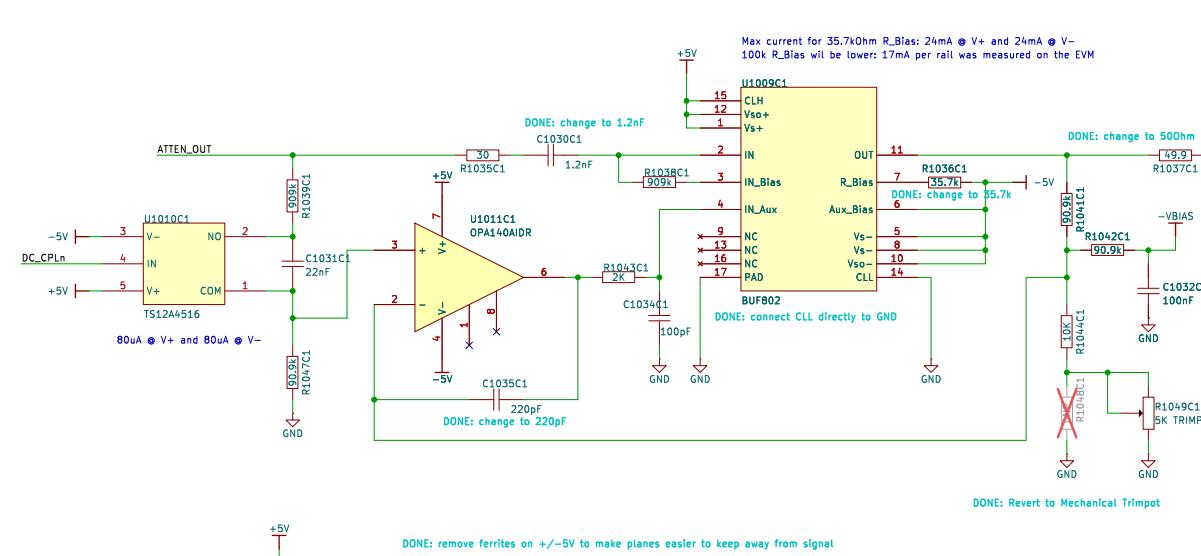


EEVengers	Drawn by: Aleksa Bjelogrlic
Sheet: /CH2/	
File: FE_Channel.kicad_sch	
Title: ThunderScope	
Size: A3	Date: 2023-08-15
KiCad E.D.A. 8.99.0-3402-gadd58faa30	Rev: 5
	Id: 2/16

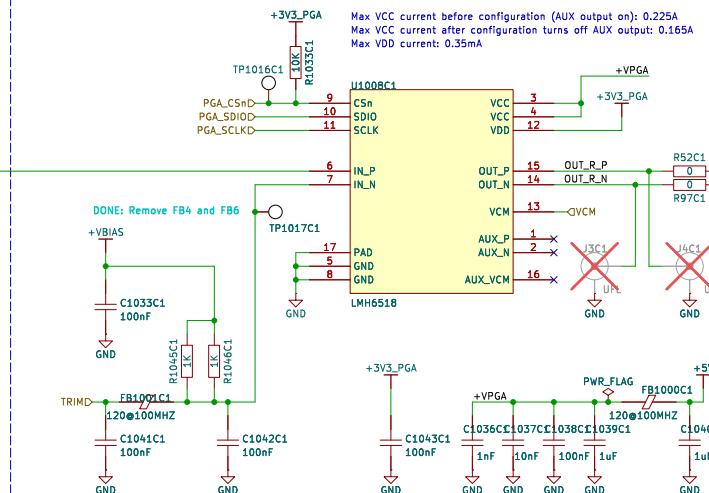
Termination and Attenuation



Input Buffer and AC/DC Coupling

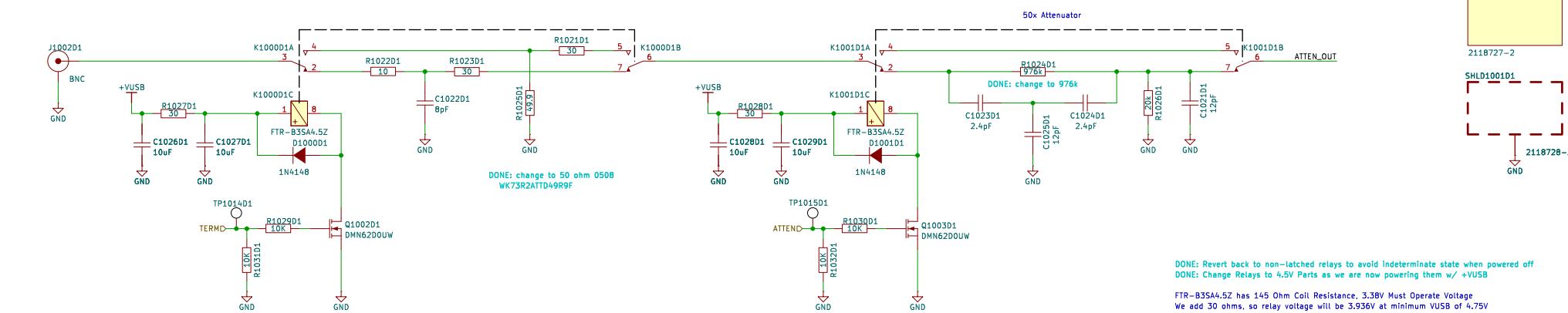


Programmable Gain Amplifier

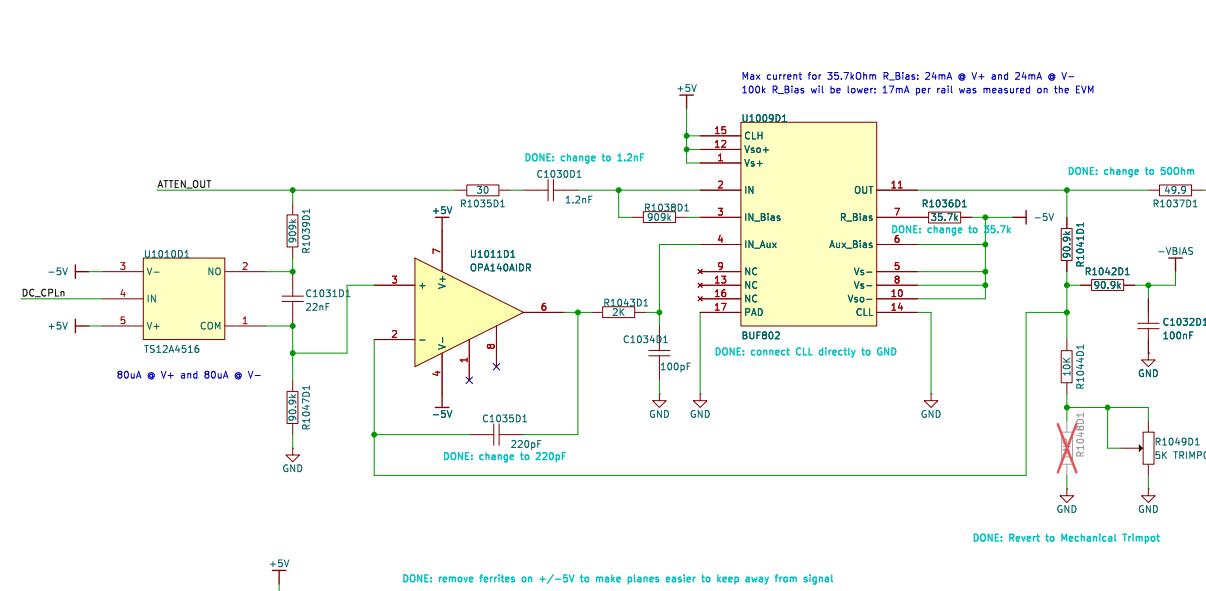


EEVengers Drawn by: Aleksa Bjelogrlic
Sheet: /CH3/
File: FE_Channel.kicad_sch
Title: ThunderScope
Size: A3 Date: Rev: 5
KiCad E.D.A. 8.99.0-3402-gadd58faa30 Id: 2/16

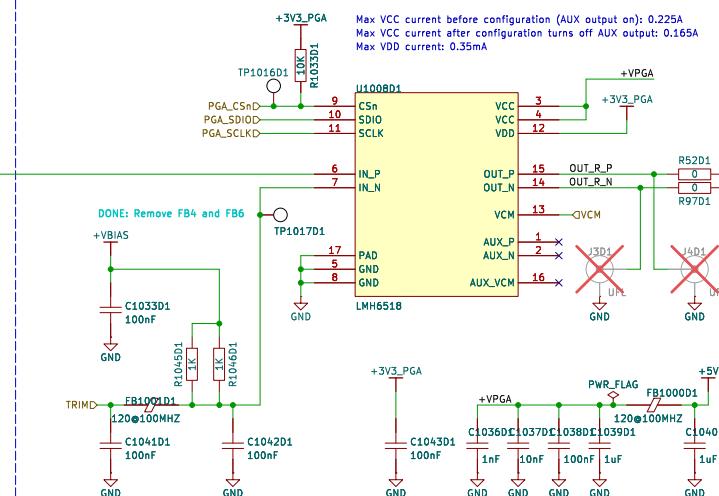
Termination and Attenuation



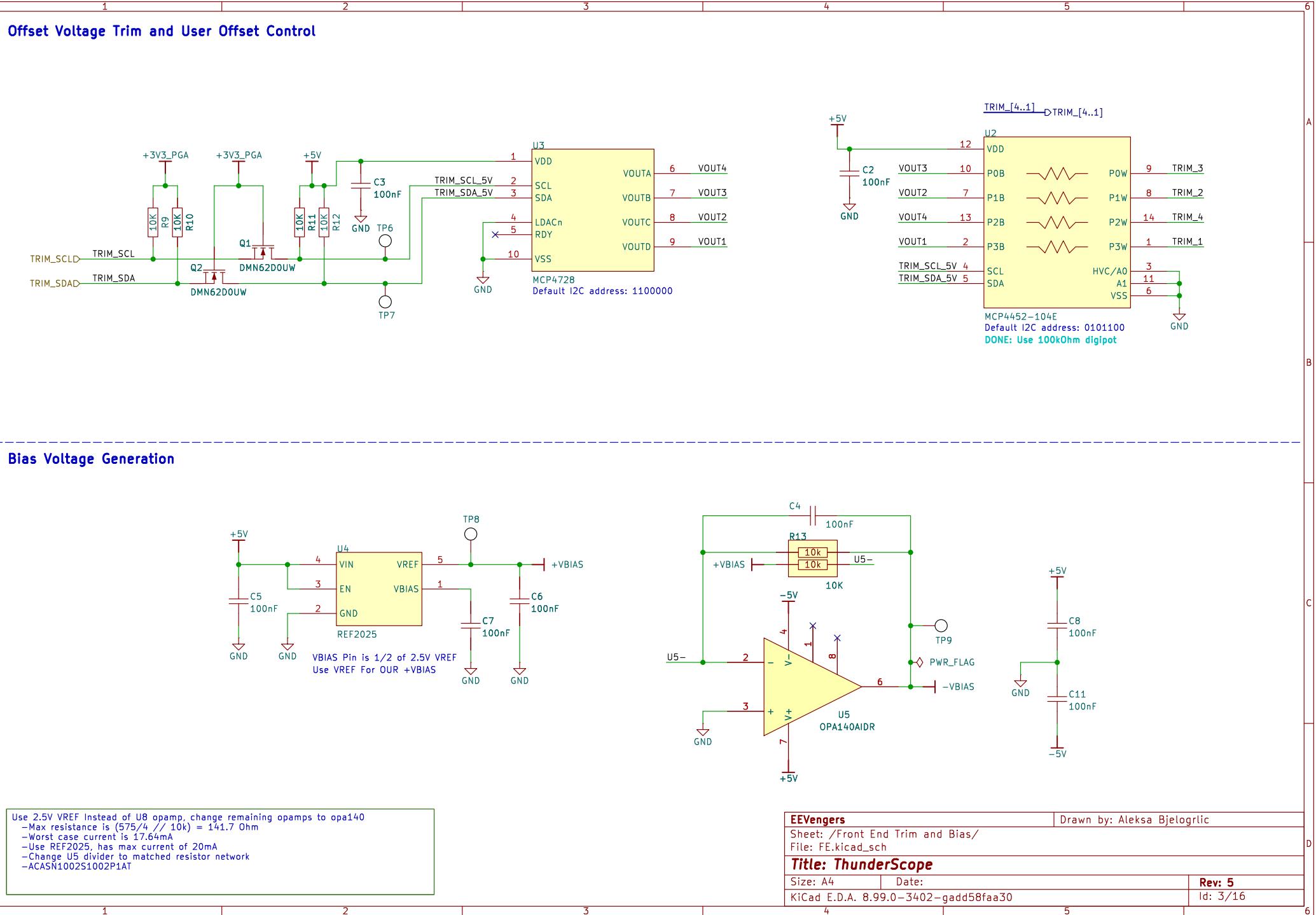
Input Buffer and AC/DC Coupling

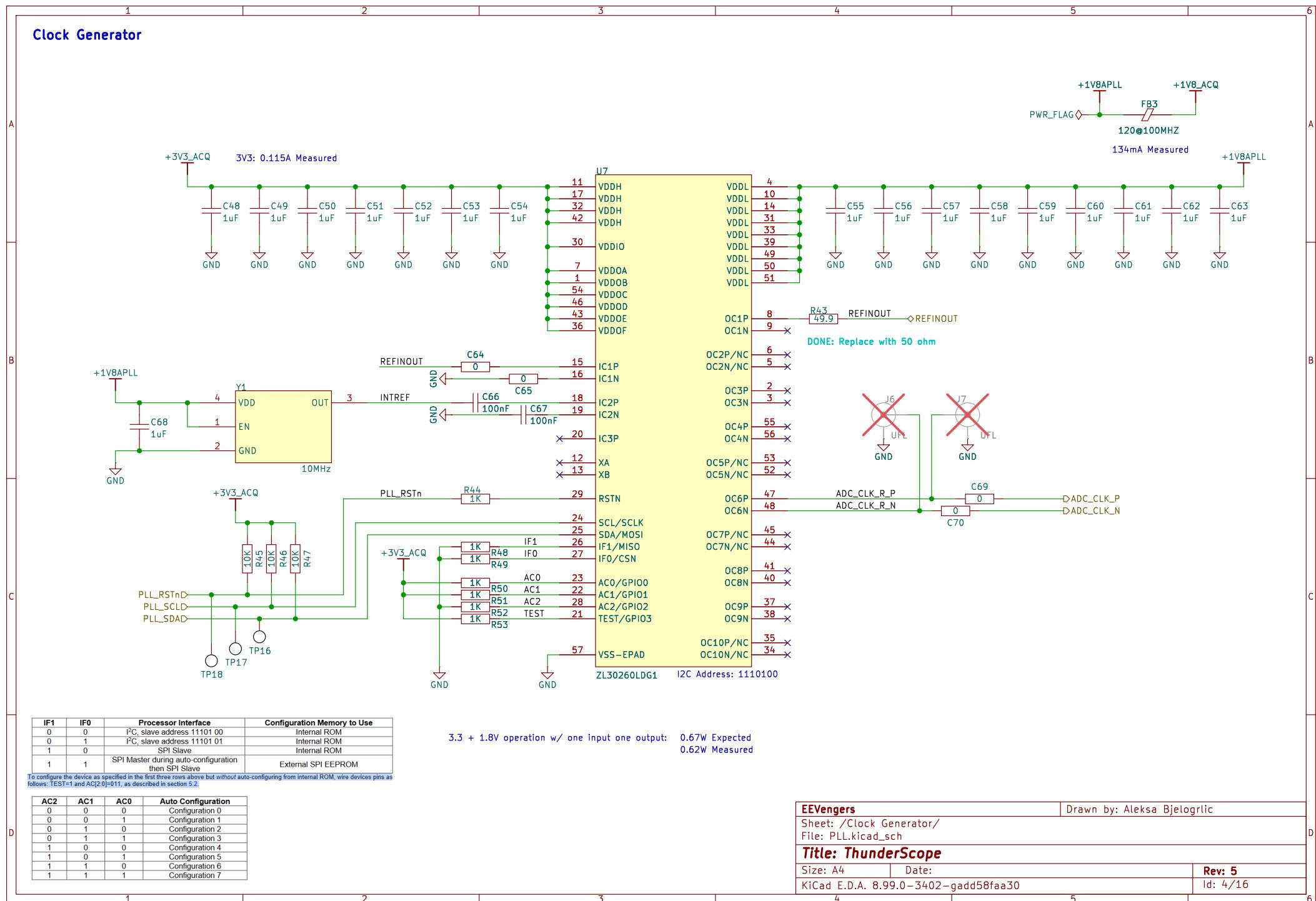


Programmable Gain Amplifier

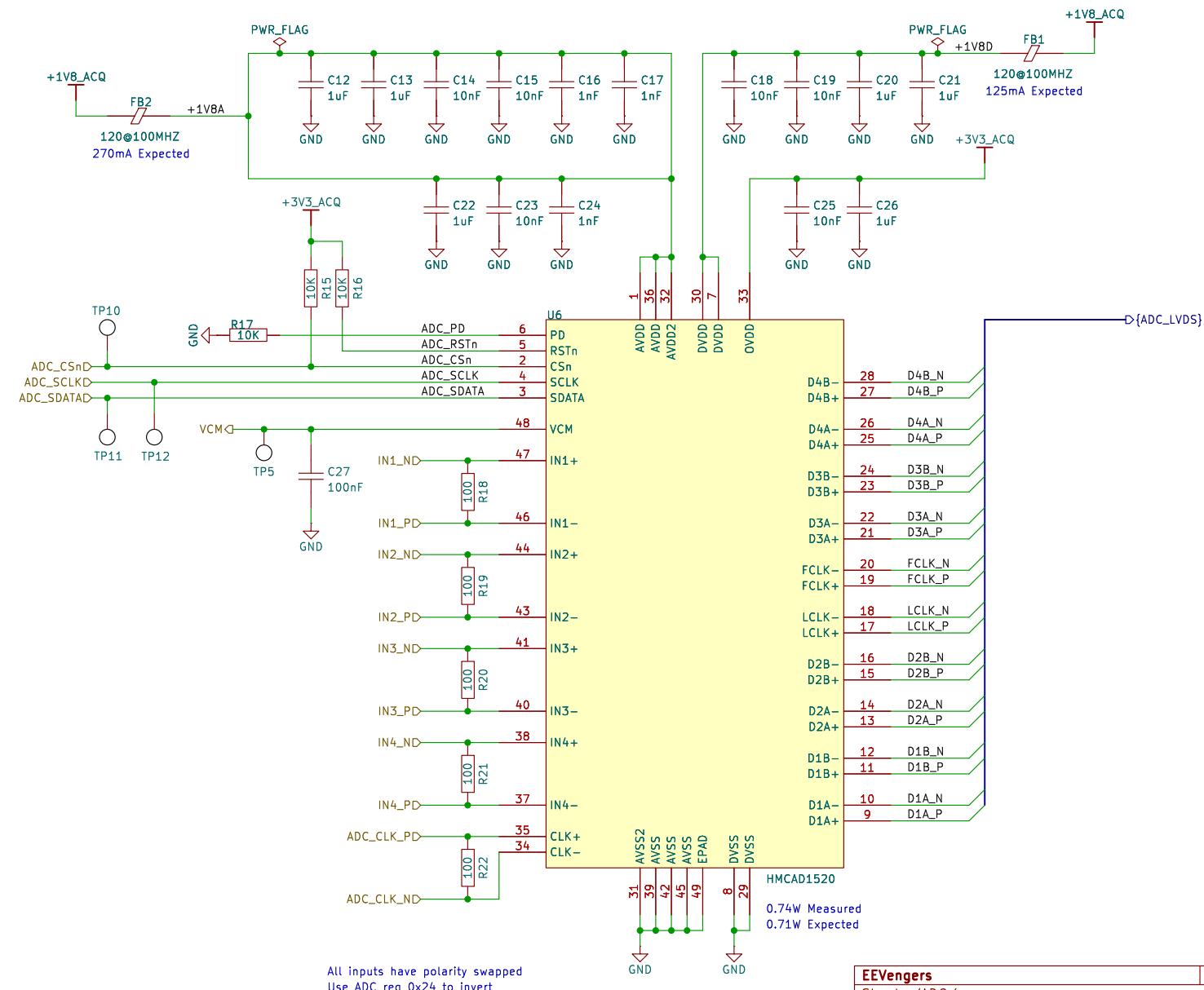


EEVengers
Sheet: /CH4/
File: FE_Channel.kicad_sch
Title: ThunderScope
Size: A3 Date: Rev: 5
KiCad E.D.A. 8.99.0 - 3402-gadd58faa30 Id: 2/16





1 2 3 4 5 6

ADC

EEVengers

Drawn by: Aleksa Bjelogrlic

Sheet: /ADC/

File: ADC.kicad_sch

Title: ThunderScope

Size: A4 Date:

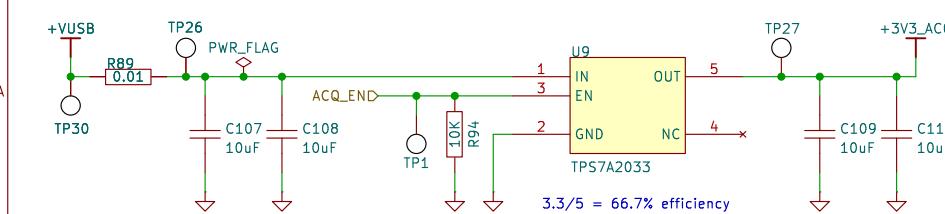
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Rev: 5

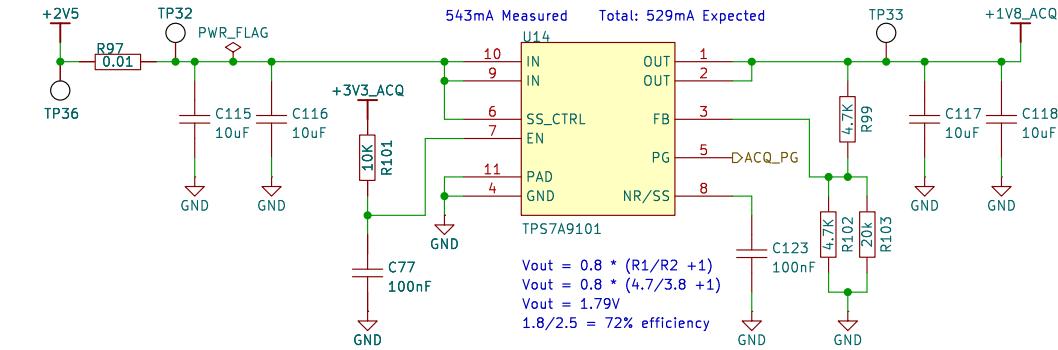
Id: 5/16

1 2 3 4 5 6

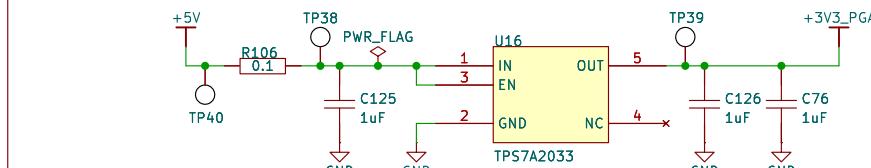
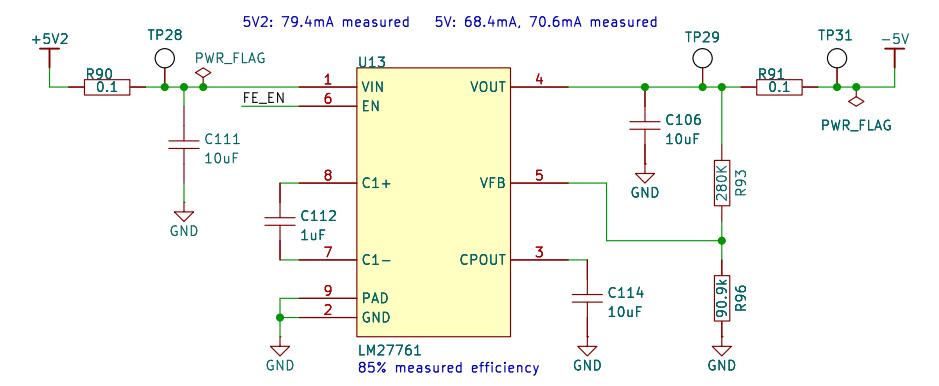
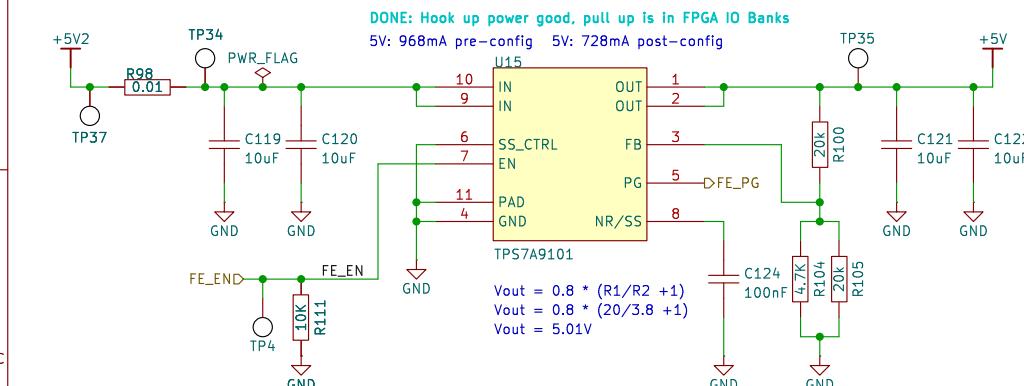
Acquisition Voltage Regulators



DONE: Hook up power good, pull up is in FPGA IO Banks



Front End Voltage Regulators



EEVengers

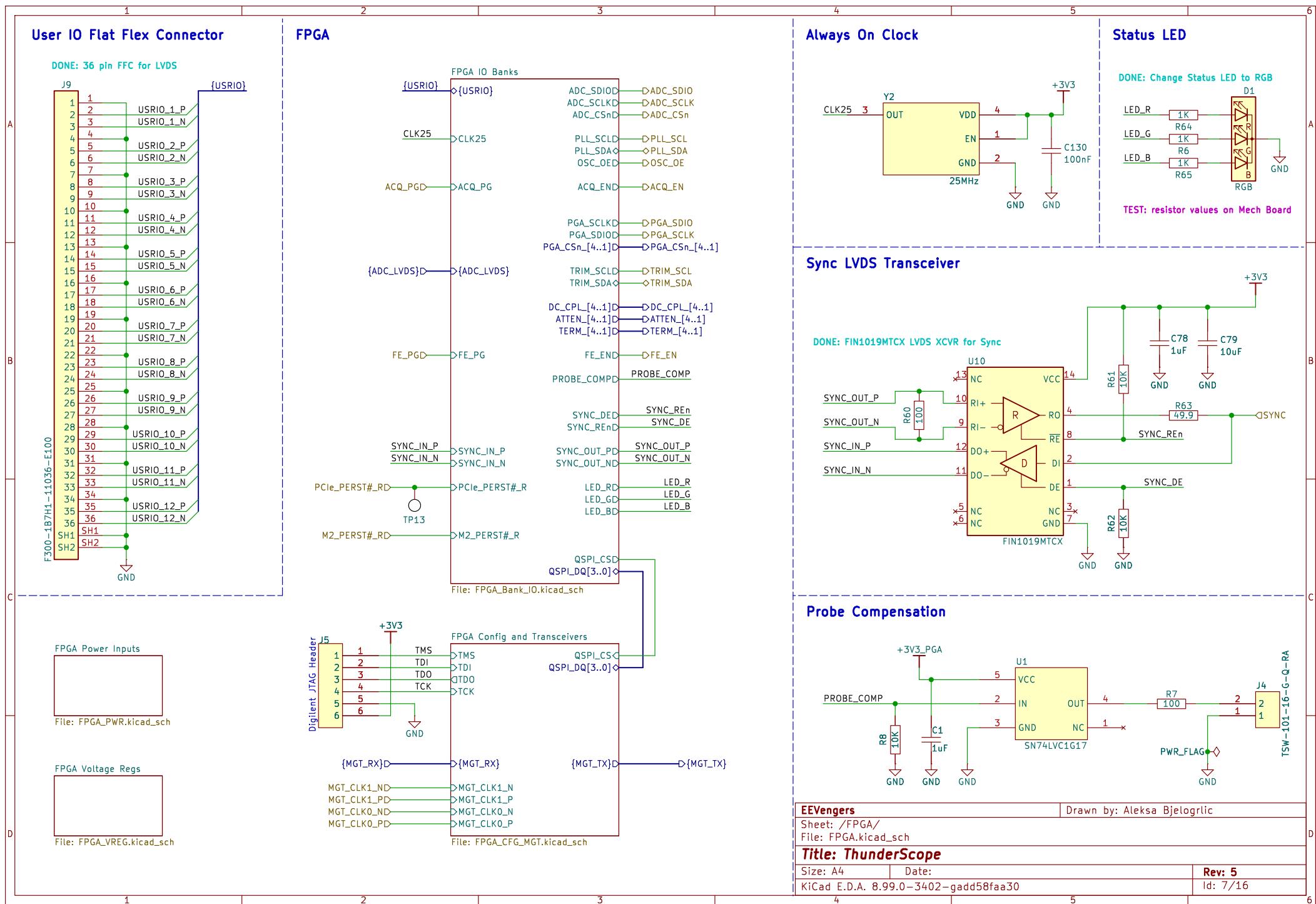
Sheet: /ACQ and FE Voltage Regs/
File: ACQ_FE_VREG.sch

Title: ThunderScope

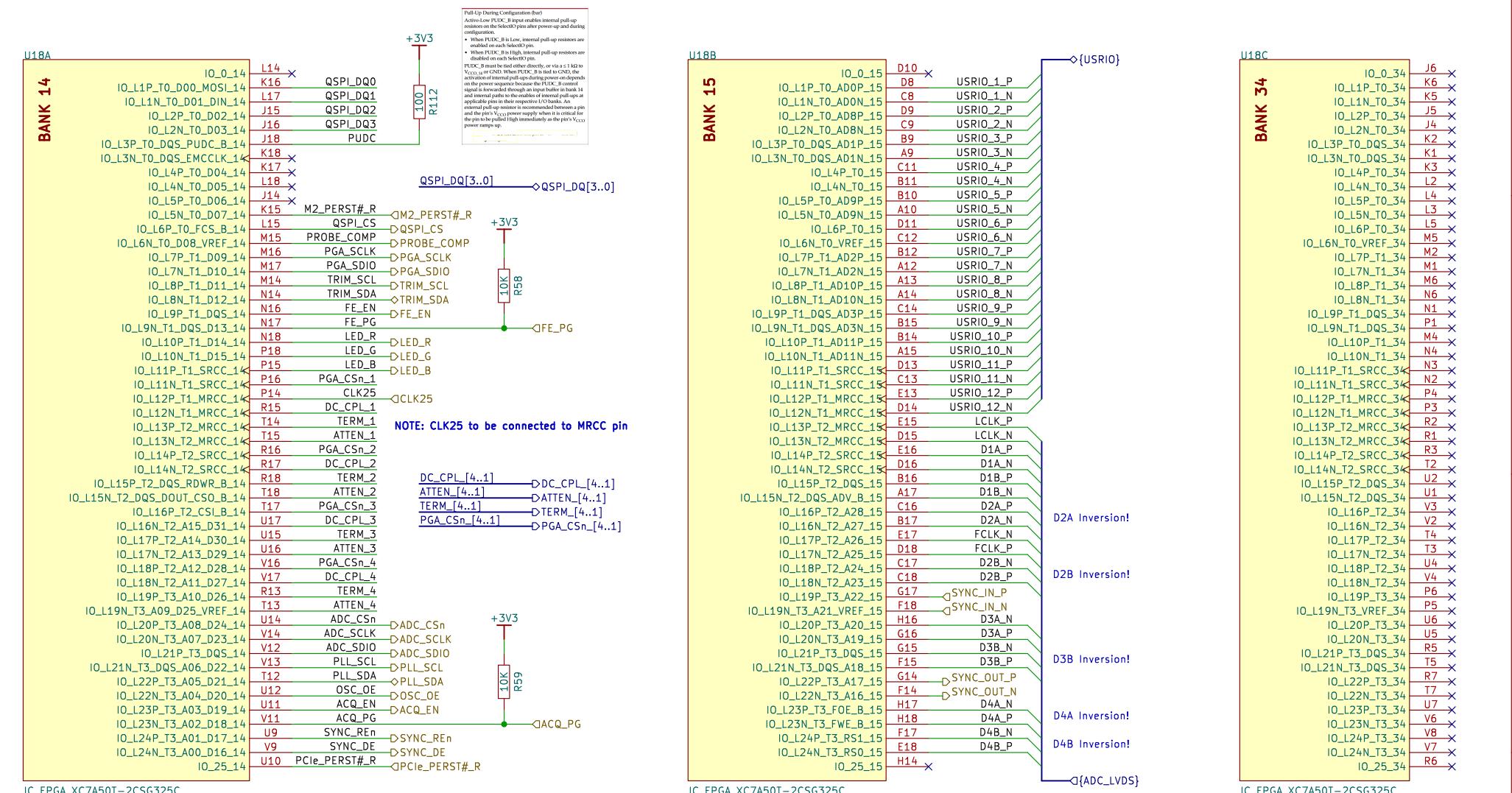
Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 6/16



FPGA IO Banks



EEVengers

Sheet: /FPGA/FPGA IO Banks/
File: FPGA_Bank_IO.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0 -3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

Rev: 5
Id: 8/16

FPGA Configuration

A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

Note: DONE has an internal pull-up resistor of approximately 10 k Ω . There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330 Ω resistor circuits are not required but can be used as they have been in previous generations.

Connect INIT_B to a $\leq 4.7\text{ k}\Omega$ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external $\leq 4.7\text{ k}\Omega$ pull-up resistor to V_{CCO_0} to ensure a stable High input, and

Table 2-1: 7 Series FPGA Configuration Modes			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

Table 2-6: Spartan-7, Artix-7 and Kintex-7 FPGA Configuration Mode, Compatible Memory and SDRAM Connection

Voltages, and CFGBVS Connection

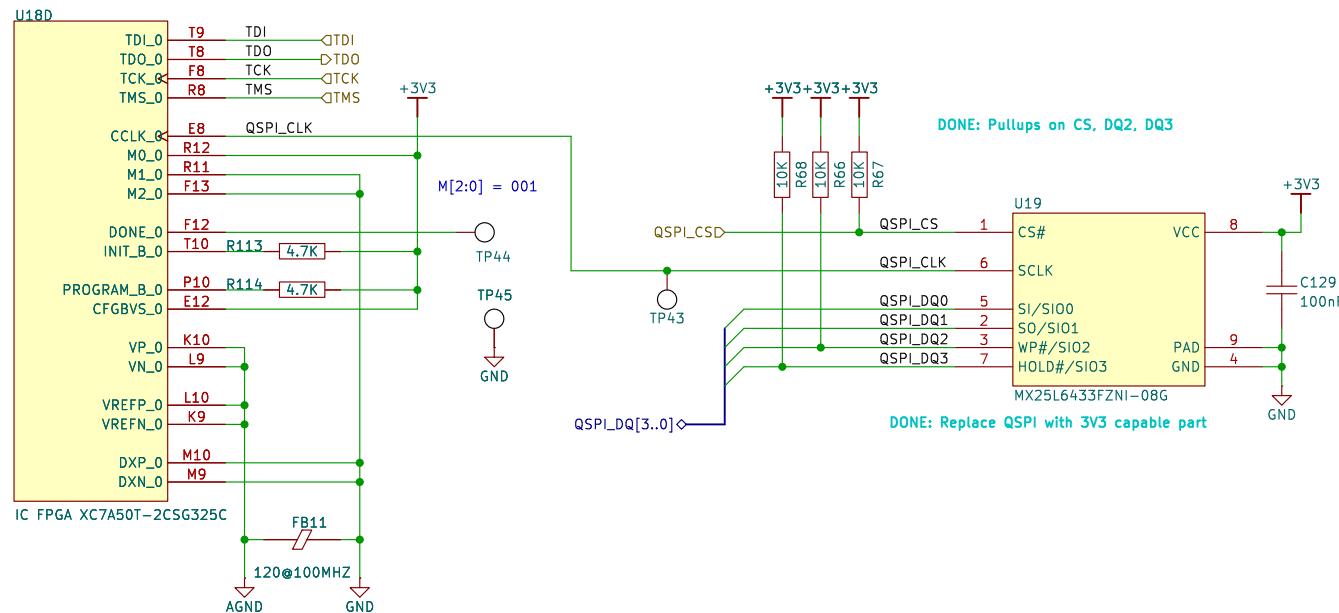
Configuration Mode	Banks Used	Configuration Interface I/O Multilane	Bank 0	HR Bank 14	HR Bank 15	CFGBVS
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		Voltage	VCCO_d	Notes
JTAG (only)	0	3.3V	Any	VCCO_d
		2.5V	Any	VCCO_d
		1.8V	Any	GND
		1.5V	Any	GND
Serial, SPI, or SelectMAP	0, 14 ^(d)	3.3V	3.3V	VCCO_d
		2.5V	2.5V	VCCO_d
		1.8V	1.8V	GND
		1.5V	1.5V	GND
		3.3V	3.3V	VCCO_d
BPI ^(e)	14, 15	2.5V	2.5V	VCCO_d
		1.8V	1.8V	GND
		1.5V	1.5V	GND
		3.3V	3.3V	VCCO_d
		2.5V	2.5V	VCCO_d

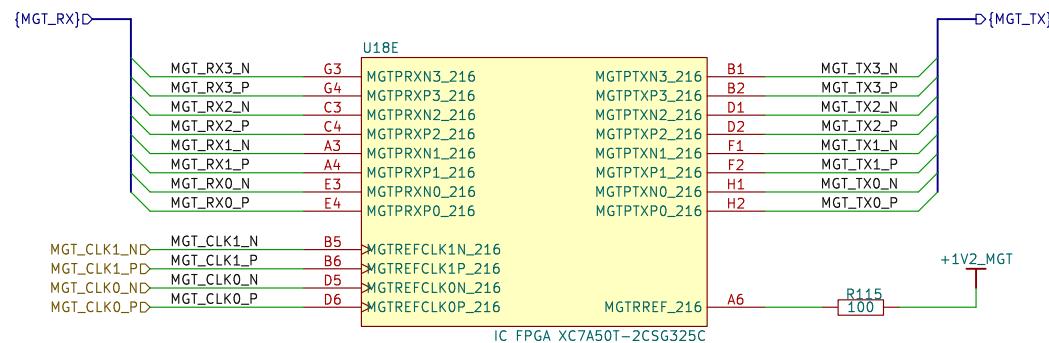
Notes:

- RS[1:0] for MultiBoot or Fallback are in bank 15 but are typically only used in BPI mode and not supported in SFI mode.

2. BPI mode is not available in the Spartan-7 family.



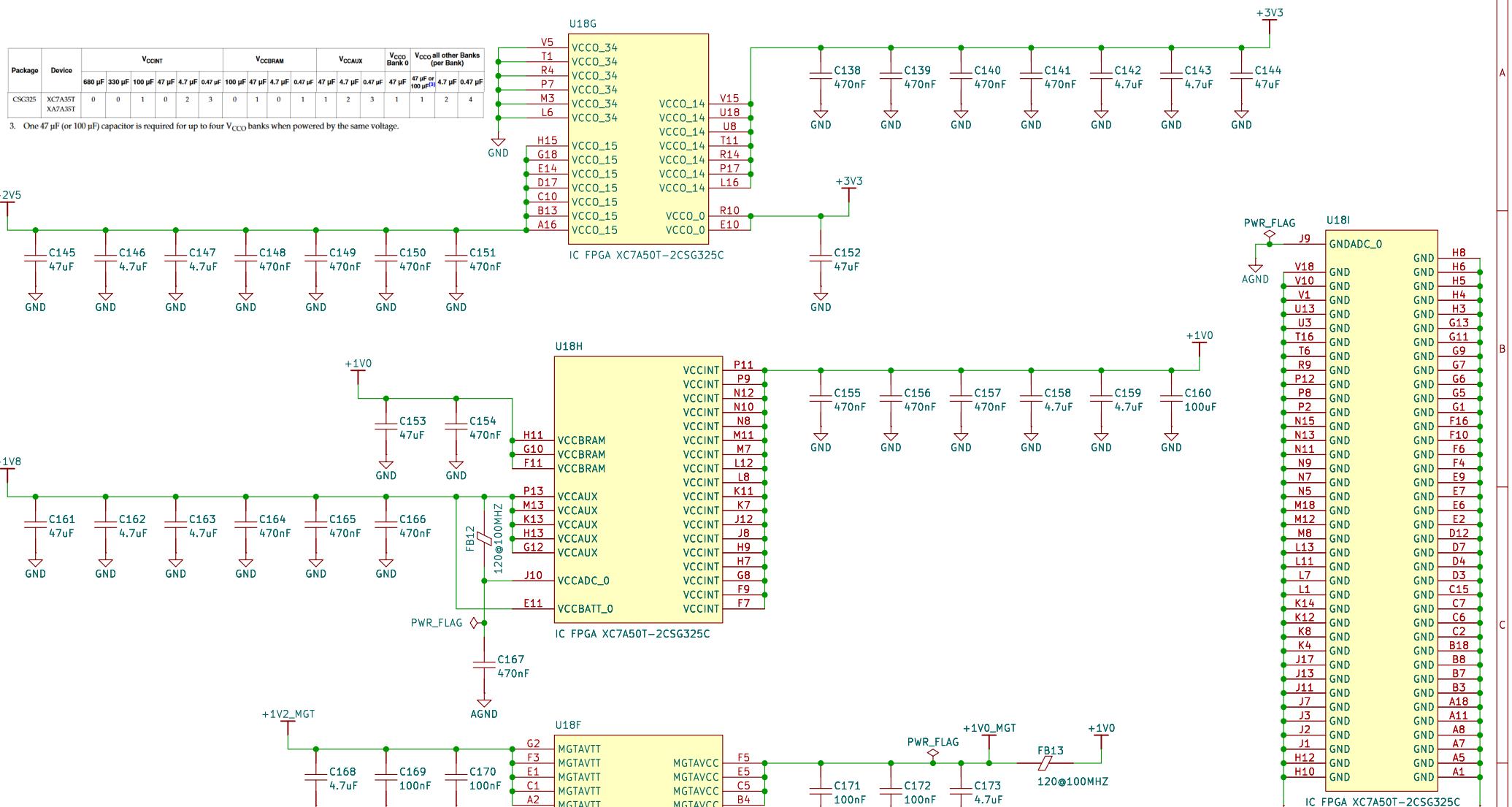
FPGA Transceivers



FPGA Power Inputs

Package	Device	V _{CCINT}				V _{CCBRAM}				V _{CCAUX}				V _{CCO} Bank 0	V _{CCO} all other Banks (per Bank)			
		680 µF	330 µF	100 µF	47 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF			
CSC325	XC7A35T XA7A35T	0	0	1	0	2	3	0	1	0	1	1	2	3	1	1	2	4

One 47 μ F (or 100 μ F) capacitor is required for up to four V_{CCO} banks when powered by the same voltage.



Capacitor	Package Pins			Value
	MGTAVCC	MGTAVTT	GND	
Cap1		F3	F4	0.1 µF
Cap2		A2	A1	
Cap3	B4		B3	
Cap4	F5		F6	

Qty/Power Supply Group		Capacitance (μ F)	Tolerance	Type
MGTAVCC	MGTAVTT			
1	1	4.7	10%	Ceramic
2	2	0.1	10%	Ceramic

FFVengers

Sheet: /FPGA/FPGA Power Inputs

File: FPGA_PWR.kicad_sch

Title: ThunderSce

Size: A4 Date:

Drawn by: Alekса Bielogorli

Page 10

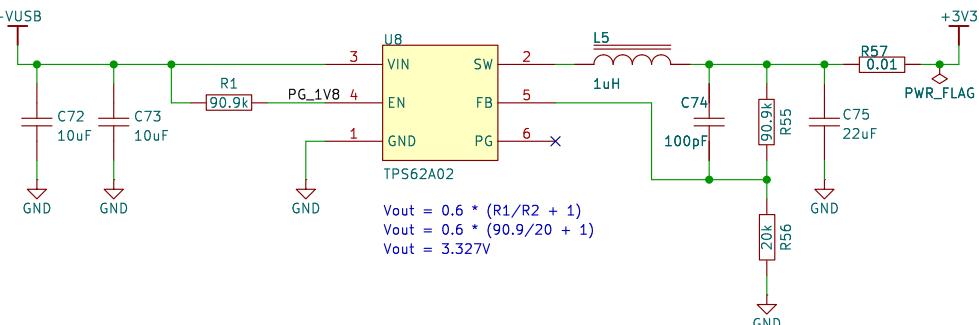
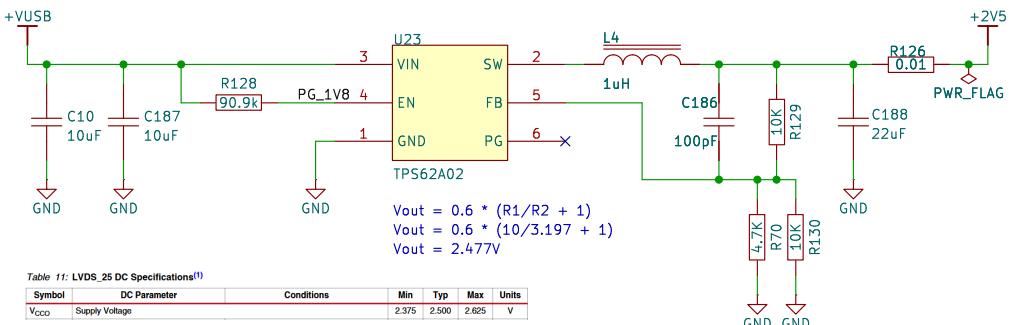
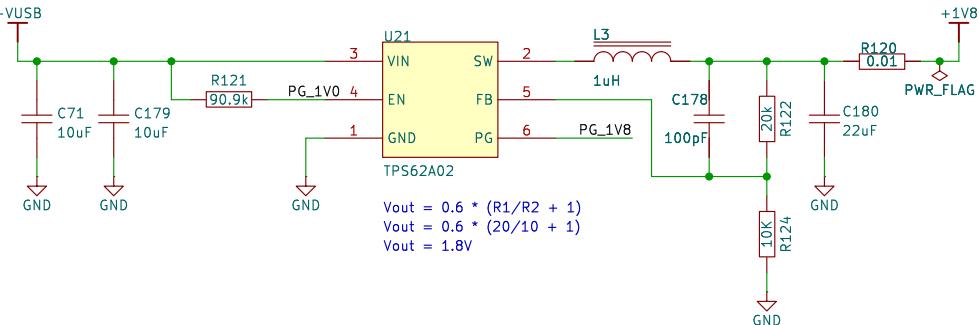
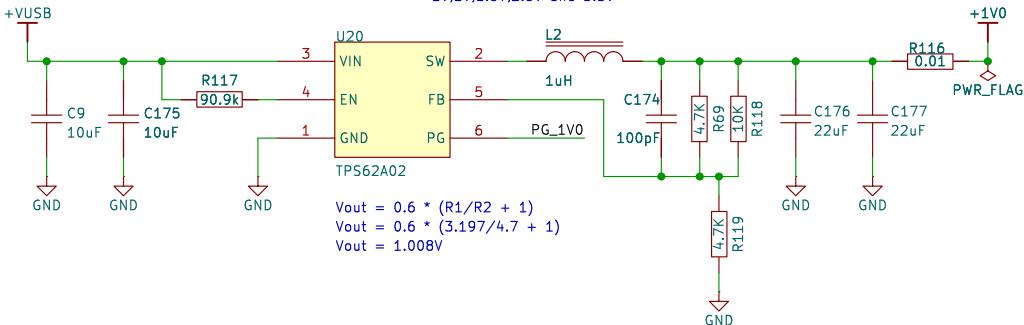
10 of 10

Rev: 5

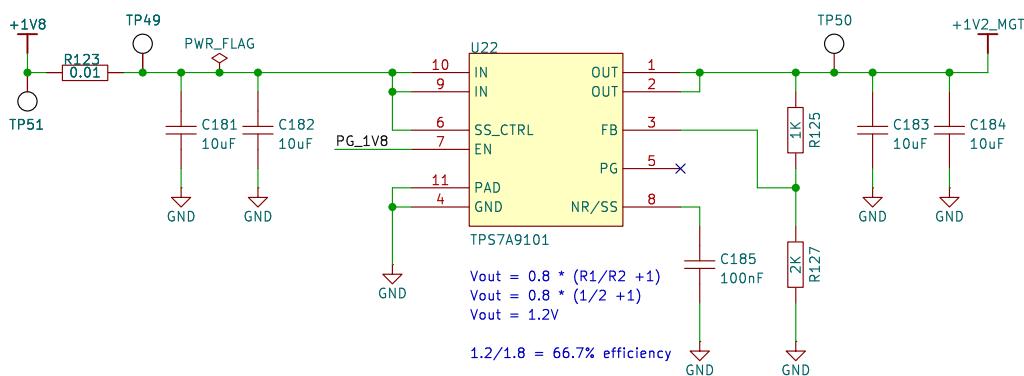
1 2 3 4 5 6

FPGA Voltage Regulators

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
1V,1V,1.8V,2.5V and 3.3V



Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V _{CCO}	Supply Voltage		2.375	2.500	2.625	V



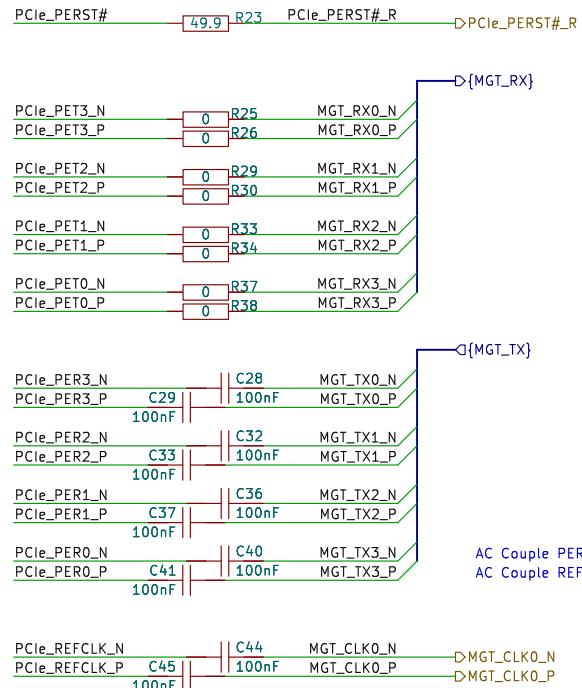
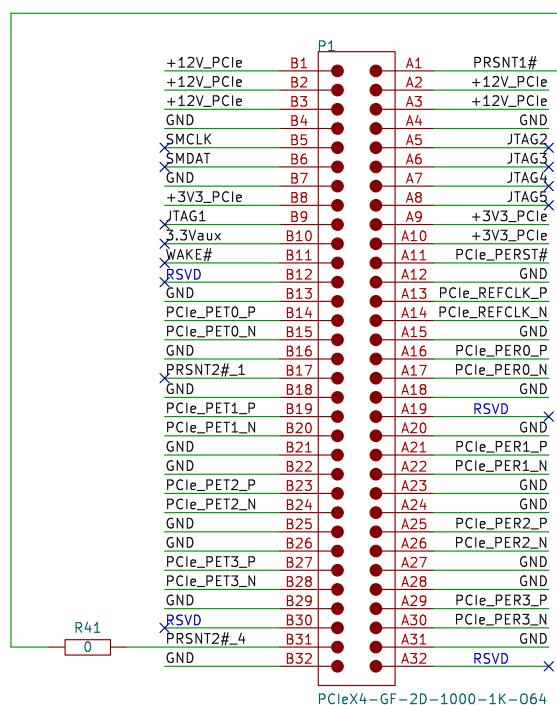
The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT
1V,1V,1.2V

EEVengers	Drawn by: Aleksa Bjelogrlic
Sheet: /FPGA/FPGA Voltage Regs/	
File: FPGA_VREG.kicad_sch	
Title: ThunderScope	
Size: A4	Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30	Rev: 5
	Id: 11/16

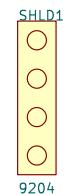
1 2 3 4 5 6

1 2 3 4 5 6

PCIe x4 Edge Connector



PCIe bracket



A

B

C

A

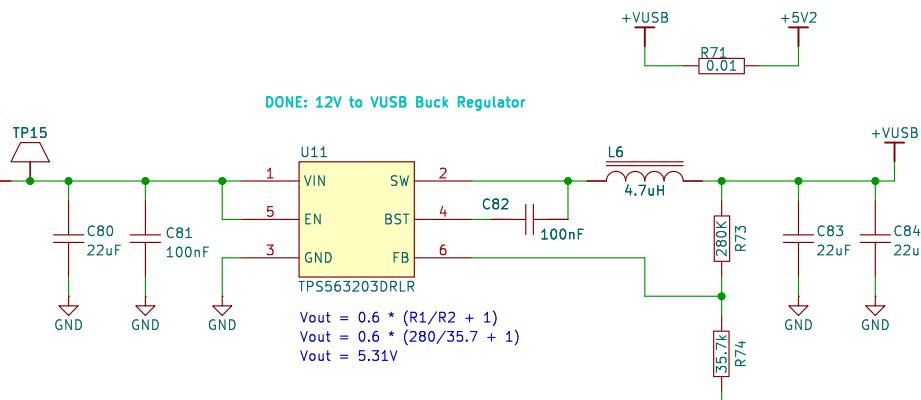
B

C

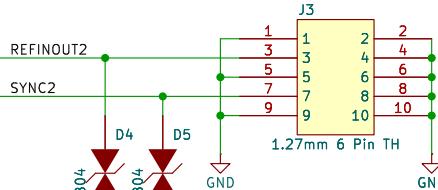
D

D

5V2 Buck Converter



Refclock and Sync Header



EEVengers

Sheet: /PCIe_x4/
File: CON_PCIe_X4.kicad_sch

Title: ThunderScope

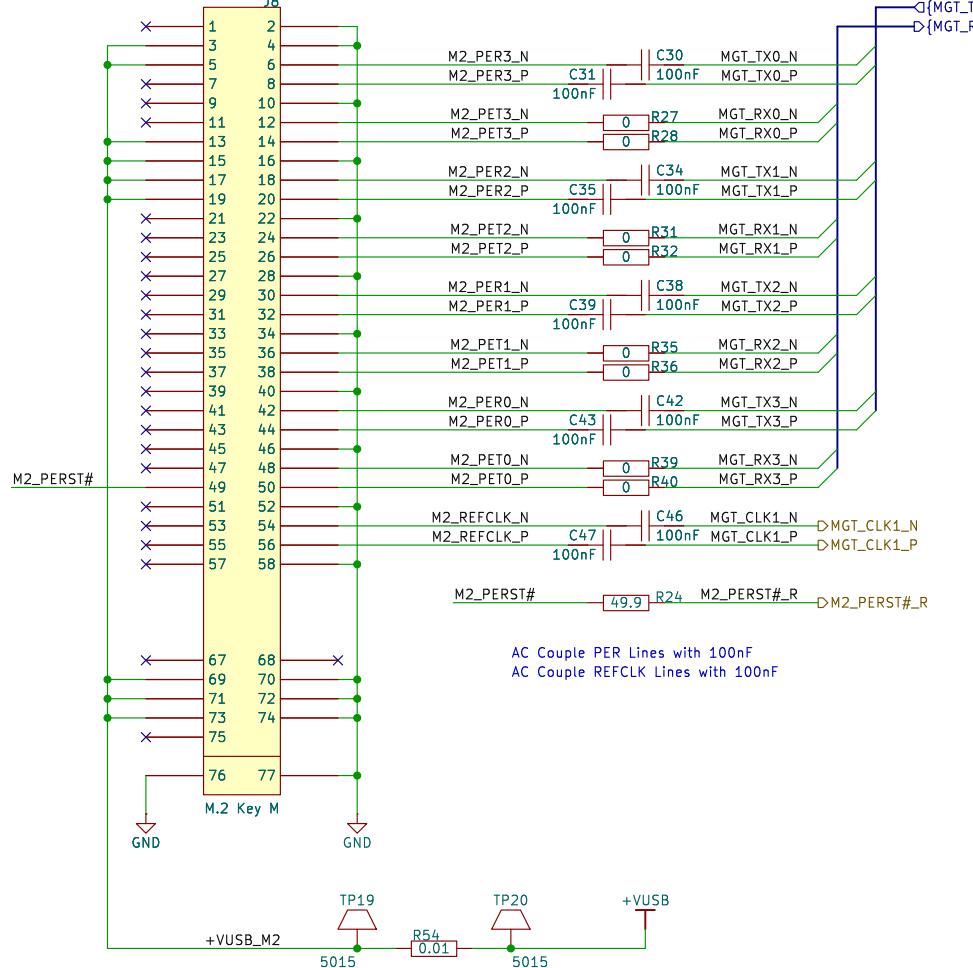
Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

Drawn by: Aleksa Bjelogrlic

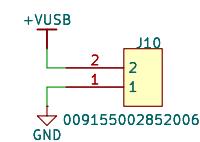
Rev: 5
Id: 12/16

1 2 3 4 5 6

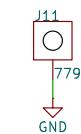
M.2 Key M Connector – Custom Pinout



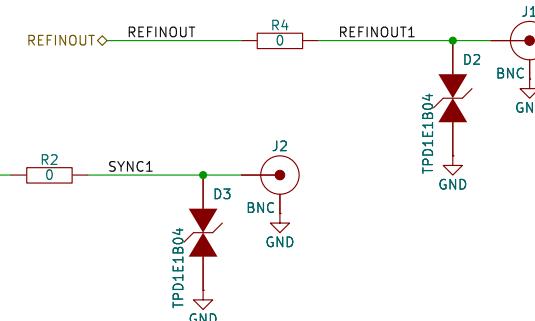
Fan Connector



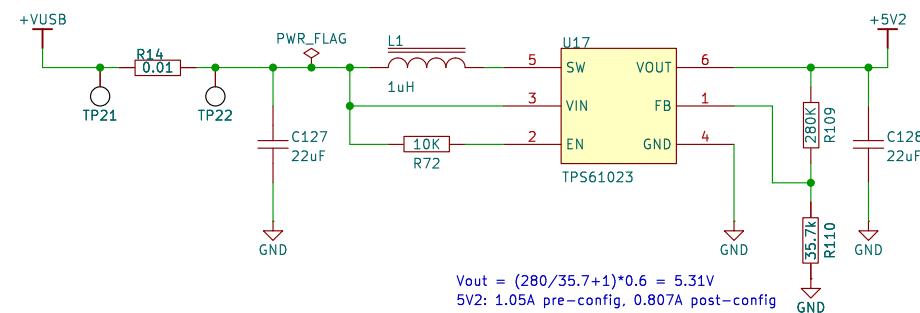
Ground Lug



Refclock and Sync BNCs



5V2 Boost Converter



EEVengers

Sheet: /M.2_Key_M/
File: M2_KEY_M.kicad_sch

Title: ThunderScope

Size: A4 Date:
KiCad E.D.A. 8.99.0-3402-gadd58faa30

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Rev: 5
Id: 13/16