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### SRM Institute of Science and Technology

## Tiruchirappalli Campus, Trichy – 621 105 Faculty of Engineering and Technology

Continuous Learning Assessment - I, Third Semester, August-2023.

21CSS201T - Computer Organization and Architecture (Regulations 2021)

Date: 10.08.2023/AN

Time: 60 Minutes

Max. Marks: 25

	Answer ALL Questions.	and the second
	$\mathbf{PART} \mathbf{A} - (5 \times 1 = 5 \text{ marks})$	
	The radical of Hexa decimal number system is:	3
1	A. 2.	CO 1
1.	B. 8.	<b>V</b>
	£. 16.	L1
	D. 15.	
	Find out the octal value of 85 <sub>10</sub> .	
	A. 35.	CO 1
2.	-B. 125.	1
	C. 75.	L3
	D. 45	
	Convert the (A2C6) <sub>16</sub> to decimal.	
	A. 2035.	00.1
3.	B. 51065.	CO 1
	C. 85005.	L3
	D. 41670.	
4.	Which code is called as self-complementary code?	CO 1
	A. BCD.	L1
	B. XS-3.	LI
	C. 2421.	
	D. Hexadecimal	
	Find 2's Complement of the number: 8	001
	A. 1000.	CO 1
	B. 1001.	L3
	C. 0111.	
	D. 1010.	

	Answer AL Questions.	/	
	PART B – $(2 \times 4 = 8 \text{ marks})$	1	
,	Elaborate on Number systems with suitable examples.	1	CO 1
5.		1.00	L2
	a) Convert (543.21) <sub>8</sub> into Hexa decimal. (2 marks)		CO 1
7.	b) Convert (CA7) <sub>16</sub> to Octal. (2 marks)		L3

	Answer ALL Questions.	
	<b>PART</b> C – $(1 \times 12 = 12 \text{ marks})$	, American
	a) Conver Binary to Gray: (4	4
	marks)	
	i) 110011 ii) 011101	
8.	b) Convert the number into XS-3: (4 marks)	CO 1
٥.	i) (34) <sub>10</sub> ii) (86) <sub>10</sub>	L3
	c) Find the two's complement of the number (43)10 and convert	Later State
	into Octal. (4	
	marks)	
	OR	
12	a) Perform the addition operation.	
	i) $1111+0111+1101+1011$ (3 marks)	
	ii) $(35)_{10} + (72)_{10} + (23)_{10}$ (3 marks)	
		CO1
9.	b) Perform the subtraction operation.	L3
	i) 10001-01111 (3 marks)	
	ii) $(65)_{10} - (32)_{10}$ (3 marks)	
	(3 marks)	

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Reg. No:

#### SRM Institute of Science and Technology

#### Tiruchirappalli- 621 105

Faculty of Engineering and Technology

Continuous Learning Assessment - II, Third Semester, September-2023.

21CSS201T - Computer Organization and Architecture

(II.Btech CSE, ECE) (Regulations 2021)

Date: 26.09.2023/AN

Time: 90 Minutes

Max. Marks: 50

	Answer ALL Questions.	
	<b>PAR</b> $\mathbf{A} - (10 \times 1 = 10 \text{ marks})$	
1.	The sign magnitude is represented using:  A. MSD (Most Significant Digit)  B. LSD (Least Significant Digit)  C. MSD (Middle Significant Digit)  D. LSD (Last Significant Digit)	COI LI
2.	makes decisions based on a combination of digital inputs.  A. AND gate B. NOT gate C. Neither A or B D. Both A and B	CO1 L2
3.	Which of the following instruction preserves the value in LOCA and adds the value to R()?  A. PRESERVE LOCA,R0  B. ADD LOCA,R0  C. REPLACE LOCA,R0  D. READD LOCA,R0	CO2 L3
4.	holds the value of information during transfer  A. Bus B. Register  Buffer register D. Processor	CO2 L2

5.	If a	
	If a computer is 64 bits a single	
	If a computer is 64 bits, a single word can hold uptoASCII characters.	
	A. 6	CON
	8	CO2
	C. 16	L3
*	DD 4	1
6.	At some point, when the current instruction I is it is	
	Polity Wilell the current instruction has 6 11 1	
	executing and the control moves to the next instruction to be	
	executed. What happens to the Program Counter (PC)?	CO <sub>2</sub>
	A. Decremented	100000000000000000000000000000000000000
	B. Does not change	L3
	C. Points to the current instruction	
	and to the current instruction.	1.0
7.	V./ Incremented.	
1.	32 bits	
	$b_{31} b_{30} \cdots b_1 b_0$	
		COS
	In the above figure, if b <sub>31</sub> value is 1, what can be described about	CO2
	the whole number stored in the 32 bits?	L3
	A. Positive	
	Negative Negative	
	C. Decimal	
	D. None of the above.	
8.		
0.	The left hand side (LHS) of De Morgan's theorem represents a	
	NAND gate with inputs A and B, whereas the right hand side	
	(RHS) of the theorem represents on OD	
	(Ki is) of the theorem represents an OR gate with inverted inputs	CO3
	(RHS) of the theorem represents an OR gate with inverted inputs.  A. Simple NAND	CO3
	A. Simple NAND	CO3 L4
	A. Simple NAND  Bubbled OR	
	A. Simple NAND Bubbled OR C. Bubbled NOR	
0	A. Simple NAND  Bubbled OR  C. Bubbled NOR  D. XNOR	
9.	A. Simple NAND  Bubbled OR  C. Bubbled NOR  D. XNOR  is a powerful tool in digital design.	
9.	A. Simple NAND  Bubbled OR  C. Bubbled NOR  D. XNOR  is a powerful tool in digital design.  A. Logic gates	
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	A. Simple NAND  Bubbled OR  C. Bubbled NOR  D. XNOR  is a powerful tool in digital design.  A. Logic gates  De Morgan's theorem  C. Bubbled NOR  D. ALU (Arithmetic and Logic Unit)	L4 CO3
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	A. Simple NAND Bubbled OR C. Bubbled NOR D. XNOR  is a powerful tool in digital design. A. Logic gates B. De Morgan's theorem C. Bubbled NOR D. ALU (Arithmetic and Logic Unit)  The LHS of De Morgan's theorem represents a NOR gate with inputs A and B, whereas the RHS represents an AND gate with inverted inputs.	CO3 L1
	A. Simple NAND  Bubbled OR  C. Bubbled NOR  D. XNOR  is a powerful tool in digital design.  A. Logic gates  De Morgan's theorem  C. Bubbled NOR  D. ALU (Arithmetic and Logic Unit)  The LHS of De Morgan's theorem represents a NOR gate with inputs A and B, whereas the RHS represents an AND gate with inverted inputs.  A. Simple NAND	CO3 L1
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ACCOUNTS AND VALUE OF THE	Answer Any Four Questions.	
	<b>PART B</b> – $(4 \times 4 = 16 \text{ marks})$	
11.	Explain the relationship between the memory and processor with suitable diagram.	L2
12.	Write the operating steps involved in executing an instruction	CO2 L2
13.	Define byte addressability and what are the ways the byte address can be assigned across words?	L2
14.	Explain the AND, OR NAND and EX-OR gate with its truth- table and logical symbol.	CO2 L3
15.	Perform the binary multiplication for the following:  (a) (13) <sub>10</sub> * (23) <sub>10</sub> (2marks	1 1 3
16.	(b) (45) <sub>10</sub> * (34) <sub>10</sub> (2marks)  Perform the BCD Subtraction for the following:  (a) (565) <sub>10</sub> + (346) <sub>10</sub> (2marks)  (b) (782) <sub>10</sub> + (477) <sub>10</sub> (2marks)	

	Answer ALL Questions.	
	<b>PART C</b> $-(2 \times 12 = 24 \text{ marks})$	
17.	(a) Apply the zero address and two address instructions for the following expressions  i) X=(A+B+C)×(D×Z)+(N+M)  ii) n=(a×n)+(b+s)÷(f×d)  or  (b) Apply the one address and three address instructions for the following expressions  i) Z=(A-B+C)*(D/E)-(F+G+H)  ii)M=(N+6)/(O+P+Q)*K	CO3 L3
18.	(a) What is the role of adders in ALU process? Explain it with its types  or  (b)Explain the theorems used to solve the Expressions of Boolean algebra with corresponding truth table and list its applications.	CO3 L2



### SRM Institute of Science and Technology Tiruchirappalli- 621 105

Faculty of Engineering and Technology

# Continuous Learning Assessment - III, Third Semester, September-2023. (Regulations 2021) (CSE and ECE)

Date: 08.11.2023/AN

Time: 90 Minute's Max. Marks: 50

	Answer ALL Questions.	
•	PART A - (10 x 1 = 10 marks)	
	Poeth Algorithm is implemented for	
1.	A. Unsigned Multiplication  B. Signed Multiplication	CO 3
•	C. Division D. Carry Save addition	LI
	Carry-Save Adder (CSA) is also known as	
	A. 2-2 adder	•
2.	B. 3-2 adder	CO 3
۷.	C. Multiplier	LI
	D. Divider	
	In Restoring method, if MSB of A is 0 then, Q <sub>0</sub> will be.  A. 10	4 1
3.	B. 01	CO 3
٥.	C. 0	L3
	D. 1	
4.	Which is not a IEEE 754 basic component?  A. Normalized Monti	CO 4
	A. Normalia 754 basic component?	LI
	A. Normalized Montissa  B. Exponent	LI
	C. The biggs	
	oldsed expo-	2
5.	D. The Sign of Mantissa  IR<- [PC], this instruction belongs to phase.  B. execution	CO
	A. assignment dellon helphase.	L3
	B. execution	נט
	C. fetch	
	D. addition	
6.	IVIDR has	CO 4
	A a line	L3
	B. 2,2 output(s)	L3

	C. 1,1	. *
	D. 1,2	1
7.	Which of the following is not leignal?	CO 4
	Which of the following is not a conditional signal?  A. wake	L3
	B. start	
	C. stop	
	D. restart	
8.	MFC stands for	CO 4
	A. Member Function Connect	L3
	D. MICHIOLY FUNCTION O	
	C. INCHIOLALING	
	D. Member Function Complete	
9.	ARM works based on	CO 5
	A. ISA	L1
	B. RISC	
	C. CISC	
	D. 8085	
10.	Parallelism cannot be performed at	CO 5
	A. Bit level	L3
	B. Instruction level	
	C. Task level	
	D. Sentence level	

Answer Any Four Questions.  PART B – $(4 \times 4 = 16 \text{ marks})$		
11.	Write the control sequence for the following instruction	CO4
12.	Perform the unsigned multiplication for the following numbers:	CO3
13.	How an instruction is executed with a single processor bus?  Explain it with a suitable diagram	CO4
14.	Divide 63 by 8 using Restoring method	L3 CO3
18.	Define Parallelism Explain its types.	L3
1.6	Perform multiplication with a stream	CO5
16.	using pipelining method  A <sub>i</sub> *B <sub>i</sub> *C <sub>i</sub> where i=1 to 7	CO2 L3

	Answer ALL Questions.	
	PART C – (2 x 12 = 24 marks)  Explain about carry look-ahead adder and implement 4bit value as example	CO3, L2
17.	or (b) Compare sequential and pipelining process by implementing	CO4, L2
18.	(a) Describe about Flynn's classification with its types or (b) Explain about the different types of hazards with an example.	CO4,5 L2