SRM Institute of Science and Technology
Tiruchirappalli Faculty of Engineering and Technology
Dept. of Electronics and Communication Engineering

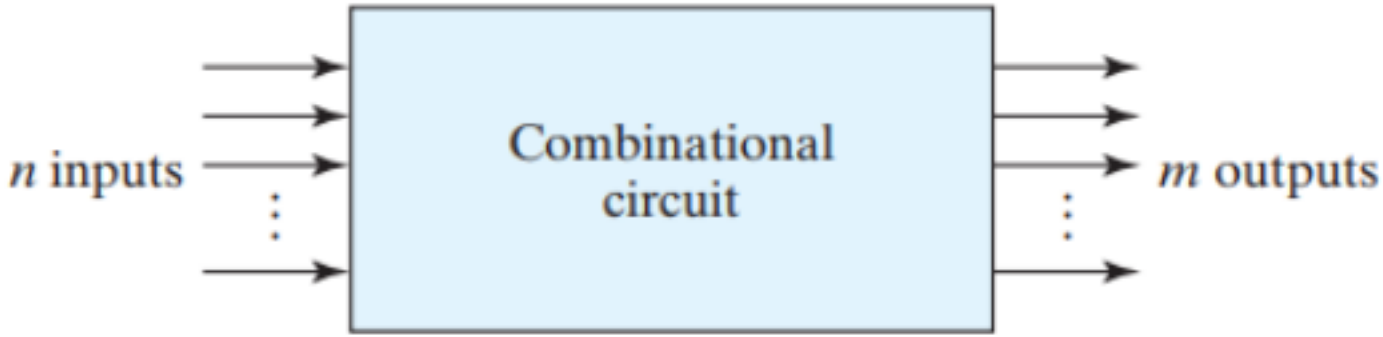
21ECC303T
VLSI Design and Technology

Unit III – VLSI subsystem design and Introduction to CMOS logic styles

Prepared by
Dr. S. Aditya,
AP/Dept. of ECE,
SRMIST Tiruchirappalli

Combinational Circuit

- Interconnection of logic gates
- n-inputs are obtained by externalsource
- *m* output variables are produced by the internal combinational logic circuit and go to anexternal destination
    - The diagram of a combinational circuit has logic gates with no feedback paths or memory



elements

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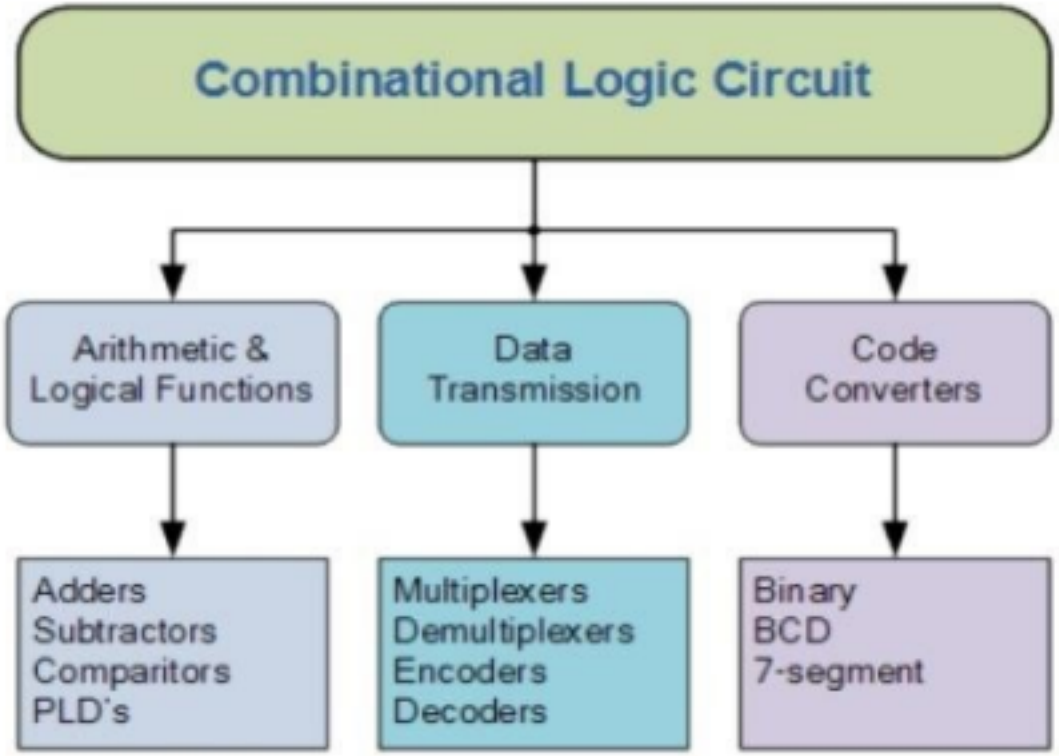
Classificaition

Classification of Combinational Logic



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Steps in Combinational Circuit Design

The different steps involved in the design of a combinational logic circuit are asfollows:

1. Statement of the problem.

2. Identification of input and output variables.

3. Expressing the relationship between the input and output variables. 4. Construction of a truth table to meet input–output requirements.

5. Writing Boolean expressions for various output variables in terms of input variables. 6. Minimization of Boolean expressions.

7. Implementation of minimized Boolean expressions.

Decoders

•A decoder, is a combinational circuit that decodes the information on n input lines to a maximum of 2^n unique output lines.

• It has an n-bit binary input code and one activated output out of 2^n output code.

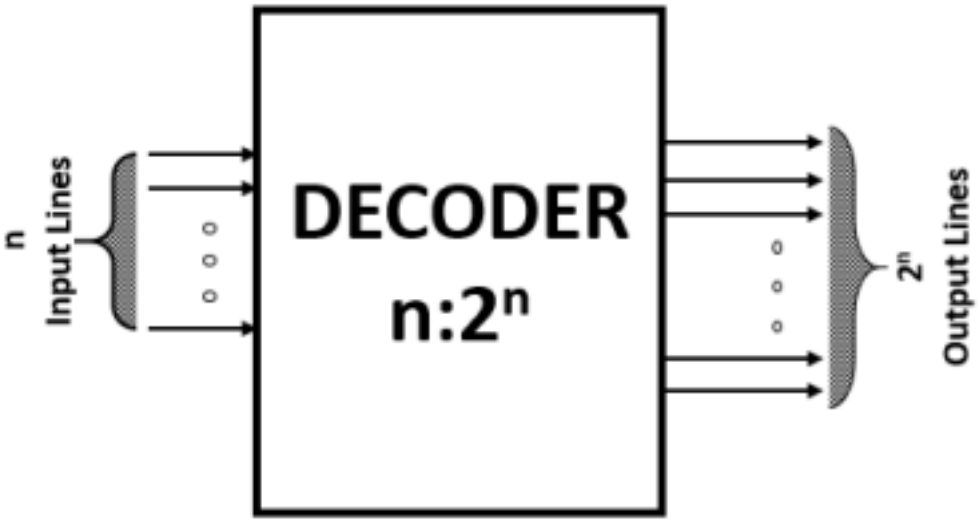
• A binary decoder is used when it is necessary to activate exactly one of 2^n outputs based on an n-bit input value.

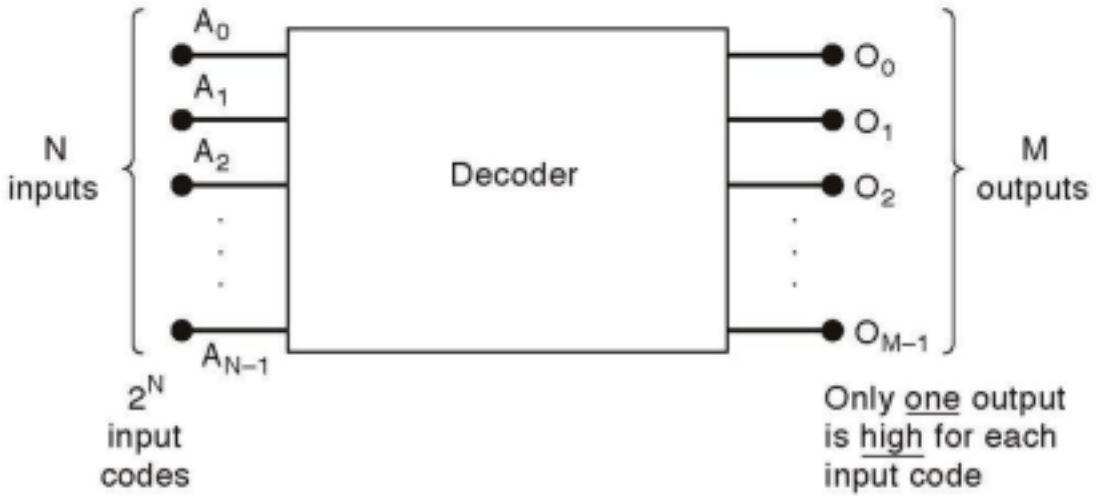
•It is similar to demultiplexer, with only one exception that it has no data input.

Input – n

Output – 2^n

Decoder – n : 2^n





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Decoders

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Comparators

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Adders

Standard adder cell

Adder - RCA

• Abinary adder is a digital circuit that produces the arithmetic sum of two binary numbers. • It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of the next full adder in the chain.

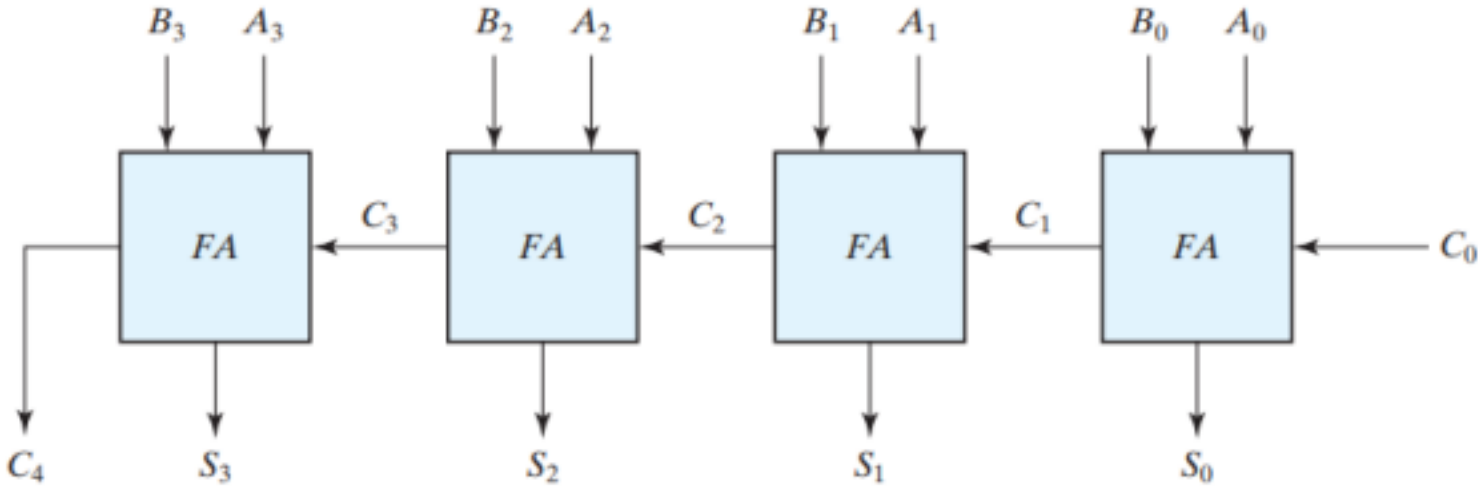

FIGURE 4.9
Four-bit adder

Subscript *i*:	3	2
Input carry	0	1
Augend	1	0
Addend	0	0
Sum	1	1
Output carry	0	0

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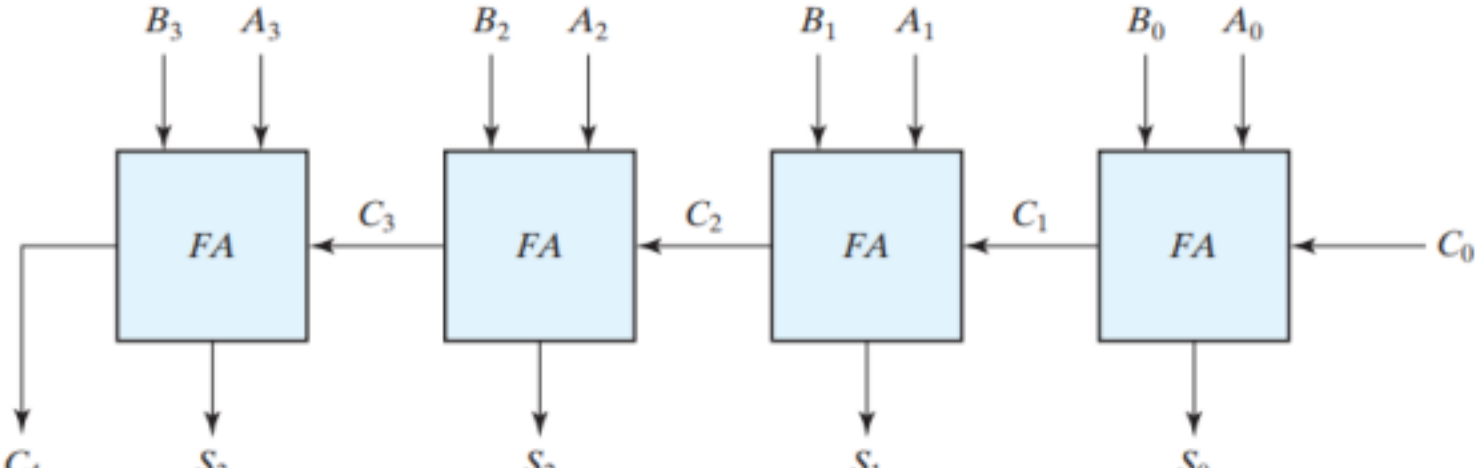
Adder - RCA

- Inputs $A3$ and $B3$ are available as soon as input signals are applied to the adder. However, input carry $C3$ doesnot settle to its final value until $C2$ is available from the previous stage. Similarly, $C2$ has to wait for $C1$ and so on down to $C0$. Thus, only after the carry propagates and ripples through all stages will the last output $S3$ and carry



One Gate Delay (Δ)

Each stage needs 2Δ to generate carry
Total delay in n-bit RCA **2nΔ**

Drawback: The time required to add long data words may be prohibitive, because the carry has to propagate from the least significant bit to the most significant bit.

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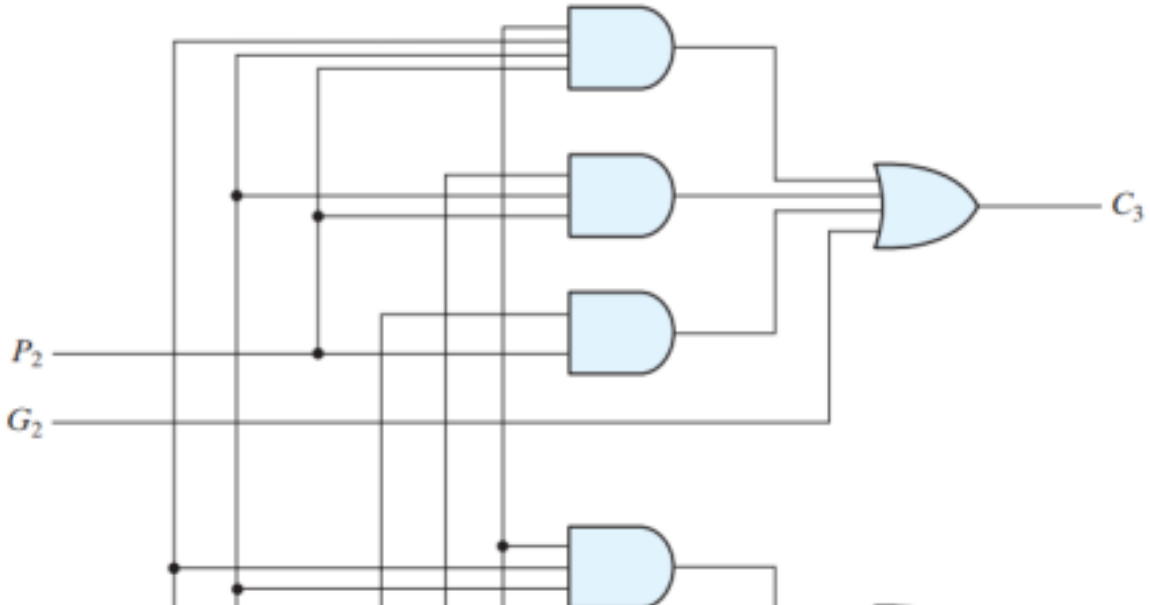
Adder - CLA

The carry propagation time is an important attribute of the adder because it limits the speed with which two numbers are added.

carry look ahead logic is a technique for reducing the carry propagation time in a parallel adder

Pi called CARRY PROPAGATE and Gi called CARRY GENERATE.



$$S_i = P_i \oplus C_i$$
$$C_{i+1} = G_i + P_i C_i$$

C_0 = input carry

$C_1 = G_0 + P_0 C_0$

$$C_2 = G_1 + P_1 C_1 = G_1 + P_1(G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0$$
$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 = P_2 P_1 P_0 C_0$$

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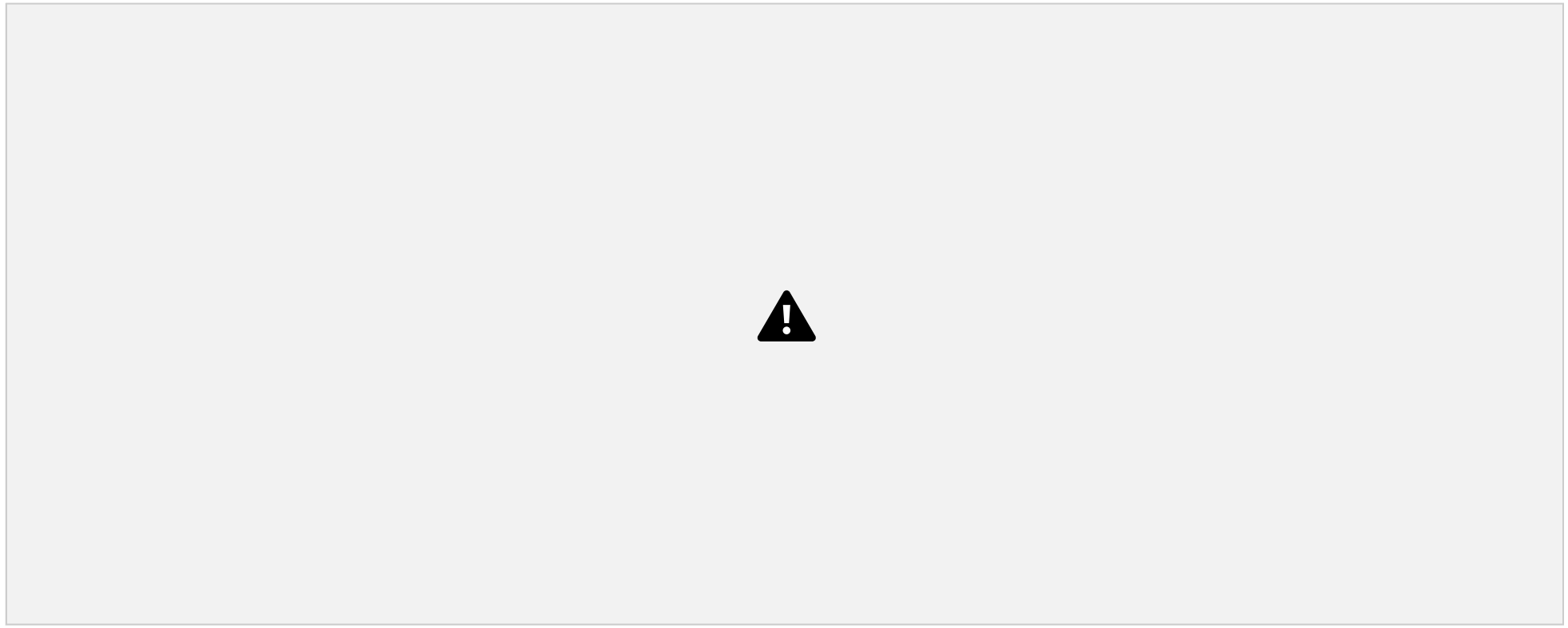
Adder - CLA



$$P_i = A_i \oplus B_i$$
$$G_i = A_i B_i$$

$$C_2 = G_1 + P_1 C_1 = G_1 + P_1(G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0$$
$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 = P_2 P_1 P_0 C_0$$

Adder - CLA

Let Δ be One gate delay •Delay of one Δ to calculate p, g

•Delay of two Δ to generate Ci

•Delay of two Δ to generate Si

•Total of five Δ regardless of n.

CLA compared to ripple-carry adder:

• 4 times Faster but delay still linear (w.r.t. # of bits)

• Larger area

  • P, G signal generation

  • Carry generation circuit for each bit position (no re-use) •

  Carry generation circuits

• Limitation: cannot go beyond 4 bits of look-ahead

• Large fan-in slows down carry generation

Adder - CLA

Verilog code

```
module CLA_4bmod(sum,c_4,a,b,c_0);
input [3:0]a,b;
input c_0;
output [3:0]sum;
output c_4;
wire p0,p1,p2,p3,g0,g1,g2,g3;
wire c1,c2,c3,c4;
assign
p0=a[0]^b[0], p1=a[1]^b[1], p2=a[2]^b[2], p3=a[3]^b[3], g0=a[0]&b[0], g1=a[1]&b[1], g2=a[2]&b[2],g3=a[3]&b[3];
assign
c1=g0|(p0&c_0), c2=g1|(p1&g0)|(p1&p0&c_0), c3=g2|(p2&g1)|(p2&p1&g0)|(p2&p1&p0&c_0),
c4=g3|(p3&g2)|(p3&p2&p1&g1)|(p3&p2&p1&g0)|(p3&p2&p1&p0&c_0);
assign
sum[0]=p0^c_0, sum[1]=p1^c1, sum[2]=p2^c2, sum[3]=p3^c3, c_4=c4;
endmodule
```

Adder - CSL

Consists of two ripple carry adders and a multiplexer.

• Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders). • The calculation is performed twice, one time with the assumption of the carry-in being zero the other assuming it will be one.

• After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the

multiplexer once the correct carry-in is known

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Adder - CSL

- The number of bits in each carry select block can be uniform, or variable.
- In the uniform case, the optimal delay occurs for a block size of (O$\sqrt{n}$).
- When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it

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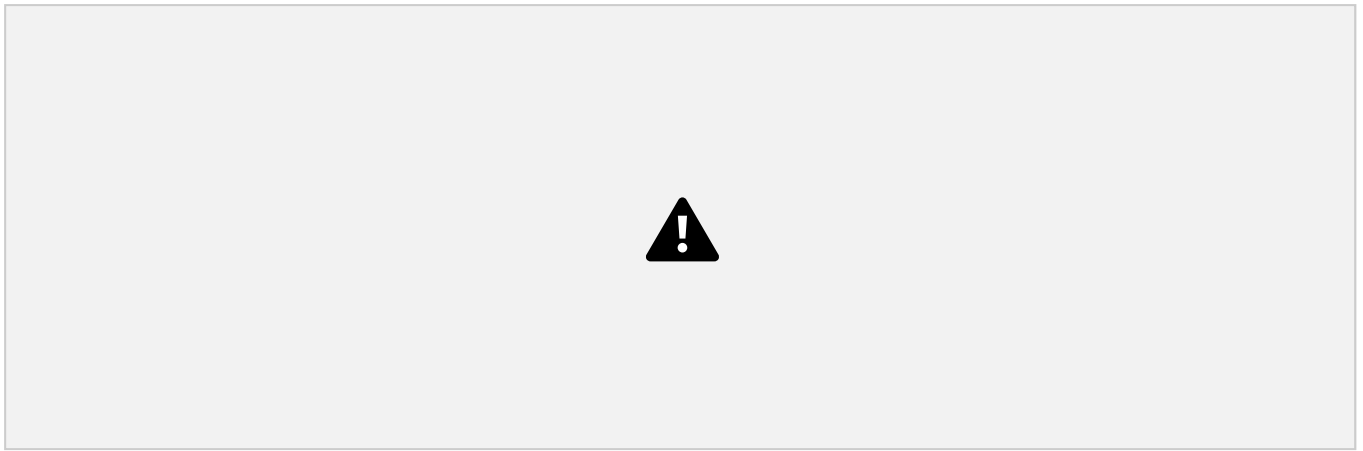
Adder - CSA

- A carry-save adder or CSA is a type of digital adder mainly used for computing the sum of a minimum of three or above binary numbers

very efficiently.

- This type of adder is very different as compared to other types because it doesn't transmit the middle carries toward the next stages, but in its place, it saves the carry & addends to the sum of the next stage with another fuller adder (FA).



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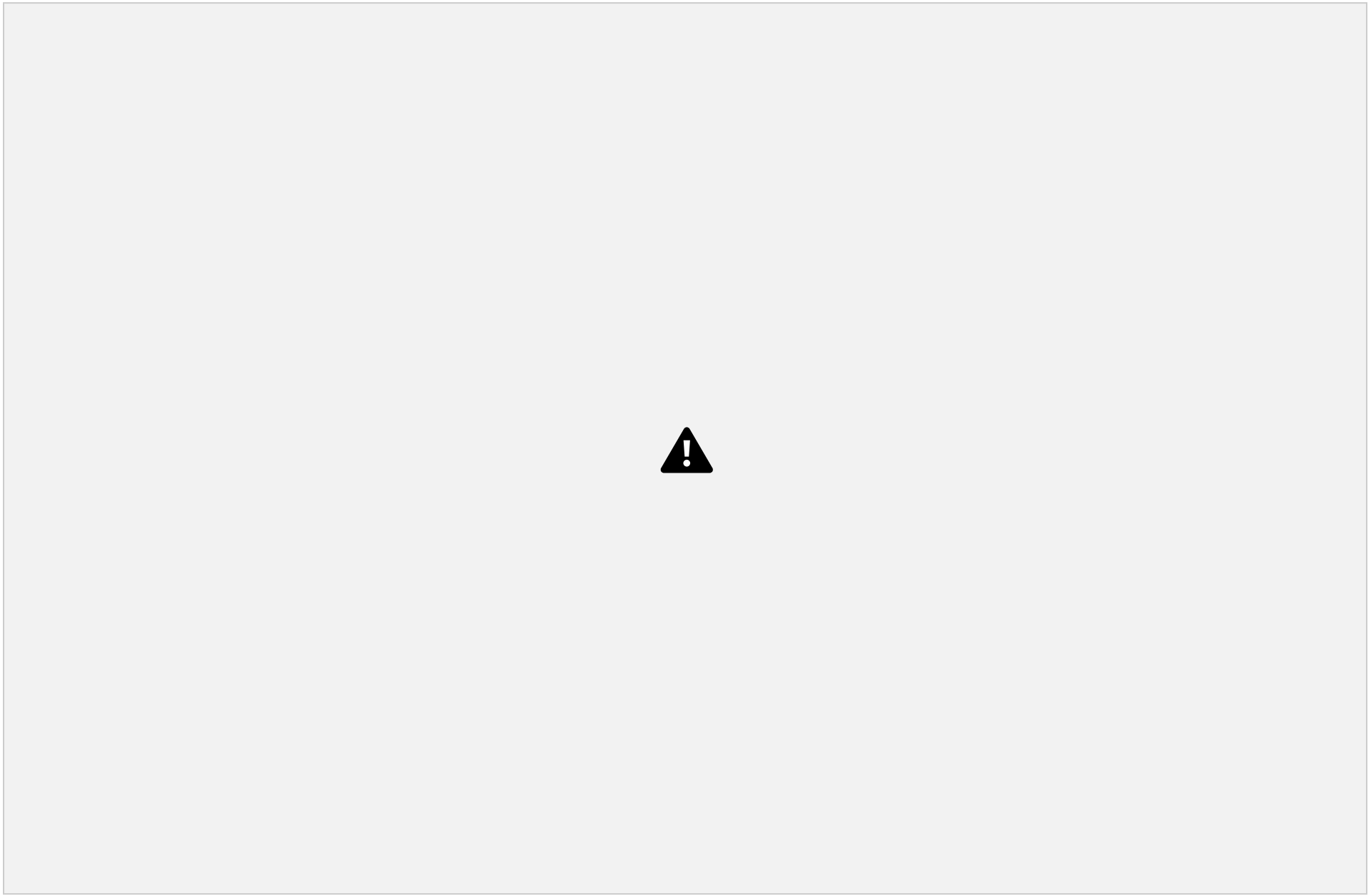
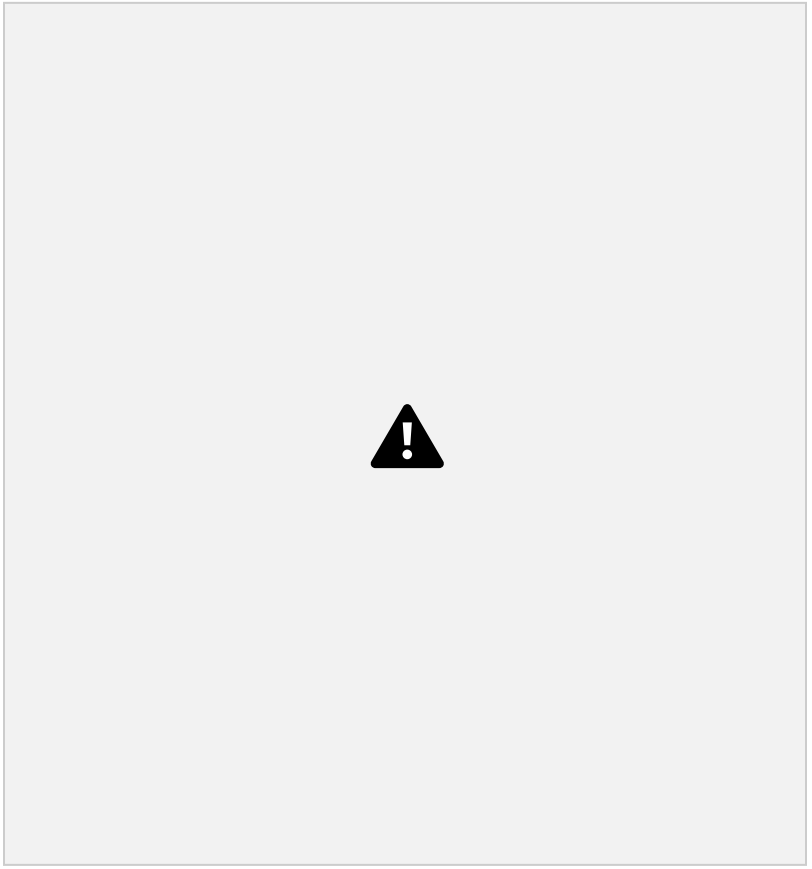
Adder - CSA



Adder - CSK

- A Carry skip adder/ Carry bypass adder improves the delay of a ripple carry adder (RCA)
- It is a RCA which is partitioned into several full adder blocks and a skip circuit is attached with each block
- A skip circuit detects the propagation condition of the block • Carry bypass the block where the carry propagation condition holds
  - Carry ripples through the full adders where the carry propagation condition does not hold

Adder - CSK



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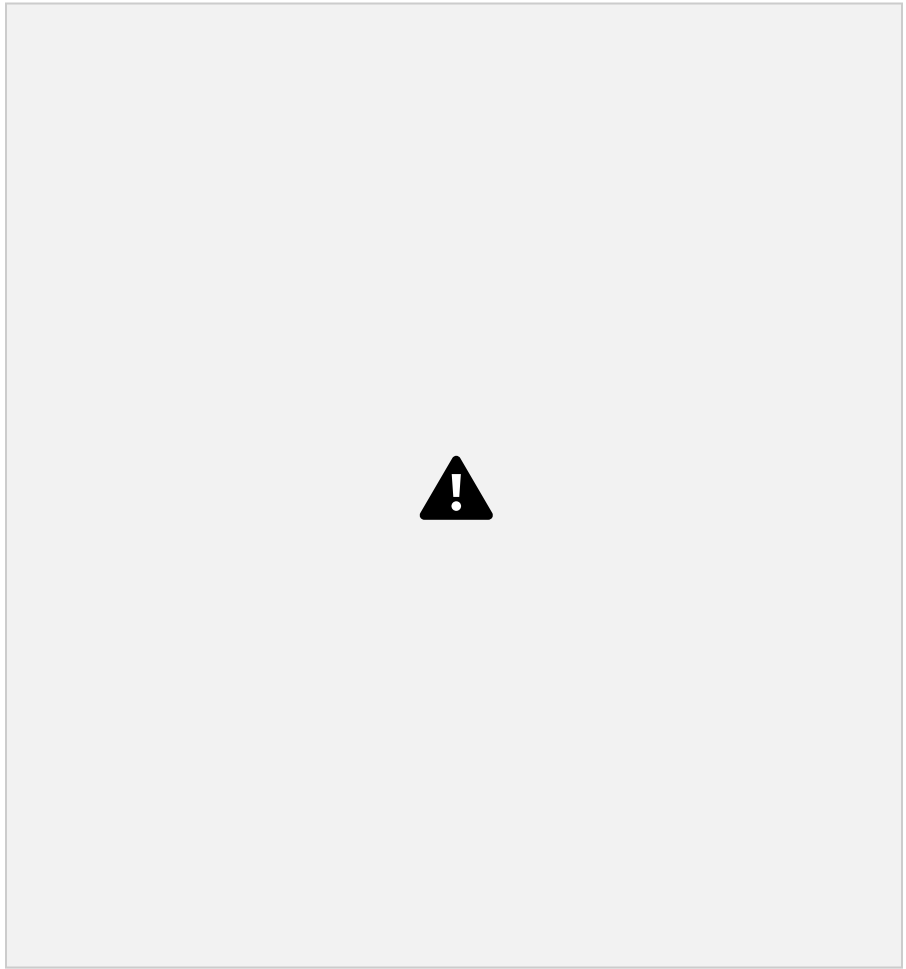
Adder - CSK



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Adder - CSK