Lecture 33 Multistage Amplifiers (Cont.)

DC Coupling: General Trends

* **Goal**: want both input and output to be "centered" at halfway between the positive and negative supplies (or ground, for a single supply) -- in order to have maximum possible swing at the input and at the output.

  Summary of DC shifts through the single stages:

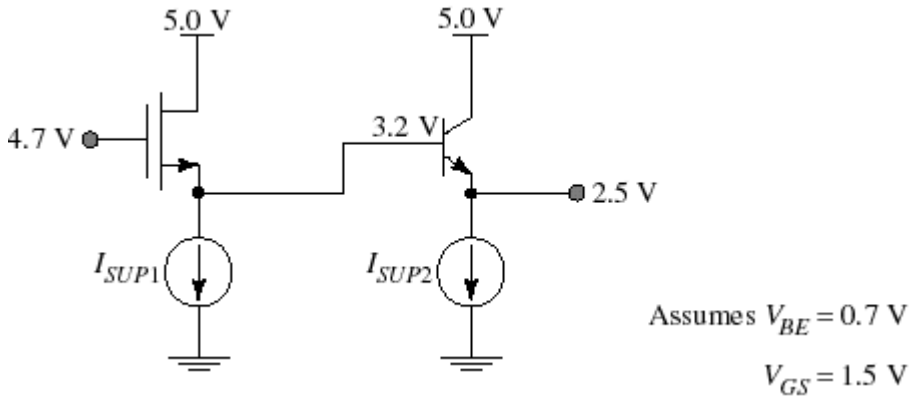
BJT Amp. Type	npn version
CE	positive
CB	positive
CC	negative*

MOS Amp. Type	n-channel version	p-channel version
CS	positive	negative
CG	positive	negative
CD	negative*	positive*

The DC voltage shifts for CC/CD stages are set by the V_{BE} = 0.7 V drop or by the V_{GS} of the transistor and can be specified by the designer.

DC Coupling Example

* Common drain - common collector cascade (infinite input resistance, fairly low output resistance, unity voltage gain ... reasonable voltage buffer)



For CC stage, the optimum output voltage of 2.5 V
(centered between + 5 V and ground for maximum swing) -->

$$V_{IN2} = \text{DC input of CC amp} = 2.5 + 0.7 \text{ V} = 3.2 \text{ V}$$

The DC of the n-channel CD amplifier is then:

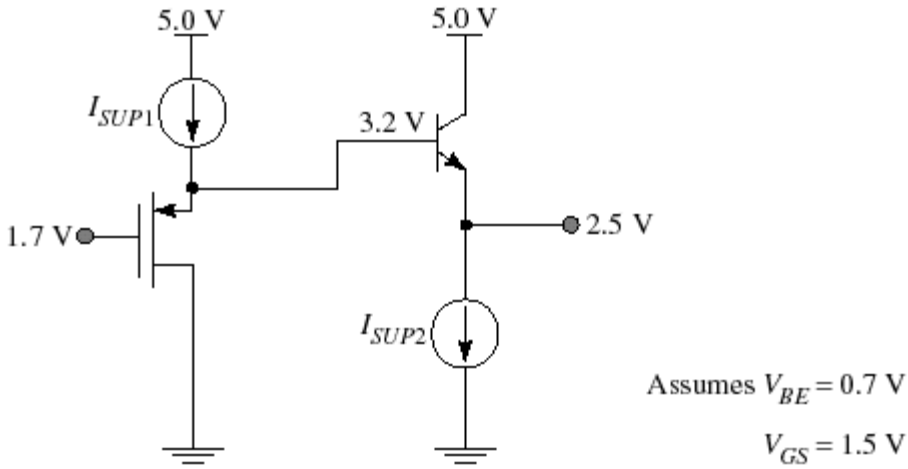
$V_{IN} = \text{DC input of CD amp} = V_{IN2} + V_{GS1} = 3.2 \text{ V} + 1.5 \text{ V} = 4.7 \text{ V}$

where we have assumed that $V_{GS1} = 1.5$ V as a typical gate-source voltage (actual number comes from $I_{SUP1}$and (W/L)).

* too close to the supply voltage -- input DC level should be centered at or near 2.5 V.

DC Biasing Example (Cont.)

* Solution: use p-channel CD amplifier since it shifts the DC level in the **positive** direction from input to output



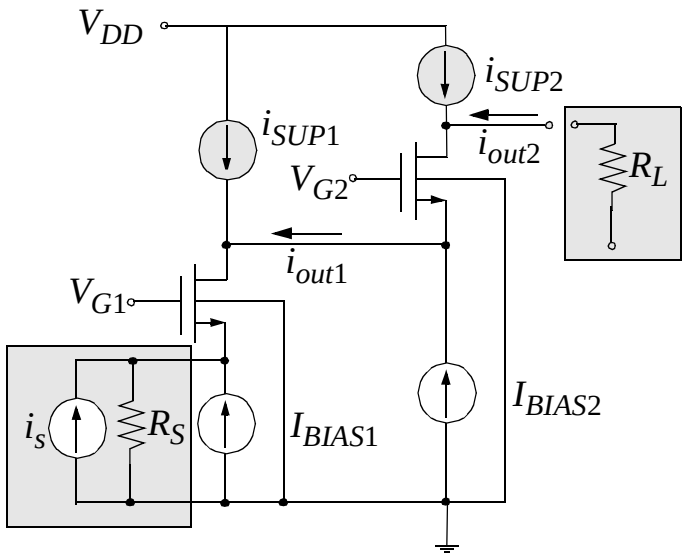
Selection of large (*W/L*) for the p-channel --> input DC level can be adjusted closer to 2.5 V.

General principal:

mix PMOS/NMOS versions of amplifier stages to cancel out large shifts in the DC level of the signal

DC Biasing of Current Buffer Stages

* Example: CG/CG cascade that have separate supply and bias sources

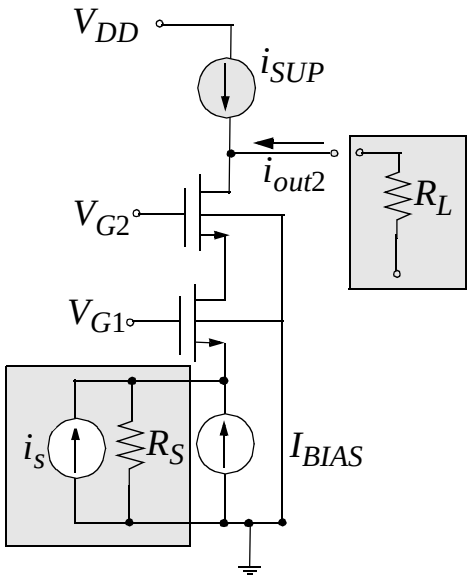


Why not use the DC current from the CG1 to bias CG2, in order to simplify the circuit?

(In some cases, the ability to set the current levels separately may make it worthwhile to *not* "stack" them up ...)

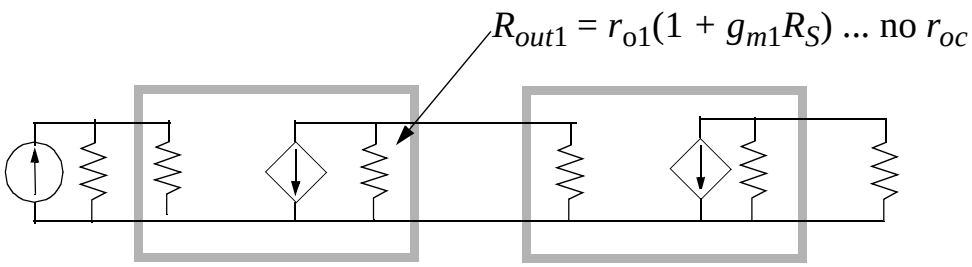
DC Biasing of Current Buffer Stages

* Example: CG/CG cascade that share a supply and a bias source



Two-port model for the first stage (M_1) is modified from the standard form:

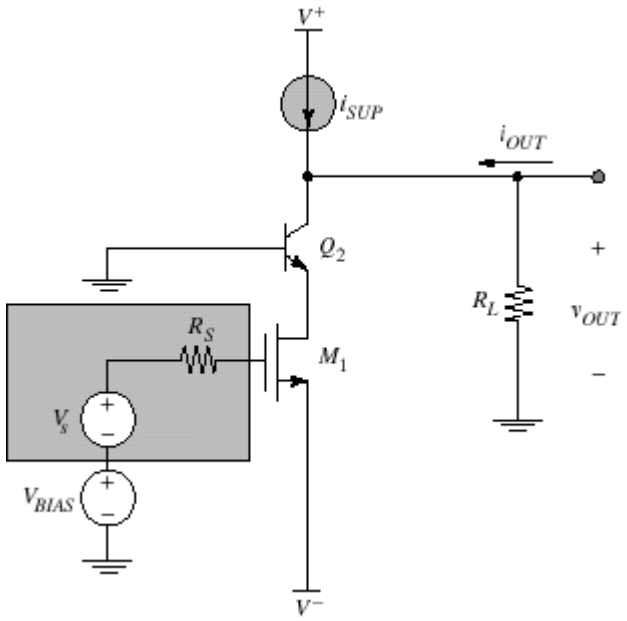
Why? There's no supply current source attached directly to M_1



Sharing a Current Supply: the "Cascode"

* Common-source/common-base two-stage transconductance (or voltage) amplifier can also make use of a shared current supply

  common-source transistor is used to provide bias current to the common-base transistor

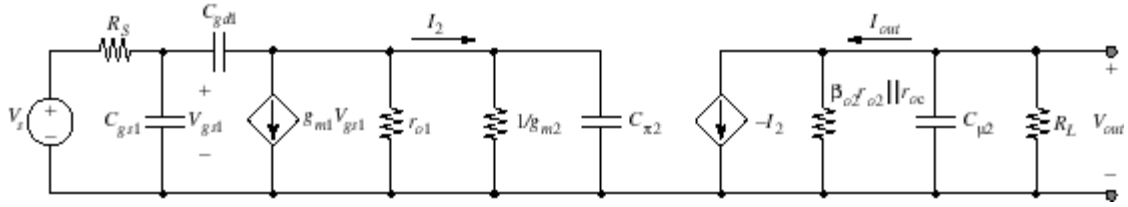


* Similar configurations are also referred to as a "cascode topology:

  CE/CB, CE/CG, CS/CB, and CS/CG are also cascodes

Two-Port Model for a Cascode

The common-source first stage is modified ... no supply resistance appears in its output resistance



Voltage gain of first stage:

Miller capacitor at input ... MUCH reduced

Voltage gain ... similar to CS alone ... but needs another stage to reduce its very high output resistance

Cascodes are standard building blocks for analog IC design