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B.Tech DEGREE EXAMINATION, NOVEMBER 2023

Third Semester

18ECC103J - DIGITAL ELECTRONIC PRINCIPLES

(For the candidates admitted during the academic year 2020 - 2021 & 2021 - 2022)

Note:

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

ii. **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours **Max. Marks: 100**

PART - A (20 × 1 = 20 Marks)
Answer **all** Questions

		Marks	BL	CO
1.	BCD equivalent of $(57)_{10}$ is (A) 1010 1111 (B) 1110 0101 (C) 0101 0111 (D) 0110 0101	1	1	1
2.	Find the 2's Complement of 1011011 (A) 0100101 (B) 0100100 (C) 0100111 (D) 1011000	1	1	1
3.	Convert Binary $(1011)_2$ to Gray (A) 1111 (B) 1110 (C) 0001 (D) 1010	1	1	1
4.	Expansion of ASCII (A) American Standard code for Information Interchange (B) American Standard code for Interchange Information (C) American Standard code for Identity Information (D) American Standard code for Identity Interchange	1	1	1
5.	The main disadvantage of TTL, with Totem pole output is (A) High power dissipation (B) Wire ANDing operation is not allowed (C) Low fan out (D) Low noise Margin	1	1	2
6.	A Logic signal experiences a delay in going through a circuit the two propagation delay times are defined as (A) t_{PLH} & t_{PHL} (B) t_{DLH} & t_{DHL} (C) t_{HPL} & t_{HPL} (D) t_{LDH}& t_{HDL}	1	1	2
7.	Which logic family provides minimum power dissipation? (A) TTL (B) CMOS (C) ECL (D) JFET	1	1	2
8.	If a logic circuit has a fan-out of 8 then the circuit (A) Has 8 inputs (B) Has 8 outputs (C) Can drive maximum of 8 inputs (D) Gives output 8 times the input	1	1	2
9.	The device which changes from serial data to parallel data is (A) Counter (B) Multiplexer (C) Demultiplexer (D) Flip flop	1	1	3
10.	To secure a higher speed of addition, which of the following is the preferred solution? (A) serial adder (B) parallel adder (C) adder with a look-ahead carry (D) full adder	1	1	3

11.	Which one of the following set of gates is best suited for parity checking and parity generation? (A) AND , OR , NOT gates (B) Ex-NOR , Ex-OR gates (C) NAND gate (D) AND gate	1	1	3
12.	A combinational circuit with n inputs and maximum of 2^n outputs is (A) Encoder (B) Decoder (C) Multiplexer (D) Demultiplexer	1	1	3
13.	How many Flip-Flops are required for mod–16 counter? (A) 5 (B) 6 (C) 3 (D) 4	1	1	4
14.	Data can be changed from special code to temporal code by using (A) Shift registers (B) Counters (C) Combinational circuits (D) A/D converters	1	1	4
15.	A ring counter consisting of five Flip-Flops will have (A) 5 states (B) 10 states (C) 32 states (D) Infinite states	1	1	4
16.	In a JK Flip-Flop, toggle means (A) Set Q = 1 and Q = 0 (B) Set Q = 0 and Q = 1 (C) Change the output to the opposite state (D) No change in output	1	1	4
17.	EPROM contents can be erased by exposing it to (A) Ultraviolet rays (B) Intense heat radiations (C) Burst of microwaves (D) Infrared rays	1	1	5
18.	_____ memory is a volatile memory. (A) ROM (B) RAM (C) PROM (D) EEPROM	1	1	5
19.	The difference between a PLA and a PAL is (A) the PLA has a programmable OR plane and a Programmable AND plane, while PAL only has a programmable AND plane (B) the PAL has a programmable OR plane and a programmable AND plane , while the PLA only has a programmable AND plane (C) the PAL has more possible product terms than the PLA (D) PAL and PLA are the same thing	1	1	5
20.	What is the storage element for a static RAM? (A) Diode (B) Resistor (C) Capacitor (D) Flip flop	1	1	5

PART - B (5 × 4 = 20 Marks)

Answer **any 5** Questions

		Marks	BL	CO
21.	Simplify A + AB + ABC + ABCD + ABCDE using Boolean laws.	4	3	1
22.	Perform the BCD addition of $[917]_{BCD} + [215]_{BCD}$.	4	2	1
23.	Explain the DTL circuit.	4	4	2
24.	Design a half subtractor circuit.	4	1	2
25.	Explain 2-bit synchronous up counter using D Flipflop with timing diagram.	4	4	3
26.	Obtain the characteristic table and excitation table for SR flip flop.	4	3	3

27.	Implement the following Boolean functions using PROM. $A(X,Y,Z)=\sum m(5,6,7)$ $B(X,Y,Z)=\sum m(3,5,6,7)$	4	3	4

PART - C (5 × 12 = 60 Marks)

Answer **all** Questions

		Marks	BL	CO
28.	(a) Simplify the Boolean function $Y(A, B, C, D) = \Sigma\, m(0,1,3,5,9,12)+\Sigma\, d(2,4,6,7,11)$	12	3	1
	(OR)			
	(b) Apply De Morgan's theorem to simplify (A+BC')'.			
29.	(a) Explain the operation of Multi emitter TTL NAND gate .	12	1	2
	(OR)			
	(b) Explain the circuit of PMOS NAND gate and PMOS NOR gate.			
30.	(a) Design a 3:8 decoder.	12	4	3
	(OR)			
	(b) Design and implement the logic function $F(A,B,C,D)=\sum m(0,1,3,4,8,9,15)$ using 8:1 multiplexer.			
31.	(a) Design a universal Shift register.	12	4	4
	(OR)			
	(b) Design MOD-8 counter using D-Flip flop.			
32.	(a) Implement the following Boolean functions using a 3 × 4 × 2 PLA. $F_1(A, B, C) = (3, 5, 6, 7)$ and $F_2(A, B, C) = (0, 2, 4, 7)$	12	4	5
	(OR)			
	(b) Implement the following Boolean function using PAL $w(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13)$ $x(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13,14)$ $y(A, B, C, D) = \sum m(2, 3, 8, 9, 10, 12, 13)$ $z(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 12, 14)$			

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