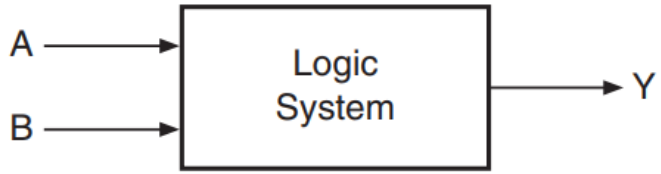
UNIT-I

DIGITAL LOGIC FAMILIES

Digital Logic

Logic: High ‘H’ is set to be binary 1 (+Vcc)

Low ‘L’ is set to be binary 0 (gnd)



(a)

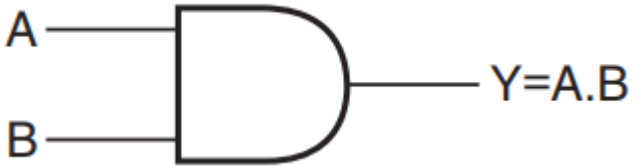
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(b)

Figure 4.1 Two-input logic system.

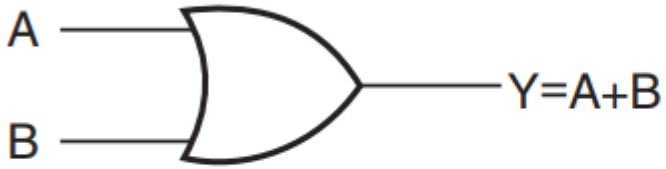
Basic Logic gates

- **Logic gates**
  - Basic building block of any digital system
  - Implemented with electronic circuits
  - Three basic logic gates (**AND, OR** and **NOT**)
  - Used to construct any logic circuit for given logic expression



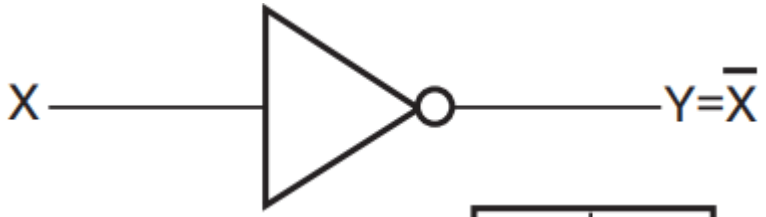
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Figure 4.7 Two-input AND gate.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Figure 4.3 Two-input OR gate.



X	Y
0	1
1	0

Figure 4.10 (a) Circuit symbol of a NOT circuit and (b) the truth table of a NOT circuit.

EXCLUSIVE-OR (EX-OR) and EXCLUSIVE-NOR (EX-NOR) Logic gates

- **EX-OR**
  - Output is 1 when the inputs are unlike
  - Output is 0 when the inputs are like

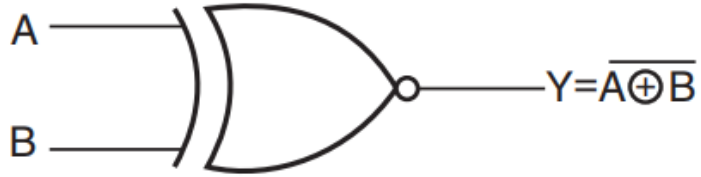
(a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(b)

$$Y = (A \oplus B) = \overline{A}B + A\overline{B}$$

- **EX-NOR**
  - Output is 0 when the inputs are unlike
  - Output is 1 when the inputs are like



(a)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

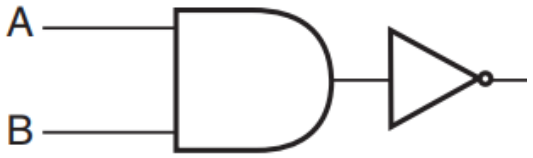
(b)

$$Y = (\overline{A \oplus B}) = (A.B + \overline{A}.\overline{B})$$

Universal Gates (NAND and NOR)

NAND (AND NOT Gate)

$$Y = \overline{A.B}$$



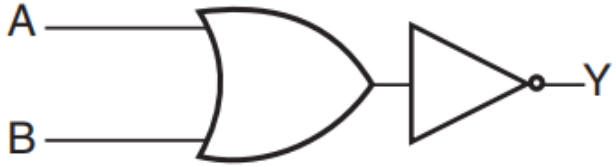
(a)

(b)

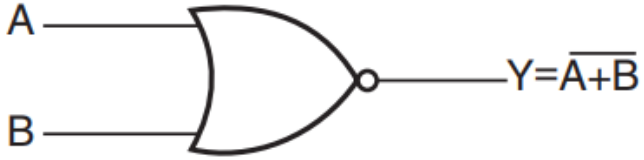
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR (OR NOT Gate)

$$Y = \overline{(A + B)}$$



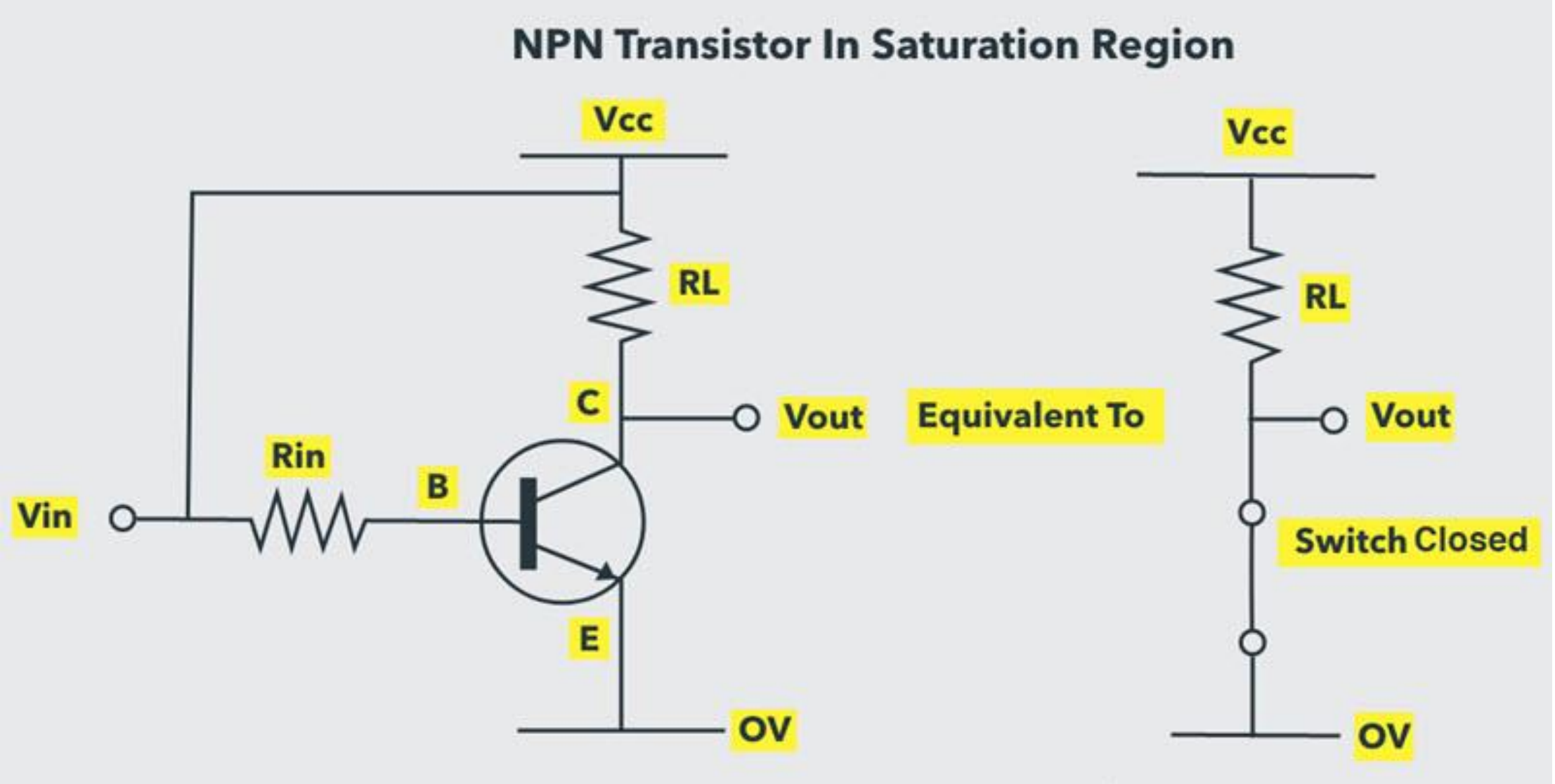
(a)



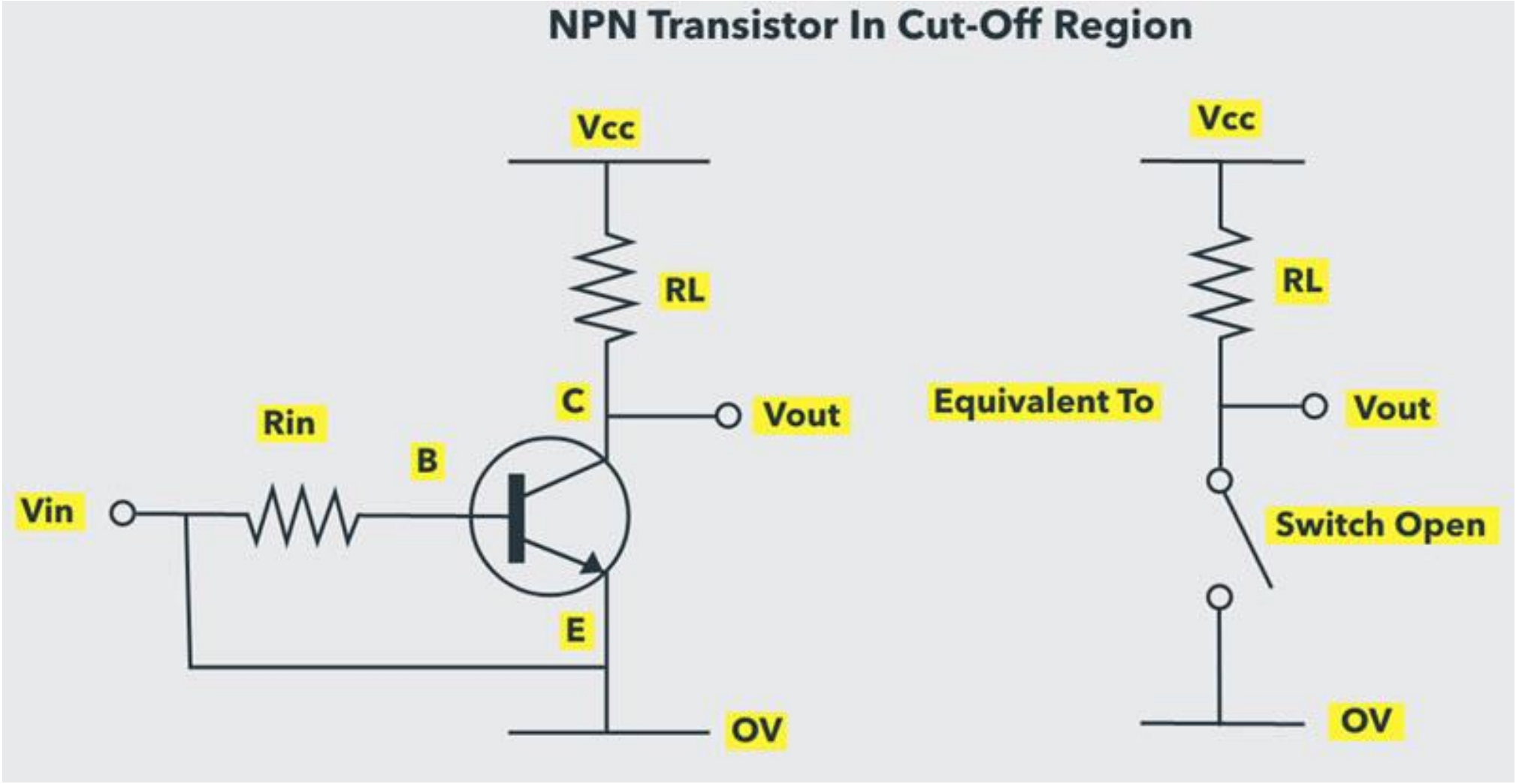
(b)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Transistor as an electronic switch



Transistor as an electronic switch



Digital Logic Families

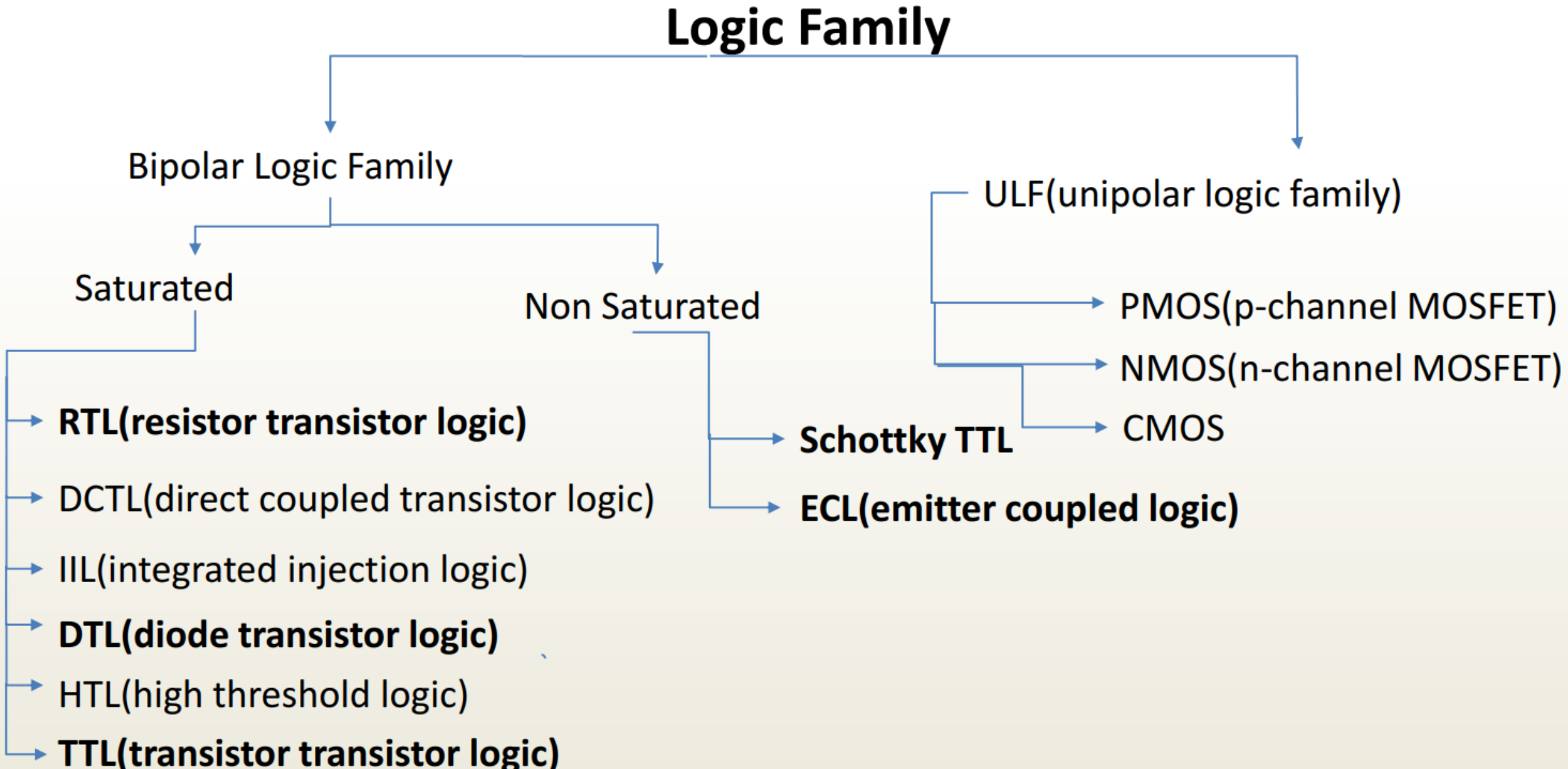
Introduction

Logic families represent kind of digital circuit/methodologies for logic expression.

Integration levels :

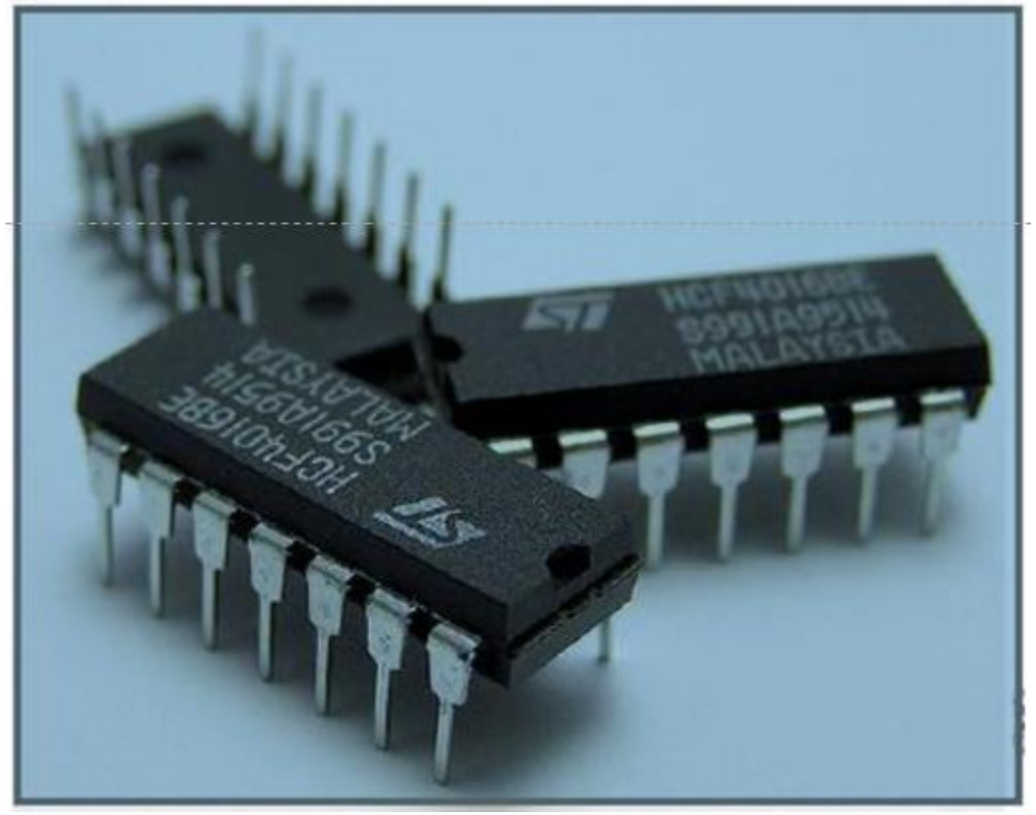
SSI:	Small scale integration	12 gates/chip
MSI:	Medium scale integration	100 gates/chip
LSI:	Large scale integration	1K gates/chip
VLSI:	Very large scale integration	10K gates/chip
ULSI:	Ultra large scale integration	100K gates/chip

Digital Logic Families
Classification

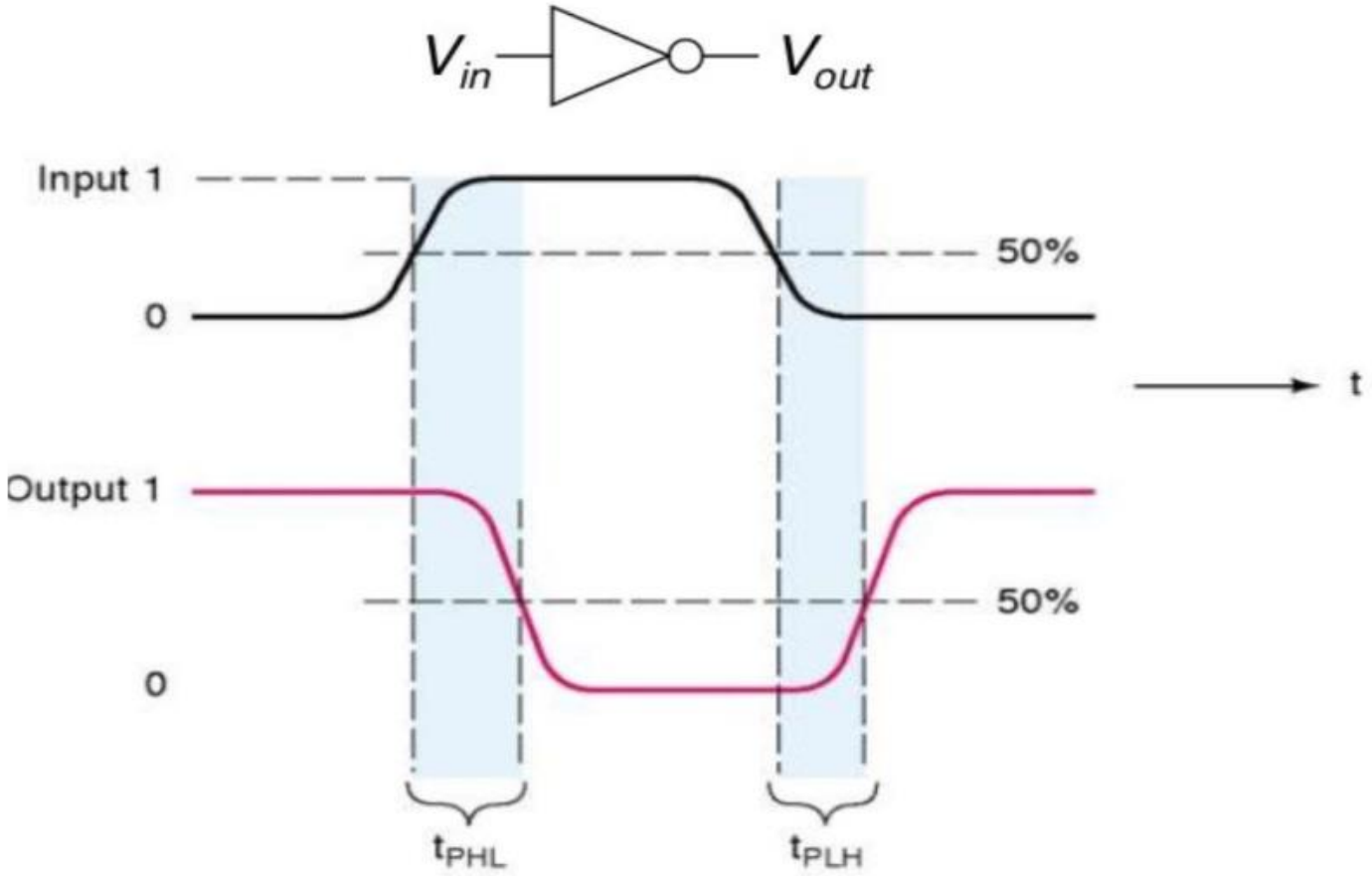


Characteristics of Logic Families

- Speed
- Propagation Delay
- Fan-in
- Fan-out
- Noise margin
- Power Dissipation



Propagation Delay



A measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

t_{PHL} - the time it takes the output to go from a high to a low

t_{PLH} - the time it takes the output to go from a low to a high

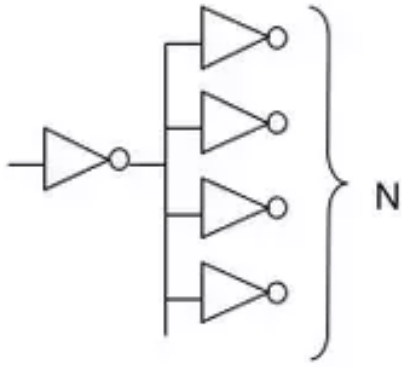
Average Propagation Delay Time $t_p = \frac{t_{pHL} + t_{pLH}}{2}$

Speed and Power dissipation

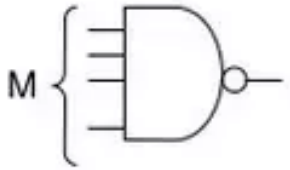
- Speed: Speed of a logic circuit is determined by the time between the application of input and change in the output of the circuit.
- Power Dissipation (P_D): Circuit dissipates power when it switches from one state to the other state (Dynamic) and when it is stable in either of the state (ON or OFF)(Static).
- Speed power product: A useful figure-of-merit used to evaluate different logic families is the speed–power product, expressed in picojoules, which is the product of the propagation delay (measured in nanoseconds) and the power dissipation per gate (measured in milliwatts).

$$F = PD * t_{PD}$$

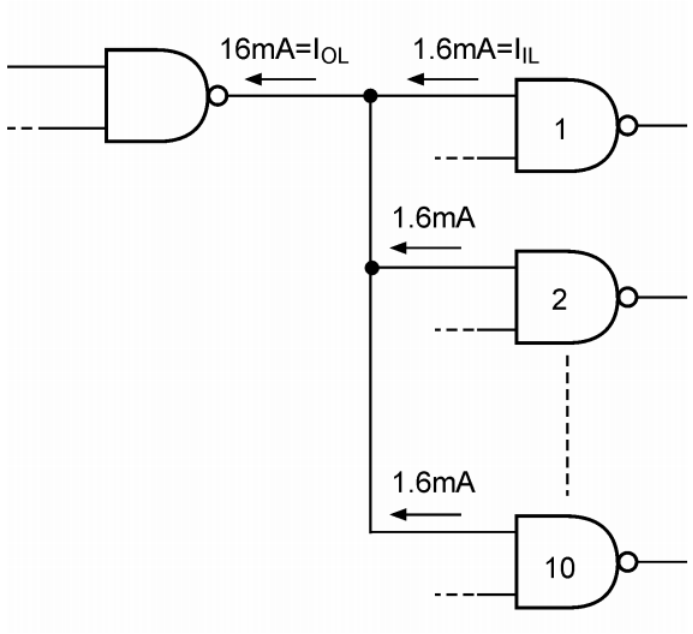
Fan-out and Fan-in



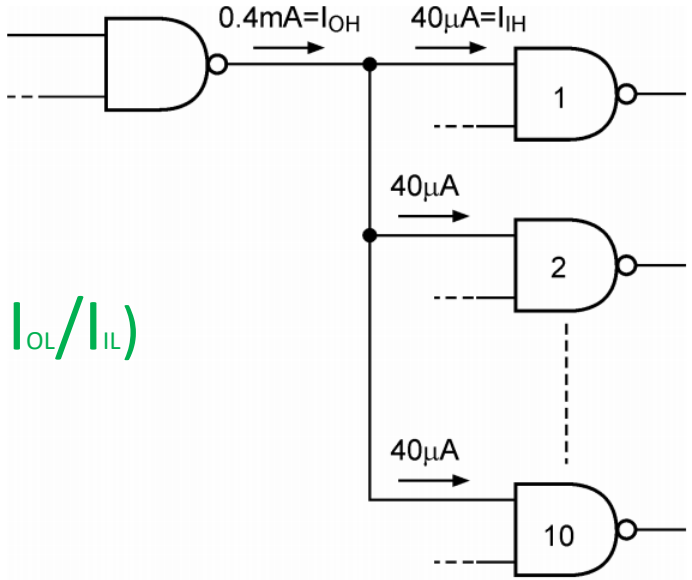
Fan-out: It determines the **number of outputs** logic gates can drive without causing any false output.



Fan-in: It determines the **number of inputs** the logic gate can handle.



fan-out = smallest(I_{OH}/I_{IH} , I_{OL}/I_{IL})



Noise Margin

- Noise is present in all real systems. This adds random fluctuations to voltages representing logic levels
- Hence, the voltage ranges defining the logic levels are more tightly constrained at the output of a gate than at the input.
- Small amounts of noise will not affect the circuit. The maximum noise voltage that can be tolerated by a circuit is termed its noise immunity (Noise Margin)

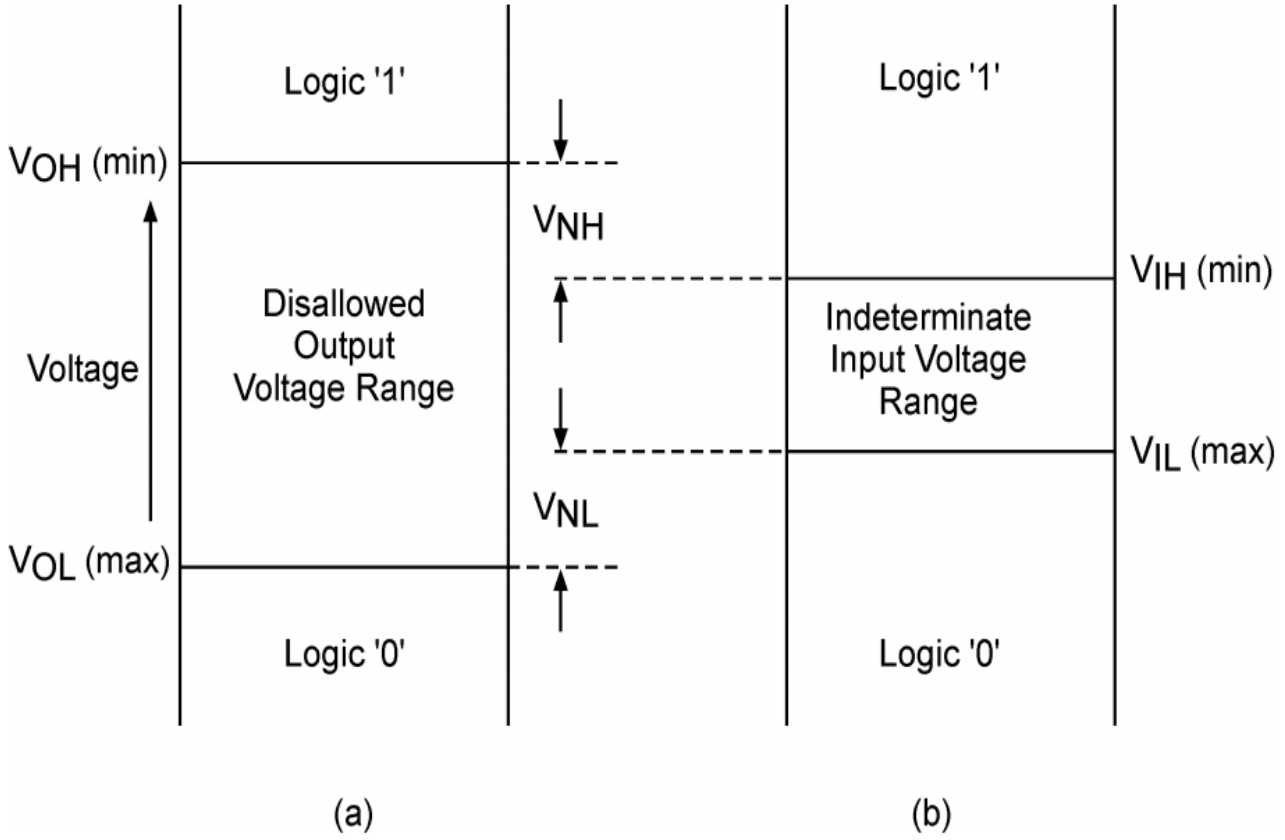
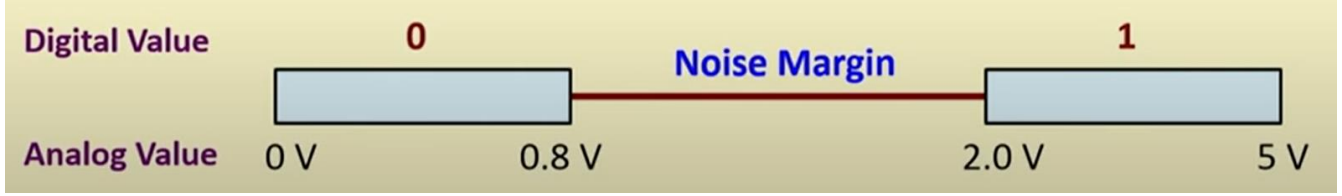


Figure 5.5 Noise margin.



Transistor Transistor Logic family

- Totem pole TTL
- Open-collector and tristate TTL
- Schottky and standard TTL characteristics

Multiple Emitter Transistor

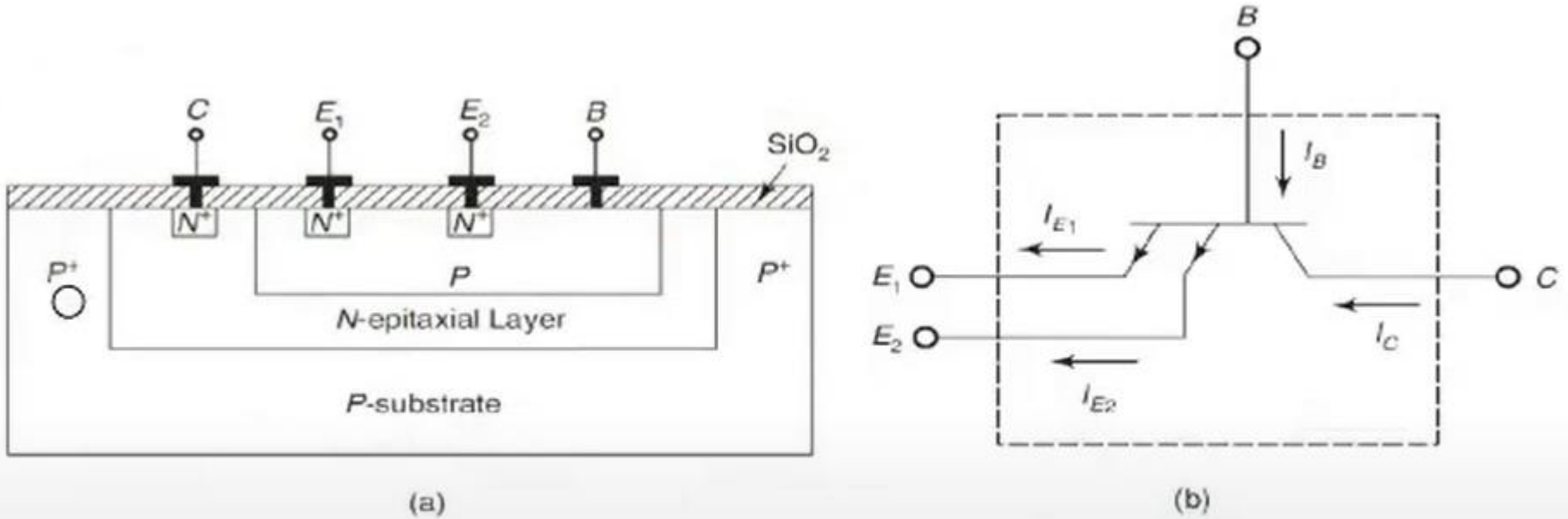


Fig. 2.35 *Multi-emitter transistor: (a) Cross-sectional view, (b) Symbol*

Standard TTL gate with Totem pole output

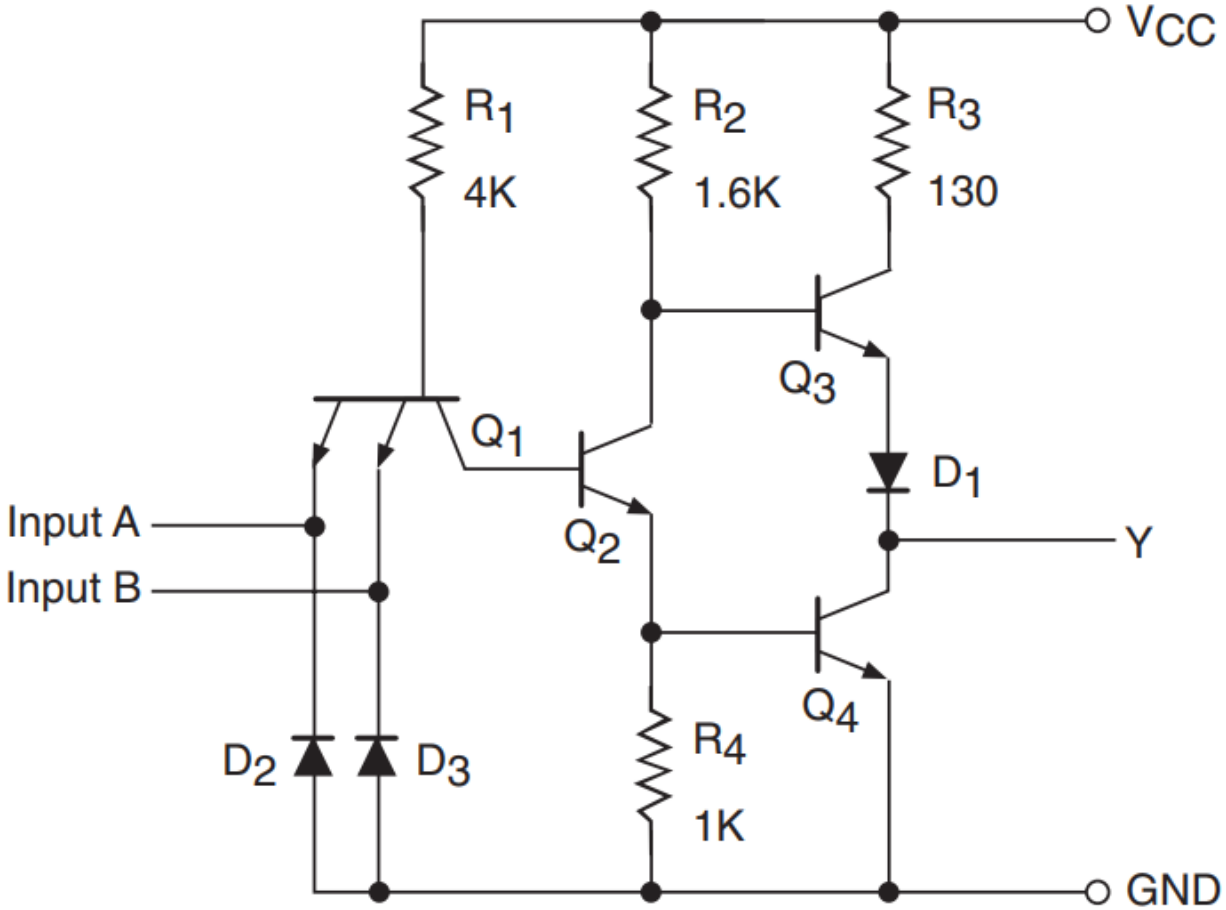


Figure 5.6 Standard TTL NAND gate.

- Three stages:
  1. Multi emitter input stage
  2. Phase splitter
  3. Totem-pole output stage
- The active pull-up circuit at the output gives a reduced propagation delay than a passive resistor pull-up circuit
- However, not suitable for implementing common bus system i.e., the outputs cannot be tied together to form a wired-logic

Propagation delay of a transistor:

- storage time constant (saturation)
- RC time constant

TTL with open collector

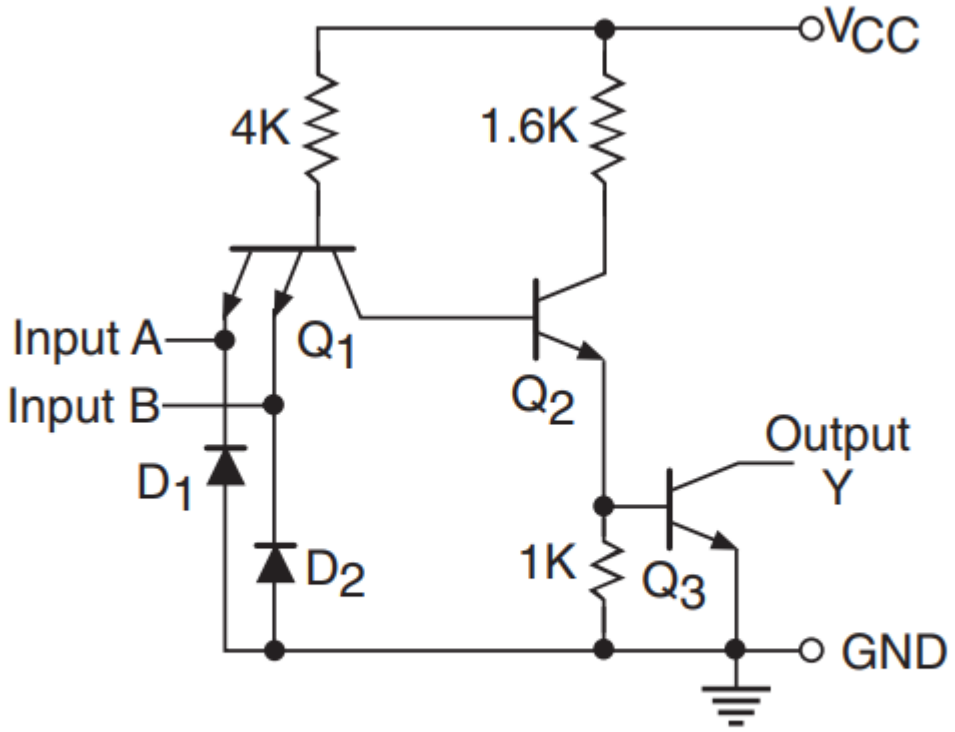


Figure 5.14 NAND gate with an open collector output.

- Three stages:
  1. Multi emitter input stage
  2. Phase splitter
  3. open collector output stage
- A resistor connected to Vcc must be inserted externally to the IC package for the output to be pulled high

Applications:

- Driving a lamp or relay
- performing wired logic
- constructing a common bus system

Schottky TTL

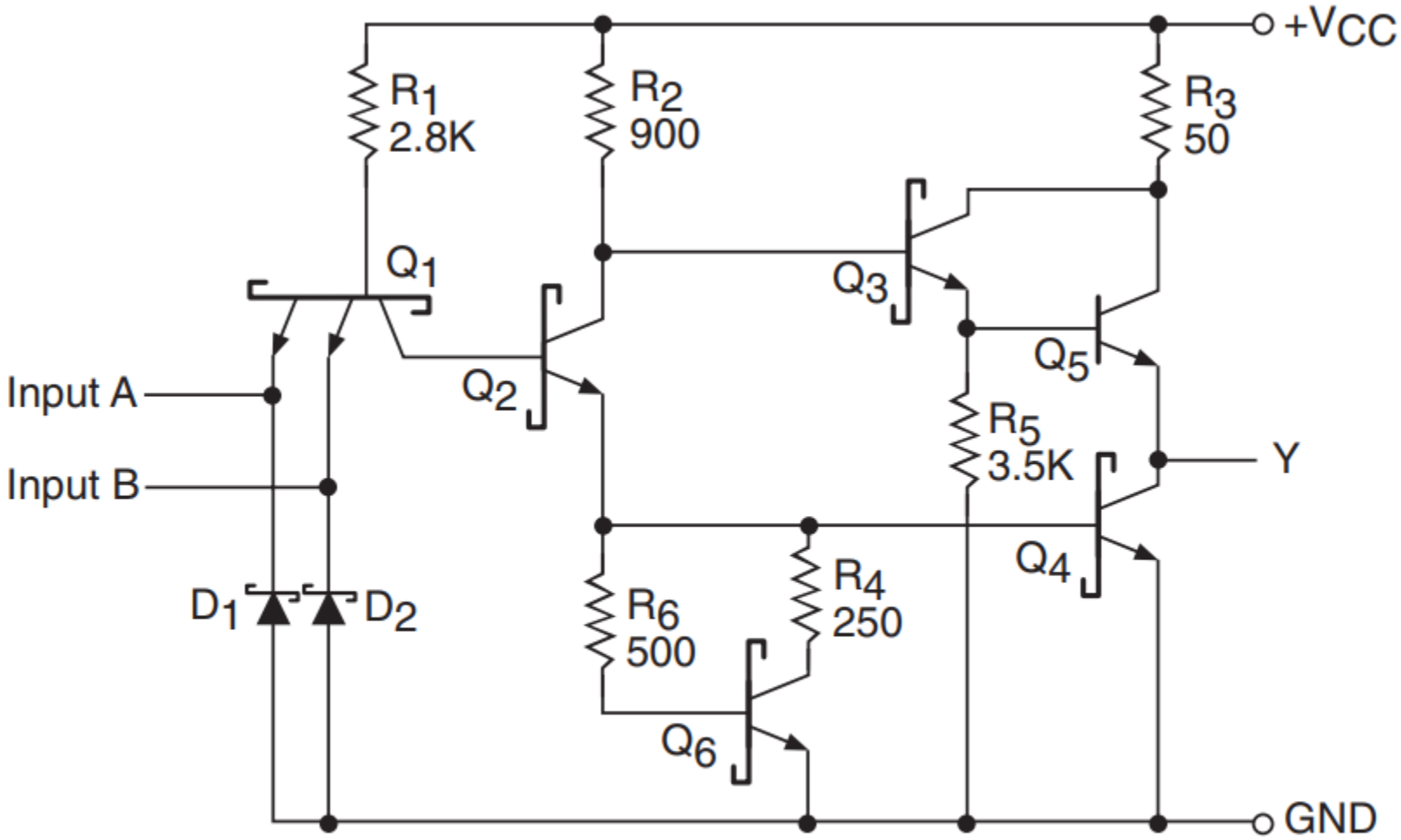
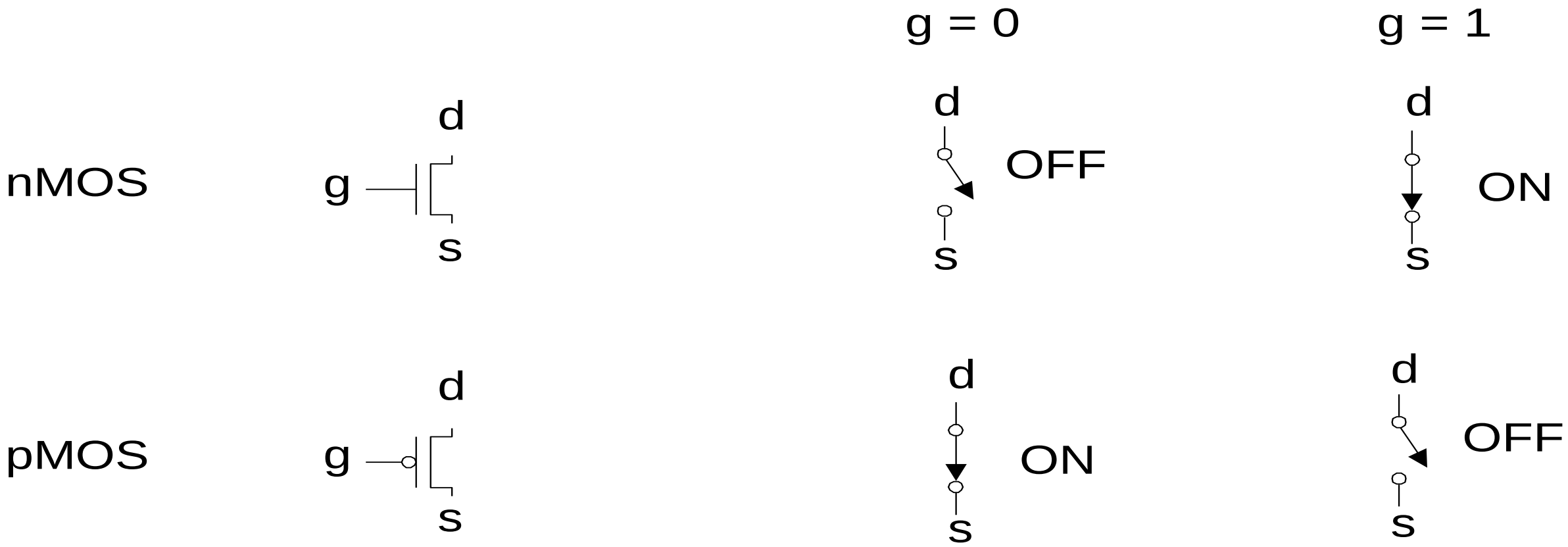


Figure 5.19 NAND gate in the Schottky TTL.

Switch models of MOSFETs

Vi (Vgs)	Logic Level	nMOS	pMOS
Vdd	1	ON	OFF
Vss(GND)	0	OFF	ON



MOSFET - Uses

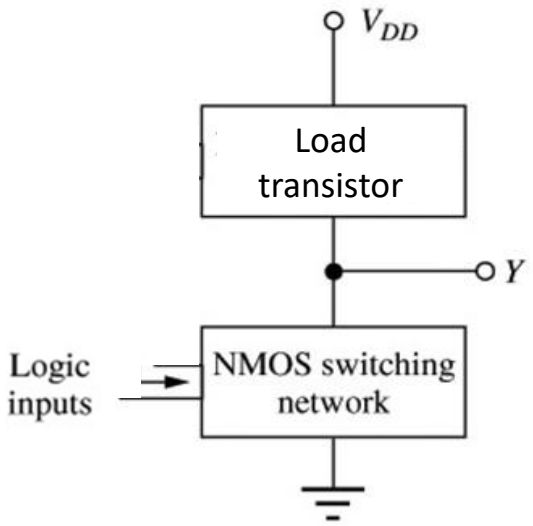
- Most important device in digital design
- Very good as a switch
- Relatively few parasitics
- Rather low power consumption
- High integration density
- Simple manufacturing
- Economical for large complex circuits

Power Supply Voltage

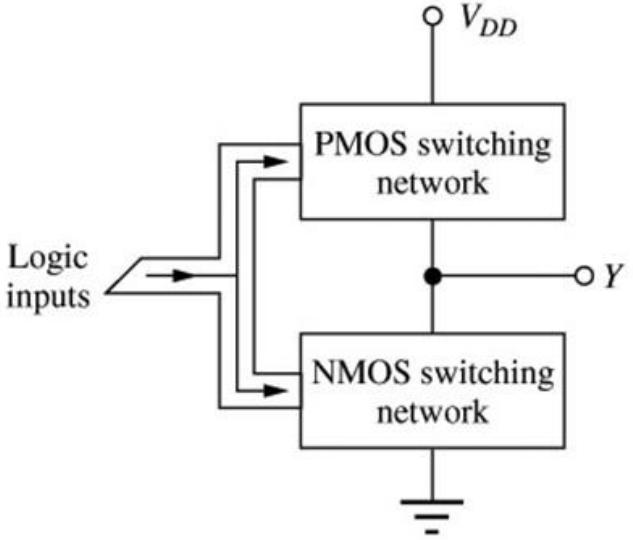
- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

CMOS Logic Design

- The design of logic gates for CMOS inverter is different from the similar logic design for NMOS inverters that we considered earlier.
- For NMOS gates, the logic involved only the switching transistor.
- For CMOS, both transistors are involved, since the input affects both in symmetrical way.
- Thus, for each logic input variable in CMOS gate there is *one transistor in NMOS* network and *one transistor in PMOS* network.



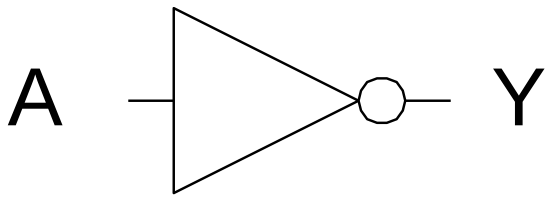
NMOS logic gate structure

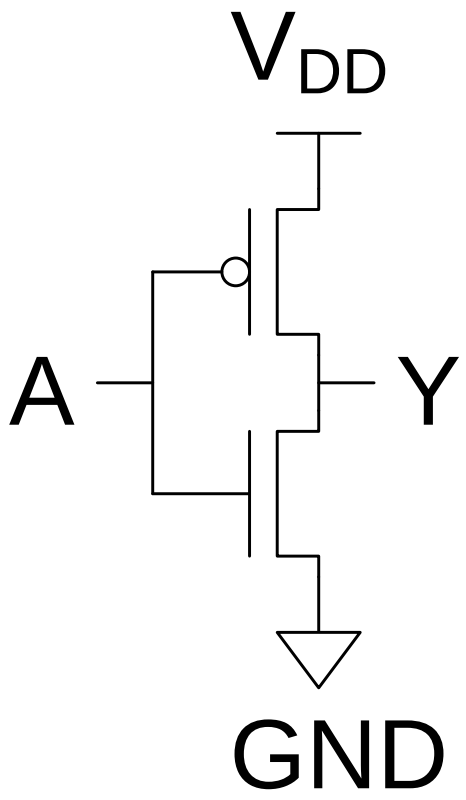


CMOS logic gate structure

CMOS Inverter

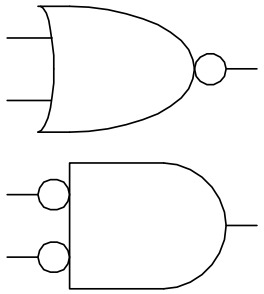
A	Y
0	1
1	0

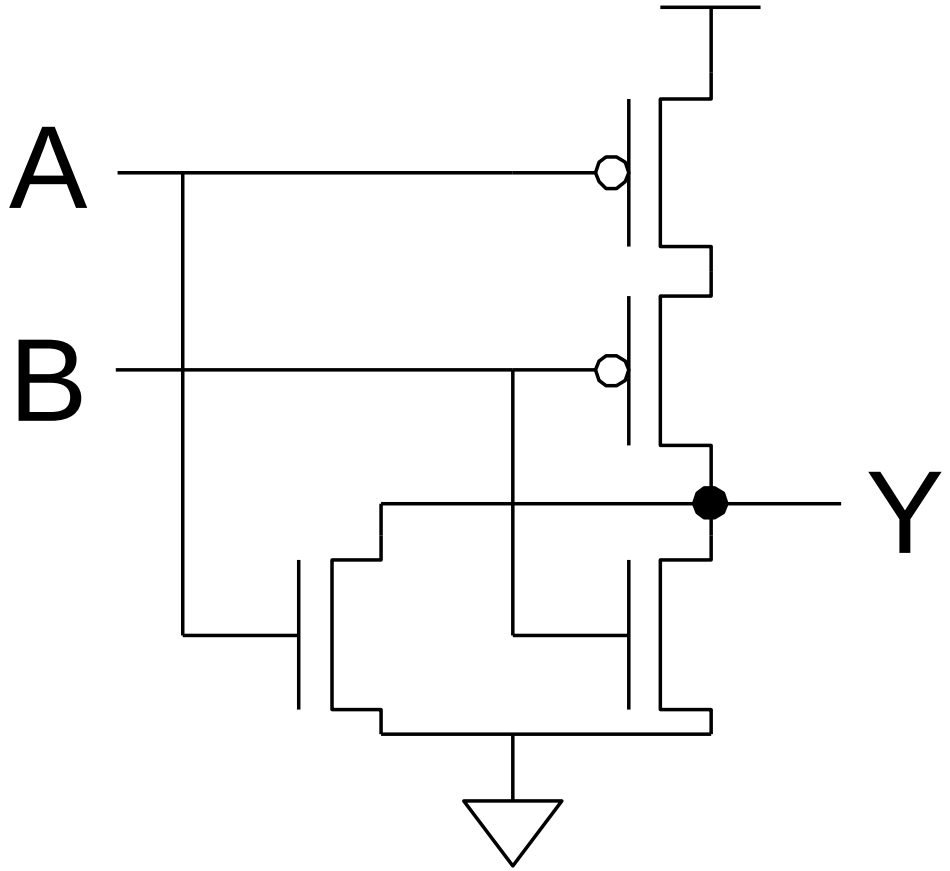




CMOS NOR Gate

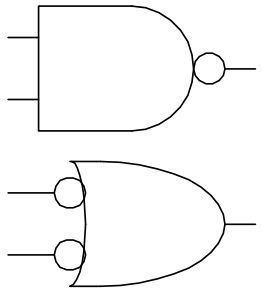
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

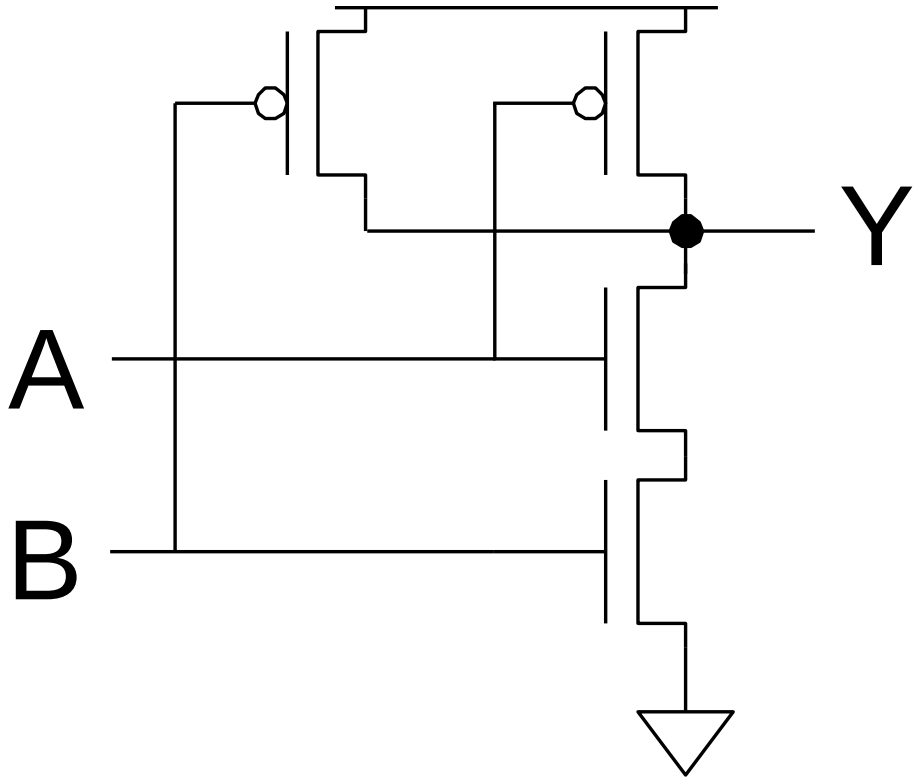




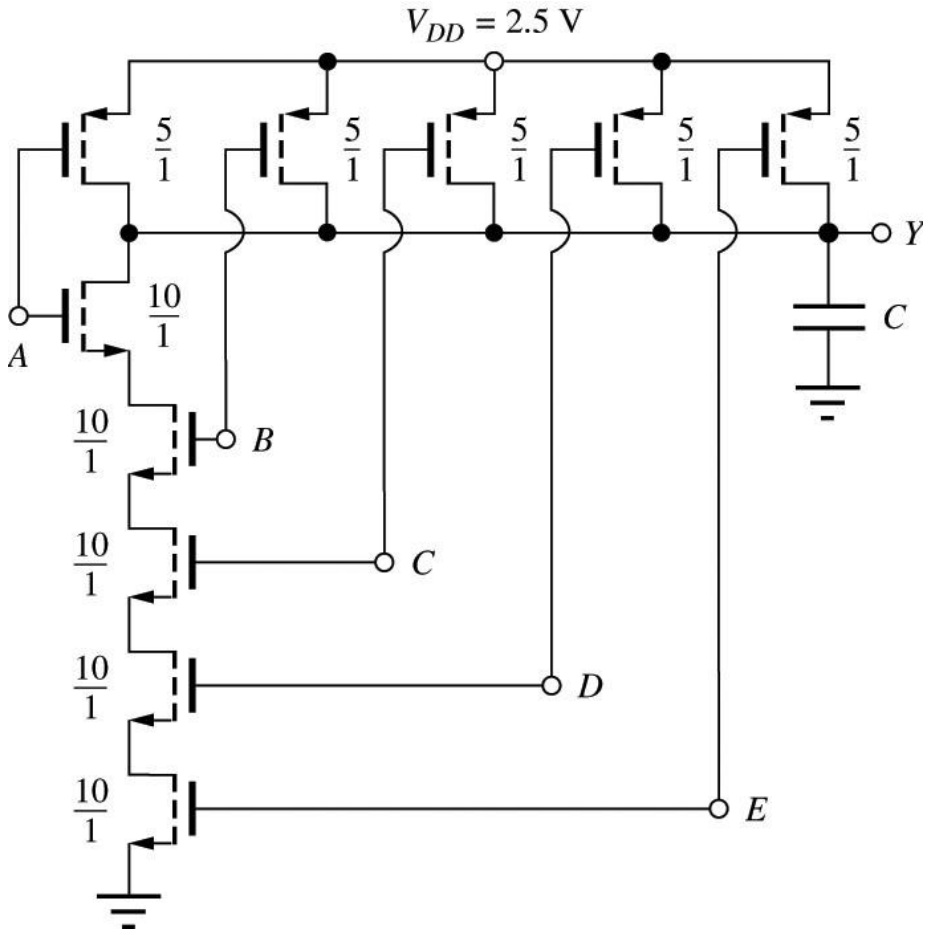
CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0





Multi-Input CMOS NAND Gates



CMOS vs TTL

	CMOS	TTL
Cost	More expensive than TTL but are less costly at a system level. Also, they are smaller.	Less expensive but not as economical as CMOS.
Propagation Delays	Between 20 and 50 nS,	Around 10 nS.
Rise and Fall Times	Longer rise and fall times, resulting in simpler, less costly digital signals.	Shorter rise and fall times.
Voltage Levels	Part of being more energy efficient includes having low voltage levels, usually between 0 to 1/3 VDD at a low level and 2/3VDD to VDD at high levels.	TTL chips have a high operating voltage level, typically ranging from 4.75 V to 5.25 V.
Current Draw	CMOS chips require less current, which limits power consumption. Therefore, they make it easier to design circuits with better power management.	Like voltage, TTL chips require more current.

CMOS vs TTL

Electromagnetic Disruptions	CMOS chip components are more sensitive to electromagnetic disruptions.	TTL logic components are less susceptible to electromagnetic disruptions.
Standard Load Connections (Fan-out)	The number of loads connectable to the gate output under normal operation is 50.	The number here is significantly lower. Only 10.
Standard Input Connections (Fan-in)	The number of connectable inputs to the gate is only 10.	TTL has the upper hand because the number is slightly higher (12 - 14).
Noise Immunity	Better noise immunity.	Not as immune as CMOS chips to noise.
Basic Logic Gates	Feature NAND and NOR gates to carry out logic functions.	It contains only NAND gates
Design	Simpler design with n-type and p-type metal oxide field-effect transistors.	More complex design with bipolar junction transistors.

The CMOS logic gate circuit is more energy-efficient, produces less noise, and packs a higher density of logic gates.