Static CMOS logic Styles

Tristate circuits :- (restoring logic)

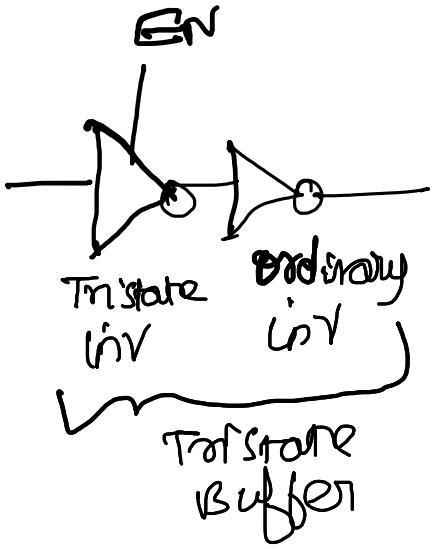
Tristate Buffer :-

when ENABLE = 1 output Y = input A

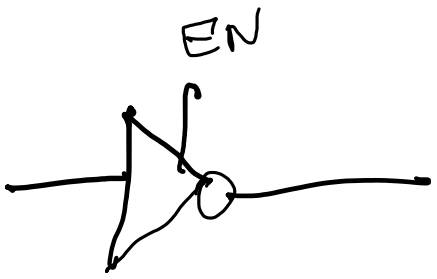
ENABLE = 0 output Y = Z

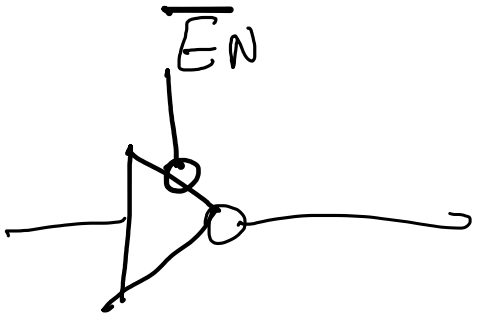
Truth table

EN/$\overline{EN}$	A	Y
0/1	0	Z
0/1	1	Z
1/0	0	0
1/0	1	1



Tristate Inverter :-

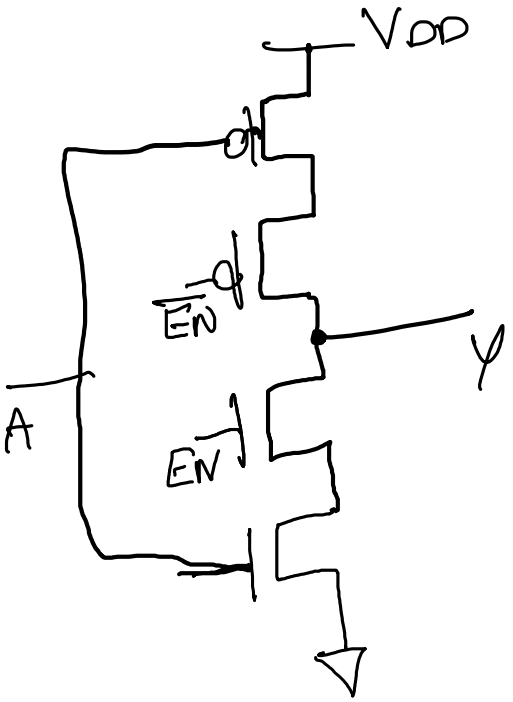




Truth table

EN/$\overline{EN}$	A	Y
0/1	0	Z
0/1	1	Z
1/0	0	1
1/0	1	0

Tristate inverter circuit

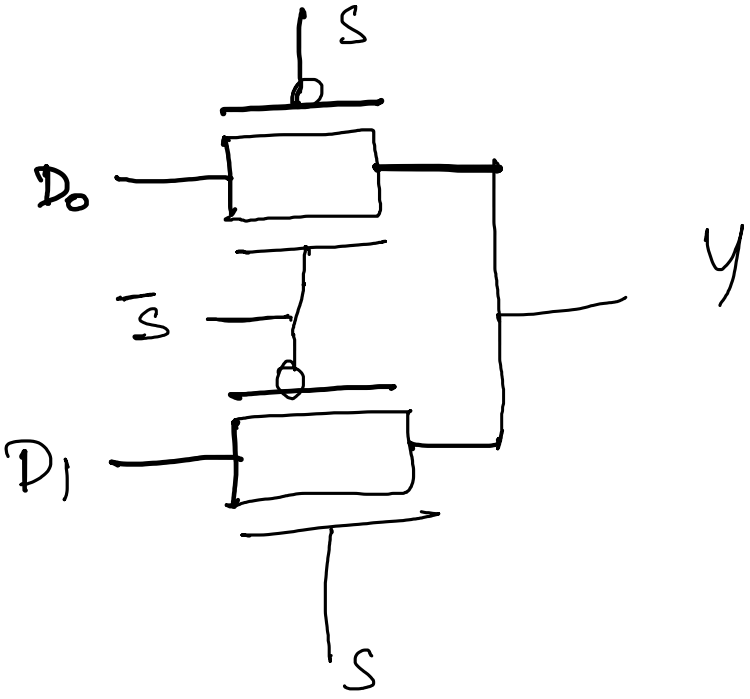


Multiplexers :-

2 : 1 MUX

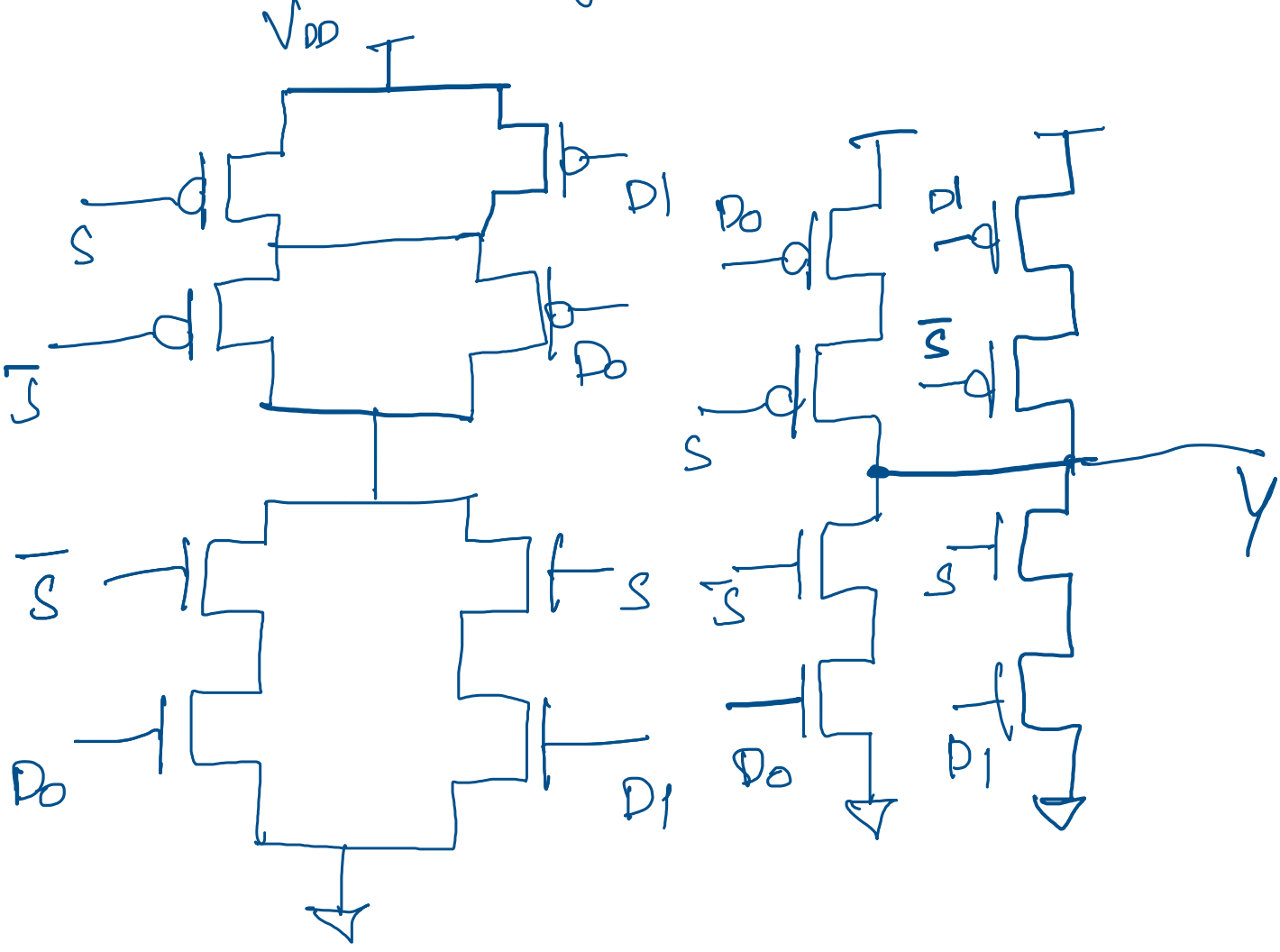
S/$\overline{S}$	D1	D0	Y
0/1	X	0	0
0/1	X	1	1
1/0	0	X	0
1/0	1	X	1

$$Y = \overline{S} D_0 + S D_1$$



2:1 MUX using TG

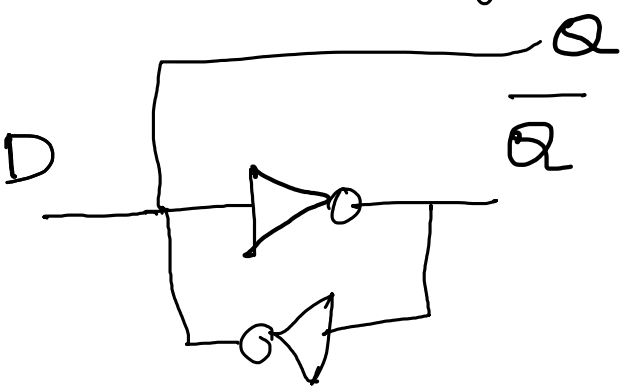
Multiplexer using Tristate logic

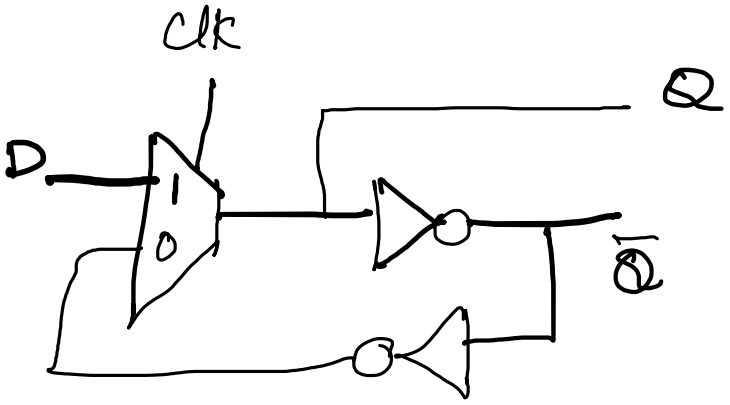


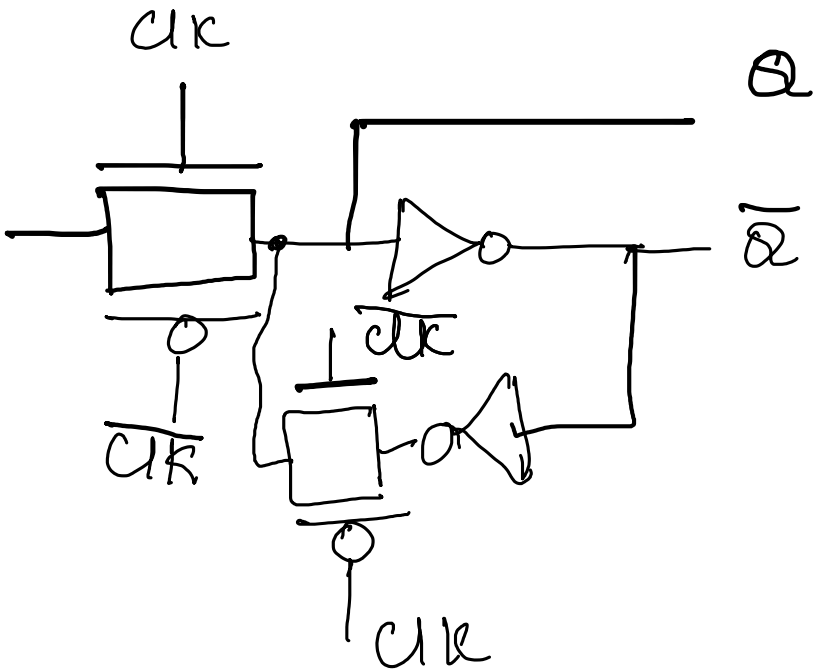
CMOS logic

Tristate 2:1 MUX

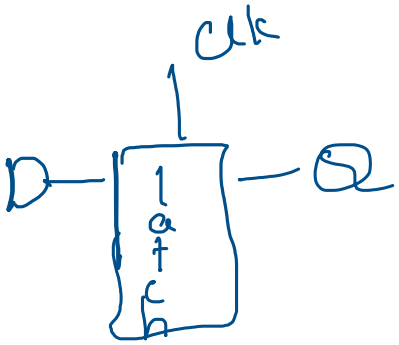
Clocked CMOS logic :-



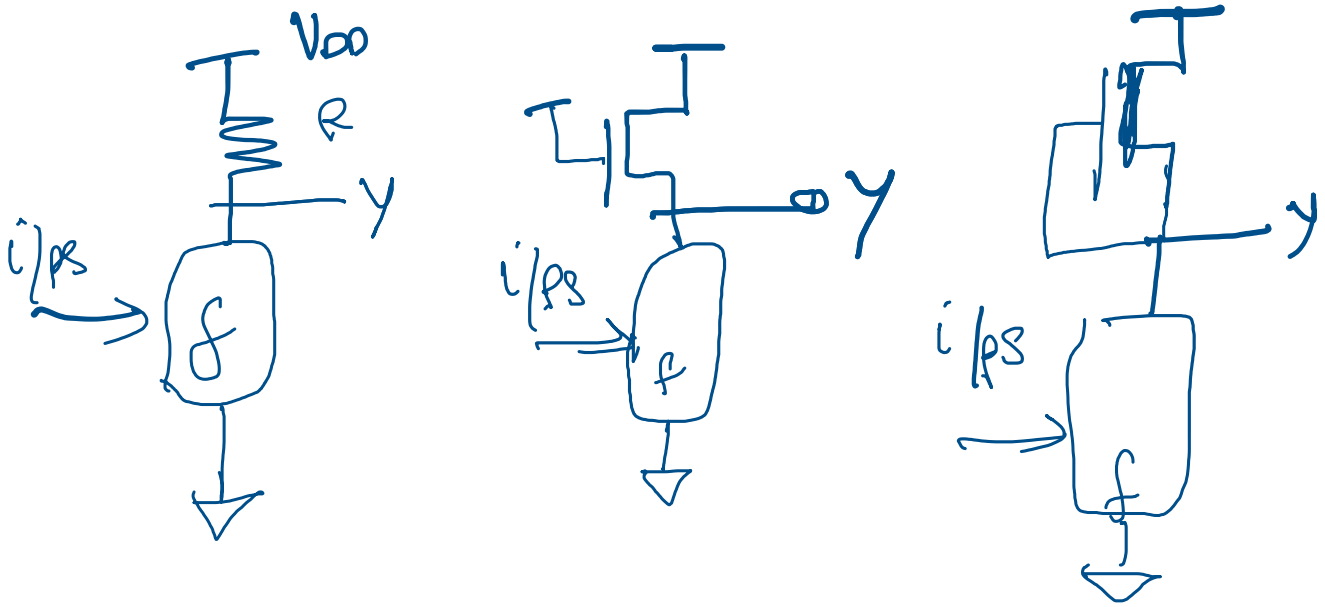




CMOS positive level sensitive Latch



Ratioed circuits :-



Pseudo nMOS :-

* Static load build from Si PMOS transistor rather than from either a high value resistor or depletion mode transistor

* in pseudo nMOS circuits static PMOS load is always gso so the transistor is always ON.

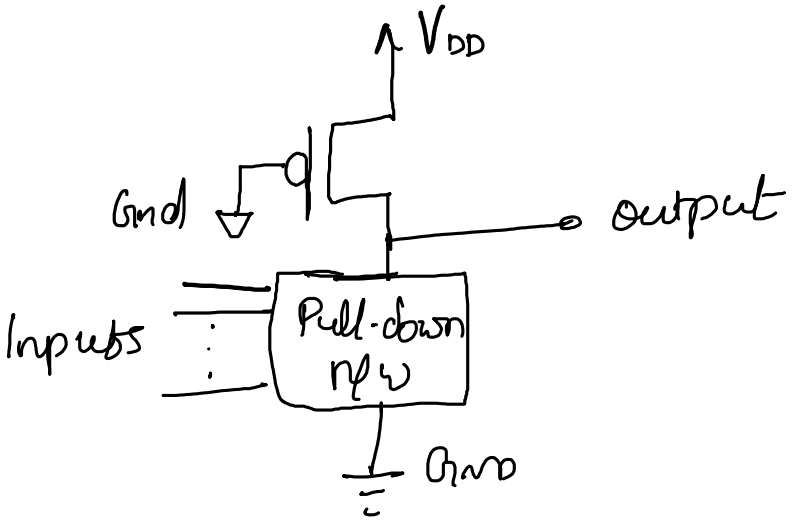
* Drawback is static power consumption but requires less no. of transistors to implement a logic.

* The main drawback of complementary logic circuit design is that it occupies larger area on the chip because for a given n inputs, the required number of transistor is 2n in the design.

* Also CMOS logic is slower because the applied input must drive both pull-up network (pMOS) and pull-down network (nMOS).

* pMOS has lower mobility than electron of nMOS and must be sized larger to achieve comparable current

* One approach to reduce the no. of transistors and area is to use single pMOS transistor with gate connected to ground so that pMOS is always ON and act as load. This is pseudo-nMOS logic.



Adv of pseudo nMOS logic over CMOS logic :-

* less no. of transistors is used.

For a given n inputs, the number of transistors required is (n+1) compared to 2n in CMOS logic

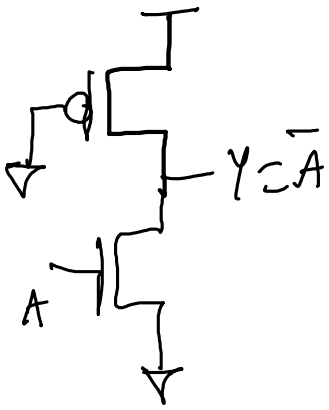
* less area on the chip
* compatible with CMOS
* hardwired logic compatible

Dis Adv :

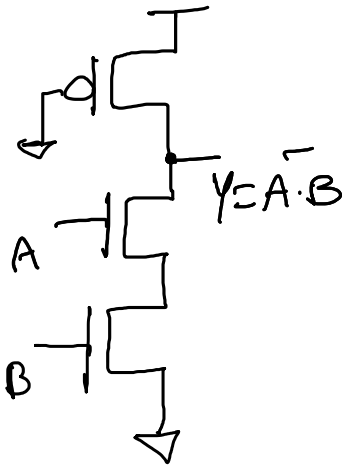
* reduced voltage swing at the o/p
* has non zero static power dissipation if output is zero.
* Ratioed logic

Examples :-

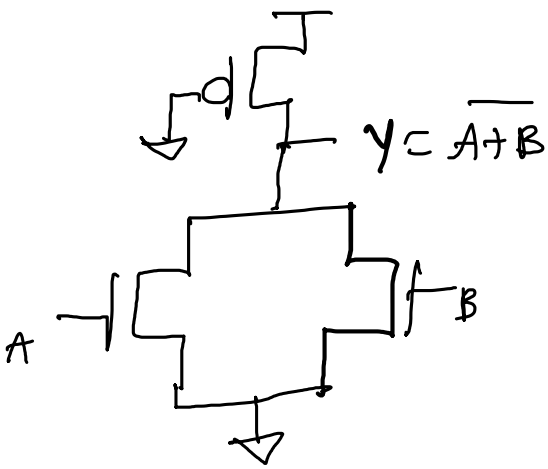
INV



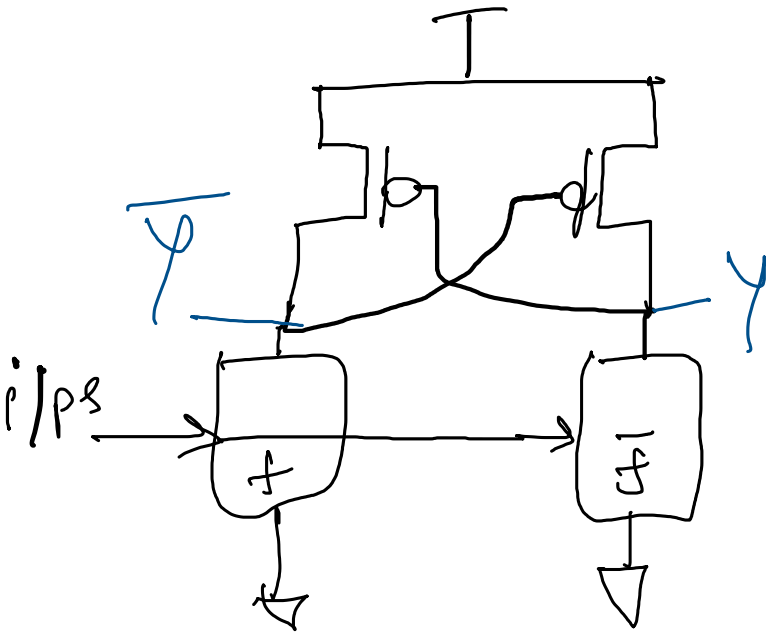
2-i/p NAND



2-i/p NOR



CVSL (Cascode voltage switch logic)
or DCVSL (Differential cascode voltage switch logic)

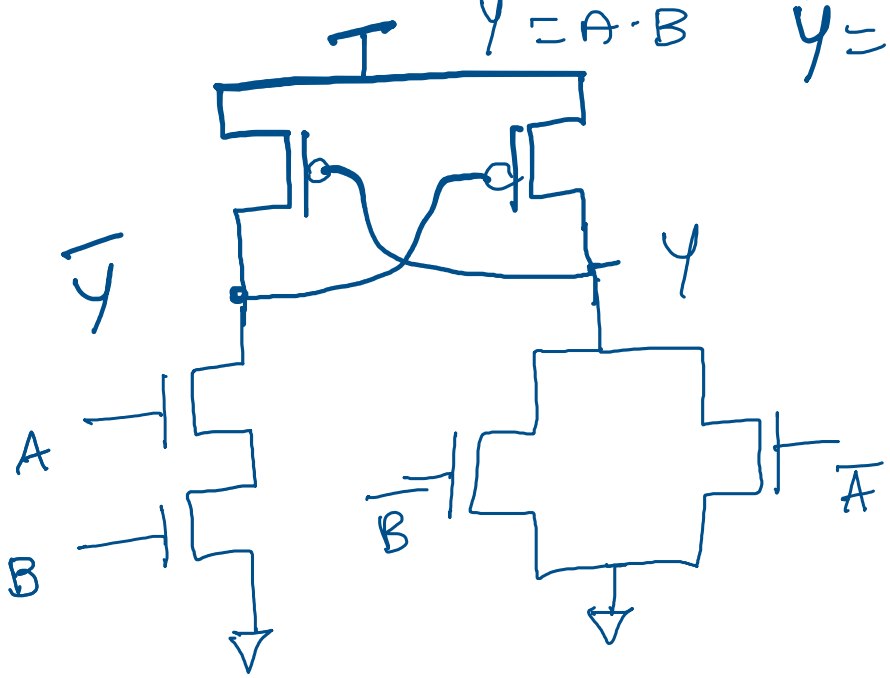


f → True form

$\bar{f}$ → Complement form

Eg :- 2 i/p AND gate

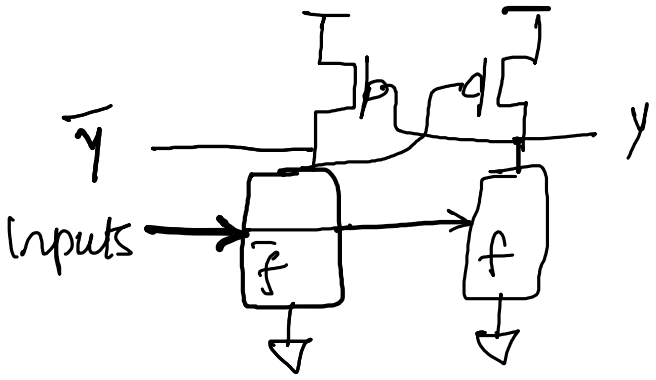
$Y = A \cdot B$ $\quad \bar{Y} = \overline{A \cdot B} = \bar{A} + \bar{B}$



DCVSL is an improved circuit design to eliminate the static current problem in pseudo-nMOS logic style.

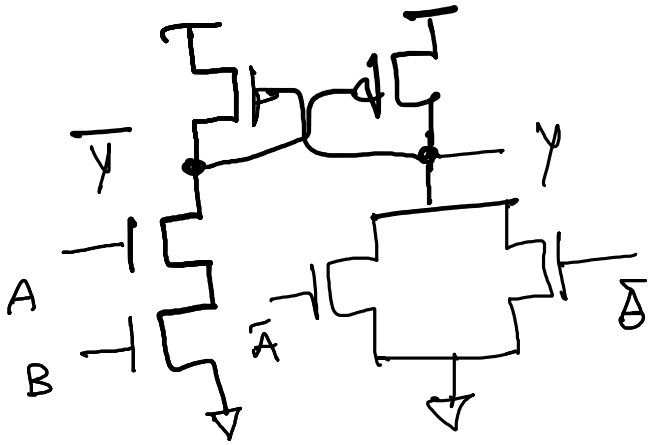
* DCVSL uses both true and complementary input signals and computes both true and complementary output signals.

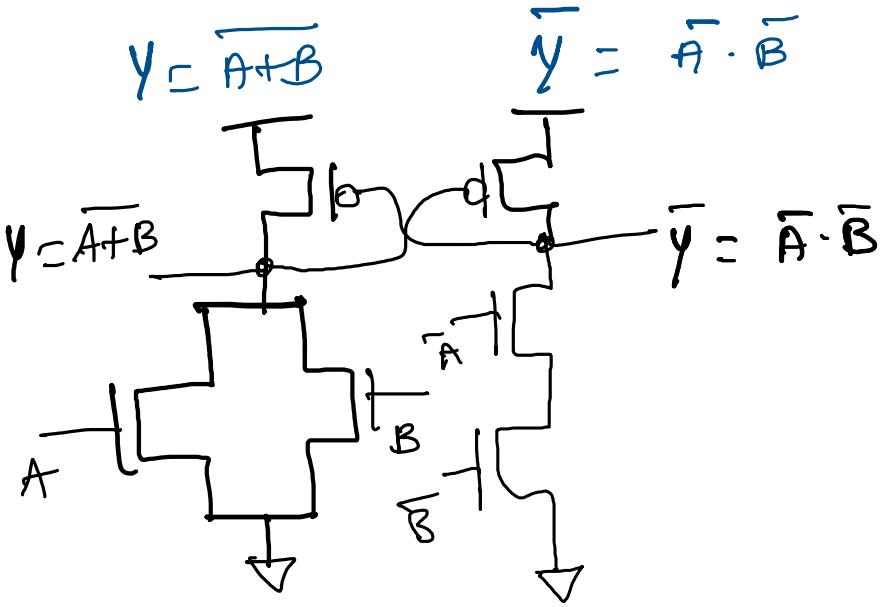
* It uses a pair of nMOS pull down networks



* Two functions of pull down n/w pair are complement of each other

$$Y = \overline{A \cdot B} \qquad \bar{Y} = \bar{A} + \bar{B} = A \cdot B$$




$Y = \overline{A+B}$
$\bar{y} = \bar{A} \cdot \bar{B}$
$Y = \overline{A+B}$
$\bar{y} = \bar{A} \cdot \bar{B}$
A
B
$\bar{A}$
$\bar{B}$