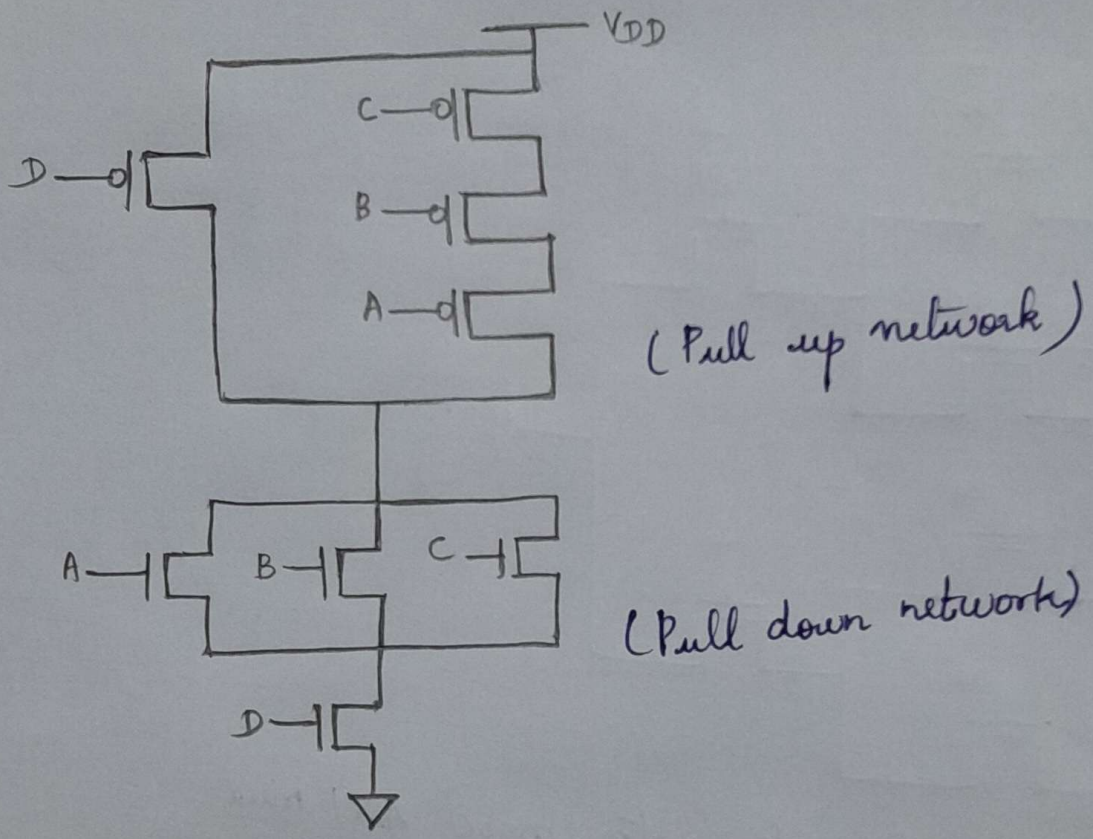
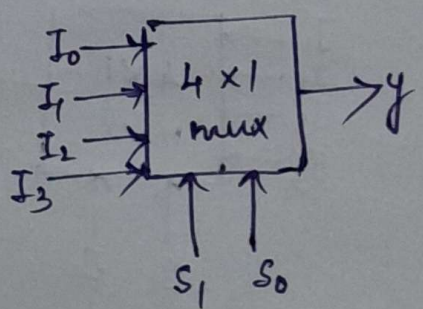
1. Sketch a Static CMOS gate computing $Y = \overline{(A+B+C)\cdot D}$



2. Design a 4 to 1 mux using

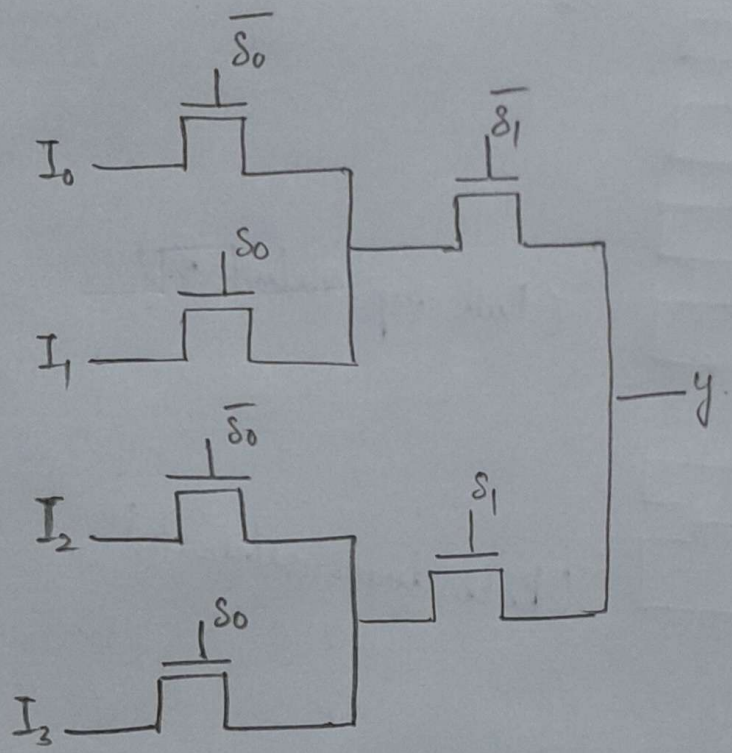
i) Pass transistor logic.

S_1	S_0	y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



$$y = \bar{S_1}\bar{S_0} I_0 + \bar{S_1} S_0 I_1 + S_1 \bar{S_0} I_2 + S_1 S_0 I_3$$

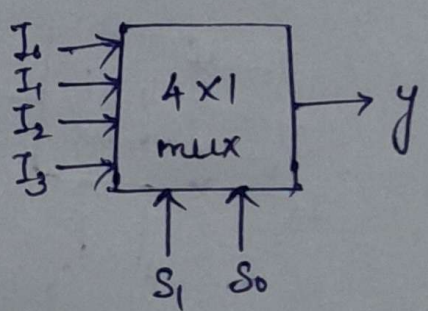
$$y = \bar{S_1}(\bar{S_0} I_0 + S_0 I_1) + S_1(\bar{S_0} I_2 + S_0 I_3)$$



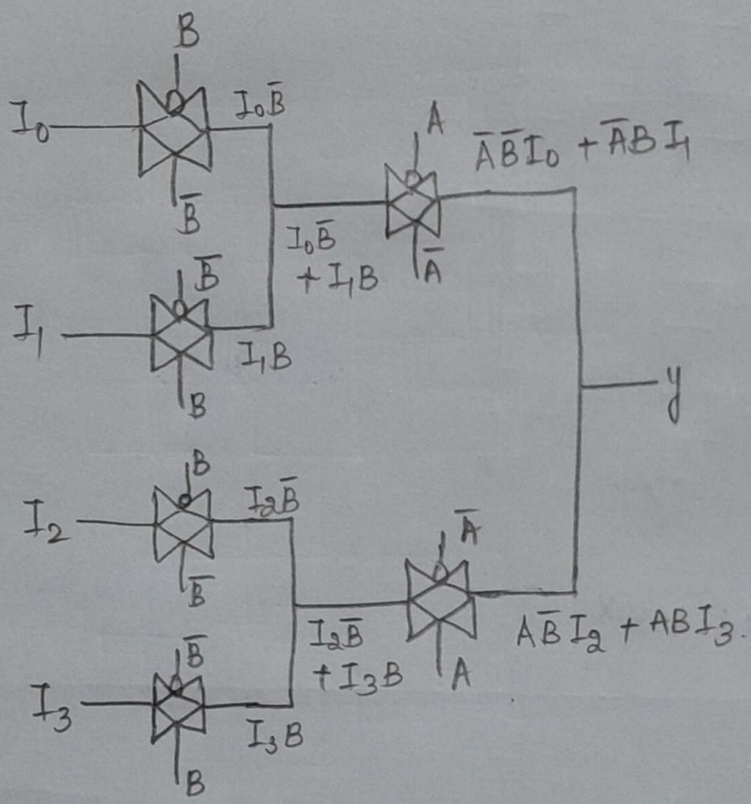
Pass transistor logic 4×1 mux.

ii) Transmission gate logic:

A	B	y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



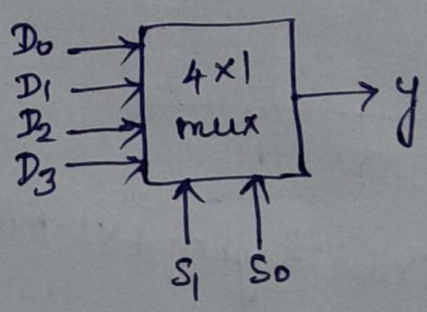
$$y = \bar{A}\bar{B}\cdot I_0 + \bar{A}BI_1 + A\bar{B}\cdot I_2 + ABI_3$$

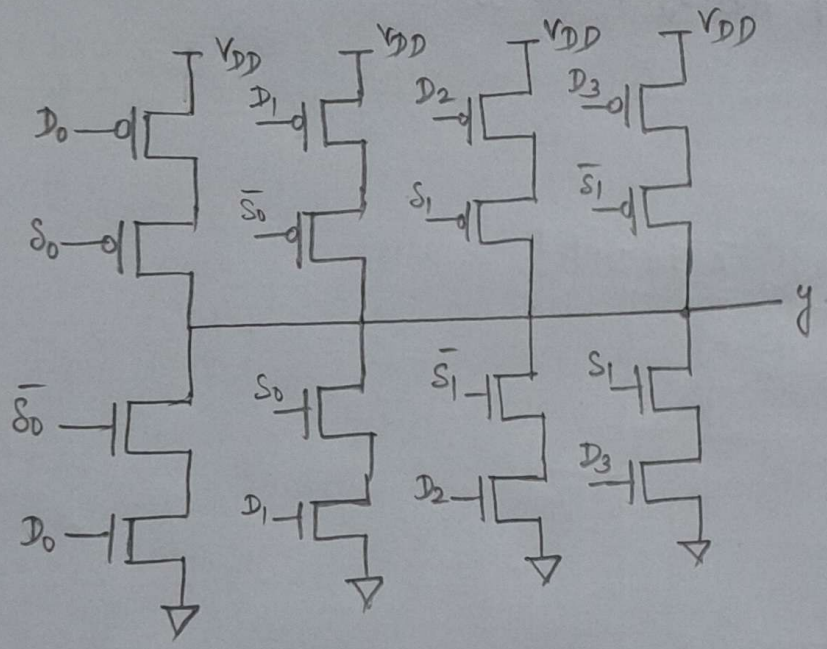


Transmission gate logic using 4×1 mux

iii) Tristate logic:

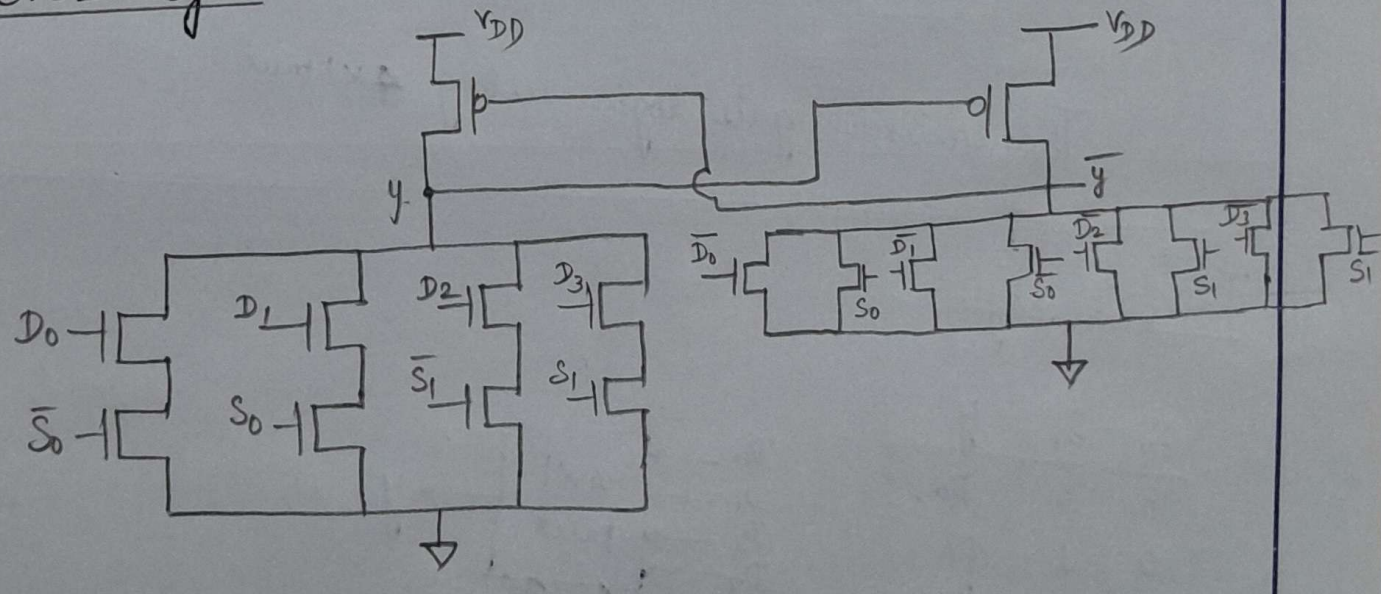
S_1	S_1	y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3





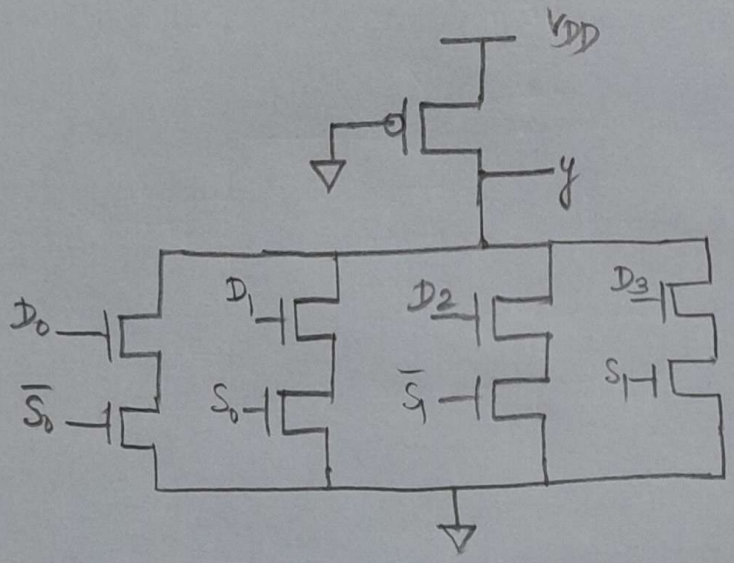
Tristate 4×1 mux.

iv) DCVSL Logic:



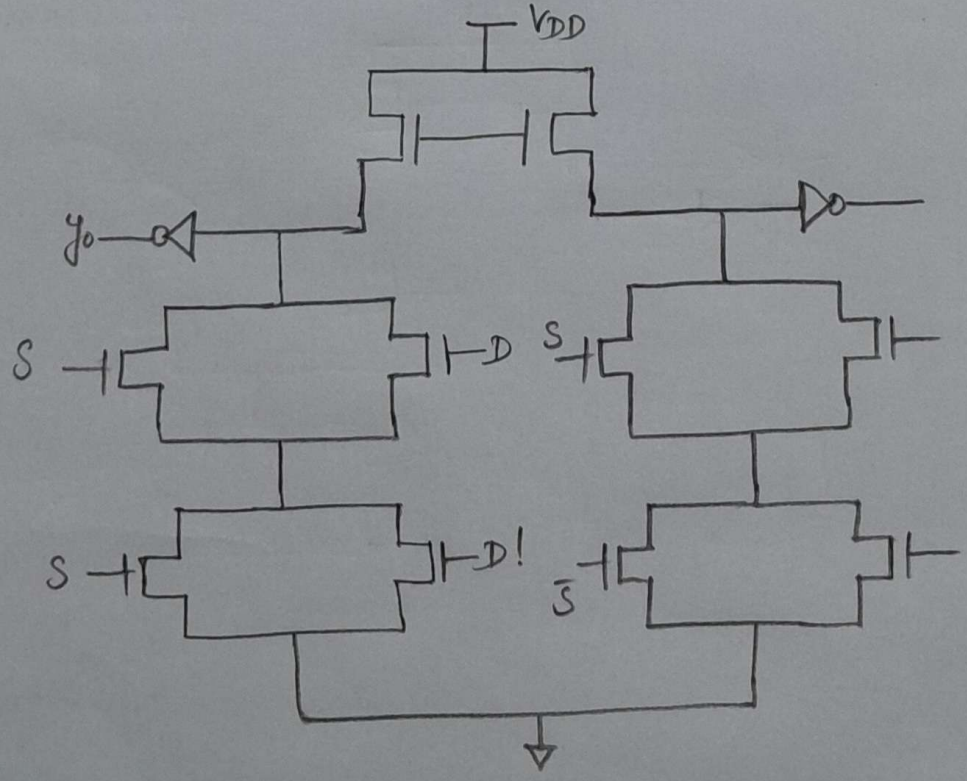
DCVSL Logic 4×1 mux.

v) Pseudo Nmos:



Pseudo Nmos 4×1 mux.

Design a 2×1 mux using domino logic:



Domino Logic 2×1 mux.