5TH SEM VLSI NOTES

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Th.2 VLSI & EMBEDDED SYSTEM

SYLLABUS

Unit-1: Introduction to VLSI & MOS Transistor

1.1 Historical perspective- Introduction

1.2 Classification of CMOS digital circuit types

1.3 Introduction to MOS Transistor& Basic operation of MOSFET.

1.4 **Structure and operation of MOSFET (n-MOS enhancement type) & COMS**

1.5 MOSFET V-I characteristics,

1.6 **Working of MOSFET capacitances.**

1.7 Modelling of MOS Transistors including Basic concept the SPICE level-1 models, the level-2 and level-3 model.

1.8 Flow Circuit design procedures

1.9 VLSI Design Flow & Y chart

1.10 Design Hierarchy

1.11 VLSI design styles-FPGA, Gate Array Design, Standard cells based, Full custom

Unit-2: Fabrication of MOSFET

2.1 Simplified process sequence for fabrication

2.2 Basic steps in Fabrication processes Flow

2.3 Fabrication process of nMOS Transistor

2.4 CMOS n-well Fabrication Process Flow

2.5 MOS Fabrication process by n-well on p-substrate

2.6 CMOS Fabrication process by P-well on n-substrate

2.7 Layout Design rules

2.8 Stick Diagrams of CMOS inverter

Unit-3: MOS Inverter

3.1 Basic nMOS inverters,

3.2 Working of Resistive-load Inverter

3.3 Inverter with n-Type MOSFET Load – Enhancement Load, Depletion n-MOS inverter

3.4 CMOS inverter – circuit operation and characteristics and interconnect effects: Delay time definitions

3.5 CMOS Inventor design with delay constraints – Two sample mask lay out for p-type substrate.

Unit-4: Static Combinational, Sequential, Dynamics logic circuits & Memories

4.1 Define Static Combinational logic ,working of Static CMOS logic circuits (Two-input NAND Gate)

4.2 CMOS logic circuits (NAND2 Gate)

4.3 CMOS Transmission Gates(Pass gate)

4.4 Complex Logic Circuits - Basics

4.5 Classification of Logic circuits based on their temporal behaviour

4.6 SR Flip latch Circuit,
4.7 Clocked SR latch only.
4.8 CMOS D latch.
4.9 Basic principles of Dynamic Pass Transistor Circuits
4.10 Dynamic RAM, SRAM,
4.11 Flash memory

Unit-5: System Design method & synthesis

5.1 Design Language (SPL & HDL)& HDL & EDA tools & VHDL and packages Xlinx

5.2 Design strategies & concept of FPGA with standard cell based design

5.3 VHDL for design synthesis using CPLD or FPGA

5.4 Raspberry Pi - Basic idea

Unit-6: Introduction to Embedded Systems

6.1 Embedded Systems Overview,list of embedded systems,characteristics ,example – A Digital Camera

6.2 Embedded Systems Technologies--Technology – Definition
-Technology for Embedded Systems
-Processor Technology
-IC Technology

6.3 Design Technology-Processor Technology,General Purpose Processors – Software, Basic Architecture of Single Purpose Processors – Hardware

6.4 Application – Specific Processors,Microcontrollers,Digital Signal Processors(DSP)

6.5 IC Technology- Full Custom / VLSI,Semi-Custom ASIC (Gate Array & Standard Cell), PLD (Programmable Logic Device)

6.6 Basic idea of Arduino micro controller

Unit-1

Introduction to VLSI & MOS Transistor

1.1 Historical perspective- Introduction

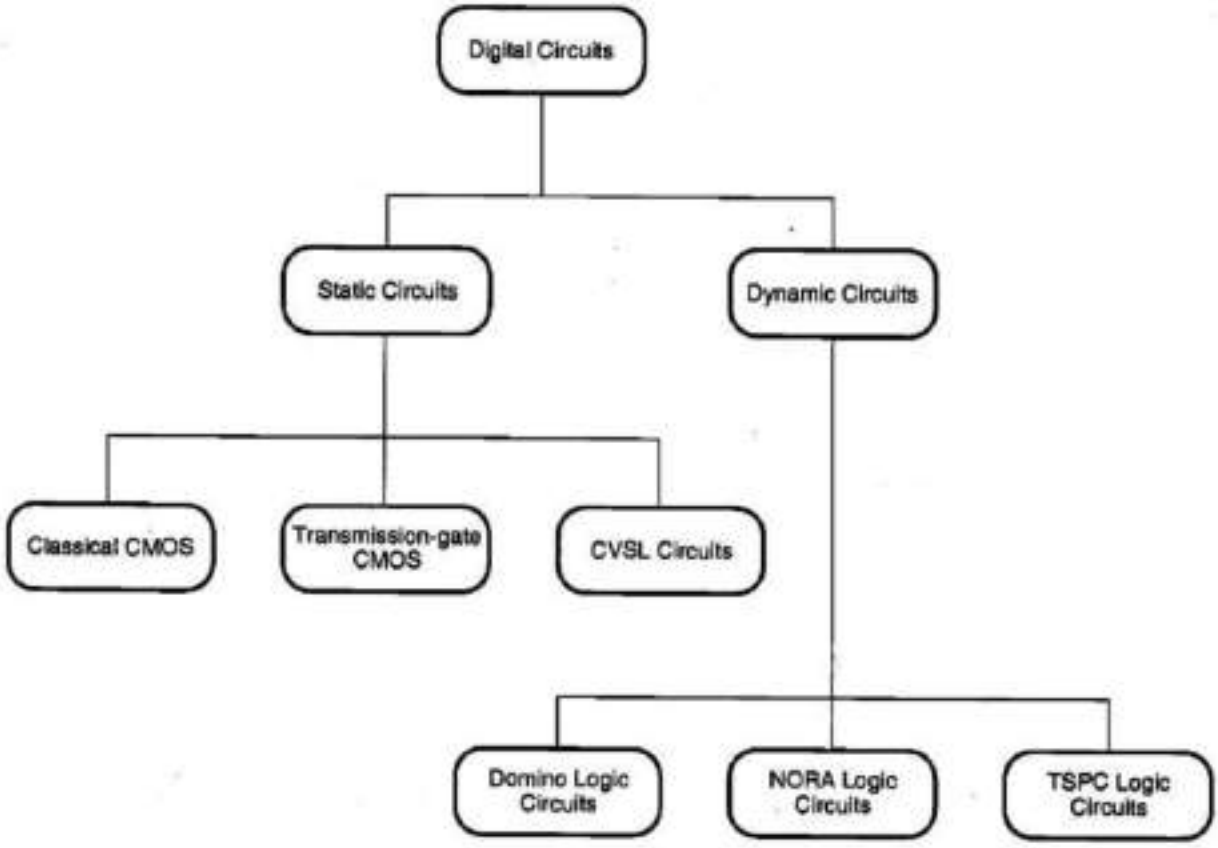
- The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in integration technologies and large-scale systems design.
- The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace.
- The current leading edge technologies (such as low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications for VLSI and systems design.
- The other important characteristic is that the information services tend to become more personalized, which means that the information processing devices must be more intelligent and also be portable to allow more mobility.
- The level of integration as measured by the number of logic gates in a monolithic chip has been steadily rising for almost three decades, mainly due to the rapid progress in processing technology and interconnect technology. Table 1.1 shows the evolution of logic complexity in integrated circuits over the last three decades, and marks the *milestones* of each era.
- A logic block can contain anywhere from 10 to 100 transistors, depending on the function. State-of-the-art ULSI chips, such as the *DEC Alpha* or the *INTEL Pentium,* contain 3 to 6 million transistors.

ERA	DATE	COMPLEXITY (# of logic blocks per chip)
Single transistor	1958	< 1
Unit logic (one gate)	1960	1
Multi-function	1962	2 - 4
Complex function	1964	5 - 20
Medium Scale Integration (MSI)	1967	20 - 200
Large Scale Integration (LSI)	1972	200 - 2,000
Very Large Scale Integration (VLSI)	1978	2,000 - 20,000
Ultra Large Scale Integration (ULSI)	1989	20,000 - ?

Table 1.1. Evolution of logic complexity in integrated circuits.

1.2 Classification of CMOS digital circuit types

- CMOS has become the technology of choice in many applications in recent years, the fundamental concepts of nMOS logic provide a strong basis both for the conceptual understanding and for the development of CMOS designs.
- Based on the fundamental operating principles, the circuits are classified into two main categories, i.e., static circuits and dynamic circuits. The static CMOS circuits are further divided into sub-categories such as classical (fully complementary) CMOS circuits, transmission-gate logic circuits, passtransistor logic circuits and cascade voltage switch logic (CVSL) circuits. The dynamic CMOS circuits are divided into sub-categories such as domino logic, NORA, and true ingle-phase clock (TSPC) circuits.



Classification of CMOS digital circuit types.

1.3 Introduction to MOS Transistor& Basic operation of MOSFET.

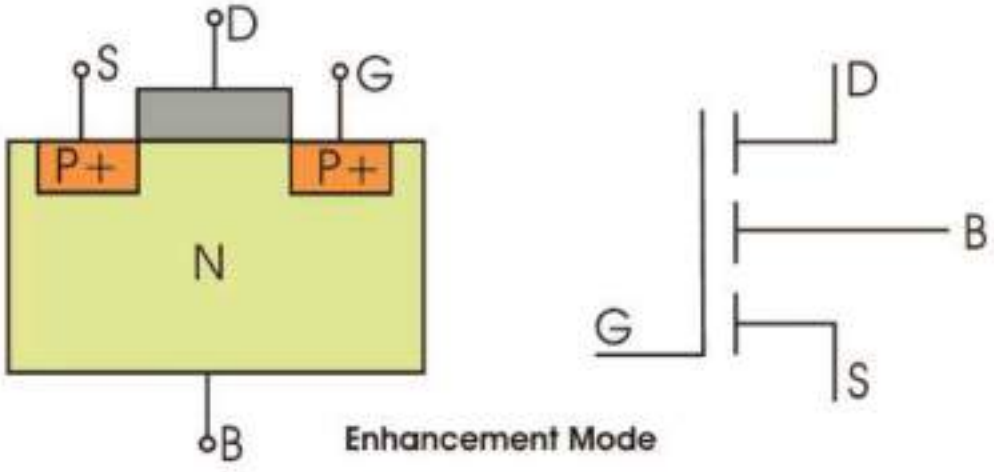
- The *MOS Field Effect Transistor* (MOSFET) is the fundamental building block of MOS and CMOS digital integrated circuits.
- Compared to the bipolar junction transistor (BJT), the MOS transistor occupies a relatively smaller silicon area, and its fabrication involves fewer processing steps. These technological advantages, together with the relative simplicity of

MOSFET operation, have helped make the MOS transistor the most widely used switching device in LSI and VLSI circuits.

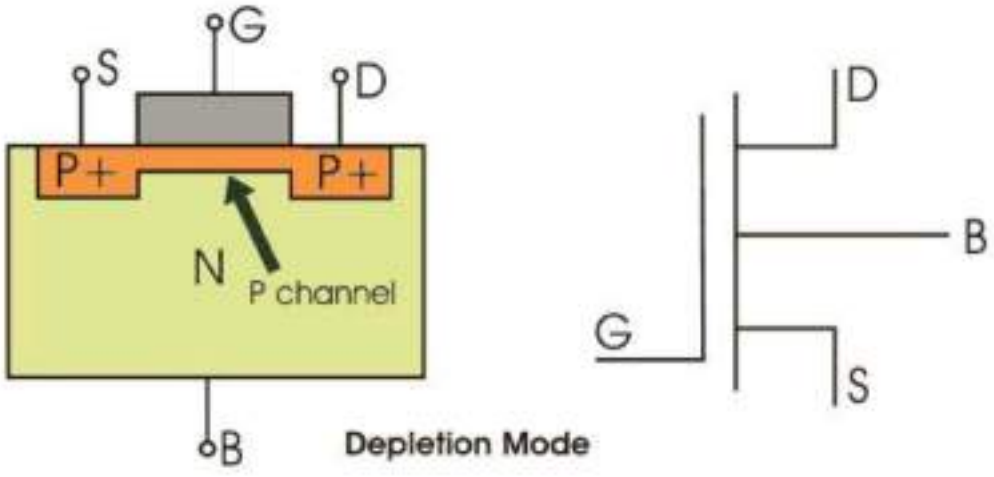
- The nMOS transistor is used as the primary switching device in virtually all digital circuit applications, whereas the pMOS transistor is used mostly in conjunction with the nMOS device in CMOS circuits. However, the basic operation principles of both nMOS and pMOS transistors are very similar to each other.

MOSFET OPERATION

- The working of a MOSFET depends upon the MOS capacitor. The MOS capacitor is the main part of MOSFET. The semiconductor surface at the below oxide layer which is located between source and drain terminals. It can be inverted from p-type to n-type by applying positive or negative gate voltages.
- When we apply positive gate voltage the holes present under the oxide layer with a repulsive force and holes are pushed downward with the substrate. The depletion region populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach the channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the



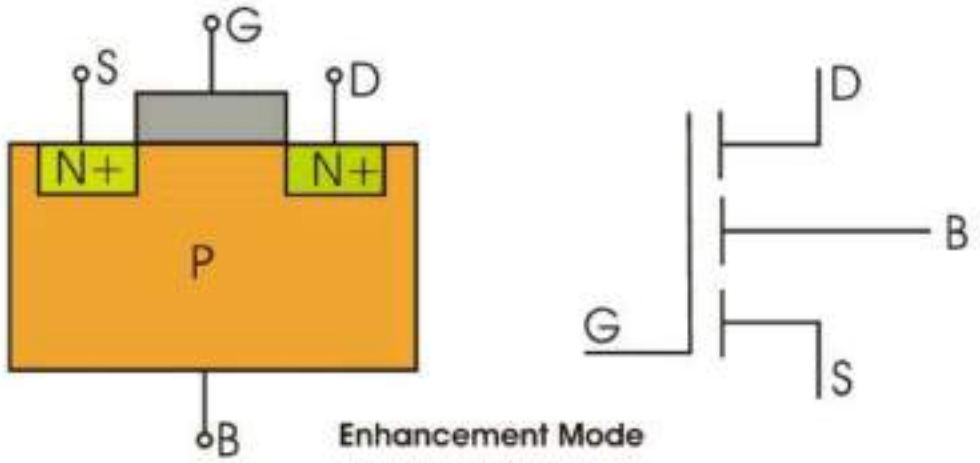
Enhancement Mode



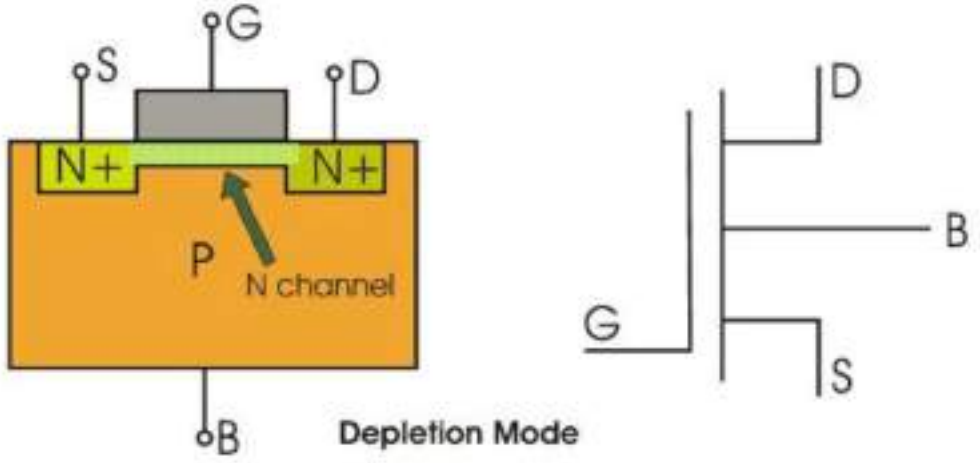
Depletion Mode

electrons in the channel. If we apply negative voltage, a hole channel will be formed under the oxide layer.

- P-Channel MOSFET
- P-Channel MOSFET
- The drain and source are heavily doped p+ region and the substrate is in n-type. The current flows due to the flow of positively charged holes also known as p-channel MOSFET. When we apply negative gate voltage, the electrons present beneath the oxide layer experience repulsive force and they are pushed downward in to the substrate, the depletion region is populated by the bound positive charges which are associated with the donor atoms. The negative gate voltage also attracts holes from p+ source and drain region into the channel region.
- N-Channel MOSFET
- N-Channel MOSFET



Enhancement Mode



Depletion Mode

- The drain and source are heavily doped n+ region and the substrate is p-type. The current flows due to the flow of negatively charged electrons, also known as n-channel MOSFET. When we apply the positive gate voltage the holes present beneath the oxide layer experience repulsive force and the holes are pushed downwards in to the bound negative charges which are associated with the acceptor atoms. The positive gate voltage also attracts electrons from n+

source and drain region in to the channel thus an electron reach channel is formed.

1.5 MOSFET V-I characteristics voltages

It is a graph of drain current I_d versus drain to source voltage V_{DS} for different values of the gate to source voltage V_{GS}. It has three regions; **saturation, cut-off,** and **ohmic region.** In the application where the MOSFET used as a switch, the device works in the cut-off region and ohmic region when turned OFF and ON respectively. The operation in the saturation region avoided reducing the power dissipation in the on-state.

1. Cut-Off Region
   Cut-off region is a region in which the MOSFET will be OFF as there will be no current flow through it. In this region, MOSFET behaves like an open switch and is thus used when they are required to function as electronic switches.
2. Ohmic or Linear Region
   Ohmic or linear region is a region where in the current I_{DS} increases with an increase in the value of V_{DS}. When MOSFETs are made to operate in this region, they can be used as amplifiers.
3. Saturation Region
   In saturation region, the MOSFETs have their I_{DS} constant inspite of an increase in V_{DS} and occurs once V_{DS} exceeds the value of pinch-off voltage V_P. Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows. As a result, this operating region is chosen whenever MOSFETs are required to perform switching operations.

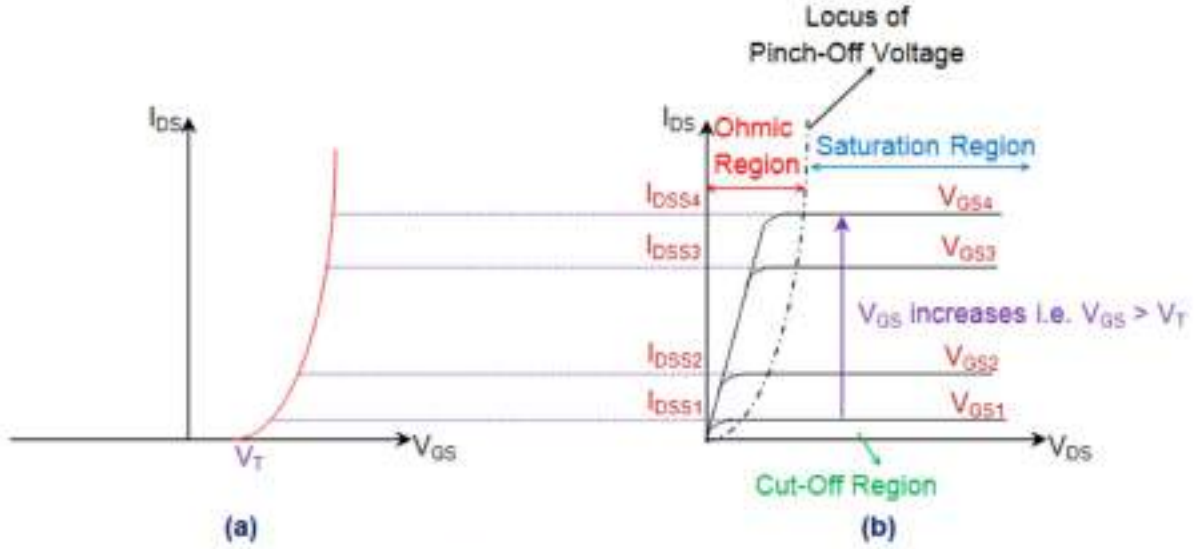


Figure 1 *n*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

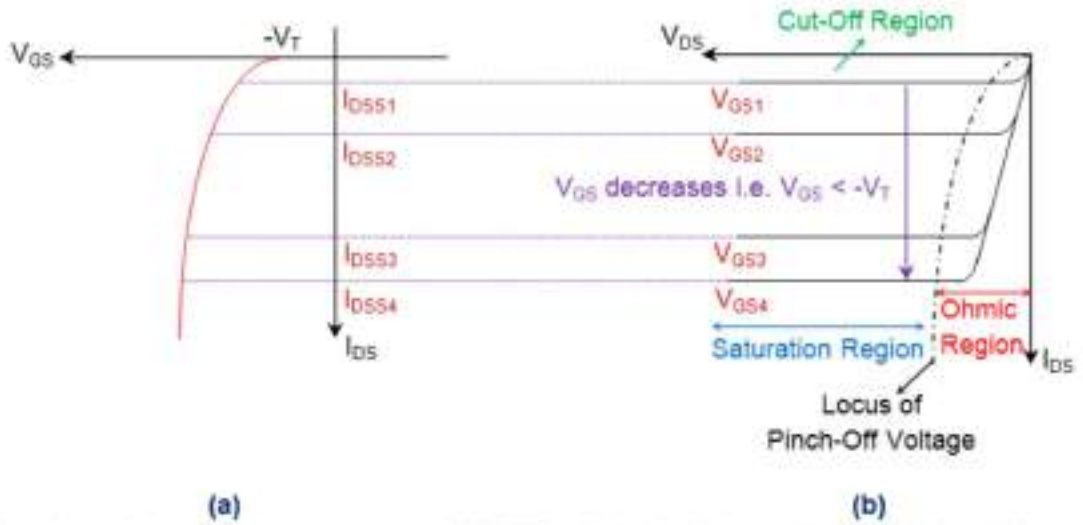


Figure 2 *p*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

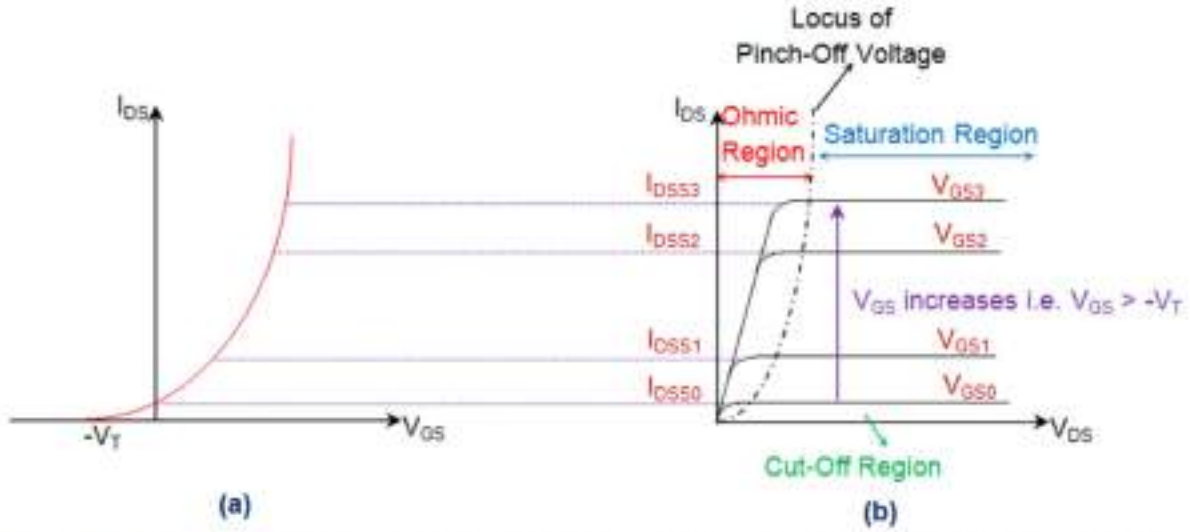


Figure 3 *n*-Channel Depletion type MOSFET (a) Transfer Characteristics (b) Output Characteristics

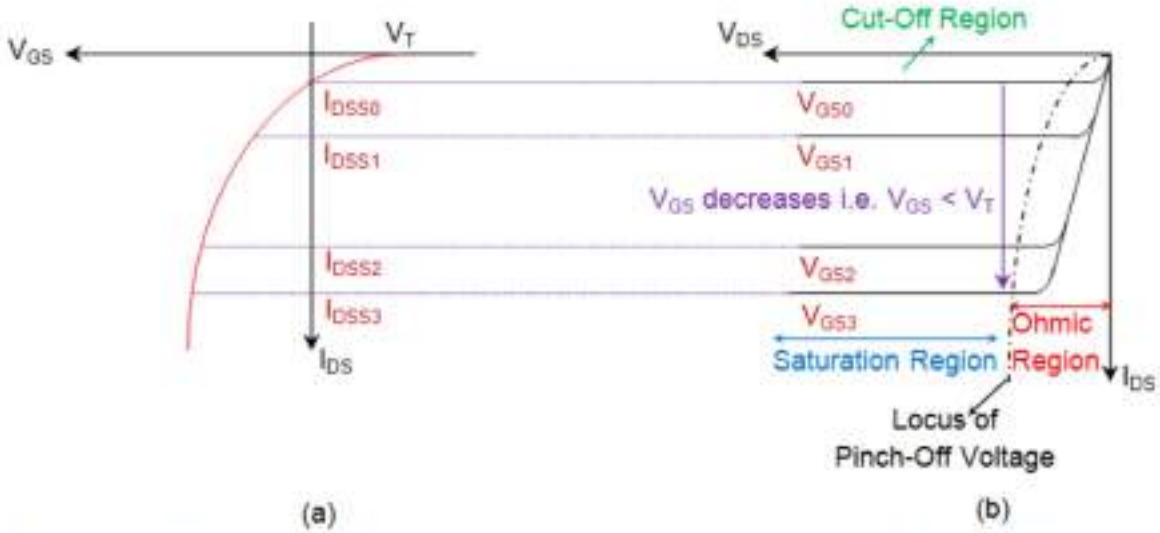


Figure 4 *p*-Channel Depletion type MOSFET (a) Transfer Characteristics (b) Output Characteristics

Kind of MOSFET	Region of Operation		
	Cut-Off	**Ohmic/Linear**	**Saturation**
n-channel Enhancement-type	$V_{GS} < V_T$	$V_{GS} > V_T$ and $V_{DS} < V_P$	$V_{GS} > V_T$ and $V_{DS} > V_P$
p-channel Enhancement-type	$V_{GS} > -V_T$	$V_{GS} < -V_T$ and $V_{DS} > -V_P$	$V_{GS} < -V_T$ and $V_{DS} < -V_P$
n-channel Depletion-type	$V_{GS} < -V_T$	$V_{GS} > -V_T$ and $V_{DS} < V_P$	$V_{GS} > -V_T$ and $V_{DS} > V_P$
p-channel Depletion-type	$V_{GS} > V_T$	$V_{GS} < V_T$ and $V_{DS} > -V_P$	$V_{GS} < V_T$ and $V_{DS} < -V_P$

1.7 Modelling of MOS Transistors including Basic concept the SPICE level-1 models, the level-2 and level-3 model

SPICE (Simulation Program with Integrated Circuit Emphasis)

- It is a general-purpose, open source analog electronic circuit simulator.
- It is a program used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behaviour.
- It is used in transistor level design.
- SPICE is one of the oldest and most popular simulating software.

There are three levels of SPICE:

- Level 1
- Level 2
- Level 3

Level 1: -

- It is developed in 1973 which was originally written in FORTRAN
- It can be use for quick estimates when accuracy is not a concern.
- It used nodal analysis and fixed step transient analysis which were creating problems and hence an improved version called SPICE level 2 came into picture.
- It provides the unique and rough estimate of the circuit performance without much accuracy.

Level 2: -

- It is a geometric base model which use detail device physics to define its equations.
- It handles velocity saturation.
- Mobility degradation.
- 3D effects of an submicron process in a pure physics based modes become complex and in accurate.
- Level 2 was released in 1975 which is also written FORTRAN.
- It is capable of during anythings like AC analysis, transfer function analysis, transient analysis.

- The level 2 Model requires the larger time.

SPICE Level 3 Model : -

Level 3 is a semi empirical model. It relieves on a mixer of analysical and empirical expression and uses device data to determine the main parameters.

- It works quite well for channel length less than 1 mm
- Level 3 was released 1989 which was written in C.
- Level 3 are sophisticated MOSFET models
- It had a command line features
- The CPU time needed for model evaluation is less.
- 1.8 Flow Circuit design procedures

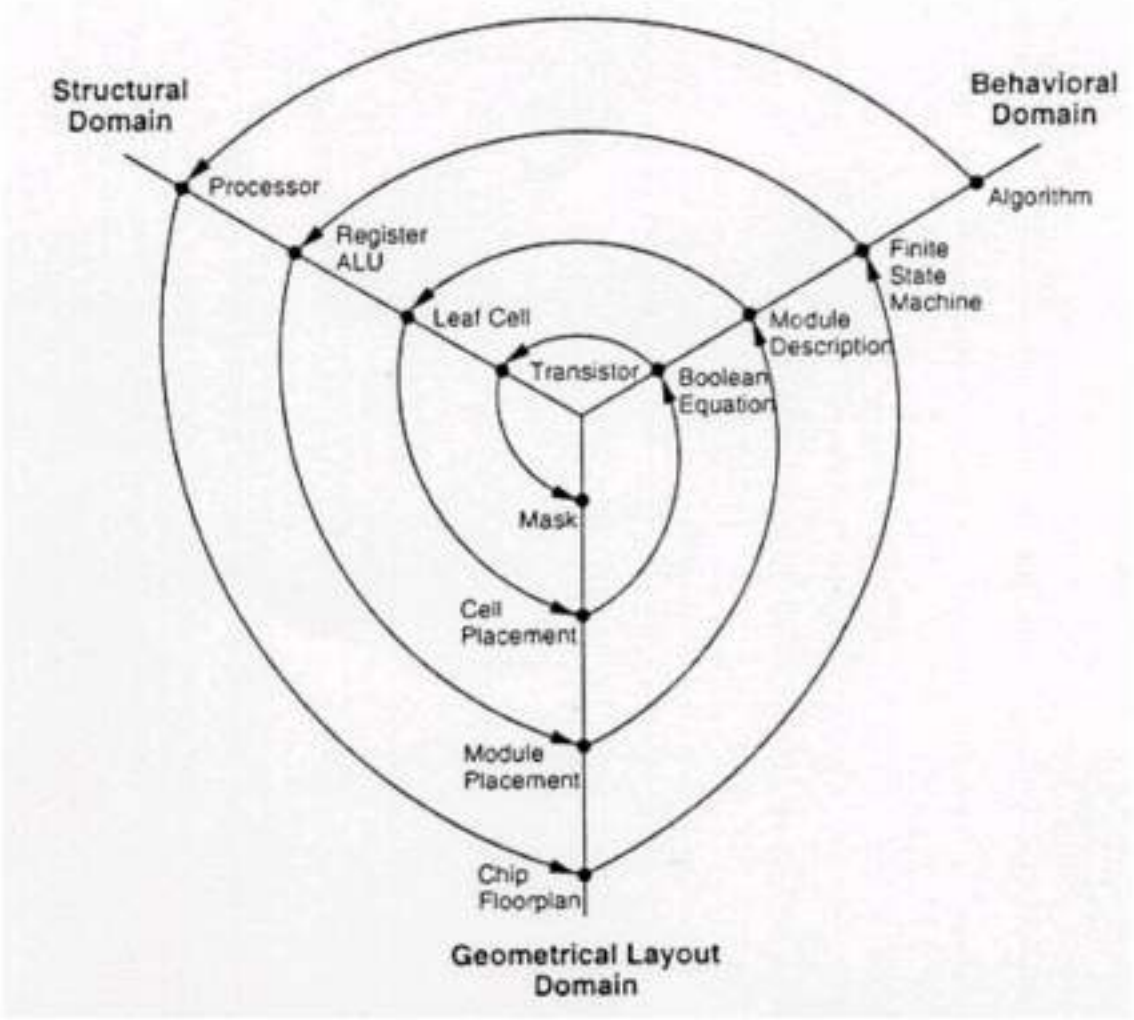
1.9 VLSI Design Flow & Y chart

VLSI Design Flow :-

- In design process, at various levels, is usually evolutionary in nature. It starts with a given set of requirements.
- Initial design is developed and tested as per the requirements.
- When requirements are not met, the design has to be improved.
- If such improvement is either not possible or too costly, then a revision of requirements and an impact analysis must be considered.

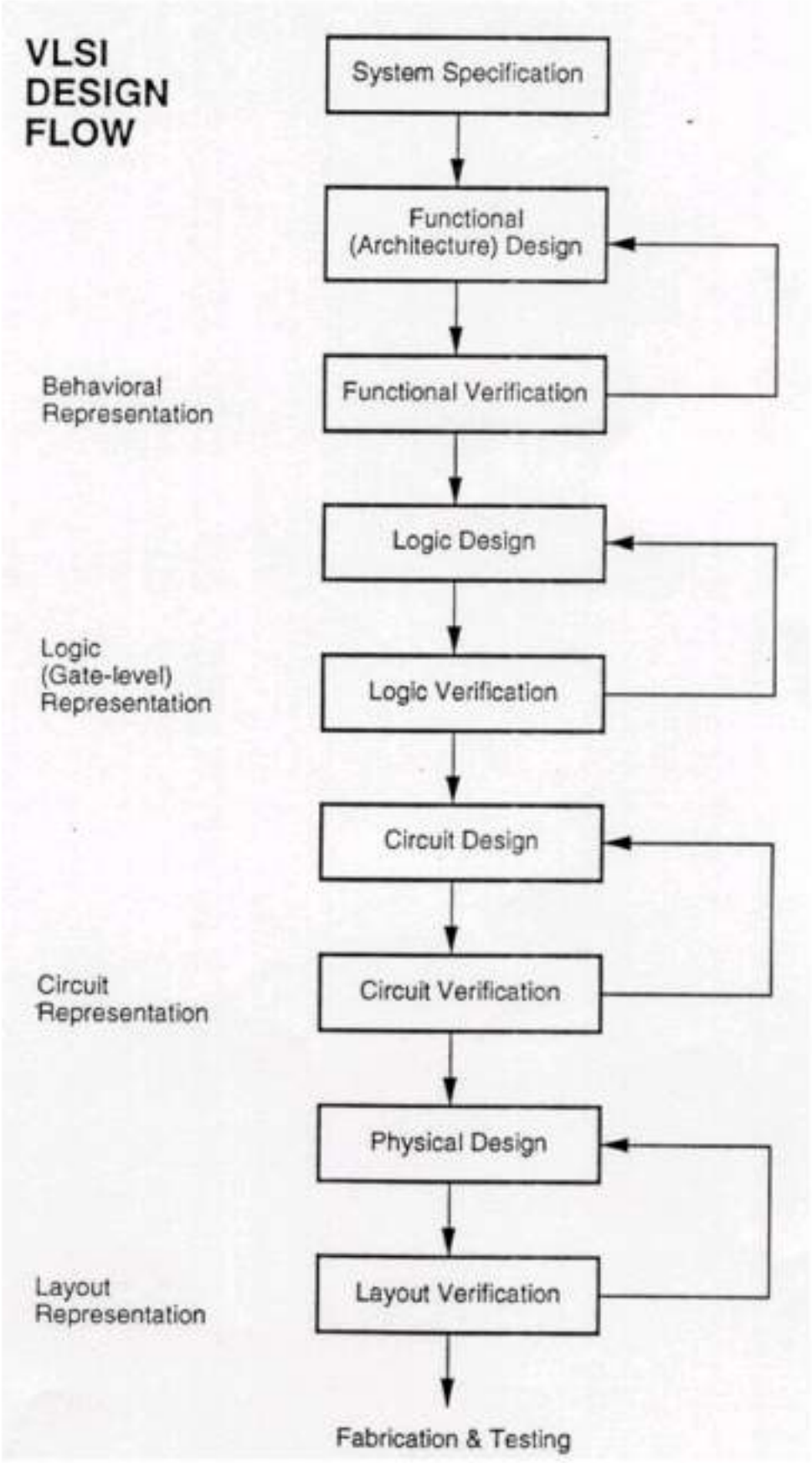
Y-chart :-

- Y-chart is introduced by D. Gayske.
- Y- chart explains a simplified design flow for most logic chips using design actuates on three different axis which ressemble the "Y" letter.
- The Y-chart consists of three domains which are represented with three axis, namely:-
    - Behavioural Domain.
    - Structural Domain.
    - Geometrical Layout Domain.



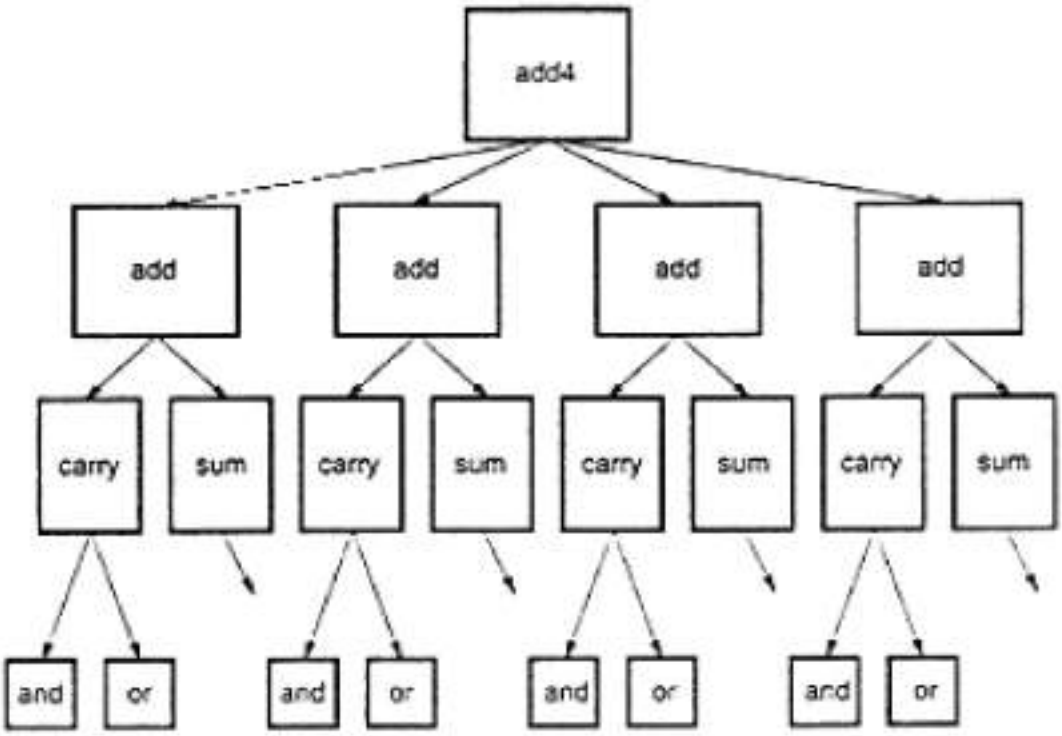
- The design flow starts from the algorithm that describes the behavior of the target chip.
- The corresponding architecture of the processor is first define in the structural domain. It is mapped onto the chip surface by floor planning.
- The next design evolution in the behavioral domain defines finite state machines (FSMs) which are structurally implemented with functional modules such as registers and arithmetic logic units (ALUs).
- These modules are then geometrically placed onto the chip surface using CAD tools for automatic module placement followed by routing, with a goal of minimizing the interconnection area and signal delays.
- The third evolution starts with a behavioral module description then individual modules are then implemented with leaf cells at this stage the chip is described in terms of logic gates or leaf cells, which can be placed and interconnected by using a cell placement.
- The last evolution involves a detailed Boolean description of leaf cells followed by a transistor level implementation of leaf cells and mask generation.
- In the cell based design style, leaf cells are pre designed and stored in a library for logic implementation, effectively eliminating the need for the transistor level design.

SIMPLIFIED VIEW OF THE VLSI DESIGN FLOW



1.10 Design Hierarchy :-

- The use of the hierarchy, or "divide and conquer".
- Dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.
- This approach is very similar to software development wherein large programs are split into smaller and smaller sections until simple subroutines, with well-defined functions and interfaces, can be written.
- In the physical domain, partitioning a complex system into its various functional blocks will provide a valuable guide for the actual realization of these blocks on the chip.



Regularity, Modularity and Locality

Regularity means that the hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible.

- A good example of regularity is the design of array structures consisting of identical cells - such as a parallel multiplication array.

Modularity in design means that the various functional blocks which make up the larger system must have *well-defined functions* and *interfaces.*

- Modularity allows that each block or module can be designed relatively independently from each other, since there is no ambiguity about the function and the signal interface of these blocks.

Locality also ensures that connections are mostly between neighboring modules, avoiding long-distance connections as much as possible. This last point is extremely important for avoiding long interconnect delays.

1.11 VLSI design styles-FPGA, Gate Array Design, Standard cells based, Full custom

❖ VLSI design styles-FPGA:-

FPGA (Field Programmable Gate Array):-

- It contain thousands or even more, of logic gates with programmable interconnections.
- Programmable interconnects, are available to users for their custom hardware programming to realize desired functionality.
- A typical field programmable gate array (FPGA) chip consists of I/O buffers, an array of configurable logic blocks (CLBs), and routing channel.

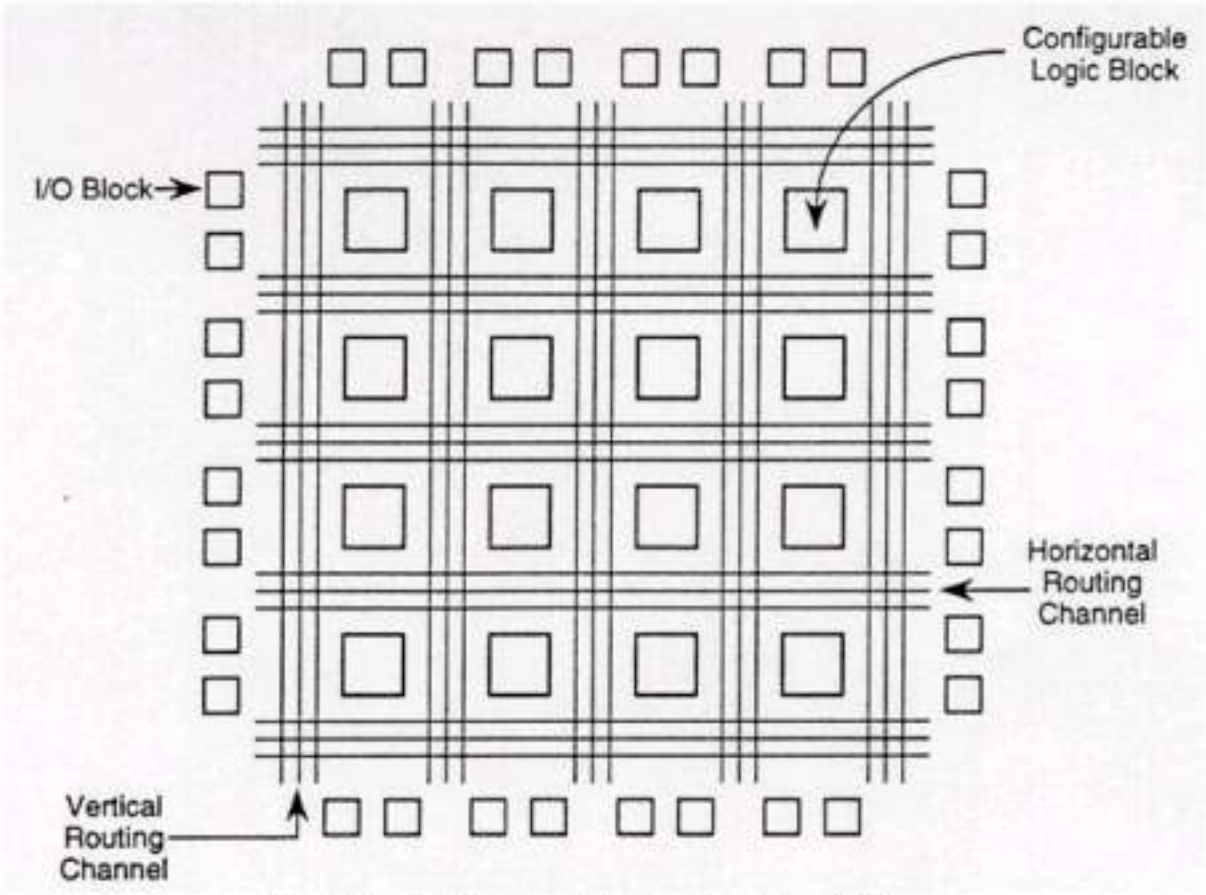


Figure 14.10. **General architecture of Xilinx FPGAs.**

- I/O blocks are designed and numbered.
- CLB perform the logic operation given to the module.
- The connection between CLB and I/O blocks are done through vertical routing channel are horizontal routing channel and programmable multiplexer.
- The complexity of FPGA depends on the number of CLB.
- The function of CLB are defined by VHDL.
- CLB consists of D flip flop.
- The CLB minimise the number of blocks.

Advantages of FPGA:-

- It requires very time (starting from design process to functional chip)
- No physical manufacturing steps.

Disadvantages of FPGA:-

- It is costlier.

❖ Gate Array Design:-

- The gate array (GA) ranks second after the FPGA in terms of f, metal mask design and processing is used for
- Gate array implementation requires a two-step manufacturing process:
- The first phase results in an array of uncommitted transistor. Then the metal interconnectivity between the transistors of the array are define.
- The patterning of metallic interconnects is done at the end of the chip fabrication process, the turn-around time can still be short.
- Gate array platform used channel for itercell routing.
- Multiple metal layers are used for channel routing.

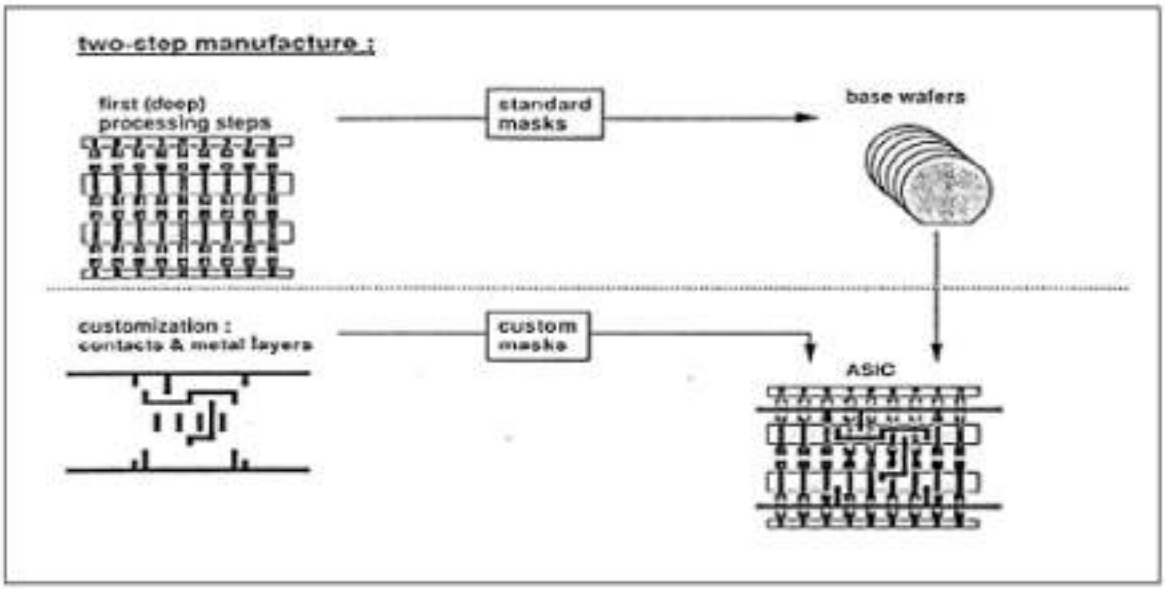


Figure . **Basic processing steps required for gate array implementation.**

❖ Standard Cells Based:-

- The standard-cells based design which require development of a full custom mask set.
- The standard cell is also called the polycell. In this design style, all of the commonly used logic cells are developed.
- Characterized, and stored in a standard cell library.
- For automated placement of cell and routing each cell layout is designed with a fixed fight so that a number of cell can be bounded to form rows.

- Each cell is characterized according to several different characterization categories, including

    * Delay time versus load capacitance
    * Circuit simulation model
    * Timing simulation model
    * Fault simulation model
    * Cell data for place-and-route
    * Mask data

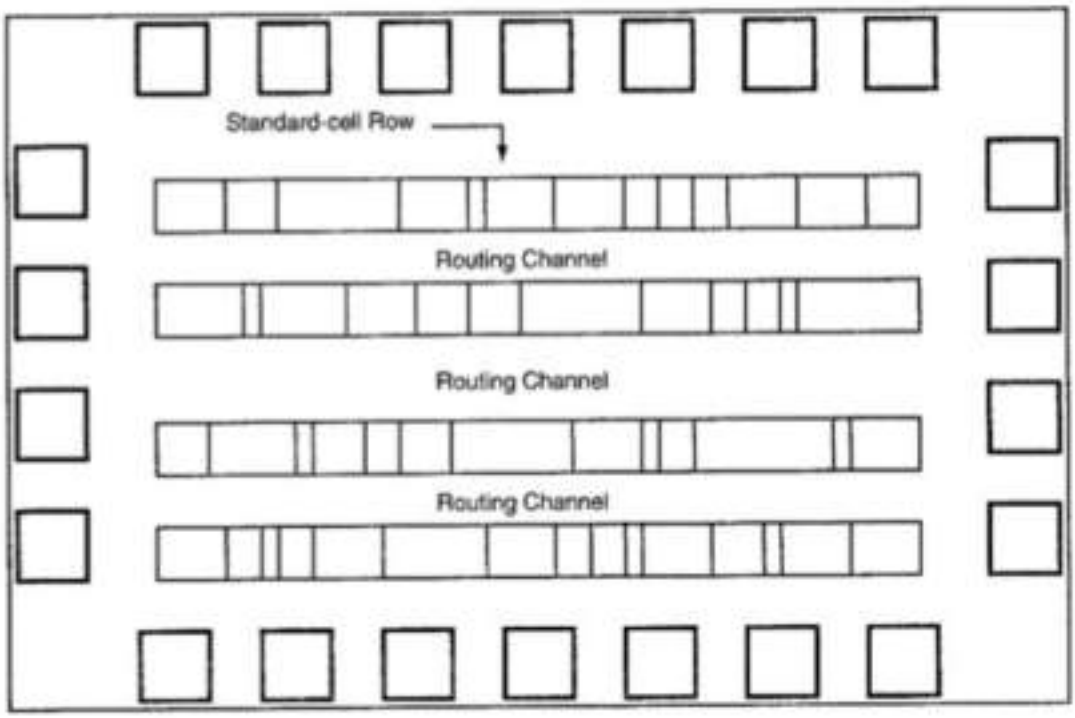
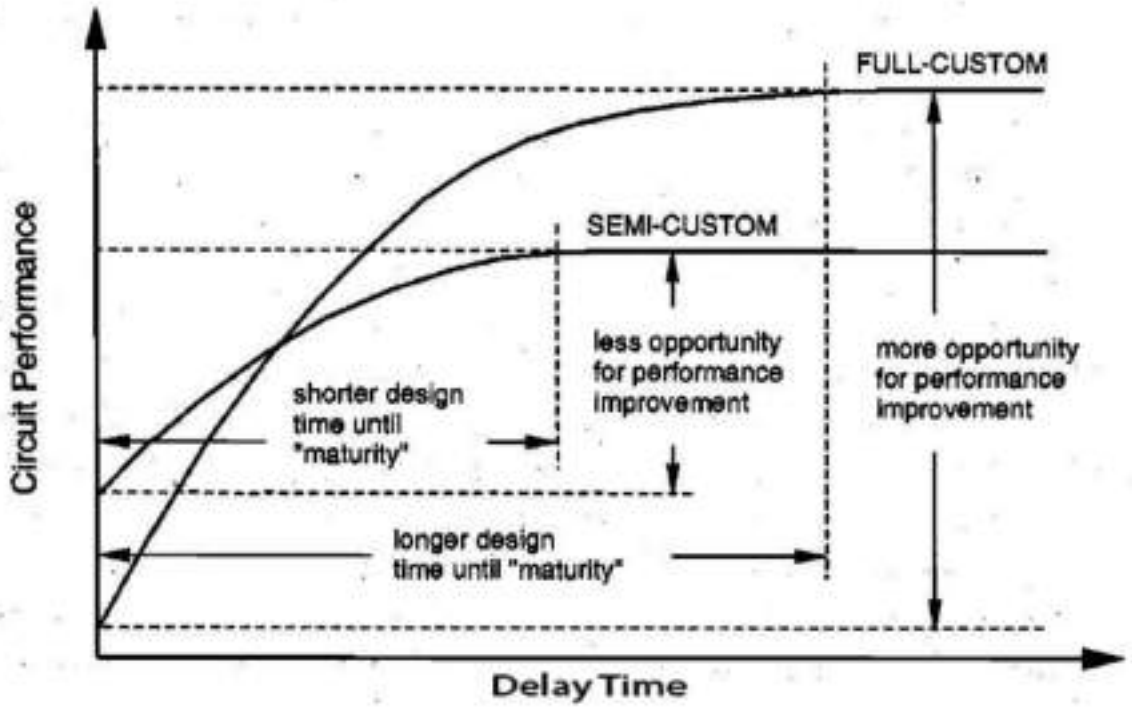


Figure 14.20. **A simplified floorplan of standard-cell-based design.**

❖ FULL CUSTOM DESIGN: -

- Using the full-custom design style where the geometry and the placement of every transistor can be optimized individually.
- This design requires a longer time until design maturity can be reached.
- It flexibility of adjusting almost every aspect of circuit design.
- It allows far more opportunity for circuit performance improvement during the design cycle.
- The final product typically has a high level of performance (e.g. high processing speed, low power dissipation) and the silicon area is relatively small because of better area utilization. But this comes at a larger cost in terms of design time.



❖ **SEMI-CUSTOM DESIGN –**

- In case of a semi-custom design style (such as standard-cell based design or FPGA) will allow a shorter design time until design maturity can be achieved.
- In the early design phase, the circuit performance can be even higher than that of a full-custom design, since some of the components used in semi-custom design are already optimized.
- But the semi-custom design style offers less opportunity for performance improvement over the long run, and the overall performance of the final product will inevitably be less than that of a full-custom design. In addition to the proper choice of a VLSI design style, there are other issues which must be addressed in view of the constantly evolving nature of the VLSI manufacturing technologies
- Approximately every two years, a new generation of technology is introduced, which typically allows for smaller device dimensions and consequently, higher integration density and higher performance.

Unit-2: Fabrication of MOSFET

2.1 Simplified Process Sequence for Fabrication:-

- The simplified process sequence for the fabrication of integrated circuits on a p-type silicon substrate.
- The process starts with the creation of the n-well regions for pMOS transistors, by impurity implantation into the substrate.
- Then, a thick oxide is grown in the regions surrounding the nMOS and pMOS *active regions.*
- The thin gate oxide is subsequently grown on the surface through thermal oxidation.
- These steps are followed by the creation of n+ and p+ regions (source, drain, and channel stop implants) and by final metallization (creation of metal interconnects).

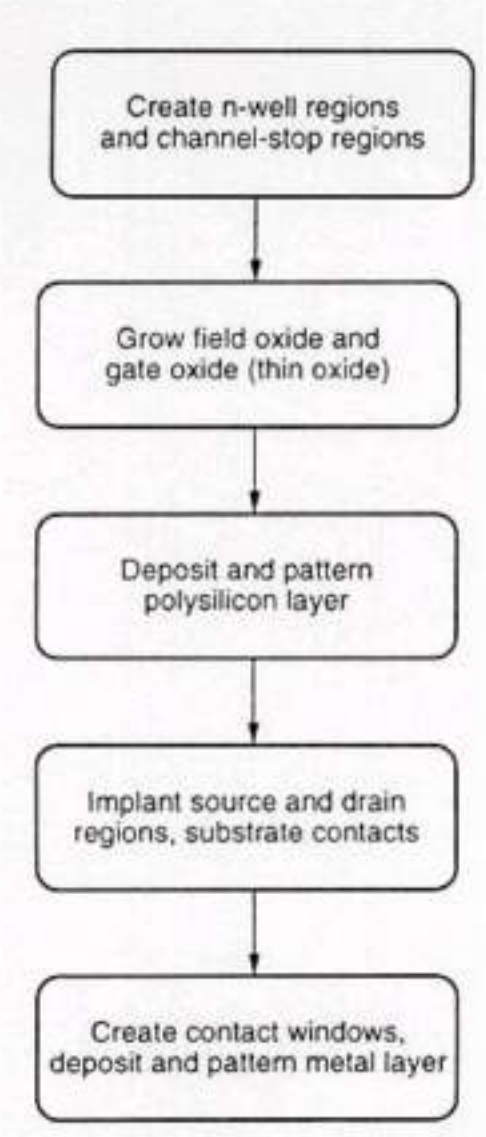
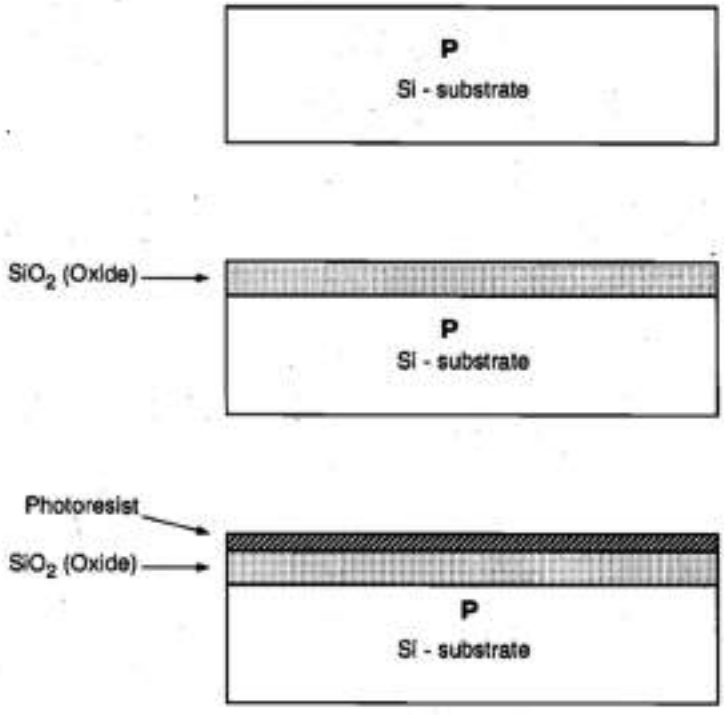


Figure **Simplified process sequence for the fabrication**

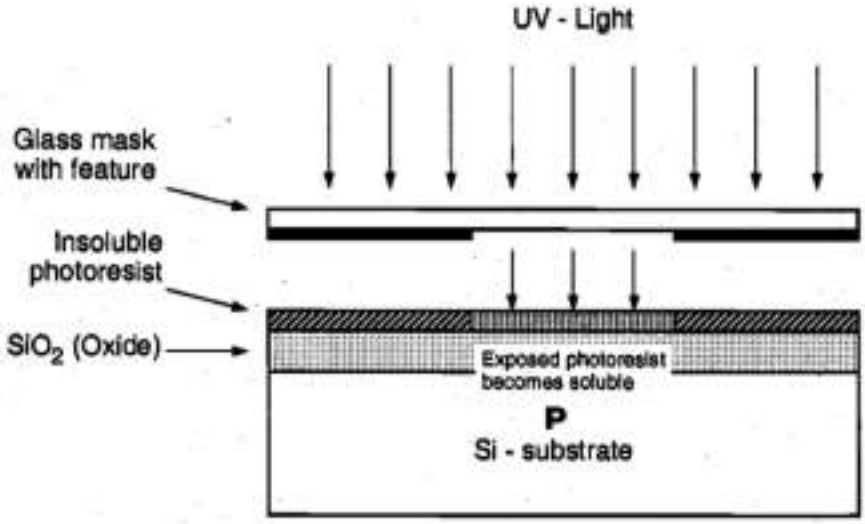
2.2 Basic steps in Fabrication processes Flow

❖ FABRICATION PROCESS:-

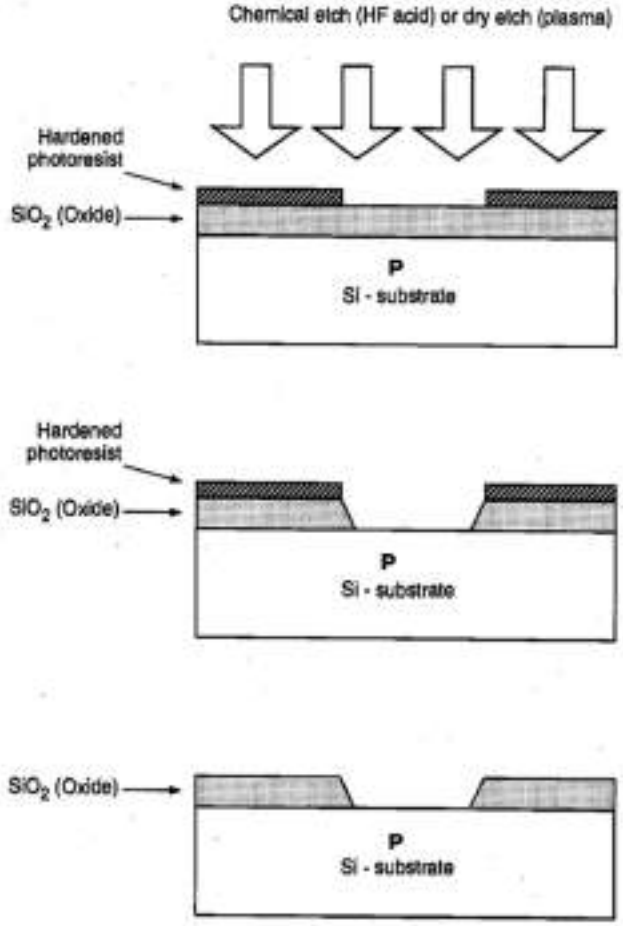
- The process starts with the creation of the n-well regions for pMOS transistors, by impurity implantation into the substrate.
- Then, a thick oxide is grown in the regions surrounding the nMOS and pMOS active regions.
- The thin gate oxide is subsequently grown on the surface through thermal oxidation.
- These steps are followed by the creation of n+ and p+ regions (source, drain, and channel stop implants) and by final metallization (creation of metal interconnects).
- Each processing step requires that certain areas are defined on chip by appropriate masks.
- As a result patterned layers of doped silicon, polysilicon, metal, and insulating silicon dioxide.
- In general, a layer must be patterned before the next layer of material is applied on the chip.
- The process used to transfer a pattern to a layer on the chip is called *lithography.*
- Since each layer has its own distinct patterning requirements, the lithographic sequence must be repeated for every layer, using a different mask
- By the thermal oxidation of the silicon surface, by which an oxide layer of about 1 m thickness, for example, is created on the substrate.
- Then entire oxide surface is then covered with a layer of photo-resist, which is essentially a light-sensitive.



- The photo-resist can be either positive type or negative type material.
- The type of photo-resist which is initially insoluble and becomes soluble after exposure to UV light is called *positive photo-resist.*
- There is another type of photo-resist which is initially soluble and becomes insoluble (hardened) after exposure to UV light, called *negative photo-resist.*

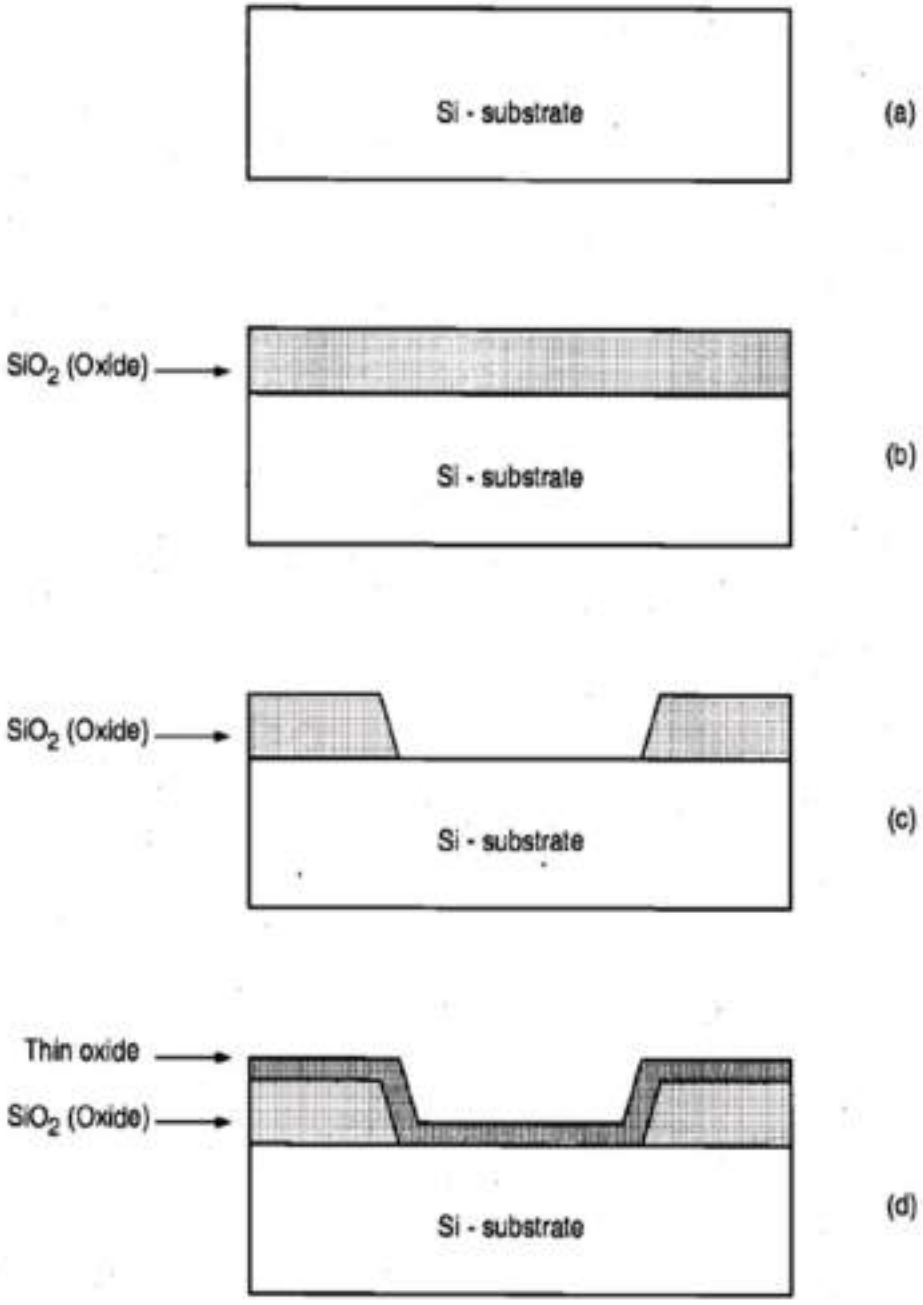


- The areas which are not shielded from the UV light by the opaque mask features become insoluble, whereas the shielded areas can subsequently be etched by a chemical solution or dry etching to form pattern on SiO_2 layer or Si-subtrate.

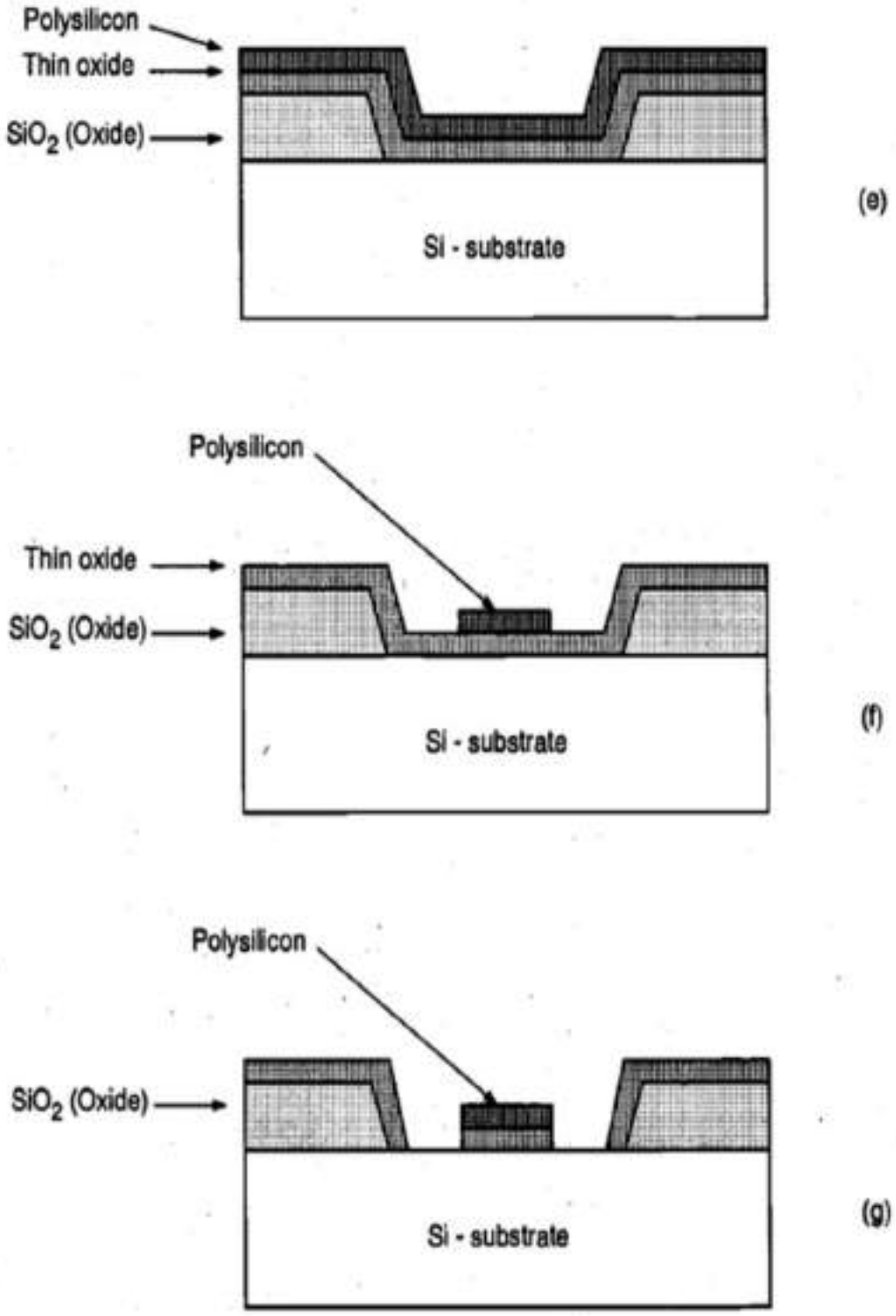


2.3 Fabrication process of nMOS Transistor

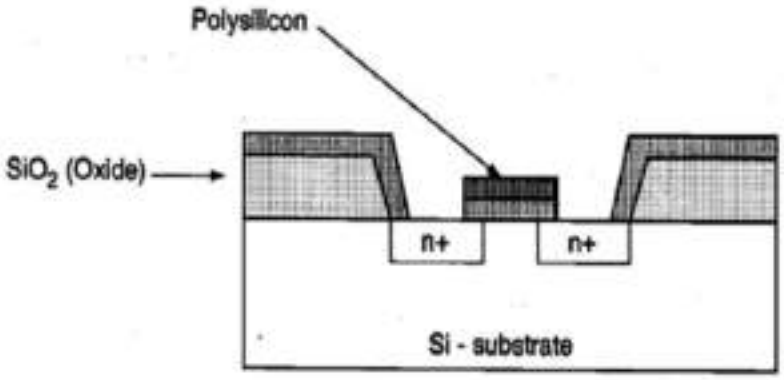
- The process starts with of silicon substrate as shown in figure (a) in which a thick dioxide layer, also called field oxide, is created on the surface (b).
- Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created (Fig. (c)).
- Following this step, the surface is covered with a thin, high-quality oxide layer, which will eventually form the gate oxide of the n- mos transistor.



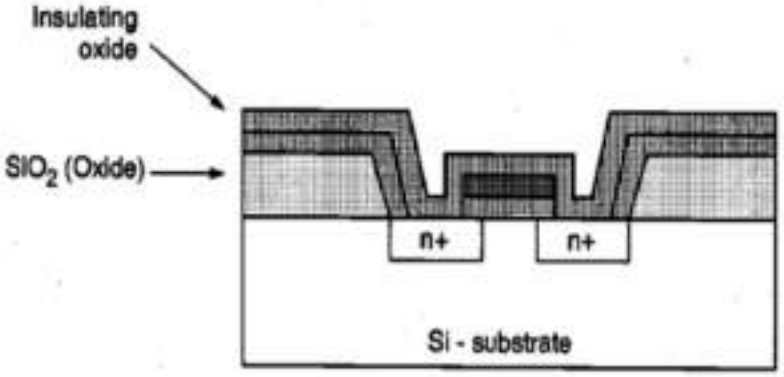
- On top of the thin oxide layer, a layer of polysilicon (polycrystalline silicon) is deposited (Fig. (e)).



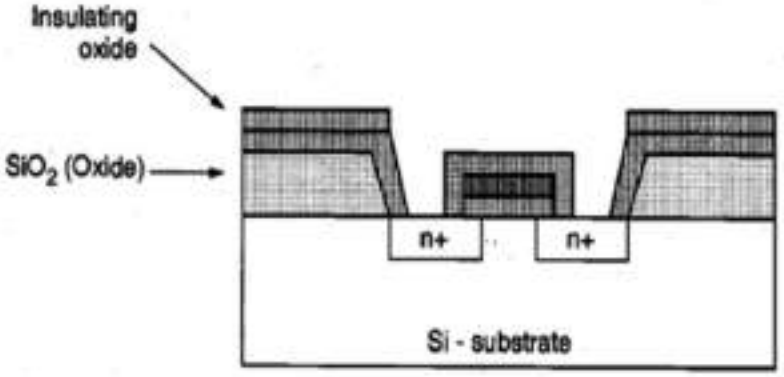
- Polysilicon is used both as gate electrode material for MOS transistors and also as an interconnect medium in silicon integrated circuits.
- After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates (Fig. (f)).
- The thin gate oxide not covered by polysilicon is also etched away, which exposes the bare silicon surface on which the source and drain junctions are to be formed (Fig. (g)).
- The entire silicon surface is then doped with a high concentration of impurities, either through diffusion or ion implantation in this case with donor atoms to produce n-type doping. Figure (h)



(h)



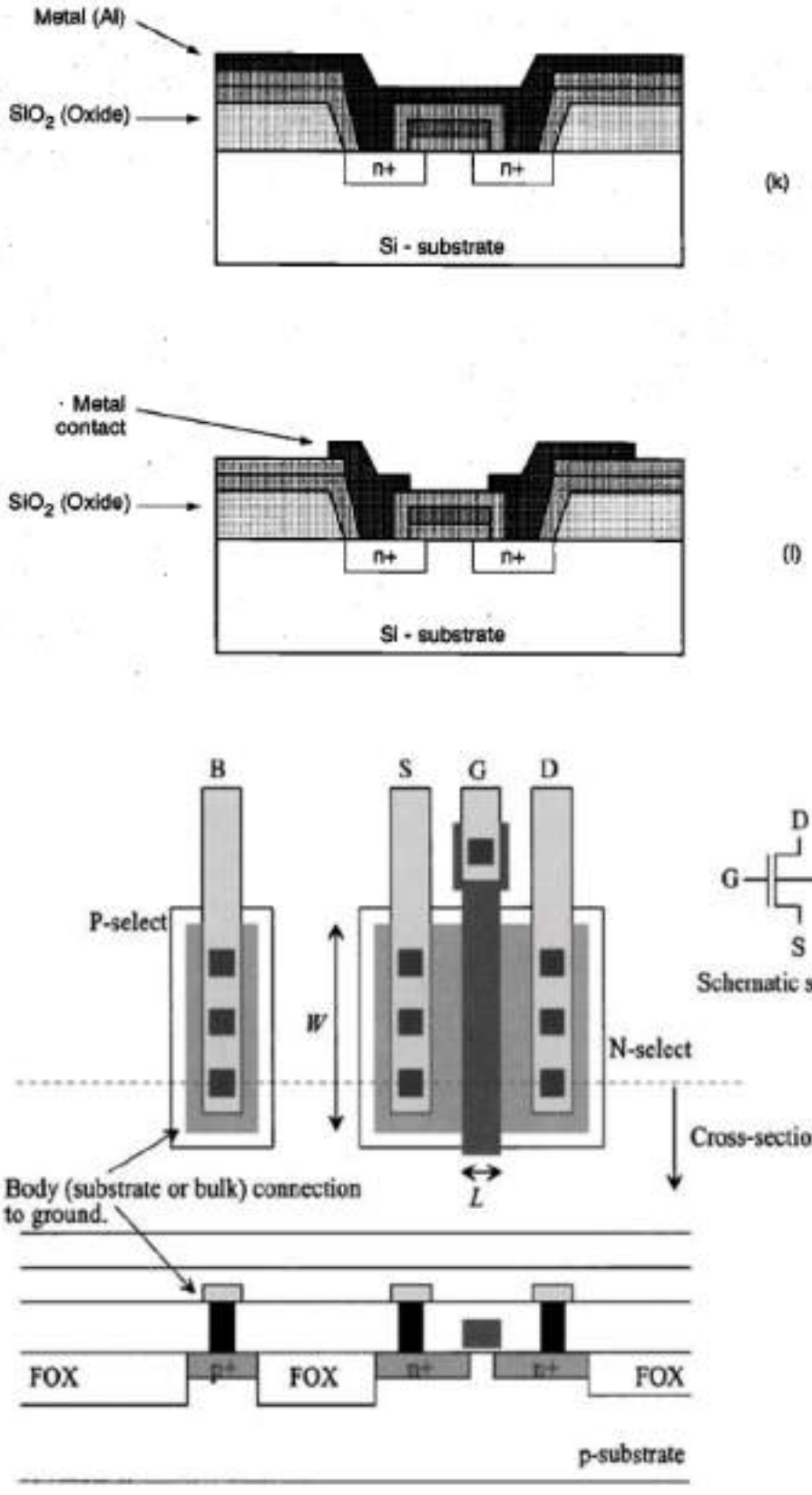
(i)



(j)

- The polysilicon on the surface, reducing its resistivity. Note that the polysilicon gate, which is patterned *before* doping, actually defines the precise location of the channel region and, hence, the location of the source and the drain regions.
- Since this procedure allows very precise positioning of the two regions relative to the gate, it is also called the *self-aligned process*.
- Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide (Fig. (i)).
- Then the insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions (Fig. (j)).
- The surface is covered with evaporated aluminium which will form the interconnects (Fig. (k)).

- Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface (Fig. (1)).



2.4 CMOS n-well Fabrication Process Flow

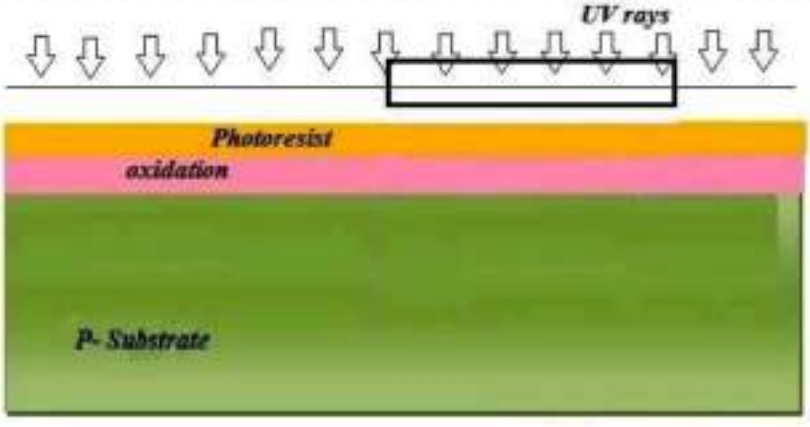
❖ The CMOS n-Well Process:-

Step 1: First we choose a substrate as a base for fabrication. For N- well, a P-type silicon substrate is selected.

Step 2 – Oxidation: The selective diffusion of n-type impurities is accomplished using SiO2 as a barrier which protects portions of the wafer against contamination of the substrate. SiO_2 is laid out by oxidation process done exposing the substrate to high-quality oxygen and hydrogen in an oxidation chamber at approximately 1000^0c

Step 3 – Growing of Photoresist: At this stage to permit the selective etching, the SiO2 layer is subjected to the photolithography process. In this process, the wafer is coated with a uniform film of a photosensitive emulsion.

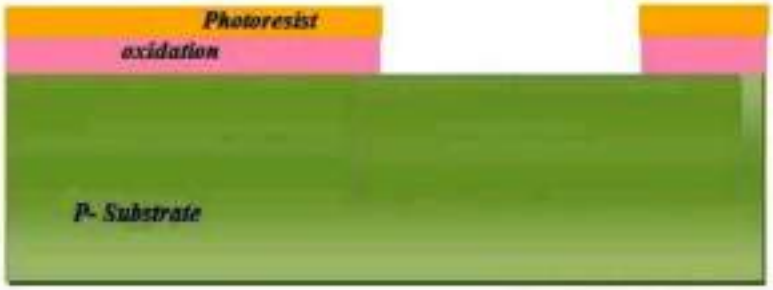
Step 4 – Masking: This step is the continuation of the photolithography process. In this step, a desired pattern of openness is made using a stencil. This stencil is used as a mask over the photoresist.



The substrate is now exposed to **UV rays** the photoresist present under the exposed regions of mask gets polymerized.

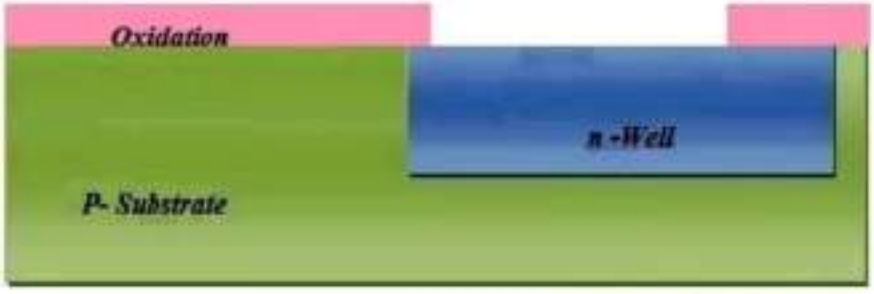
Step 5 – Removal of Unexposed Photoresist: The mask is removed and the unexposed region of photoresist is dissolved by developing wafer using a chemical such as Trichloroethylene.

Step 6 – Etching: The wafer is immersed in an etching solution of hydrofluoric acid, which removes the oxide from the areas through which dopants are to be diffused.



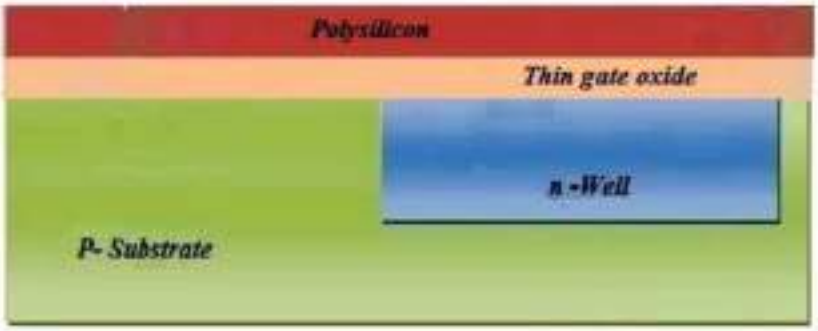
Step 7 – Removal of Whole Photoresist Layer: During the **etching process**, those portions of SiO2 which are protected by the photoresist layer are not affected. The photoresist mask is now stripped off with a chemical solvent (hot H2SO4).

Step 8 – Formation of N-well: The n-type impurities are diffused into the p-type substrate through the exposed region thus forming an N- well.



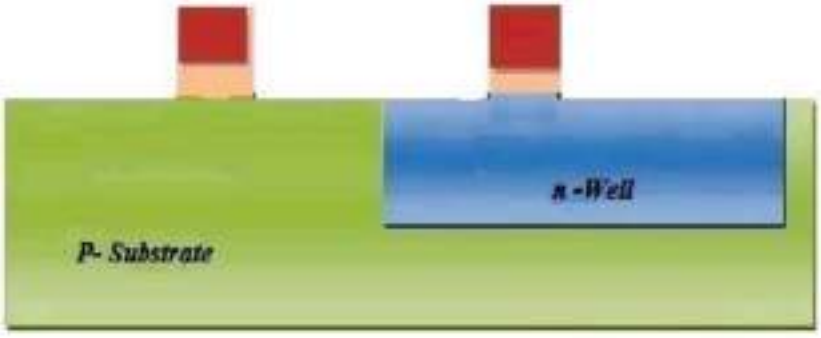
Step 9 – Removal of SiO2: The layer of SiO2 is now removed by using hydrofluoric acid.

Step 10 – Deposition of Polysilicon: The misalignment of the gate of a **CMOS transistor** would lead to the unwanted capacitance which could harm circuit. So to prevent this "Self-aligned gate process" is preferred where gate regions are formed before the formation of source and drain using ion implantation.

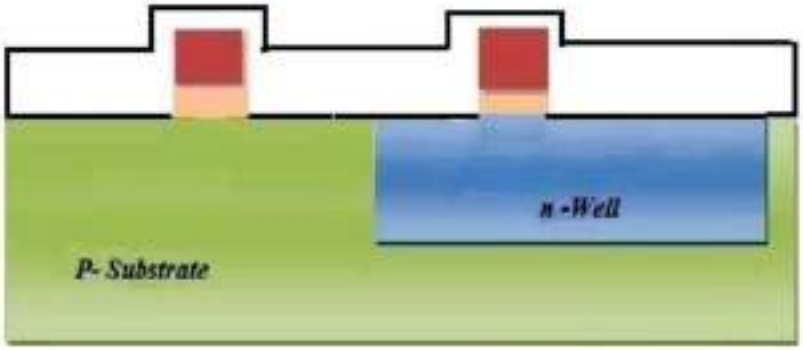


Polysilicon is used for formation of the gate because it can withstand the high temperature greater than 8000^0c when a wafer is subjected to annealing methods for formation of source and drain. Polysilicon is deposited by using **Chemical Deposition Process** over a thin layer of gate oxide. This thin gate oxide under the Polysilicon layer prevents further doping under the gate region.

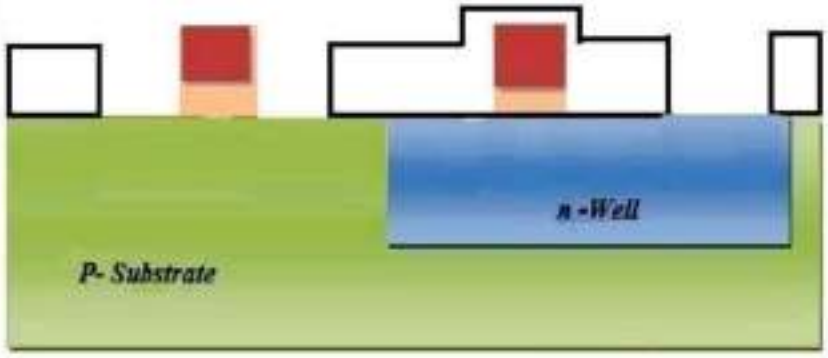
Step 11 – Formation of Gate Region: Except the two regions required for formation of the gate for **NMOS and PMOS transistors** the remaining portion of Polysilicon is stripped off.



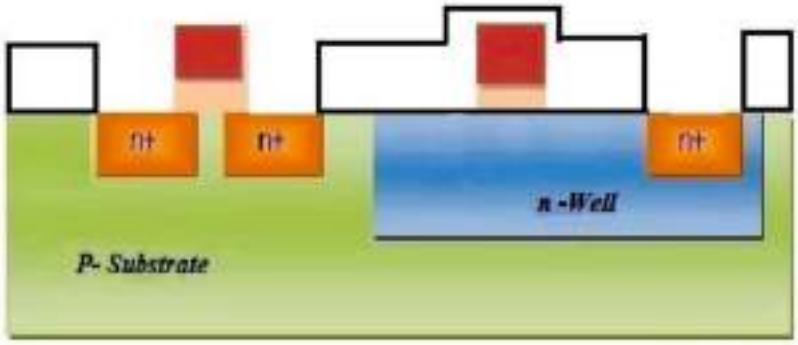
Step 12 – Oxidation Process: An oxidation layer is deposited over the wafer which acts as a shield for further **diffusion and metallization processes**.



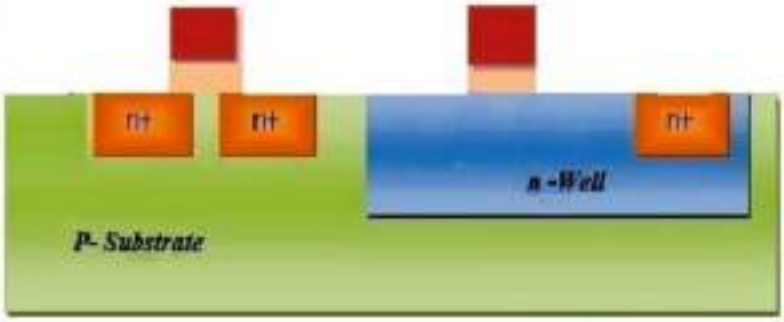
Step 13 – Masking and Diffusion: For making regions for diffusion of n-type impurities using masking process small gaps are made.



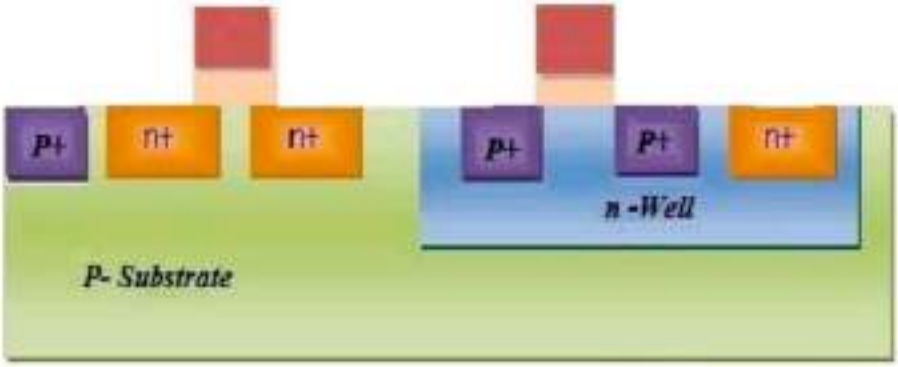
Using diffusion process three n+ regions are developed for the formation of terminals of NMOS.



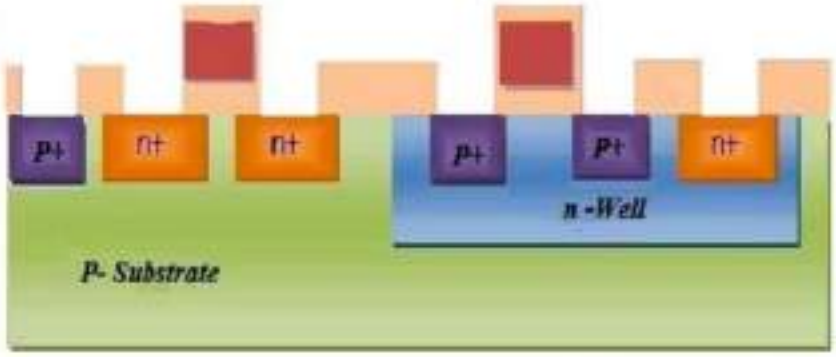
Step 14 – Removal of Oxide: The oxide layer is stripped off.



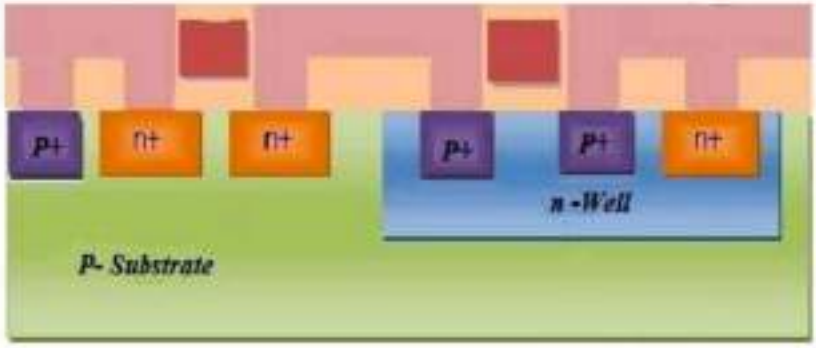
Step 15 – P-type Diffusion: Similar to the n-type diffusion for forming the terminals of PMOS p-type diffusion are carried out.



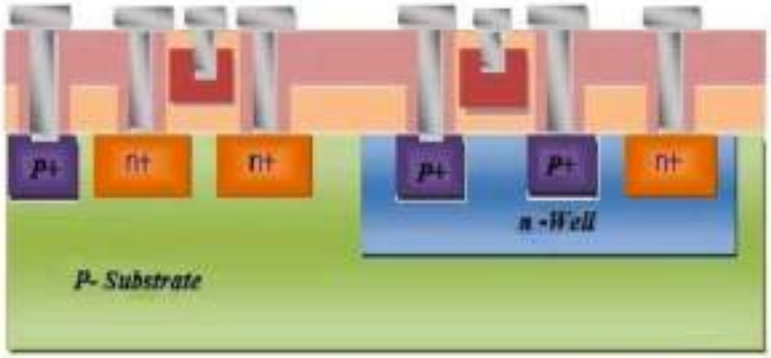
Step 16 – Laying of Thick Field oxide: Before forming the metal terminals a thick field oxide is laid out to form a protective layer for the regions of the wafer where no terminals are required.



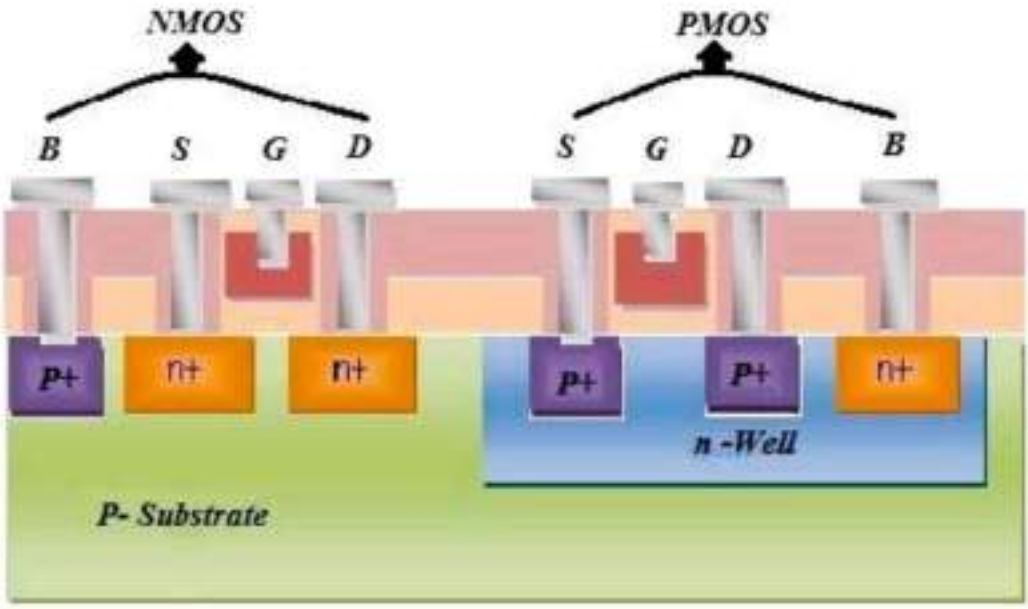
Step 17 – Metallization: This step is used for the formation of metal terminals which can provide interconnections. Aluminum is spread on the whole wafer.



Step 18 – Removal of Excess Metal: The excess metal is removed from the wafer.
Step 19 – Formation of Terminals: In the gaps formed after removal of excess metal terminals are formed for the interconnections.



Step 20 – Assigning the Terminal Names: Names are assigned to the terminals of **NMOS and PMOS transistors**.



2.6 CMOS Fabrication process by P-well on n-substrate

- ❖ CMOS fabrication can be accomplished using either of the three technologies:
  - N-well/P-well technologies
  - Twin well technology
  - Silicon On Insulator (SOI)

- ➢ The **N-well / P-well technology**:- where n-type diffusion is done over a p-type substrate or p-type diffusion is done over n-type substrate respectively.
- ➢ The **Twin well technology**:- where **NMOS and PMOS transistor** are developed over the wafer by simultaneous diffusion over an epitaxial growth base, rather than a substrate.
- ➢ The **silicon On Insulator** process,:-where rather than using silicon as the substrate an insulator material is used to improve speed and latch-up susceptibility.

❖ N- well/ P- well Technology

- CMOS can be obtained by integrating both **NMOS and PMOS transistors** over the same silicon wafer. In N–well technology an n-type well is diffused on a p-type substrate whereas in P- well it is vice- verse.

2.7 Layout Design rules

❖ **Layout Design Rules :-** The physical mask layout of any circuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, which are generally called layout design rules.

- The design rules are usually described in two ways:

(i) Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers, or,

(ii) Lambda rules, which specify the layout constraints in terms of a single parameter () and thus allow linear, proportional scaling of all geometrical constraints.

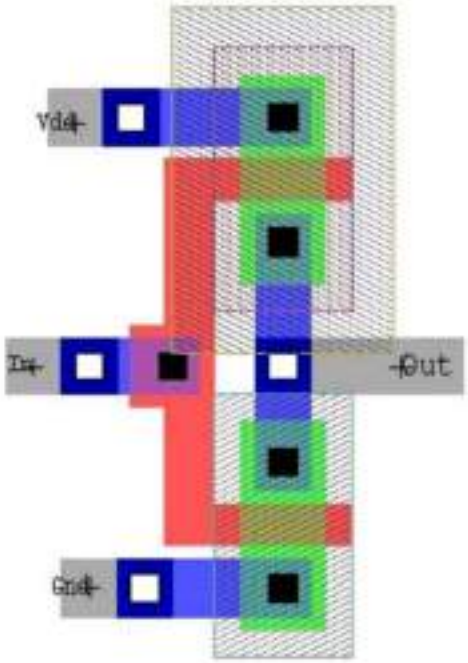


Figure :CMOS Inverter Layout Figure

2.8 Stick Diagrams of CMOS inverter

❖ Stick Diagrams

- It is the Stick and colour representation of the n- mos and c-mos circuit presentation and constructed as per the given rules.
- In this, the designer draws a freehand sketch of a layout, using colored lines to represent the various process layers such as diffusion, metal and polysilicon .
- Where polysilicon crosses diffusion, transistors are created and where metal wires join diffusion or polysilicon, contacts are formed.
- This notation indicates only the relative positioning of the various design components.
- The absolute coordinates of these elements are determined automatically by the editor using a compactor.
- The compactor translates the design rules into a set of constraints on the component positions, and solve a constrained optimization problem that attempts to minimize the area or cost function.
- The **advantage** of this symbolic approach is that the designer does not have to worry about design rules, because the compactor ensures that the final layout is physically correct.
- The **disadvantage** of the symbolic approach is that the outcome of the compaction phase is often unpredictable.

- The resulting layout can be less dense than what is obtained with the manual approach.

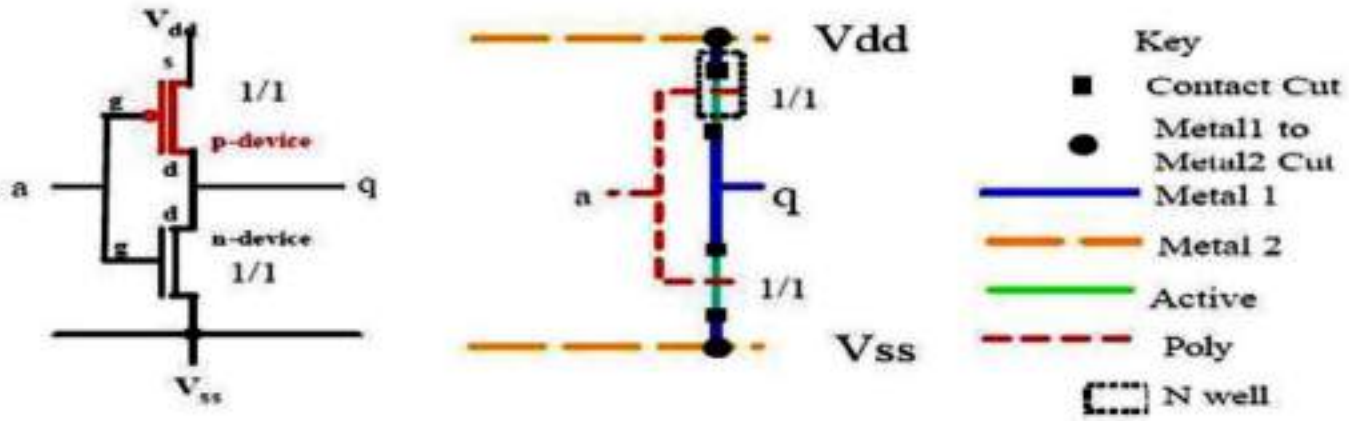


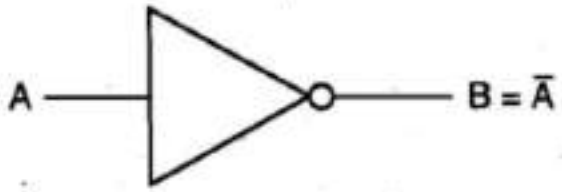
Figure : Stick Diagram of a CMOS Inverter

Unit-3: MOS Inverter

3.1 Basic nMOS inverters

❖ Inverter

- Inverter is the basic building block of all digital design.
- The logic symbol and the truth table of the ideal inverter are shown in Fig. 1.



Symbol

A	B
0	1
1	0

Truth Table

Fig.1 Logic symbol and truth table of the inverter

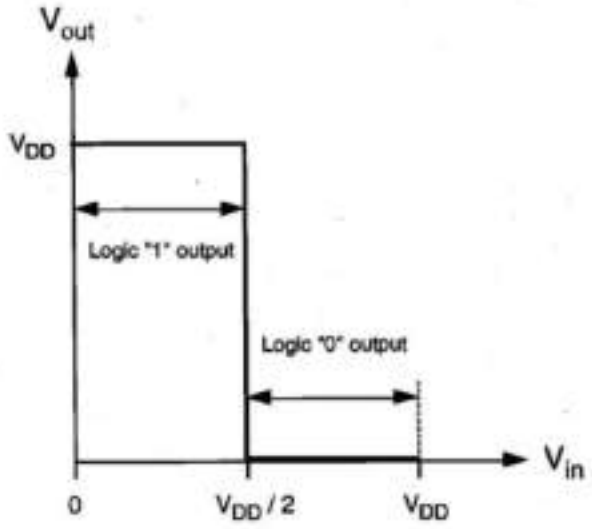
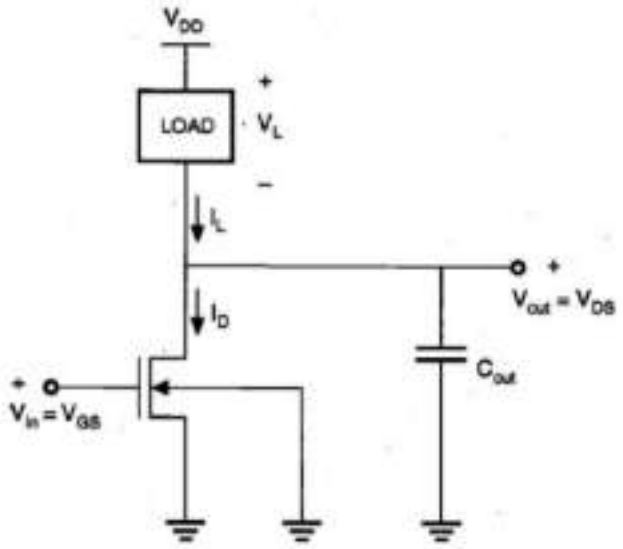


Fig Voltage transfer characteristic (VTC) of the ideal inverter.

- Here the input variable is A and the output variable is B using positive logic the logic value of "1" can be represented by a high voltage of VDD, and the logic value of "0" can be represented by a low voltage of 0.

- The voltage Vth is called the inverter threshold voltage. For any input voltage between 0 and Vth= VDD/2 , the output voltage is equal to VDD (logic" 1).
- The output switches from VDD to 0 when the input is equal to Vth.
- For any input voltage between Vth and VDD, the output voltage assumes a value of 0 (logic "0").
- Thus, an input voltage $0 < Vi. < V_{th}$ is interpreted by this ideal inverter as a logic "0."
- While an input voltage Vth <Vin < VDD s interpreted as a logic " 1."

❖ n-MOS inverter



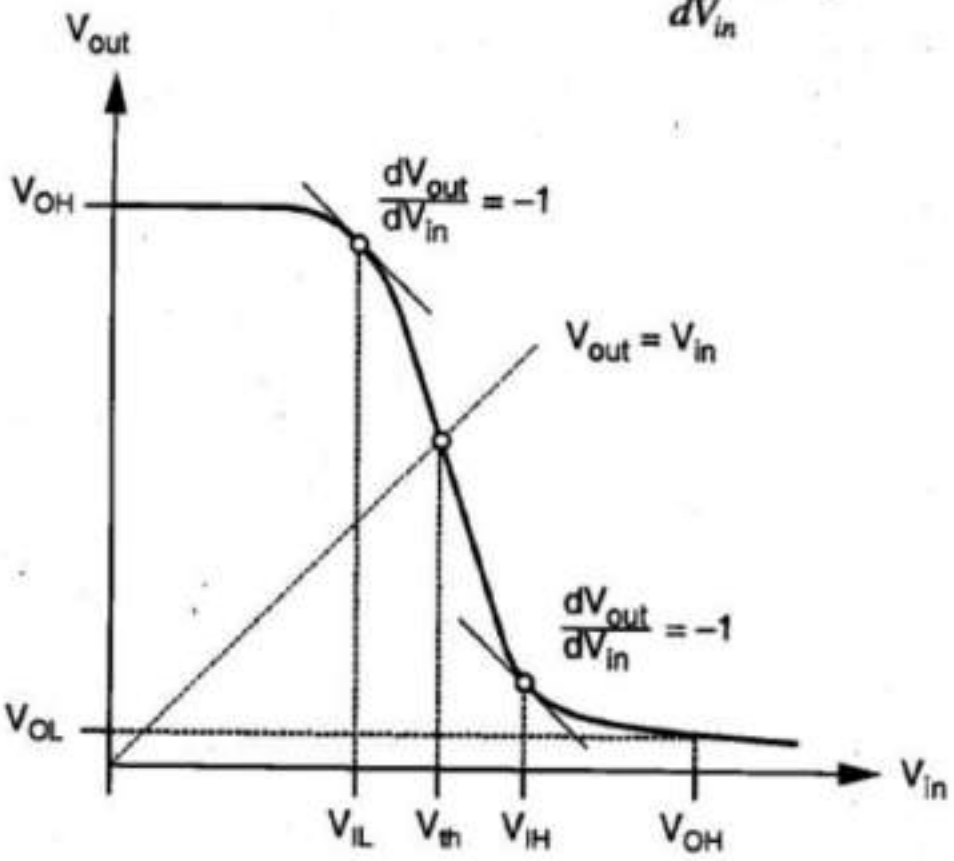
- In this case the n-mos is known as driver transistor and V_{GS} is the input voltage.
- V_{DS} is the output voltage
- Substrate is grounded.
- In case of load we use register n-mos depletion type or enhancemet type MOSFET.
- When the input of driver transistor is less than threshold voltage that is V_{in} is less than V_{th} **($V_{in} < V_{th}$)** the driver transistor is in cut- off mode and does not conduct any current. So the output voltage V_{DD} when the input voltage is greater than V_{th} driver transistor start conducting and n-mos goes into saturation region and the output is zero.

❖ Voltage Transfer Characteristics :-

- For very low input voltage levels, the output voltage V is equal to the high value of *VOH (output high voltage).*

- In this case, the driver nMOS transistor is in cut-off, and hence, does not conduct any current. So that the output voltage is high as the input voltage increase above threshold then the driver transistor strat conducting eventually the output voltage decrease. It decrease gradually and with a finite slope = -1. i.e.,

$$\frac{dV_{out}}{dV_{in}} = -1$$



V_{OH}: Maximum output voltage when the output level is logic " 1"

V_{OL} Minimum output voltage when the output level is logic "0"

V_{IL}: Maximum input voltage which can be interpreted as logic "0"

V_{IH}: Minimum input voltage which can be interpreted as logic " 1"

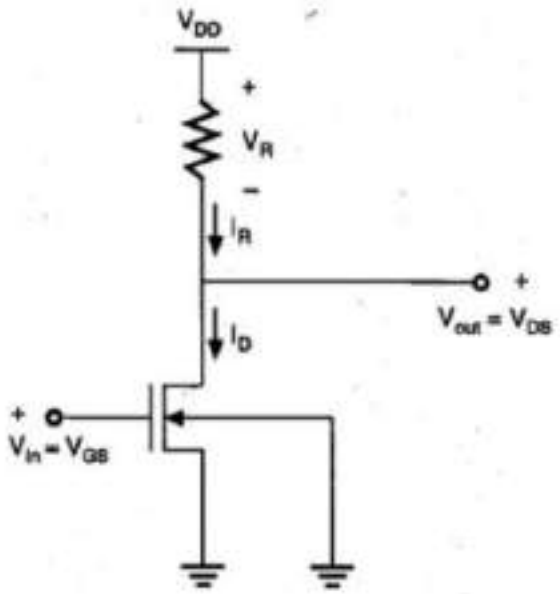
3.2 Working of Resistive-load Inverter

❖ **Resistive-Load Inverter**

- ❖ The basic structure of the resistive-load inverter circuit is shown in Fig..
- ❖ Here n-mos is acts as a diver transistor and load is simple register. The power supply voltage of this circuit is VDD.
- ❖ As we consider DC steady state operation so that

$$I_r = I_D$$

- ❖ As the substrate terminals of the driver transistor are both connected to the ground; hence, VSB = 0.



- As the input voltage is increased beyond V_{th}., the driver transistor starts conducting a nonzero drain current. Note that the driver MOSFET is initially in saturation, since its drain-to-source voltage. (VDs = V_{out}) is larger than (V_{in} – V_{GS}.). Thus,

$$I_R = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

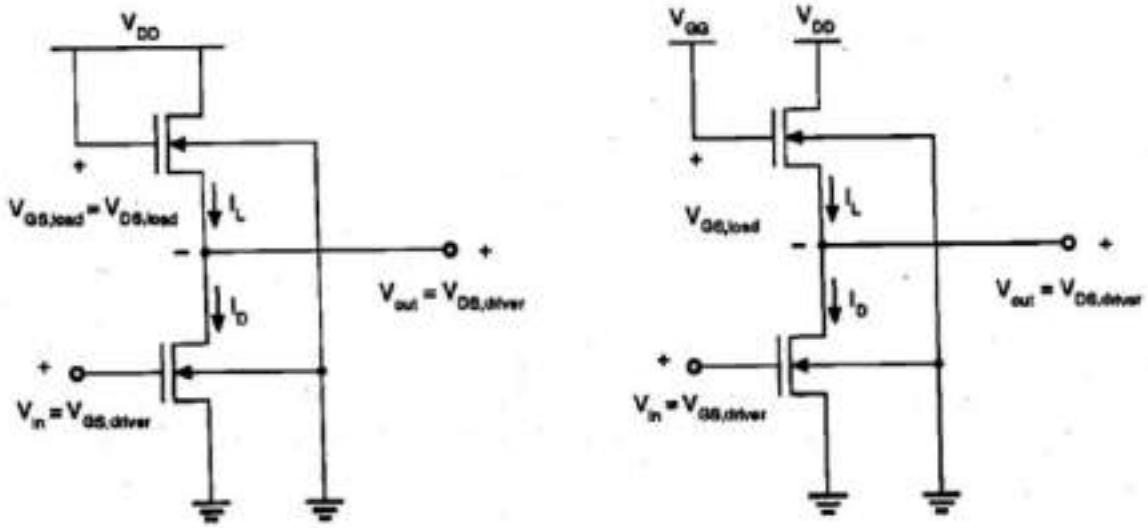
3.3 Inverter with n-Type MOSFET Load – Enhancement Load, Depletion n-MOS inverter

Inverter with n-Type MOSFET

- Resistive-load is not a suitable for most digital VLSI system applications, primarily because of the large area occupied by the load resistor. So by using an nMOS transistor as the *active load* device, instead of the linear load resistor.The main advantage of using a MOSFET as the load device is that the silicon area occupied by the transistor is usually smaller than that occupied by a comparable resistive load.
- By using n-mos active load rather than resistive passive load the over all performance is improved.

❖ Enhancement Load n-mos inverter:-

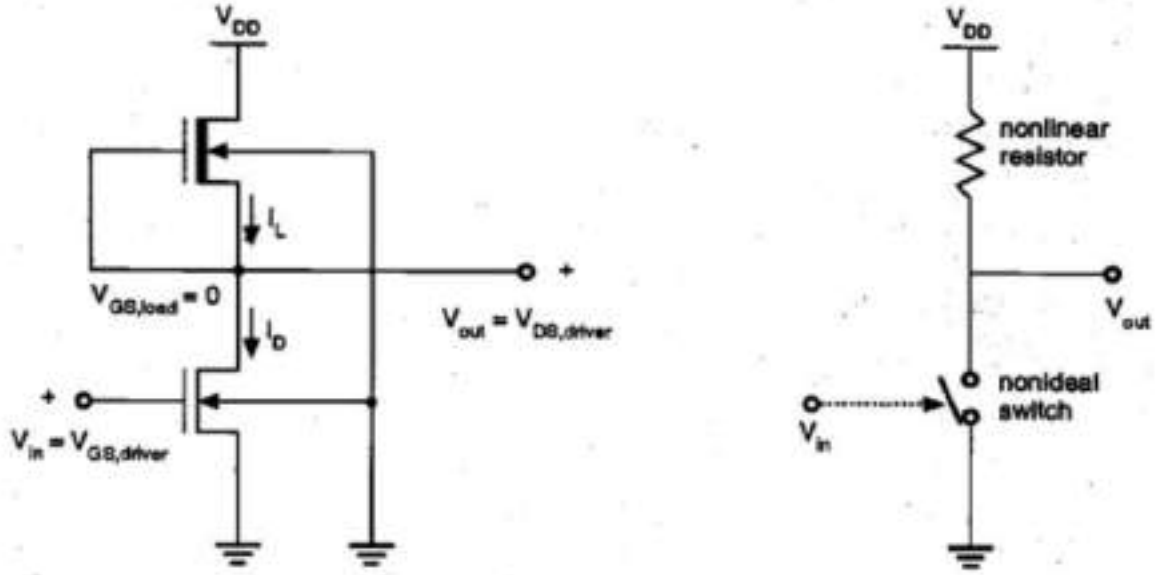
- ❖ The load transistor can be operated either in the saturation region or in the linear region depending on the bias voltage applied to its gate terminal.



- ❖ Figure show the saturated enhancement load inverter it requires single voltage supply and simple fabrication process. So V_{OH} is limited $V_{DD} - V_{TH.}$

❖ Depletion n-MOS inverter:-

- ❖ In this case the gate and source terminal of the load is connect. So the $V_{GC} = 0$. So the threshold volatage of the load is negative.
- ❖ There are load device has always a condition channel regardless of input and output.

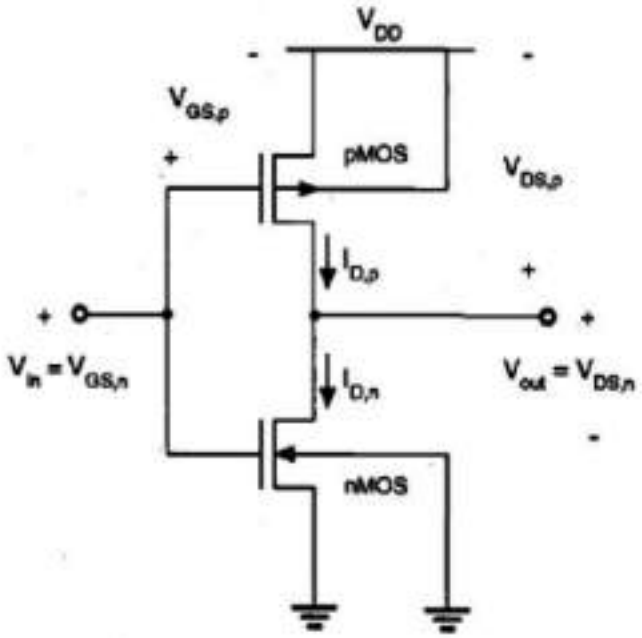


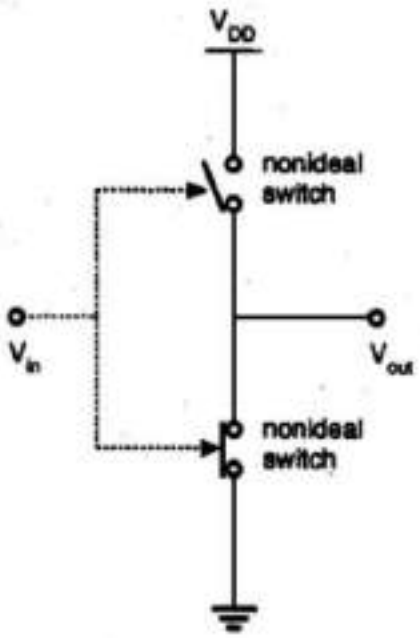
- ❖ The advantage of depletion load inverter are:-
  - Sharp V_{TC}(Voltage transfer characteristics)
  - Better noise margin
  - Single power supply and smaller overall layout area.

3.4 CMOS inverter – circuit operation and characteristics and interconnect effects: Delay time definitions

❖ CMOS Inverter

- C – mos inverter consists of an enhancement-type nMOS transistor and an enhancement-type pMOS transistor.
- The source of PMOS and its substrate are connected to V_{DD} and the source, substrate of n-mos are connected to the ground.
- The drain of both p-mos and n-mos are shorted from where the output is taken.





- The CMOS is operated push-pull for high input, the nMOS transistor drives (pulls down) the output node while the pMOS transistor acts as the load, and for low input the pMOS transistor drives (pulls up) the output node while the nMOS transistor acts as the load. So considering CMOS at a time one transistor is "on" and other is "off".

❖ **Operating region of p-mos and n-mos transistor:-**

- In this curve C-MOS inverter VTC is super imposed operating region on the n-mos and p-mos.

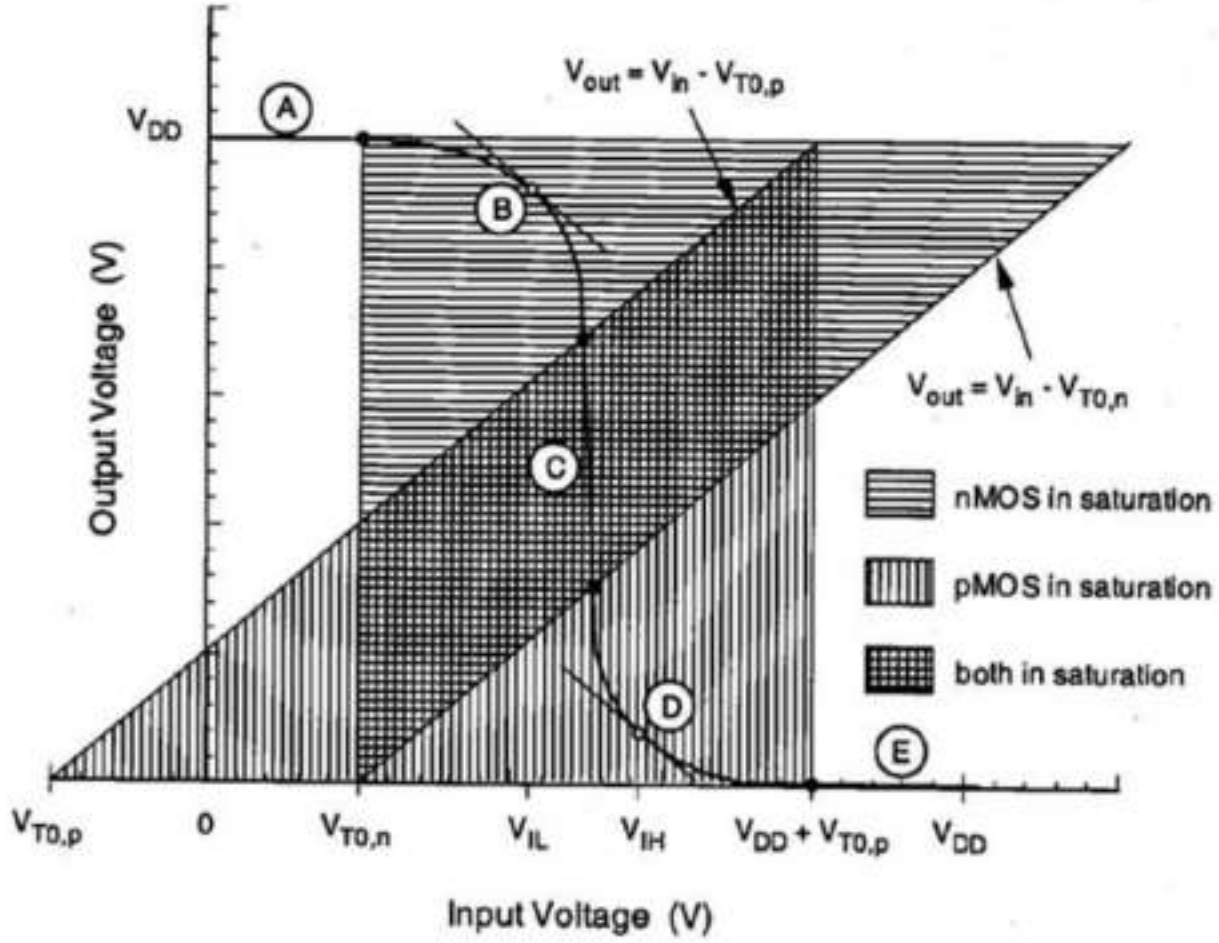


Fig Operating regions of the nMOS and the pMOS transistors

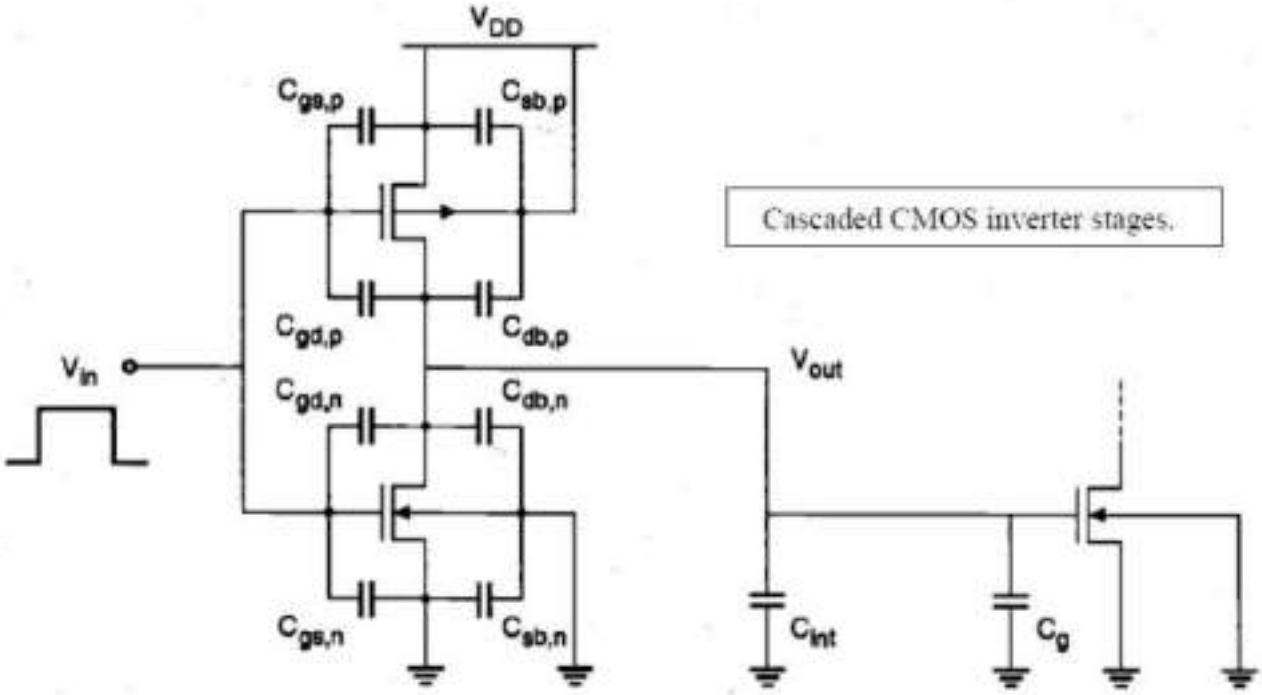
❖ The table below lists these regions and the corresponding critical input and output voltage levels.

Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$>(V_{DD} + V_{T0,p})$	V_{OL}	linear	cut-off

❖ Cascaded CMOS inverter stages

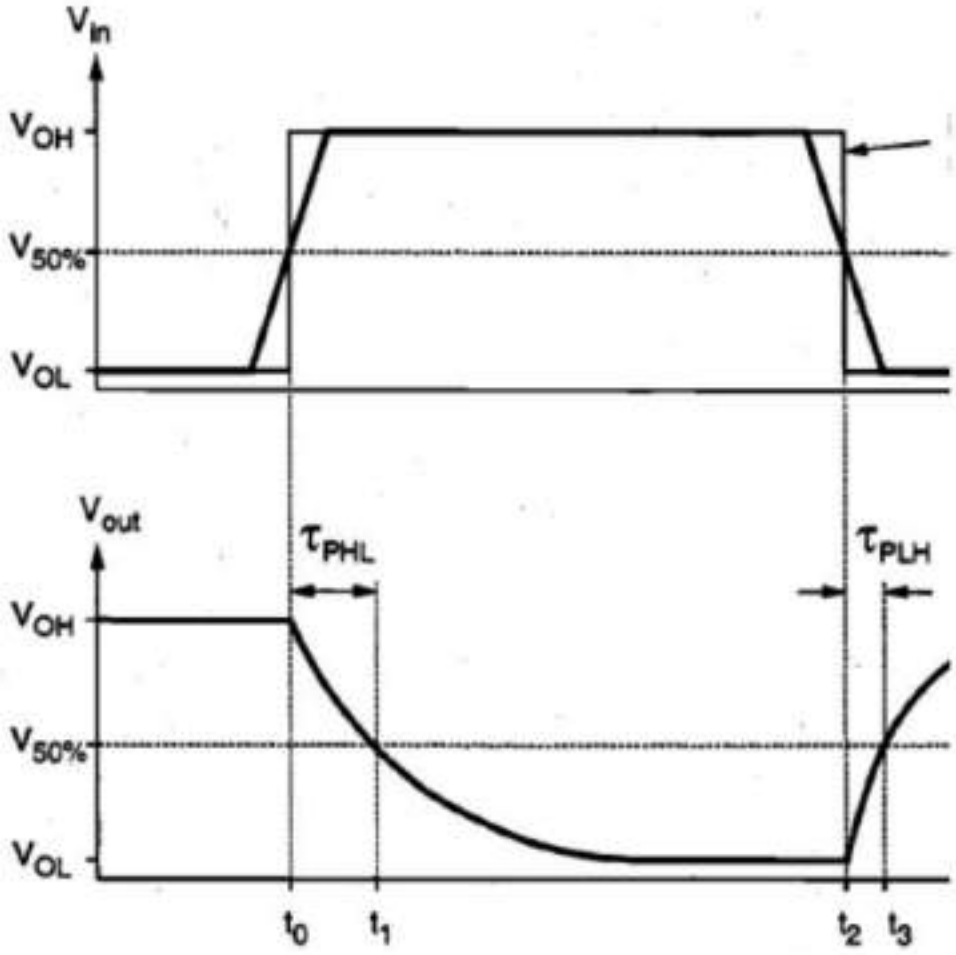
- The parasitic capacitance associated with MOSFET
- C_{gd}, C_{gs} = gate overlap with diffusion.
- C_{db}, C_{sb} = voltage dependent junction capacitance.
- C_g = Thin oxide capacitance over the gate.
- C_{int} = Lumped inter connect capacitance.

$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{int} + C_g$$



Cascaded CMOS inverter stages.

❖ **Input and output voltage waveforms of a typical inverter:**



τ_{PHL} and τ_{PLH} - Propagation delay time

τ_{PHL} - propagation delay during high to low

τ_{PLH} - propagation delay during low to high

- τ_{PHL} – It is the time delay between the $V_{50\%}$-transition of the rising input voltage and the V_{50} -transition of *the falling* output voltage.
- τ_{PLH} – It is defined as the time delay between the V_{50} -transition of *the falling* input voltage and the $V_{50\%}$-transition of the *rising* output voltage.

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OL} + V_{OH})$$

$$\tau_{PHL} = t_1 - t_0$$

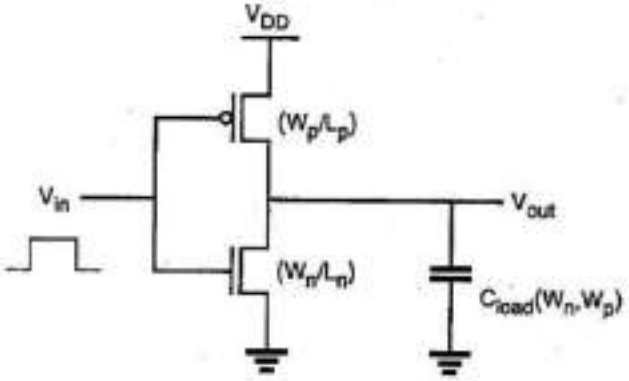
$$\tau_{PLH} = t_3 - t_2$$

➢ The average propagation delay τP of the inverter characterizes the average time required for the input signal to propagate through the inverter.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

3.5 CMOS Inventor design with delay constraints – Two sample mask lay out for p-type substrate.

- **Invertor design with delay constraints.**
  - The propagation delay equations on chart 4-5 can be rearranged to solve for W/L.
  - After determining the desired W/L values, we can obtain the device widths W based on the technology minimum design device lengths L
  - Other constraints such as rise time/fall time or rise/fall symmetry may also need to be considered in addition to rise and fall delay.



$$\left(\frac{W_n}{L_n}\right)=\frac{C_{load}}{\tau^*_{PHL}\,\mu_n\,C_{ox}\left(V_{DD}-V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{DD}-V_{T,n}}+\ln\left(\frac{4\left(V_{DD}-V_{T,n}\right)}{V_{DD}}-1\right)\right]$$

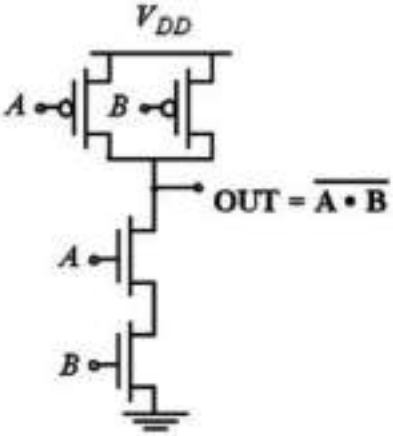
$$\left(\frac{W_p}{L_p}\right)=\frac{C_{load}}{\tau^*_{PLH}\,\mu_p\,C_{ox}\left(V_{DD}-\left|V_{T,p}\right|\right)}\left[\frac{2\left|V_{T,p}\right|}{V_{DD}-\left|V_{T,p}\right|}+\ln\left(\frac{4\left(V_{DD}-\left|V_{T,p}\right|\right)}{V_{DD}}-1\right)\right]$$

Unit-4: Static Combinational, Sequential, Dynamics logic circuits & Memories

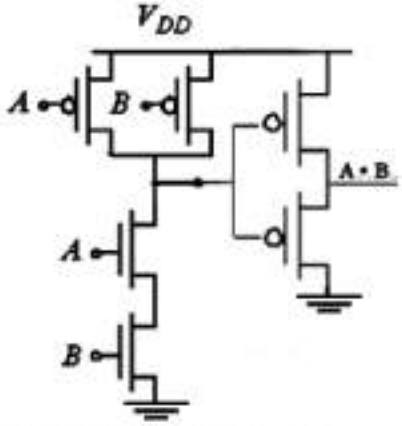
4.1 Define Static Combinational logic ,working of Static CMOS logic circuits (Two-input NAND Gate)

- **Static Logic:-**
  - Static CMOS logic is a circuit design technique where the output is always strongly driven due to it always being connected to either V_{CC} or ground.
  - A static C-MOS circuit consist of two networks.
    - **I.** Pull up network – A set of PMOS transistor connected in between V_{DD} and output line.
    - **II.** Pull down network – A set off n-MOS transistor connected between ground and output line.

AND Gate Using CMOS:-



2 input NAND gate (Static Logic)



2 input AND gate (Static Logic)

- **Circuit Description:-**
  - This applet demonstrates the static two-input NAND and AND gates in CMOS technology.
  - The two-input NAND2 gate shown on the left is built from four transistors. The series-connection of the two n-channel transistors between GND and the gate-output ensures that the gate-output is only driven low (logical 0) when both gate inputs A or B are high (logical 1). The complementary parallel connection of the two transistors between VCC and gate-output means that the gate-output is driven high (logical 1) when one or both gate inputs are low (logical 0). The net result is the logical NAND function:

NAND2

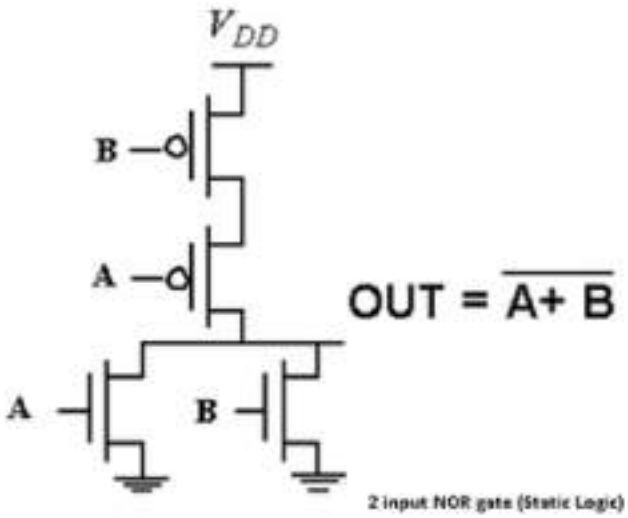
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

AND2

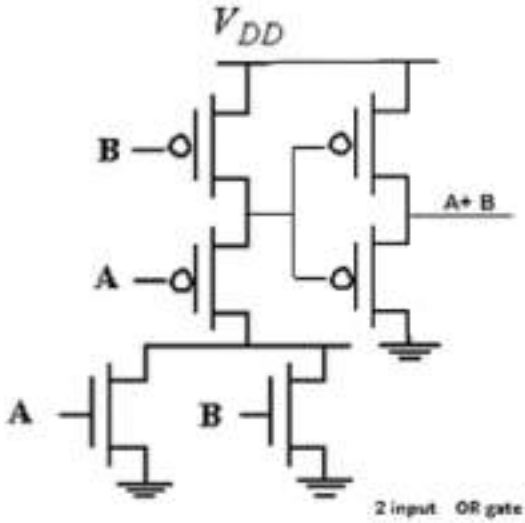
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

  - As shown on the right, the corresponding AND gate is constructed from the NAND followed by a standard static inverter.

OR Gate Using CMOS:-



2 input NOR gate (Static Logic)



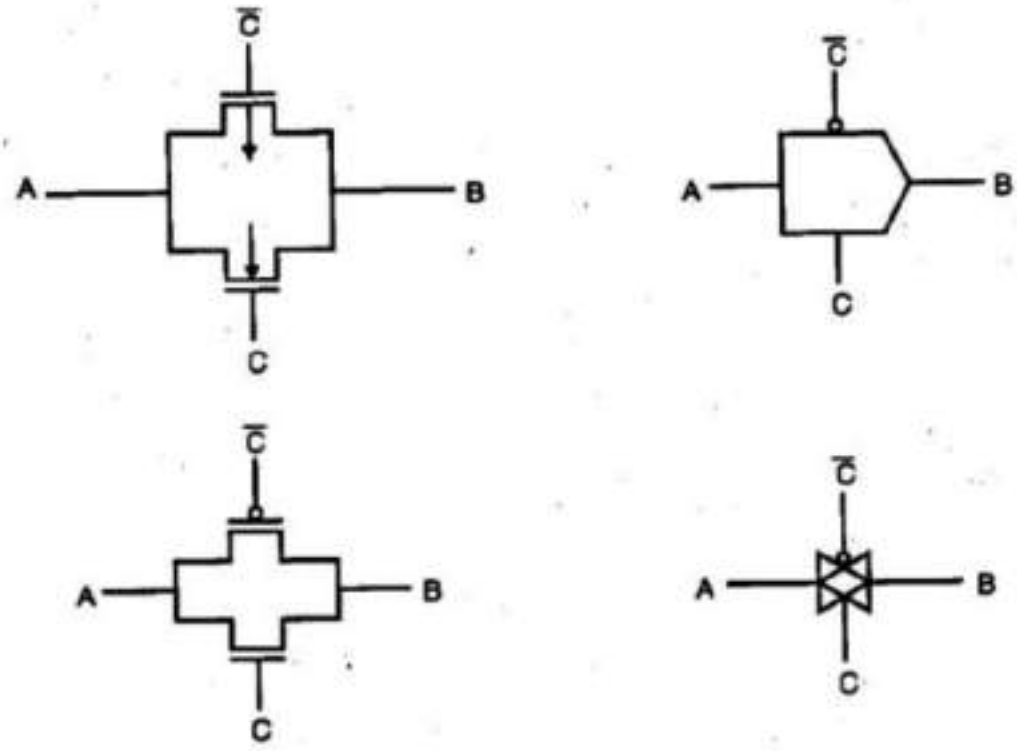
2 input OR gate (Static Logic)

- **Circuit Description**
  - This applet demonstrates the static two-input NOR and OR gates in CMOS technology.
  - The two-input NOR2 gate shown on the left is built from four transistors. The parallel connection of the two n-channel transistors between GND and the gate-output ensures that the gate-output is driven low (logical 0) when either gate input A or B is high (logical 1). The complementary series-connection of the two transistors between VCC and gate-output means that the gate-output is driven high (logical 1) when both gate inputs are low (logical 0). The net result is the logical NOR function:

NOR2			OR2		
A	B	Y	A	B	Z
0	0	1	0	0	0
0	1	0	0	1	1
1	0	0	1	0	1
1	1	0	1	1	1

  - As shown on the right, the corresponding OR gate is constructed from the NOR2 followed by a standard static inverter.

- Complementary pass transistor logic:-
  - It is a logic circuit which use the transmission gate as the basic building blocks.
  - CMOS transmission gate consists of one VnMOS and one pMOS transistor, connected in parallel.
  - The CMOS TG operates as a bidirectional switch between the nodes A and B which is controlled by signal C.
  - If the control signal C is logic-high, i.e., equal to *VDD*, then both transistors are turned on and provide a low-resistance current path between the nodes A and B.



- If, on the other hand, the control signal C is low, then both transistors will be off, and the path between the nodes A and B will be an open circuit. This condition is also called the high-impedance

➢ **Dynamic Logic:-**

- It is a design methodology particularly used in mos technology
- Dynamic logic circuit are usually static logic and also required less surface area.
- In case of dynamic logic a clock signal is used to evaluate the combinational logic.
- The operation of dynamic logic gates depends on the temporary storage of charge in parasitic node capacitance.
- Dynamic logic circuit required periodic clock signal in order to control the charge replacing.

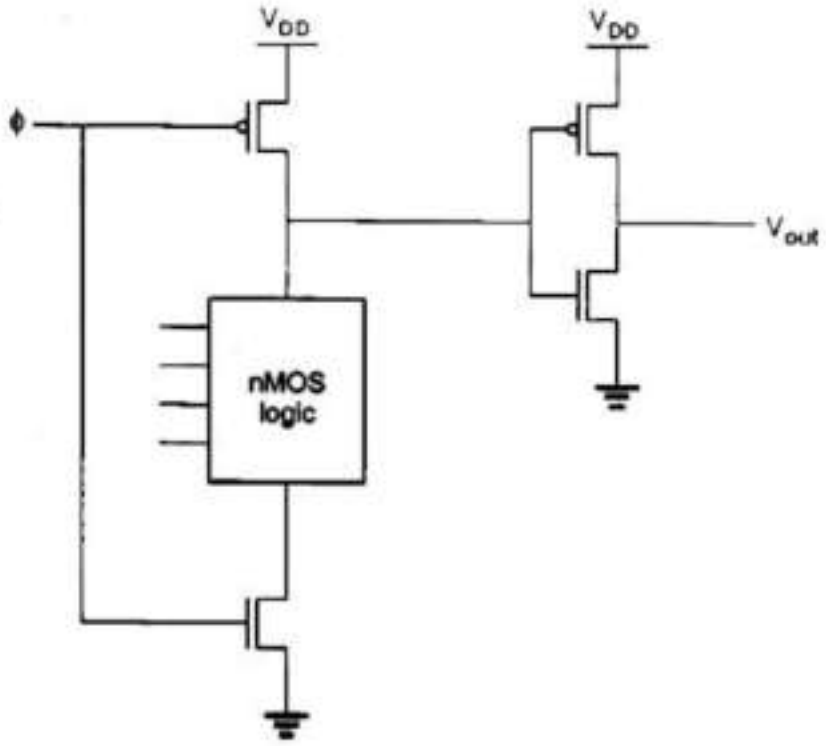
➢ **Difference between static and dynamic logic:-**

Static Logic	Dynamic Logic
It does not required a clock	It operates on clock
This logic is used for low performance digital implementation.	It use for high performance digital implementation.

Static cmos circuit uses complementary nmos pull down and pmos pull up network to implement logic gates.	Dynamic logic uses clocked pmos pull up network. The function of dynamic logic canbe achieve by two mode precharge and evaluate.
The number of transistor required = **2XN**	The number of transistor required = **N+2**
Slower switching speed	Faster switching speed
Over all load capacitance is increased	Over all load capacitance is reduced.

- **High performance dynamics CMOS circuits.**
  - They are designed to take full advantage of the obvious benefits of dynamic operation and at the same time, to allow unrestricted cascading of multiple stages.
  - The ultimate goal is to achieve reliable, high-speed, compact circuits using the least complicated clocking scheme possible.

- **Domino CMOS Logics:-**
  - A dynamic CMOS logic stage, such as the one shown in Fig , is cascaded with a static CMOS inverter stage.

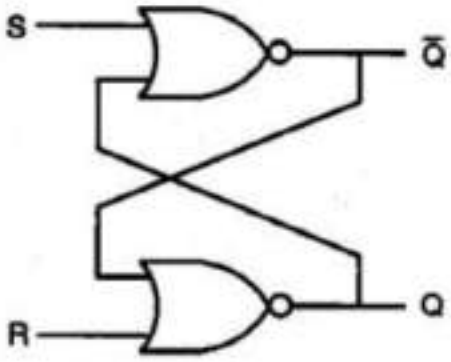


  - The addition of the inverter allows us to operate a number of such structures in cascade.

- During the precharge phase (when CK = 0), the output node of the dynamic CMOS stage is precharged to a high logic level, and the output of the CMOS inverter (buffer) becomes low.
- When the clock signal rises at the beginning of the evaluation phase, there are two possibilities:
  I. The output node of the dynamic CMOS stage is either discharged to a low level through the nMOS circuitry (1 to 0 transition), or it remains high.
  II. Consequently, the inverter output voltage can also make at most one transition during the evaluation phase, from 0 to 1. Regardless of the input voltages applied to the dynamic CMOS stage.

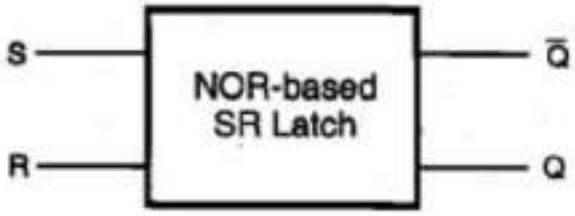
❖ **SR Latch Circuit** :-

- The bistable element consisting of two cross-coupled inverters.



SR latch truth table

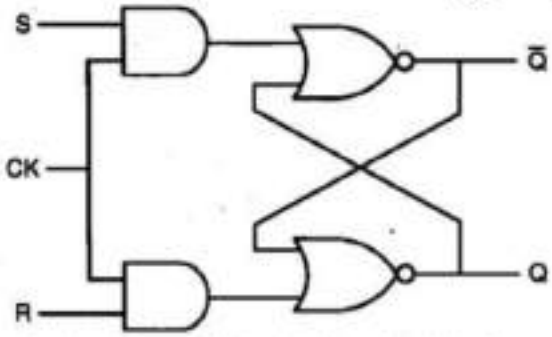
S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	Q_n	$\overline{Q_n}$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed



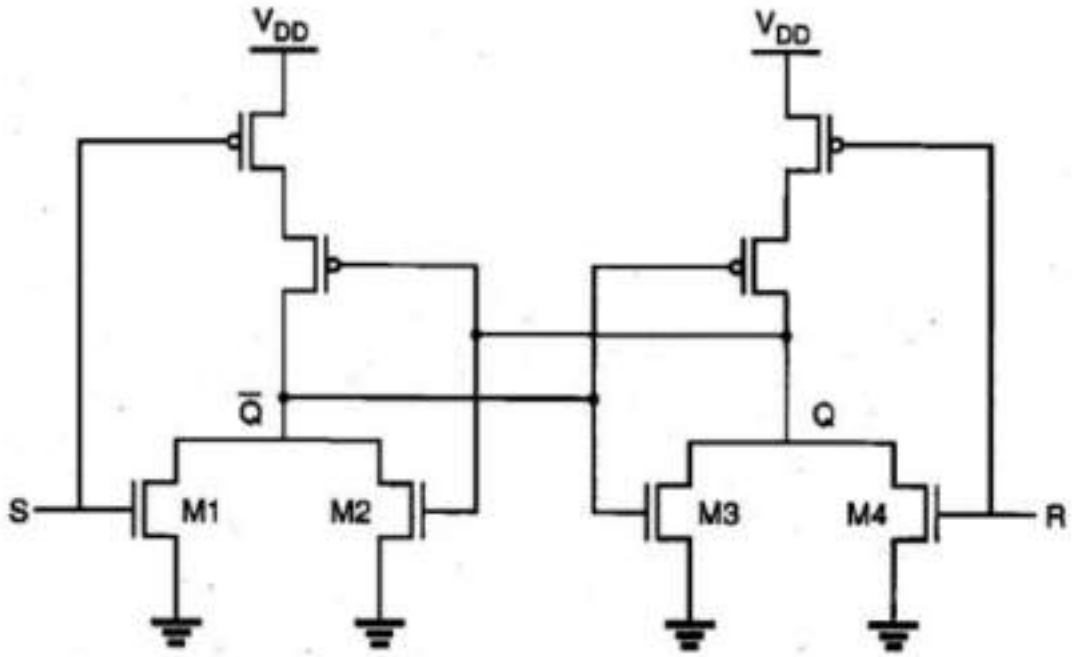
NOR Truth Table

inputs		output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

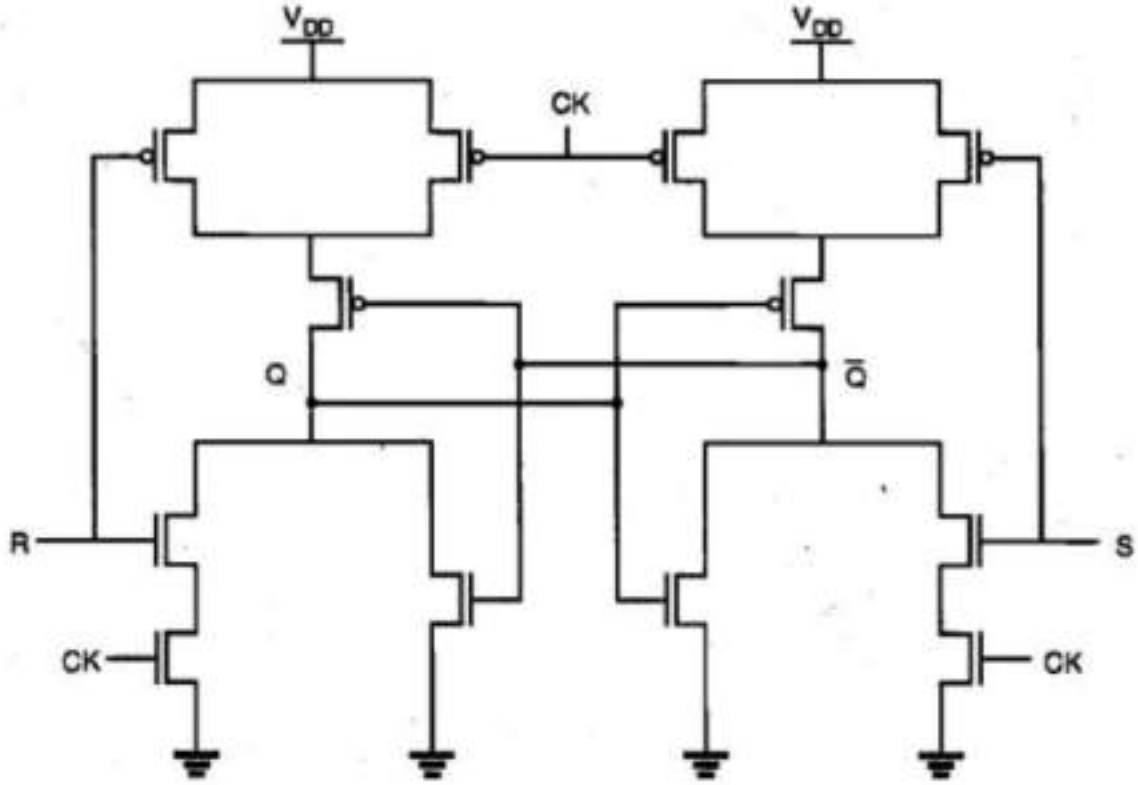
- The circuit preserves its state (either one of the two possible modes) as long as the power supply voltage is provided; hence, the circuit can perform a simple memory function of *holding* its state figure shows the circuit structure of the simple CMOS SR latch.
- This simple SR latch can be implemented by CMOS NOR two gates, one of the input terminals of each NOR gate is used to cross-coupled to the output of other NOR gate. While the second input enables the triggering of the circuit.



(Gate-level schematic of the clocked NOR-based SR latch).



Circuit structure of the simple CMOS SR latch



Implementation of the clocked NOR-based SR latch circuit

RAM (Ramdom Access Memory):-

- In this memory reading and writing is possible
- RAM can be divided into two types
  - Static RAM (S-RAM)
  - Dynamic RAM (D-RAM)

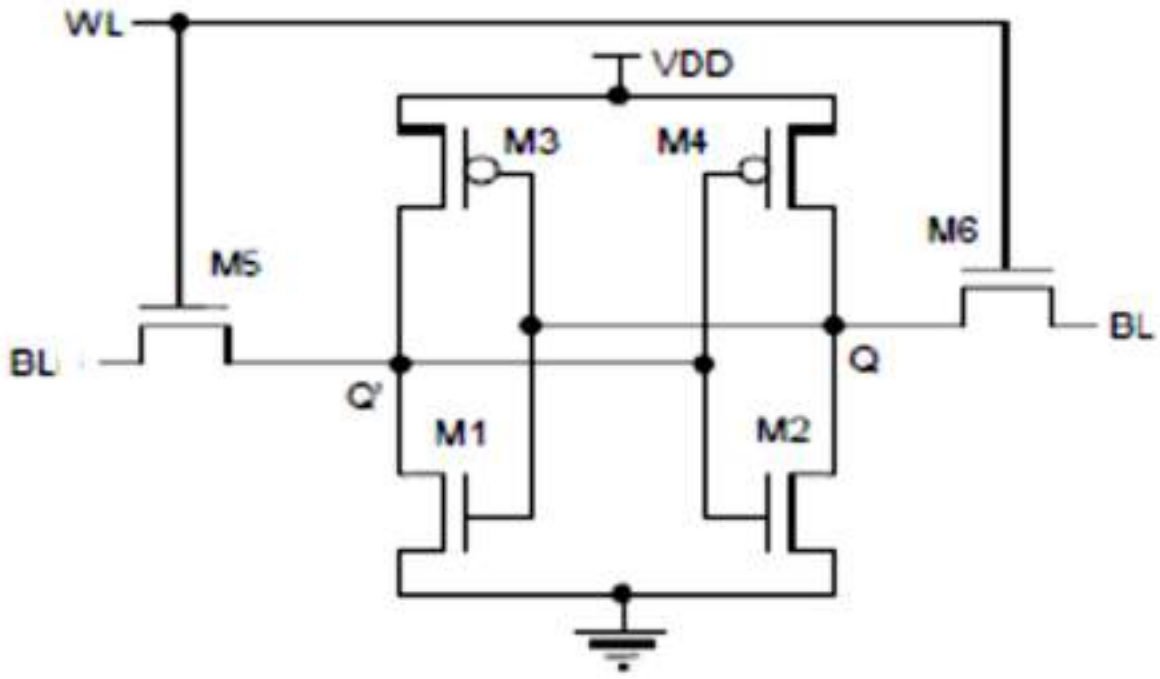
- S-RAM and D-RAM need a supply voltage to hold their information.
- Dynamic RAM - In dynamic RAM the word dynamic stands for periodical refresh which is needed for data integrity.

Static RAM (S-RAM):-

- S-RAM is usually built in cmos technology with 6 transistor.
- Two cross coupled inverter are used to store the information like a flip flop.
- For the access control further two transistor are used.
- If the write line is enable then the data can be read and set with the bit line.

States of a S-RAM:-

- **Stand by –**
  - In this case the write line is disable and no reading and writing operation is possible.
- **Reading :-**
  - Reading starts with pre-leading the bit lines to one and the write gets activated.
  - If Q is one then BL is pulled to one and $\overline{BL}$ pulled zero.



- **Writing :-**
  - setting the bit to one that is BL = 1 and $\overline{BL} = 0$ then by enabling write line we can write.

Advantages:-

- Quick and easy control.
- It can be integrated in a chip.
- It is fast because there is no bus require.

Disadvantages:-

- Many transistor are needed.
- Expensive and higher power consumption.

Dynamic RAM (D-RAM):-

- Here one MOSFET with a capacitor is needed.
- The word line enables writing and reading with the bit lines.
- The reading with the bit lines.
- The D-RAM cell has to be refreshed periodically since the charged gradually leaks.

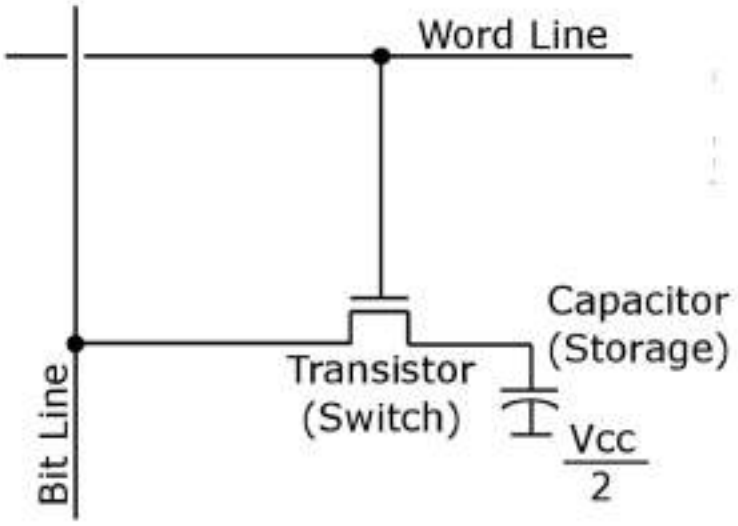
- **Read operation:-**
  - The two bit lines are pre charged between a high and low level.
  - The word line gets activated if the storage capacitor discharged.
  - The small voltage reference between the odd and even row bit line is getting amplify of particular column until one bit line is high and other is law.
- **Write operation:-**
  - Writing words with the bit line to charged or on charged the capacitor.

Advantages:-

- Production is cheaper
- Low power consumption.

Disadvantages:-

- Slower than S-RAM



❖ **Flash memory:-**

- It is a non – volatile memory that can be electrical erased and reprogrammed.
- It is used in memory card and USB flash drive for general storage and transfer of data.
- Flash memory is non-volatile that means no power is need to maintain the information to stored in the chip.
- It is durable when packaged in a memory card.
- It is slower than D-RAM and S-RAM.

Unit-5: System Design method & synthesis

5.1 Design Language (SPL & HDL)& HDL & EDA tools & VHDL and packages Xlinx

❖ VHDL:-

- VHDL is a hardware description language which is strandardise with IEEE 1076 in 1987.
- It include a wide range of data type including numerical logical, character, array of bits and string.
- It was originally developed under contract F33615-83-C-1003 from the United States Air Force awarded in 1983 to a team with Intermetrics, Inc. as language experts and prime contractor, with Texas Instruments as chip design experts and IBM as computer system design experts.
- VHDL is commonly used to write text models that describe a logic circuit.
- Such a model is processed by a synthesis program, only if it is part of the logic design.
- A simulation program is used to test the logic design using simulation models to represent the logic circuits that interface to the design.
- This collection of simulation models is commonly called a *testbench*.
- VHDL can handle the parallelism inherent in hardware designs.
- VHDL is not case sensitive.
- VHDL has an extended set of bolleen operation including NAND and NOR.

- **Advantages:-**
  - When used for systems design, is that it allows the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware.
  - It allows the description of concurrent system VHDL is a dataflow language mean it can process multiple instruction at a time.

❖ XILING:-

- Xilinx ISE (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.
- The Spartan-3 platform was the industry's first 90nm FPGA, delivering more functionality and bandwidth.
- XILING design develops and market and programmable logic products including IC, software develop tool and predefine system function delivered as intellectual code, design services
- XILING sells both FPGA and CPLDA for electronics equipment manufactures in communication industrial consumer and data processing field.

❖ HDL (Hardware Description Language):-

- It is a specialized computer language which is used to program electronic and digital logic circuit.
- Instead of generating a computer executable files the HDL provide a gate map which is then downloaded to the programming device to check the operation of device circuits
- HDL can be of three types:-
  - Verilog
  - VHDL
  - System C

❖ Need of HDL :-

- HDL provides timing information where as C programming does not.
- Complex digital design includes development, synthesis, simulation and debugging by using HDL each module can be operated by a separate team.
  - XILING (VHSIC Hardware Description Language)
  - VHSIC – Very High Speed Integrated Circuit.

Unit-6: Introduction to Embedded Systems

6.1 Embedded Systems Overview, list of embedded systems, characteristics, example – A Digital Camera

❖ **EMBEDDED SYSTEM OVERVIEW:-**

- Computing systems are everywhere. There is no surprise that millions of computing systems are built every year destined for desktop computers (Personal Computers, or PC's), workstations, mainframes and servers.
- The billions of computing systems are built every year for a very different purpose: they are embedded within larger electronic devices, repeatedly carrying out a particular function, often going completely unrecognized by the device's user.
- An embedded system is nearly any computing system other than a desktop, laptop, or mainframe computer

.

❖ **Shortlist of embedded systems:-**

- Embedded systems are found in a variety of common electronic devices, such as:
  - I. **Consumer electronics** -- cell phones, pagers, digital cameras, camcorders, videocassette recorders, portable video games, calculators, and personal digital assistants;
  - II. **Home appliances** -- microwave ovens, answering machines, thermostat, home security, washing machines, and lighting systems;
  - III. **Office automation** -- fax machines, copiers, printers, and scanners;
  - IV. **Business equipment** -- cash registers, curbside check-in, alarm systems, card readers, product scanners, and automated teller machines;

V. **Automobiles** -- transmission control, cruise control, fuel injection, anti-lock brakes, and active suspension.

❖ Characteristics of embedded systems:-

- Embedded systems have several common characteristics:

1) Single-functioned: An embedded system usually executes only one program, repeatedly. For example, a pager is always a pager. A desktop system executes a variety of programs, like spreadsheets, word processors, and video games, with new programs added frequently.

2) Tightly constrained: All computing systems have constraints on design metrics. A design metric is a measure of an implementation's features, such as cost, size, performance, and power. Embedded systems often must cost just a few dollars, must be sized to fit on a single chip, must perform fast enough to process data in real-time, and must consume minimum power to extend battery life or prevent the necessity of a cooling fan.

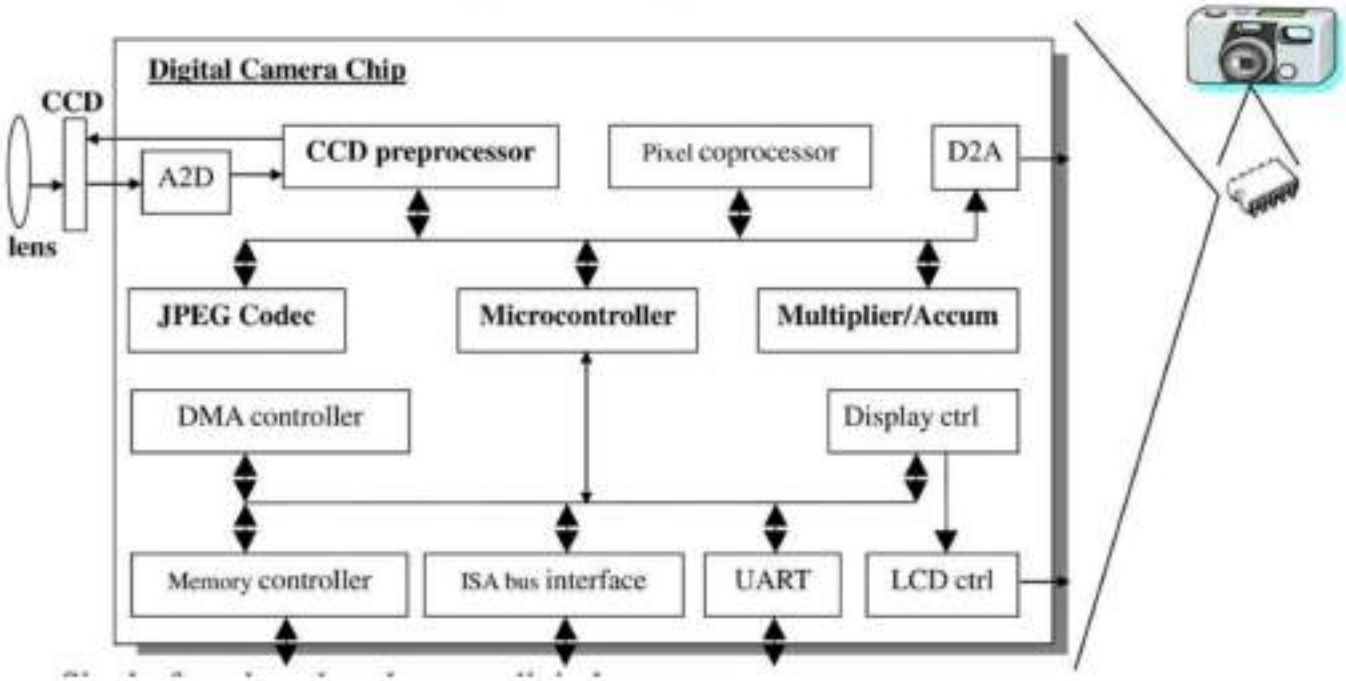
3) Reactive and real-time: Many embedded systems must continually react to changes in the system's environment, and must compute certain results in real time without delay. For example, a car's cruise controller continually monitors and reacts to speed and brake sensors. It must compute acceleration or decelerations amounts repeatedly within a limited time; a delayed computation result could result in a failure to maintain control of the car.

❖ A DIGITAL CAMERA:-

- The **A2D** and **D2A** circuits convert analog images to digital and digital to analog, respectively.
- The **CCD preprocessor** is a charge-coupled device preprocessor.
- The **JPEG codec** compresses and decompresses an image using the JPEG2 compression standard, enabling compact storage in the limited memory of the camera.
- The **Pixel coprocessor** aids in rapidly displaying images.
- The **Memory controller** controls access to a memory chip also found in the camera, while the **DMA controller** enables direct memory access without requiring the use of the microcontroller.
- The **UART** enables communication with a PC's serial port for uploading video frames, while the **ISA bus interface** enables a faster connection with a PC's ISA bus.
- The **LCD ctrl** and **Display ctrl** circuits control the display of images on the camera's liquid-crystal display device.
- A **Multiplier/Accum** circuit assists with certain digital signal processing.
- The heart of the system is a **microcontroller**, which is a processor that controls the activities of all the other circuits. Each device as a processor designed for a particular task, while the microcontroller is a more general processor designed for general tasks.

- This example illustrates some of the embedded system characteristics described above. It performs a single function repeatedly. The system always acts as a digital camera, wherein it captures, compresses and stores frames, decompresses and displays frames, and uploads frames.
- It is tightly constrained. The system must be low cost since consumers must be able to afford such a camera. It must be small so that it fits within a standard-sized camera. It must be fast so that it can process numerous images in milliseconds. It must consume little power so that the camera's battery will last a long time.

A Simple Digital Camera



- This particular system does not possess a high degree of the characteristic of being reactive and real-time, as it only needs to respond to the pressing of buttons by a user, which even for an avid photographer is still quite slow with respect to processor speeds.

6.2 Embedded Systems Technologies--Technology – Definition -Technology for Embedded Systems -Processor Technology -IC Technology

❖ **EMBEDDED SYSTEMS TECHNOLOGIES:-**

- There are three technologies in the embedded system design:
  1. Processor technologies
  2. IC technologies
  3. Design technologies

- **PROCESSOR TECHNOLOGY:-**
  - **General Purpose Processors --- Software:-**
  - The general-purpose processor builds a device suitable for a variety of applications, to maximize the number of devices sold.
  - One feature of such a processor is a program memory – the designer does not know what program will run on the processor, so the program cannot be build into the digital circuit.
  - An embedded system simply uses a general-purpose processor, by programming the processor's memory to carry out the required functionality.

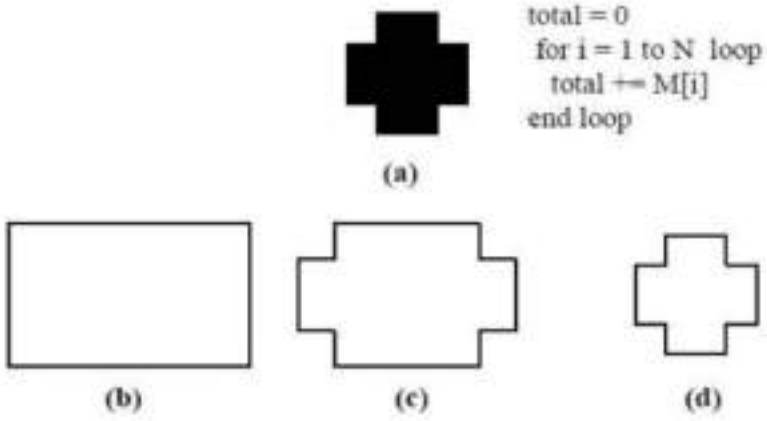
1. Design time and **NRE** *cost* are low, because the designer must only write a program, but need not do any digital design.

2. Flexibility is high, because changing functionality requires only changing the program.

3. Unit cost may be relatively low in small quantities, since the processor manufacturer sells large quantities to other customers.

4. Performance may be fast for computation-intensive applications, if using a fast processor, due to advanced architecture features and leading edge IC technology.

Figure 1 : Processors very in their customization for the problem at hand: (a) desired functionality, (b) general-purpose processor, (b) application-specific processor, (c) single-purpose processor.



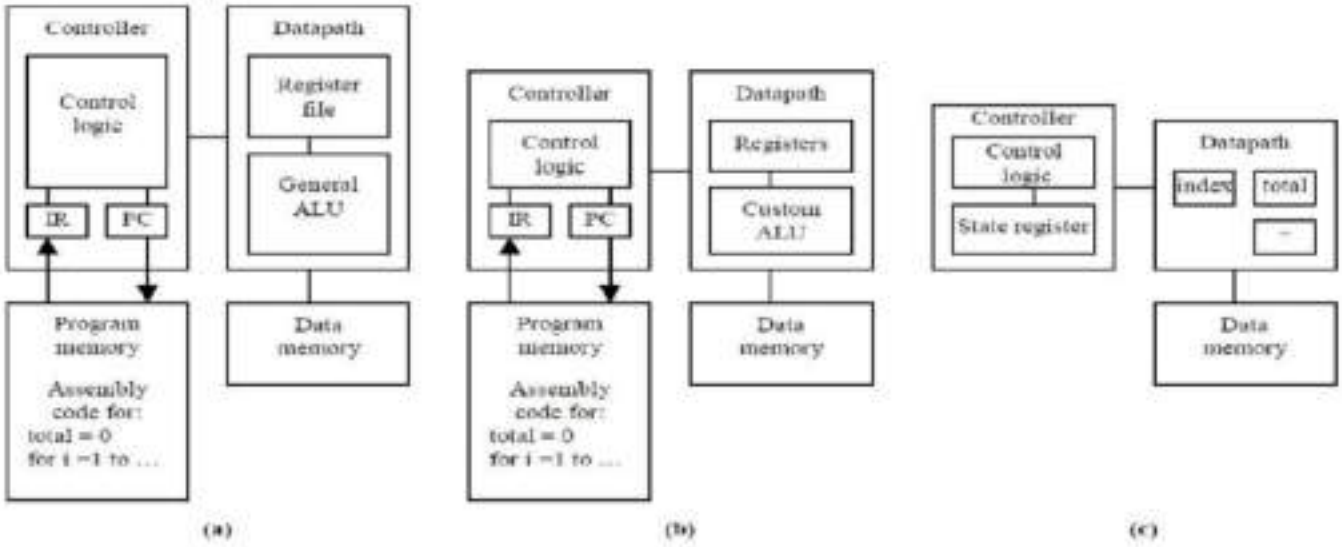
There are also some design-metric drawbacks.

a. Unit cost may be too high for large quantities.

b. Performance may be slow for certain applications.

c. Size and **power** may be large due to unnecessary processor hardware.

Implementing desired functionality on different processor types: (a) general-purpose, (b) application-specific, (c) single-purpose.

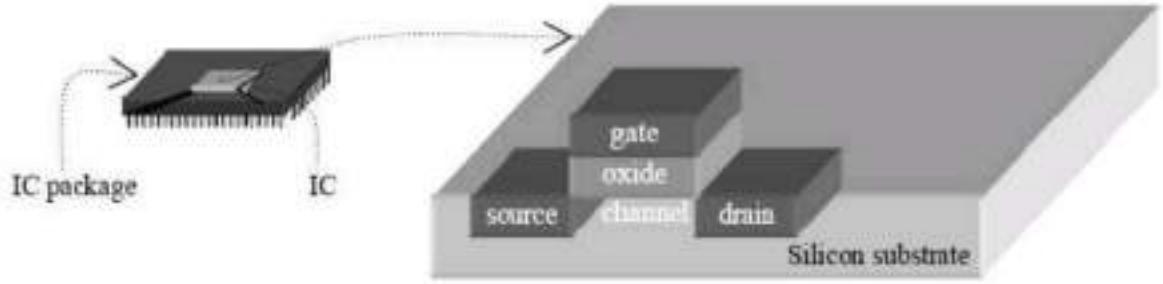


- **Single Purpose Processors ---- Hardware:-**
  - A single-purpose processor is a digital circuit designed to execute exactly one program. For example, consider the digital camera. All of the components other than the microcontroller are single-purpose processors. The JPEG codec, for example, executes a single program that compresses and decompresses video frames.
  - An embedded system creates a single-purpose processor by designing a custom digital circuit.
  - Using a single-purpose processor in an embedded system results in several design metric benefits and drawbacks, which are essentially the inverse of those for general purpose processors.
  - Performance may be fast, size and power may be small, and unit-cost may be low for large quantities, while design time and NRE costs may be high, flexibility is low, unit cost may be high for small quantities, and performance may not match general-purpose processors for some applications.

- **IC TECHNOLOGY:-**
  - Every processor must eventually be implemented on an IC.
  - An IC (Integrated Circuit), often called a "chip," is a semiconductor device consisting of a set of connected transistors and other devices.
  - A number of different processes exist to build semiconductors, the most popular of which is CMOS (Complementary Metal Oxide Semiconductor).

- Semiconductors consist of numerous layers as shown in the figure given below.

Figure : IC's consist of several layers. Shown is a simplified CMOS transistor; an IC may possess millions of these, connected by layers of metal (not shown).



- The bottom layers form the transistors. The middle layers form logic gates. The top layers connect these gates with wires. These layers can be created by depositing photo-sensitive chemicals on the chip surface and then shining light through masks to change regions of the chemicals. A set of masks is often called a layout. The narrowest line that we can create on a chip is called the feature size.

6.4 Application – Specific Processors,Microcontrollers,Digital Signal Processors(DSP)

❖ **APPLICATION -**

❖ **SPECIFIC PROCESSORS:-**

- An application-specific instruction-set processor (or ASIP) can serve as a compromise between the other processor.
- An ASIP is designed for a particular class of applications with common characteristics, such as digital-signal processing, telecommunications, embedded control, etc.
- An ASIP in an embedded system can provide the benefit of flexibility while still achieving good performance, power and size.
- Such processors can require large NRE cost to build the processor itself.

❖ **Microcontrollers:-**

- A microcontroller is a microprocessor that has been optimized for embedded control applications.
- Such applications typically monitor and set numerous single bit control signals but do not perform large amount of data computations. Thus microcontrollers tend to have simple datapaths that excel bit-level operations and reading and writing external bits.
- Furthermore, they tend to incorporate on the microprocessor chip several peripheral components common in control applications like serial communication peripherals, times, counters, pulse width modulators and analog

to digital converters. Such incorporation of peripherals enables single chip implementations and hence smaller and lower cost product.

❖ **Digital Signal Processing:-**

- Digital-signal processors (DSPs) are a common class of ASIP.
- A DSP is a processor designed to perform common operations on digital signals, which are the digital encodings of analog signals like video and audio. These operations carry out common signal processing tasks like signal filtering, transformation, or combination.
- Such operations are usually math-intensive, including operations like multiply and add or shift and add.
- To support such operations, a DSP may have special purpose datapath components such a multiply-accumulate unit, which can perform a computation like T = T + M[i]*k using only one instruction

6.5 IC Technology- Full Custom / VLSI,Semi-Custom ASIC (Gate Array & Standard Cell), PLD (Programmable Logic Device)

❖ **Full Custom / VLSI:-**

- In a full-custom IC technology, we optimize all layers for our particular embedded system's digital implementation.
- Such optimization includes placing the transistors to minimize interconnection lengths, sizing the transistors to optimize signal transmissions and routing wires among the transistors.
- Once all the masks are completed, then we send the mask specifications to a fabrication plant that builds the actual ICs.
- Full-custom IC design, often referred to as VLSI (Very Large Scale Integration) design, has very high NRE cost and long turnaround times (typically months) before the IC becomes available, but can yield excellent performance with small size and power.
- It is usually used only in high-volume or extremely performance-critical applications.

❖ **Semicustom ASIC (Gate Array and Standard Cell):-**

- In an ASIC (Application-Specific IC) technology, the lower layers are fully or partially built, leaving us to finish the upper layers.
- In a gate array technology, the masks for the transistor and gate levels are already built (i.e., the IC already consists of arrays of gates).
- The remaining task is to connect these gates to achieve our particular implementation.
- In a standard cell technology, logic-level cells (such as an AND gate or an AND-OR- INVERT combination) have their mask portions pre-designed, usually by hand.
- Thus, the remaining task is to arrange these portions into complete masks for the gate level, and then to connect the cells.ASICs are by far the most popular IC technology, as they provide for good performance and size, with much less NRE cost than full-custom IC's.

❖ **PLD:-**

- In a PLD (Programmable Logic Device) technology, layers implement a programmable circuit, where programming has a lower-level meaning than a software program.
- The programming that takes place may consist of creating or destroying connections between wires that connect gates, either by blowing a fuse, or setting a bit in a programmable switch.
- Small devices, called programmers, connected to a desktop computer can typically perform such programming.
- PLD's of two types, simple and complex. One type of simple PLD is a PLA (Programmable Logic Array), which consists of a programmable array of AND gates and a programmable array of OR gates.
- Another type is a PAL (Programmable Array Logic), which uses just one programmable array to reduce the number of expensive programmable components.
- One type of complex PLD, growing very rapidly in popularity over the past decade, is the FPGA (Field Programmable Gate Array), which offers more general connectivity among blocks of logic, rather than just arrays of logic as with PLAs and PALs, and are thus able to implement far more complex designs. PLDs offer very low NRE cost and almost instant IC availability.
- They are typically bigger than ASICs, may have higher unit cost, may consume more power, and may be slower (especially FPGAs). They still provide reasonable performance, though, so are especially well suited to rapid prototyping