* The change in the drain current due to change in gate to source voltage can be determined using the transconductance factor g_m.

$$g_m = \frac{\Delta I_d}{\Delta V_{GS}}$$

The another important parameter of JFET is drain resistance r_d.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{Constant}}$$

It determines the output impedence Z_o of the JFET amplifier

The amplification factor μ of an JFET is defined as,

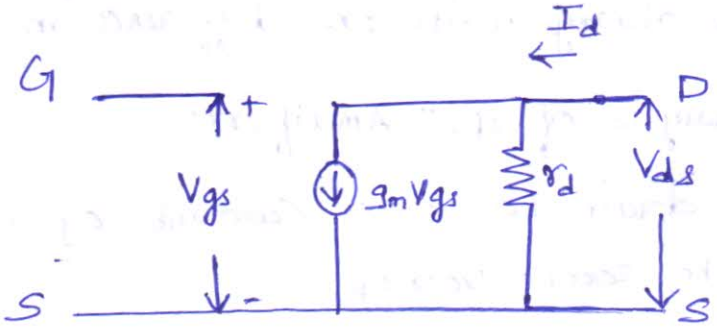
$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D = \text{Constant}}$$

The parameters g_m, r_d and μ are related by

$$\boxed{\mu = r_d g_m}$$

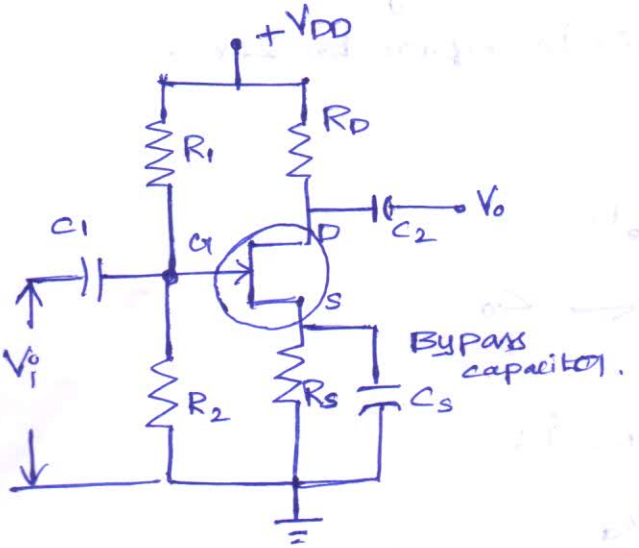
JFET Low Frequency a.c Equivalent circuit

Fig shows the small signal low frequency a.c equivalent circuit for n-channel JFET

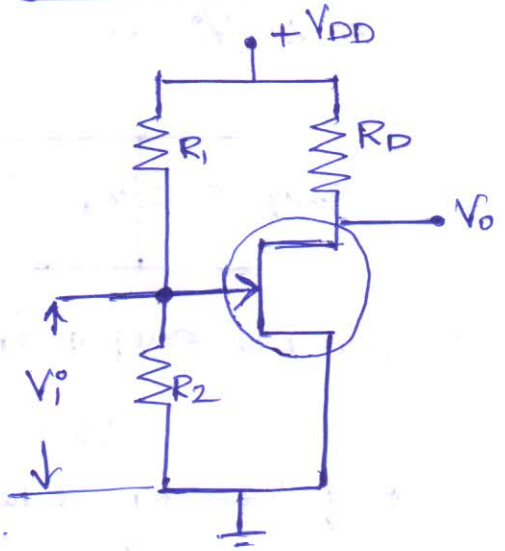


JFET with Common Source Voltage divider bias (Bypassed R_S) (with out R_S)

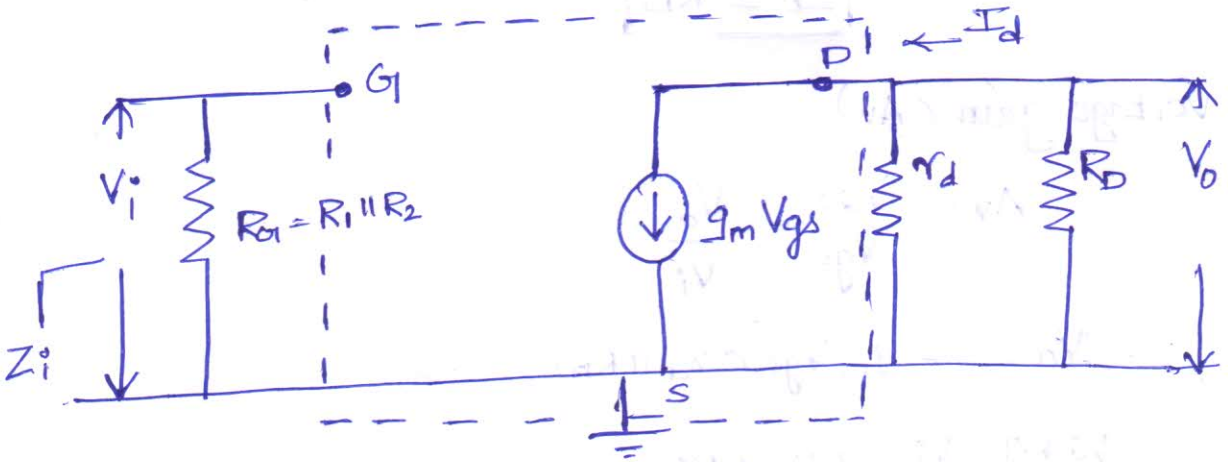
Circuit diagram:



Bypass capacitor replace by short circuit.



AC equivalent circuit.



* The Circuits is drawn by replacing all capacitors & d.c supply voltages with short circuits

1. Input Impedance (Z_i)

$$R_G = R_1 \parallel R_2$$

$$\boxed{Z_i = R_G}$$

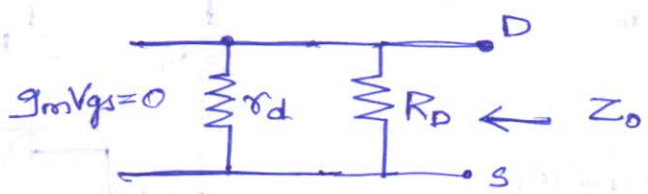
Quote:

End is not the end, in fact E.N.D means "Effort never dies"

2. Output Impedence (Z_o)

It's the impedence measured looking from the output side with input voltage (V_i) is equal to zero.

* As $V_i = 0$



so the output impedence is

$$Z_o = R_D \parallel r_d$$

* if $r_d >> R_D$ then the output impedance is

$$\boxed{Z_o \simeq R_D}$$

3. Voltage gain (A_v)

$$A_v = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{gs} (r_d \parallel R_D)$$

W.K.T $V_i = V_{gs}$ then

$$\boxed{V_o = -g_m V_i (r_d \parallel R_D)}$$

so

$$A_v = \frac{-g_m V_i (r_d \parallel R_D)}{V_i} = -g_m (r_d \parallel R_D)$$

if $r_d >> R_D$

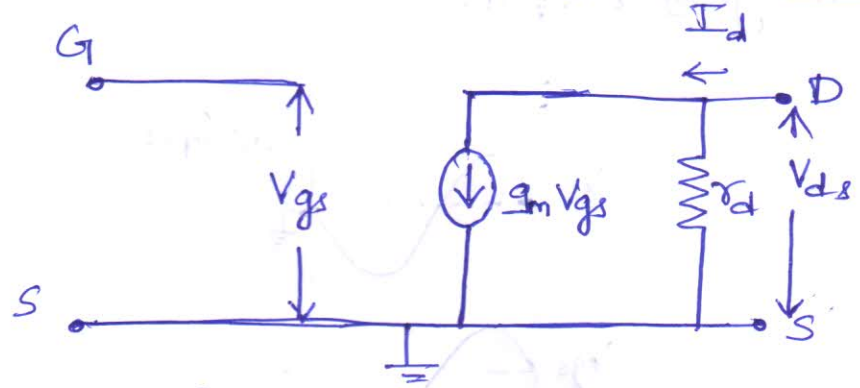
$$\boxed{A_v \simeq -g_m R_D}$$ ∴

Comment: The negative sign indicate, there is a Phase shift of 180° between the input & Output voltage.

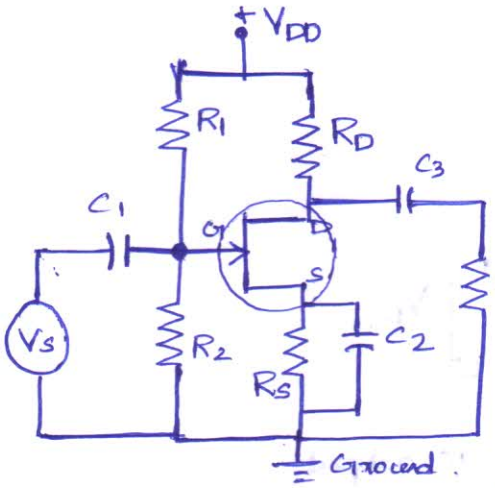
* The input impedence is represented by the open circuit at its input terminal, since I_G is zero.

* The output impedence is represented by r_d from drain to source.

* When the value of external drain resistance R_D is very small as compared to the value of output impedences represented by r_d, it's possible to replace r_d by open circuit.



Common source Circuit Analysis [Basics]



Description

① The input terminals are the gate & source. The output terminals are the drain and source.

② The source terminal is common to the both input & output. The circuit configuration is known as common source.

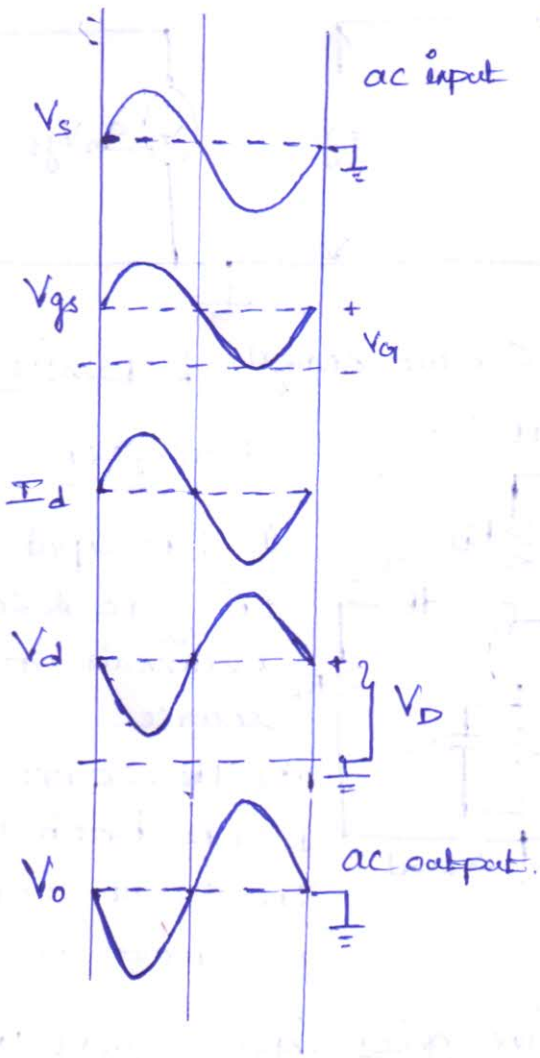
③ For positive going input signal (V_s). There is a 180° phase shift between the input & the output.

④ An increase in V_s increasing the V_{gs}. Thus raising the level of I_D & increases the voltage drop across R_D.

⑤ This produces a decreases in the level of V_D, which is capacitor coupled to the circuit output as a negative going ac output voltage (V_o)

⑥ Consequently, as V_s increases in a positive direction, V_o changes in negative direction.

⑦ Consequently, when V_s changes in negative direction, the resultant decrease in V_{gs} reduces I_d and produce a positive-going output.

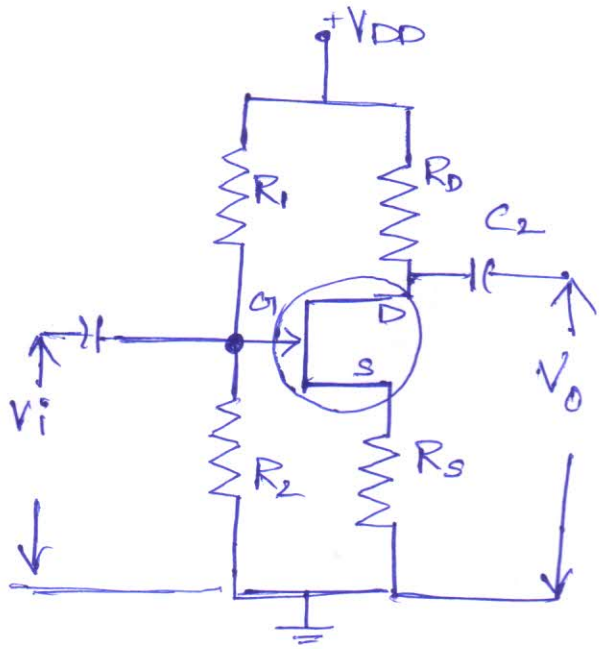


Quote:

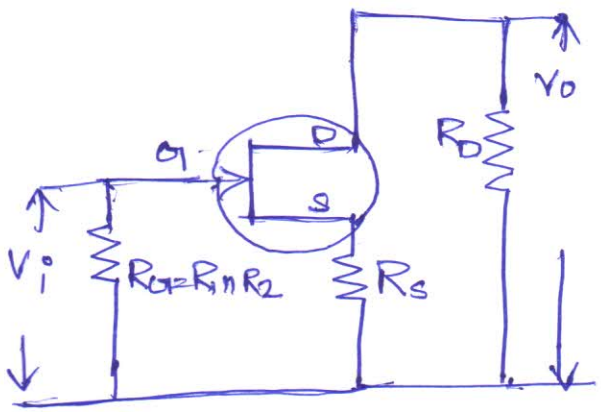
Love your job, but don't love your company because you may not know when your company stop loving you"

JFET with voltage divider Bias (unbypassed R_s)
(with source Resistor)

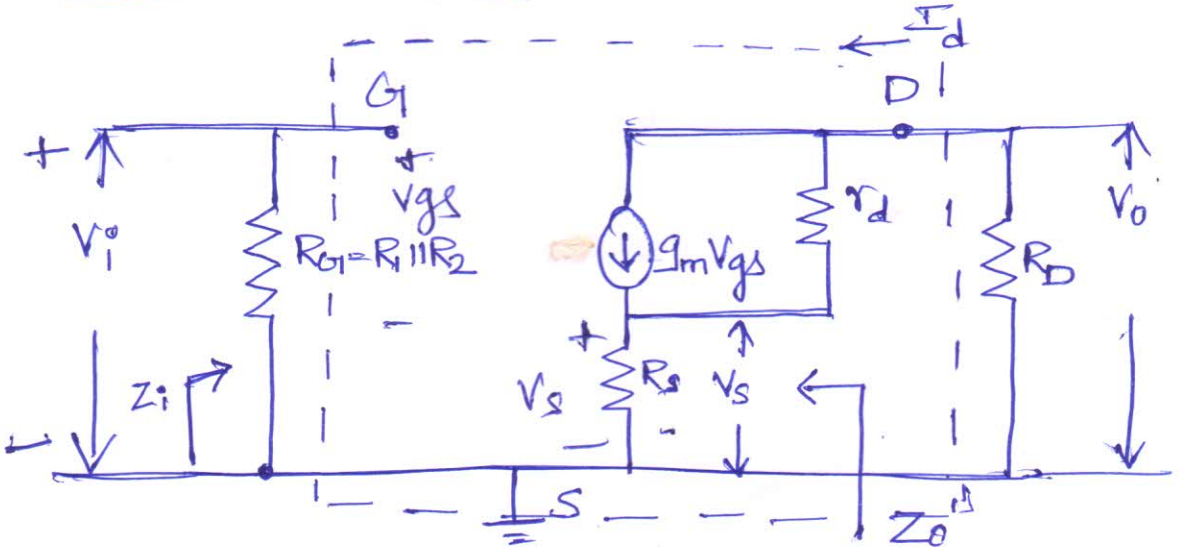
Circuit diagram:



AC Analysis



AC equivalent circuit:



① Input impedence (Z_i)

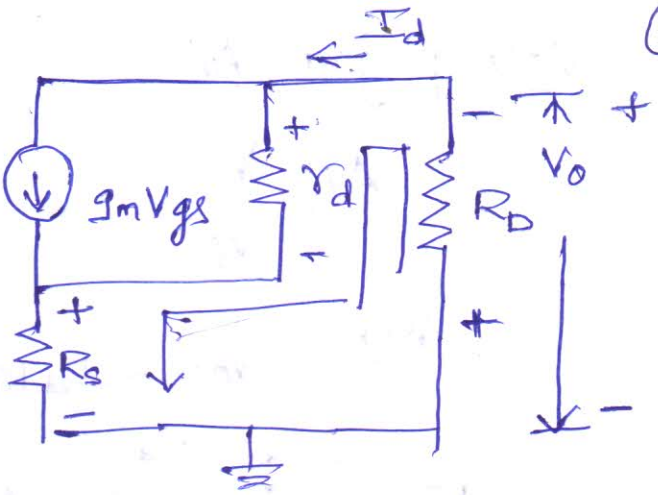
$\therefore R_G = R_1 \| R_2$

$Z_i = R_G$

Quote:

Small daily improvement over time lead to stunning results.

Output impedance:-



$$Z_o = Z_o' \parallel R_D$$

where

$$Z_o' = \frac{V_o}{I_d}\Big|_{V_i=0}$$

* Apply KVL to the output ckt

$$V_o = (I_d - g_m V_{gs}) r_d + I_d R_S \quad -①$$

* Apply KVL to the input ckt.

$$V_{gs} = V_i - I_d R_S$$

$$V_{gs} = -I_d R_S \quad -② \quad [V_i = 0]$$

Sub ② in ①

$$V_o = [I_d - g_m(-I_d R_S)] r_d + I_d R_S$$

$$V_o = [I_d + g_m(I_d R_S)] r_d + I_d R_S$$

$$V_o = I_d r_d + g_m I_d R_S r_d + I_d R_S$$

$$V_o = I_d [r_d + g_m R_S r_d + R_S]$$

$$Z_o' = \frac{V_o}{I_d} = \frac{I_d [r_d + g_m R_S r_d + R_S]}{I_d}$$

$$Z_o' = r_d + \mu R_S + R_S \qquad \because \mu = g_m r_d$$

$$Z_o' = r_d + R_S(\mu + 1)$$

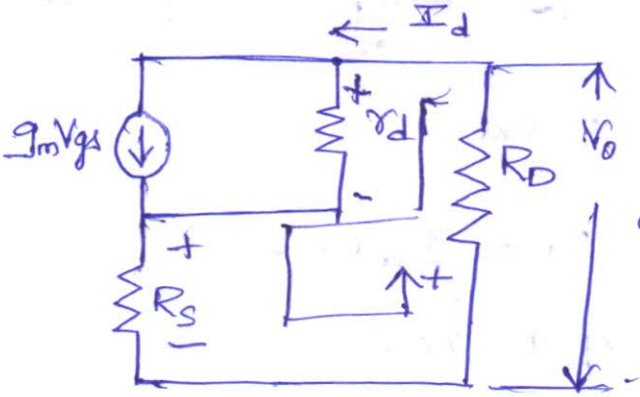
$$\boxed{Z_o = Z_o' \parallel R_D = [r_d + R_S(\mu+1)] \parallel R_D}$$

Voltage gain (A_v)

$$A_v = \frac{V_o}{V_i}$$

W.K.T

$$V_o = -I_d R_D$$



Apply KVL to the output of the circuit,

$$(I_d - g_m V_{gs})\, r_d + I_d R_S + I_d R_D = 0 \quad \text{— (3)}$$

W.K.T $V_{gs} = V_i - I_d R_S$ — (4)

sub (4) in (3)

$$[I_d - g_m(V_i - I_d R_S)]\, r_d + I_d R_S + I_d R_D = 0$$

$$I_d r_d - g_m V_i r_d + g_m I_d R_S r_d + I_d R_S + I_d R_D = 0$$

$$I_d r_d + g_m I_d R_S r_d + I_d R_S + I_d R_D = g_m V_i r_d$$

$$I_d (r_d + g_m R_S r_d + R_S + R_D) = g_m V_i r_d$$

$$I_d = \frac{g_m V_i r_d}{r_d + g_m R_S r_d + R_S + R_D} \quad \text{— (5)}$$

$$V_o = -I_d R_D$$

$$V_o = -\frac{g_m V_i r_d R_D}{r_d + g_m R_S r_d + R_S + R_D}$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_i r_d R_D}{r_d + g_m R_S r_d + R_S + R_D} \cdot \frac{1}{V_i} = \frac{-g_m r_d R_D}{r_d\left[1 + g_m R_S + \frac{R_S + R_D}{r_d}\right]}$$

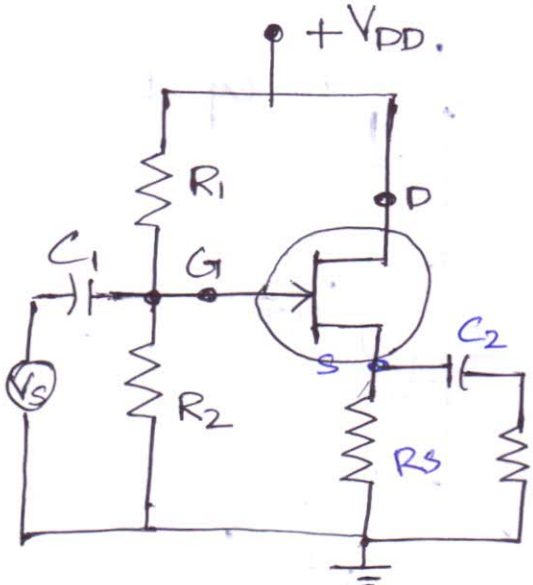
$\because r_d \gg R_S + R_D$

$$\boxed{A_v = \frac{-g_m R_D}{1 + g_m R_S}}$$

$$A_V = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_S + R_D}{r_d}} \quad \because r_d >> R_S + R_D$$

$$\boxed{A_V = \frac{-g_m R_D}{1 + g_m R_S}}$$

Common Drain Circuit Analysis / Source follower



JFET with Voltage divider bias:

Description

* The output voltage developed across the source Resistor (R_S)
* The external load (R_L) is coupled to the source terminal through capacitor.
* The gate voltage (V_G) is derived from V_{DD} by means of voltage divider resistors R_1 & R_2.

The source voltage is

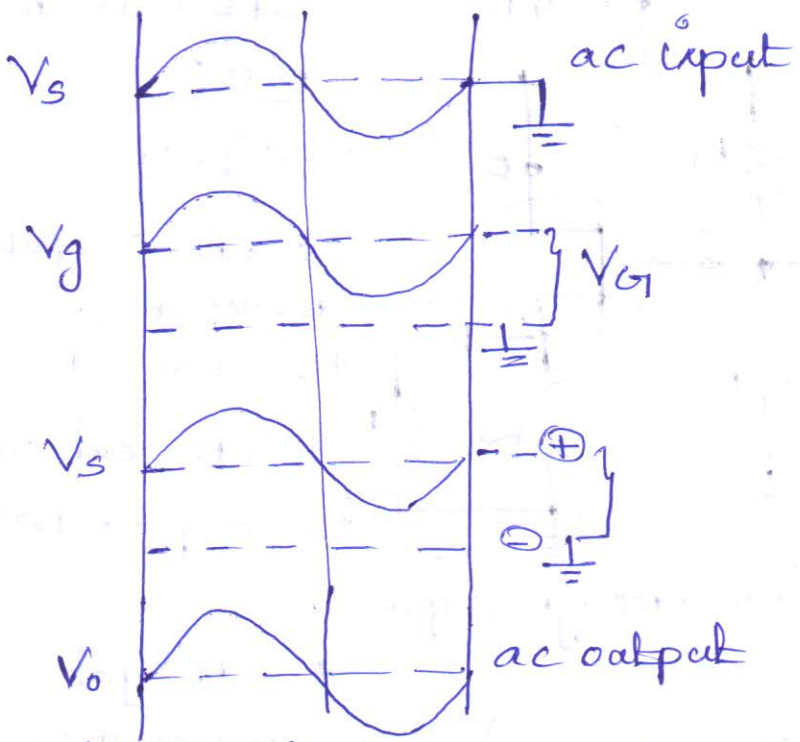
$$V_S = V_G - V_{GS}$$

* When an ac signal is applied to the gate via capacitor C_1 the V_G is increased & decreased as the instantaneous level of the signal voltage raises & falls.

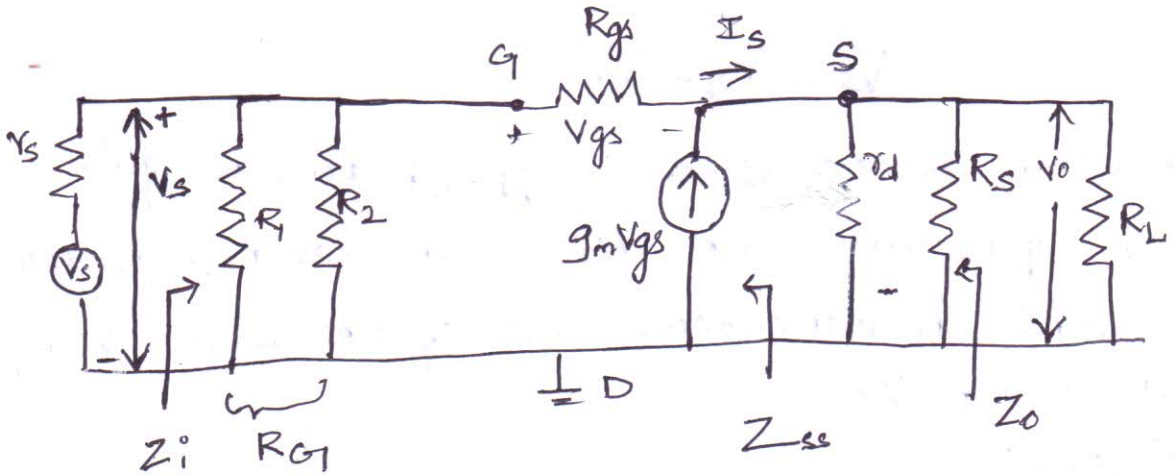
Quote:

* The ac output voltage is closely equal to the ac input voltage & the circuit can be said to have unity gain.

* Because the output voltage at the source terminal follows the signal voltage at the gate (V_{G1}). The common drain circuit is also known as a Source follower.



AC equivalent circuit:-



① Input impedence (Z_i)

$$Z_i = R_G = R_1 \parallel R_2$$

② Output impedence (Z_o)

$$I_s = g_m V_o$$

$$Z_{ss} = \frac{V_o}{I_s} = \frac{V_o}{g_m V_o} = \frac{1}{g_m}$$

$$Z_s = Z_{ss} \parallel r_d = \left(\frac{1}{g_m}\right) \parallel r_d$$

$$Z_o = Z_{ss} \parallel r_d \parallel R_s = \left(\frac{1}{g_m}\right) \parallel r_d \parallel R_s$$

③ Voltage gain (A_v)

$$A_v = \frac{V_o}{V_i}$$

$$V_o = I_s (R_s \parallel R_L) = g_m V_{gs} (R_s \parallel R_L)$$

$$V_i = V_{gs} + V_o = V_{gs} + g_m V_{gs} (R_s \parallel R_L)$$

$$V_i = V_{gs} [1 + g_m (R_s \parallel R_L)]$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{g_m V_{gs} (R_s \parallel R_L)}{V_{gs} [1 + g_m (R_s \parallel R_L)]} = \frac{g_m (R_s \parallel R_L)}{1 + g_m (R_s \parallel R_L)}$$

Comments:

The ac output voltage is usually closely equal to the input voltage, the voltage gain is normally taken as

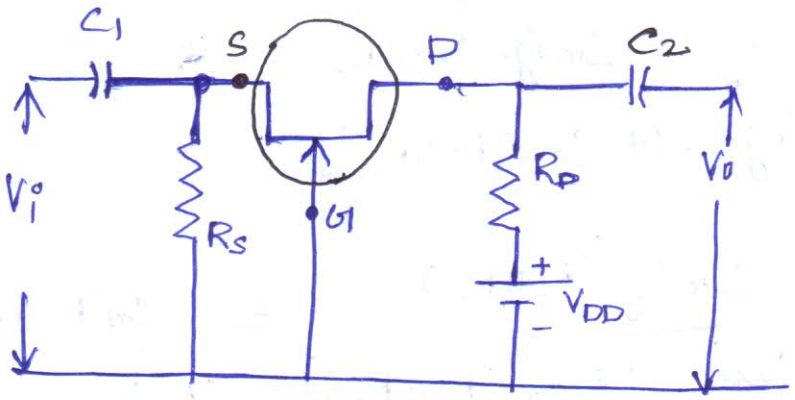
$$\boxed{A_v \simeq 1}$$

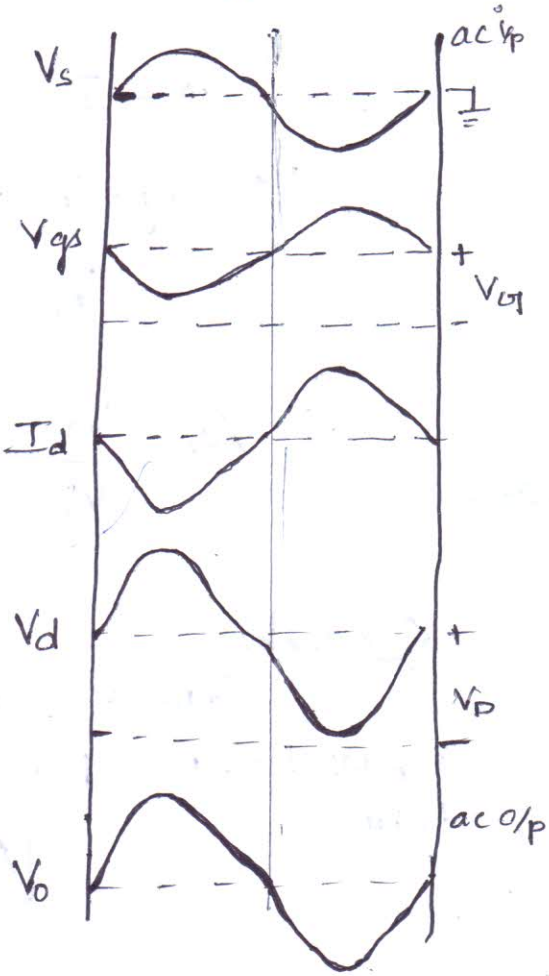
Common Gate Circuit Analysis:-

Introduction:

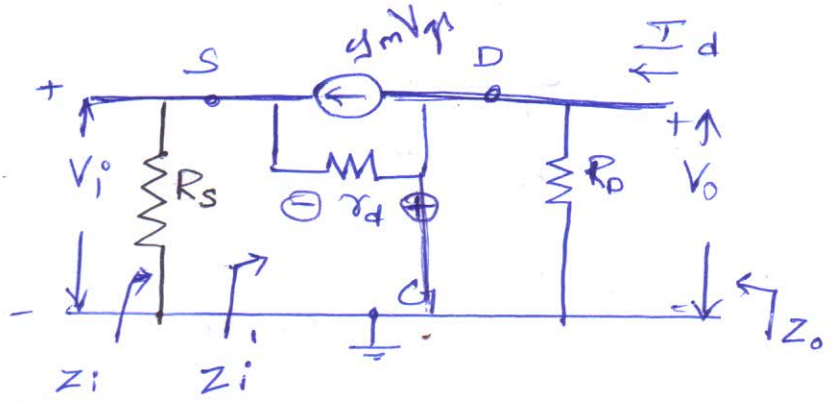
* The input is applied between source & Gate. The output is taken between drain & gate.
* The Gate voltage (V_{G1}) is at constant potential.
* Thus increase in V_s in positive direction increases the negative gate to source bias voltages.
* Due to the I_D decreases, decreasing the drop $I_D R_D$
* $V_D = V_{DD} - I_D R_D$, the reduction in I_D results in an increase in output voltage (V_o)
* When V_s decreases opposite direction decreases the output voltage.
* Thus we can say that there is no phase shift between input & output voltages.

circuit





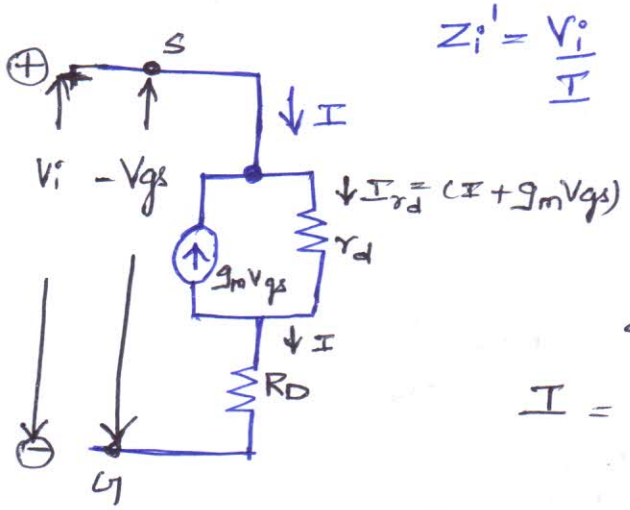
Ac equivalent circuit:



① Input impedance:-

$$Z_i = R_S \parallel Z_i'$$

$$Z_i' = \frac{V_i}{I}$$



Derivation :- By KCL

$$I_{r_d} = I + g_m V_{gs}$$

$$I = I_{r_d} - g_m V_{gs} \quad -①$$

where

$$I_{r_d} = \frac{V_i - I R_D}{r_d} \quad -②$$

sub ② in ① we get,

$$I = \frac{V_i - I R_D}{r_d} - g_m V_{gs} \quad -③$$

$V_i = -V_{gs}$ (or) $V_{gs} = -V_i$ —④ sub ④ in ③

$$I = \frac{V_i - I R_D}{r_d} - g_m(-V_i)$$

$$I = \frac{V_i - I R_D}{r_d} + g_m V_i$$

$$I = \frac{V_i}{r_d} - \frac{I R_D}{r_d} + g_m V_i$$

$$I + \frac{I R_D}{r_d} = \frac{V_i}{r_d} + g_m V_i$$

$$I\left(1 + \frac{R_D}{r_d}\right) = V_i\left(\frac{1}{r_d} + g_m\right)$$

$$V_i = \frac{I\left(1 + \frac{R_D}{r_d}\right)}{\frac{1}{r_d} + g_m}$$

$$Z_i' = \frac{V_i}{I} = \frac{1 + \frac{R_D}{r_d}}{\frac{1}{r_d} + g_m} = \frac{\frac{r_d + R_D}{r_d}}{\frac{1 + g_m r_d}{r_d}} = \frac{r_d + R_D}{1 + g_m r_d}$$

$$Z_i = Z_i' \parallel R_s$$

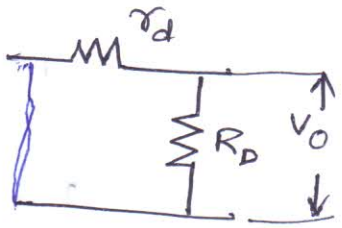
$$Z_i = R_s \parallel \frac{r_d + R_D}{1 + g_m r_d}$$

If $r_d >> R_D$ & $g_m r_d >> 1$

$$Z_i = R_s \parallel \frac{r_d}{g_m r_d} = R_s \parallel \frac{1}{g_m}$$

$$\boxed{Z_i = R_s \parallel \left(\tfrac{1}{g_m}\right)}$$

② Output impedence:



As input is short circuit, R_s is also short circuit & V_{gs} become zero & hence

$$Z_o = r_d \parallel R_D \quad \text{If } r_d >> R_D$$

$$\boxed{Z_o = R_D}$$

Quote:

Life is short. Be of use.

③ voltage gain (A_v)

$$A_v = V_o / V_i$$

$$V_o = -I_d R_D = -g_m V_{gs} R_D$$

$$V_i = -V_{gs}$$

$$A_v = \frac{-g_m V_{gs} R_D}{-V_{gs}} = g_m R_D$$

$$\boxed{A_v = g_m R_D}$$

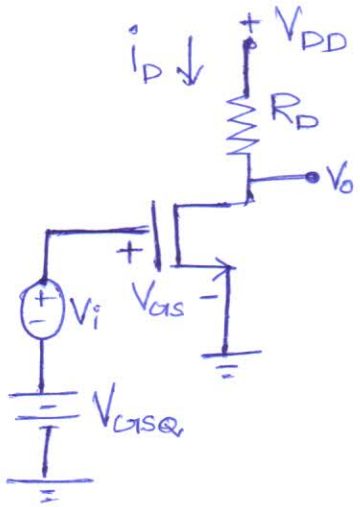
MOSFET

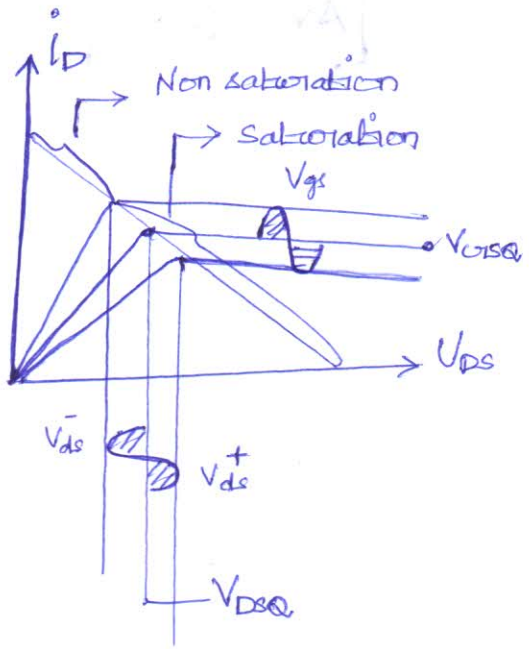
Metal oxide Semiconductor Field Effect Transistor

① Enhancement mode MOSFET common source circuit

② with a time varying (a.c voltage) source in series with the d.c source. We assume the time varying input signal is sinusoidal.

③ The transistor must be biased in the saturation region.





Important:

* $V_i = V_{gs}$ → DC
* $V_{GS} = V_{GSQ} + V_i$ → AC
* Instantaneous drain current is

$$i_D = K_n [V_{GS} - V_{TN}]^2$$

$$i_D = K_n [V_{GSQ} + V_{gs} - V_{TN}]^2 = K_n [\underbrace{V_{GSQ} - V_{TN}}_{a} + \underbrace{V_{gs}}_{b}]^2$$

$$i_D = \underbrace{K_n (V_{GSQ} - V_{TN})^2}_{I_{DQ}} + \underbrace{2K_n (V_{GSQ} - V_{TN}) V_{gs}}_{\hookrightarrow i_d} \qquad (a+b)^2 = a^2 + b^2 + 2ab$$

WKT: $I_{DQ} = K_n (V_{GSQ} - V_{TN})^2$ $\quad i_d = 2K_n (V_{GSQ} - V_{TN})$

To find g_m :-

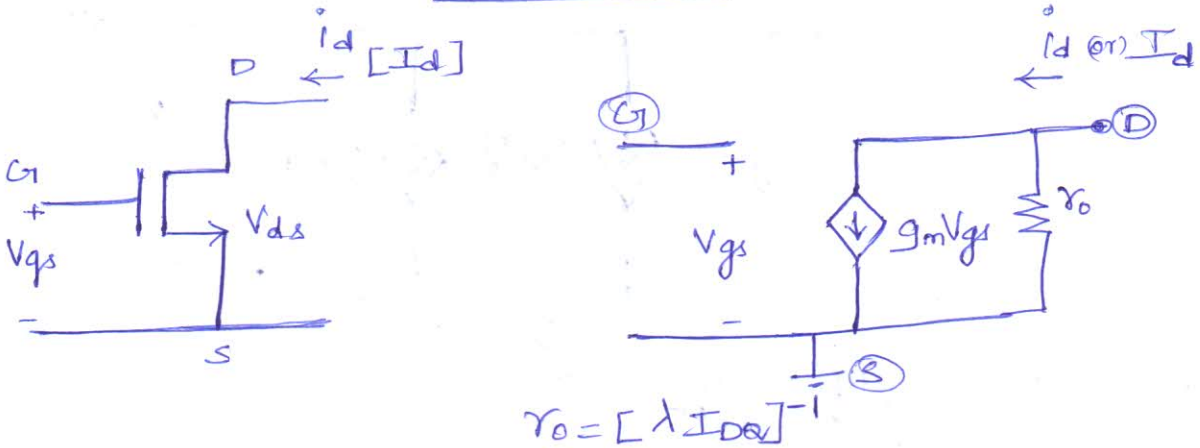
$$g_m = \frac{i_d}{v_{gs}} = \frac{2k_n(V_{GSQ} - V_{TN})v_{gs}}{v_{gs}}$$

$$g_m = 2k_n[V_{GSQ} - V_{TN}]$$

$$g_m = 2\sqrt{k_n I_{DQ}}$$

Small signal Equivalent ckt:-

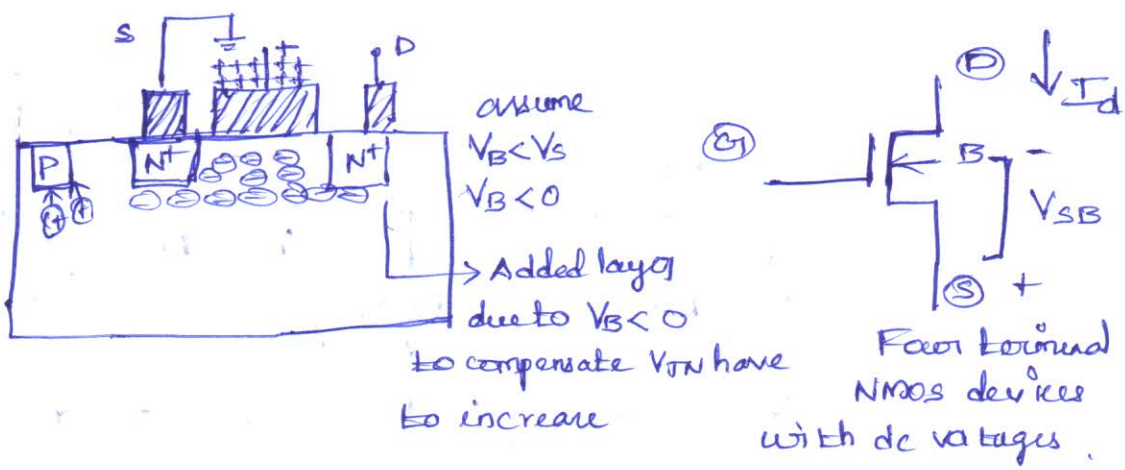
Common source with NMOS transistor



$$r_o = [\lambda I_{DQ}]^{-1}$$

Common source with PMOS transistor:

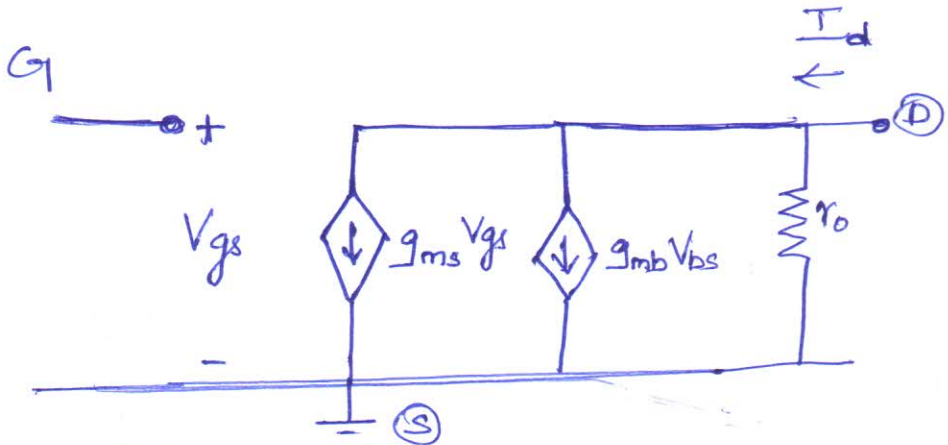
Modeling the body effect:-



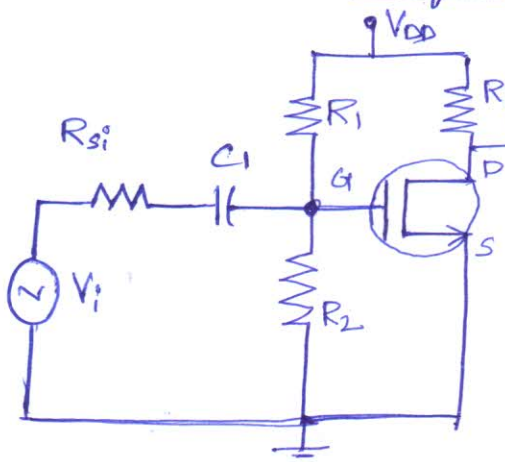
• The body effect occurs in a MOSFET in which the substrate (or) body is not connected to the source.

• For NMOS device, the body is connected to the most negative potential in the ckt & will be at signal ground.

• The V_{SB} must be greater than (or) equal to Zero.



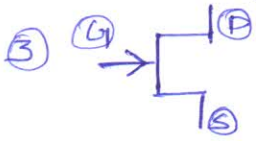
Basic transistor Amplifier configurations: Common source configuration:

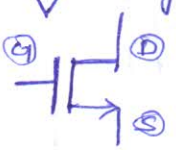


* Thinks to be remember:

① r_d should be replaced by r_o in the MOSFET equivalent ckt.

② $g_m V_{gs}$ replace by $g_m V_{gs}$

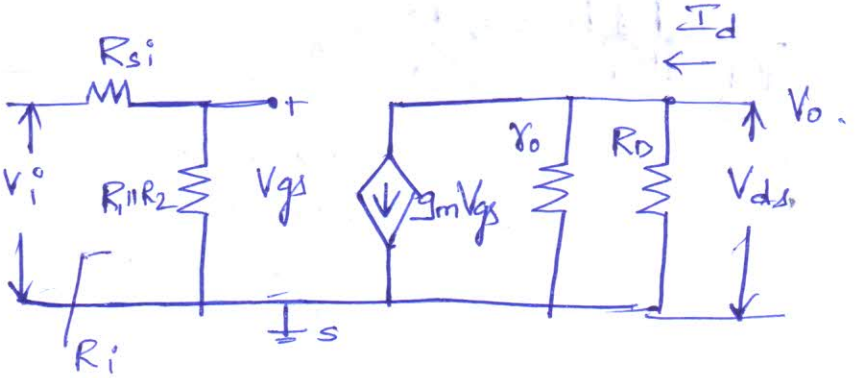
③ 

replaced to


④ Add R_{si} in the MOSFET equivalent CKT

⑤ r_o consider to be finite

AC equivalent ckt:-



Analysis

① Input impedance Z_i :

$$Z_i = R_1 \parallel R_2 = R_G$$

② Output Impedance (Z_o):

$$Z_o = r_o \parallel R_D$$

③ Voltage gain (A_V) :-

$$A_V = -g_m (r_o \parallel R_D) \cdot \frac{R_i}{R_i + R_{si}}$$

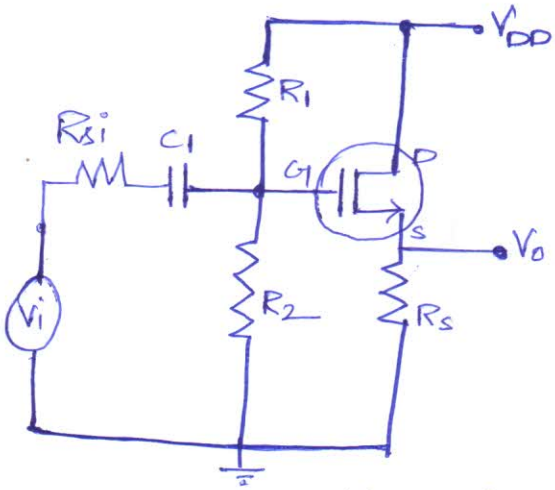
① $V_{gs} = \frac{R_i}{R_i + R_{si}} \cdot V_i$

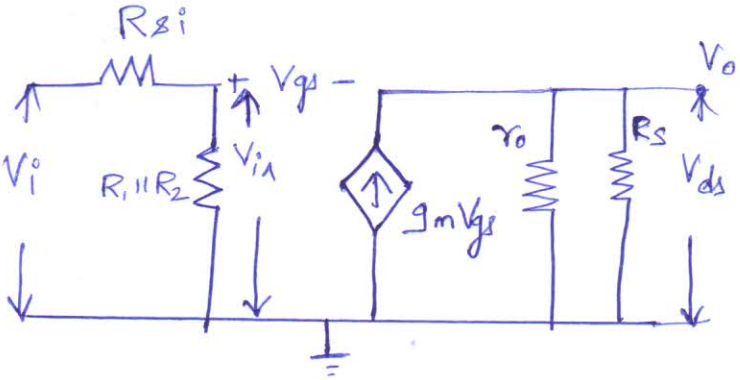
② $R_i = R_1 \parallel R_2$

* MOSFET derivation similliar to JFET.

Common drain / source follower :-

AC analysis





Input impedence (Z_i)

$$Z_i = R_G = R_1 \parallel R_2$$

Output impedence (Z_o)

$$Z_o = 1/g_m \parallel r_o \parallel R_s$$ [similliar to JFET]

Quote: Failure will never overtake me if my determination to succeed is strong enough.

Voltage gain (A_v):

$$V_o = g_m V_{gs}(r_o \| R_s) \quad -①$$

Applying KVL to the outer loop, we have

$$V_{in} - V_{gs} - V_o \quad -②$$

$$V_{in} = V_{gs} + V_o \quad -③$$

sub ① in ③ we get,

$$V_{in} = V_{gs} + g_m V_{gs}(r_o \| R_s) = V_{gs}[1 + g_m(r_o \| R_s)]$$

$$V_{gs} = \frac{V_{in}}{1 + g_m(r_o \| R_s)}$$

using VDR:- $V_{in} = \frac{R_i}{R_i + R_{si}} \cdot V_i$ ---④

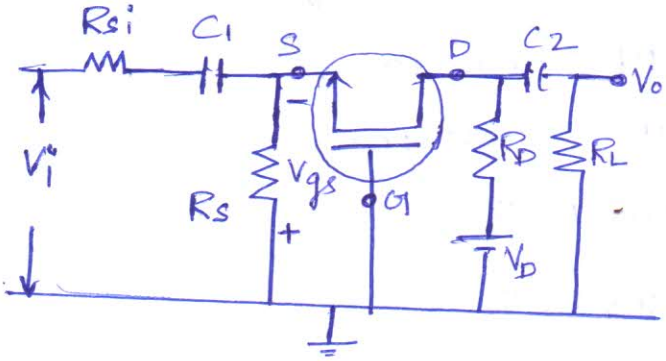
$$V_{gs} = \frac{1}{1 + g_m(r_o \| R_s)} \cdot \frac{R_i}{R_i + R_{si}} \cdot V_i \quad -④$$

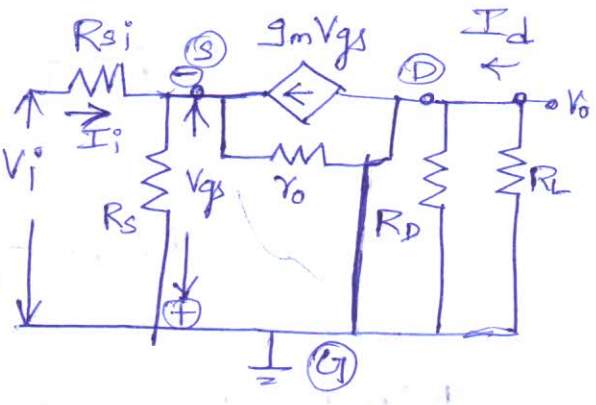
sub ④ in ① we get

$$V_o = \frac{g_m \cdot (r_o \| R_s)}{1 + g_m(r_o \| R_s)} \cdot \frac{R_i}{R_i + R_{si}} \cdot V_i$$

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m(r_o \| R_s)}{1 + g_m(r_o \| R_s)} \cdot \frac{R_i}{R_i + R_{si}}}$$

- Common gate Amplifier (MOSFET) * r_o consider to be finite





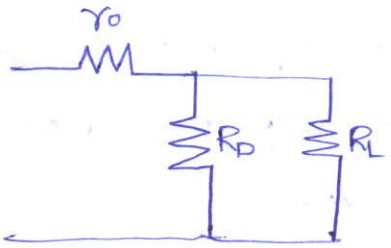
Analysis

① Input Impedence (Z_i)

$$Z_i = R_s \parallel \frac{1}{g_m}$$ [similar to JFET]

② Output Impedence (Z_o)

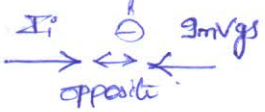
$$\boxed{Z_o = R_D \parallel R_L}$$



③ Voltage gain (A_V)

$$V_o = -I_D(R_D \parallel R_L) = -g_m V_{gs}(R_D \parallel R_L) \quad \text{— ①}$$

Apply KVL in V_p



$$V_i - I_i R_{si} + V_{gs} = (-g_m V_{gs}) R_{si} - V_{gs}$$

$$V_i = (-g_m V_{gs}) R_{si} - V_{gs}$$

$$V_{gs} = \frac{-V_i}{1 + g_m R_{si}} \quad \text{— ②}$$

$$V_o = -g_m \times \frac{-V_i}{1 + g_m R_{si}} \cdot (R_D \parallel R_L)$$

$$\boxed{A_V = \frac{V_o}{V_i} = \frac{g_m}{1 + g_m R_{si}} \cdot (R_D \parallel R_L)}$$

BICMOS cascode Amplifier:

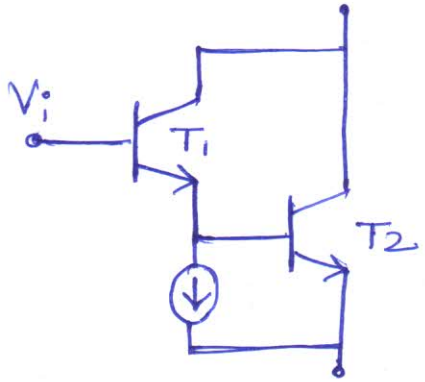
① So far we have seen 2 basic amplifier techniques

① BJT → PNP Transistor
→ NPN Transistor

② MOSFET → NMOS FET
→ PMOS FET

* The BJT have a longer transconductance than MOS transistor
* Due to longe transconductance, they provide longer voltage gain
* MOS transistors have an essentially infinite input impedance at low frequencies. Due to infinite input impedance, MOS transistor have zero input bias current.
* The advantages of these 2 technology can be exploited by combining bipolar & MOS transistors on the same substrate such technology is known as BICMOS technology

Basic Amplifier stages:



(a) Fig: Bipolar Darlington Pair configuration

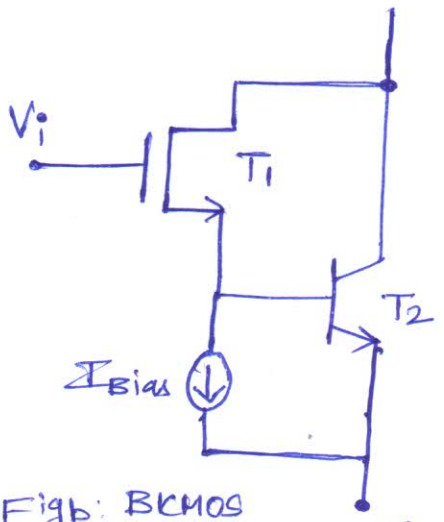


Fig b: BICMOS Darlington pair configuration

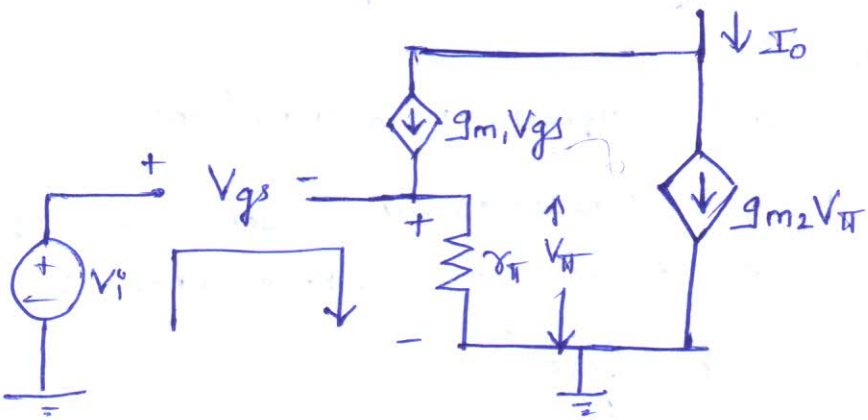
* It uses the bias current I_{bias} (or) some equivalent element to control the quiescent current in transistor $Q_1(T_1)$
* The effective current gain of bipolar transistor is boosted in this circuit.

Fig b:

* Here transistor Q_1 is replaced with MOSFET
* This circuit has following advantages,
  1. An infinite input resistance
  2. A large transconductance due to the bipolar transistor Q_2

Circuit Analysis:-

Consider the small signal equivalent circuit



* Assume $r_o = \infty$ in both directions
* The output signal current is

$$I_o = g_{m_1}V_{gs} + g_{m_2}V_\pi \quad -(1)$$

Apply KVL in input loop,

$$+V_i - V_{gs} - V_\pi$$

$$\boxed{V_i = V_{gs} + V_\pi} \quad -(2) \qquad V_\pi = g_{m_1}V_{gs} \cdot r_\pi \quad -(3)$$

Substitute ② in ③ we get

$$V_i = V_{gs} + g_{m_1} V_{gs} r_\pi$$

$$V_i = V_{gs}[1 + g_{m_1} r_\pi]$$

$$V_{gs} = \frac{V_i}{1 + g_{m_1} r_\pi} \quad -④$$

Substitute ③ in ① we get,

$$I_o = g_{m_1} V_{gs} + g_{m_2} \cdot g_{m_1} V_{gs} r_\pi$$

$$I_o = V_{gs}[g_{m_1} + g_{m_2} g_{m_1} r_\pi] \quad -⑤$$

Sub ⑤ in ④ we get

$$I_o = \frac{(g_{m_1} + g_{m_2} g_{m_1} r_\pi)}{(1 + g_{m_1} r_\pi)} \cdot V_i$$

$$\boxed{I_o = g_m^c \cdot V_i}$$

where

g_m^c – Composite transconductance.

The composite transconductance (g_m^c) is approximately in order of magnitude greater than that of MOSFET.

The circuit has following

① A large transconductance

② An infinite input resistance.

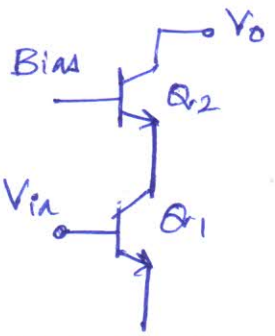


Fig: Bipolar cascode configuration