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| Course Code | 21CSS201T | Course Name | COMPUTER ORGANIZATION AND ARCHITECTURE | Course Category | S | Engineering Sciences | L | T | P | C |
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| Pre-requisite Courses | Nil | Co-requisite Courses | Nil | Progressive Courses | Nil |
| Course Offering Department | School of Computing | Data Book / Codes / Standards | Nil | | |

| Course Learning Rationale (CLR): | | The purpose of learning this course is to: | | | | | | | | | | | | Program Specific outcomes | | |
|----------------------------------|--|--|----------------------|---|---|-----------------------|-------------------------------|--------------------------------------|----------|-----------------------------|---------------------|-----------------------------|------------------------|---------------------------|----------|----------|
| CLR-1 : | Understand the Fundamentals of computers, Memory operations and Addressing Modes | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | P S O -1 | P S O -2 | P S O -3 |
| CLR-2 : | Know about Functions of Arithmetic and Logic unit | En gin ee rin g Know led ge | Pr obl em An aly sis | De sig n/d ev elo pm ent of sol uti ons | Co nd uct inv est iga tio ns of co mp lex pr obl em s | Mo de rn To ol Us age | Th e en gin eer and so cie ty | En vir on me nt & Su sta ina bili ty | Et hic s | Ind ivi du al & Te am W ork | Co m mu ni ca ti on | Pr oje ct Mg t. & Fin an ce | Lif e Lo ng Le arn ing | | | |
| CLR-3 : | Explore the Operations of Control Unit, Execution of Instruction and Pipelining | | | | | | | | | | | | | | | |
| CLR-4 : | Classify the Need for Parallelism, Multicore and Multiprocessor Systems | | | | | | | | | | | | | | | |
| CLR-5 : | Understand the Concepts and functions of Memory unit, I/O unit | | | | | | | | | | | | | | | |
| Course Outcomes (CO): | | At the end of this course, learners will be able to: | | | | | | | | | | | | | | |
| CO-1: | Identify the computer hardware and how software interacts with computer hardware | 3 | 2 | - | - | - | - | - | - | - | - | - | - | 1 | - | - |
| CO-2: | Apply Boolean algebra as related to designing computer logic ,through simple combinational and sequential logic circuits | 3 | 2 | - | - | - | - | - | - | - | - | - | - | - | 2 | - |
| CO-3: | Examine the detailed operation of Basic Processing units and the performance of Pipelining | 3 | - | - | - | - | - | - | - | - | - | - | - | - | - | 1 |
| CO-4: | Analyze concepts of parallelism and multi-core processors. | 3 | - | - | - | - | - | - | - | - | - | - | - | - | 2 | - |
| CO-5: | Classify the memory technologies, input-output systems and evaluate the performance of memory system | 3 | 2 | - | - | - | - | - | - | - | - | - | - | - | 3 | - |

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| Unit-1 - Introduction to Number System and Logic Gates | 9 Hour |
| Number Systems- Binary, Decimal, Octal, Hexadecimal; Codes- Grey, BCD,Excess-3, ASCII, Parity; Binary Arithmetic- Addition, Subtraction, Multiplication, Division using Sign Magnitude,1's compliment, 2's compliment, BCD Arithmetic; Logic Gates-AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR. | |
| Unit-2 - Basic Structure of computers | 9 Hour |
| Functional Units of a computer, Operational concepts, Bus structures, Memory addresses and operations, assembly language , Instructions, Instruction sequencing, Addressing modes. Case study: 8086. | |
| Unit-3 - Design of ALU | 9 Hour |

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| De Morgan's Theorem, Adders, Multiplier – Unsigned, Signed, Fast, Carry Save Addition of summands; Division–Restoring and Non-Restoring; IEEE 754 Floating point numbers and operations. | |
| Unit-4 - Control Unit | 9 Hour |
| Basic processing unit, ALU operations, Instruction execution, Branch instruction, Multiple bus organization, Hardwired control, Generation of control signals, Micro-programmed control; Pipelining: Basic concepts of pipelining, Performance, Hazards-Data, Instruction and Control, Influence on instruction sets. | |
| Unit-5 - Parallelism | 9 Hour |
| Need, types, applications and challenges, Architecture of Parallel Systems-Flynn's classification; ARM Processor: The thumb instruction set, Processor and CPU cores, Instruction Encoding format, Memory load and Store instruction, Basics of I/O operations. Case study: ARM 5 and ARM 7 Architecture | |

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| Learning Resources | 1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th ed., McGraw-Hill, 2015 | 5. William Stallings, Computer Organization and Architecture – Designing for Performance, 10th ed., Pearson Education, 2015 |
| | 2. Kai Hwang, Faye A. Briggs, Computer Architecture and Parallel Processing, 3rd ed., McGraw Hill, 2016 | 6. David A. Patterson and John L. Hennessy, Computer Organization and Design – A Hardware/Software Interface, 5th ed., Morgan Kaufmann, 2014 |
| | 3. Ghosh T.K., Computer Organization and Architecture, 3rd ed., Tata McGraw-Hill, 2011 | |
| | 4. P. Hayes, Computer Architecture and Organization, 3rd ed., McGraw Hill, 2015. | |

| Learning Assessment | | | | | | | |
|---------------------|------------------------------|--|----------|--------------------------------------|----------|---|----------|
| | Bloom's Level of Thinking | Continuous Learning Assessment (CLA) | | | | Summative Final Examination (40% weightage) | |
| | | Formative CLA-1 Average of unit test (50%) | | Life-Long Learning CLA-2 (10%) | | | |
| | | Theory | Practice | Theory | Practice | Theory | Practice |
| Level 1 | Remember | 30% | - | 30% | - | 30% | - |
| Level 2 | Understand | 30% | - | 30% | - | 30% | - |
| Level 3 | Apply | 20% | - | 20% | - | 20% | - |
| Level 4 | Analyze | 20% | - | 20% | - | 20% | - |
| Level 5 | Evaluate | - | - | - | - | - | - |
| Level 6 | Create | - | - | - | - | - | - |
| | Total | 100 % | | 100 % | | 100 % | |

| Course Designers | | |
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| Experts from Industry | Experts from Higher Technical Institutions | Internal Experts |
| 1. Mr. Saminath Sanjai, Borqs Technologies, Inc. Bengaluru | | 1. Dr. K. Vijaya, Dr. Anitha D, SRMIST |