Unit - V

Programmable Logic Devices

RAM Memory decoding

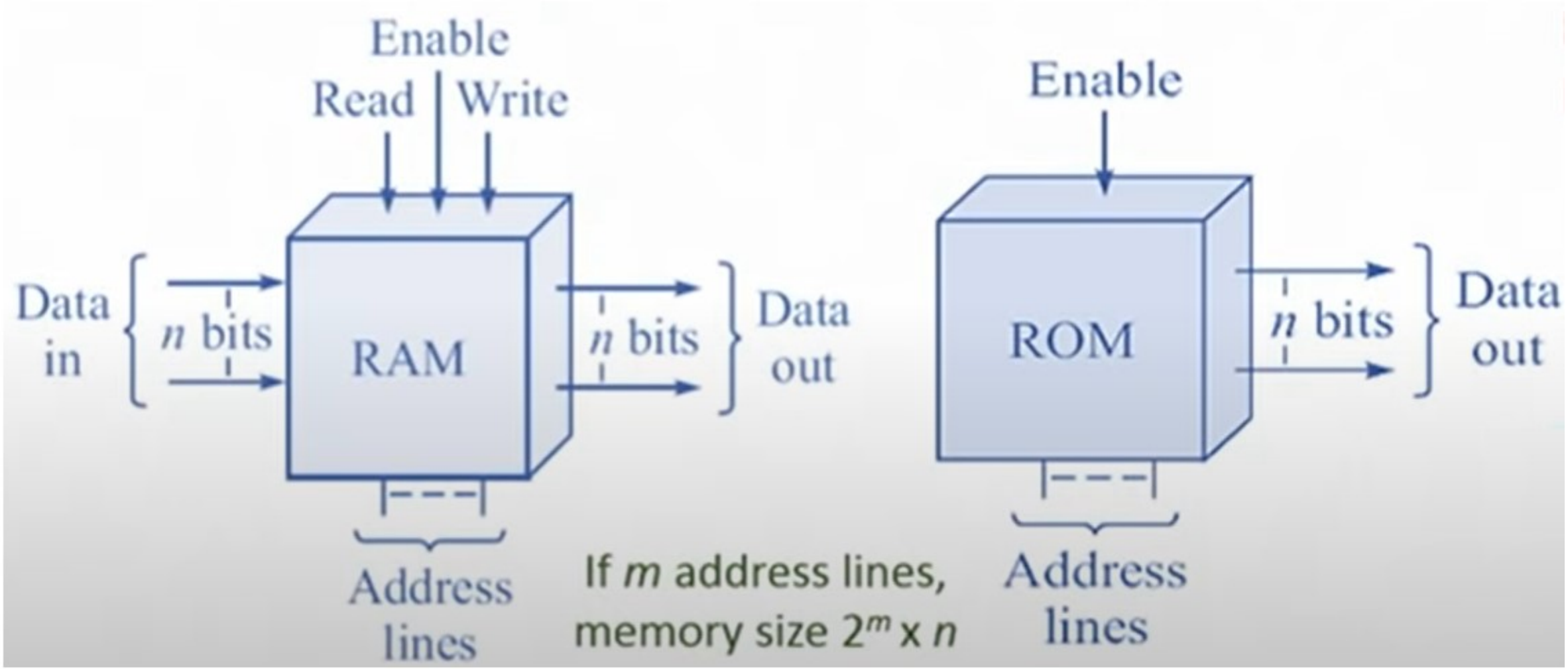
Circuits and /or systems designed specifically for data storage are referred to as memory

Memory may be flip-flop, register, semiconductor memory chips (also magnetic, optical disc).

There are two types of memories that are used in digital systems:

- Random-access memory(RAM): perform both the write and read operations. Is volatile
- Read-only memory(ROM): perform only the read operation. Content is written by developer by special mechanism. Is non-volatile. Also random access (independent of the physical position of the memory within memory block.
  - The read-only memory is a programmable logic device.
  - Other such units are the programmable logic array(PLA),
  - the programmable array logic(PAL),
  - and the field-programmable gate array(FPGA).

RAM and ROM


Enable
Read
Write
Data in
n bits
RAM
n bits
Data out
Address lines
If m address lines, memory size 2^m x n
Enable
ROM
n bits
Data out
Address lines

RAM

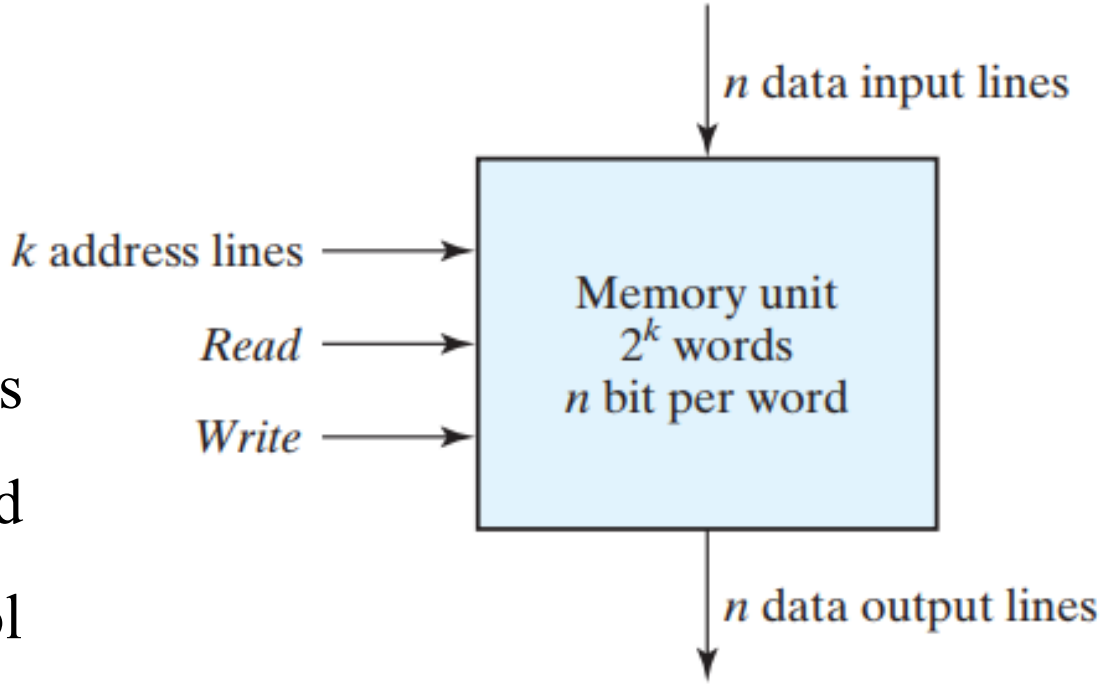
Random-Access Memory

- A memory unit stores binary information in groups of bits called words.

1 byte = 8 bits

1 word = 2 bytes (or more)

- The communication between a memory and its environment is achieved through data input and output lines, address selection lines, and control lines that specify the direction of transfer.



RAM Memory Contents

Each word in memory is assigned an identification number, called an address, starting from 0 up to 2^k -1,

where k is the number of address lines.

• The number of words in a memory

with one of the letters K=2^{10},

M=2^{20}, or G=2^{30}

64K = 2^{16}

2M = 2^{21}

4G = 2^{32}

Memory address		Memory content
Binary	decimal	
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Content of a 1024 × 16 Memory

RAM Memory Write/Read operation

Transferring a new word to be stored into memory:

1. Apply the binary address of the desired word to the address lines.

2. Apply the data bits that must be stored in memory to the data input lines.

3. Activate the write input.

Transferring a stored word out of memory:

1. Apply the binary address of the desired word to the address lines.

2. Activate the read input.

• Commercial memory sometimes provide the two control inputs for reading and writing in a different configuration.

Control Inputs to Memory Chip

Memory Enable	Read/Write	Memory Operation
0	X	None
1	0	Write to selected word
1	1	Read from selected word

Types of Memories

In random-access memory, the word locations may be thought of as being separated in space, with each word occupying one particular location.

- In sequential-access memory, the information stored in some medium is not immediately accessible, but is available only certain intervals of time. A magnetic disk or tape unit is of this type.

In a random-access memory, the access time is always the same regardless of the particular location of the word.

- In a sequential-access memory, the time it takes to access a word depends on the position of the word with respect to the reading head position; therefore, the access time varies.

Types of RAM: Static RAM

SRAM consists essentially of internal latches that store the binary information.

- The stored information remains valid as long as power is applied to the unit.
- SRAM is easier to use and has shorter read and write cycles.
    - Low density
    - Low capacity
    - High cost
    - High speed
    - High power consumption

Types of RAM: Dynamic RAM

DRAM stores the binary information in the form of electric charges on capacitors.

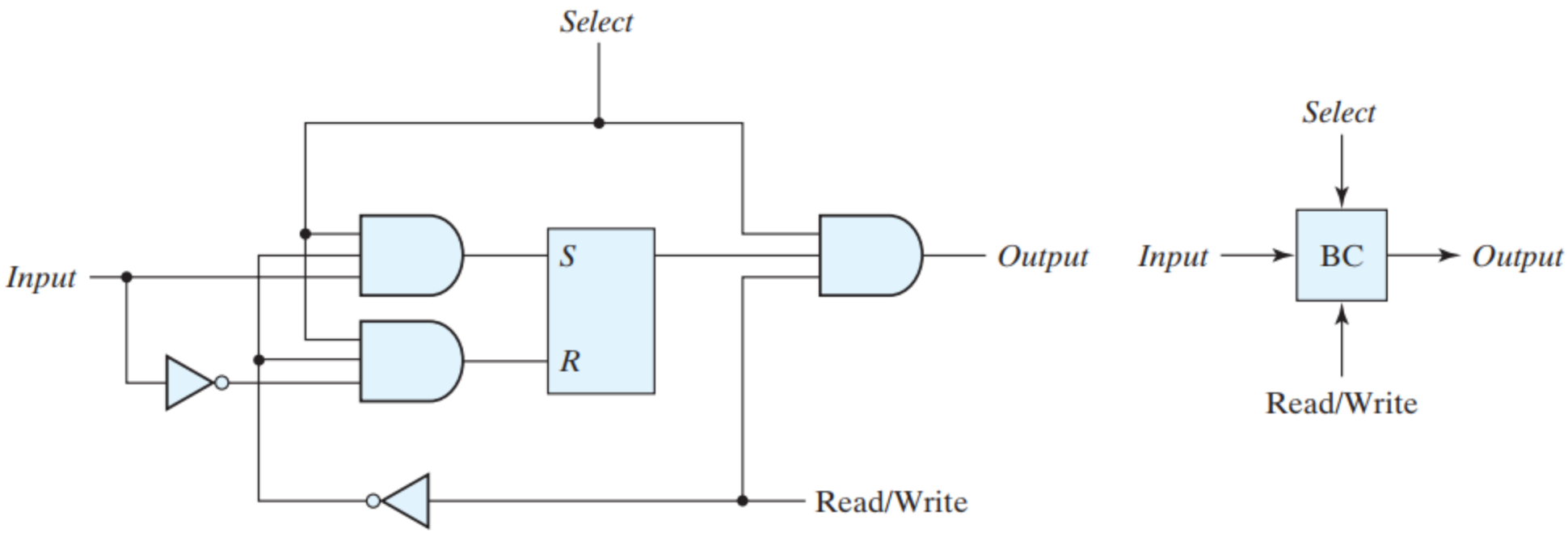
• The capacitors are provided inside the chip by MOS transistors.

• The capacitors tends to discharge with time and must be periodically recharged by refreshing the dynamic memory.

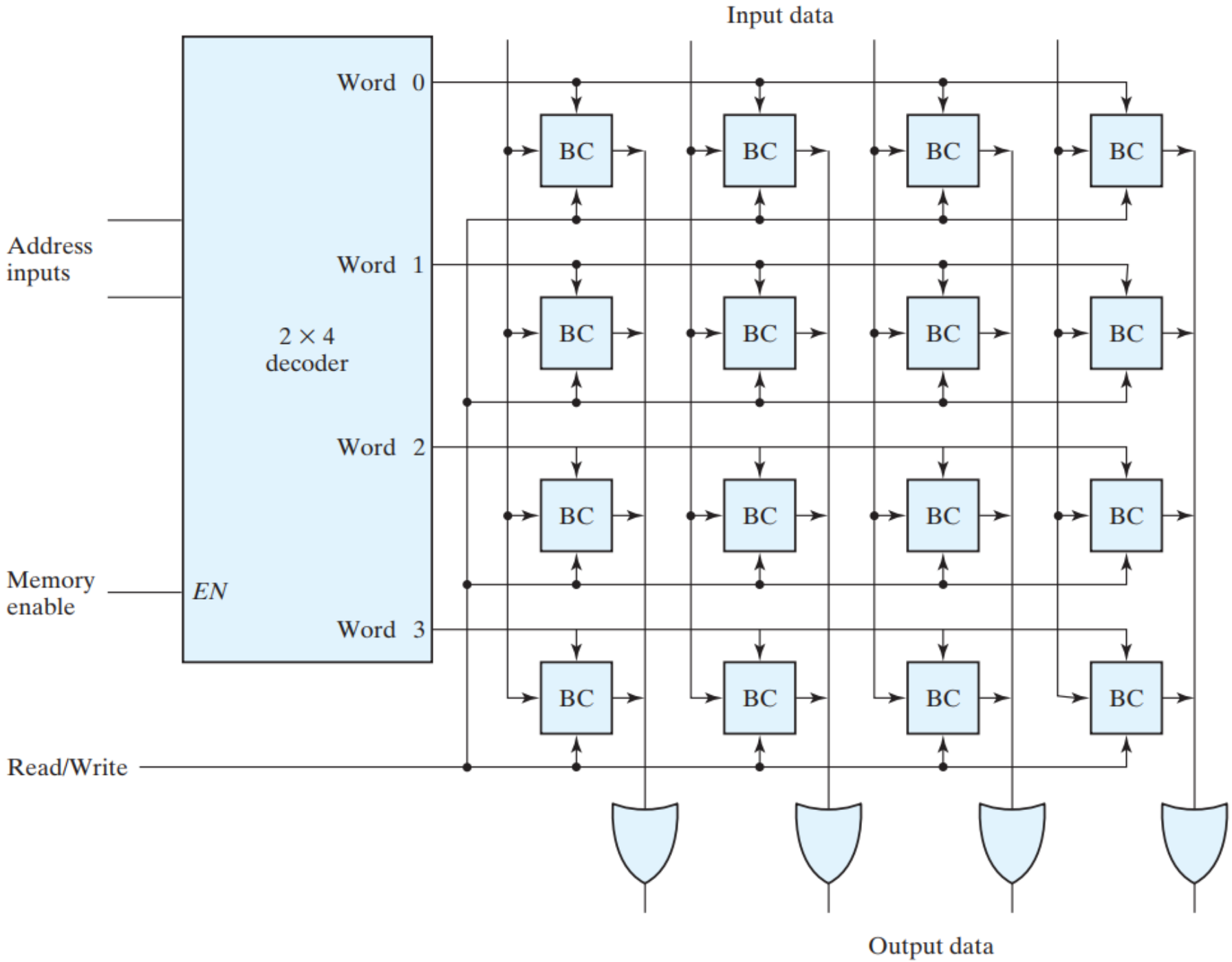
DRAM offers reduced power consumption and larger storage capacity in a single memory chip.

- High density
- high capacity
- low cost
- low speed
- low power consumption

Memory Decoding

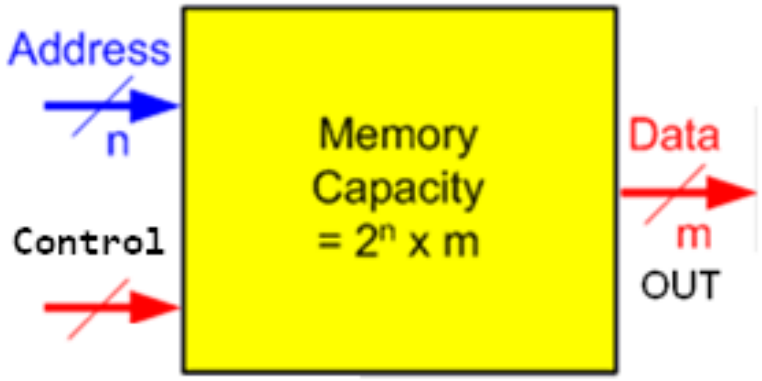


Memory cell


Input data
Word 0
Word 1
Word 2
Word 3
Address inputs
2 × 4 decoder
Memory enable
EN
Read/Write
BC
Output data

Read only memory (ROM)

- Data stored in a ROM is non-volatile, i.e. this data is permanently stored until erased or changed through re-programming (if applicable)
- The ROM has n input lines for the address and m output data lines
- Total memory capacity of a ROM is 2^n x m bits
- ROMs do not have input lines as a write operation does not exist in them
- Programmable ROMs receive data to be programmed on the output lines
- Generally, system-level programs that need to be accessed frequently and at power up access are stored in the computer's ROM, e.g. the BIOS firmware



Types of ROM

- Simply ROM: Programmed only once and by the manufacturer (in factory), based on the client's truth table
- PROM: A ROM programmable only once by the user (in the field). The user blows fuses to remove unwanted connections. This process is irreversible and hence device is programmed only once
- EPROM: Erasable, Programmable ROMs. Can have their data erased using Ultraviolet light and reprogrammed. The user can then reprogram the ROM many times using special programmers.

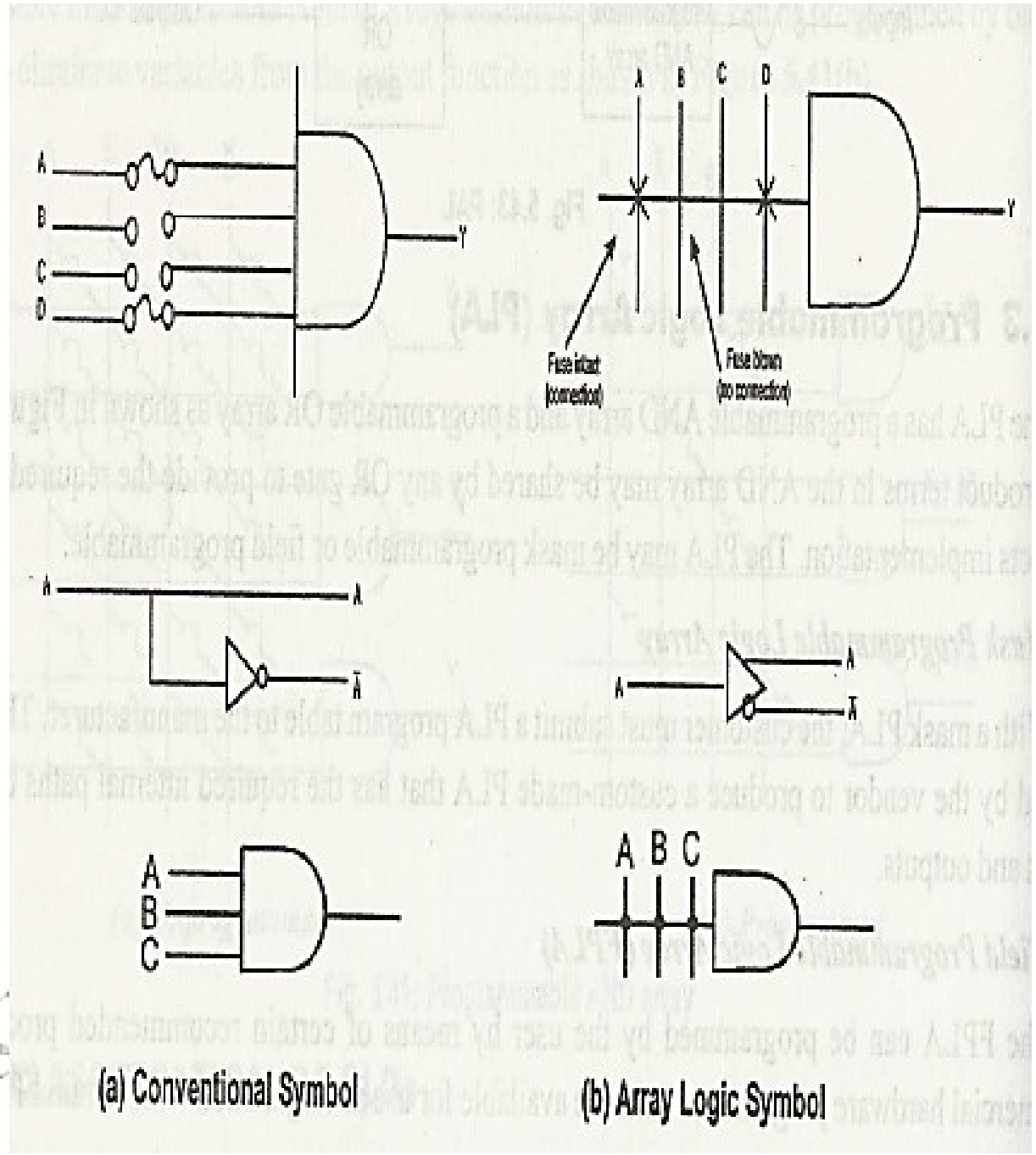
EEPROMs: Electrically Erasable Programmable ROMs. Have memory cells that can be erased and reprogrammed by exposure to electrical signals.

Erasure/Programming is now much easier. The processor can now "write" into the EEPROM.

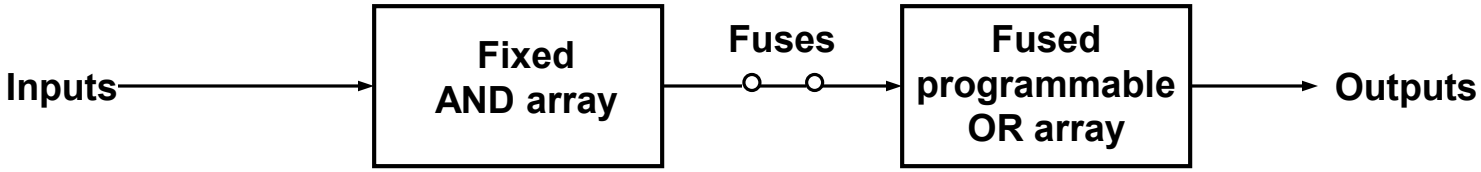
- Flash memory devices:
  - Memory cells are erased in blocks not one-by-one as in EEPROMs → Shorter life but faster operation

Programmable Logic Devices (PLD)

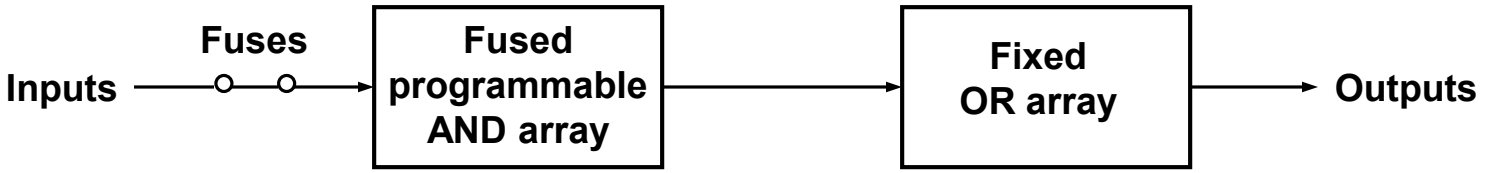
- Programmable Logic Devices (PLDs) are IC chips with internal logic gates connected by electronic fuses.
- These fuses can be ‘blown’ (by programming) to obtain different circuit configurations.
- Semi-customized chips that give high packing density at reasonable cost.
- Three classes of PLDs are :
  - ❖ Programmable Logic Array (PLA)
  - ❖ Programmable Read Only Memory (PROM)
  - ❖ Programmable Array Logic (PAL)


A
B
C
D
Y
A
B
C
D
Y
Fuse intact (connection)
Fuse blown (no connection)
A
Ā
A
Ā
A
B
C
A B C
(a) Conventional Symbol
(b) Array Logic Symbol

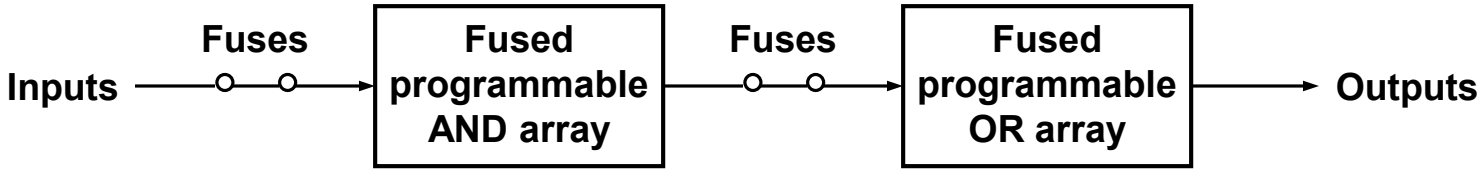
Programmable Logic Devices



Programmable Read Only Memory (PROM)



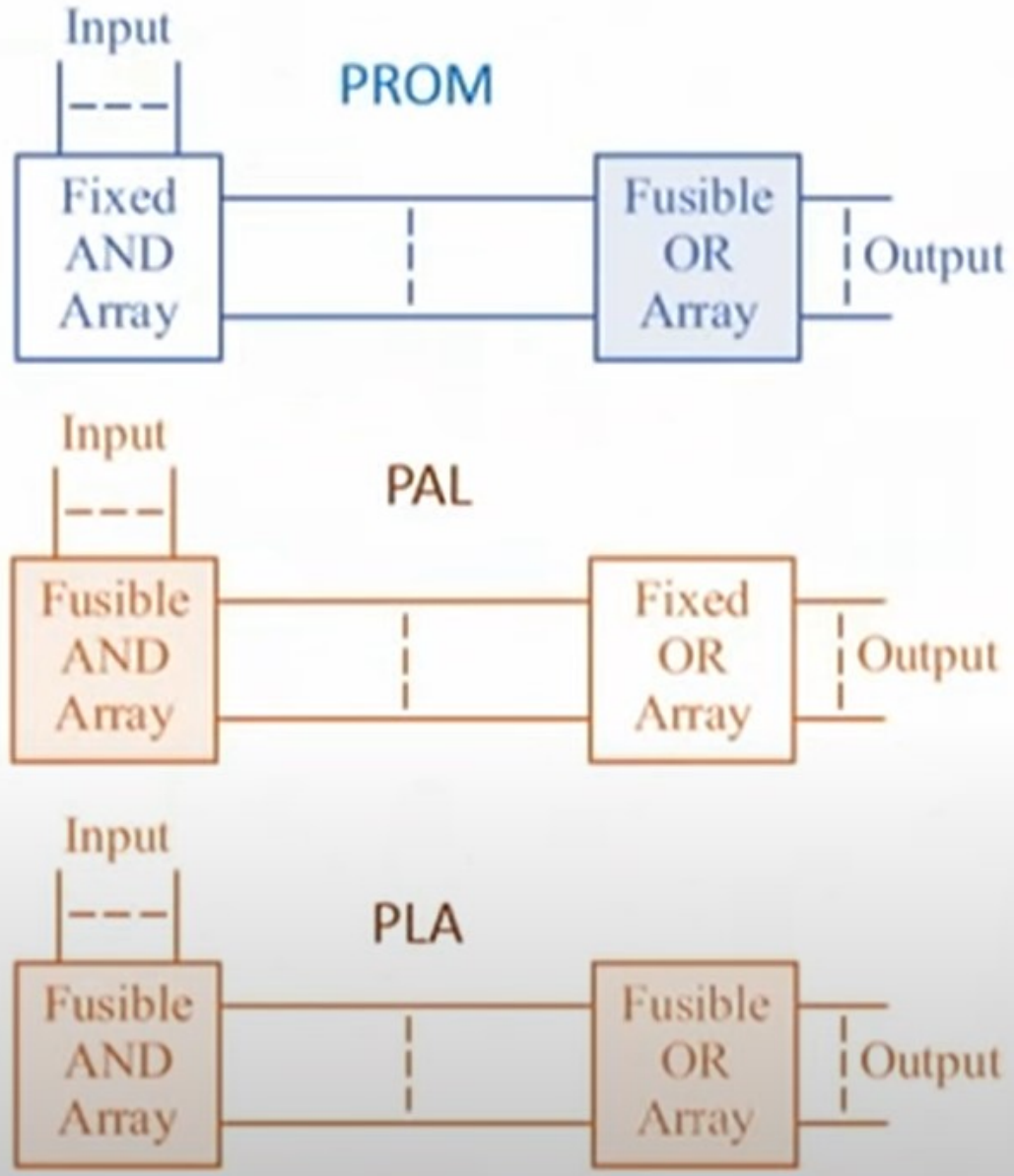
Programmable Array Logic (PAL)



Programmable Logic Array (PLA)

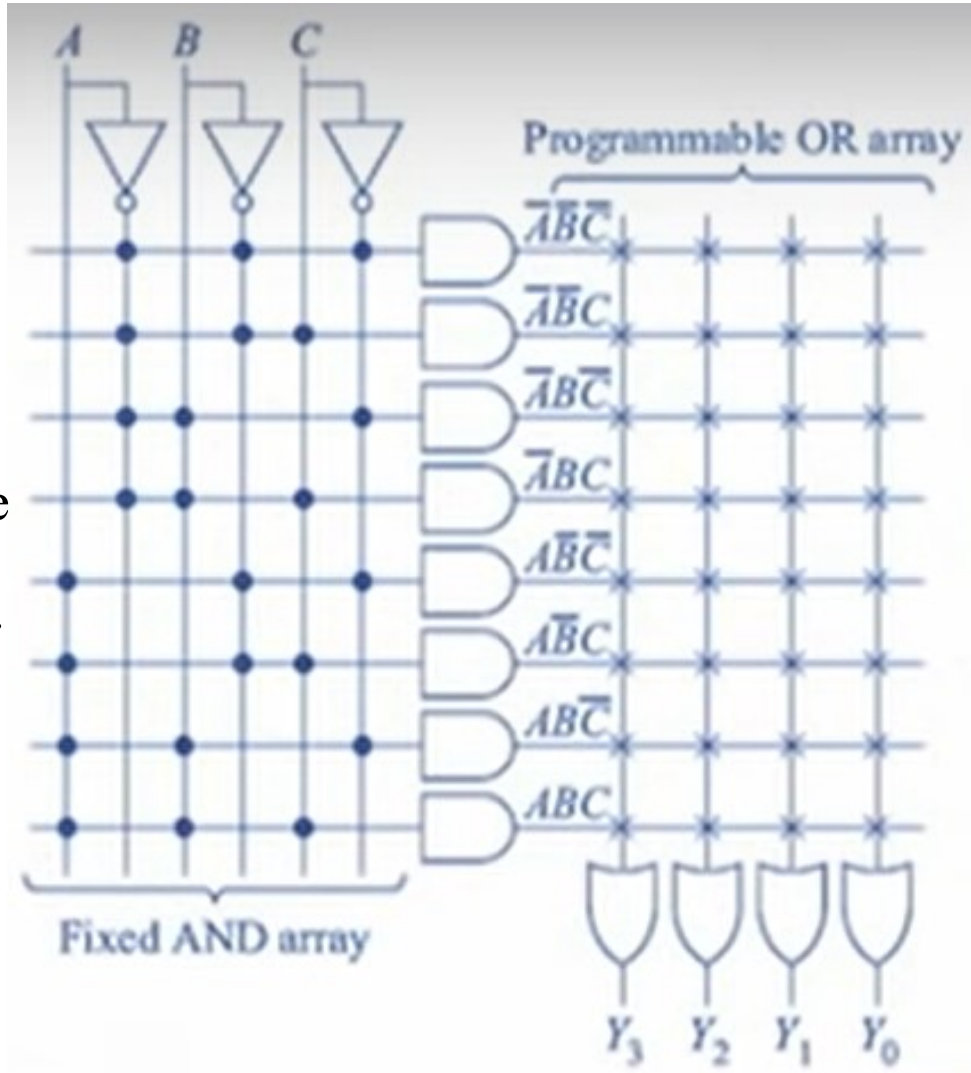
PROM to PAL, PLA

- In PROM (Programmable Read Only Memory), AND array is fixed and OR array is programmable.
- In PAL (Programmable Array Logic), OR array is fixed, AND array is programmable.
- In PLA (Programmable Logic Array), both AND and OR array are programmable.



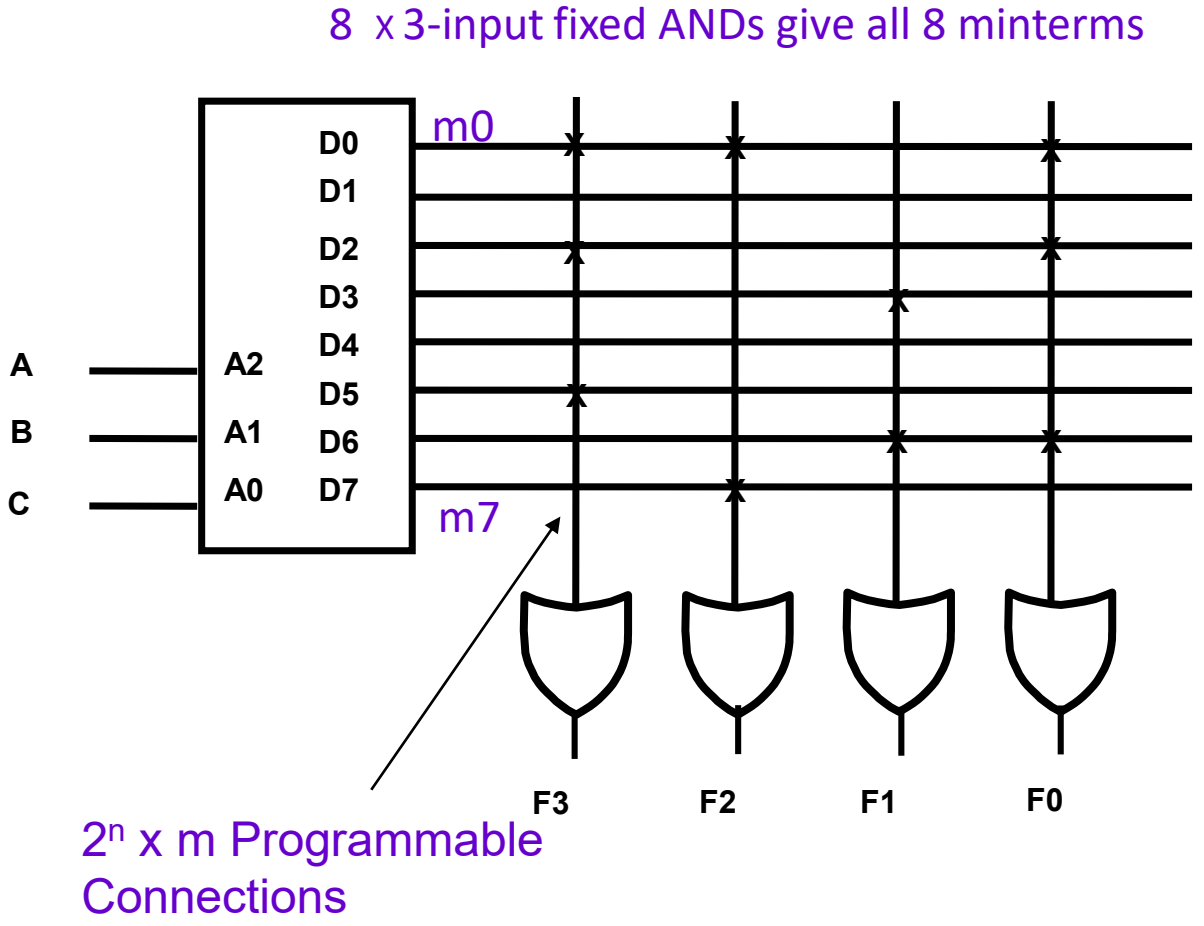
Programmable Read Only Memory (PROM)

- Read Only Memories (ROM) have:
  - n input (address) lines → 2^n locations → 2^n decoded minterms
  - m output lines (word width)
- **Fixed** array of 2^n AND gates implementing all the N-literal minterms.
- **Programmable** OR Array with m outputs lines to form up to m expressions, each being a sum of selected minterm.
- The program for a PROM is simply the multiple-output truth table to be implemented
  - If a 1 entry, a connection is made to the corresponding minterm for the corresponding output
  - If a 0, no connection is made
- Can be viewed as a *memory* with the inputs as *addresses* of *data* (output values), hence ROM or PROM names!



Programmable Read Only Memory (PROM)
Programmable sum of (fixed) minterms

- **Example:** 8 X 4 PROM (n = 3 input lines, m = 4 output lines)
- The fixed "AND" array is a "decoder" with 3 inputs and 8 outputs implementing minterms
- The programmable "OR" array uses a single line to represent all inputs to an OR gate. An "X" in the array corresponds to attaching the minterm to the OR
- **Read Example:**
- For input $(A_2,A_1,A_0)= 010$, output is $(F_3,F_2,F_1,F_0) = 1001$.

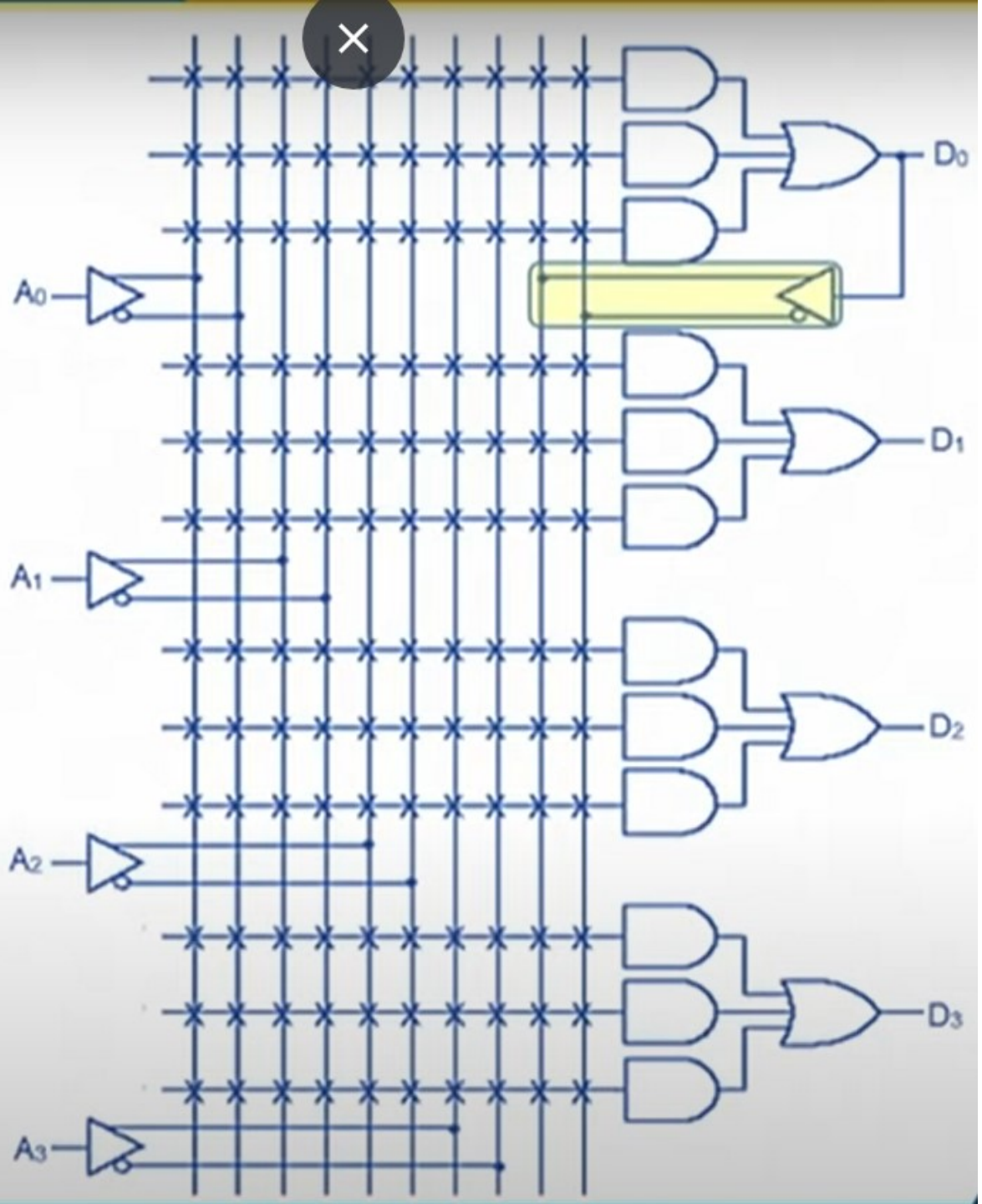


Advantages and Disadvantages

Advantages:	Can implement any function (all the minterms are available) Program is derived directly from the truth table (uses the canonical form)
Disadvantages:	Becomes complex for a large number of inputs n (# of ANDs = 2^n, each n-input wide) Does not support multi-level circuits (no outputs brought back as inputs)

PAL

- A representative Programmable Array Logic (PAL) circuit is shown.
- Each input is complemented as well as uncomplemented.
- Output comes from *three wide* AND-OR array sections.
- One of the output is fed back and is available to AND gate as input (complemented and uncomplemented).
- Each AND gate along the horizontal line has 10 programmable input connections that connect to vertical lines.



Programmable Logic Array (PLA)

- Combination of a programmable AND array followed by a programmable OR array.
- Example: Design a PLA to realise the following three logic functions and show the internal connections.

$f_1(A,B,C,D,E) = A'.B'.D' + B'.C.D' + A'.B.C.D.E'$

$f_2(A,B,C,D,E) = A'.B.E + B'.C.D'.E$

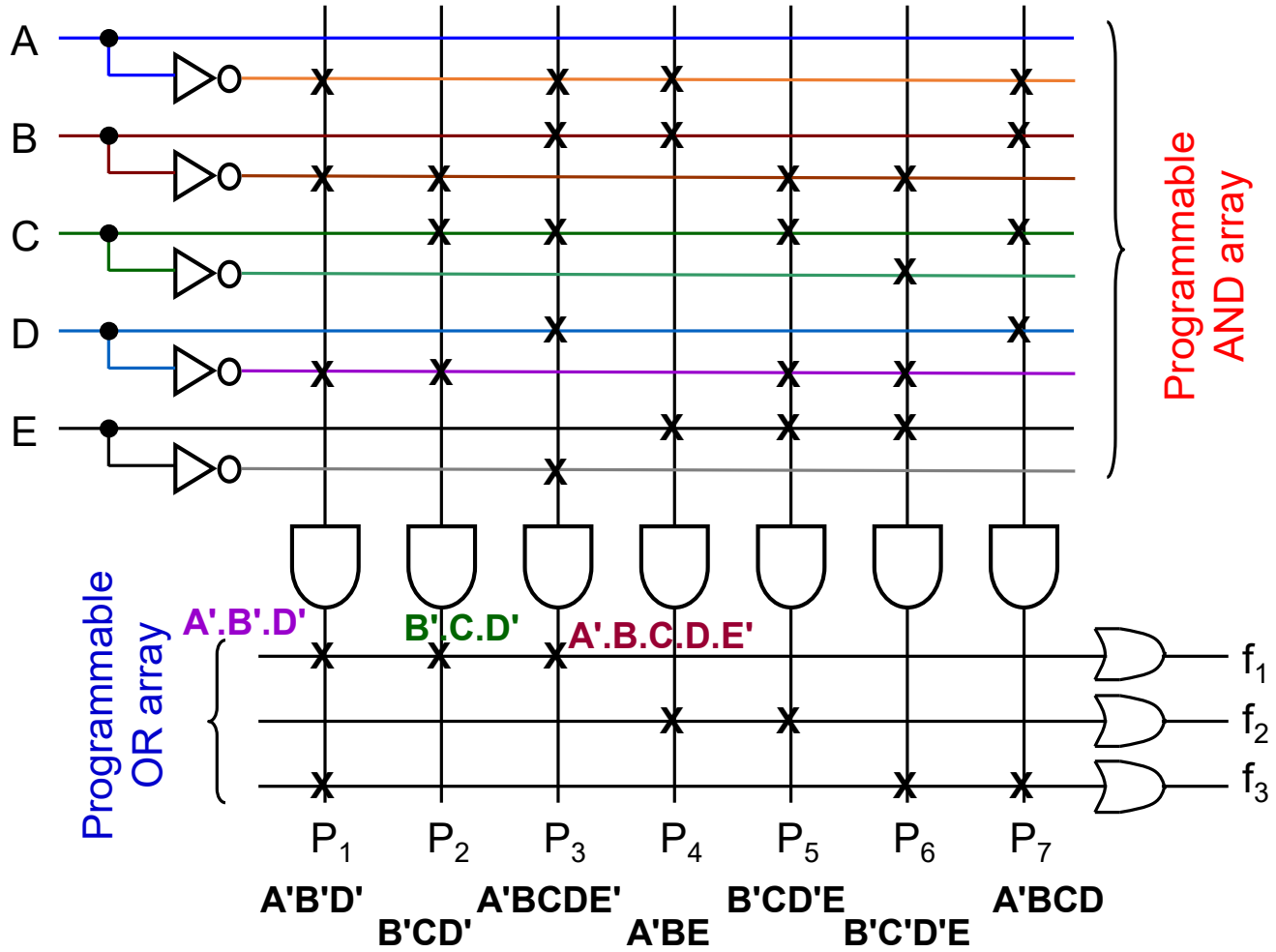
$f_3(A,B,C,D,E) = A'.B'.D' + B'.C'.D'.E + A'.B.C.D$

Realising Logic Functions with PLAs

$f_1(A,B,C,D,E) = A'.B'.D' + B'.C.D' + A'.B.C.D.E'$

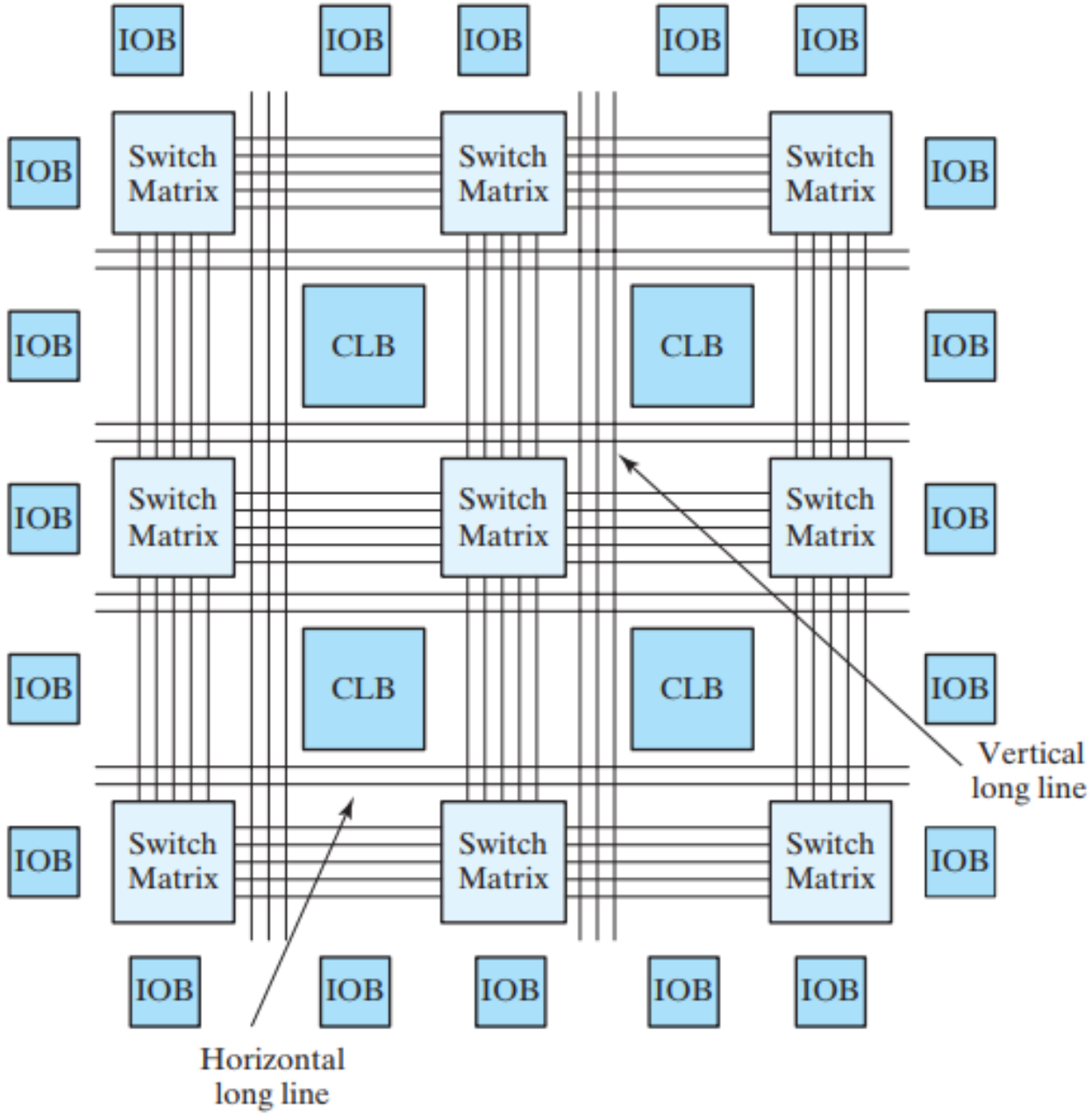
$f_2(A,B,C,D,E) = A'.B.E + B'.C.D'.E$

$f_3(A,B,C,D,E) = A'.B'.D' + B'.C'.D'.E + A'.B.C.D$



FPGA(Field Programmable Gate Array)

- The basic component used in VLSI design is the *gate array*. Arrays of one thousand to several hundred thousand gates are fabricated within a single IC chip, depending on the technology used.
- A field-programmable gate array (FPGA) is a VLSI circuit that can be programmed at the user's location.
- A typical FPGA consists of an array of millions of logic blocks, surrounded by programmable input and output blocks and connected together via programmable interconnections.
- The performance of each type of device depends on the circuitcontained in its logic blocks and the efficiency of its programmed interconnections.



FPGA(Field Programmable Gate Array)

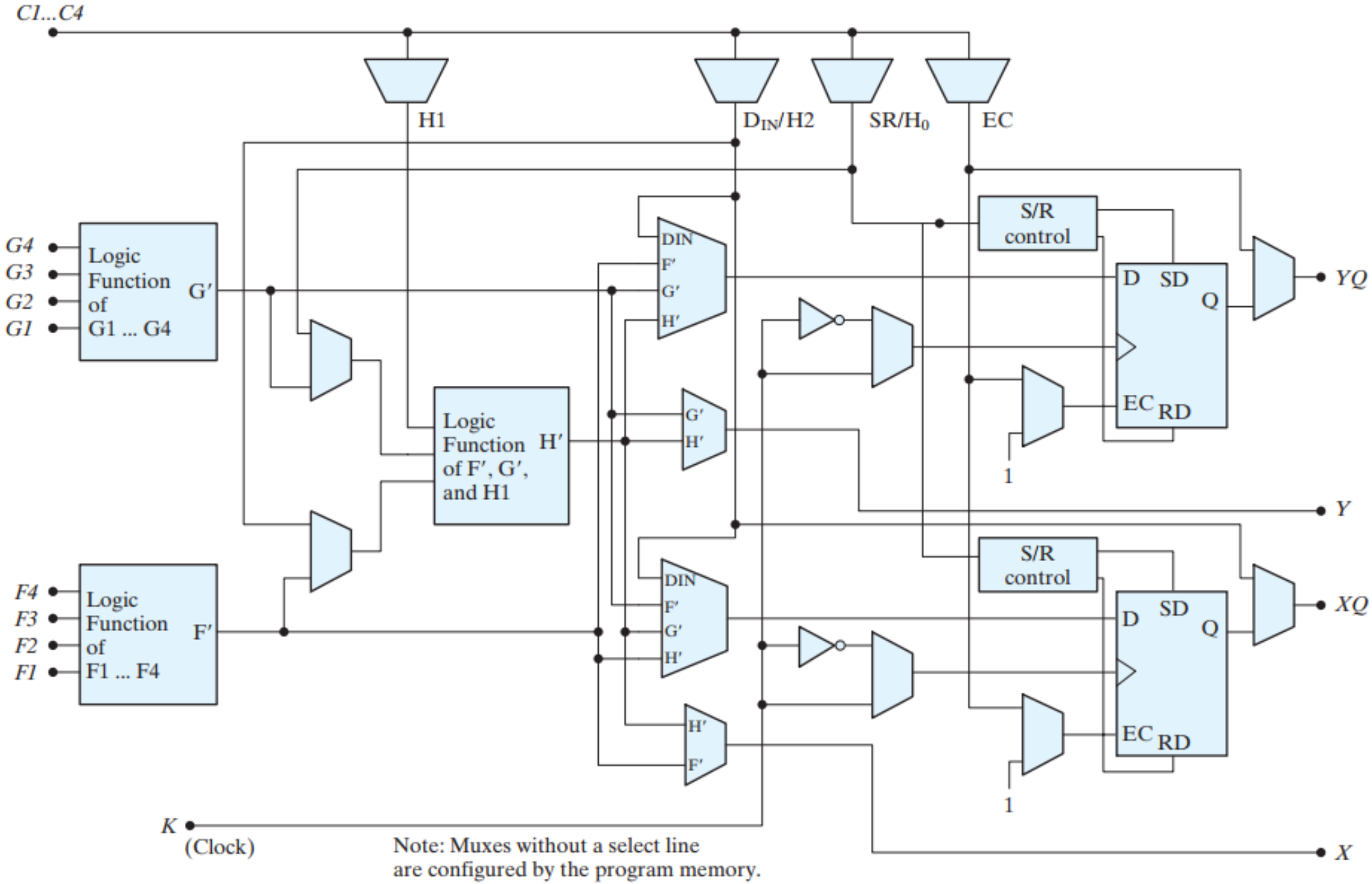
- A typical FPGA logic block consists of lookup tables, multiplexers, gates, and flip-flops.
- A lookup table is a truth table stored in an SRAM and provides the combinational circuit functions for the logic block.
- The design with PLD, CPLD, or FPGA requires extensive computer-aided design (CAD) tools to facilitate the synthesis procedure.

Configurable Logic Block(CLB):

Each CLB consists of a programmable lookup table, multiplexers, registers, and paths for

control signals.

- Two of the function generators (F and G) of the lookup table can generate any arbitrary function of four inputs, and the third (H) can generate any Boolean function of three inputs.
- The H-function block can get its inputs from the F and G lookup tables or from external inputs. The three function generators can be programmed to generate
  - (1) three different functions of three independent sets of variables (two with four inputs and one with three inputs one function must be registered within the CLB),
  - (2) an arbitrary function of five variables,
  - (3) an arbitrary function of four variables together with some functions of six variables, and
  - (4) some functions of nine variables.


C1...C4
H1
DIN/H2
SR/H0
EC
G4
G3
G2
G1
Logic Function of G1 ... G4
G′
Logic Function of F′, G′, and H1
H′
F4
F3
F2
F1
Logic Function of F1 ... F4
F′
DIN
F′
G′
H′
S/R control
D
SD
Q
EC
RD
1
YQ
Y
XQ
X
K
(Clock)
Note: Muxes without a select line are configured by the program memory.