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B.Tech. DEGREE EXAMINATION, JUNE 2023

Third Semester

18ECC103J - DIGITAL ELECTRONIC PRINCIPLES

(For the candidates admitted during the academic year 2018-2019 to 2021-2022)

Note:

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40 minutes.
ii. **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours **Max. Marks: 100**

Part - A (20 × 1 Marks = 20 Marks)

Answer **All** Questions

		Marks	BL	CO
1.	The digital logic family which has minimum power dissipation is (A) TTL (B) RTL (C) DTL (D) CMOS	1	1	2
2.	The time required for a pulse to change from 10 to 90 percent of its maximum value is called (A) Rise Time (B) Decay time (C) Propagation time (D) Operating Speed	1	1	2
3.	The figure of merit of the logic family is often measured in unit of (A) Nanoseconds (B) Picojoules (C) Megahertz (D) Microwatts	1	1	2
4.	On a K-Map, grouping the 0s produces (A) PoS expression (B) don't care condition (C) AND-OR expression (D) SoP expression	1	1	1
5.	Simplified form of A + A'B +A'B'C +A'B'C'D is equal to (A) A (B) A+B (C) A+B+C+D (D) A+B+C	1	2	1
6.	The following switching function is to be implemented using multiplexer $f = \sum m(1, 2, 4, 8,14, 45)$. What is the size of multiplexer? (A) 32-to-1 line (B) 64-to-1 line (C) 16-to-1 line (D) 8-to-1 line	1	2	3
7.	Full adder circuit adds the number of bits at a time (A) 1 (B) 2 (C) 3 (D) 4	1	1	3
8.	In a 4-bit full adder, the carry propagation delay is (A) Increases in direct ratio to the total number of full-adder stages, but is not a factor in limiting the speed of arithmetic operations (B) Decreases in direct ratio to the total number of full-adder stages (C) Normally not a consideration because the delays are usually in the nanosecond range (D) Cumulative for each stage and limits the speed at which arithmetic operations are performed	1	2	3
9.	In a two-bit magnitude comparator, the logical expression for A > B is (A) A1 B1' + A0 B1'B0' + A1 A0 B0' (B) A1' B1 + A0' B1B0' + A1 A0' B0' (C) A1 B1 + A0 B1B0 + A1 A0 B0 (D) A1' B1 + A0' B1B0 + A1' A'0 B0	1	2	3

10.	What is the simplified form of the following Boolean function F= ∑(4,6,8,10,11,12,15) using K-map is (A) ACD+AB'D'+A'BD' (B) AC'D+A'CD'+AB'D'+A'BD' (C) AC'D'+ACD+AB'D'+A'BD' (D) AC'D+ACD+A'BD'+AB'CD'	1	2	1
11.	A flip-flop is a binary storage device capable of storing bit of information (A) 1 (B) 2 (C) 3 (D) 4	1	1	4
12.	The characteristic equation of J-K flip-flop is (A) Q(n+1) =JQ(n)+K'Q(n) (B) Q(n+1) =JQ'(n)+K'Q(n) (C) Q(n+1) =JQ'(n)+KQ(n) (D) Q(n+1) =J'Q(n)+KQ'(n)	1	1	4
13.	How many flip-flops are required to construct a decade counter? (A) 4 (B) 2 (C) 3 (D) 10	1	1	4
14.	A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is (A) 12 ns (B) 48 ns (C) 60 ns (D) 24 ns	1	5	4
15.	The minimum number of MOS Transistor required to be make a dynamic RAM Cell is (A) 1 (B) 2 (C) 3 (D) 4	1	1	5
16.	A ROM which can be programmed is called a (A) MROM (B) EEPROM (C) EPROM (D) PROM	1	1	5
17.	The decimal equivalent of the highest possible address for an 8-bit address bus is (A) 8 (B) 127 (C) 256 (D) 255	1	1	5
18.	Addressing of a 32K x16 memory is realized using a single decoder. The minimum number of AND gates required to the decoder (A) 2^{19} (B) 2^{15} (C) 2^{32} (D) 2^{8}	1	5	5
19.	A PLA is (A) Mask programmable (B) field programmable (C) can be programmed by a user (D) can be erased and programmed	1	1	5
20.	Mod 2 counter and mod 17 counter are cascaded. The modulus of the resultant counter will be (A) mod 17 (B) mod 9 (C) mod 2 (D) mod 34	1	2	4

Part - B (5 × 4 Marks = 20 Marks)

Answer **any 5** Questions

		Marks	BL	CO
21.	Define hamming code and how does it work?	4	3	1
22.	How a transistor can act as a switch? Discuss the characteristics of digital ICs.	4	3	2
23.	Give the truth table of a 3 to 8 decoder & draw its circuit diagram.	4	3	3
24.	Along with a diagram, explain the table for the operation of a right shift serial input serial output shift register.	4	4	4
25.	What is a programmable logic array? How it differs from ROM?	4	2	5

26.	How CMOS can work as an inverter explain with a circuit diagram.	4	2	2
27.	Describe the operation of a Mod-10 counter using a JK flip flop.	4	3	4

Part - C (5 × 12 Marks = 60 Marks)

Answer **All** Questions

		Marks	BL	CO
28.	a. Along with a diagram, discuss how 3 input NAND gate functioning can be achieved using Transistor Transistor Logic (TTL). **(OR)** b. Along with a diagram, discuss how 3 input NOR/OR gate functioning can be achieved using Emitter Coupled logic (ECL).	12	4	2
29.	a. Implement the following two Boolean functions using PLA: F1 (A, B, C) = ∑ (0, 1, 2, 4) F2 (A, B, C) = ∑ (0, 5, 6, 7) **(OR)** b. Implement the following Boolean functions using PAL: W (A, B, C, D) = ∑ (2, 12, 13) X (A, B, C, D) = ∑ (7, 8, 9, 10, 11, 12, 13, 14, 15) Y (A, B, C, D) = ∑ (0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15) Z (A, B, C, D) = ∑ (1, 2, 8, 12, 13)	12	4	5
30.	a. State the truth table of a JK flip flop. Use it to derive (i) Characteristics table (ii) State equation (iii) Excitation table (iv) State diagram. **(OR)** b. Along with a diagram discuss how a Master Slave flip flop solves the problem of race around the condition.	12	4	4
31.	a. Simplified form of the following Boolean function F= ∑ (0,1,3,7,8,9,11,15) using Quine McCluskey method. **(OR)** b. State and prove De Morgan's Theorem using the truth table.	12	4	1
32.	a. What are combinational circuits? Along with a diagram, discuss the operation of a 1x8 de-multiplexer. **(OR)** b. Give the truth table of an 8 to 3 Encoder & draw its circuit diagram.	12	3	3

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