Department of ECE

21ECC203T Digital Logic Design

Assignment 2

Each Question Carry 4 marks

1. A, B, B_{in}, D and B_{out} are respectively the minuend, the subtrahend, the BORROW-IN, the DIFFERENCE output and the BORROW-OUT in the case of a full subtractor. Determine the bit status of D and B_{out} for the following values of A, B and B_{in}:

(a) A = 0, B = 1, B_{in} = 1

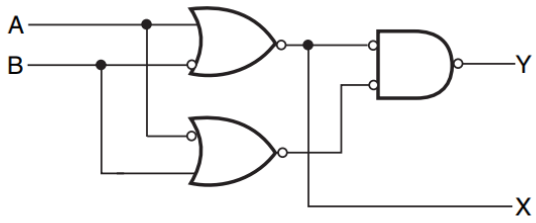
(b) A = 1, B = 1, B_{in} = 0

(c) A = 1, B = 1, B_{in} = 1

(d) A = 0, B = 0, B_{in} = 1

2. Determine the number of half and full adder circuit blocks required to construct a 64-bit binary parallel adder. Also, determine the number and type of additional logic gates needed to transform this 64-bit adder into a 64-bit adder–subtractor.

3. Prove that the logic diagram of Fig. performs the function of a half-subtractor provided that Y represents the DIFFERENCE output and X represents the BORROW output.



4. Implement the Boolean function with a suitable Multiplexer f (A, B, C) = $\prod$ (1, 2, 5)

5. Design a 10 line Decimal to BCD Priority Encoder

6. A combinational circuit is defined by F = $\sum$ (0, 2, 5, 6, 7). Hardware implement the Boolean function F with a suitable decoder and an external OR/NOR gate having the minimum number of inputs.