SRM INSTITUTE OF SCIENCE AND TECHNOLOGY
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Ans.1) A, B, B_{in}, D and B_{out} are respectively the minuend, the subtrahend, the BORROW - IN, the DIFFERENCE output and the Borrow - out in the case of full subtractor. Determine the bit status of D and B_{out} for the following values of A, B and B_{in}.

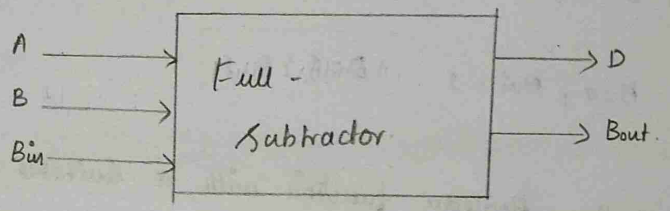
a). A = 0, B = 1, B_{in} = 1.

b). A = 1, B = 1, B_{in} = 0

c). A = 1, B = 1, B_{in} = 1.

d). A = 0, B = 0, B_{in} = 1.

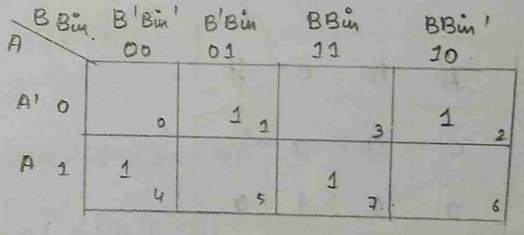
BLOCK DIAGRAM.



TRUTH TABLE FOR FULL SUBTRACTOR,

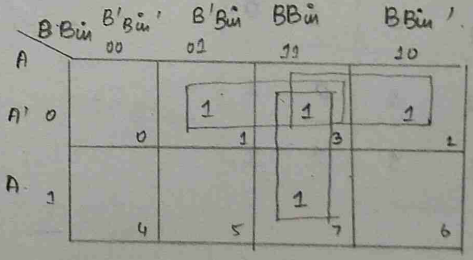
B	A	B	B_{in}	D	B_{out}
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1.

(i). Difference,



$D = AB'B_{in}' + A'B'B_{in} + ABB_{in} + A'BB_{in}'$

(ii). Borrow,



$D = A'B_{in} + BB_{in} + A'B.$

$D = B_{in}(A' + B) + A'B.$

a). A=0, B=1, Bin = 1. D=0 ; B=1

b). A=1, B=1, Bin = 0 D=0 ; B=0

c). A=1 ; B=1, Bin = 1 D=1 ; B=1

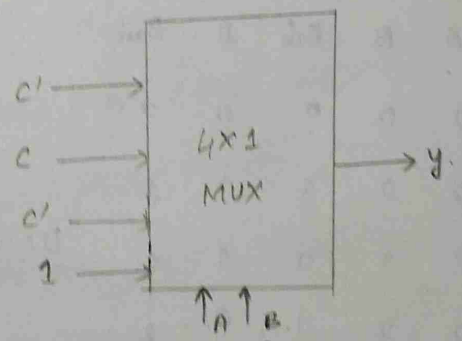
d). A=0, B=0, Bin = 1 D=1 ; B=1.

4). Implement the Boolean function with a Suitable multiplexer,

$f(A,B,C) = \Pi(1,2,5)$. Π represents Maxterm,

where output are represented by 0.

D	A	B	C	y	
0	0	0	0	1	→ y = c'
1	0	0	1	0	
2	0	1	0	0	→ y = c
3	0	1	1	1	
4	1	0	0	1	→ y = c'
5	1	0	1	0	
6	1	1	0	1	→ y = 1.
7	1	1	1	1	

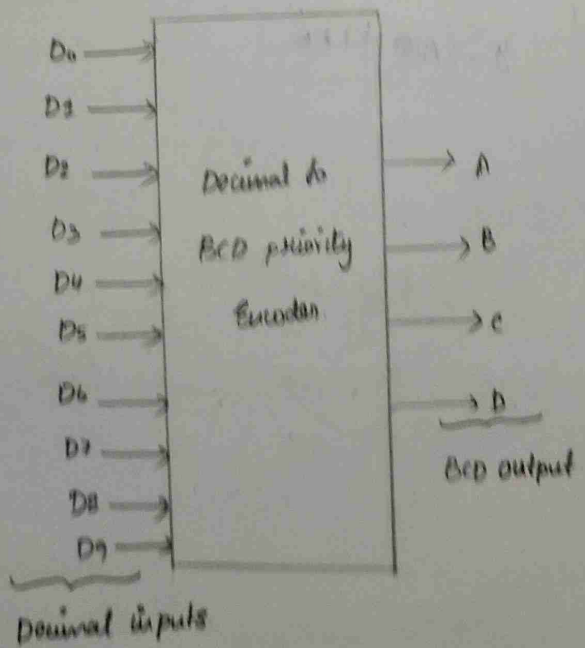


4x1 Multiplexer

8) Design a 10 line decimal to BCD priority Encoder.

											8	4	2	1
$D_{Decimal}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	A	B	C	D
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	X	X	0	0	0	0	0	0	0	0	0	0	0	1
2	X	X	1	0	0	0	0	0	0	0	0	0	1	0
3	X	X	X	1	0	0	0	0	0	0	0	0	1	1
4	X	X	X	X	1	0	0	0	0	0	0	1	0	0
5	X	X	X	X	X	1	0	0	0	0	0	1	0	1
6	X	X	X	X	X	X	1	0	0	0	0	1	1	0
7	X	X	X	X	X	X	X	1	0	0	0	1	1	1
8	X	X	X	X	X	X	X	X	1	0	1	0	0	0
9	X	X	X	X	X	X	X	X	X	1	1	0	0	1

Block diagram.



6). A combinational circuit is defined by $F = \Sigma(0, 2, 5, 6, 7)$. Hardware implement the Boolean function F with a suitable decoder and an external OR/NOR gate having the minimum number of inputs.

D	A	B	C	y.
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1.

$y = A'B'C' + A'BC' + AB'C + ABC' + ABC.$

$= A'C'(B'+B) + AB(C+C') + AB'C$

$= A'C' + AB + AB'C.$

$\boxed{y = A'C' + A(B+B'C).}$

$y = A'B'C' + A'BC' + AB'C + ABC' + ABC.$

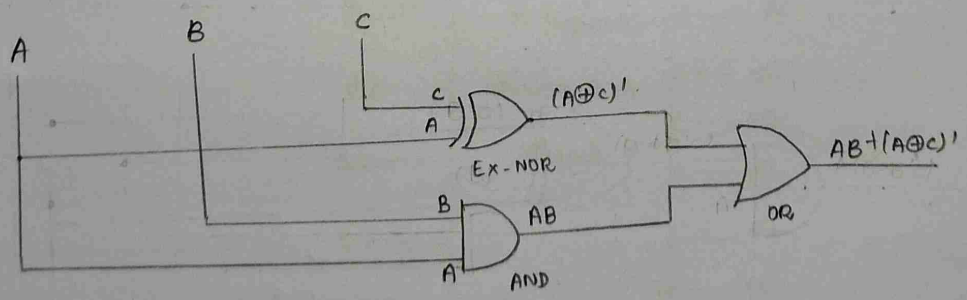
$= A'C'(B'+B) + AB(C'+C) + AB'C.$

$= A'C' + A(B+B'C) = A'C' + A(B+C).$

$x(y+z) = xy+yz$

$= A'C' + AB + AC.$

$\boxed{y = (A \oplus C)' + AB.}$



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21. Determine the number of half and full adder circuit blocks required to construct a 64-bit binary parallel adder. Also, determine the number and type of additional logic gates needed to transform this 64 bit adder into a 64-bit adder-subtractor.

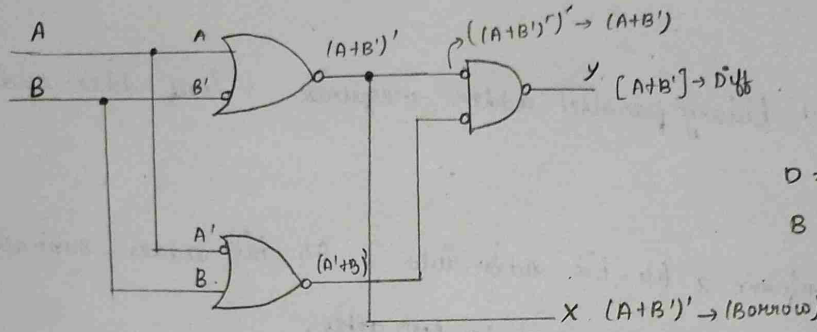
(i). An 64 bit binary parallel adder requires 1 half adder and 63 full adder.

(ii). To Transform a 64-bit adder into a 64-bit adder-subtractor, we need to add 64 XOR gates and 64 AND gates.

- XOR Gates : 64
- AND Gates : 64
- The total number of additional logic gates is 128.

[64 bit adder] + [64 XOR gates] + [64 AND gates] = 64-bit adder subtractor.

31. Prove that the logic diagram of fig performs the function of half subtractor provided that y represents the difference output and x represents the Borrow output.



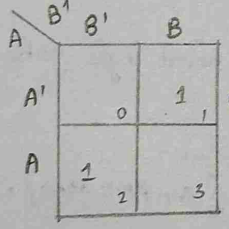
D = A+B'

B = (A+B')'

Design of half - subtractor,

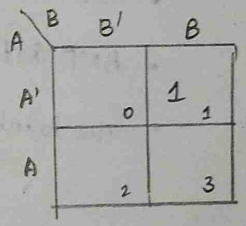
A	B	diff	Bor.
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

k-map. for difference.



y = A'B + AB'

EX-NOR.



y = A'B.

AND.

For Borrow = A'B

For Difference = A'B + AB'.

From the above logic diagram, it is seen that y (Difference) is A ⊕ B that is Ex-OR, and x (Borrow) is A'B (AND Gate).

Hence, it is proved.