Course 21ECC203J Course Code	Sourse Digital Logic Design		Course L T P C Category 3 0 1 3
Pre-requisite Courses 21EES101T	Co- requisite NIL Courses		Progressive Courses 21ECC333L
Course Offering Department E	Electronics and Communication Engineering	Data Book / Codes / Standards	NIL

Course Le	Course Learning Rationale (CLR): The purpose of learning this course is to:				Program Outcomes (PO)	m Ou	tcome	es (P(<u>(</u>				٩	oaram	
CLR-1:	Understand binary codes, able to simplify Boolean logic expressions and understand the basic TTL and CMOS gates operate at the component level	-	2 3 4 5 6 7 8 9 10 11 12	3	4	2		∞	6	9	7	12	of the	Specific outcomes	
CLR-2:	gates and MSI circuits														
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CEV-3	and able to design of sequential logic circuits.	Engi	U Proble /d	esigni. evel lin	esti N	po B	е <u>-</u>		idual		J O F	ā			
CI B.A.	Able to design application level circuits and adopt systematic approach with the use of Sequence	neeri	7 6 20 1	omen ga	tion T	<u>a</u> .	e de	EH	<u>۔</u> ∞ ا	Comm	Mgt	oug -	PSOP	SOPS	
	detector,	Know	Analyst (<u> </u>	<u> </u>	sa si	Sis	8	5 E	nc Su	ع <u>ن</u> نا ت∞	earni .earni	·,·)))
CLR-5 :	Know how to implement logic circuits using PLDs	edge	<u>⊼ ≃</u> ^	olinio S	6	<u>a</u>	aine Figure		Wor			<u></u>			
				<u>5</u>	<u> </u>			_	_						

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Course (Course Outcomes (CO); At the end of this course, learners will be able to:													
CO-1:	Simplify Boolean expressions; implement gates as well as other types of IC devices using two major 3 - IC technologies, TTL and CMOS.	3	1	,	,	3	1	1			1	3	'	
CO-2:	Identify eight basic types of fixed-function combinational logic functions and demonstrate how the devices / circuits can be used in building complete digital systems such as computers.	1	2	2 2	1	က	1	1	1	1	1		1	1
CO-3:	Understand and design sequential circuits using several types of flip-flops		2	2 2 - 3	-	3	1	-	-			-	•	
CO-4:	Design of advanced circuit and Design the advanced sequential logic circuits.	ı	2	2	-	- 3	-	-	-	_		 	-	
CO-5:	Implement multiple output combinational logic circuits using PLDs; Explain the operation of a CPLD and FPGA.	1	2	2 2	1	3	1	1		1	1		1	

Unit-1: Basics and Logic Family

Boolean algebra, Karnaugh Map - Quine McClusky minimization technique(4 -variable) - Logic Families:-Introduction - TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out, CMOS

Unit-2: Combinational circuit
 Combinational logic circuits: Half adder – Full Adder – Half subtractor - Full subtractor – Parallel binary adder - 2's complement subtraction using parallel adders - Multiplexer/Demultiplexer – decoder - encoder -code converters - Magnitude Comparator.

Unit-3: Sequential Circuits

Flip-flop and Latch: SR latches- JK flip-flop, T flip-flop, D flip-flop-Master-slave JK flip-flop- Register Counters- Ring counter, Johnson counter-Shift registers (SISO, SIPO, PISO, PIPO)--Universal shift register-Counters:-Asynchronous/Ripple counters--Synchronous counters-Modulus-n Counter -Up-Down counter- -State reduction-State assignment

Unit-4: Advanced Combinational, Sequential logic

Advance sequential logic:-- Mealy and Moore model- Analyze and design synchronous sequential circuits - FSM - Sequence detector - Vending Machine - Advanced digital 9 Hours circuits:- Hamming code - Delay in a ripple carry adder - Carry Look Ahead adder -2 Bit Multiplier

unit-5: PLD's and Memory

9 Hours RAM Memory decoding-ROM--Basic concepts:-Programmable Logic Devices (PLDs):-Basic concepts-PROM as PLD-Programmable Array Logic PAL)--Programmable Logic Array (PLA)-FPGA

1. Morris Mano M, Michael D. Ciletti, Digital Design with an Introduction to the Verilog HDL, 5th ed., Pearson Education, 2014
2. Charles H Roth (Jr), Larry L. Kinney, Fundamentals of Logic Design, 5th ed., Cengage Learning India Edition, 2010

 Ronald J. Tocci, Digital System Principles and Applications, 10th ed., Pearson Education, 2009
 Donald P Leach, Albert Paul Malvino, Goutam Saha, Digital Principles and

3. Thomas L. Floyd, Digital Fundamentals, 10th ed., Pearson Education, 2013 Applications, 6th ed., TataMcgraw Hill, 2008

			Continuous Learning	Continuous Learning Assessment (CLA)			0,1000
	Bloom's Level of Thinking	Fon CLA-1 Avera (5	Formative Average of unit test (50%)	Life Long Learning CLA-2 – (10%)	y Learning 1-2 – 1%)	Final E (40%)	Summative Final Examination (40% weightage)
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	15%		15%		15%	
Level 2	Understand	72%	•	50%	•	25%	1
Level 3	Apply	30%		25%		30%	
Level 4	Analyze	30%	•	72%	•	30%	-
Level 5	Evaluate		•	10%	•		
Level 6	Create	•	•	2%	•	•	1
	Total	11	700 %	101	7000%	4	400 %

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
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	2.	2.