SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

18ECC201J – ANALOG ELECTRONIC CIRCUITS

LABORATORY MANUAL

SEMESTER IV

SRM Institute of Science and Technology ,Tiruchirappalli, Tamilnadu-621105.

List of Experiment

Lab 1: Learning to design BJT amplifier and oscillator circuits

Lab 2: Design and analyze BJT amplifier (CC & CB) configurations

Lab 3: Design and analyze multistage amplifier configurations

Lab 4: Design & analyze differential amplifier

Lab 5: Design and analyze negative feedback amplifier configurations

Lab 6: Design and analyze RC oscillators

Lab 7: Design and analyze LC oscillators

Lab 8: Classes of power amplifier

Lab 9: Design and analyze FET CS amplifier with active load

Lab 10: Design and analyze BJT CE amplifier with active load

EX.NO:1

DATE:

LEARNING TO DESIGN AMPLIFER AND OSCILLATIOR CIRCUITS

AIM:

To design a Common Emitter amplifier with self bias and determine the voltage gain to plot the frequency response.

a. Gain of the amplifier
b. Bandwidth of the amplifier
c. Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	60kΛ, 1kΛ, 2.2kΛ ,10kΛ	Each 1
4	Power supply	(0-30)V	1
5	Transistors	BC 107	1
6	Capacitors	10μF	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A common emitter amplifier is type of BJT amplifier which increases the voltage level of the applied input signal V_{in} at output of collector. The CE amplifier typically has a relatively high input resistance (1 - 10 KΩ) and a fairly high output resistance. Therefore it is generally used to drive medium to high resistance loads. It is typically used in applications where a small voltage signal needs to be amplified to a large voltage signal like radio receivers.

The input signal Vin is applied to base emitter junction of the transistor and amplifier output Vo is taken across collector terminal. Transistor is maintained at the active region by using the resistors R1,R2 and Rc. A very small change in base current produces a much larger change in collector current.

The output Vo of the common emitter amplifier is 180 degrees out of phase with the applied the input signal $V_{in.}$

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CE amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CE amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for at least 20 different values for the considered range.
5. The voltage gain is calculated as

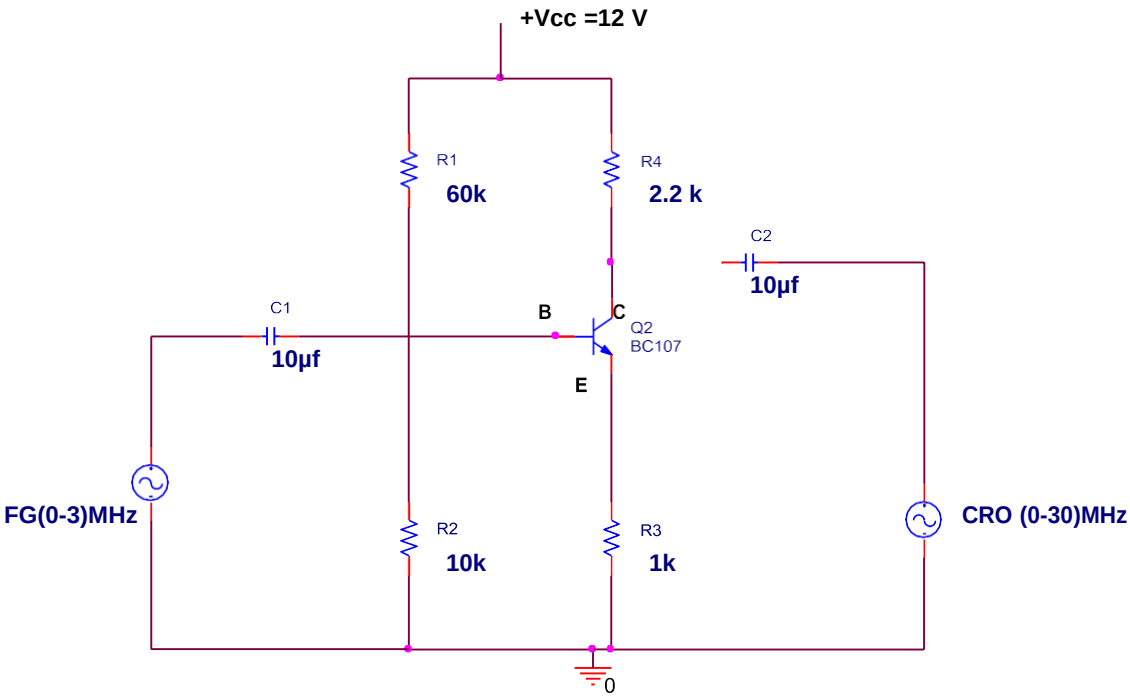
$$\mathbf{A_v = 20\log (V_0/V_i)\ dB}$$

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.

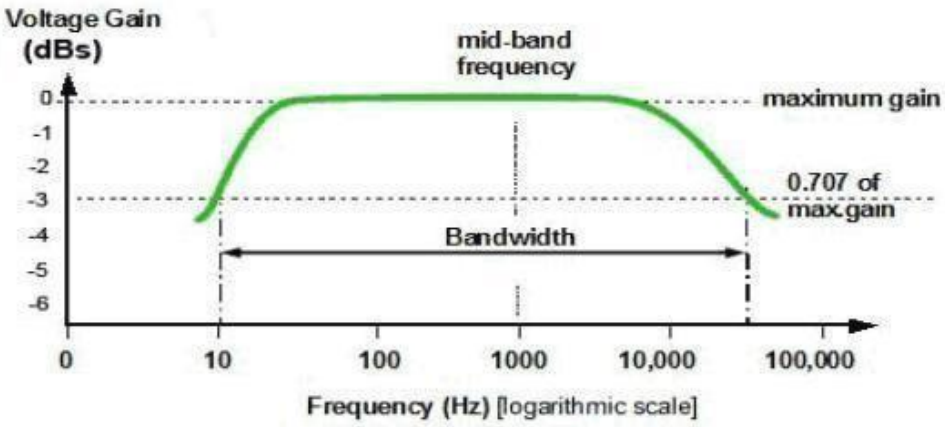
Bandwidth, BW = f_2-f_1

where
f_1 lower cut-off frequency
f_2 upper cut-off frequency

COMMON EMITTER CIRCUIT DIAGRAM:



MODEL GRAPH :



RESULT:

Thus the Common Emitter amplifier was constructed .

EX.NO:2(a)
DATE:

DESIGN AND ANALYZE FREQUENCY RESPONSE OF COMMON COLLECTOR AMPLIFILER

AIM:

To design a Common Collector amplifier with self bias and determine the voltage gain to plot the frequency response.

a. Gain of the amplifier
b. Bandwidth of the amplifier
c. Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	60kΛ, 1kΛ, 2.2kΛ ,10kΛ	Each 1
4	Power supply	(0-30)V	1
5	Transistors	BC 107	1
6	Capacitors	10μF	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A common collector amplifier is type of BJT amplifier which increases the voltage level of the applied input signal V_{in} at output of collector.

The CC amplifier typically has a relatively high input resistance (1 - 10 KΩ) and a fairly high output resistance. Therefore it is generally used to drive medium to high resistance loads. It is typically used in applications where a small voltage signal needs to be amplified to a large voltage signal like radio receivers.

The input signal Vin is applied to base emitter junction of the transistor and amplifier output Vo is taken across collector terminal. Transistor is maintained at the active region by using the resistors R1,R2 and Rc. A very small change in base current produces a much larger change in collector current

The output Vo of the common emitter amplifier is 180 degrees out of phase with the applied the input signal V_{in}

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CC amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CC amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for at least 20 different values for the considered range.
5. The voltage gain is calculated as

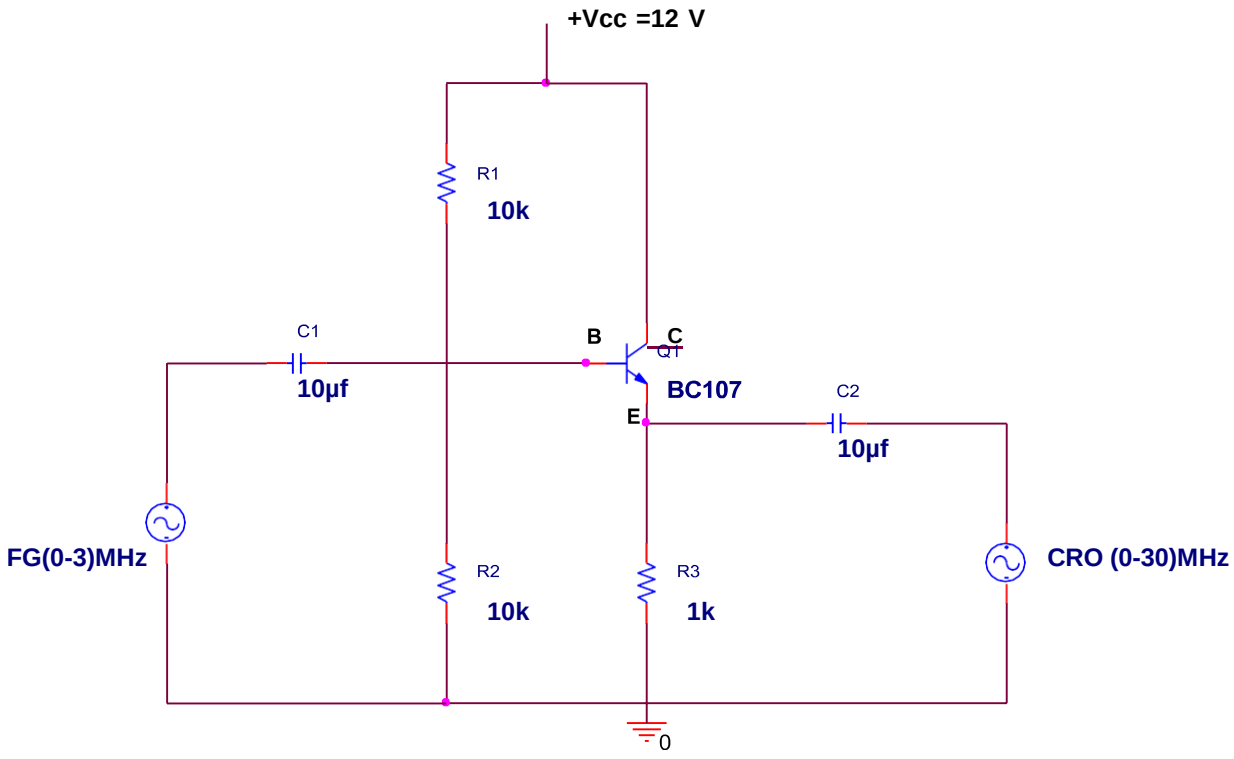
$$\mathbf{A_V = 20\log (V_0/V_i)\ dB}$$

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

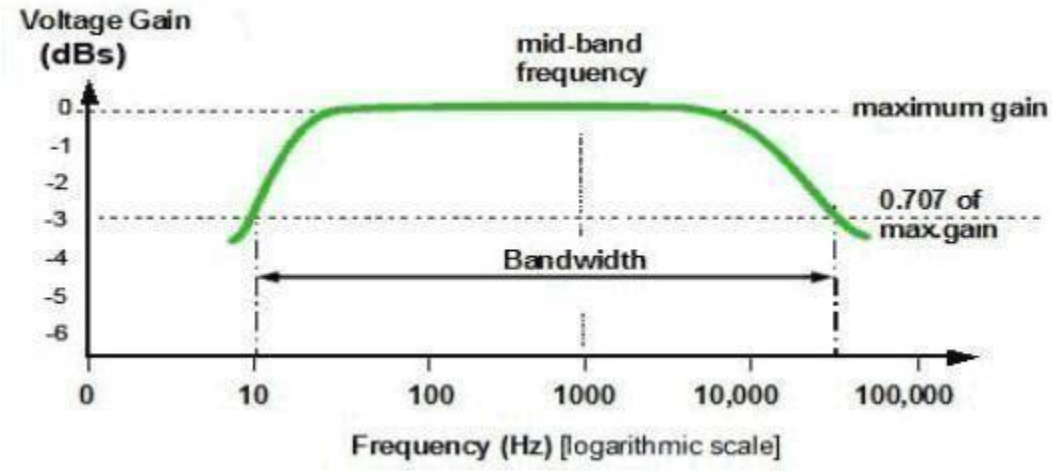
Bandwidth, BW = f_2-f_1

where
f_1 lower cut-off frequency
f_2 upper cut-off frequency

COMMON COLLECTOR CIRCUIT DIAGRAM:



MODEL GRAPH



TABULATION:

Input voltage constant (vin) =

FREQUENCY (in Hz)	OUTPUT V_O(V)	Gain in dB= 20log(V_o/V_{in}) dB

RESULT:

Thus the Common Collector amplifier was constructed and the frequency response curve I has been plotted.

EX.NO:2(b)
DATE:

DESIGN AND ANALYZE FREQUENCY RESPONSE OF COMMON BASE AMPLIFILER

AIM:

To design a Common Base amplifier with self bias and determine the voltage gain to plot the frequency response.

a. Gain of the amplifier
b. Bandwidth of the amplifier
c. Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1kΛ, ,10kΛ	Each 1
4	Power supply	(0-30)V	1
5	Transistors	BC 107	1
6	Capacitors	10μF,1 μF	Each 1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A common base amplifier is type of BJT amplifier which increases the voltage level of the applied input signal Vin at output of collector.

The Common base amplifier typically has good voltage gain and relatively high output impedance. But the Common base amplifier unlike CE amplifier has very low input impedance which makes it unsuitable for most voltage amplifier. It is typically used as an active load for a cascode amplifier and also as a current follower circuit.

Circuit Operation:

A positive-going signal voltage at the input of a CB pushes the transistor emitter in a positive direction while the base voltage remains fixed, hence Vbe reduces. The reduction in V_{BE} results in reduction in V_{RC}, consequently V_{CE} increases. The rise in collector voltage effectively rises the output voltage. The positive going pulse at the input produces a positive-going output, hence the there is no phase shift from input to output in CB circuit. In the same way the negative-going input produces a negative-going output.

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CB amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CB amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

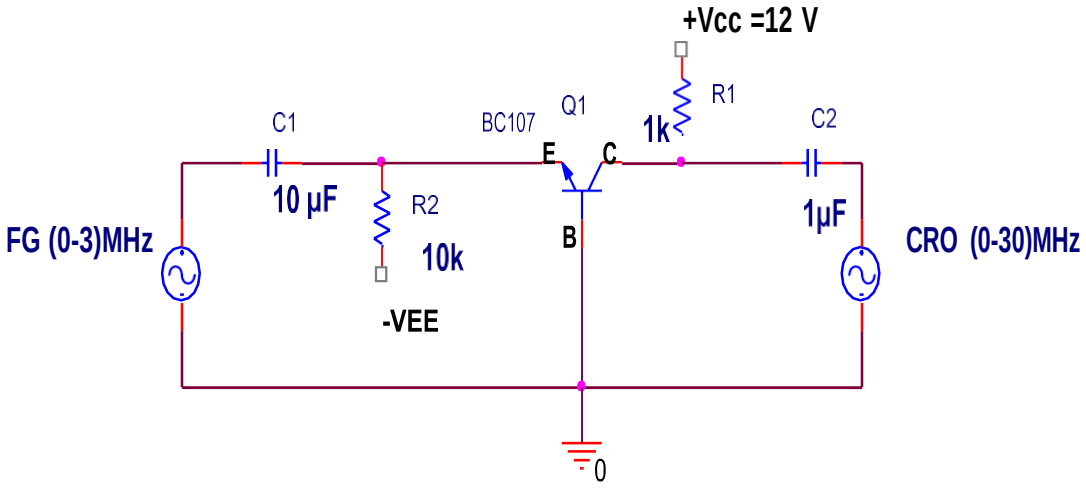
$$\mathbf{A_v = 20log\ (V_0/V_i)\ dB}$$

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

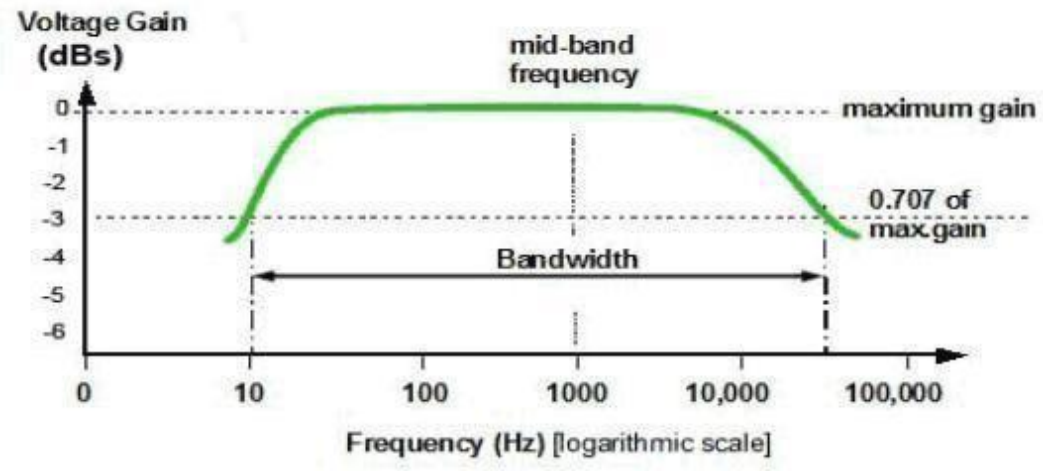
Bandwidth, BW = f_2-f_1

where
f_1 lower cut-off frequency
f_2 upper cut-off frequency

COMMON BASE CIRCUIT DIAGRAM:



MODEL GRAPH :



TABULATION:

Input voltage constant (V in) =

FREQUENCY (in Hz)	OUTPUT V_O(V)	Gain in dB= 20log(V_o/V_{in}) dB

RESULT:

Thus the Common Base amplifier was constructed and the frequency response curve has been plotted.

EX.NO:3

DATE:

DESIGN AND ANALYZE MULTISTAGE AMPLIFIER CONFIGURATIONS

AIM:

To design and construct a multistage amplifier and to plot the frequency response characteristics.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1KΛ,	3
		10KΛ,25KΛ,270 KΛ,120 KΛ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	1
6	Capacitor	0.01µf,10mf	2,1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

The cascode configuration has one of two configurations of multistage amplifier. In each case the collector of the leading transistor is connected to the emitter of the following transistor. The arrangement of the two transistors is shown in the circuit diagram. The cascode amplifier consists of CE stage connected in series with CB stage. The arrangement provides a relatively high input impedance with low voltage gain for the first stage to ensure the input miller capacitance is at a minimum, whereas the following CB stage provides an excellent high frequency response.

Features:

1. It provides high voltage gain and has high input impedance.
2. It provides high stability and has high output impedance

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CE amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CE amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

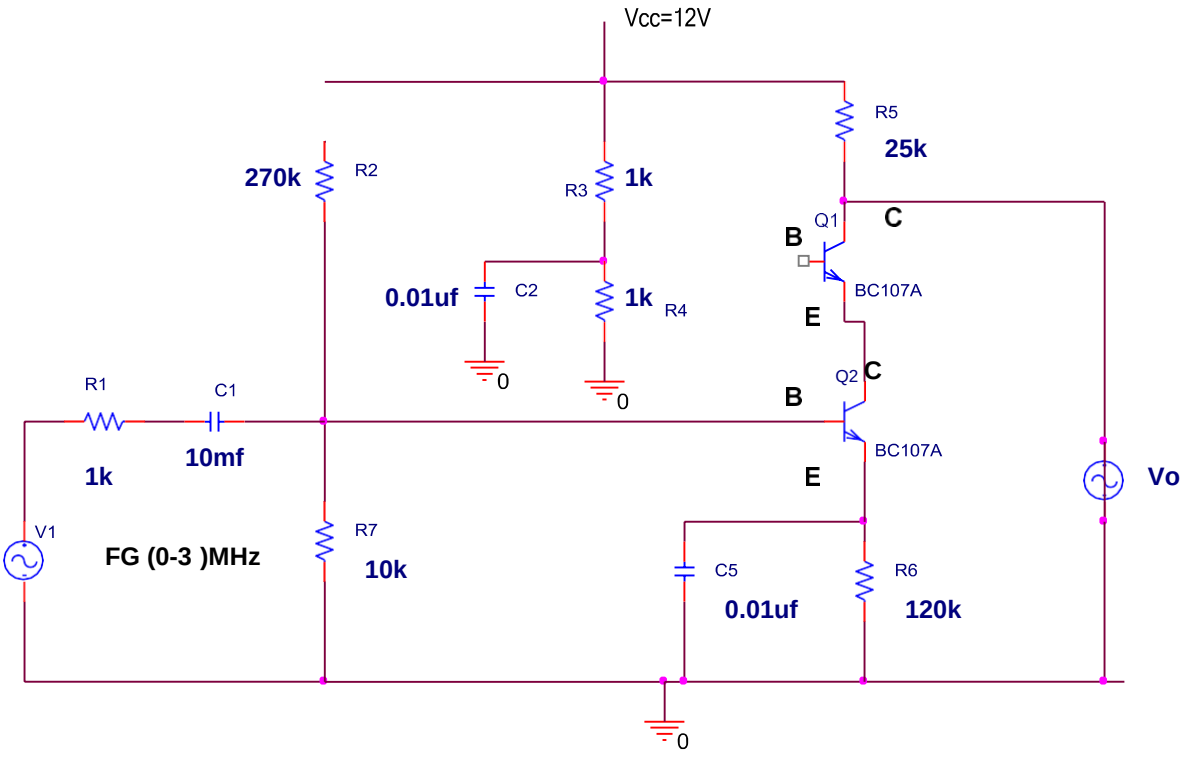
$$\mathbf{A_v = 20log\ (V_0/V_i)\ dB}$$

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

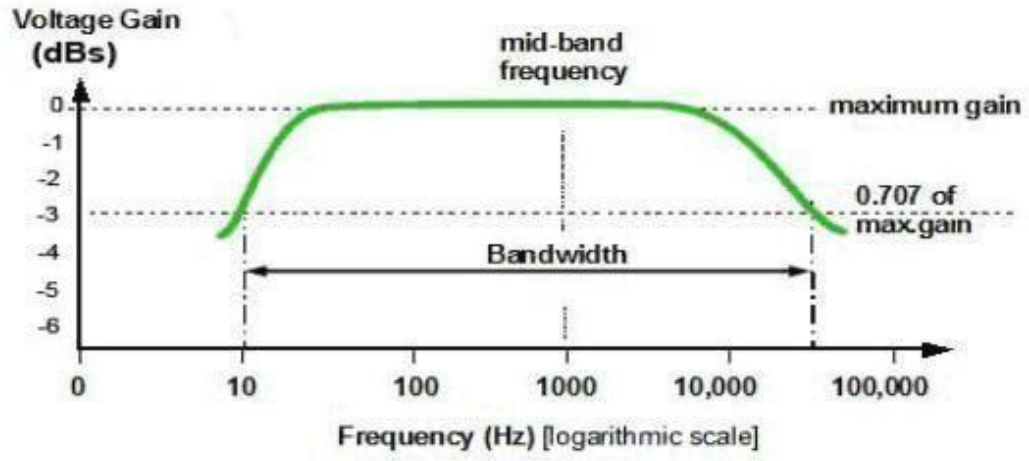
Bandwidth, BW = f_2-f_1

where
f_1 lower cut-off frequency
f_2 upper cut-off frequency

CIRCUIT DIAGRAM:



MODEL GRAPH :



TABULATION:

Input voltage constant (vin) =

FREQUENCY (in Hz)	OUTPUT V_O(V)	Gain in dB= 20log(V_o/V_{in}) dB

RESULT:

Thus multistage amplifier was constructed and the frequency response curve has been plotted in graph.

EX.NO: 4

DATE:

DESIGN AND ANALYZE DIFFERENTIAL AMPLIFIER

AIM:

To Design and Construct a Differential **A**mplifier using BJT and to determine its:

a. Transfer Characteristics.

b. Gain of the amplifier in common mode.

c. Gain of the amplifier in differential mode.

d. CMRR (Common Mode Rejection Ratio).

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1KΛ,1KΛ,10kΛ,4.7KΛ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	1
6	Bread Board	-	1
7	Connecting Wires	Single strand	as required

THEORY:

A differential amplifier is a type of electronic amplifier that amplifies the difference between two voltages but does not amplify the particular voltages. The need for differential amplifier arises in many physical measurements where response from D.C to many MHZ is required. It is also used in input stage of integrated amplifier.

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the Differential amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to amplifier using AC analysis.
4. Determine the Transfer characteristics of Differential amplifier by plotting the graph for normalized differential input voltage [$(Vb1 – V_{b2}) / V_T$] vs. Normalized collector current [Ic / Io].
5. Calculate the voltage gain of differential amplifier for differential mode as

$$A_d = 20\log (V_0/V_i)$$

Where Vi = V1 – V2

6. Calculate the voltage gain of differential amplifier for Common mode as

$$AC = 20\log (V0/Vi)$$

Where Vi = (V1+ V2 / 2)

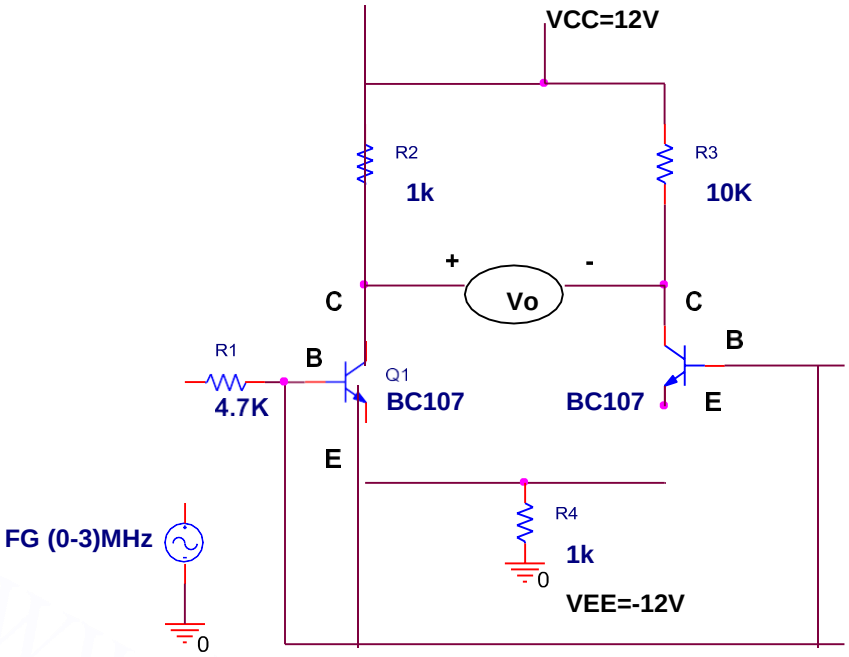
7. Find the Common mode rejection ratio of differential amplifier using the formula given below.

$$CMRR= 20 \log10 (Ad/Ac)$$

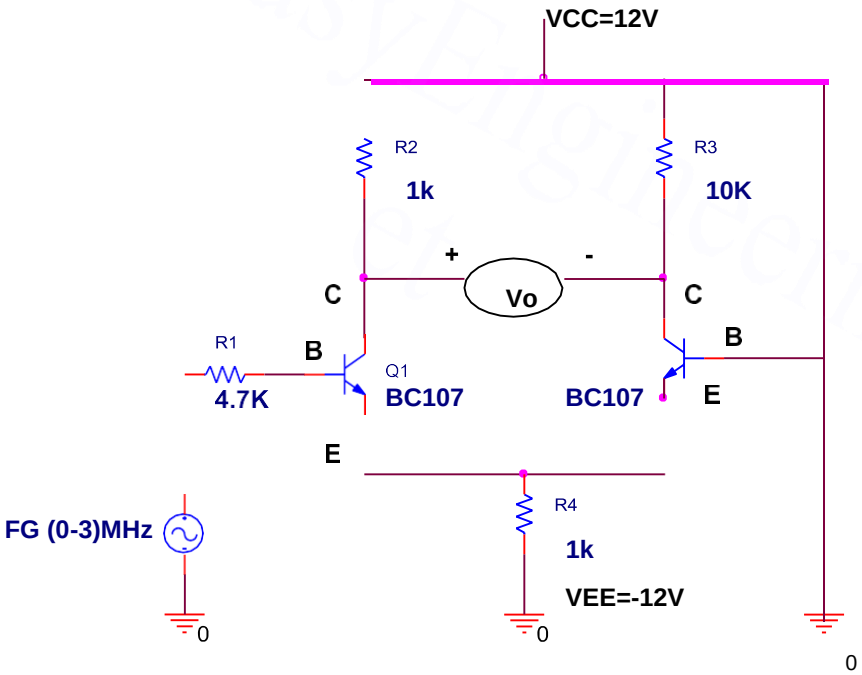
Where Ad- Differential mode gain in dB

Ac – Common Mode gain in dB

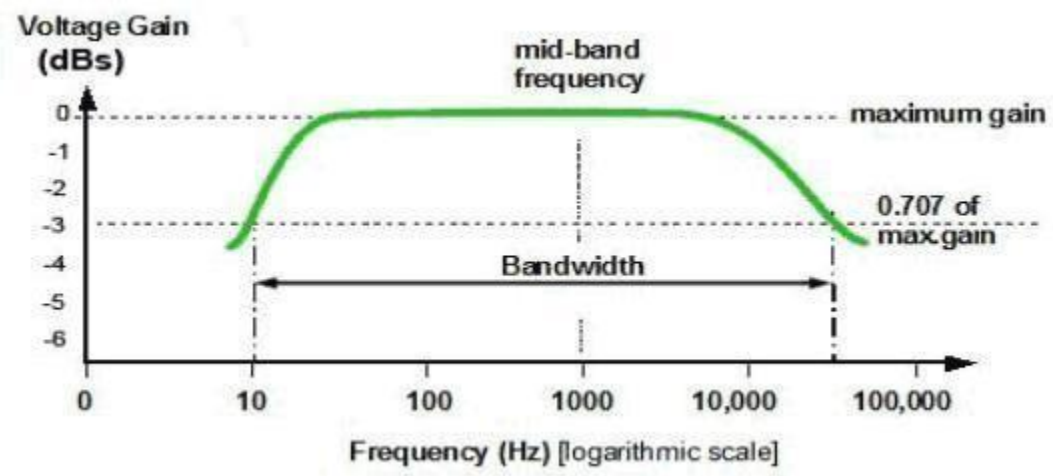
COMMON MODE CIRCUIT DIAGRAM:



DIFFERENTIAL MODE CIRCUIT DIAGRAM:



MODEL GRAPH :



TABULATION:

Common Mode (V in) =

Differential Mode (Vin) =

S.No	Frequency (in Hz)	Vo (in volts)		Gain in dB= $20\log(V_o/V_{in})$dB		CMRR(dB)
		Common mode	Differential Mode	Common mode	Differential Mode	

TRANSFER CHARACTERISTICS CALCULATION:

S.NO	INPUT VOLTAGE V_I = (VB1 – VB2) IN VOLTS	OUTPUT CURRENT I_{C2} IN AMPERE
1.		
2.		
3.		
4.		
5.		
6.		

RESULT:

Thus the gain of the differential amplifier was constructed and the frequency response curve has been plotted

EX.NO: 5.(a)

DATE:

DESIGN AND ANALYZE CURRENT SERIES FEEDBACK AMPLIFIER

AIM:

To design and plot the frequency response of current series feedback amplifier.

APPARATUS REQUIRED:

Sl. No.	Components	Specification	Quantity
1	Transistor	BC 107	1
2	Resistance	56K,2k,12k,470Ω	1
3	Capacitance	2.2µf	2
		47 µf	1
4	AFO, CRO, Bread board		1(Each)
5	Connecting wires		As required
6	Power Supply	(0-30V)	1

THEORY:

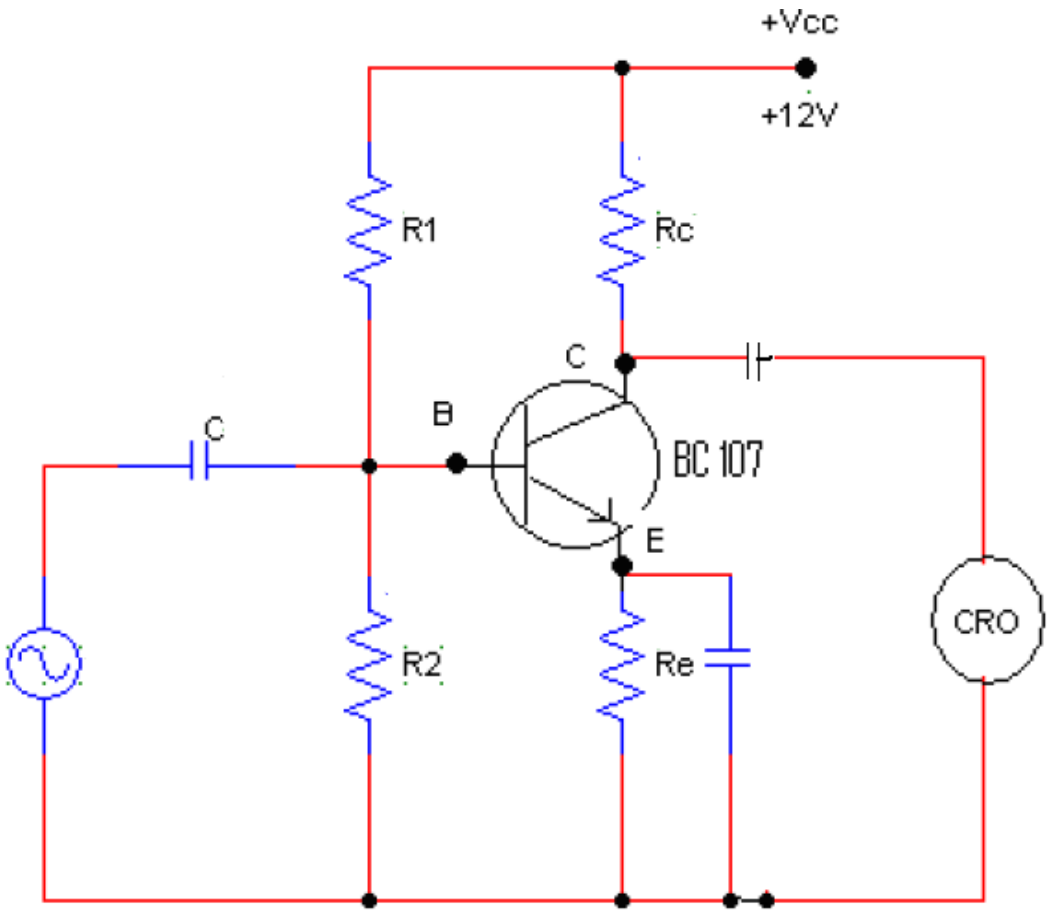
An amplifier whose fraction of output is fed back to the input is called feedback amplifier. A feedback amplifier consists of two parts namely amplifier circuit and feedback circuit. Depending upon whether the feedback signal increases or decreases the input signal it is classified into two i. Positive Feedback – If the feedback signal is in phase with the input signal

.ii Negative feedback – If the feedback signal is out of phase with the input signal. The positive feedback increases the gain of the amplifier whereas the negative feedback decreases the gain. In the current series feedback connection a fraction of the output current is converted into a proportional voltage by the feedback network and then applied in series with the input.

PROCEDURE :

1. The connections are done as shown in the circuit diagram for without feedback amplifier.
2. The input voltage is set to a fixed value.
3. Vary the frequency and note down the output voltage.
4. Calculate the gain and plot the graph.
5. Repeat the above procedure for the circuit with feedback.

CIRCUIT DIAGRAM: CURRENT SERIES FEEDBACKAMPLIFIER

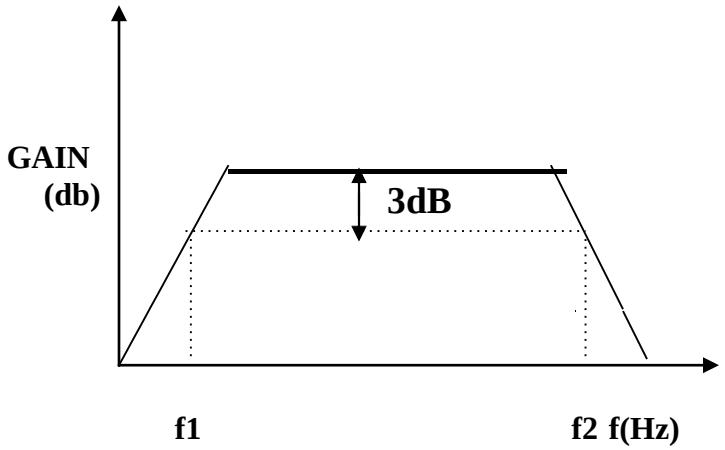


TABULATION:

V_i =

S.No	FREQUENCY in Hz	OUTPUT VOLTAGE V_o in volts	GAIN = 20 log(V_o / Vi)in db

MODEL GRAPH



f2 – f1 = Bandwidth with feedback circuit

DESIGN:

Specifications: $V_{CC} = 10V \qquad I_C = 2mA \qquad \beta = 250$

$$Let \quad V_{CE} = \frac{V_{CC}}{2} \; ; \qquad V_{CE} = 5V$$

$$V_E = \frac{V_{CC}}{10} \quad and \quad I_E = I_C$$

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} =$$

$$R_E = \frac{V_E}{I_E} =$$

$$R_2 = 0.1 \times h_{fe} \times R_E =$$

$$V_B = V_{BE} + V_E =$$

$$V_B = \frac{V_{CC} R_2}{(R_1 + R_2)}$$

$$R_1 = \frac{V_{CC} R_2 - V_B R_2}{V_B} =$$

Design of input , output and emitter by pass capacitor:

$$hie = \beta r_e = 11.44k\Omega \quad where \; r_e = \frac{26mV}{I_E}$$

$$X_{Ci} = (R_B \; // \; hie)/10 = \qquad where \quad R_B = R_1 \parallel R_2$$

$$C_i = \frac{1}{2\pi f X_{Ci}} = \qquad for \quad f = 1000Hz$$

$$X_{C0} = \frac{R_C}{10} =$$

$$C_0 = \frac{1}{2\pi f X_{Co}} = \qquad for \; f = 1000Hz$$

$$X_{CE} = \frac{R_E}{10} = 1$$

$$C_E = \frac{1}{2\pi f X_{CE}} = 1.33\mu F \qquad for \; f = 1000Hz$$

RESULT :

The current series feed back amplifier was designed and frequency response is plotted.

Upper cutoff frequency:
Lower cutoff frequency:
Bandwidth:

EX.NO: 5.(a)

DATE:

DESIGN AND ANALYZE VOLTAGE SHUNT FEEDBACK AMPLIFIERDATE

AIM:

To design and plot the frequency response of voltage shunt feedback amplifier.

APPARATUS REQUIRED:

Sl. No.	Components	Specification	Quantity
1	Transistor	BC 107	1
2	Resistance	56K,2k,12k,43k,470Ω	1
3	Capacitance	0.01µf,2.2µf	1,2
4	AFO, CRO, Bread board		1(each)
5	Connecting wires		As required
6	Power supply	(0-30V)	1

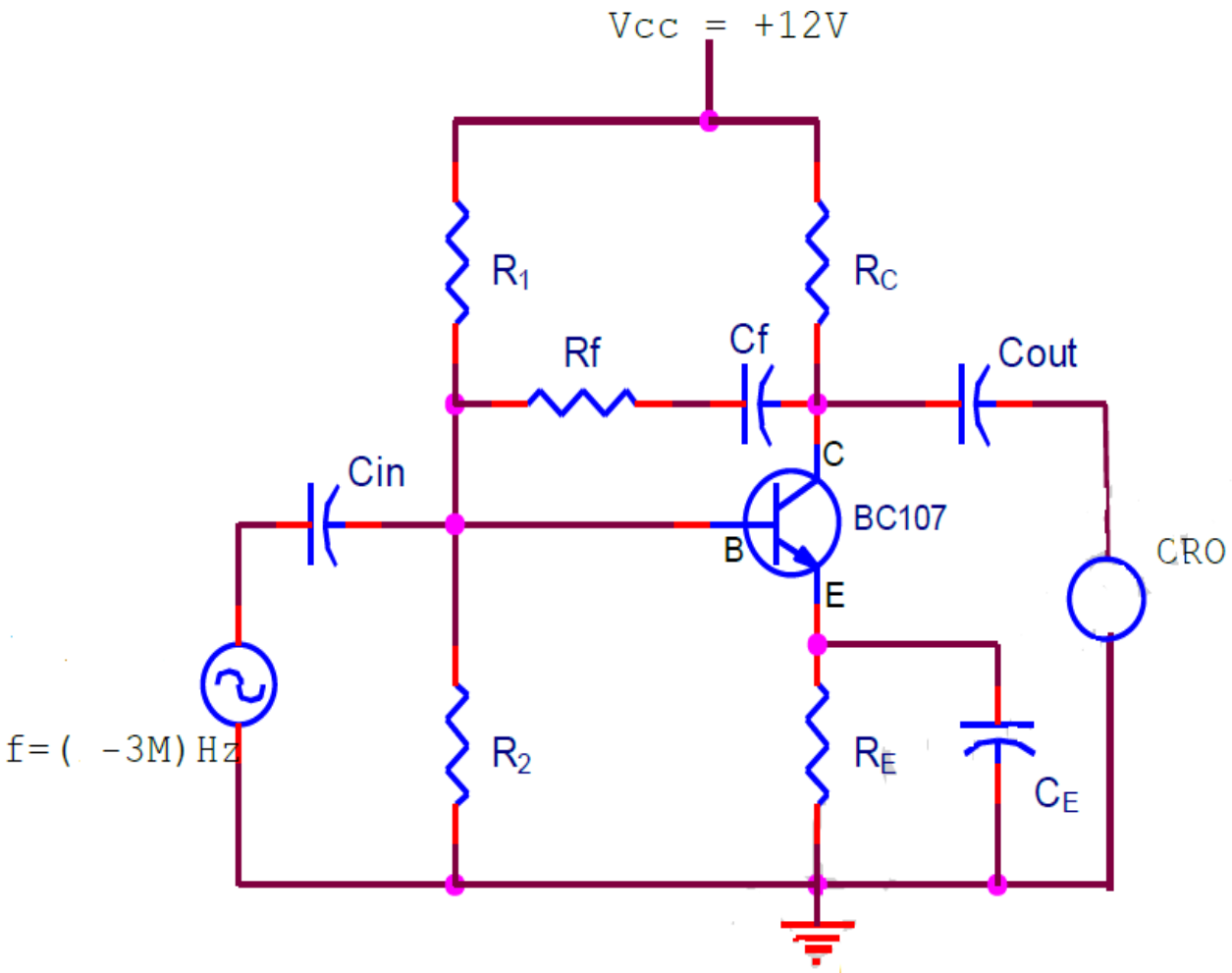
THEORY:

An amplifier whose fraction of output is fed back to the input is called feedback amplifier. A feedback amplifier consists of two parts namely amplifier circuit and feedback circuit. Depending upon whether the feedback signal increases or decreases the input signal it is classified into two i. Positive Feedback – If the feedback signal is in phase with the input signal .ii Negative feedback – If the feedback signal is out of phase with the input signal. The positive feedback increases the gain of the amplifier whereas the negative feedback decreases the gain. In the voltage shunt feedback connection a fraction of the output voltage is applied in parallel with the input voltage through the feedback network The voltage shunt feedbackconnection decreases both input and output resistances of the feedback amplifier by a factor equal to (1+ βAv).

PROCEDURE :

1. The connections are done as shown in the circuit diagram for without feedback amplifier
2. The input voltage is set to a fixed value.
3. Vary the frequency and note down the output voltage.
4. Calculate the gain and plot the graph.
5. Repeat the above procedure for with feedback.

CIRCUIT DIAGRAM: VOLTAGE SHUNT FEEDBACK AMPLIFIER

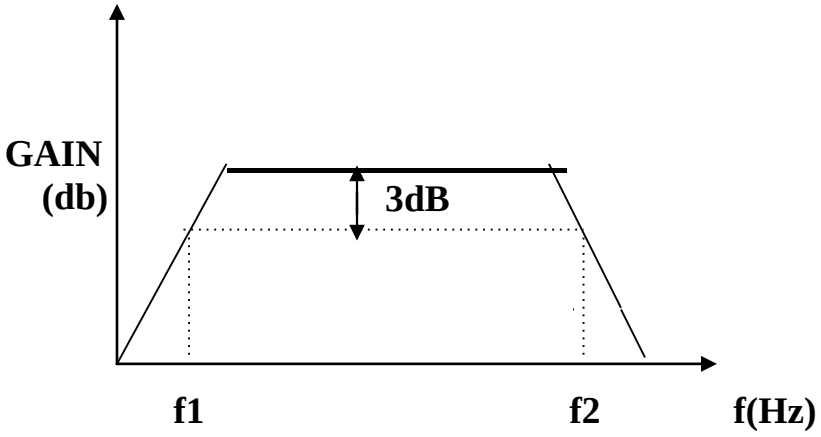


TABULATION:

V_i =

S.No	FREQUENCY in Hz	OUTPUT VOLTAGE V_o in volts	GAIN = 20 log(V_o / Vi)in db

MODEL GRAPH



f2 – f1 = Bandwidth with feedback circuit

DESIGN:

Specifications: $V_{CC} = 10V \qquad I_C = 2mA \qquad \beta = 250$

$$Let \quad V_{CE} = \frac{V_{CC}}{2} \; ; \qquad V_{CE} = 5V$$

$$V_E = \frac{V_{CC}}{10} \quad and \quad I_E = I_C$$

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} =$$

$$R_E = \frac{V_E}{I_E} =$$

$$R_2 = 0.1 \times h_{fe} \times R_E =$$

$$V_B = V_{BE} + V_E =$$

$$V_B = \frac{V_{CC} R_2}{(R_1 + R_2)}$$

$$R_1 = \frac{V_{CC} R_2 - V_B R_2}{V_B} =$$

Design of input , output and emitter by pass capacitor:

$$hie = \beta \, r_e = 11.44k\Omega \quad where \; r_e = \frac{26mV}{I_E}$$

$$X_{Ci} = (R_B \; // \; hie)/10 = \qquad where \quad R_B = R_1 \parallel R_2$$

$$C_i = \frac{1}{2\pi f X_{Ci}} = \qquad for \quad f = 1000Hz$$

$$X_{C0} = \frac{R_C}{10} =$$

$$C_0 = \frac{1}{2\pi f X_{Co}} = \qquad for \; f = 1000Hz$$

$$X_{CE} = \frac{R_E}{10} =$$

$$C_E = \frac{1}{2\pi f X_{CE}} = \qquad for \; f = 1000Hz$$

RESULT:

The Voltage shunt feedback amplifier was designed and frequency response is plotted.

Upper cutoff frequency:
Lower cutoff frequency:
Bandwidth:

Ex.No:6

DATE:

DESIGN AND ANALYZE RC PHASE SHIFT OSCILLATORS

AIM:

To design a RC phase shift oscillator to generate a sinusoidal Waveform.

APPARATUS REQUIRED:

Sl. No.	Components	Specification	Quantity
1	Transistor	BC 107	1
2	Resistance	2.2K,56k,560Ω	1(each)
		6.2k	4
3	Capacitance	0.01µf	4
		10 µf,47µf	1(each)
4	AFO, CRO, Bread board		1(each)
5	Connecting wires		As required
6	Power supply	(0-30V)	1

THEORY:

Oscillator is a feedback circuit where a fraction of output voltage of an amplifier is fed back to the input in the same phase. RC phase shift oscillators are a sine wave oscillator which is used in the audio frequency range. It has a CE amplifier ,which provides 180°.phase shift to the input signal and three frequency selective RC phase shift networks provides a phase shift of 60°of each , a total of 180° for a signal with frequency equal to specific value, which corresponds to the output of the oscillator. Thus the total phase shift between the input and output is360°.

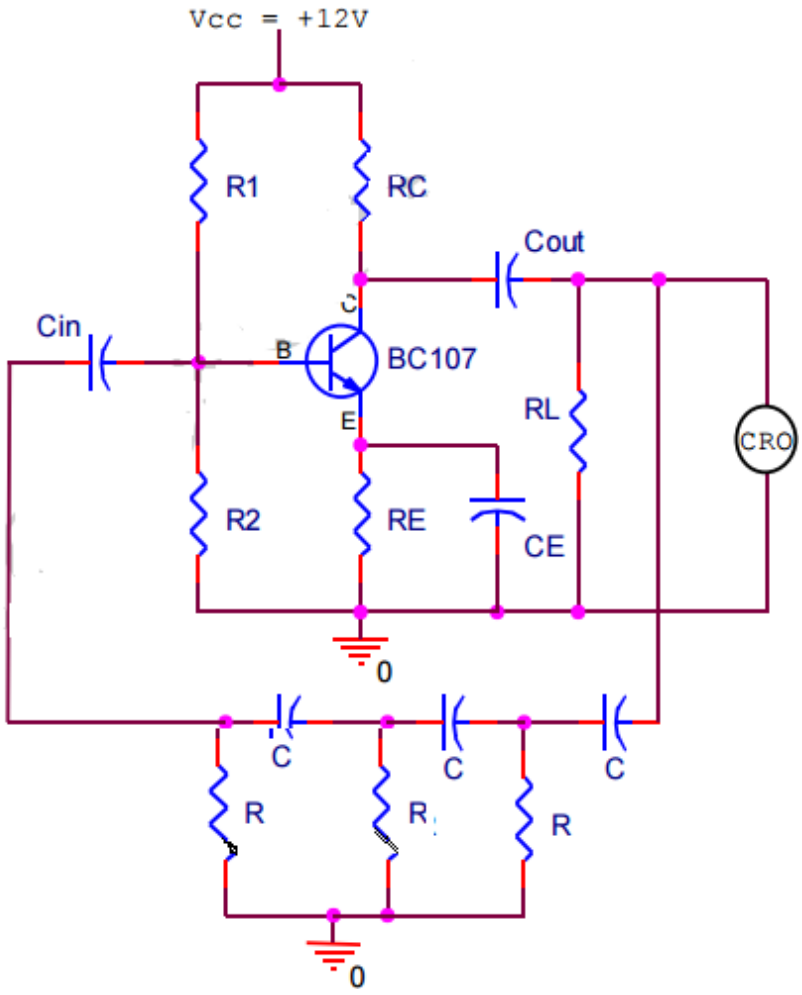
PROCEDURE:

1. The connection is made as per the circuit diagram.
2. Set the RPS to 20Volts.
3. Observe the output and measure the time period of the output waveform V_o , determine the frequency and trace it
4. Plot the output on a graph sheet.

Compare the experimental value with the theoretical value of output frequency

CIRCUIT DIAGRAM:

RC PHASE SHIFT OSCILLATOR



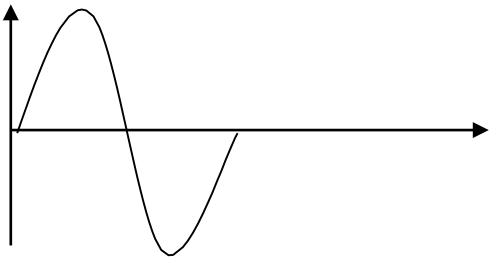
TABULATION:

Amplitude in volts	Time period (ms) (T)	Frequency in Hz (f= 1/ T)

MODEL GRAPH

amplitude in volts

T in ms



Frequency:

RESULT:

The RC phase shift oscillator is designed and the frequency of oscillation is obtained

Theoretical frequency: Hz.

Practical frequency: Hz.

Ex.No:7

DATE:

DESIGN AND ANALYZE LC OSCILLATORS

AIM:

To design a Wein bridge oscillator and to generate sinusoidal wave form.

APPARATUS REQUIRED:

Sl. No.	Components	Specification	Quantity
1	Transistor	BC 107	2
2	Resistance	4.7K,680K,10K,47K	2(each)
		2.7K,1.2K	1(each)
			1
3	Capacitance	0.01µf	2
		47µf,0.01	1(each)
4	AFO,CRO, Bread board		1(Each)
5	Connecting wires		As required
6	Power Supply	(0-30V)	1

THEORY:

Wien Bridge oscillator is one of the most popular type of sinusoidal oscillator which used in audio and sub-audio frequency range(2-20KHZ).The maximum output frequency of a typical Wien bridge oscillator is only about 1MHZ. This is also infact a phase –shift oscillator. It employs two transistors each producing a phase shift of 180 degree, and thus producing a total shift of 360 degree .It is essentially a two stage amplifier with an R-C bridge circuit. R-C bridge circuit is a lead – lag networK. By adding Wien bridge feedbacK networK, the oscillatorbecomes sensitive to a signal of only one particular frequency. This particular frequency is that atwhich Wien Bridge is balanced and for which the phase shift is 0 degree. Thus by employing wien bridge feedbacK networK frequency stability is increased.

PROCEDURE:

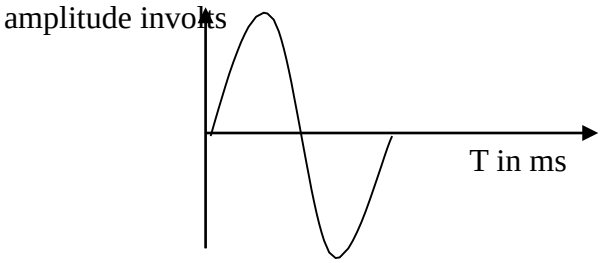
1. The connections are made as per the circuit diagram.
2. Observe the output and measure the amplitude and time period of the output waveformV_o.
3. Measure the amplitude and frequency of oscillator.
4. Plot the output.

CIRCUIT DIAGRAM:

TABULATION:

Amplitude in volts	Time period (ms) (T)	Frequency in Hz (f= 1/ T)

MODEL GRAPH



FREQUENCY:

RESULT:

The Wien bridge oscillator is designed and the frequency of oscillation is obtained

Theoretical frequency: Hz

Practical frequency: Hz.

EX.NO: 8(a)

DATE:

CLASS A AMPLIFIER

AIM:

To construct a Class A power amplifier and observe the waveform and to compute maximum output power and efficiency.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1 KΛ,330Λ,220KΛ,220 Λ	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	1
6	Capacitor	4.7µf,	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

The power amplifier is said to be Class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input signal cycle. For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally. The collector current flows for 360 (full cycle) of the input signal. i e the angle of the collector current flow is 360 .

PROCEDURE:

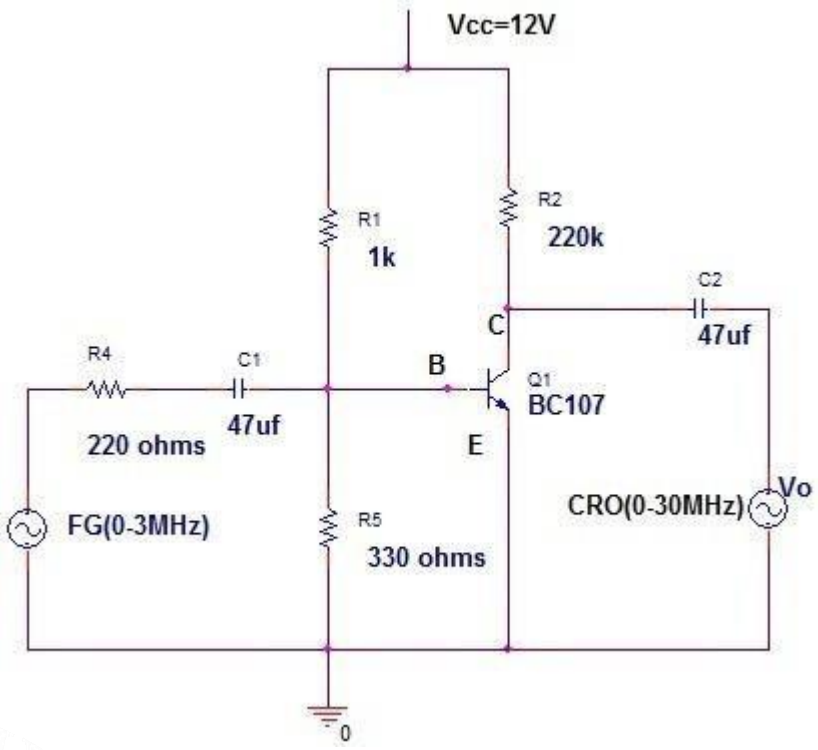
1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mv, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 10 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) vs Frequency (Hz).

FORMULA

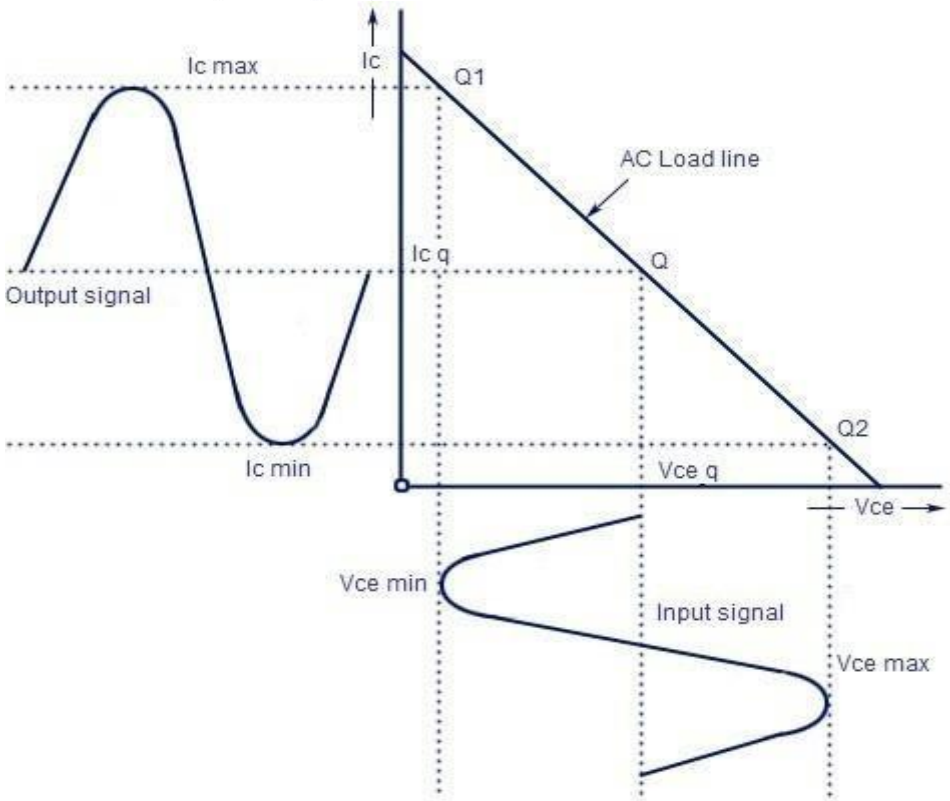
Maximum power transfer = $P_{o,max}=V_o^2/R_L$

Efficiency ,$\eta = P_{o,max}/P_c$

CLASS A AMPLIFIER CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

Signals	Amplitude (volt)	Time period (sec)
Input signal		
Output signal		

RESULT :

Thus the Class A amplifier was constructed and observed the waveforms values are plotted in graph.

EX.NO: 8(b)

DATE:

CLASS B AMPLIFIER

AIM:

To construct a Class B complementary symmetry power amplifier and observe the waveforms with and without cross-over distortion and to compute maximum output power and efficiency.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	4.7KΛ,1.5KΛ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	2
6	Capacitor	100µf,	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A power amplifier is said to be Class B amplifier if the Q-point and the input signal are selected such that the output signal is obtained only for one half cycle for a full input cycle. The Q-point is selected on the X-axis. Hence, the transistor remains in the active region only for the positive half ofthe input signal. There are two types of Class B power amplifiers: Push Pull amplifier and complementary symmetry amplifier. In the complementary symmetry amplifier, one n-p-n and another p-n-p transistor is used. The matched pair of transistor are used in the common collector configuration. In the positive half cycle of the input signal, the n-p-n transistor is driven into active region and starts conducting and in negative half cycle, the p-n-p transistor is driven into conduction. However there is a period between the crossing of the half cycles of the input signals, for which none of the transistor is active and output, is zero

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Observe the waveforms and note the amplitude and time period of the input signal and distorted waveforms.
3. Connections are made with proper biasing.
4. Observe the waveforms and note the amplitude and time period of the input signal and output Signal.
5. Draw the waveforms for the readings.
6. Calculate the maximum output power and efficiency.

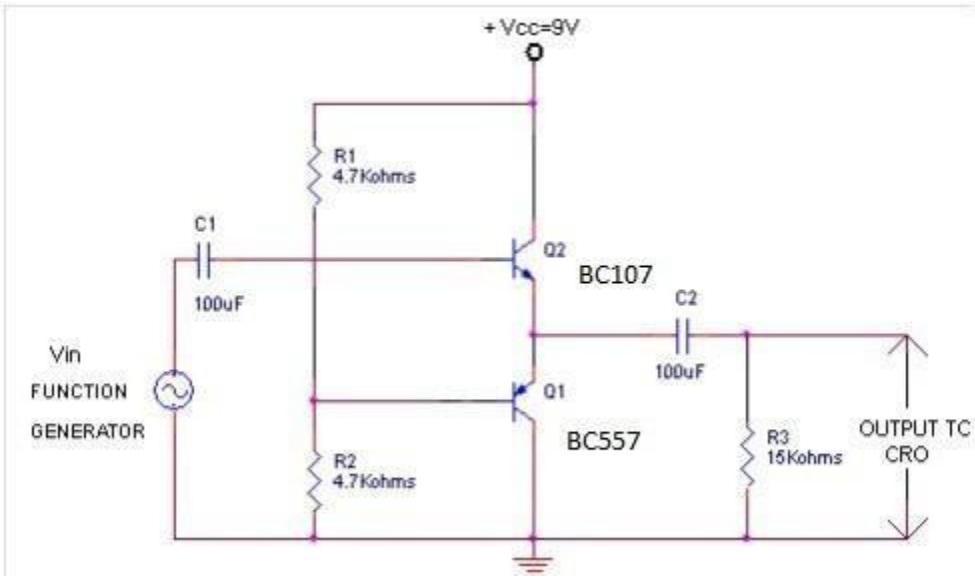
FORMULA:

Input power, Pin=2VccIm/Π

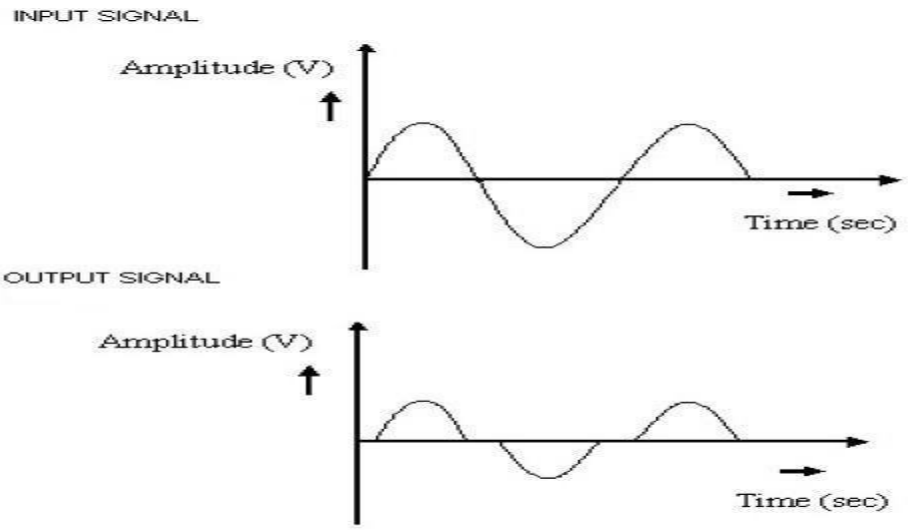
Output power, Pout=VmIm/2

Power Gain or efficiency, η=л/4(Vm /Vcc) 100

CLASS B AMPLIFIER CIRCUIT DIAGRAM:



MODEL GRAPH



TABULATION:

Signals	Amplitude (volt)	Time period (sec)
Input signal		
Output signal		

RESULT :

Thus the Class B complementary symmetry power amplifier was constructed and the waveforms values are plotted in graph.

EX.NO:9

DATE:

FREQUENCY RESPONSE OF COMMON SOURCE AMPLIFILER

AIM:

To design a Common Source amplifier with self bias and determine the voltage gain to plot the frequency response.

a. Gain of the amplifier

b. Bandwidth of the amplifier

c. Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1kΛ, ,10kΛ,2KΛ,	Each 1
4	Power supply	(0-30)V	1
5	JFET	BFW10	1
6	Capacitors	10μF,1 μF	Each 1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

There are three basic types of FET amplifier or FET transistor namely common source amplifier, common gate amplifier and source follower amplifier.

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier.

i) As a transconductance amplifier, the input voltage is seen as modulating the current going to the load.

As a voltage amplifier, input voltage modulates the amount of current flowingthroughthe FET, changing the voltage across the output resistance according to Ohm's law.

However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain morefavorable output and frequency characteristics

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CS amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CS amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

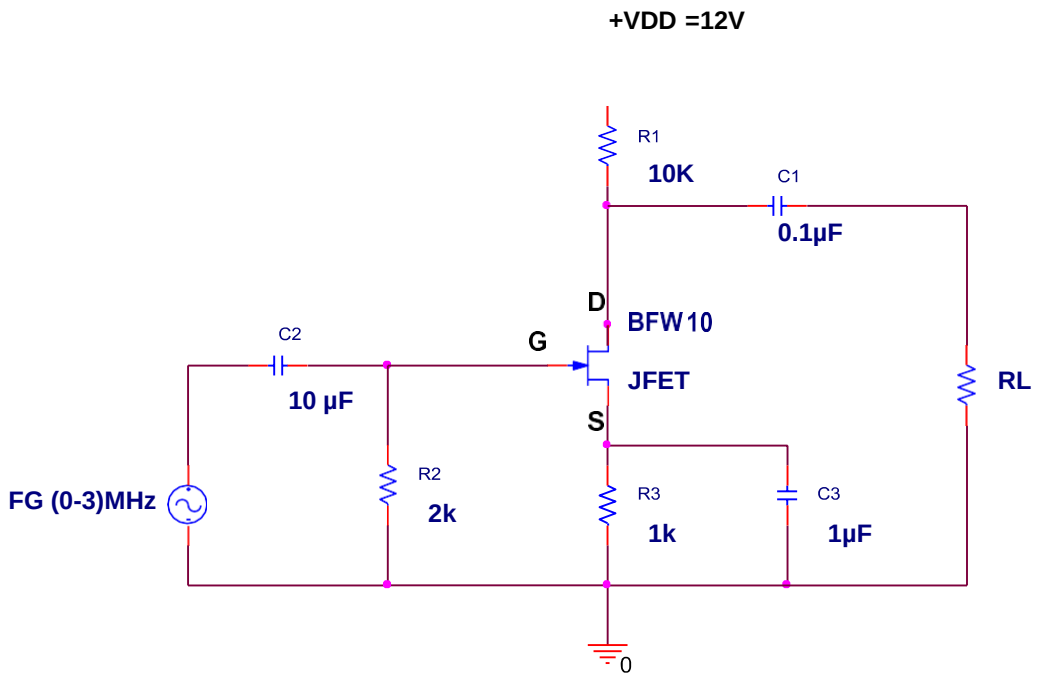
$$\mathbf{A_V = 20log\ (V_0/V_i)\ dB}$$

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

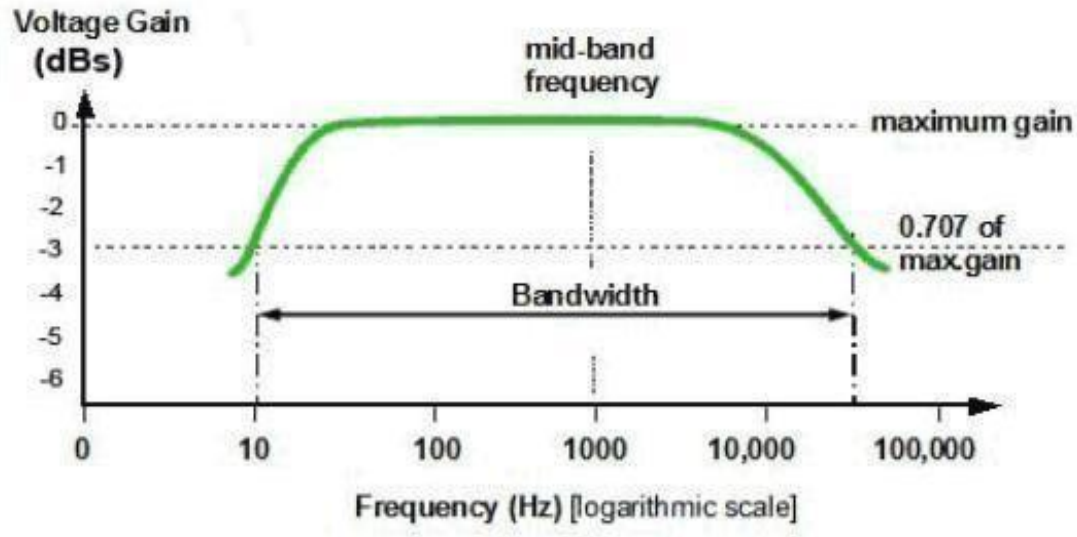
Bandwidth, BW = f_2-f_1

where
f_1 lower cut-off frequency
f_2 upper cut-off frequency

COMMON SOURCE CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

Input voltage constant (V in) =

FREQUENCY (in Hz)	OUTPUT V_O(V)	Gain in dB= 20log(V_o/V_{in})dB

RESULT:

Thus the Common Source amplifier was constructed and the frequency response curve I has been plotted.

EX.NO:9

DATE:

DESIGN AND ANALYZE COMMON-SOURCE AMPLIFIER

AIM:

To design and construct a common-source amplifier circuit and to determine its frequency response.

COMPONENTS & EQUIPMENTS REQUIRED:

S.NO	COMPONENT	RANGE	QUANTITY
1	Transistor	BFW 10	1
2	RPS	(0-30)V	1
3	Signal Generator	(0-3)MHz	1
4	CRO	(0-30)MHz	1
5	Bread Board	-	1
6	Resistors	10K, 2.2K, 3.3M	1
7	Capacitors	0.1uf	2
8	Single strand Wires	-	-
9	CRO Probes	-	3

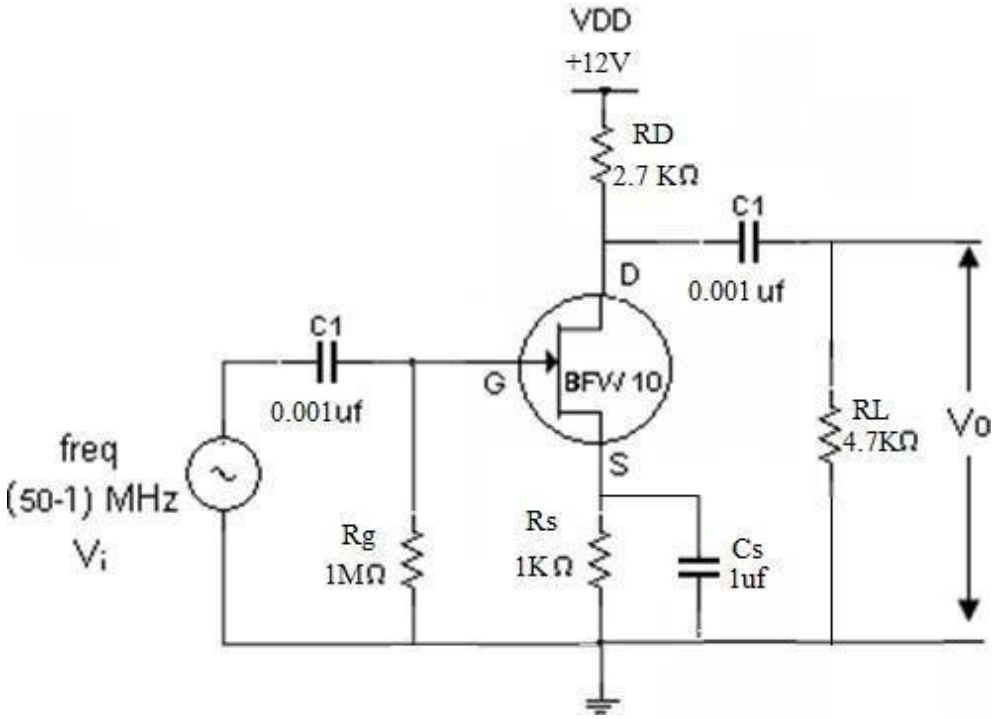
PROCEDURE:

1. Connect the circuit diagram as per the circuit diagram.
2. Set Vi = 50mV, using the signal generator.
3. Keeping the input voltage constant, Vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: Gain (dB) vs Frequency (Hz)
5. Calculate the bandwidth from the graph.

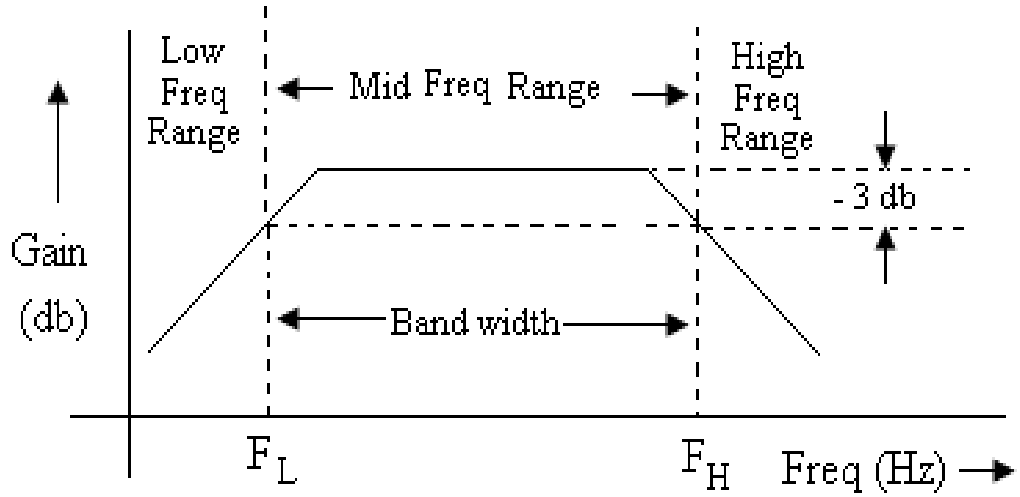
THEORY :

The common source configuration for a FET is similar to the common emitter bipolar transistor configuration, The common source amplifier can provide both a voltage and current gain. Since the input resistance looking into the gate is extremely large the current gain available from the FET amplifier can be quite large, but the voltage gain is generally inferior to that available from a bipolar device. Thus FET amplifiers are most useful with high output-impedance signal sources where a large current gain is the primary requirement. The source by-pass capacitor provides a low impedance path to ground for high frequency components and hence AC signals will not cause a swing in the bias voltage.A basic common-source amplifier circuit containing an N-channel JFET. The characteristics of this circuit include high input impedance and a high voltage gain. The function of the circuit components are C1 and C2 are the input and output coupling capacitors. Rg is the gate return resistor.

CIRCUIT DIAGRAM OF COMMON SOURCE AMPLIFIER



Model Graph



Design Specifications

V_{DD}=12V, V_{GS}=-2V, for N-Channel JFET (BFW10) Ro=40K, and g_m=2.5mA/V at I_D=2mA, and V_P=8V

Design of Rg

Select Rg=1MΩ (since voltage across Rg assumed to be 0V)

Design of R_D

V_{RD}=45% of V_{DD} = 5.4V

$V_{RD}=I_d*R_D$

$RD= V_{RD}/I_d= 2.7K\Omega$

Design of R_S

$Rs=V_{RS}/I_S =V_{RS}/I_D$ ($I_D=I_S=2mA$)

V_{RS}=Vg-VGS

V_{RS} =0-(-2V) =2V

$RS=2/2*10^{-3}=1K\Omega$

Design of R_L

Gain of CS amp $A=gm(R_D \| R_L)$

The required gain=15

$R_L=4.7K\Omega$

To find C_S (Bypass capacitor)

$X_{CS} =R_S / 10 =1000 /10 =100$

$X_{CS} =100$

$X_{CS} =1 / 2\pi f C_S$

Let f=1000

$C_S = 1 / 2\pi f X_{CS}$

$C_S = 1 / 2*\pi *1000* 100$

$C_S = 1 \mu f$

To find C_i (Input capacitor)

$X_{Ci} =Rg /10=0.1M\Omega$

$X_{Ci} =1 / 2\pi f C_i$

Let f=1000

$C_i = 1 / 2\pi f X_{Ci}$

$C_i = 1 / 2*\pi *1000* 0.1M\Omega$

$C_i = 0.001 \mu f$

To find C_O (Output capacitor)

$X_{CO} =R_S / 10 = 100$

$X_{CO} =1 / 2\pi f C_O$

Let f=1000

$C_O = 1 / 2\pi f X_{CO}$

$C_O = 1 / 2*\pi *1000* 1000$

$C_O =1.5 \mu f$ use approx 1 µf

TABULATION:

S.NO	Frequency in Hz	Vo in Volts	Gain : 20 Log(Vo/Vin)

RESULT:

Thus the common source amplifier has been constructed, and frequency response of the amplifier has drawn.

EX.NO:10

DATE:

DESIGN AND ANALYZE BJT CE AMPLIFIER WITH ACTIVE LOAD

AIM:

To design a Common Emitter amplifier with active load and determine the voltage gain to plot the frequency response.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	10kΛ, 1kΛ, 22kΛ ,10kΛ	Each 1
4	Power supply	(0-30)V	1
5	Transistors	BC 107	3
6	Capacitors	1μF	1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A common emitter amplifier is type of BJT amplifier which increases the voltage level of the applied input signal V_{in} at output of collector. The CE amplifier typically has a relatively high input resistance (1 - 10 KΩ) and a fairly high output resistance. Therefore it is generally used to drive medium to high resistance loads. It is typically used in applications where a small voltage signal needs to be amplified to a large voltage signal like radio receivers.

The input signal Vin is applied to base emitter junction of the transistor and amplifier output Vo is taken across collector terminal. Transistor is maintained at the active region by using the resistors R1,R2 and Rc. A very small change in base current produces a much larger change in collector current.

The output Vo of the common emitter amplifier is 180 degrees out of phase with the applied the input signal $V_{in.}$

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CE amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CE amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for at least 20 different values for the considered range.
5. The voltage gain is calculated as

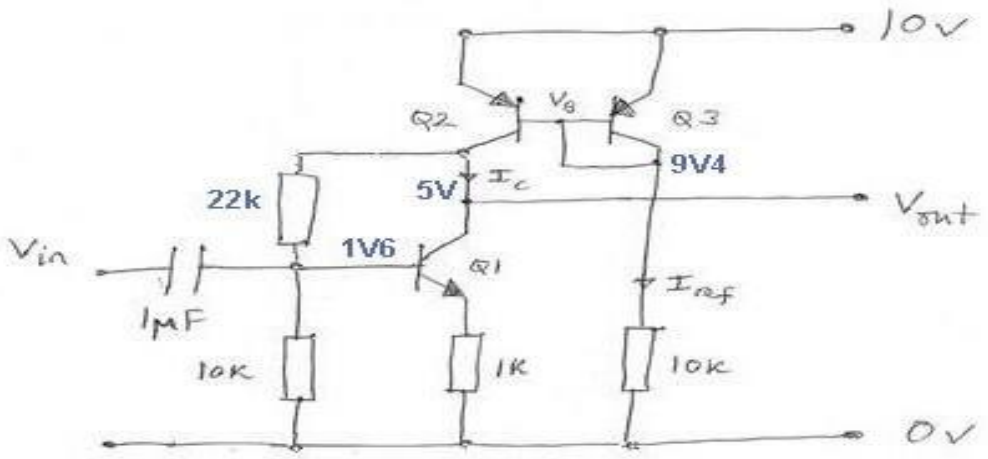
$$\mathbf{A_v = 20\log (V_0/V_i)\ dB}$$

Bandwidth, BW = f_2-f_1

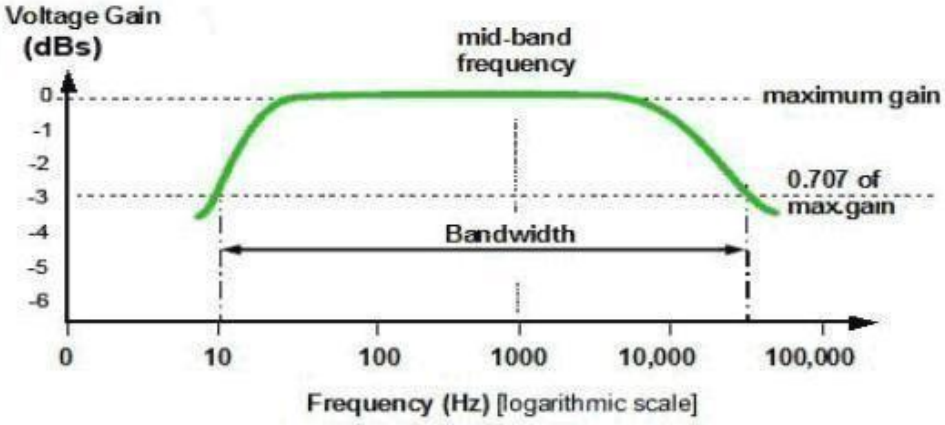
where
f_1 lower cut-off frequency
f_2 upper cut-off frequency

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axi

COMMON EMITTER CIRCUIT DIAGRAM:



MODEL GRAPH :



TABULATION:

Input voltage constant (vin) =

FREQUENCY (in Hz)	OUTPUT V_O(V)	Gain in dB= 20log(V_o/V_{in}) dB

RESULT:

Thus the Common Emitter amplifier with active load was constructed .