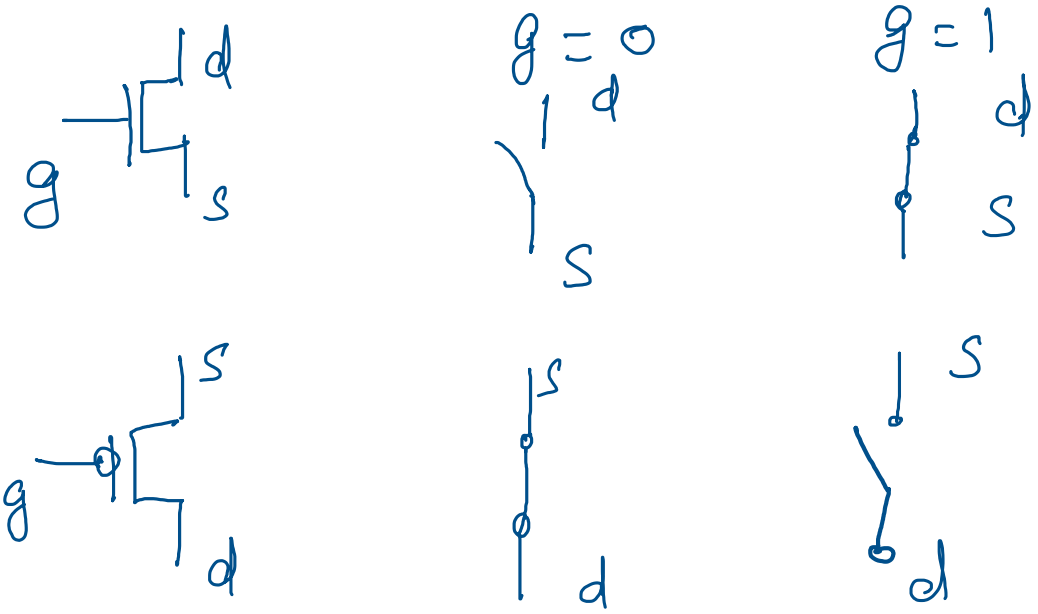
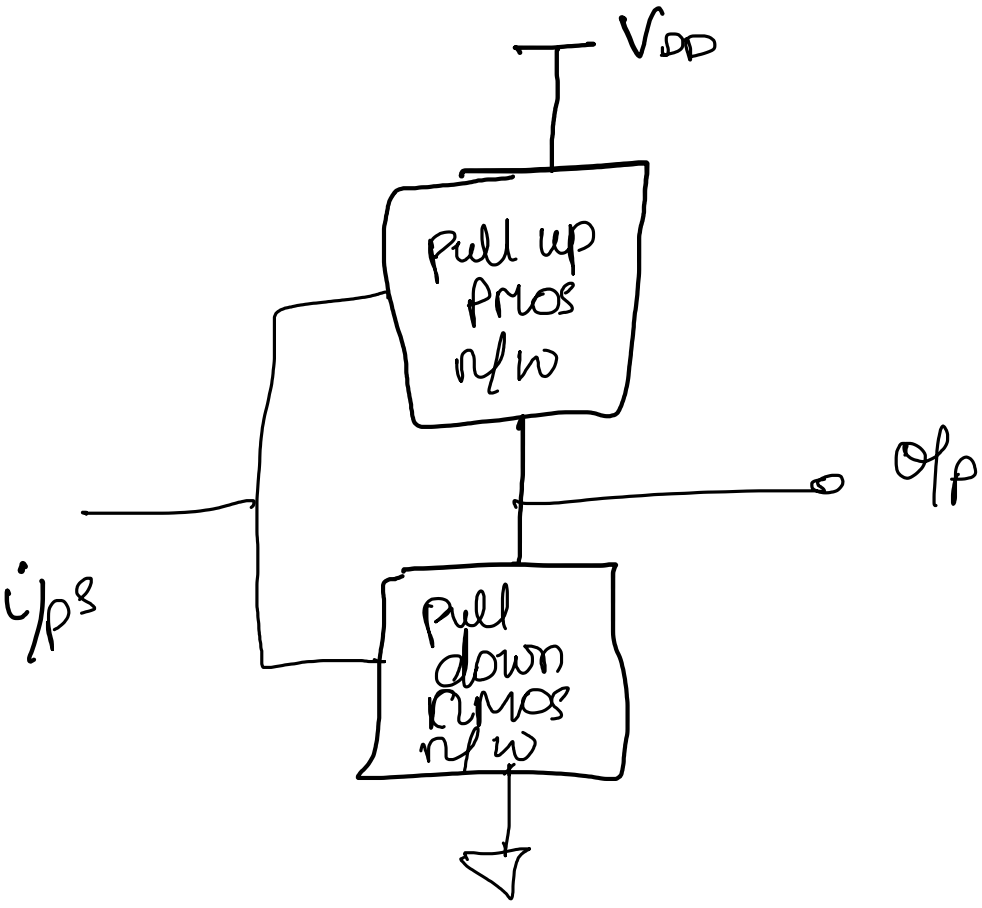
CMOS logic or fully restored logic :-

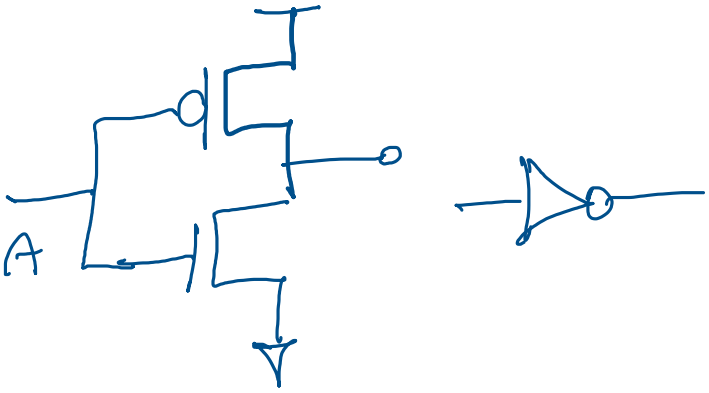
switch level models





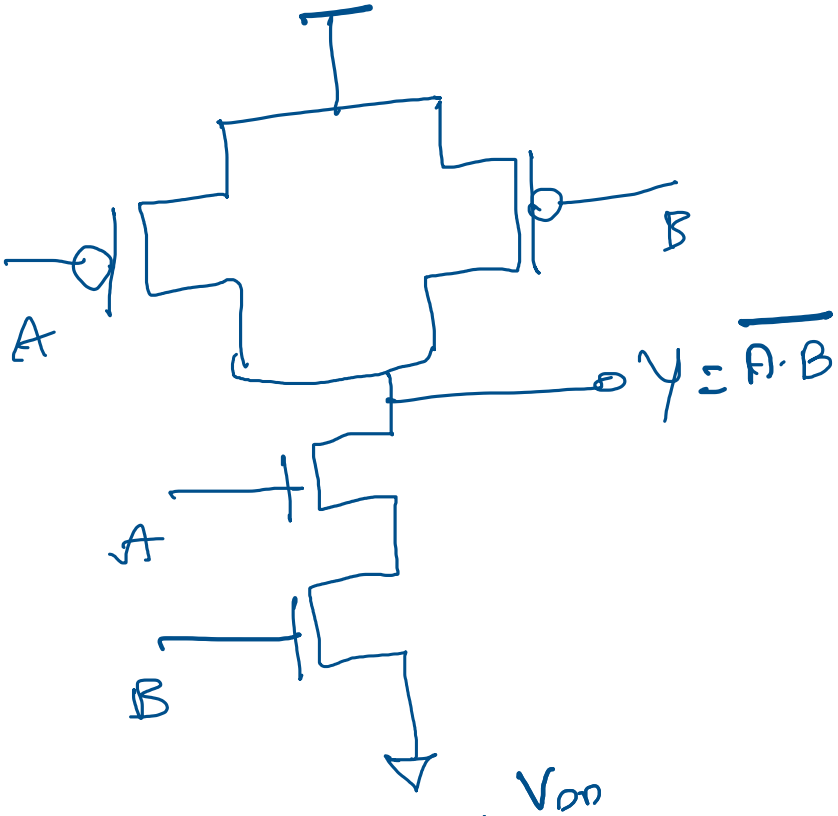
Inverter :-

A	Y
0	1
1	0



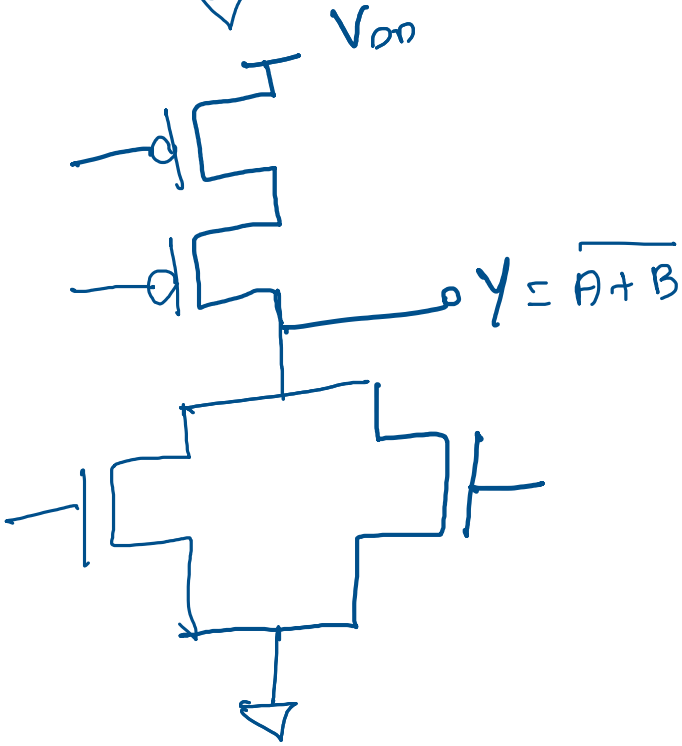
NAND gate :-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



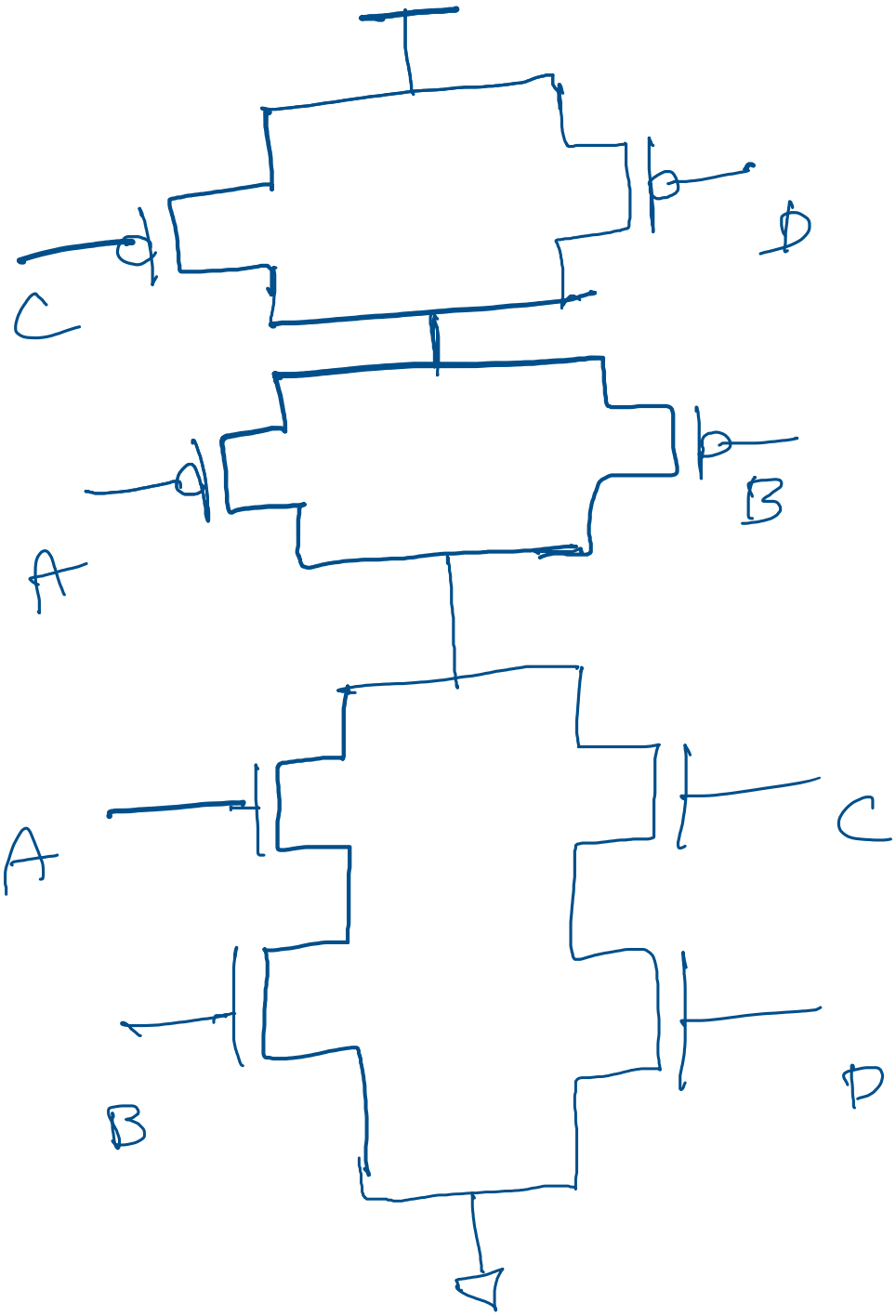
NOR gate :-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



Compound gates:-

$Y = A \cdot B + C \cdot D$



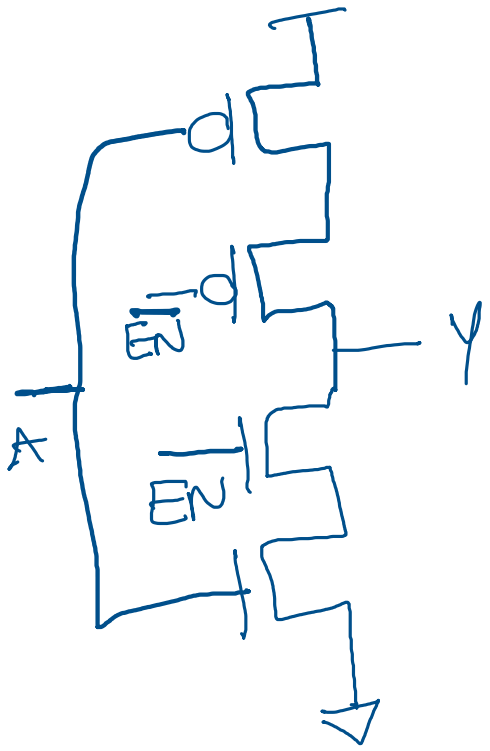
Tristate logic :-

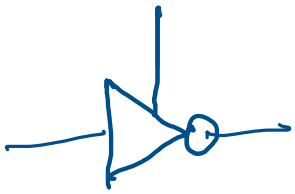
EN / $\overline{EN}$	A	Y
0 / 1	0	Z
0 / 1	1	Z
1 / 0	0	0
1 / 0	1	1

TG or PG has only 2 transistors and can be used to implement tristate buffer but it is a non restoring logic. If the input is corrupted due to noise, the same noisy i/p is passed

Tristate Inverter:

EN/$\overline{EN}$	A	Y
0/1	0	Z
0/1	1	Z
1/0	0	1
1/0	1	0





Practice:-

2:1 Multiplexer using TG and CMOS logic