SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

21ECC222L – ANALOG AND LINEAR ELECTRONIC CIRCUITS LABORATORY

LABORATORY MANUAL

SEMESTER IV

Prepared By
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SRM
INSTITUTE OF SCIENCE & TECHNOLOGY
(Deemed to be University u/s 3 of UGC Act, 1956)

SRM Institute of Science and Technology

Tiruchirappalli,

21ECC222L	ANALOG AND LINEAR ELECTRONIC CIRCUITS LABORATORY	Periods per week				Credits
		L	T	P	R	
Regulation - R21		**0**	**0**	**4**		**2**

PREREQUISITES:
Nil

COURSE OBJECTIVES:	
1.	understand the operation of BJT and MOSFET amplifier
2.	study the concept of multi stage amplifier and differential amplifier
3.	understand class C power amplifier and oscillator
4.	study various Op amp configurations and comparator applications
5.	design and implement filters and Digital to analog converters

COURSE OUTCOMES (COs):		
Upon completion of this course, student will be able to:		Bloom's level
CO1:	Compile the operation of BJT and MOSFET amplifier	K4
CO2:	Design multistage amplifier and differential amplifier	K5
CO3:	Implement class C power amplifier and oscillator in electronic application	K6
CO4:	Design linear and nonlinear application of op amp	K5
CO5:	Illustrate filters and digital to analog converters	K3

MAPPING OF COURSE OUTCOMES (CO) WITH PROGRAMME OUTCOME (PO)												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	2	-	3	-	-	-	-	-	-	-	
CO2	2	2	-	3	-	-	-	-	-	-	-	
CO3	2	2	-	3	-	-	-	-	-	-	-	
CO4	2	2	-	-	-	-	-	-	-	-	-	
CO5	2	2	-	-	-	-	-	-	-	-	-	
3 – High : 2 - Medium : 1 – Low : '-' - No correlation												

List of Experiments

1. BJT configuration, input characteristics, output characteristics, transient analysis, frequency response,
2. common source amplifier with current series feedback transient and frequency response, common source amplifier with voltage series feedback transient and frequency response.
3. Cascode amplifier transient response and frequency response, Bandwidth calculation.
4. Differential amplifier frequency response, common mode gain, differential mode gain, common mode rejection ratio.
5. Class C power amplifier transient response, Class C power amplifier frequency response, quality factor,
6. Design of LC oscillator, feedback fraction, frequency of oscillation.

7. Inverting amplifier noninverting amplifier, voltage follower, closed loop gain, Inverting comparator, non-inverting comparator, Schmitt trigger, upper threshold point, lower threshold point calculation,
8. monostable multivibrator using IC 555, Astable multivibrator, duty cycle measurement.
9. Butterworth low pass filter frequency response, Butterworth high pass filter frequency response,
10. Bandpass filter, Band reject filter, R-2R ladder type digital to analog converter.

TOTAL PERIODS:	**60**

Learning Resources :

1. David A. Bell, "Electronic Devices and Circuits", 5th ed., Oxford University Press, 2015
2. Donald Neaman,"Electronic Circuits: Analysis and Design", 3rd ed., Mc-Graw-Hill Education, 2011
3. Muhammad Rashid, "Microelectronic Circuits: Analysis and Design" 2nd ed., Cengage Learning, 2010
4. Robert L. Boylastaed Louis Nashelsky, "Electronic Devices and Circuit Theory", 11th ed.Peason Education, 2013

List of Experiments (Analog Circuits) – Cycle I	
1.	Design and analyze BJT amplifier (CE, CC & CB) & configurations

2.	Design and analyze multistage amplifier configurations
3.	Design & analyze differential amplifier
4.	Design and analyze LC oscillators
5.	Classes of power amplifier – Class C
6.	Design and analyze FET CS amplifier with active load (MOSFET)
7.	Design and analyze RC oscillators (Content Beyond syllabus - Experiment)

List of Experiments (Linear Electronic Circuits) – Cycle II	
1.	Basic op-amp circuits, Integrators and differentiators
2.	Comparators
3.	Astable Multivibrator using IC 555
4.	Monostable Multivibrator using IC 555
5.	Active Low Pass and High Pass Filter , Active Band Pass Filter
6.	DAC - R- 2R ladder type
7.	Voltage Regulator Using LM 317 (Content Beyond syllabus - Experiment)

List of Experiments (Linear Electronic Circuits) – Cycle II	
1.	Basic op-amp circuits, Integrators and differentiators
2.	Comparators
3.	Astable Multivibrator using IC 555
4.	Monostable Multivibrator using IC 555
5.	Active Low Pass and High Pass Filter , Active Band Pass Filter
6.	DAC - R- 2R ladder type
7.	Voltage Regulator Using LM 317 (Content Beyond syllabus - Experiment)

EX.NO: 1 (A)

DATE:

DESIGN AND ANALYZE FREQUENCY RESPONSE OF COMMON COLLECTOR AMPLIFILER

AIM:

To design a Common Collector amplifier with self bias and determine the voltage gain to plot the frequency response.

a. Gain of the amplifier
b. Bandwidth of the amplifier
c. Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	60kΛ, 1kΛ, 2.2kΛ ,10kΛ	Each 1
4	Power supply	(0-30)V	1
5	Transistors	BC 107	1
6	Capacitors	10μF	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A common collector amplifier is type of BJT amplifier which increases the voltage level of the applied input signal V_{in} at output of collector.

The CC amplifier typically has a relatively high input resistance (1 - 10 KΩ) and a fairly high output resistance. Therefore it is generally used to drive medium to high resistance loads. It is typically used in applications where a small voltage signal needs to be amplified to a large voltage signal like radio receivers.

The input signal Vin is applied to base emitter junction of the transistor and amplifier output Vo is taken across collector terminal. Transistor is maintained at the active region by using the resistors R1,R2 and Rc. A very small change in base current produces a much larger change in collector current

The output Vo of the common emitter amplifier is 180 degrees out of phase with the applied the input signal V_{in}

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CC amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CC amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for at least 20 different values for the considered range.
5. The voltage gain is calculated as

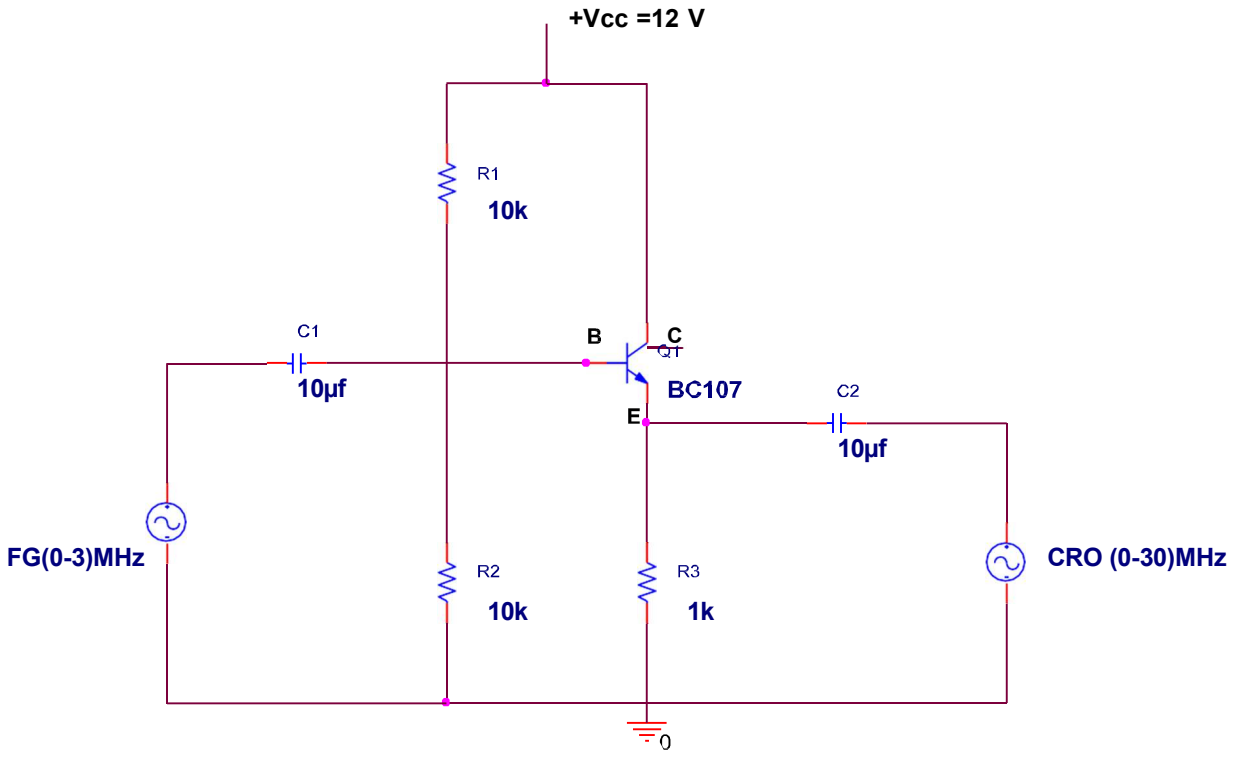
$$\mathbf{A_V = 20\log (V_0/V_i)\ dB}$$

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

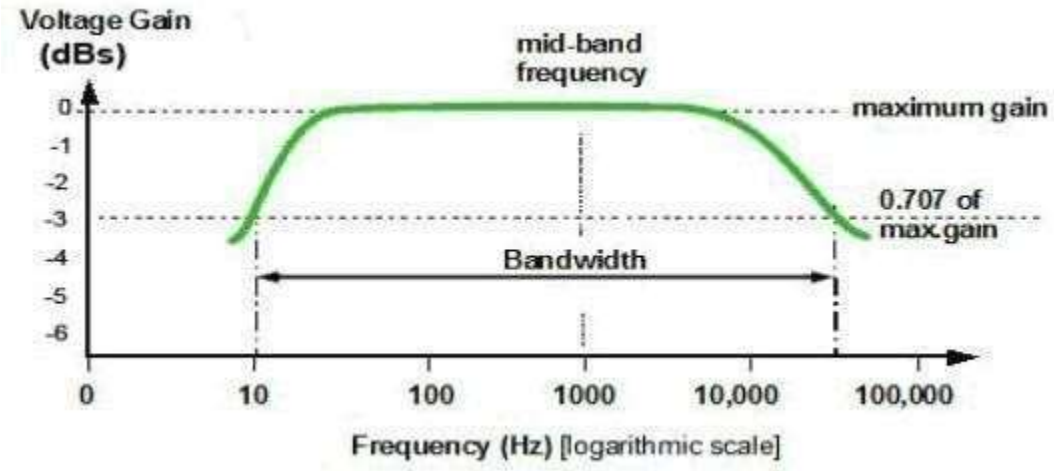
Bandwidth, BW = f_2-f_1

where
f_1 lower cut-off frequency
f_2 upper cut-off frequency

COMMON COLLECTOR CIRCUIT DIAGRAM:



MODEL GRAPH



TABULATION:

Input voltage constant (vin) =

FREQUENCY (in Hz)	OUTPUT V_O(V)	Gain in dB= 20log(V_o/V_{in}) dB

RESULT:

Thus the Common Collector amplifier was constructed and the frequency response curve I has been plotted.

EX.NO: 1(b)
DATE:

DESIGN AND ANALYZE FREQUENCY RESPONSE OF COMMON BASE AMPLIFILER

AIM:

To design a Common Base amplifier with self bias and determine the voltage gain to plot the frequency response.

a. Gain of the amplifier
b. Bandwidth of the amplifier
c. Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1kΛ, ,10kΛ	Each 1
4	Power supply	(0-30)V	1
5	Transistors	BC 107	1
6	Capacitors	10μF,1 μF	Each 1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A common base amplifier is type of BJT amplifier which increases the voltage level of the applied input signal Vin at output of collector.

The Common base amplifier typically has good voltage gain and relatively high output impedance. But the Common base amplifier unlike CE amplifier has very low input impedance which makes it unsuitable for most voltage amplifier. It is typically used as an active load for a cascode amplifier and also as a current follower circuit.

Circuit Operation:

A positive-going signal voltage at the input of a CB pushes the transistor emitter in a positive direction while the base voltage remains fixed, hence Vbe reduces. The reduction in V_{BE} results in reduction in V_{RC}, consequently V_{CE} increases. The rise in collector voltage effectively rises the output voltage. The positive going pulse at the input produces a positive-going output, hence the there is no phase shift from input to output in CB circuit. In the same way the negative-going input produces a negative-going output.

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CB amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CB amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

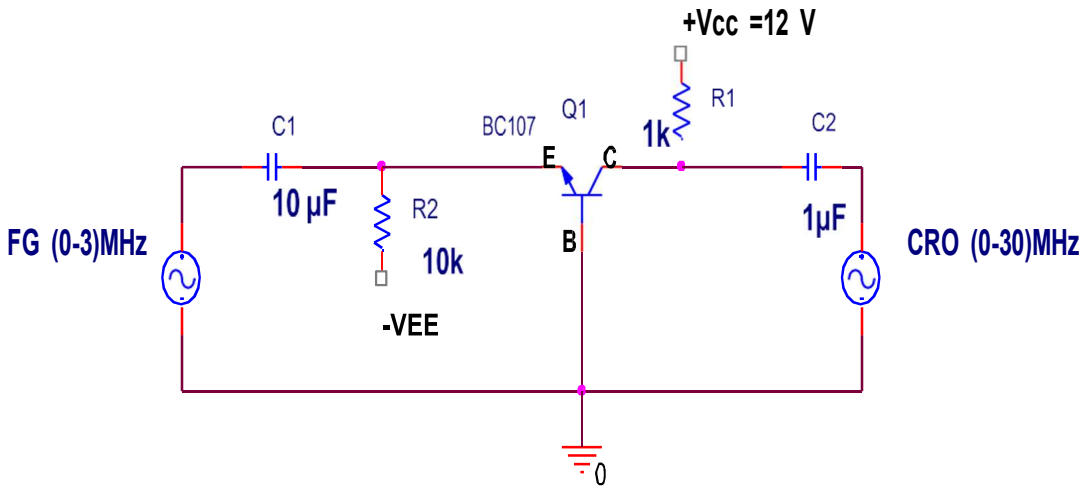
$$\mathbf{A_V = 20\log (V_0/V_i)\ dB}$$

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

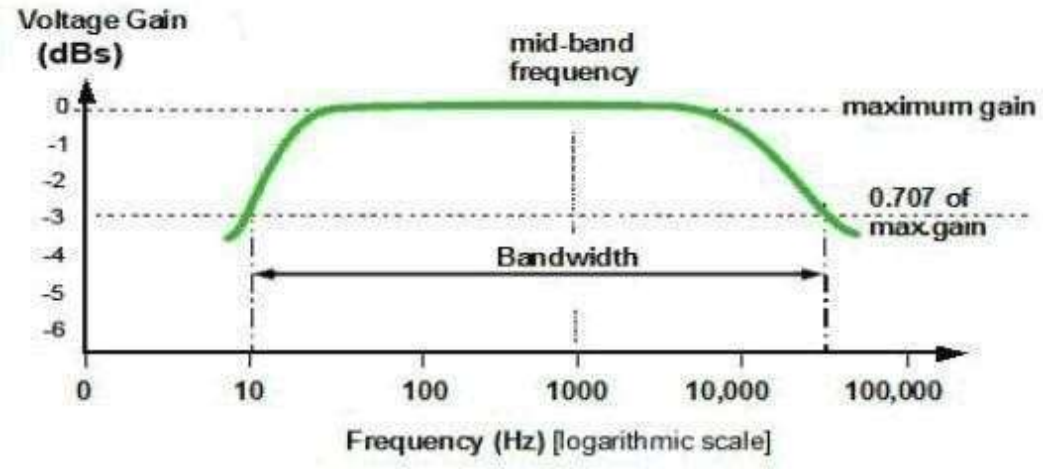
Bandwidth, BW = f_2-f_1

where
f_1 lower cut-off frequency
f_2 upper cut-off frequency

COMMON BASE CIRCUIT DIAGRAM:



MODEL GRAPH :



TABULATION:

Input voltage constant (V in) =

FREQUENCY (in Hz)	OUTPUT V_O(V)	Gain in dB= 20log(V_o/V_{in}) dB

RESULT:

Thus the Common Base amplifier was constructed and the frequency response curve has been plotted.

EX.NO: 2

DATE:

DESIGN AND ANALYZE MULTISTAGE AMPLIFIER CONFIGURATIONS

AIM:

To design and construct a multistage amplifier and to plot the frequency response characteristics.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1KΛ,	3
		10KΛ,25KΛ,270 KΛ,120 KΛ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	1
6	Capacitor	0.01µf,10mf	2,1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

The cascode configuration has one of two configurations of multistage amplifier. In each case the collector of the leading transistor is connected to the emitter of the following transistor. The arrangement of the two transistors is shown in the circuit diagram. The cascode amplifier consists of CE stage connected in series with CB stage. The arrangement provides a relatively high input impedance with low voltage gain for the first stage to ensure the input miller capacitance is at a minimum, whereas the following CB stage provides an excellent high frequency response.

Features:

1. It provides high voltage gain and has high input impedance.
2. It provides high stability and has high output impedance

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CE amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CE amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

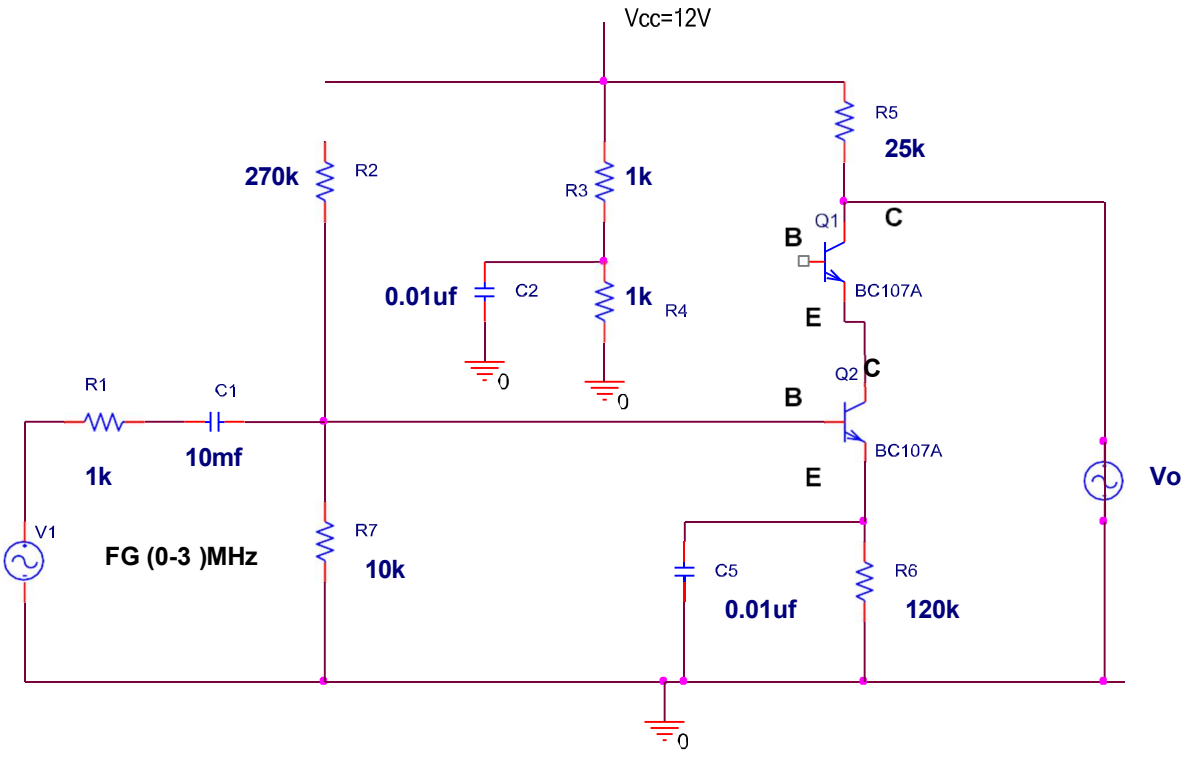
$$\mathbf{A_V = 20\log (V_0/V_i)\ dB}$$

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

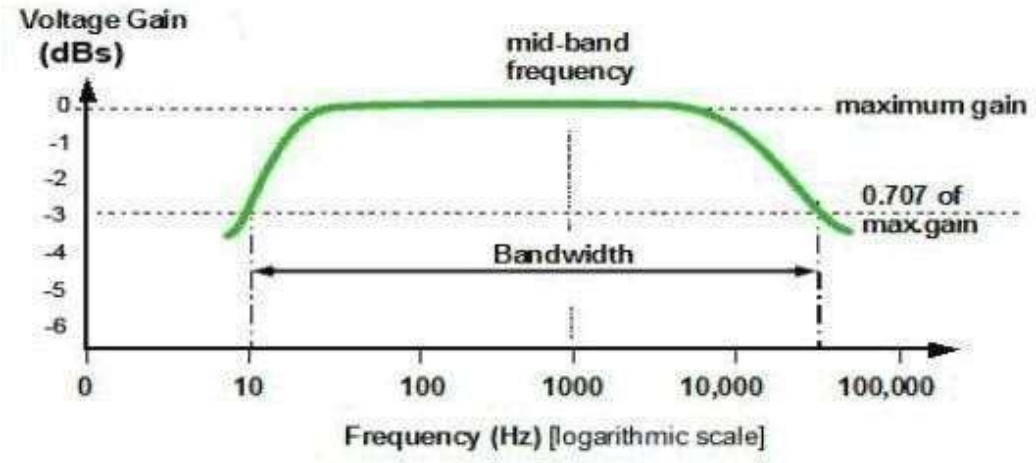
Bandwidth, BW = f_2-f_1

where
f_1 lower cut-off frequency
f_2 upper cut-off frequency

CIRCUIT DIAGRAM:



MODEL GRAPH :



TABULATION:

Input voltage constant (vin) =

FREQUENCY (in Hz)	OUTPUT V_O(V)	Gain in dB= 20log(V_o/V_{in}) dB

RESULT:

Thus multistage amplifier was constructed and the frequency response curve has been plotted in graph.

EX.NO: 3

DATE:

DESIGN AND ANALYZE DIFFERENTIAL AMPLIFIER

AIM:

To Design and Construct a Differential **A**mplifier using BJT and to determine its:

a. Transfer Characteristics.
b. Gain of the amplifier in common mode.
c. Gain of the amplifier in differential mode.
d. CMRR (Common Mode Rejection Ratio).

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1KΛ,1KΛ,10kΛ,4.7KΛ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	1
6	Bread Board	-	1
7	Connecting Wires	Single strand	as required

THEORY:

A differential amplifier is a type of electronic amplifier that amplifies the difference between two voltages but does not amplify the particular voltages. The need for differential amplifier arises in many physical measurements where response from D.C to many MHZ is required. It is also used in input stage of integrated amplifier.

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the Differential amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to amplifier using AC analysis.
4. Determine the Transfer characteristics of Differential amplifier by plotting the graph for normalized differential input voltage [$(Vb1 – V_{b2}) / V_T$] vs. Normalized collector current [Ic / Io].
5. Calculate the voltage gain of differential amplifier for differential mode as

$$A_d = 20\log (V_0/V_i)$$

Where Vi = V1 – V2

6. Calculate the voltage gain of differential amplifier for Common mode as

$$AC = 20\log (V0/Vi)$$

Where Vi = (V1+ V2 / 2)

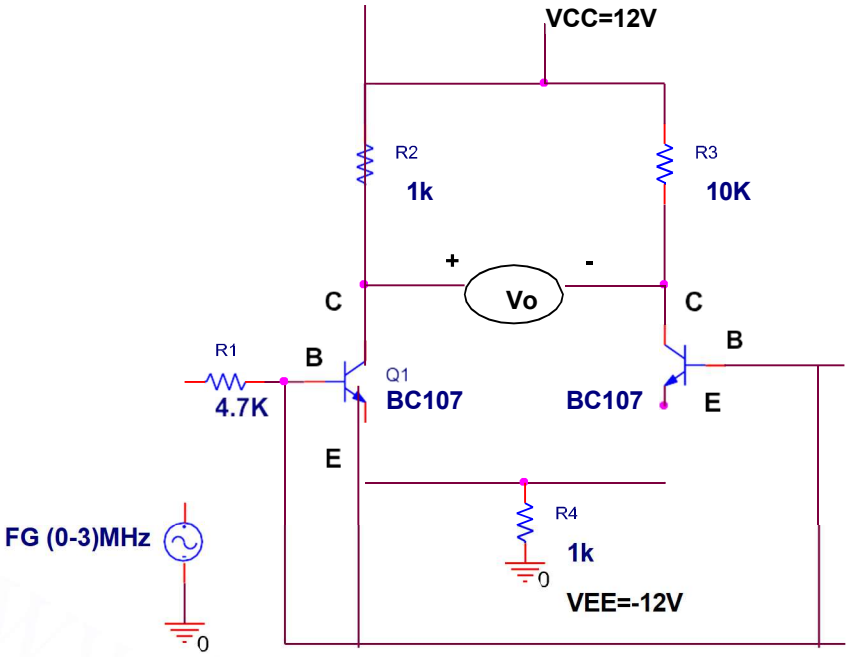
7. Find the Common mode rejection ratio of differential amplifier using the formula given below.

$$CMRR= 20 \log10 (Ad/Ac)$$

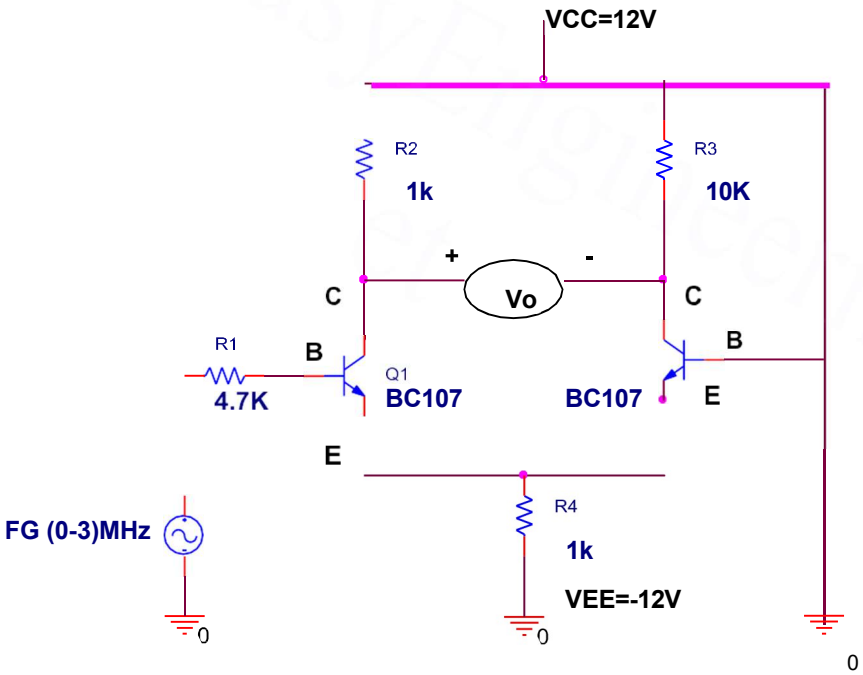
Where Ad- Differential mode gain in dB

Ac – Common Mode gain in dB

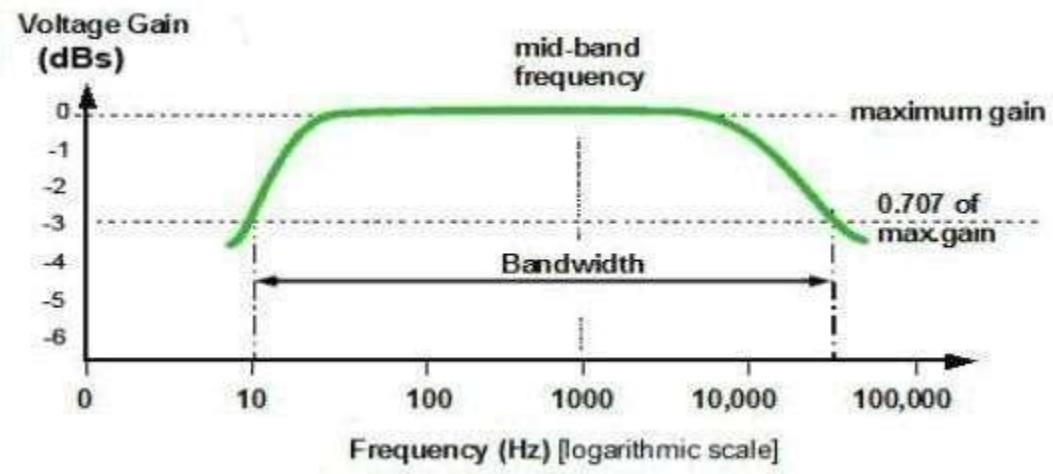
COMMON MODE CIRCUIT DIAGRAM:



DIFFERENTIAL MODE CIRCUIT DIAGRAM:



MODEL GRAPH :



TABULATION:

Common Mode (V in) =

Differential Mode (Vin) =

S.No	Frequency (in Hz)	Vo (in volts)		Gain in dB= $20\log(V_o/V_{in})$dB		CMRR(dB)
		Common mode	Differential Mode	Common mode	Differential Mode	

TRANSFER CHARACTERISTICS CALCULATION:

S.NO	INPUT VOLTAGE V_I = (VB1 – VB2) IN VOLTS	OUTPUT CURRENT I_{C2} IN AMPERE
1.		
2.		
3.		
4.		
5.		
6.		

RESULT:

Thus the gain of the differential amplifier was constructed and the frequency response curve has been plotted

Ex.No: 4

DATE:

DESIGN AND ANALYZE LC OSCILLATORS

AIM:

To design a Wein bridge oscillator and to generate sinusoidal wave form.

APPARATUS REQUIRED:

Sl. No.	Components	Specification	Quantity
1	Transistor	BC 107	2
2	Resistance	4.7K,680K,10K,47K	2(each)
		2.7K,1.2K	1(each)
			1
3	Capacitance	0.01μf	2
		47μf,0.01	1(each)
4	AFO,CRO, Bread board		1(Each)
5	Connecting wires		As required
6	Power Supply	(0-30V)	1

THEORY:

Wien Bridge oscillator is one of the most popular type of sinusoidal oscillator which used in audio and sub-audio frequency range(2-20KHZ).The maximum output frequency of a typical Wien bridge oscillator is only about 1MHZ. This is also infact a phase –shift oscillator. It employs two transistors each producing a phase shift of 180 degree, and thus producing a total shift of 360 degree .It is essentially a two stage amplifier with an R-C bridge circuit. R-C bridge circuit is a lead – lag networK. By adding Wien bridge feedbacK networK, the oscillatorbecomes sensitive to a signal of only one particular frequency. This particular frequency is that atwhich Wien Bridge is balanced and for which the phase shift is 0 degree. Thus by employing wien bridge feedbacK networK frequency stability is increased.

PROCEDURE:

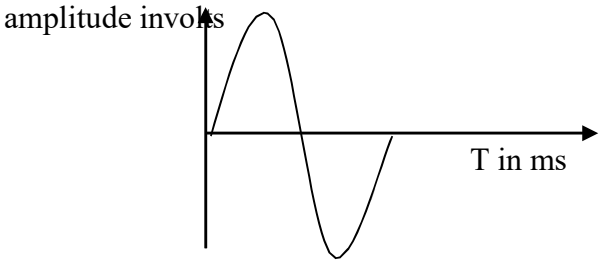
1. The connections are made as per the circuit diagram.
2. Observe the output and measure the amplitude and time period of the output waveformV_o.
3. Measure the amplitude and frequency of oscillator.
4. Plot the output.

CIRCUIT DIAGRAM:

TABULATION:

Amplitude in volts	Time period (ms) (T)	Frequency in Hz (f= 1/ T)

MODEL GRAPH



FREQUENCY:

RESULT:

The Wien bridge oscillator is designed and the frequency of oscillation is obtained

Theoretical frequency: Hz

Practical frequency: Hz.

EX.NO: 5

DATE:

CLASS C AMPLIFIER

AIM:

To construct a Class A power amplifier and observe the waveform and to compute maximum output power and efficiency.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1 KΛ,330Λ,220KΛ,220 Λ	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	1
6	Capacitor	4.7µf,	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

The power amplifier is said to be Class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input signal cycle. For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally. The collector current flows for 360 (full cycle) of the input signal. i e the angle of the collector current flow is 360 .

PROCEDURE:

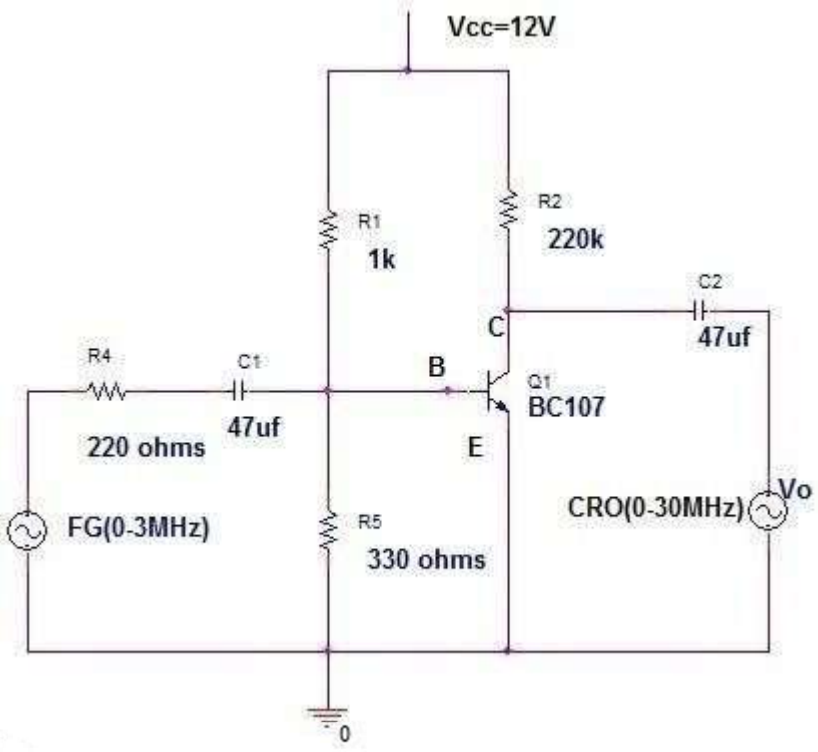
1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mv, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 10 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) vs Frequency (Hz).

FORMULA

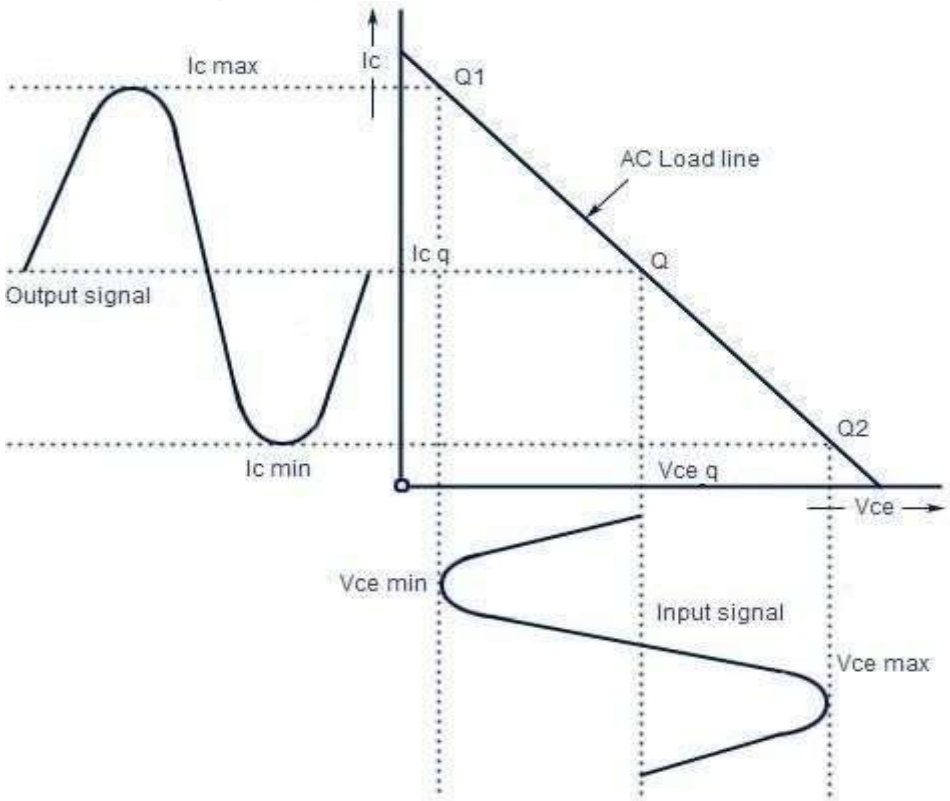
Maximum power transfer = $P_{o,max}=V_o^2/R_L$

Efficiency ,$\eta = P_{o,max}/P_c$

CLASS A AMPLIFIER CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

Signals	Amplitude (volt)	Time period (sec)
Input signal		
Output signal		

RESULT :

Thus the Class A amplifier was constructed and observed the waveforms values are plotted in graph.

EX.NO:6

DATE:

DESIGN AND ANALYZE F E T COMMON-SOURCE AMPLIFIER (MOSFET)

AIM:

To design and construct a common-source amplifier circuit and to determine its frequency response.

COMPONENTS & EQUIPMENTS REQUIRED:

S.NO	COMPONENT	RANGE	QUANTITY
1	Transistor	BFW 10	1
2	RPS	(0-30)V	1
3	Signal Generator	(0-3)MHz	1
4	CRO	(0-30)MHz	1
5	Bread Board	-	1
6	Resistors	10K, 2.2K, 3.3M	1
7	Capacitors	0.1uf	2
8	Single strand Wires	-	-
9	CRO Probes	-	3

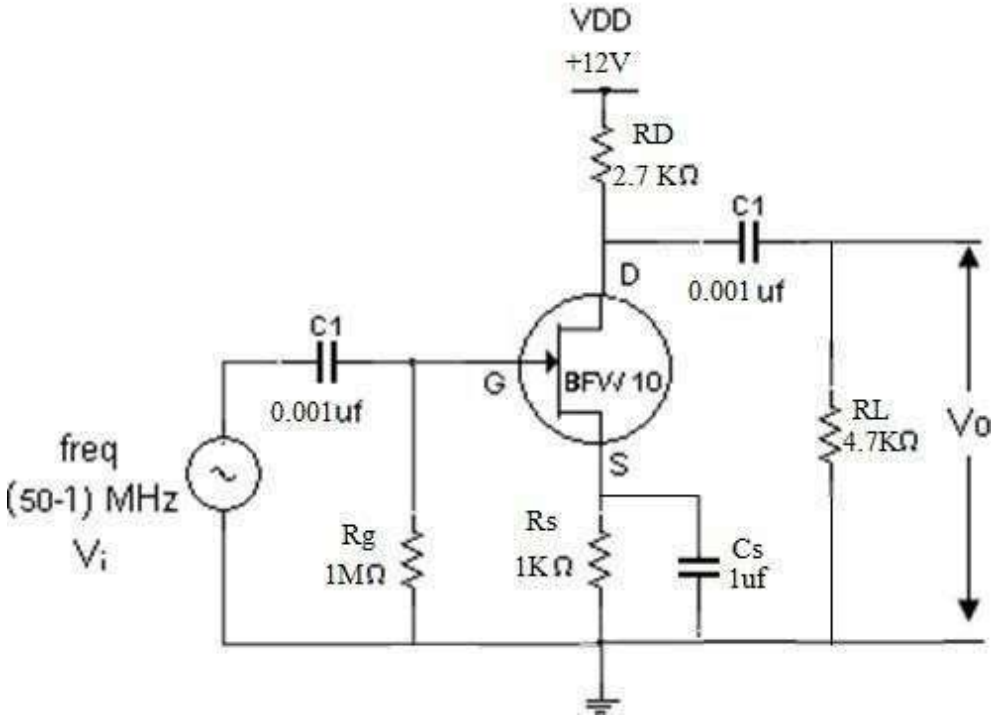
PROCEDURE:

1. Connect the circuit diagram as per the circuit diagram.
2. Set Vi = 50mV, using the signal generator.
3. Keeping the input voltage constant, Vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: Gain (dB) vs Frequency (Hz)
5. Calculate the bandwidth from the graph.

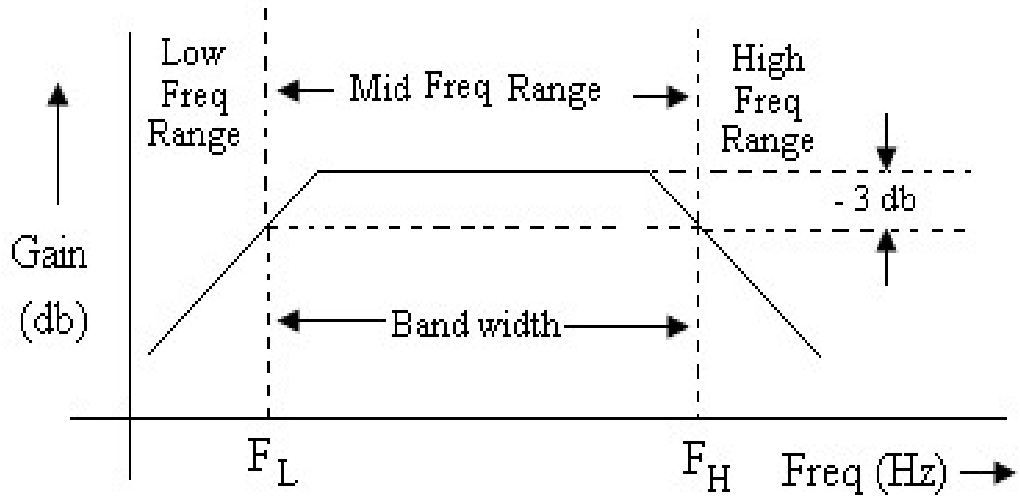
THEORY :

The common source configuration for a FET is similar to the common emitter bipolar transistor configuration, The common source amplifier can provide both a voltage and current gain. Since the input resistance looking into the gate is extremely large the current gain available from the FET amplifier can be quite large, but the voltage gain is generally inferior to that available from a bipolar device. Thus FET amplifiers are most useful with high output-impedance signal sources where a large current gain is the primary requirement. The source by-pass capacitor provides a low impedance path to ground for high frequency components and hence AC signals will not cause a swing in the bias voltage.A basic common-source amplifier circuit containing an N-channel JFET. The characteristics of this circuit include high input impedance and a high voltage gain. The function of the circuit components are C1 and C2 are the input and output coupling capacitors. Rg is the gate return resistor.

CIRCUIT DIAGRAM OF COMMON SOURCE AMPLIFIER



Model Graph



Design Specifications

V_{DD}=12V, V_{GS}=-2V, for N-Channel JFET (BFW10) Ro=40K, and g_m=2.5mA/V at I_D=2mA, and V_P=8V

Design of Rg

Select Rg=1MΩ (since voltage across Rg assumed to be 0V)

Design of R_D

V_{RD}=45% of V_{DD} = 5.4V

$V_{RD}=I_d*R_D$

RD= V_{RD}/I_d= 2.7KΩ

Design of R_S

$Rs=V_{RS}/I_S=V_{RS}/I_D$ ($I_D=I_S$=2mA)

V_{RS}=Vg-VGS

V_{RS} =0-(-2V) =2V

$RS=2/2*10^{-3}$=1KΩ

Design of R_L

Gain of CS amp $A=gm(R_D \| R_L)$

The required gain=15

R_L=4.7KΩ

To find C_S (Bypass capacitor)

X_{CS} =R_S / 10 =1000 /10 =100

X_{CS} =100

X_{CS} =1 / 2π f C_S

Let f=1000

C_S = 1 / 2π f X_{CS}

C_S = 1 / 2*π *1000* 100

C_S = 1 μf

To find C_i (Input capacitor)

X_{Ci} =Rg /10=0.1MΩ

X_{Ci} =1 / 2π f C_i

Let f=1000

C_i = 1 / 2π f X_{Ci}

C_i = 1 / 2*π *1000* 0.1MΩ

C_i = 0.001 μf

To find C_O (Output capacitor)

X_{CO} =R_S / 10 = 100

X_{CO} =1 / 2π f C_O

Let f=1000

C_O = 1 / 2π f X_{CO}

C_O = 1 / 2*π *1000* 1000

C_O =1.5 μf use approx 1 μf

TABULATION:

S.NO	Frequency in Hz	Vo in Volts	Gain : 20 Log(Vo/Vin)

RESULT:

Thus the common source amplifier has been constructed, and frequency response of the amplifier has drawn.

Ex.No: 7

DATE:

DESIGN AND ANALYZE RC PHASE SHIFT OSCILLATORS

AIM:

To design a RC phase shift oscillator to generate a sinusoidal Waveform.

APPARATUS REQUIRED:

Sl. No.	Components	Specification	Quantity
1	Transistor	BC 107	1
2	Resistance	2.2K,56k,560Ω	1(each)
		6.2k	4
3	Capacitance	0.01µf	4
		10 µf,47µf	1(each)
4	AFO, CRO, Bread board		1(each)
5	Connecting wires		As required
6	Power supply	(0-30V)	1

THEORY:

Oscillator is a feedback circuit where a fraction of output voltage of an amplifier is fed back to the input in the same phase. RC phase shift oscillators are a sine wave oscillator which is used in the audio frequency range. It has a CE amplifier ,which provides 180°.phase shift to the input signal and three frequency selective RC phase shift networks provides a phase shift of 60°of each , a total of 180° for a signal with frequency equal to specific value, which corresponds to the output of the oscillator. Thus the total phase shift between the input and output is360°.

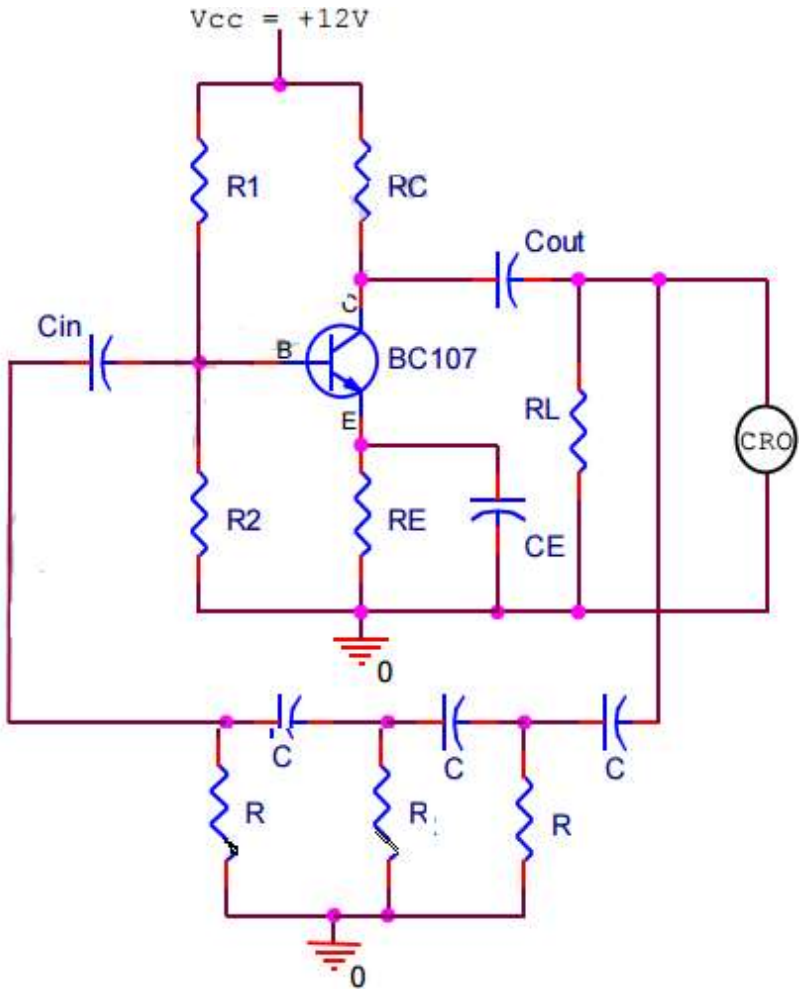
PROCEDURE:

1. The connection is made as per the circuit diagram.
2. Set the RPS to 20Volts.
3. Observe the output and measure the time period of the output waveform V_o, determine the frequency and trace it
4. Plot the output on a graph sheet.

Compare the experimental value with the theoretical value of output frequency

CIRCUIT DIAGRAM:

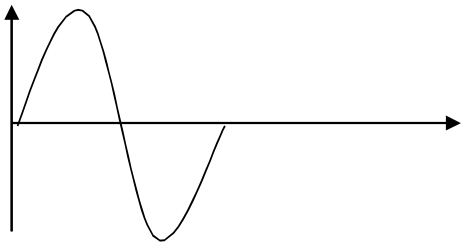
RC PHASE SHIFT OSCILLATOR



TABULATION:

Amplitude in volts	Time period (ms) (T)	Frequency in Hz (f= 1/ T)

MODEL GRAPH



Frequency:

Amplitude:

RESULT:

The RC phase shift oscillator is designed and the frequency of oscillation is obtained Theoretical frequency: Hz.

Practical frequency: Hz.

List of Experiments (Linear Electronic Circuits) – Cycle II	
8.	Basic op-amp circuits, Integrators and differentiators
9.	Comparators
10.	Astable Multivibrator using IC 555
11.	Monostable Multivibrator using IC 555
12.	Active Low Pass and High Pass Filter , Active Band Pass Filter
13.	DAC - R- 2R ladder type
14.	Voltage Regulator Using LM 317 (Content Beyond syllabus - Experiment)

Ex. No : 1	**BASIC OP-AMP CIRUITS**
DATE :	

AIM:

1. To measure the following parameters of op-amp.
   i)Input bias current ii) Input offset voltage

2. To operate and obtain the output of i) Summing amplifier ii) Subtractor.

APPARATUS REQUIRED:

S.No.	APPARATUS	TYPE	RANGE	QUANTITY
1)	Op-Amp	µA741		1
2)	Resistors		100 / 10K / 1M	2 / 4/ 2
3)	Capacitors		0.01µF	1
4)	Signal Generator			1
5)	CRO			1
6)	Dual power supply			1
7)	Bread Board			1
8)	Connecting wires			

THEORY:

Input bias current: The inverting and noninverting terminals of an op-amp are actually two base terminals of transistors of a differential amplifier. In an ideal op-amp it is supported that no current flows through these terminals. However, practically a small amount of current flows through these terminals which is on the order of nA (typical and maximum values are 80 and 1500nA) in bipolar op-amps and pA for FET op-amps. Input bias current is defined as the average of the currents entering into the inverting and noninverting terminals of an op-amp. To compensate for bias currents a compensating resistor R_{comp} is used. Value of R_{comp} is parallel combination of the resistors connected to the inverting terminal. Input bias current $I_B = \frac{(I_{B1} + I_{B2})}{2}$, where I_{B1} and I_{B2} are the base bias currents of the op-amp.

Input offset voltage: Even if the input voltage is zero, output voltage may not be zero. This is because of the circuit imbalances inside the op-amp. In order to compensate this, a small voltage should be applied between the input terminals. Input offset voltage is defined as the voltage that must be applied between the input terminals of an op-amp to nullify the output voltage. Typical and maximum values of input offset voltage are 2mV and 6mV.

Summing Amplifier: Op-amp may be used to perform summing operation of several input signals in inverting in inverting and non-inverting mode. The input signals to be summed up are given to inverting terminal or non-inverting terminal through the input resistance to perform inverting and non-inverting summing operations respectively.

Subtractor: The basic difference amplifier can be used as a subtractor. The signals to be subtracted are connected to opposite polarity inputs i.e. in inverting or non-inverting terminals of the op-amp.

PROCEDURE:

i) Input Bias Current:

1. Connect the circuit as shown.
2. Measure the output voltage from which the inverting input bias current can be calculated as $I_B^- = Vo / R$
3. Connect the circuit as shown .
4. Measure the output voltage from which the non-inverting input bias current can be calculated as $I_B^+ = Vo / R_f$.
5. Average of magnitude of both I_B^- and I_B^+ gives the input bias current.

ii) Input Offset Voltage:

1. Connect the circuit as shown.
2. Measure the output voltage using multimeter.
3. Calculate offset voltage as $V_{ios} = V_o / (1+ R_f / R_1)$.

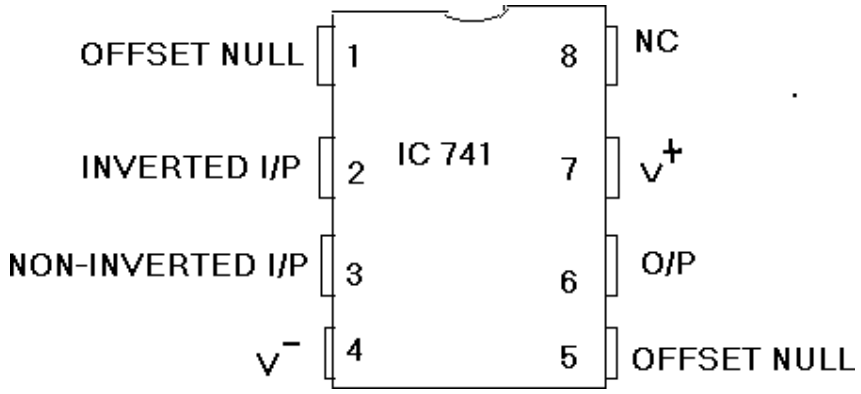
iii) Inverting Summing Amplifier:

1. Connect the circuit as shown in figure.
2. Connect batteries for voltage V_1, V_2.
3. Measure and note the output voltage and compare it with theoretical value , $Vo = -(R_f / R_i) (V_1+V_2)$.

iv) Subtractor:

1. Connect the circuit as shown in figure.
2. Measure and note the output voltage and compare it with theoretical value, $Vo = (V_1- V_2)$.

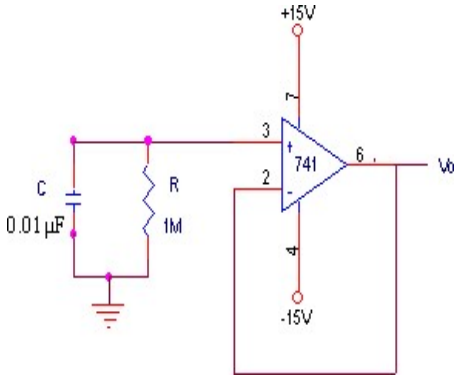
PIN DIAGRAM:

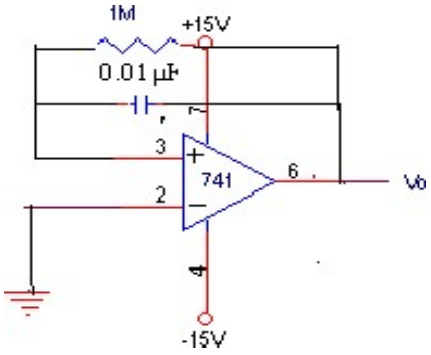


CIRCUIT DIAGRAMS:

1) To measure the following parameters:

i)To measure input bias current:

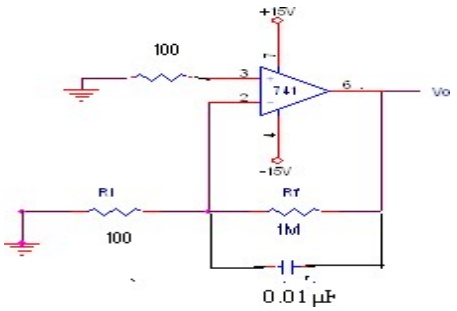




TABULAR COLUMN:

SI.NO	$I_B^- = Vo/R$	$I_B^+ = Vo/R_f$
	Input bias current , $I_B = \frac{I_B^+ + I_B^-}{2}$ =	

ii) To measure input offset voltage :



TABULAR COLUMN:

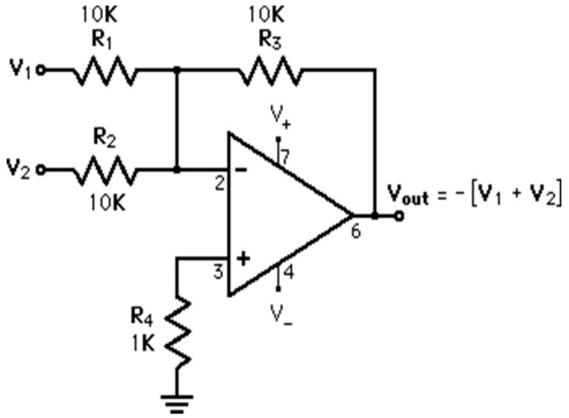
SI.NO	$V_{ios} = V_o / (1+ R_f / R_1)$..
	$V_o =$

TYPICAL VALUES OF ELECTRICAL CHARACTERISTICS OF µA741:

Input bias current = 80-500nA
Input offset voltage = 1-5mV

2. To know the applications of op-amp:

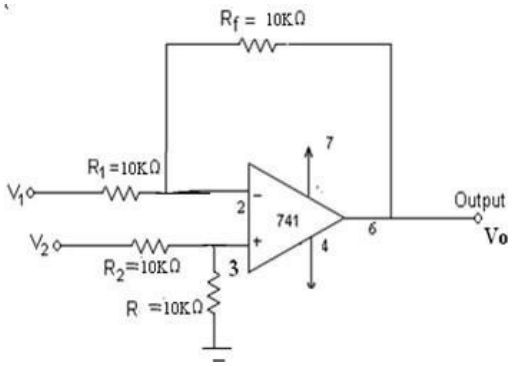
i) Summing Amplifier:



TABULAR COLUMN:

S.No.	V_1	V_2	Theoretical $V0 = -(V_1 + V_2)$	Practical V0

ii) Subtractor:



TABULAR COLUMN:

S.No.	V1	V2	Theoretical V0=V1-V2	Practical V0

RESULT:

1. The input bias current and input offset voltage of the op-amp were determined.

   Input bias current = ...A
   Input offset voltage = ... mV

2. The applications of op-amps like summing amplifier and subtractor were understood.

Ex. No : 1 (a)	INTEGRATORS AND DIFFERENTIATORS
DATE :	

AIM:

To demonstrate the use of op-amp as Integrator and Differentiator .

APPARATUS REQUIRED:

S.No.	APPARATUS	TYPE	RANGE	QUANTITY
1)	Op-Amp	µA741-		1
2)	Resistors		1.5K / 10K/ 15K / 100K	2/2/ /1 / 1
3)	Capacitors		0.1 µ F / 0.01 µ F	1 / 1
4)	Signal Generator			1
5)	CRO			1
6)	Dual power supply			1
7)	Bread Board			1
8)	Connecting wires			

THEORY:

Integrator: Integrator is used to integrate the input waveform. i.e; $V_O = \int V_{in}\, dt$. Here in the inverting amplifier configuration, the feedback resistor R_f is replaced by capacitor C_f. Integrators are commonly used in wave shaping news, signal generators etc. For proper wave integration, T >> RC. Gain and linearity of the o/p are two advantages of op-amp integrators. Linearity is due to linear charging of capacitor. Its limitation is for Vin=0 and for low frequencies, $X_{Cf} = \infty$ or the capacitor C_f acts as an open circuit. Therefore the op-amp integrator works as an open loop amplifier and the gain becomes infinity or very high.

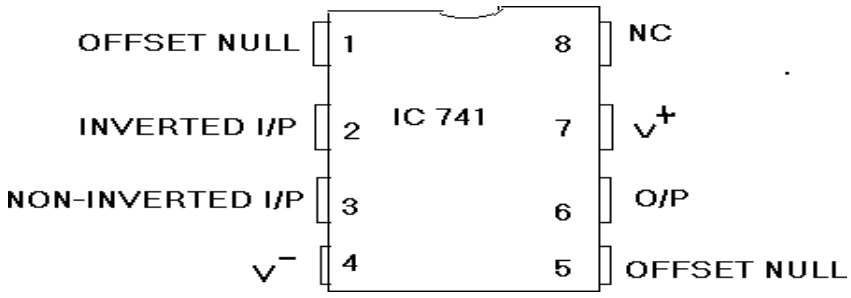
Differentiator: Here the output waveform is the derivative of the i/p waveform. In a basic inverting amplifier, if R_1 is replaced by C_1, we get the differentiator. But at high frequencies, the gain of the circuit (Rf/XC1) increases with increase in frequency at the rate of 20dB/decade. This makes the circuit unstable. Also X_{C1} decreases when frequency increases.

PROCEDURE:

Integrator & Differentiator:

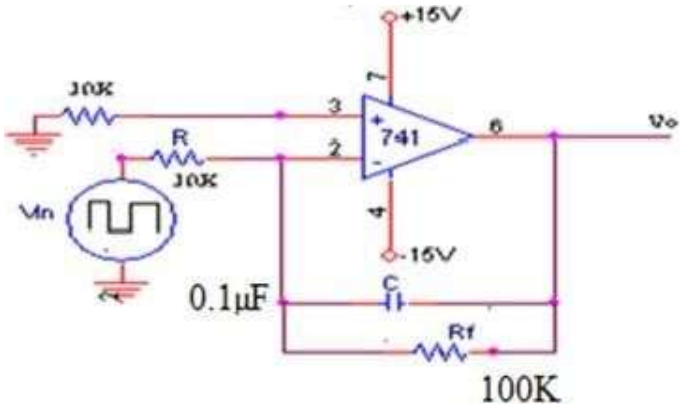
1. Connections are made as per the diagram.
2. Apply an i/p voltage of 1-2Vpp with 1kHz frequency and check the waveform on the CRO.
3. Measure the value of V_O by varying the frequency of the i/p signal.
4. Calculate gain using the formulae 20 log (V_O /V_{IN}).

PIN DIAGRAM:

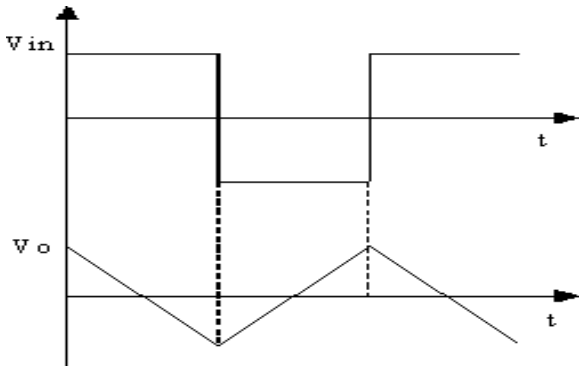


CIRCUIT DIAGRAM:

Integrator:



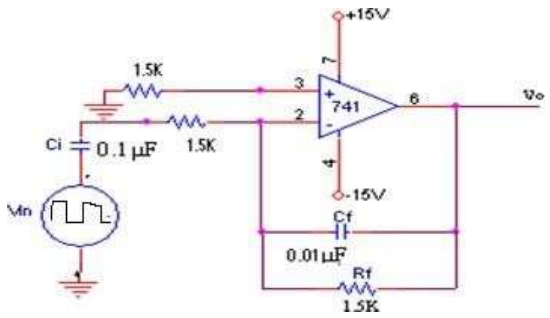
Model Graph:



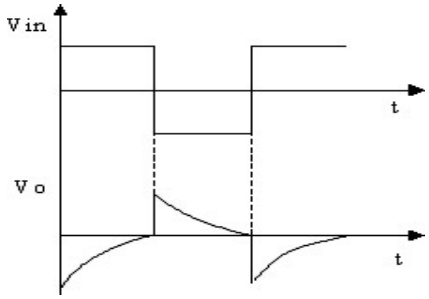
TABULAR COLUMN:

S.No:	INPUT		OUTPUT	
	Vin (V)	Time (msec)	Vout(V)	Time (msec)

Differentiator:



Model Graph:



TABULAR COLUMN:

S.No:	INPUT		OUTPUT	
	Vin (V)	Time (msec)	Vout(V)	Time (msec)

RESULT:

Thus the output waveforms of integrator and differentiator were obtained and the graphs were drawn.

Ex. No : 2	COMPARATORS
DATE :	

AIM : To obtain the output of voltage comparator and zero crossing detector.

APPARATUS REQUIRED:

S.No.	APPARATUS	TYPE	RANGE	QUANTITY
1)	Op-Amp	µA741		1
2)	Resistors		1K	2
4)	Signal Generator			1
5)	CRO			1
6)	Dual power supply			1
7)	Bread Board			1
8)	Connecting wires			

THEORY:

Voltage Comparator: A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with output $\pm V_{sat} = (V_{cc})$. If the signal is applied to the inverting terminal of the op-amp it is called inverting comparator and if the signal is applied to non-inverting terminal of the op-amp it is called non-inverting comparator. In an inverting comparator if input signal is less than reference voltage, output will be $+V_{sat}$. When input signal voltage is greater than reference voltage output will be $-V_{sat}$. The vice-versa takes place in non-inverting comparator.

PROCEDURE:

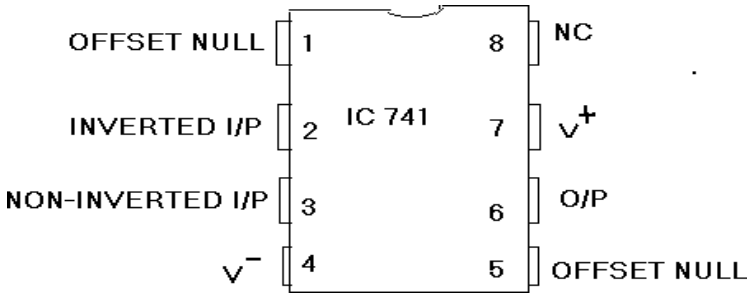
1) Voltage comparator:

1. Connect the circuit as shown in the figure.
2. Connect an alternating waveform to the non-inverting input of the op-amp.
3. Connect a reference voltage source to inverting input of the op-amp.
4. Plot the input and output waveforms.

2) Zero crossing detector:

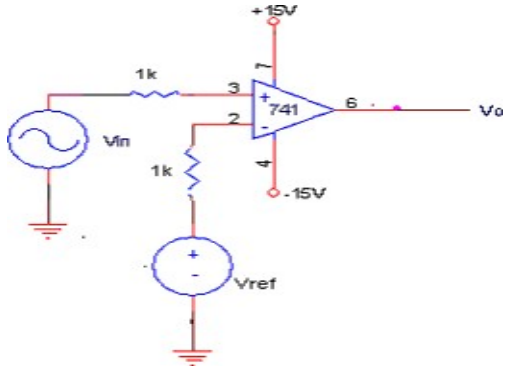
1. Connect the circuit as shown in figure.
2. Connect the input to a signal generator generating a sin wave with one volt peak to peak at 1kHz.
3. Connect the input and output to dual channel CRO and compare the input and output.
4. Plot the input and output waveforms on a graph.

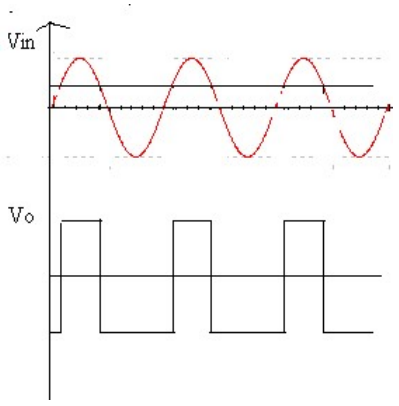
PIN DIAGRAM:



CIRCUIT DIAGRAM:

Voltage Comparator:

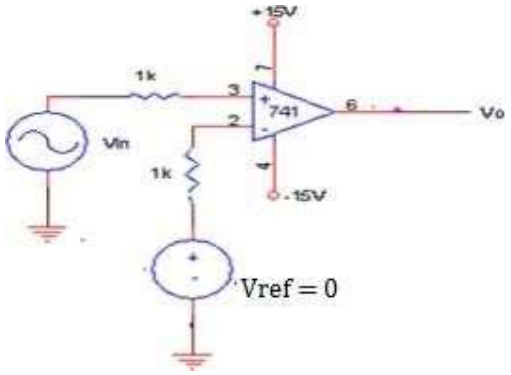




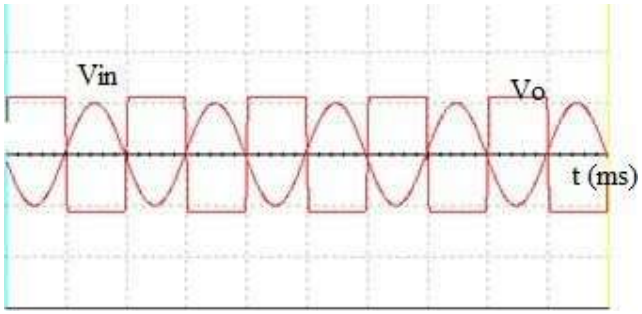
TABULAR COLUMN:

SI. NO	INPUT		OUTPUT	
	VOLTAGE (V)	TIME (ms)	VOLTAGE (V)	TIME (ms)

Zero Crossing Detector:



MODELGRAPH:



TABULAR COLUMN:

SI. NO	INPUT		OUTPUT	
	VOLTAGE (V)	TIME (ms)	VOLTAGE (V)	TIME (ms)

RESULT:

Thus the output of voltage comparator and zero crossing detector were obtained and the graphs have been drawn.

Ex. No : 3	Astable Multivibrator using IC 555
DATE :	

AIM:

To design and test astable multivibrator circuits using IC 555.

APPARATUS REQUIRED:

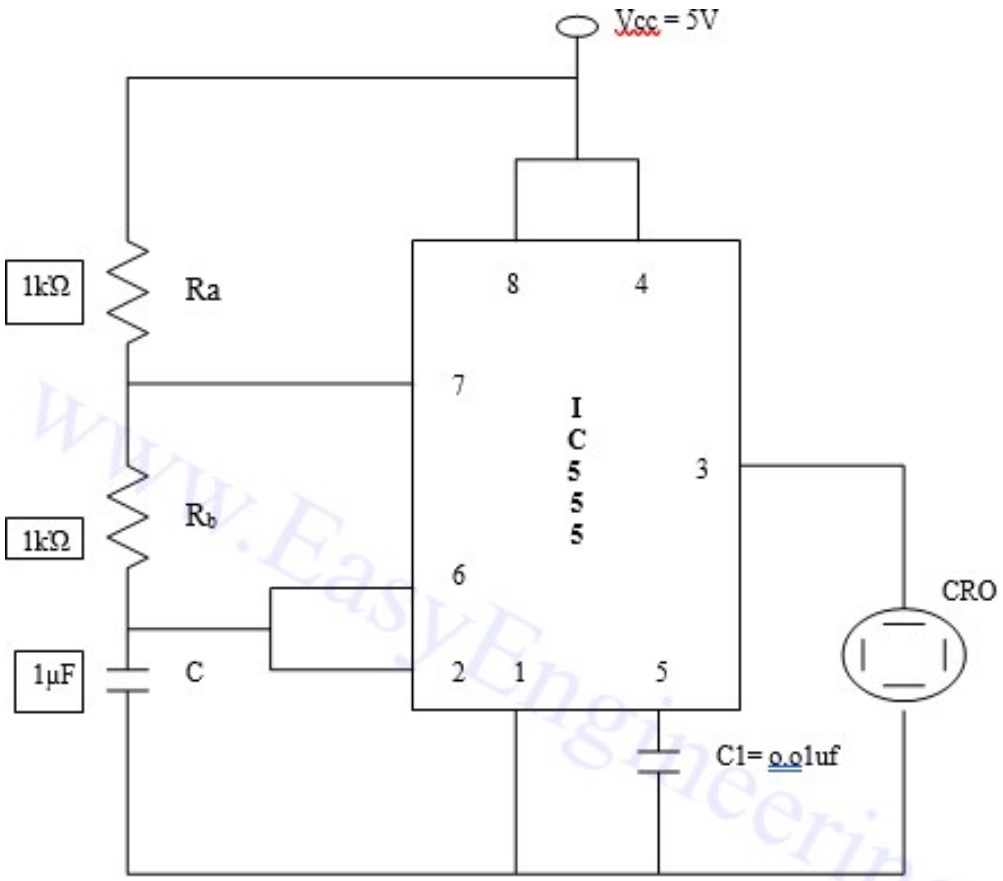
S.NO.	APPARATUS	RANGE	QUANTITY
1	Power Supply	(0 - +15)V	1
2	Signal generator	(0-1)MHz	1
3	CRO	(0-30)MHz	1
4	IC	IC 555	1
5	Resistor	1kΩ,2kΩ	1,1
6	Capacitor	0.1µf	1

THEORY:

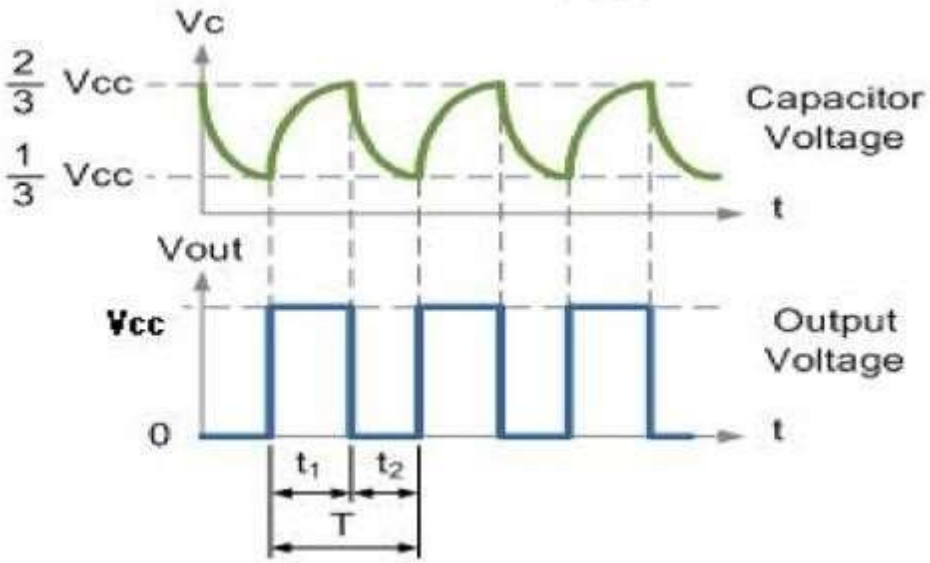
ASTABLE MULTIVIBRATOR:

The astable multivibrator is also called the free running multivibrator. It has two quasi states i.e. no stable states as such the circuit conditions oscillate between the components values used to decide the time for which circuit remains in each stable state. The principle of square wave output is to force the IC to operate in saturation region. Whenever input at the negative input terminal just exceeds Vref switching takes place resulting in a square wave output. In astable multivibrator both stable states and one quasi states are present.

CIRCUIT DIAGRAM:



MODEL GRAPH:(ASTABLE MULTIVIBRATOR)



TABULATION

S.NO	WAVEFORM	AMPLITUDE (V) *VOLTS*	TIME (T) *ms*	F =1/T *Hz*
1	CAPACITOR			
2	OUTPUT			

EXPERIMENTAL PROCEDURE:

1. Connections are as per the EXPERIMENTAL SETUP.
2. Supply is switched ON after checking the connections.
3. For monostable multivibrator trigger pulse is given and for stable it is not necessary.
4. Output square wave is noted from CRO.
5. The frequency is calculated by input.

RESULT:

Thus the Astable multivibrators is designed and tested using IC555

Ex. No : 4	Monostable Multivibrator using IC 555
DATE :	

AIM:

To design and test mono stable multivibrator circuits using IC 555.

APPARATUS REQUIRED:

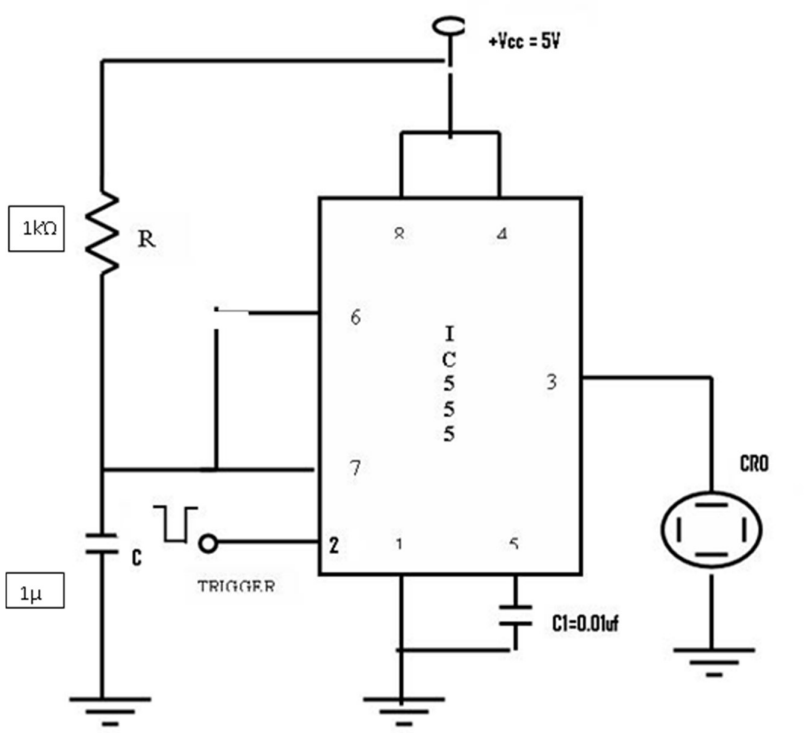
S.NO.	APPARATUS	RANGE	QUANTITY
1	Power Supply	(0 - +15)V	1
2	Signal generator	(0-1)MHz	1
3	CRO	(0-30)MHz	1
4	IC	IC 555	1
5	Resistor	1kΩ,2kΩ	1,1
6	Capacitor	0.1µf	1

THEORY:

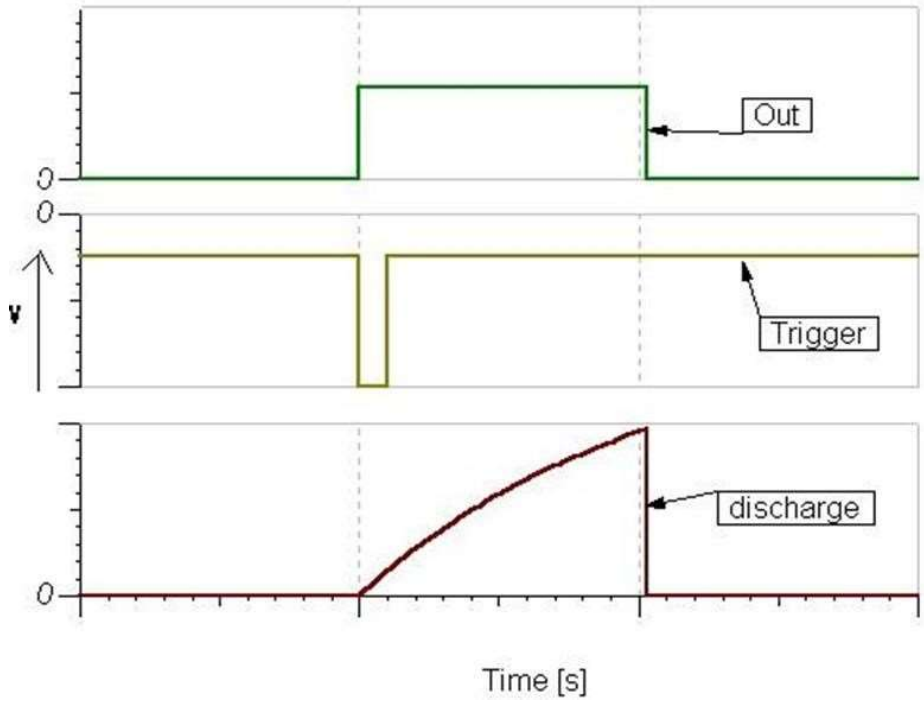
ASTABLE MULTIVIBRATOR:

The astable multivibrator is also called the free running multivibrator. It has two quasi states i.e. no stable states as such the circuit conditions oscillate between the components values used to decide the time for which circuit remains in each stable state. The principle of square wave output is to force the IC to operate in saturation region. Whenever input at the negative input terminal just exceeds V_{ref} switching takes place resulting in a square wave output. In astable multivibrator both stable states and one quasi states are present.

CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION

S.NO.	WAVEFORM	AMPLITUDE (V) *VOLTS*	TIME (T) *ms*	FREQ. f=1/T *Hz*
1	**CAPACITOR**			
2	**TRIGGER**			
3	**OUTPUT**			

EXPERIMENTAL PROCEDURE:

1. Connections are as per the EXPERIMENTAL SETUP.
2. Supply is switched ON after checking the connections.
3. For monostable multivibrator trigger pulse is given and for stable it is not necessary.
4. Output square wave is noted from CRO.
5. The frequency is calculated by input.

RESULT:

Thus the mono stable multivibrators is designed and tested using IC555

Ex. No : 5	ACTIVE LOW PASS AND HIGH PASS FILTER
DATE :	

AIM:

To design and test low pass and high pass filter using IC 741.

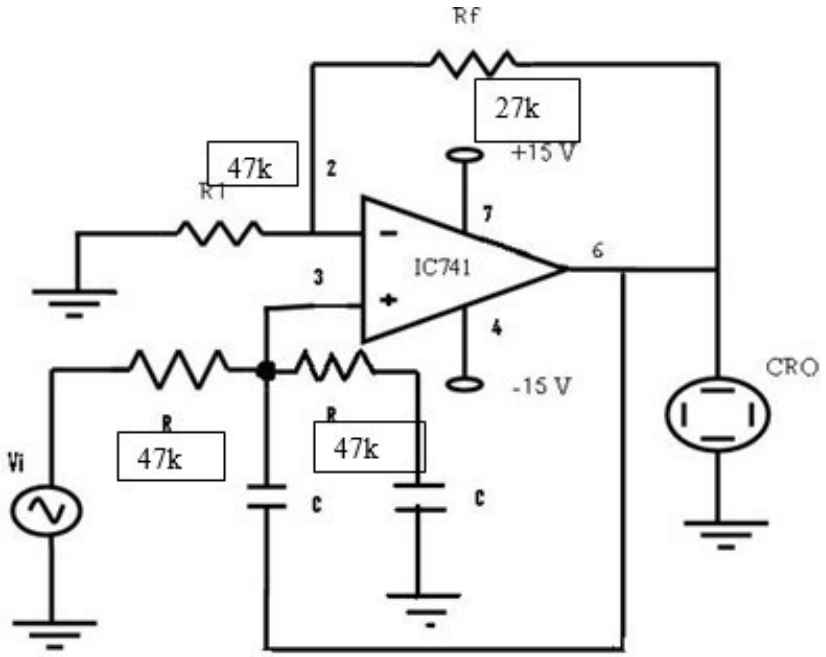
APPARATUS REQUIRED:

S.NO.	APPARATUS	RANGE	QUANTITY
1	Dual power supply	(0 - +15)V	1
2	CRO	(0-30)MHz	1
3	IC	µA 741	1
4	Resistor	10kΩ,5kΩ,	4,2
6	Capacitor	0.1µf,10µf	2,1

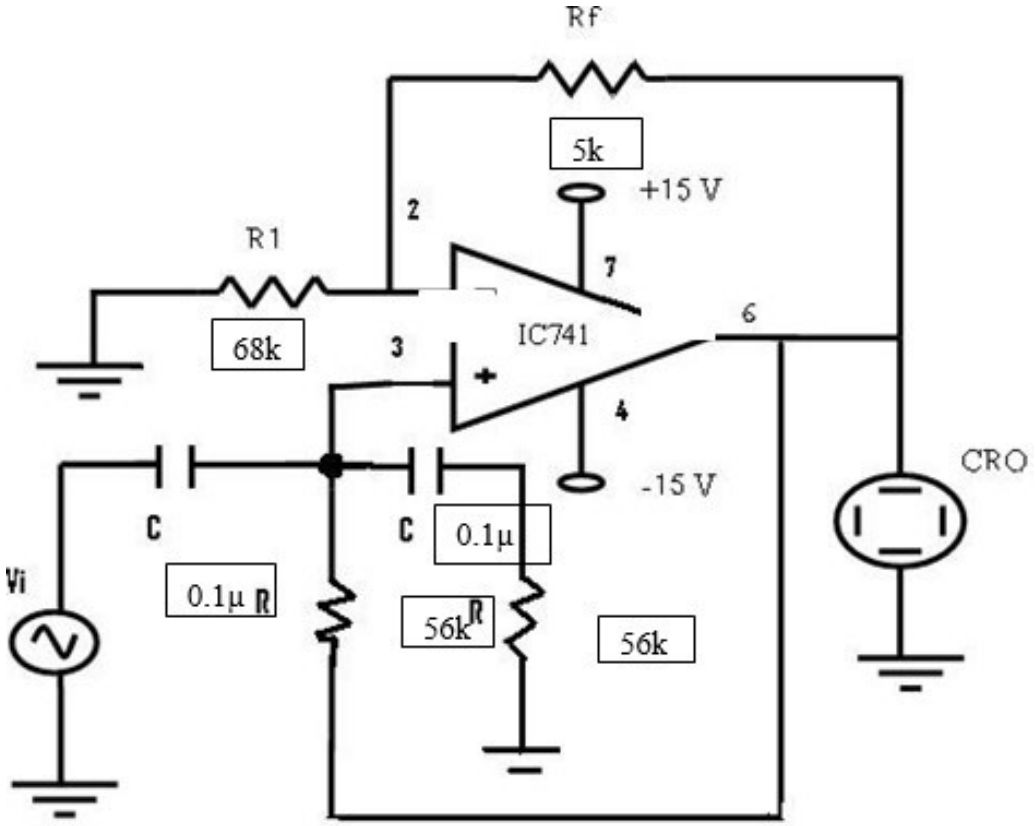
Theory:

The first order low pass and high pass filter is realized RC circuit used along with an op-amp in non-inverting configuration. A low pass and high pass filter has constant gain. Bandwidth of electric filters are used in circuits which require the separation of signals according to their frequencies. a first order low pass filter consists of a single RC network connected to the positive input terminal of non-inverting op-amp amplifier. Resistors R_i and R_f determine the gain of the filter in the pass band.

Circuit Diagram: Low Pass filter



Circuit Diagram: High Pass filter

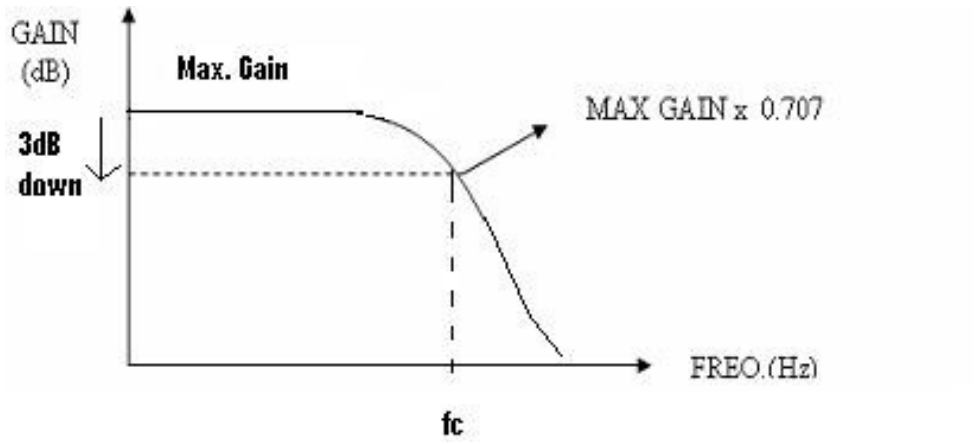


TABULATION-(ACTIVE LOW PASS FILTER) :

V_{in} =

S.NO	INPUT FREQUENCY (F_i) *Hz*	OUTPUT VOLTAGE (V_o) *mV*	GAIN = 20LOG(V_o/V_{in})

MODEL GRAPH:

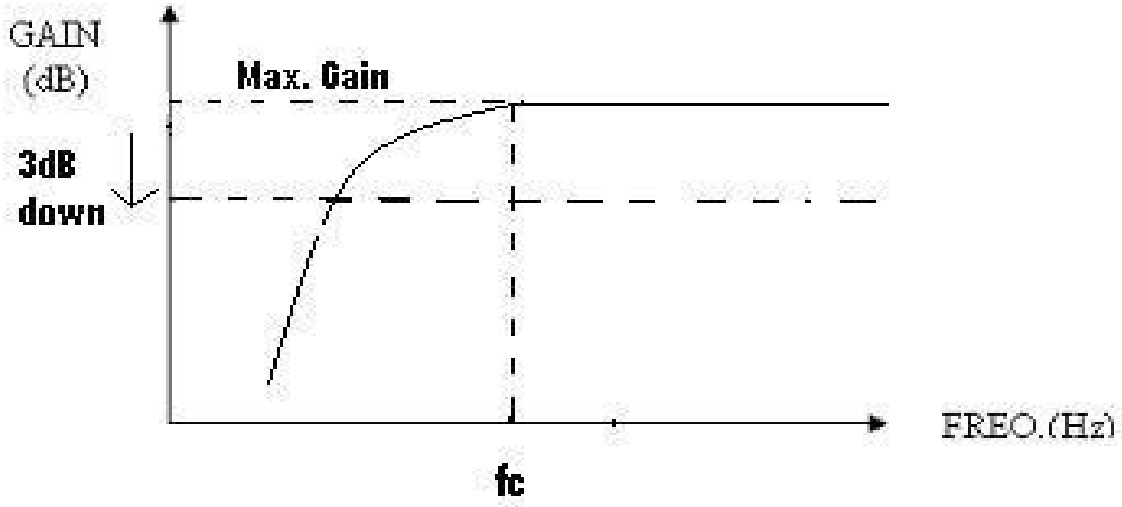


TABULATION –(ACTIVE HIGH PASS FILTER):

V_{in} =

S.NO.	INPUT FREQUENCY (F_i) *Hz*	OUTPUT VOLTAGE (Vo) *mV*	GAIN = 20LOG(V_o/V_{in})

MODEL GRAPH:



EXPERIMENTAL PROCEDURE:

1 connections are given as per the EXPERIMENTAL SETUP

2 Supply is switched ON after checking the connections.

3 Input voltage is set to 1V and by changing the input frequency, output voltage is measured.

4 The procedure is applied to active low pass, high pass and band pass filters.

RESULT:

Thus the low pass and high pass filters are designed and tested using IC741.

Ex. No : 5(a)	ACTIVE BAND PASS FILTER
DATE :	

AIM:

To design and test band pass filter using IC 741.

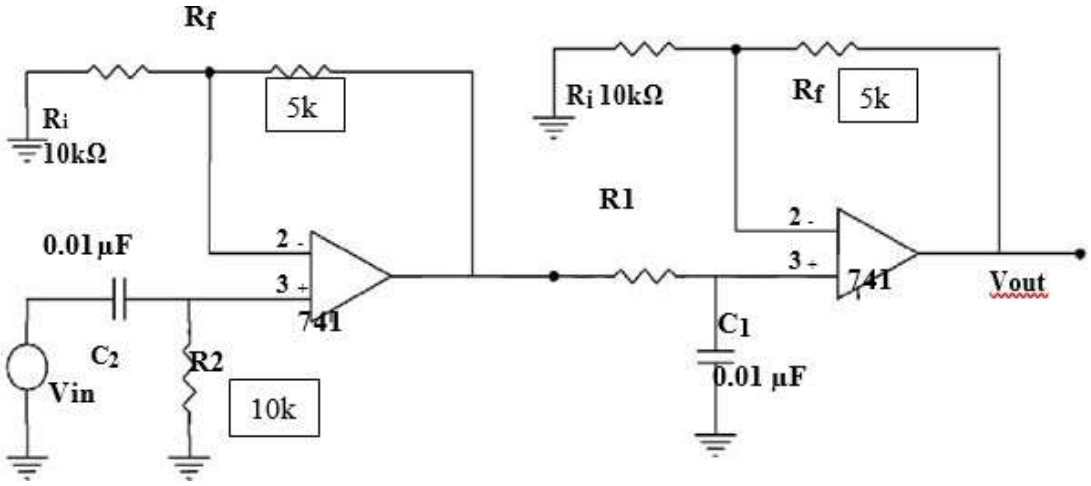
APPARATUS REQUIRED:

S.NO.	APPARATUS	RANGE	QUANTITY
1	Dual power supply	(0 - +15)V	1
2	CRO	(0-30)MHz	1
3	IC	µA 741	1
4	Resistor	10kΩ,5kΩ,	4,2
6	Capacitor	0.1µf,10µf	2,1

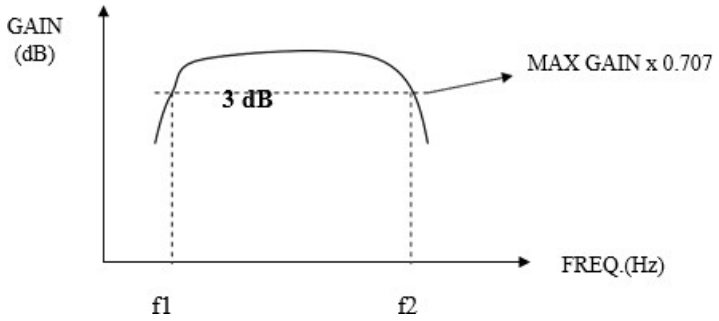
Theory:

The first order bandpass pass filter is realized RC circuit used along with an op-amp in non-inverting configuration. A low pass and high pass filter cascaded to realize the band pass filter. Bandwidth of electric filters are used in circuits which require the separation of signals according to their frequencies. a first order low pass filter consists of a single RC network connected to the positive input terminal of non-inverting op-amp amplifier. Resistors R_i and R_f determine the gain of the filter in the pass band.

Circuit Diagram:



MODEL GRAPH:



TABULATION:

Vin =

S.NO.	INPUT FREQUENCY (F_i) *Hz*	OUTPUT VOLTAGE (Vo) *mV*	GAIN = 20LOG(Vo/Vin)

EXPERIMENTAL PROCEDURE:

1 Connections are given as per the EXPERIMENTAL SETUP

2 Supply is switched ON after checking the connections.

3 Input voltage=1V and by changing the input frequency, output voltage is measured.

4 The procedure is applied to active low pass, high pass and band pass filters.

RESULT:

Thus the band pass filters is designed and tested using IC741.

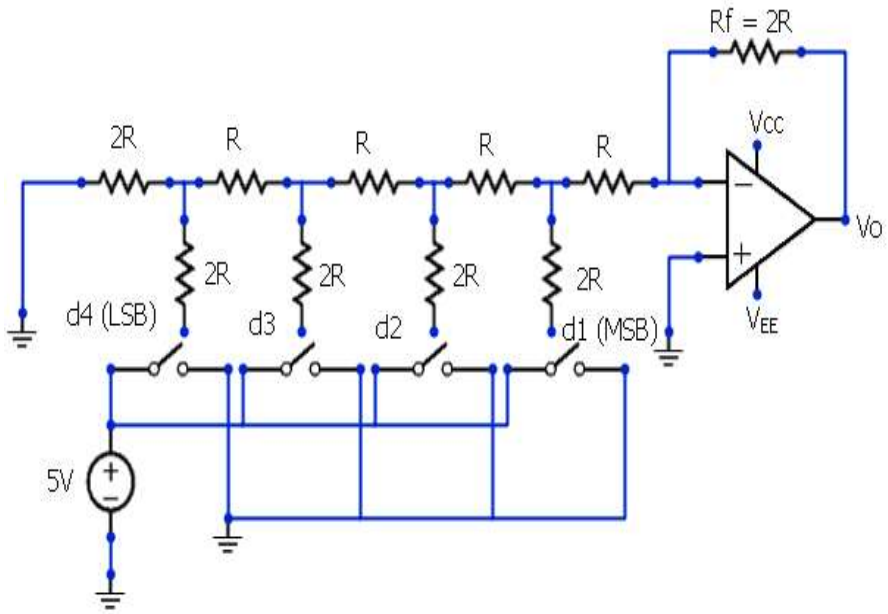
Ex. No : 6	DAC- R- 2R LADDER TYPE
DATE :	

Aim: Design of R/2R ladder 4-bit Digital to Analog Converter using IC 741

Apparatus: Digital Trainer kit, Op-amp IC 741, Breadboard, Dual power supply (0 – 30 V), Connecting wires, etc.

Circuit Diagram:

R-2R ladder DAC using Op amp IC 741



Theory:

Real world signals are analogue. Digital systems that interface with the real world do so using analogue-to-digital converters (ADC). Conversion back to analogue is accomplished using digital-to- analogue converters (DAC). The R-2R ladder network is commonly used for Digital to Analogue conversions.

In basic N bit R-2R resistor ladder network the digital inputs or bits range from the most significant bit (MSB) to the least significant bit (LSB). The bits are switched between either 0V or VR and depending on the state and location of the bits Vo will vary between 0V and VR . The MSB causes the greatest change in output voltage and the LSB causes the smallest.

The R-2R ladder is inexpensive and relatively easy to manufacture since only two resistor values are required. It is fast and has fixed output impedance R.

In R-2R ladder type D to A converter, only two values of resistor is used (i.e. R and 2R). Hence it is suitable for integrated circuit fabrication. The typical values of R are from 2.5K∧ to 10K∧ . In this output voltage is a weighted sum of digital inputs. Since the resistive ladder is a linear network, the principle of super position can be used to find the total analog output voltage for a particular digital input by adding the output voltages caused by the individual digital inputs. The output voltage is linearly proportional to the digital input and the range can be adjusted by changing the reference voltage V_R .

Calculations: Output Voltage is given by

$$\mathbf{Vo = - V_R * (Rf / 2R) * (d1/2 + d2/4 + d3/8 + d4/16)}$$

Where , V_R = 5V , Rf = 2R , d1 (MSB bit) and d4 (LSB bit)
Let R = 12 KΩ , then

Resolution = V_{FS} / (2^n- 1) , where n= no of digital inputs
V_{FS} = Value of analog output when digital input is 1111.
Resolution = 0.3125 = Value of LSB bit.

Procedure: 1. Wire the R/2R ladder 4 bit DAC circuit on the bread board.

2. Select the approximate value of R and 2R.

3. Reference voltage V_R is set as 5 V.

4. Find the output voltage V o for different combinations of digital binary inputs from 0000 to 1111.

5. Compare the calculated values with observed values and plot DAC characteristics.

OBSERVATION TABLE :

d1	d2	d3	d4	Vo (observed)	Vo (Calculated)
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
1	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

RESULT :

Ex. No : 7	VOLTAGE REGULATOR USING LM 317
DATE :	

AIM:

To conduct an experiment in order to get regulated output using LM 317.

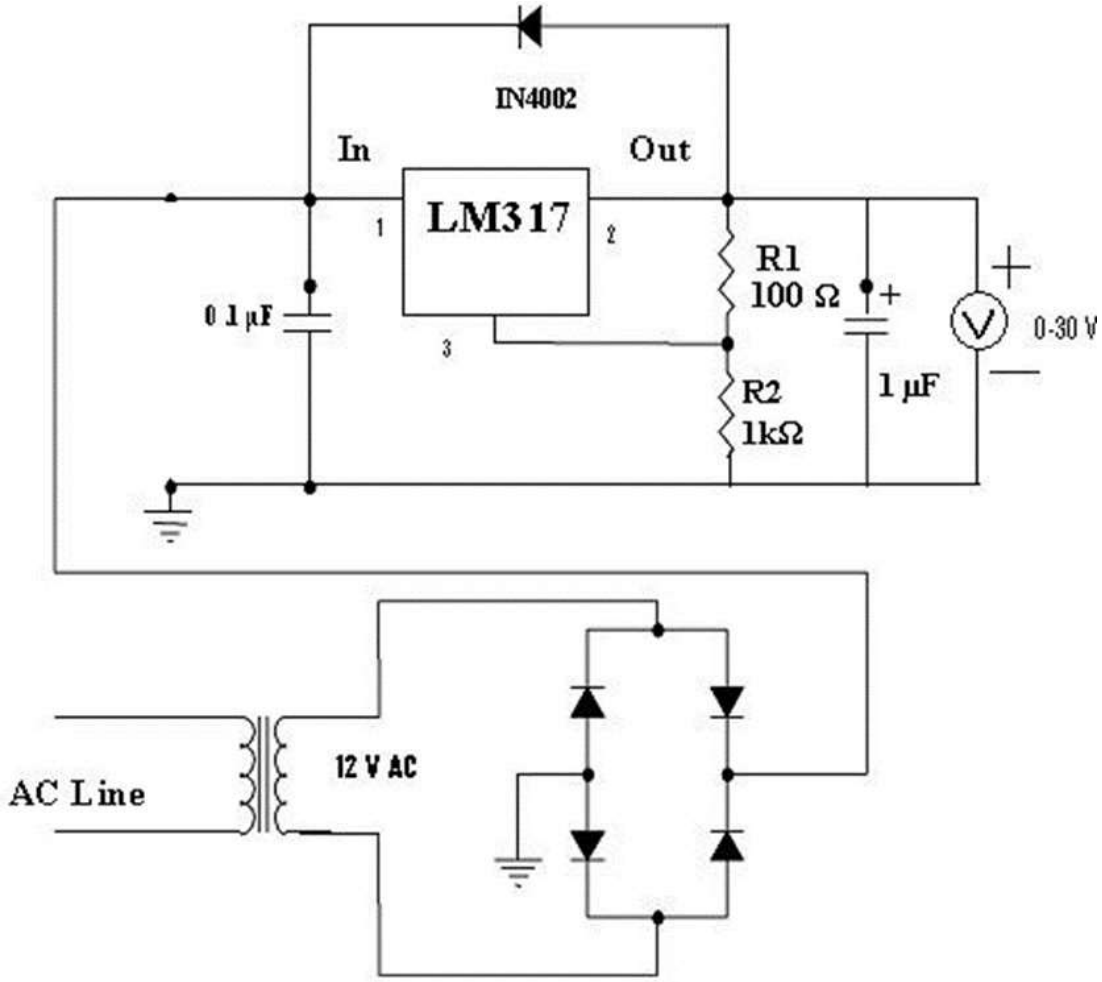
APPARATUS REQUIRED:

S.NO.	APPARATUS	RANGE	QUANTITY
1	Dual power supply	(0 - +15)V	1
2	Resistor	240Ω , 1.4KΩ	Each 1
3	Capacitor	1μF	1
4	Bread Board	-	1

THEORY:

The basic voltage regulator in its simplest form consists of a) voltage reference Vr b) error amplifier c) feedback network d) active series or shunt control unit. the voltage reference generates a voltage level which is applied to the comparator circuit, which is generally error amplifier. The second input to the error amplifier obtained through feedback network. Generally using the potential divider, the feedback signal is derived by sampling the output voltage. The error amplifier converts the difference between the output sample and the reference voltage into an error signal. This error signal in turn controls the active element of the regulator circuit, in order to compensate the changes in the output voltage. Such an active element is generally a transistor.

Circuit Diagram:



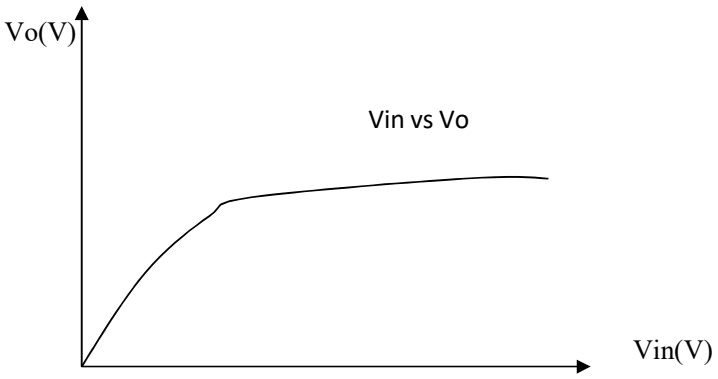
DESIGN PROCEDURE:

Besides fixed voltage regulator, Ic voltage regulators are available which allow the adjustment of the output voltage. The output voltage can be adjusted from 1.2V to as high as 5.7V with the help of such regulators. in such regulator IC's common terminal plays the role of control input and hence called as adjustment terminal. The LM 317 series is the most commonly used three terminal adjustable regulators. These devices are available in a variety of packages which can be easily mounted and handled. The power rating of such regulators is 1.5Am.the maximum input voltage of LM 317 is 40V.

TABULATION-(DC POWER SUPPLY):

S.NO.	Vin *volts*	Vo *volts*

MODEL GRAPH:



EXPERIMENTAL PROCEDURE:

1 Connections are given as per the experimental setup.

2 The input voltage is given to the circuit and output voltage varies from zero.

3 Then the output voltage attains the designed value and then it is irrespective of input voltage (the output becomes constant.

RESULT :

Thus the experiment is conducted using LM 317 and the regulated output is obtained using the op-amp circuit.

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