SRM Institute of Science and Technology Tiruchirappalli
Faculty of Engineering and Technology
Dept. of Electronics and Communication Engineering

21ECC303T
VLSI Design and Technology

Unit II – MOS Transistor

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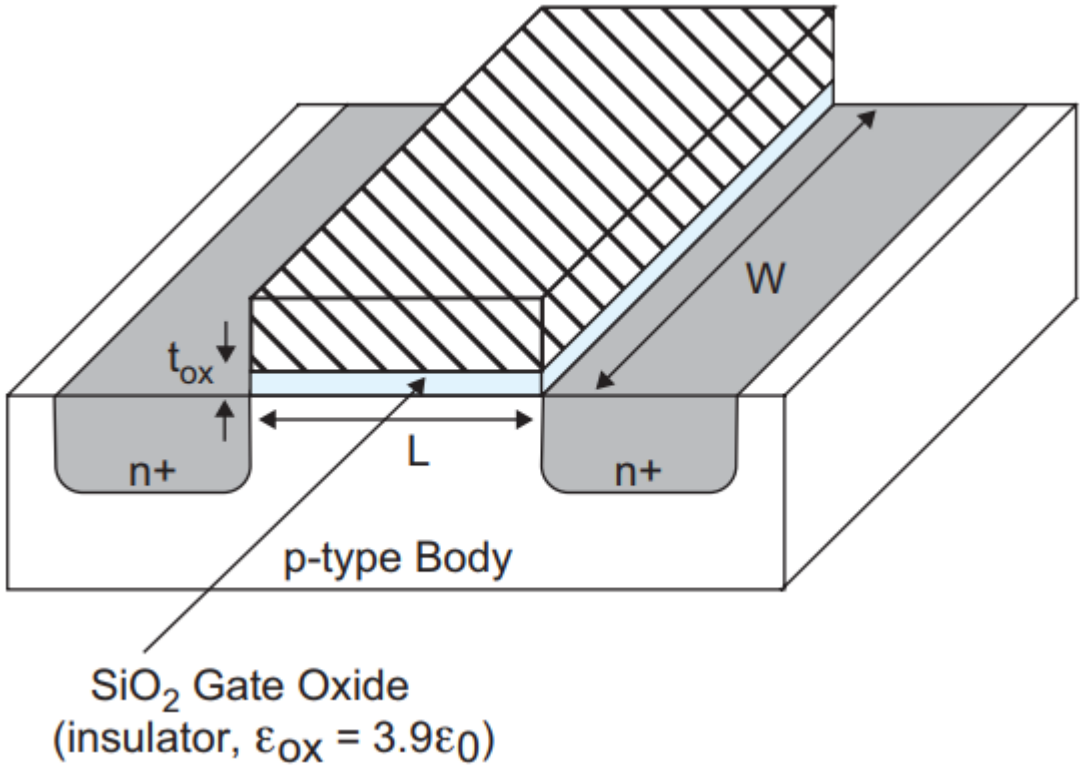
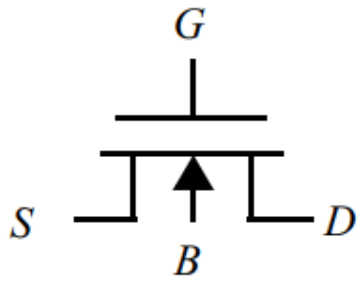
MOS Transistor Overview

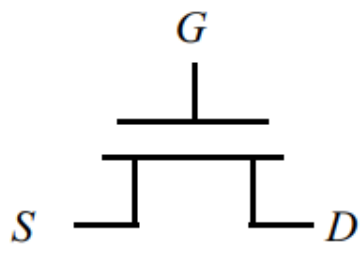
- The MOSFET is a four terminal device.
- The voltage applied to the *gate* terminal determines if and how much current flows between the *source* and the *drain* ports.
- The *body* represents the fourth terminal of the transistor.
- Its function is secondary as it only serves to modulate the device characteristics and parameters
- The MOS transistor is a *majority-carrier* device in which the current in a conducting channel between the source and drain is controlled by a voltage applied to the gate.
- In an nMOS transistor, the majority carriers are electrons; in a pMOS transistor, the majority carriers are holes.



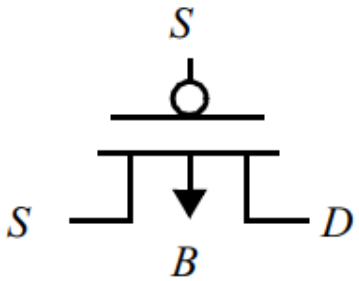
MOS Transistor Circuit Symbols



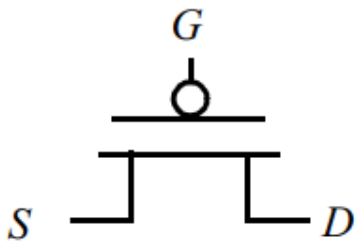
(a) NMOS transistor as 4-terminal device



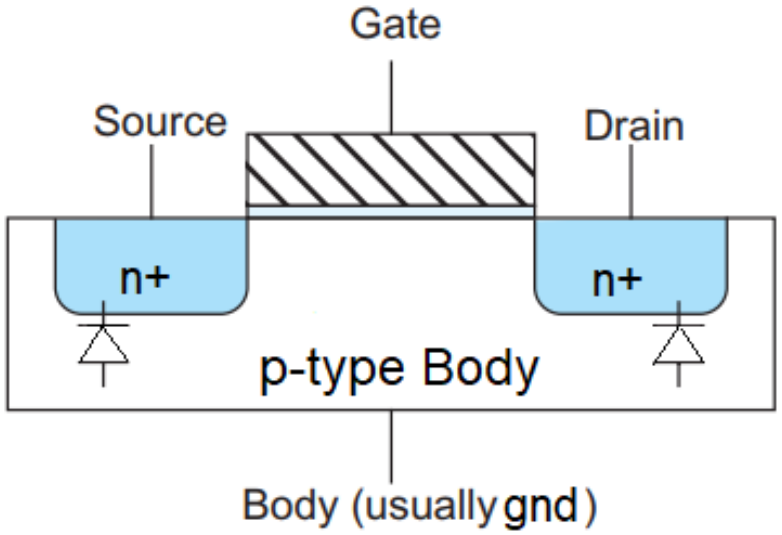
(b) NMOS transistor as 3-terminal device



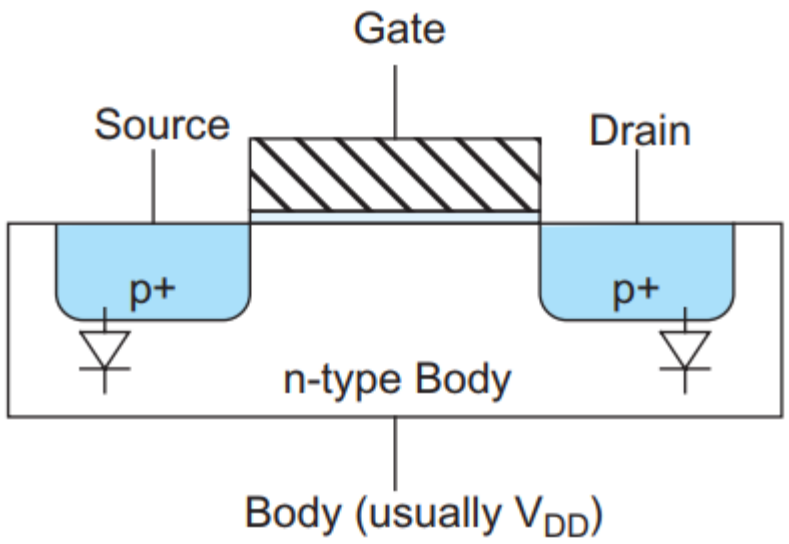
(a) PMOS transistor as 4-terminal device



(d) PMOS transistor as 3-terminal device

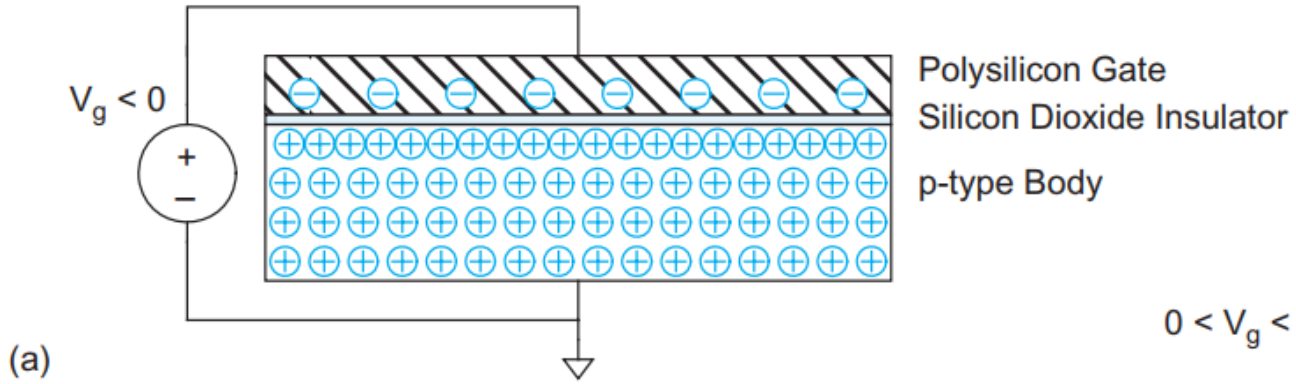


nMOS

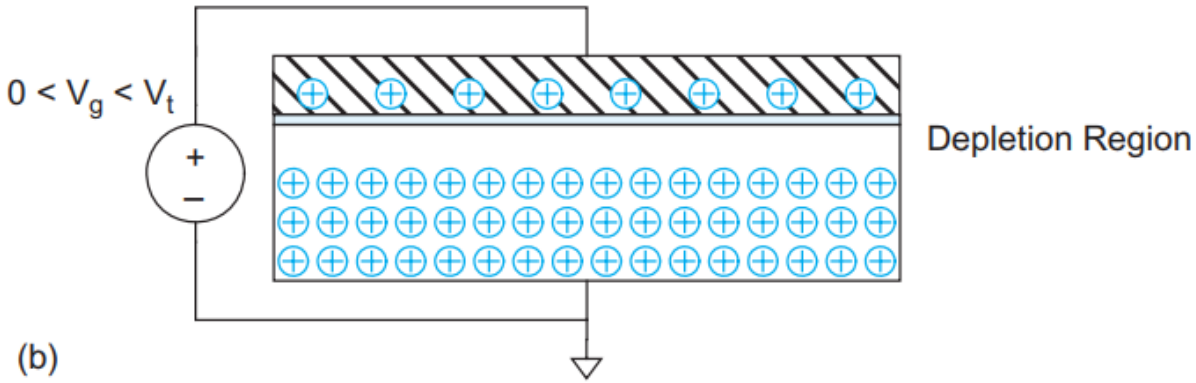


pMOS

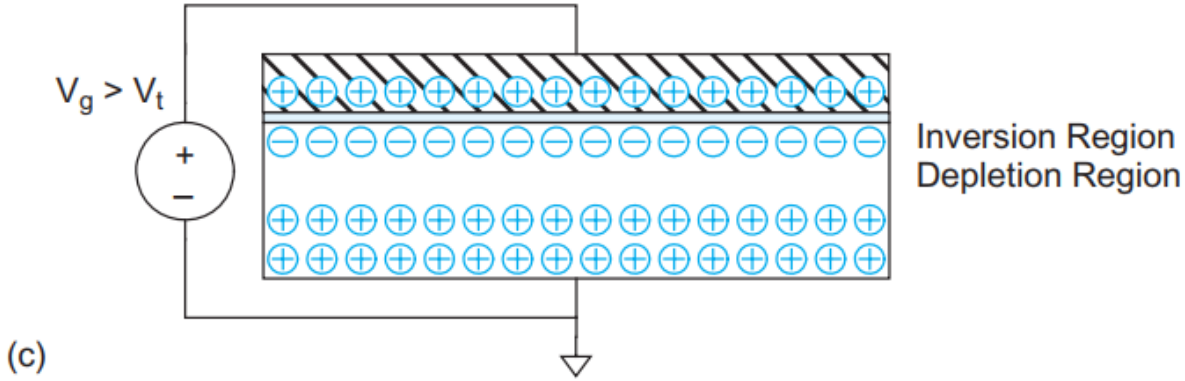
nMOS Transistor Modes of operation



Accumulation mode



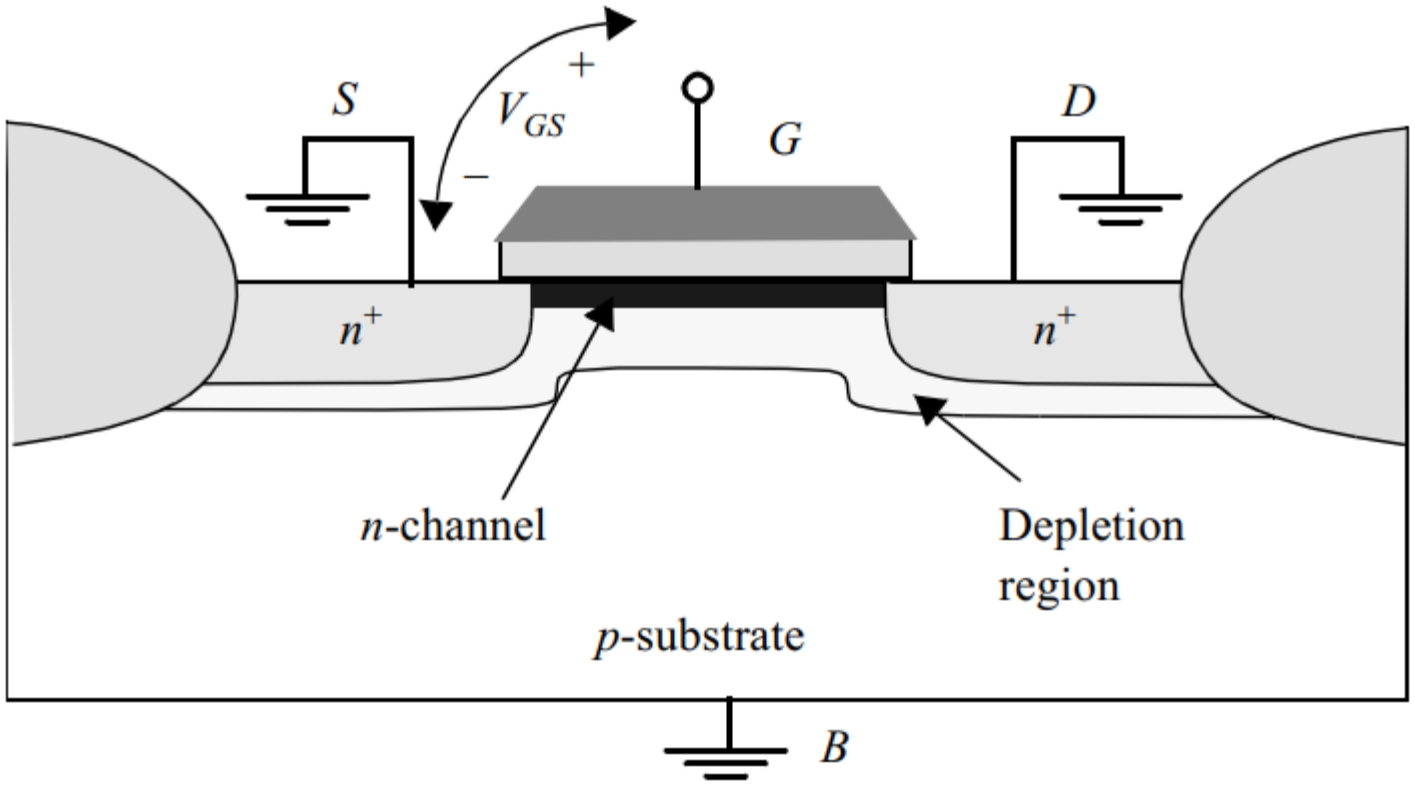
Depletion mode



Inversion mode

nMOS Cutoff region

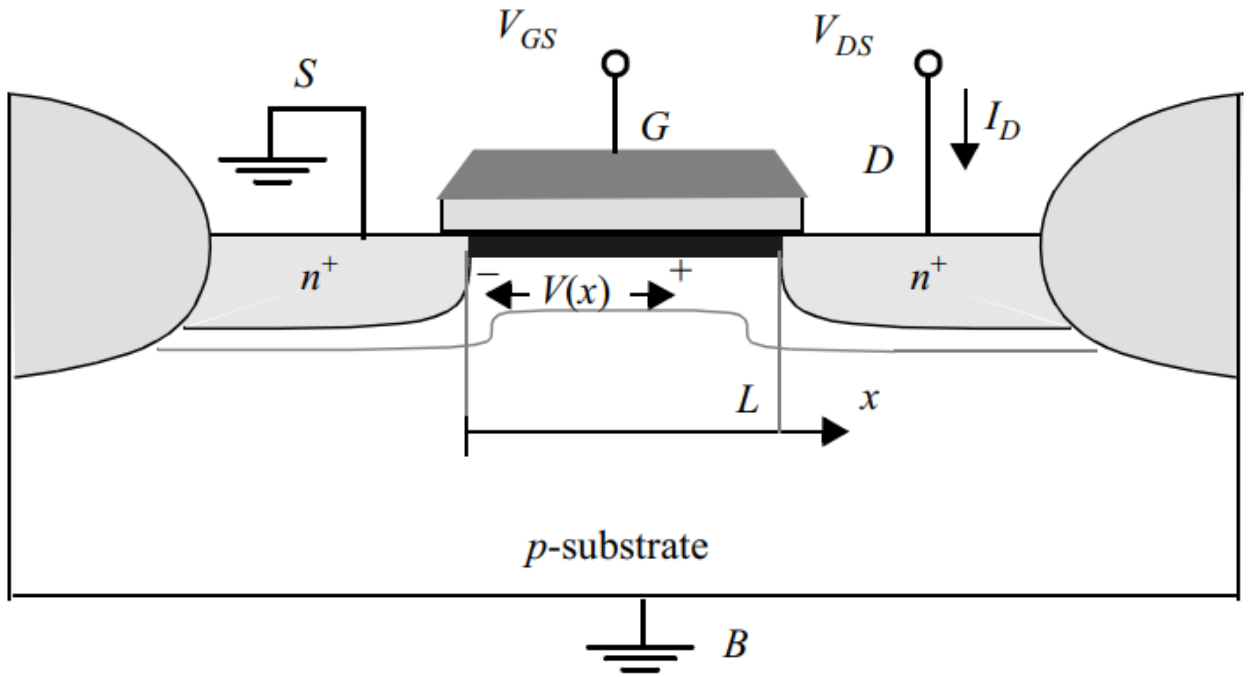
$V_{GS}<V_T$ or $V_{GS}>V_T$, $V_{DS}=0$



$$I_D = 0$$

nMOS Linear region

$V_{GS} > V_T$ and $0 < V_{DS} < V_{DS,sat}$; $V_{DS,sat} = V_{GS} - V_T$



$$I_{ds} = \beta \left(V_{gs} - V_t - \frac{1}{2} V_{ds} \right) V_{ds} \quad ---(8) \; ; V_{GS} \geq V_{th} \text{ and } V_{DS} < Vsat = V_{GS} - V_{th}$$

nMOS Saturation region

$V_{GS} > V_T$ and $0 < V_{DS} >= V_{DS,sat}$; $V_{DS,sat} = V_{GS} - V_T$

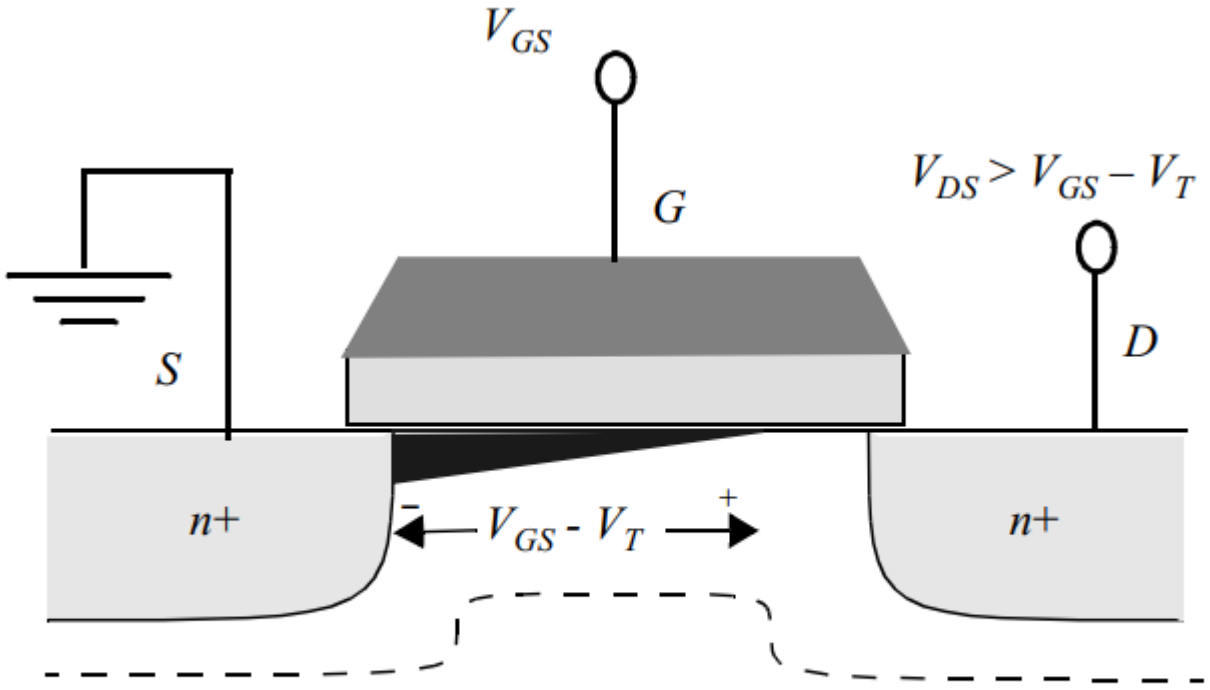


Figure 3.16 NMOS transistor under pinch-off conditions.

$$I_{ds} = \beta \left[\frac{V_{ds}^2}{2}\right] \text{--- (9)}$$

Drain current in three regions

$$\beta = \mu C_{ox} \frac{W}{L};\ V_{GT} = V_{gs} - V_t$$

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{Cutoff} \\ \beta\left(V_{GT} - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{Linear} \\ \frac{\beta}{2}V_{GT}^2 & V_{ds} > V_{dsat} \quad \text{Saturation} \end{cases}$$

MOS Transistors - Problem

Consider an nMOS transistor in a 65 nm process with a minimum drawn channel length of 50 nm ($\lambda = 25$ nm). Let $W/L = 4/2\ \lambda$ (i.e., 0.1/0.05 μm). In this process, the gate oxide thickness is 10.5 Å. Estimate the high-field mobility of electrons to be 80 $cm^2/V \cdot s$ at 70 °C. The threshold voltage is 0.3 V. Plot I_{ds} vs. V_{ds} for $V_{gs} = 0$, 0.2, 0.4, 0.6, 0.8, and 1.0 V using the long-channel model.

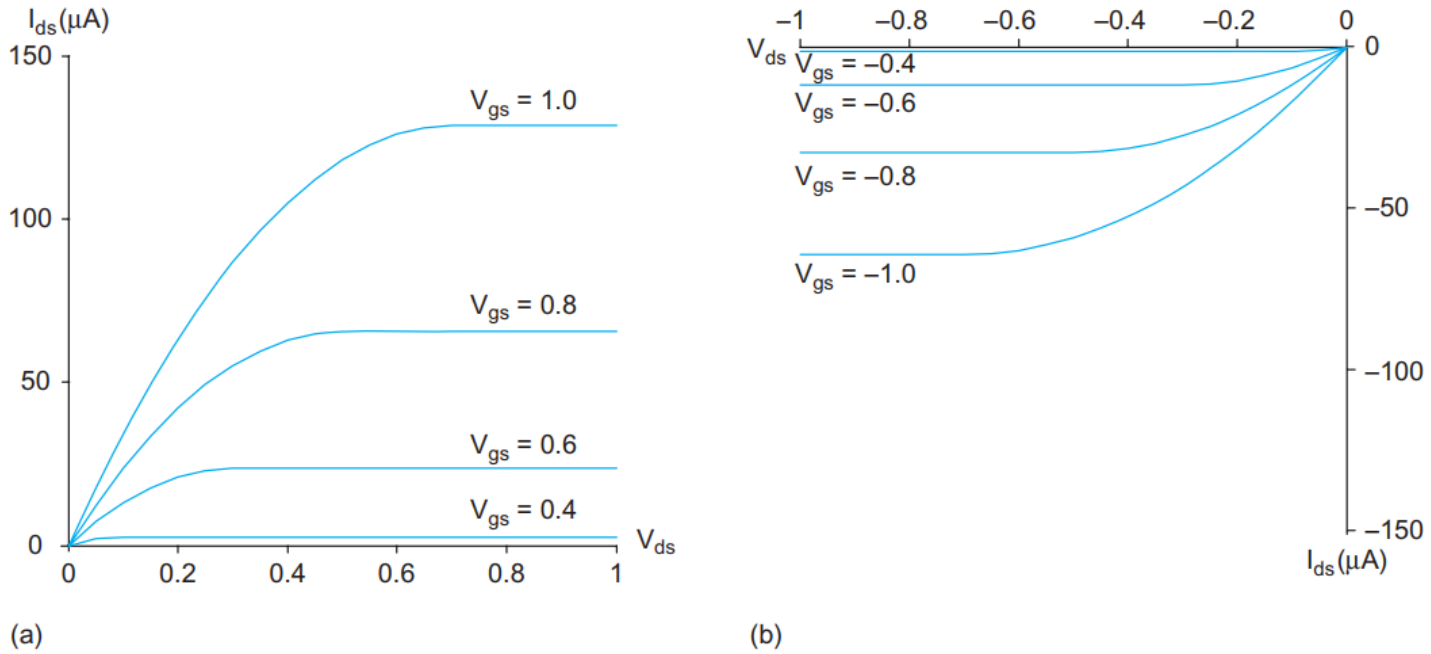
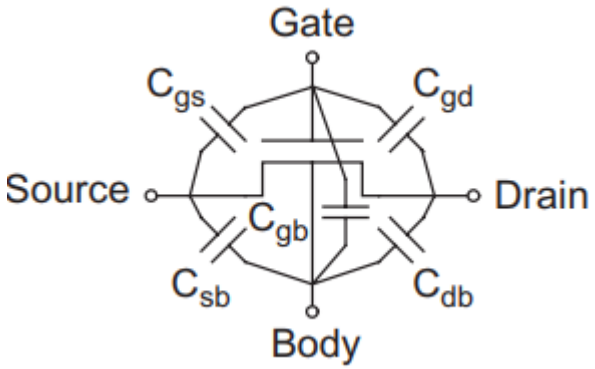


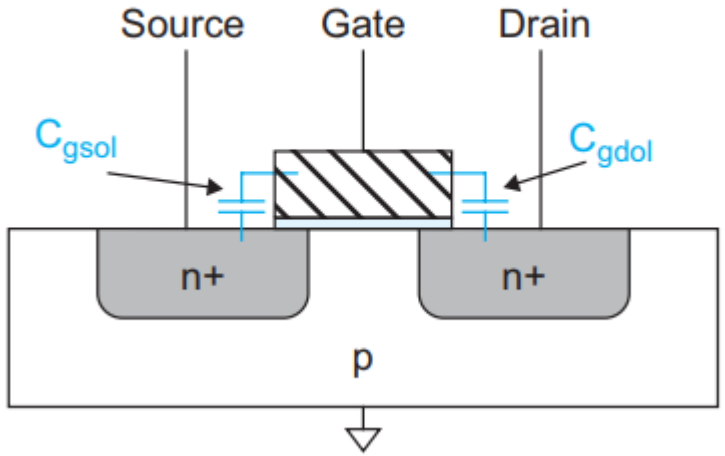
FIGURE 2.7 I-V characteristics of ideal 4/2 λ (a) nMOS and (b) pMOS transistors

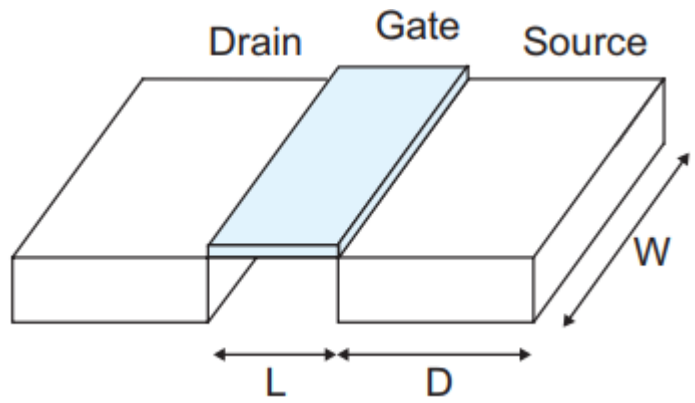
MOS Transistors - Capacitances



Parameter	Cutoff	Linear	Saturation
C_{gb}	$\leq C_0$	0	0
C_{gs}	0	$C_0/2$	$2/3\ C_0$
C_{gd}	0	$C_0/2$	0
$C_g = C_{gs} + C_{gd} + C_{gb}$	C_0	C_0	$2/3\ C_0$

MOS Transistors - Overlap and Diffusion Capacitances





$$C_{gsol(\text{overlap})} = C_{gsol} W$$
$$C_{gdol(\text{overlap})} = C_{gdol} W$$

$$C_{sb} = AS \times C_{jbs} + PS \times C_{jbssw}$$

$$C_{jbs} = C_J \left(1 + \frac{V_{sb}}{\psi_0}\right)^{-M_J} \qquad C_{jbssw} = C_{JSW} \left(1 + \frac{V_{sb}}{\psi_{SW}}\right)^{-M_{JSW}}$$

$$\psi_0 = v_T \ln \frac{N_A N_D}{n_i^2}$$