

Unit-3: Sequential Circuits	
Flip-flop and Latch: SR latches- JK flip-flop, T flip-flop, D flip-flop-Master-slave JK flip-flop- Register Counters- Ring counter, Johnson counter-Shift registers (SISO, SIPO, PISO, PIPO)--Universal shift register-Counters:-Asynchronous/Ripple counters--Synchronous counters-Modulus-n Counter -Up-Down counter- -State reduction-State assignment	9 Hours
Unit-4 : Advanced Combinational, Sequential logic	
Advance sequential logic:-- Mealy and Moore model- Analyze and design synchronous sequential circuits - FSM - Sequence detector - Vending Machine - Advanced digital circuits:- Hamming code – Delay in a ripple carry adder - Carry Look Ahead adder -2 Bit Multiplier	9 Hours
Unit-5: PLD's and Memory	
RAM Memory decoding-ROM--Basic concepts:-Programmable Logic Devices (PLDs):-Basic concepts-PROM as PLD-Programmable Array Logic (PAL)--Programmable Logic Array (PLA)-FPGA	9 Hours
Learning Resources	1. Morris Mano M, Michael D. Ciletti, Digital Design with an Introduction to the Verilog HDL, 5th ed., Pearson Education, 2014 2. Charles H Roth (Jr), Larry L. Kinney, Fundamentals of Logic Design, 5th ed., Cengage Learning India Edition, 2010 3. Thomas L. Floyd, Digital Fundamentals, 10th ed., Pearson Education, 2013 4. Ronald J. Tocci, Digital System Principles and Applications, 10th ed., Pearson Education, 2009 5. Donald P Leach, Albert Paul Malvino, Goutam Saha, Digital Principles and Applications, 6th ed., TataMcgraw Hill, 2008

Learning Assessment							
	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)					
		Formative CLA-1 Average of unit test (50%)		Life Long Learning CLA-2 – (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	15%	-	15%	-	15%	-
Level 2	Understand	25%	-	20%	-	25%	-
Level 3	Apply	30%	-	25%	-	30%	-
Level 4	Analyze	30%	-	25%	-	30%	-
Level 5	Evaluate	-	-	10%	-	-	-
Level 6	Create	-	-	5%	-	-	-
	Total	100 %		100 %		100 %	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
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	2.	2.