Down Scaling of CMOSc

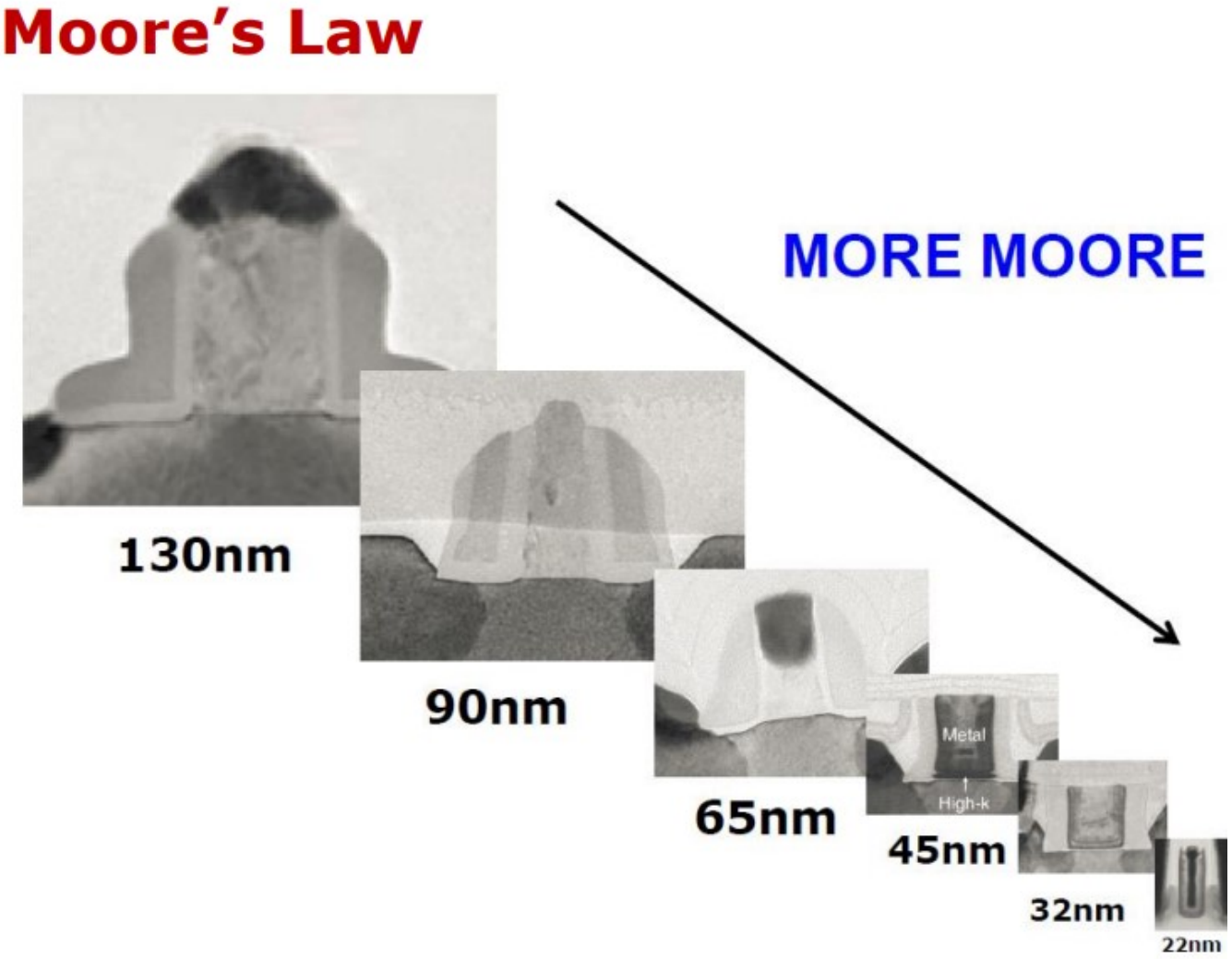
- MOS devices have been scaled to achieve
  - Higher density
  - Higher performance
  - Low power consumption

Disadvantages:

- Electric field within gate oxide grows larger
- Short channel effects

Moore's Law

- Moore's Law-In 1965, Gordon Moore postulated that the number of
  - transistors per unit area on integrated circuits will double every 18 months.
  - Clock frequency gets doubled every 34 to 36 months



Transistor size becoming smaller

Moore's Law

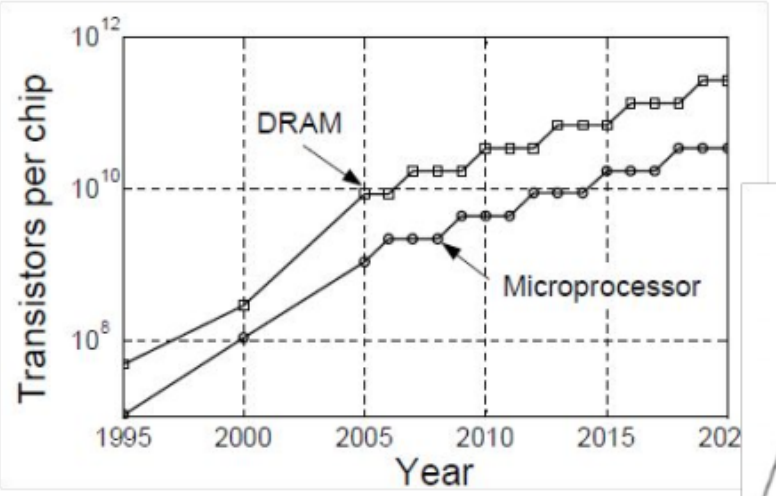


Figure 1 Evolution of the number of transistors per chip (Moore's law) predicted by the ITRS for DRAMs and high-performance microprocessors

Dennard's Scaling Rule

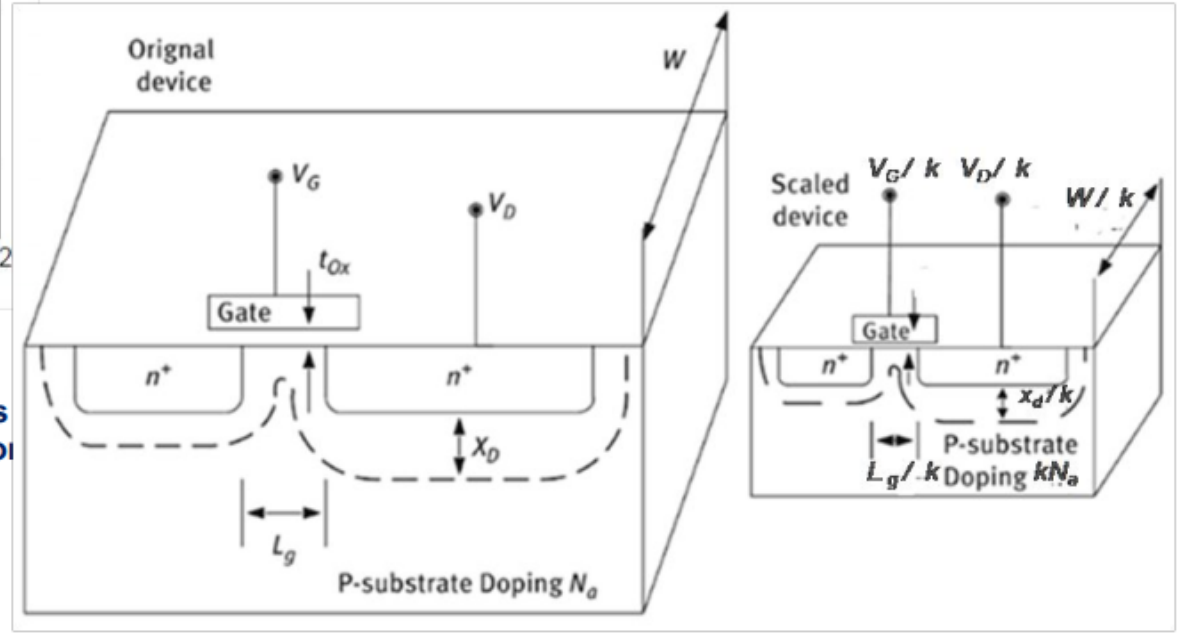


Figure 2 MOSFET scaling rule [2]

Reducing the critical dimensions while keeping the electrical field constant yields

- **higher speed**
- **reduced power** consumption of a digital MOS circuit

Scaling Rules

- Constant Field scaling
- Constant Voltage scalcing

Scaling of the device does not only mean the reduction of the Channel Length. It includes the proper scaling of all other device dimensions.

Constant Field Scaling-It yields the reduction in the power-delay product of the transistor. Hence, it requires the reduction in power supply for reduced feature size.

Constant Voltage Scaling-This is a preferred scaling technique as it provides voltage compatibility with other technologies. Due to this electric field gets higher in smaller devices which causes mobility degradation, velocity saturation etc.

Constant Field scaling

- Maintain constant electric field even though we scale down so that the pressure is constant, electric field is maintained within saturation

Parameter	Scaled parameter
Channel length (L)	$1/\alpha$
Width (W)	$1/\alpha$
Substrate doping (N_A)	α
Depletion layer thickness (d)	$1/\alpha$
Gate delay (τ_p)	$1/\alpha$
Load capacitance (C_L)	$1/\alpha$
Supply voltage (V)	$1/\alpha$
Gate oxide thickness (t_{ox})	$1/\alpha$
Current (I)	$1/\alpha$
Current density (J)	α
Transconductance (g_m)	1
Junction depth (x_j)	$1/\alpha$
Static power dissipation (P_{stat})	$1/\alpha^2$
Dynamic power dissipation (P_{dyn})	$1/\alpha^2$

Constant Voltage scaling

- The supply voltage (V_{DD}) is maintained constant but other parameter is varied to have E within saturation

Parameter	Scaled parameter
Channel length (L)	$1/\alpha$
Junction depth (x_j)	$1/\alpha$
Substrate doping (N_A)	α
Depletion layer thickness (d)	$1/\alpha$
Transconductance (g_m)	α
Static power dissipation (P_{stat})	α
Dynamic power dissipation (P_{dyn})	α
Current (I)	α
Gate delay (τ_p)	$1/\alpha^2$
Load capacitance (C_L)	$1/\alpha$
Channel width (W)	$1/\alpha$
Supply voltage (V)	1
Gate oxide thickness (t_{ox})	$1/\alpha$
Current density (J)	α^3

Components of Leakage Power due to scaling of MOSFET

$$P_{dynamic} = C_L . V_{DD}^2 . f \qquad P_{static} = I_{leak} . V_{DD}$$

- Supply voltage has been scaled down - to keep power consumption under control
- The threshold voltage scaling results in substantial increase of the leakage current

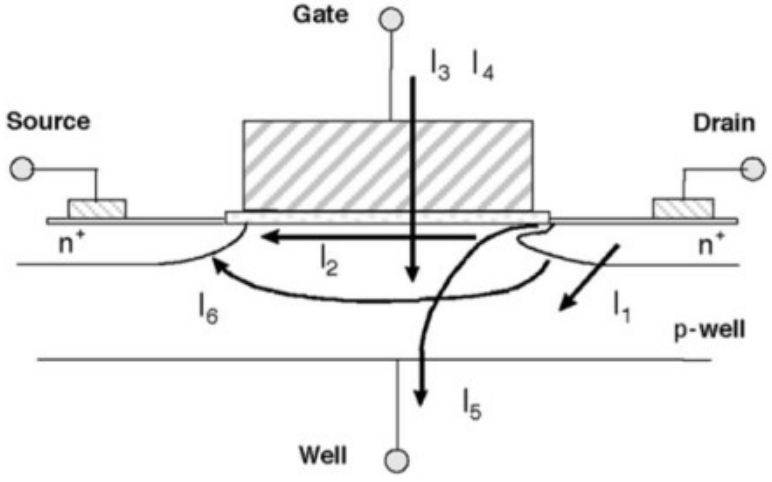


Figure b Components of leakage power due to short channel effects

- pn Junction Reverse-Bias Current (I_1)
- Subthreshold Leakage (I_2)
- Tunneling into and Through Gate Oxide(I_3)
- Injection of Hot Carriers from Substrate to Gate Oxide (I_4)
- Gate-Induced Drain Leakage (I_5)
- Punchthrough(I_6)

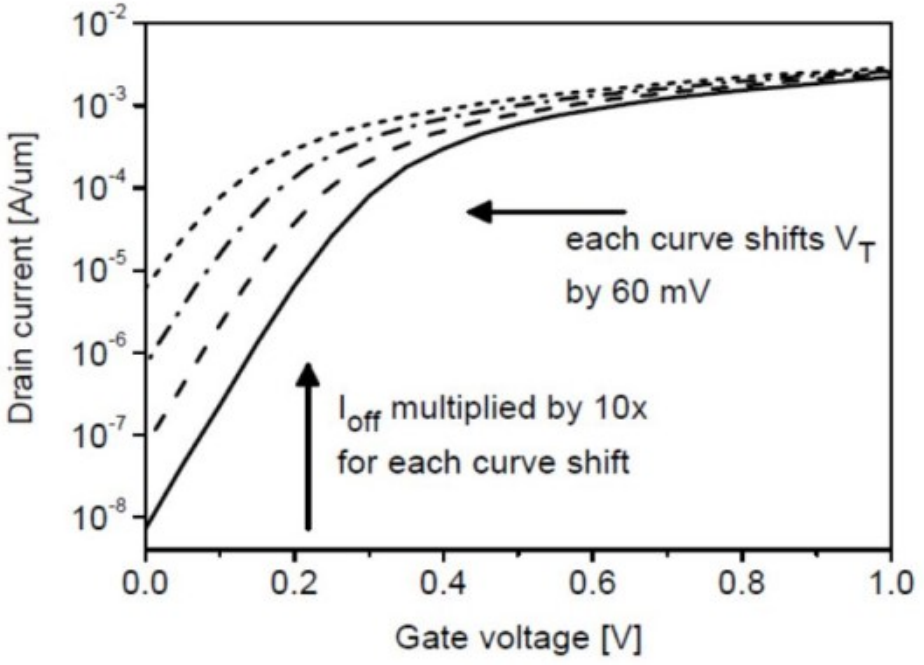


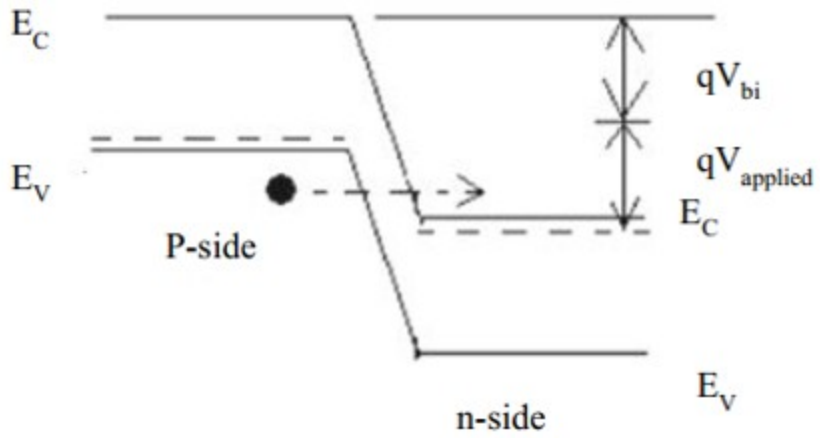
Figure c Exponential increase in the off-current of MOSFET due to the downscaling of threshold voltage reduction

Short Channel Effects

- Reverse biased diode leakage
- Gate oxide tunnelling
- Gate induced drain leakage (GIDL)
- Subthreshold leakage
- Drain-induced barrier lowering (DIBL)
- Negative bias temperature instability (NBTI)
- Hot carriers
- Lightly doped drain (LDD)

Reverse biased diode leakage

- The drain/source and substrate junctions in a MOS transistor are reverse biased during transistor operation. This results in reverse-biased leakage current in the device. This leakage current can be due to drift/diffusion of minority carriers in the reverse-biased region and electron-hole pair generation due to the avalanche effect. The pn junction reverse-biased leakage current depends on doping concentration and junction area.
- For heavily doped pn junction of drain/source and substrate regions, the band-to-band tunneling (BTBT) effect dominates the reverse bias leakage current. In band-to-band tunneling, electrons tunnel directly from the valence band of the p region to the conduction band of the n region. BTBT is visible for electric fields greater than 10^6 V/cm.



BTBT due to high electric field across reverse-biased junction

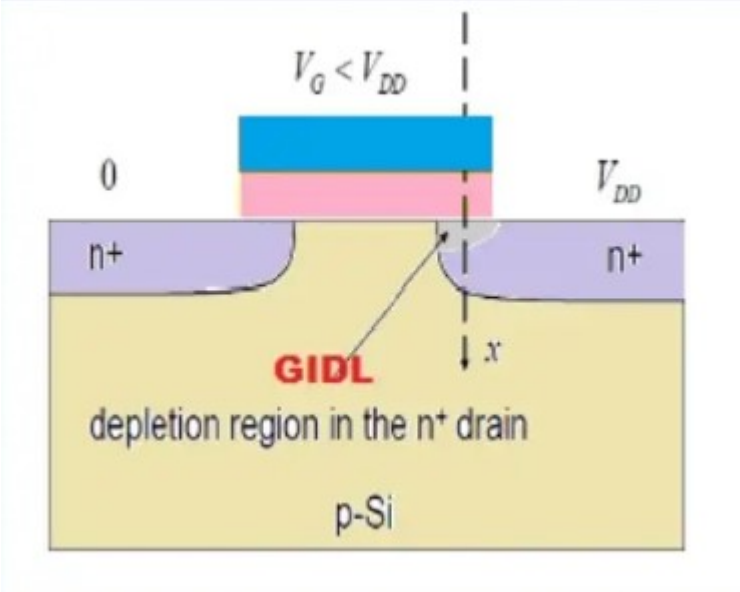
It occurs when the total voltage drop across the junction, applied reverse bias ($V_{applied}$) and the built-in potential (V_{bi}) is larger than the band-gap

Gate oxide tunneling

- With scaling of transistor to nanometer dimensions the thickness of the oxide layer is scaled down and it leads to increase in electric field across the oxide layer
- Resulting in a **leakage current from gate to substrate regio**n through the thin oxide layer due to the negative gate bias and also leakage current from substrate region to gate due to positive gate bias.

Gate Induced Drain Leakage

GIDL(Gate Induced Drain Leakage) occurs where the gate partially overlaps with the drain of the MOSFET and It is more pronounced when Vds levels are at High potential and Vgs is at low potential. Gate-induced drain leakage current is due to the band-to-band tunneling process in silicon in the gate-to-drain overlap region. This drain leakage current increases with increasing Vd and decreasing Vg.GIDL(Gate Induced Drain Leakage) is directly proportional to the gate-drain overlap area.



Subthreshold leakage

Subthreshold conduction in CMOS transistors is the leakage current that flows between the source and drain of a transistor when it is supposed to be in the 'off' state

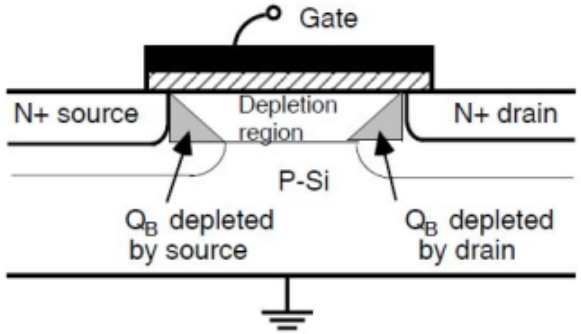
- The sub threshold current always flows from source to drain even if the gate to source voltage is lesser than the threshold voltage of the device.
- This happens due to the carrier diffusion between the source and drain regions of the CMOS transistor in weak inversion.
- When gate to source voltage is smaller than but very close to threshold voltage of the device then sub threshold current becomes significant.

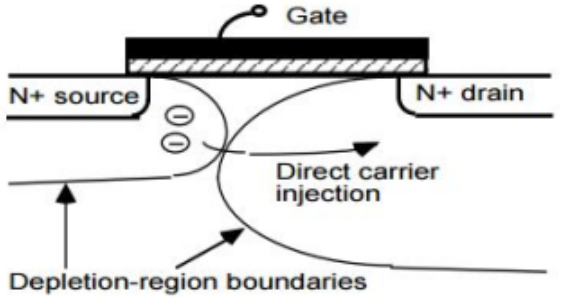
Drain-induced barrier lowering (DIBL)

One of the major challenges in transistor scaling are the ***"Short Channel Effects"*** with channel length (L_G) < 100nm.

DIBL occurs when **high drain voltage** is applied to short-channel devices, the depletion region of the drain interact with the source depletion region as the **source potential barrier height is lowered resulting in injection of the carrier into to the channel from the source** due to the reduced threshold voltage as it is not dependent of gate voltage.

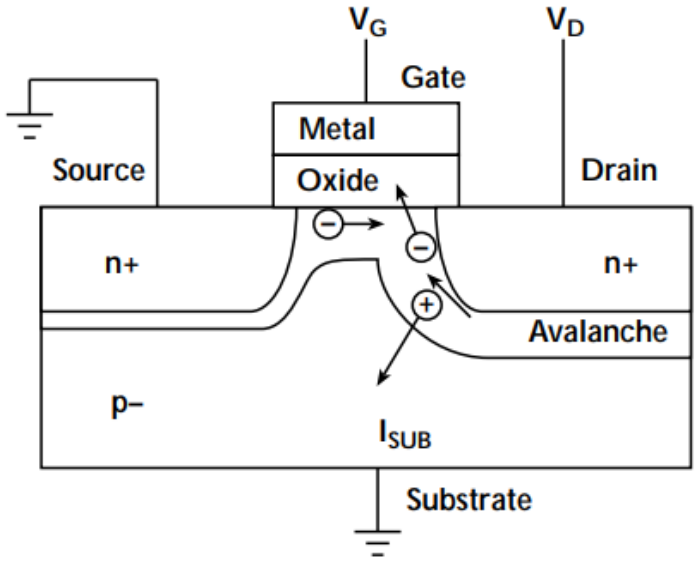
- **Punch Through** – For short Channel, the depletion region from the drain can reach the source side and reduces the barrier for electron injection
- **Drain Induced Barrier Lowering(DIBL)** - the barrier for electron injection from source to drain decreases. This is known as drain induced barrier lowering (DIBL)





Hot Carrier Effect

- With decreased MOSFET gate length, hot carrier induced degradation has become one of the most important reliability concerns.
- In the hot carrier effect, carriers are accelerated by the channel electric fields and become trapped in the oxide.
- These trapped charges cause time dependent shifts in measured device parameters, such as the
  - threshold voltage (V_{TH}),
  - transconductance (G_M),
  - linear ($I_{D,LIN}$)
  - saturation ($I_{D,SAT}$) drain current.



- In time, substantial device parameter degradation can occur, resulting in device failure.

Negative bias temperature Instability (NBTI)

- Negative Bias Temperature Instability (NBTI) is a key reliability issue in MOSFETs.
- It is of immediate concern in p-channel MOs devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism affects also n-MOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate too.
- NBTI manifests as an increase in the threshold voltage, a degradation of the mobility, drain current and trans-conductance.
- It is become a reliability issue in silicon integrated circuits, because gate electric field have increased as a result of scaling, increased chip operating temperature, surface p-channel MOSFETs have replaced buried channel devices, and nitrogen is routinely added to thermally grown SiO2.

Lightly doped drain (LDD)

- For deep submicron CMOS devices the internal lateral electric field is very high. Under this high electric field the hot carrier effects cause aging and avalanche breakdown which is not desirable for the operation of CMOS circuits.
- The hot carrier effects should be reduced, the best way to reduce is by reducing the lateral electric field in the channel at the drain side.
- The LDD structure is used to reduce the lateral electric field at the drain side by doping n- on either side and a spacer is doped around the gate