MOS Parasitic and contact resistance

Source-Drain Resistance

The performance of a CMOS circuit may further be affected by another set of parasitic elements, being the resistances in series with the drain and source regions, as shown in Figure 4a.

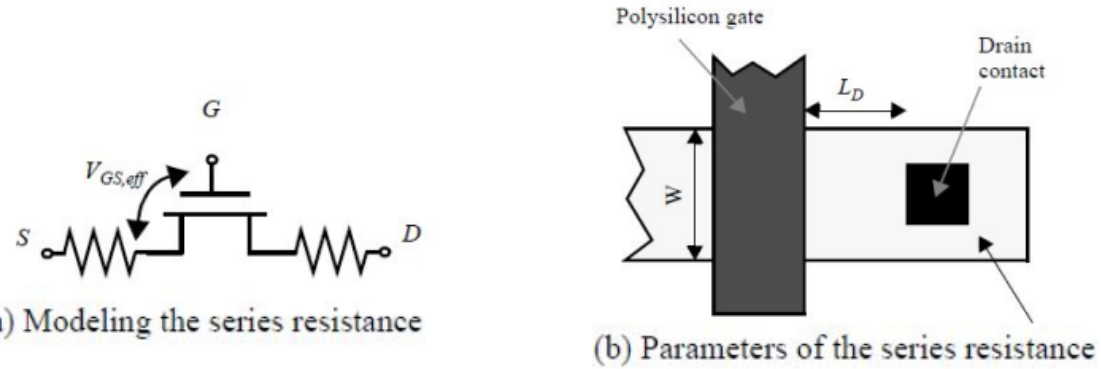
This effect become more pronounced when transistors are scaled down, as this leads to shallower junctions and smaller contact openings become smaller.

The resistance of the drain (source) region can be expressed as

$$R_{S,D} = \frac{L_{S,D}}{W} R_{\square} + R_C$$

with R_C the contact resistance, W the width of the transistor, and $L_{S,D}$ the length of the source or drain region (Figure 4b). $R_{\square}$ is the *sheet resistance* per square of the drain source diffusion, and ranges from 20 to 100 Ω/❑.

Observe that the resistance of a square of material is constant, independent of its size



(a) Modeling the series resistance

(b) Parameters of the series resistance

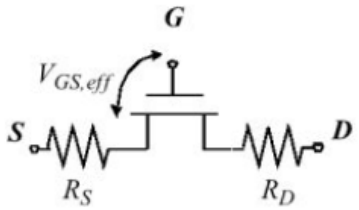
Figure 4 Series drain and source resistance.

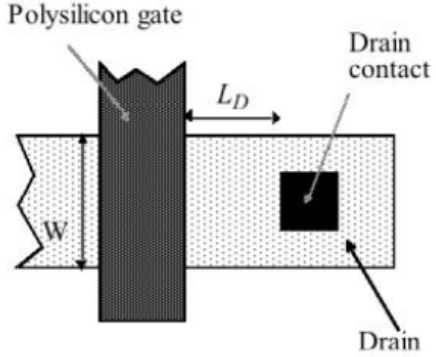
MOS Parasitic and contact resistance

Source-Drain Resistance

- The series resistance causes a deterioration in the device performance, as it reduces the drain current for a given control voltage.
- Keeping **its value as small as possible is thus an important design goal for both the device and the circuit engineer.**
- One option, popular in most contemporary processes, is to **cover the drain and source regions with a low-resistivity material such as titanium or tungsten. This process is called *silicidation*** and effectively reduces the sheet resistance to values in the range from 1 to 4 Ω/❑.

Parasitic Resistances





$R_S = (L_S/W)R_{\square} + R_C$

$R_D = (L_D/W)R_{\square} + R_C$

R_C: contact resistance

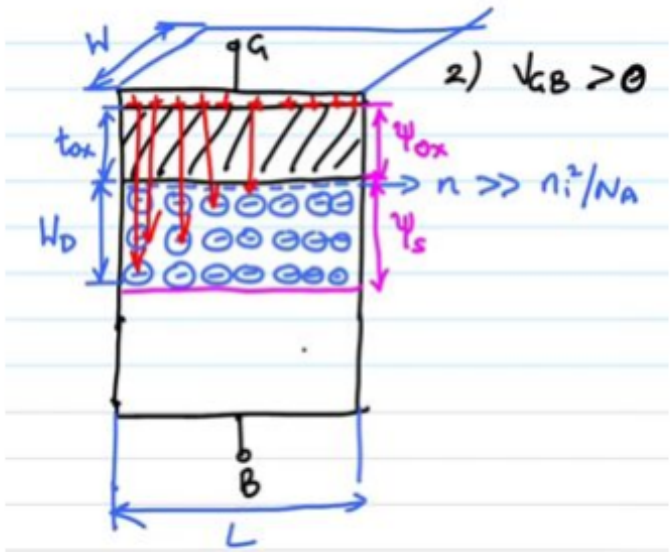
$R_{\square}$: sheet resistance per square of drain-source diffusion

Threshold Voltage

Gate potential needed to invert the surface is called as the threshold voltage

$$V_{GB} = potential\ across\ the\ oxide\ + potential\ across\ the\ surface$$

$$\boxed{V_{GB} = \psi ox\ + \psi s \text{ ---------} (1)}$$



L – Length of the channel
W – Width of the channel
ψox potential across oxide
ψs potential across surface
t_{ox} thickness of oxide layer
W_D width of the depletion region

- The electric field terminates across the immobile –ive charges and also at the free electrons.
- As the electrons are attracted towards the surface, Beyond a certain point the surface potential is pinned as a small increase in the surface concentration is like 'ln' of that and therefore the ---- stop increasing

$$\ln\left(\frac{n_s}{n_B}\right) = \frac{q\,\psi s}{KT} \text{ ----- (a)}$$

Surface Potential , ***ψs is pinned*** *when the surface concentration is approximately equivalent to the bulk concentration*

$$\text{i.e., } n_s \cong N_A$$

$$\psi s = \frac{KT}{q} \ln\left(\frac{n_s}{n_B}\right) \text{ ------ (2)}$$

Threshold Voltage

Strong inversion **occurs at a voltage equal to twice the** ***Fermi Potential***

$$\psi s = 2\frac{KT}{q}\ln\left(\frac{N_A}{n_i}\right) = 2(\text{Fermi potential}) = 2\emptyset_F$$

Gate potential needed to invert the surface is given as

$$\frac{Q_I'}{C_{ox}} = \psi s - \frac{\left(\sqrt{2\varepsilon_{si}|\psi_s|q\,N_A}\right)}{C_{ox}} = Vth \quad ----(8)$$

where, $\psi s = 2\frac{KT}{q}\ln\left(\frac{N_A}{n_i}\right) = 2(\text{Fermi potential}) = 2\emptyset_F$, ***Strong inversion*** **occurs at a voltage equal to twice the** ***Fermi Potential***

Threshold Voltage

In general the value of V_{GS} where strong inversion occurs is called the *threshold voltage* V_T

V_T is a function of several components, most of which are material constants such as

- the difference in work-function between gate and substrate material
- the oxide thickness
- the Fermi voltage
- the charge of impurities trapped at the surface between channel and gate oxide
- the dosage of ions implanted for threshold adjustment

in case a substrate bias voltage V_{SB} is applied, then $\psi s = |-2\emptyset_F + V_{SB}|$

V_{SB} is normally positive for *n*-channel devices

$$In\ general, V_{th} = V_{To} + \gamma\left(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|}\right) \quad ---(9)$$

empirical parameter V_{T0}, which is the threshold voltage for V_{SB} = 0, the parameter γ (gamma) is called the *body-effect coefficient*, and expresses the impact of changes in V_{SB}.

Observe that the threshold voltage has a **positive** value for a typical **NMOS** device, while it is **negative** for a normal **PMOS** transistor.

Threshold Voltage: Effects

$$In\ general, V_{th} = V_{To} + \gamma\left(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|}\right) \quad ---(9)$$

- In equation(9) states that the threshold voltage is only a function of the manufacturing technology and the applied body bias V_{SB}. The threshold can therefore be considered as a constant over all NMOS (PMOS) transistors in a design.
- **As the device dimensions are reduced, this model becomes inaccurate, and the threshold potential becomes a function of *L*, *W*, and V_{DS}.**

- In a **long channel device**, the channel formation is controlled by the gate and the substrate. **The gate voltage** will control essentially **all the space charge induced in the channel region**.
- As the channel length decreases, the charge control of the channel is shared by the four terminals (gate, substrate, source and drain), called charge sharing.
- The total charge below the gate controlled by the gate voltage in a short-channel device is correspondingly less than that controlled by the gate in a long-channel device.
- Consequently, **a lower gate voltage is required to attain threshold in a short-channel device**. Now as the drain voltage increases the reversed biased space charge region at the drain extends further into channel area and the gate will control even less bulk charge.
- i.e., in a short channel device the n+ type source and the drain induce a significant amount of the depletion charge that cannot be neglected. The depletion regions of the source and the drain are very close to one another.

Threshold Voltage: Effects

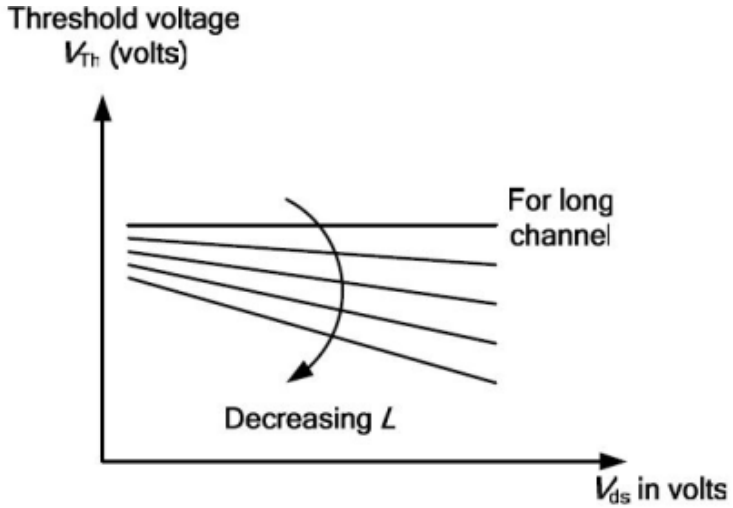


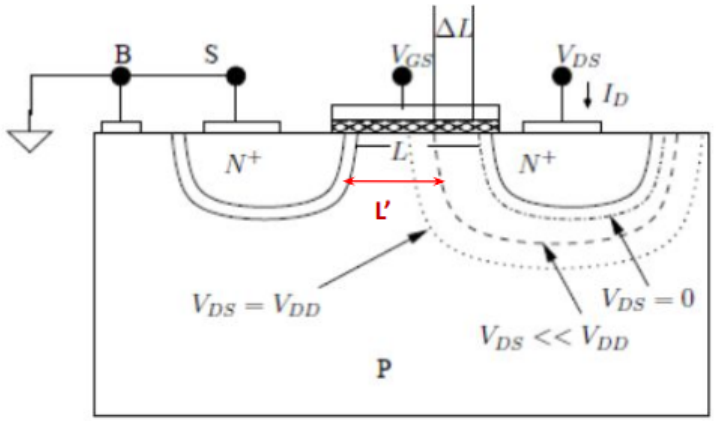
Figure 1: Effective threshold voltage as a function of *V*ds taking *L* as parameter for an n-channel MOSFET

- The deeper depletion region is accompanied by larger surface potential, which makes the channel more attractive for electrons. Thus, the device can conduct more current.
- This effect can be considered as the reduction of V_{Th} as drain current is the function of (V_{gs}-V_{Th}).
- Increase in V_{ds} and reduction of channel length will decrease the effective threshold voltage as shown in figure 1.
- Curve representing the reduction of V_{Th} with decreasing effective channel length is known as V_{Th} roll off. This adverse roll-off effect is perhaps the most daunting roadblock in future MOSFET design . The minimum acceptable channel length is primarily determined by this roll-off.

Channel length Modulation

- As per equation (9), the transistor in the **saturation mode acts as a perfect current source** or that the current between drain and source terminal is a constant, independent of the applied voltage over the terminals. **This not entirely correct.**
- The effective length of the **conductive channel is actually modulated by the applied V_{DS}**: increasing V_{DS} causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

$$I_{ds} = \beta \left[\frac{V_{ds}^2}{2}\right] \text{ -- (9)}$$



L = L' - ΔL

Note:

- Channel length modulation effect is more visible in short channels

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

the current increases when the length factor L is decreased

A **more accurate description of the current of the MOS transistor** is therefore given in equation (10)

$$I_D = I_D'(1 + \lambda V_{DS}) \quad \text{---- (10)}$$

with I_D' the current expressions derived earlier, and λ an empirical parameter, called the *channel-length modulation*.

Velocity Saturation

- The behavior of transistors with very short channel lengths (called *short-channel devices)* deviates considerably from the resistive and saturated models, due to channel length modulation

- **The main culprit for this deficiency is the *velocity saturation effect*.** *Eq. (11)* $\upsilon_n = -\mu_n \xi(x) = \mu_n \frac{dV}{dx}$ states that the velocity of the carriers is proportional to the electrical field, independent of the value of that field.
  - The electric field is given by $dV/dx = V_{ds}/L$, So if the channel length is reduced then dx gets too small blowing up the electric field and hence saturating the velocity.
  - The velocity is saturated beyond a critical field $E_{critical}$. Electrons encounter more collision and hence don't pick up speed.
  - **Maximum velocity of electrons/holes = 10^5 m/s.**

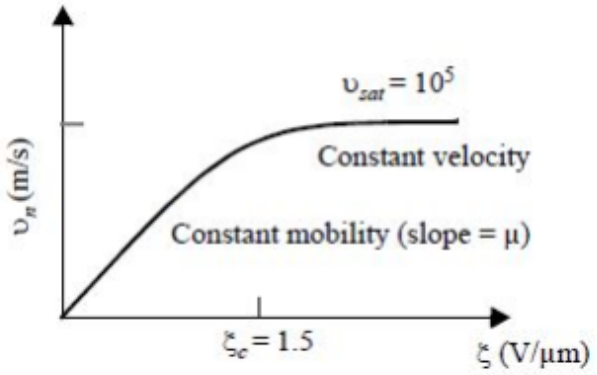


Fig. a : Velocity-saturation effect

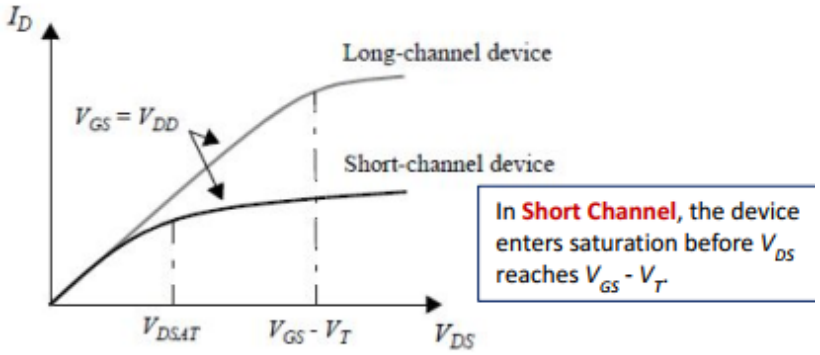


Fig. b: Short-channel devices display an extended saturation region due to velocity-saturation

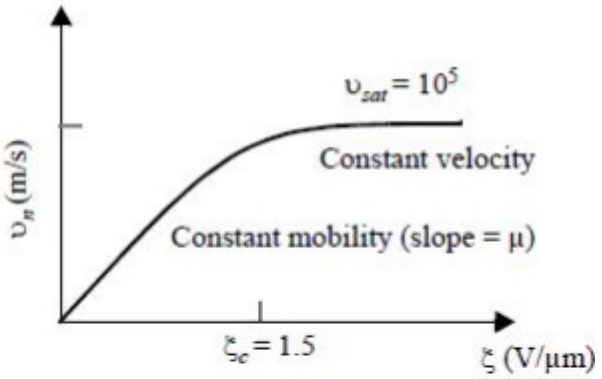


Fig. a : Velocity-saturation effect

$$\upsilon = \frac{\mu_n \xi}{1 + \xi/\xi_c} \quad \text{for} \quad \xi \le \xi_c$$

$$= \upsilon_{sat} \quad \text{for} \quad \xi \ge \xi_c$$

- In other words, the carrier mobility is a constant. However, **at high field strengths, the carriers fail to follow this linear model.** In fact, **when the electrical field along the channel reaches a critical value** $E_{critical}$, ***the velocity of the carriers tends to saturate*** **due to scattering effects** (collisions suffered by the carriers).

Mobility Degradation

There are two reasons for mobility reduction in MOSFET

1. Mobility reduction with the gate voltage due to the vertical electric field
2. Mobility reduction with the drain voltage due to the horizontal electric field

- So far we have only considered the effects of the **tangential field** along the channel du to the V_{DS}, when considering **velocity-saturation effects**.
- However, there **also exists a normal (vertical) field originating from the gate voltage** that further inhibits channel carrier mobility. This effect, which is called ***mobility degradation***, reduces the surface mobility with respect to the bulk mobility. Eq. (12) provides a simple estimation of the mobility reduction.

$$\mu_H = \frac{\mu_0}{1+\frac{V_{ds}}{L_{eff}E_{crit}}} = \frac{\mu_0}{1+\theta_2 V_{ds}} \quad \text{----- (12)}$$

- $1/L_{eff}E_{crtit}$ is referred as drain bias mobility reduction parameter and in some texts denoted as θ_2. E_{crit} is the electric field shown in figure (a)
- For large transistor θ_2 is smaller than 1 thus $\mu_H = \mu_0$.
- **when L_{Eff} decreases, $\theta_2$increases and $\theta_2 V_{ds}$ becomes important, lowering the mobility below μ_0**

Mobility Degradation

Mobility reduction with the gate voltage due to the vertical electric field

In a MOS transistor, **the current flows very close to the silicon surface**. As a consequence, the **mobility of current carriers is lower than deep inside the substrate** (typically two to three times lower), **due to various scattering mechanisms**

- A **vertical electric field** exists in MOSFET due to the applied gate voltage, which creates the conduction channel.
- When carriers move within the channel under the effect of horizontal electric field, they feel the effect of gate induced vertical electric field, **pushing carriers towards the gate oxide** as shown in figure 2.

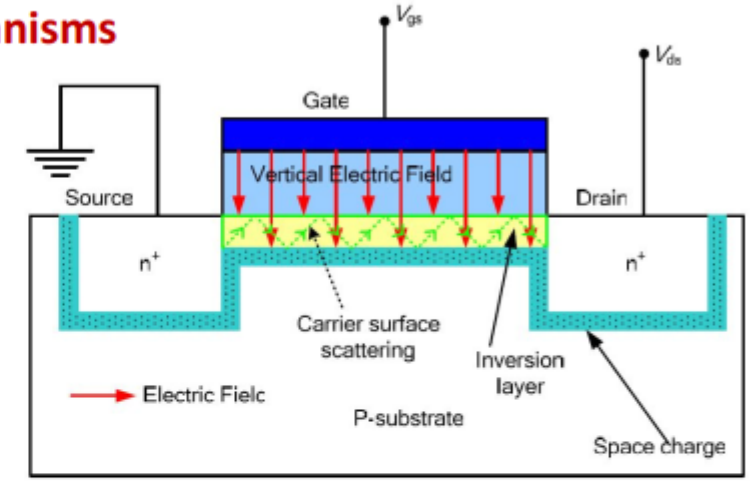


Figure 2: Vertical electric field in a short channel MOSFET and due to that surface scattering

- This provokes carriers to make the collision with the oxide channel interface. The oxide –channel interface is rough and imperfect, thus carriers loses mobility. This **effect is known as surface scattering.**

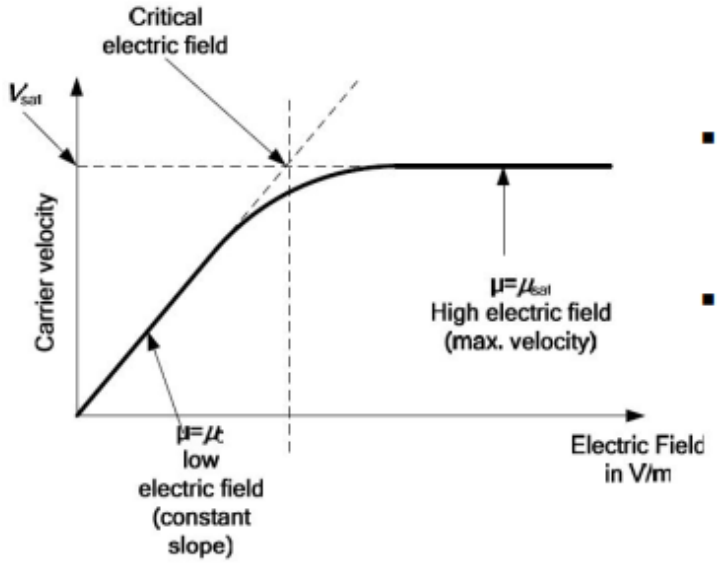
- The **surface mobility depends on how much the electrons interact with the interface**, and therefore, on the vertical electric field which "pushes" the electrons against the interface. We will note **as the surface mobility in absence of such an electric field. The higher the electric field, the lower is the surface mobility.**

Mobility Degradation

The reduction in the surface mobility can be modeled as

$$\mu_H = \frac{\mu_0}{1+\frac{V_{ds}}{L_{eff}E_{crit}}} = \frac{\mu_0}{1+\theta_2 V_{ds}}$$

- $1/L_{eff}E_{crtit}$ is referred as drain bias mobility reduction parameter and in some texts denoted as θ_2. E_{crit} is the electric field shown in figure (a)
- For large transistor θ_2 is smaller than 1 thus $\mu_H = \mu_0$.
- **when L_{Eff} decreases, θ_2 increases and $\theta_2 V_{ds}$ becomes important, lowering the mobility below μ_0**



- At **low electric field**, the **electron drift velocity** V_d in the **channel varies linearly** with the electric field intensity.
- However as **the electric field increases above 10^4 V/cm**, the **drift velocity tends to increase more slowly**, and approaches **a saturation value of $V_{d(sat)} = 10^7$ cm/s** around the electric field $=10^5$ v/cm at 300k

Figure a: Electric field versus Carrier velocity in a solid