ADITYA KANNAV

DESIGN & VERIFICATION ENGINEER

CONTACT

+91 9623996412

kannav.aditya@gmail.com

https://tinyurl.com/3vb2raku

https://github.com/adityak95

At.Post mahur Dist. Nanded

EDUCATION

2019 - 2023
PIMPRI CHINCHWAD COLLEGE OF ENGINEERING
- BE-Electronics & Telecommunication
- CGPA: 7.92 / 10.0

2018 - 2019
BLUE BELLS JR. COLLEGE
- HSC-PCM
- Percentage-71.69

2016 - 2017
ARYA CHANAKYA VIDYADHAM
- Percentage-89.60

TECHNICAL SKILLS

- DIGITAL DESIGN
- VERILOG
- SYSTEM VERILOG
- UNIVERSAL VERIFICATION METHOD (UVM) ESSENTIALS
- BASIC APB , AHB PROTOCOL
- UART , SPI , I2C PROTOCOLS
- AXI PROTOCOL
- LINUX

TOOLS

- QUESTASIM & MODELSIM
- GVIM , EDA PLAYGROUND
- VIRTUAL UBUNTU(PROMPT)
- MICROSOFT POWER BI

PROFILE

A hardworking and passionate job seeker with strong organizational skills eager to secure an entry-level **Verilog** Programmer position. Ready to help the team achieve the company's goals. Offering excellent communication, teamwork, multitasking, quick adaptable, time management, positive attitude, an organized and dependable candidate. Having knowledge of **Python basics, Verilog, System verilog, UVM Essentials, protocols.**

CAREER

To gain more knowledge while working with people of different background in order to improve myself as a good professional as well as good person.

PROJECTS

SPI Controller
JULY-2024

- Developed a **synthesizable** SPI controller module that enabled efficient communication between **master** and **slave** devices, ensuring reliable data transfer and minimizing errors.
- Implemented **clock domain crossing** increase in data transfer rate, while reducing power consumption.
- Wrote comprehensive testbenches in verilog and system verilog & UVM to verify the SPI controller's functionality, ensuring compliance with SPI protocol standards .

Interrupt Controller
JULY-2024

- Developed a flexible and scalable interrupt controller module that enabled efficient **handling of multiple interrupt** sources, **prioritization**, and masking, ensuring seamless interaction between peripherals and the processor.
- Created a robust interrupt handling mechanism that supported edge-triggered and level-triggered interrupts, with features such as interrupt nesting, prioritization, and vectored interrupts, ensuring efficient and reliable system response to interrupts.

First In First Out
JULY -2024

- Developed a synthesizable FIFO module that enabled efficient **data buffering** and transfer between **asynchronous clock domains**, ensuring data integrity and minimizing errors.
- Incorporated features such as programmable depth, almost-full and almost-empty flags, and optional data width conversion, while optimizing the design for **low area and power consumption**.
- Wrote comprehensive testbenche in verilog and system verilog and UVM to verify the FIFO's functionality, including simulation of various data transfer scenarios, error injection, and corner cases, ensuring correct data storage and retrieval, and achieving 100% code coverage.

INTERNSHIP

VLSIGURU-DV Engineer **April 2024 - Ongoing**

- Learned about verilog HDL language and various verification language such as system verilog and UVM.
- Learned AXI ,basics of APB & AHB , I2C , SPI , UART protocols.
- Did various projects in verilog such as memory ,FIFO ,Pattern Detector, SPI and INTERRUPT controller etc.
- Did the verification in Systen Verilog and UVM Essentials .

SOFT SKILLS

- Problem Solving and Analytical Skill
- Time management & project management
- Good Communication & Presentation Skills
- Quick Adaptability
- Multitasking
- Teamwork
- Microsoft Suite

ACHIEVEMENTS

- Member Civil services club
- Sports Secretary of college
- Member of ETSA
- Cleared CDS & AFCAT
- Member of Discipline committee

TRAINING & CERTIFICATION

The Linux Command Line Bootcamp: Beginner To Power User

- Mastered Linux commands and file management.
- gain practical experience in using command line tools, automating tasks, and troubleshooting, empowering them to become proficient Linux users

Communication Protocol: UART, SPI and I2C in Verilog on UDEMY

- Learnt to implement UART, SPI, and I2C protocols in Verilog.
- Gain hands-on experience with communication interfaces in digital design.

HOBBIES & INTEREST

- Volleyball
- Trekking
- Reading Books

LANGUAGES

- English (Fluent)
- Marathi (Fluent)
- Hindi (Fluent)

DECLARATION

I hereby declare that information in this document is correct to my knowledge and I bear the responsibility for the correctness of the above-mentioned particulars.