M.Tech. Embedded System and VLSI Design

Programme Structure (70 Total Credits).

1. Professional Core Courses (C)
(7 Courses)

Course Code	Course Title	Hours/ Week L	T	P	C
21MAC506T	Graph Theory and Algorithms	3	0	0	3
21ECC570J	Advanced Digital System Design	3	0	2	4
21ECC571J	Embedded Programming	3	0	2	4
21ECC572J	Embedded OS and RTOS	3	0	2	4
21ECC573J	Reconfigurable Computing	3	0	2	4
&21ECC574P	Computer Vision and Embedded AI	2	0	2	3
21ECCXXXJ	Research Methodology & Publication Ethics	2	1	2	4
	Total Learning Credits				**26**

3. Project Work(P)

Course Code	Course Title	Hours/ Week L	T	P	C
21ECP601L	Comprehensive Project Work	0	0	40	20
	OR				
21ECP602L	Condensed Project Work	0	0	30	20
21ECP603L	Domain Internship	0	0	10	
	Total Learning Credits	0	0	40	20

4. Open Elective Courses (O)
(Any 1 Course)

Course Code	Course Title	Hours/ Week L	T	P	C
21XXXXXXT	Any one Professional elective course offered by other than student's department	3	0	0	3
	Total Learning Credits				**3**

5. Mandatory Courses (Non-Credit)
(3 Course)

Course Code	Course Title	Hours/ Week L	T	P	C
21XXXXXXT	Professional Soft Skills – I	0	0	2	0
21XXXXXXT	Professional Soft Skills – II	0	0	2	0
	Total Learning Credits	**0**	**0**	**4**	**0**

2. Professional Elective Courses (E)
(7 Courses)

Course Code	Course Title	Hours/ Week L	T	P	C
	Program Elective – 1				
21ECE570T	Signal Integrity for High Speed Design	3	0	0	3
21ECE571T	VLSI for Signal Processing	3	0	0	
21ECE572T	CMOS RF Circuit Design	3	0	0	
21ECE573T	Multiprocessor Real Time Systems	3	0	0	
21ECE574T	Microcontroller Architecture Programming	3	0	0	
21ECE575J	Sensing and Actuation from Devices	2	0	2	
	Program Elective – 2				
21ECE576T	Networks on Chip	3	0	0	3
21ECE577J	VLSI Architecture for System Design	2	0	2	
21ECE578J	Soft Computing	2	0	2	
	Program Elective – 3				
21ECE579T	Algorithms for VLSI Design Automation	3	0	0	3
21ECE580T	CAD Tools for VLSI	3	0	0	
$21ECE581T	Testing of VLSI Circuits	3	0	0	
	Program Elective – 4				
21ECE582T	Hardware – Software Co-design of Embedded System	3	0	0	3
21ECE583T	Computer Aided Design Automation	3	0	0	
21ECE584T	Design of Embedded Control System	3	0	0	
	Program Elective – 5				
21ECE670T	VLSI for Wireless Communications	3	0	0	3
21ECE671T	Machine Learning for VLSI	3	0	0	
21ECE672T	CMOS Analog IC Design	3	0	0	
	Program Elective – 6				
$21ECE673T	Robotics and Control	3	0	0	3
$21ECE674T	Medical Electronics and Instrumentation	3	0	0	
21ECE675T	Embedded Automation Systems	3	0	0	
	Program Elective – 7				
21ECE676T	MEMS and Micro Systems	3	0	0	3
21ECE677T	Embedded System Design	3	0	0	
21ECE678T	Embedded C	3	0	0	
	Total Learning Credits				**21**

Implementation Plan – M.Tech Embedded System and VLSI Design

Semester - I

Course Code	Course Title	Hours/ Week L	T	P	C
21MAC506T	Graph Theory and Algorithms	3	0	0	3
21ECC570J	Advanced Digital System Design	3	0	2	4
21ECC571J	Embedded Programming	3	0	2	4
21ECE5XXT	Professional Elective – 1 / MOOC	3	0	0	3
21ECCXXXJ	Research Methodology & Publication Ethics	2	1	2	4
21XXXXXXT	Professional Soft Skills – 1	0	0	2	0
	Total Learning Credits				**18**

Semester - II

Course Code	Course Title	Hours/ Week L	T	P	C
21ECC572J	Embedded OS and RTOS	3	0	2	4
21ECC573J	Reconfigurable Computing	3	0	2	4
21ECE5XXT	Professional Elective – 2 / MOOC	3	0	0	3
21ECE5XXT	Professional Elective – 3 / MOOC	3	0	0	3
21ECE5XXT	Professional Elective – 4 / MOOC	3	0	0	3
21XXXXXXT	Professional Soft Skills – 2	0	0	2	0
	Total Learning Credits				**17**

Semester - III

Course Code	Course Title	Hours/ Week L	T	P	C
&21ECC574P	Computer Vision and Embedded AI	2	0	2	3
21ECE5XXT	Professional Elective – 5 / MOOC	3	0	0	3
21ECE5XXT	Professional Elective – 6 / MOOC	3	0	0	3
21ECE5XXT	Professional Elective – 7 / MOOC	3	0	0	3
21XXX6XXT	Open Elective / MOOC	3	0	0	3
	Total Learning Credits				**15**

Semester - IV

Course Code	Course Title	Hours/ Week L	T	P	C
21ECP601L	Comprehensive Project Work	0	0	40	20
	OR				
21ECP602L	Condensed Project Work	0	0	30	20
21ECP603L	Domain Internship	0	0	10	
	Total Learning Credits				**20**

Total Credits: 70

&: Fully Internal Course
$: Online delivery

Course Code	21MAC5O6T	Course Name	Graph Theory And Algorithms	Course Category	P	Professional Core	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Mathematics	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1:	explore the fundamental concepts of Graph Theory and its properties.
CLR-2:	infer matrix representation of graphs
CLR-3:	analyze the graph coloring and planarity
CLR-4:	explore matching theory and its properties
CLR-5:	interpret shortest path algorithms

Course Outcomes (CO):	At the end of this course, learners will be able to:	Bloom's Level	Programme Outcomes(PO)			PSO
		K1-K6	1	2	3	1
CO-1:	apply the various types of graphs, graph properties and give examples for the given property.	K3	3	3	-	-
CO-2:	model the given problem from their field to underlying graph model.	K3	3	3	-	-
CO-3:	proceed to solve the problem either through approximation algorithm or exact algorithm depending on the problem nature.	K4	3	3	-	-
CO-4:	appreciate the applications of digraphs and graphs in various communication networks.	K4	3	3	-	-
CO-5:	identify the applications of graphs and digraphs in various other fields.	K4	3	3	-	-

Module-1 - Fundamentals and Properties of Graph Theory	12 Hour
Basic definitions, examples and some results, relating degree, walk, trail, path, tour, cycle, complement of a graph, self-complementary graph, Connectedness, Connectivity, distance, shortest path, radius, diameter and Bipartite graphs. Some eccentric properties of graphs, tree, spanning tree, coding of spanning tree. Number of spanning trees in a complete graph. Recursive procedure to find number of spanning trees. Construction of spanning trees.	
Module-2 - Exploring Directed Graphs	**12 Hour**
Directed graphs: some standard definitions and examples of strongly, weakly, unilaterally connected digraphs, strong components and deadlock. Matrix representation of graph and digraphs. Some properties (proof not expected). Eulerian graphs and standard results relating to characterization of Eulerian graphs. Hamiltonian graph-standard theorems (Dirac theorem, Chavtal theorem, closure of graph). Non Hamiltonian graph with maximum number of edges. Self-centered graphs and related simple theorems.	
Module-3 - Graph Coloring and Planarity	**12 Hour**
Chromatic number; vertex chromatic number of a graph, edge chromatic number of a graph (only properties and examples)-application to coloring. Planar graphs, Euler's formula, maximum number of edges in a planar graph, some problems related to planarity and non-planarity, Five color theorem, Vertex Covering, Edge Covering, Vertex independence number, Edge independence number, relation between them and number of vertices of a graph.	

Module-4 - Matching Theory and Tournaments	***12 Hour***
Matching theory, maximal matching and algorithms for maximal matching. Perfect matching (only properties and applications to regular graphs). Tournaments, some simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs.	
Module-5 - Graph Algorithms and Complexity	***12 Hour***
DFS-BFS algorithm, shortest path algorithm, Min-spanning tree and Max-spanning tree algorithm, Planarity algorithm. Flows in graphs; Maxflow mincut theorem, algorithm for maxflow. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples.	

Learning Resources	1. *Richard J.Trudeau, "Introduction to Graph Theory", Dover Publications, Inc,New York, 1993.* 2. *Jonathan L. Gross and Jay Yellen, "Graph Theory and its Applications", Boca Raton – CRC Press 2019.* 3. *J.A. Bondy and U.S.R.Murthy, "Graph Theory with Applications", Macmillan, London, 1976, EBook, Freely Downloadable.* 4. *2. Cormen, Leiserson, Rivest and Stein, "Introduction to Algorithms", 2nd Edition, McGraw-Hill, 2001.* 5. *M.Gondran and M.Minoux, "Graphs and Algorithms", John Wiley, 1984.* 6. *H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*15%*	-	*15%*	-	*15%*	-
Level 2	*Understand*	*25%*	-	*20%*	-	*25%*	-
Level 3	*Apply*	*30%*	-	*25%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*25%*	-	*30%*	-
Level 5	*Evaluate*	-	-	*15%*	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. *Mr. V. Maheshwaran, CTS, Chennai, maheshwaranv@yahoo.com*	1. *Dr. K. C. Sivakumar, IIT Madras, kcskumar@iitm.ac.in*	1. *Dr. M. Sivaji, Assistant Professor, Department of Mathematics, SRM IST, Tiruchirappalli.*
	2. *Dr. Y V S S. Sanyasiraju, IIT Madras, sryedida@iitm.ac.in*	2. *Dr. C.Arun kumar, Assistant Professor, Department of Mathematics, SRM IST, Tiruchirappalli.*

Course Code	21ECC570J	Course Name	Advanced Digital System Design	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		NIL	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*Provide basic understanding on Digital System design*
CLR-2:	*introduce complex design and understand the finite state machines*
CLR-3:	*design of advanced circuit and Design the advanced sequential logic circuits*
CLR-4:	*Design of data paths and control unit*
CLR-5:	*introduce the concepts of Built-In-Self-Test, concepts behind Memory and Fault testing*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*Attain comprehensive understanding of computer arithmetic fundamentals.*	K3	2	2	3	2
CO-2:	*Attain comprehensive understanding of digital design fundamentals*	K3	2	2	3	2
CO-3:	*Attain understanding in designing and analysing combinational circuit and subsystems.*	K4	2	3	3	3
CO-4:	*Attain understanding in designing and analysing sequential circuit and subsystems.*	K4	3	3	3	3
CO-5:	*Enable design of data path units and control units for microcomputer designs.*	K4	3	3	3	3
C0-6	*Understand digital logic testing methods for reliability and their applications.*	K4	3	3	3	2

Module-1: PROCESSOR ARITHMETIC: ***15 Hours*** *Two's Complement Number System – Arithmetic Operations, Floating Point Number system – IEEE 754 format & POSIT Basic binary codes.*
Module-2: COMBINATIONAL LOGIC DESIGN - ***15 Hours*** *Functional blocks – Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators, Adders, subtractors, carry look- ahead adder, timing analysis. Combinational multiplier structures. Timing hazards*

Module-3: SEQUENTIAL LOGIC DESIGN	***15 hours***
Latches and Flip-Flops, Sequential logic circuits – timing analysis (Set up and hold times) Synchronizers and met stability, State machines – Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; FSM Design examples: Vending machine, Traffic light controller, Washing machine.	
Module-4: DIGITAL SUBSYSTEMS	***15 Hours***
ALU, 4-bit combinational multiplier, Barrel shifter, Simple fixed point to floating point encoder, Dual Priority encoder, Cascading comparators.Pattern (sequence) detector, Programmable Up-down counter, Round robin arbiter with 3 requesters Process Controller, FIFO	
Module-5: DIGITAL LOGIC TESTING	***15 Hours***
Introduction to digital logic testing Fault modelling, fault collapsing, fault simulation, test generation, Introduction to Design For Testability(DFT),DFT and Built-In-Self-Test(BIST)	

Learning Resources	1. *Digital Design by M. Morris R. Mano and Michael D. Ciletti., Person Education.* 2. *Digital Design by Frank,John Wiley and Sons Publishers.* 3. *Digital Computer Arithmetic Datapath Design Using Verilog HDL by James E. Stine, Spinger* 4. *Gustafson and Yonemoto. 2017. Beating Floating Point at its Own Game: Posit Arithmetic. Supercomputing Frontiers and Innovations: an International Journal, Volume 4I, ssue 2, June 2017 , pp 71–86, https://doi.org/10.14529/jsfi170206.*	5. *Digital Design Principles and Practices by John F. Wakerly, Pearson Education.* 6. *An Introduction to Logic Circuit Testing by Parag K. Lala, Morgan & Claypool Publishers.* 7. *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by M. Bushnell , Vishwani Agrawal,Springer.* 8. *Digital Systems Testing and Testable Design by Melvin A. Breuer , Arthur D. Friedman, Miron Abramovici, Wiley-IEEE Press.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*5%*	*5%*	*15%*	*15%*	*10%*	
Level 4	*Analyze*	*10%*	*5%*	*15%*	*15%*	*10%*	
Level 5	*Evaluate*	*5%*	*5%*	*10%*		*10%*	
Level 6	*Create*	-		-		*5%*	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. *Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member* 2. *Venkat Sunkara, Founder & CEO, ChipEdge Technologies Pvt Ltd, Bengaluru.*	1. *Dr.Pratap Kumar S, Director, NIELIT Calicut* 2. *Mr. Nanda Kumar. R Scientist – D, NIELIT Calicut- VLSI*	*Dr. S. Aditya, Assistant Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	21ECC571J	Course Name	Embedded Programming	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*Attain comprehensive understanding of fundamentals of C Programming*
CLR-2:	*Attain comprehensive understanding of Embedded C*
CLR-3:	*Attain comprehensive understanding of Embedded Programming and development Tools*
CLR-4:	*Attain comprehensive understanding of fundamentals of Comprehend the fundamentals of C++*
CLR-5:	*Attain comprehensive understanding of the state-of- art hardware and software tools for Embedded software development*
CLR-6	*Attain comprehensive understanding of the Embedded Programming Coding standards & Concepts*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*Attain comprehensive understanding of fundamentals of C Programming*	K3	2	3	3	2
CO-2:	*Attain comprehensive understanding of Embedded C*	K3	2	3	3	2
CO-3:	*Attain comprehensive understanding of Embedded Programming and development Tools*	K4	3	3	3	3
CO-4:	*Attain comprehensive understanding of fundamentals of Comprehend the fundamentals of C++*	K4	3	3	3	3
CO-5:	*Attain comprehensive understanding of the state-of- art hardware and software tools for Embedded software development.*	K4	3	3	3	3
CO-6:	*Attain comprehensive understanding of the Embedded Programming Coding standards & Concepts*	K3	3	3	3	2

Module-1: Introduction to Programming & algorithms for problem solving ***15 Hours***

The Basic Model of Computation, Algorithms, Flow-charts, Programming Languages, Compilation, Linking and Loading, Testing and Debugging, Algorithms for Problem Solving: Decimal Base to Binary Base conversion, Reversing digits of an integer, GCD (Greatest Common Division), LCM etc.

Practice 1: *Design flow-charts for the algorithms of various algorithms.*

Module-2: C Programming Basics	***15 Hours***
GNU Tools: gcc, gdb, gprof, Makefiles, Basic data types, operations, and flow control (decision-making statements), Flow control (loops), typecasting, and computer logic, Switch-case, arrays, and the basics of strings, pointers, functions, storage class. ***Practice 2:*** *gcc introduction, c programming basics,* ***Practice 3:*** *flow control, decision making C programming examples,* ***Practice 4:*** *arrays, strings, pointers,* ***Practice 5:*** *functions*	
Module-3: Advanced C programming for Embedded Systems Deep Learning	***15 Hours***
Structure and union, Linear and nonlinear data structures, Linked List. ***Practice 6:*** *Structures and unions,* ***Practice 7:*** *Data structures,* ***Practice 8:*** *Linked Lists*	
Module-4: Object Oriented Programming concepts with C++	***15 Hours***
Overview of C++, Fundamentals of the object-oriented approach, Class hierarchy, Advanced class concepts, Templates, Accessing data and dealing with exceptions. ***Practice 9****: Access specifiers, constructers and destructors,* ***Practice 10:*** *Hierarchy in C++,* ***Practice 11:*** *Polymorphism in C++,* ***Practice 12:*** *Templates,* ***Practice 13:*** *Exception Handling*	
Module-5: Scripting tools for Embedded Applications	***15 Hours***
Introduction to Bash scripting, Shell basics: environment, variables and commands, Python basics: syntax, variables and data types, Writing & running Python scripts, Functions, modules & packages ***Practice 14:*** *Bash scripting examples,* ***Practice 15:*** *Python scripting examples*	

Learning Resources	1.	*C Programming language, Kernighan, Brian W, Ritchie, Dennis M, Prentice Hall PTR*
	2.	*"Embedded C",Michael J. Pont, Addison Wesley*
	3.	*The Complete Reference C++, Herbert Schildt, TMH*
	4.	*GNU C++ For Linux, Tom Swan , Prentice Hall India*
	5.	*Gowrishankar S & Veena A, "Introduction to Python Programming", CRC Press, Taylor & Francis Group, 2019.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*			*15%*	*5%*	
Level 2	*Understand*	*10%*			*15%*	*10%*	
Level 3	*Apply*	*10%*			*30%*	*10%*	
Level 4	*Analyze*	*15%*			*30%*	*15%*	
Level 5	*Evaluate*	*10%*			*10%*	*10%*	
Level 6	*Create*	-			-	-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Mr.M.K. Martin, Scientist – F & Chief Investigator, NIELIT, Calicut* 2. *Mr. Rajesh. M, Scientist E, NIELIT Calicut*	1. *Dr. Noor Mahammad, Associate Professor, Department of CSE, IIITDM, Kancheepuram, Chennai.* 2. *Dr. M. Gulam Nabi Alsath, Associate Professor, Department of ECE, Anna University, College of Engineering, Guindy, Chennai.*	*Dr.S.Anandpushparaj, Assistant Professor, Department of ECE, SRMIST, Tiruchirappalli*

Course Code	21ECC572J	Course Name	Embedded OS & RTOS	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*Get knowledge in Embedded OS (Linux) fundamentals*
CLR-2:	*Comprehend Embedded Processor and its software*
CLR-3:	*Comprehend Embedded Linux Drivers*
CLR-4:	*Learn about the basics of real-time concepts*
CLR-5:	*Incorporate RTOS in an Embedded system.*
CLR-6	*Apply the knowledge for developing practical applications of modern real-time systems.*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*Get knowledge in Embedded OS (Linux) fundamentals*	K3	3	3	3	2
CO-2:	*Comprehend Embedded Processor and its software*	K3	2	3	3	2
CO-3:	*Comprehend Embedded Linux Drivers*	K3	3	3	3	3
CO-4:	*Learn about the basics of real-time concepts*	K4	3	3	3	3
CO-5:	*Incorporate RTOS in an Embedded system.*	K4	3	3	3	3
CO-6:	*Apply the knowledge for developing practical applications of modern real-time systems.*	K3	3	3	3	2

Module-1: Introduction to Embedded Linux ***15 Hours***

Overview of Linux OS, Directory structures, basic Linux shell commands, Overview of Systems Calls, Classification of system Calls, Inter Process Communication, Multithreading and Thread Management

Practice 1&2: *System Calls – file management,* ***Practice 3&4:*** *System Calls – Process management,* ***Practice 5&6:*** *Inter-Process communication,* ***Practice 7&8:*** *Multi-Threading.*

Module-2: Embedded Linux Driver Development ***15 Hours***

Linux Kernel Module Programming, Character device driver development, USB device driver development

Practice 9&10: *Kernel Module Programming*

Module-3: Building and Customization of Linux for Embedded systems	***15 Hours***
Linux booting procedure, Bootloader, qemu, Linux build tools ***Practice 11&12:*** *Kernel compilation*	
Module-4: *Overview of Real-Time OS*	***15 Hours***
Basics of RTOS: Real-time concepts, Hard Real-time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, RTOS Issues – Selecting a Real-Time Operating System ***Practice 13:*** *RTOS scheduling concepts*	
Module-5: RTOS for Embedded Applications	***15 Hours***
FreeRTOS, Thread creation & Management, Inter thread Communication, Mutual Exclusion, porting RTOS to Embedded hardware. ***Practice 14:*** *Threads Creations & Management,* ***Practice 15:*** *Inter Thread communication, Mutual Exclusion*	

Learning Resources	1. *GNU/LINUX Application Programming, Jones, M Tims* 2. *Sreekrishnan Venkateswaran Essential Linux Device Drivers, Prentice Hall 2008* 3. *Embedded/Real-Time Systems Concepts, Design and Programming Black Book, Prasad, KVK* 4. *Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society* 5. *Free RTOS Reference Manual*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*			*15%*	*5%*	
Level 2	*Understand*	*10%*			*15%*	*10%*	
Level 3	*Apply*	*10%*			*30%*	*15%*	
Level 4	*Analyze*	*15%*			*30%*	*10%*	
Level 5	*Evaluate*	*10%*			*10%*	*10%*	
Level 6	*Create*	-			-	-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. *Dr.Pratap Kumar S, Director, NIELIT Calicut.* 2. *Mr.M.K. Martin, Scientist – F & Chief Investigator, NIELIT, Calicut*	1. *Dr. Noor Mahammad, Associate Professor, Department of CSE, IIITDM, Kancheepuram, Chennai.* 2. *Dr.P.Sakthivel, Professor, Department of ECE, Anna University, College of Engineering, Guindy, Chennai.*	*Dr.V.N.Senthil Kumaran, Associate Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	21ECC573J	Course Name	Reconfigurable Computing	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*Introduction to hardware selection criteria*
CLR-2:	*Case studies and examples illustrating hardware selection challenges and solutions.*
CLR-3:	*Overview of SoC architecture on FPGA: buses, memory hierarchy, and interconnects.*
CLR-4:	*Fundamentals of FPGA architecture and its reconfiguration capabilities.*
CLR-5:	*Overview of FPGA IP cores and their integration into system designs.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Bloom's Level***	***Programme Outcomes (PO)***			***Programme Specific Outcome (PSO)***
		K1-K6	***1***	***2***	***3***	***4***
CO-1:	*Able to select suitable hardware for an application*	K2	2	-	3	3
CO-2:	*Able to understand the design methodology of micro-processor system on Chip (SoC) buses, memory peripherals on FPGA*	K4	2	2	3	3
CO-3:	*Build reconfigurable system using FPGAs*	K6	2	3	3	3
CO-4:	*Able to evaluate hardware accelerator and achieve acceleration factor for a specific application.*	K6	3	3	3	3
CO-5:	*Demonstrate an embedded system on FPGA using IP blocks.*	K6	3	3	3	3

Module-1: Introduction to Reconfigurable Computing ***15 Hours***

Reconfigurable Architectures: Classification of Reconfigurable Architectures- FPGA Technology and Architectures, LUT devices and Mapping, Placement and Partitioning - Programming Technology: HDL Based Programming and High level Synthesis using C, Partial Reconfiguration- Intellectual Property Based Design: Soft core, Firm core and Hard Core, Software tools.

Module-2: System on chip (SoC) system in FPGA devices	***15 Hours***
Embedded computer organization and methodology of System on chip (SoC) system in FPGA devices-Design challenges and Differences GPP, DSP, ASIC and FPGA based System On Chip platforms-Application profiling and partitioning, FPGAs vs. Multi-core processor architectures- Xilinx Zynq 7000 family programmable SoC (system on chip) in particular - hybrid device with ARM + FPGA architecture.	
Module-3: Bus-protocols and Intellectual Property study	***15 Hours***
Overview of AXI Bus protocol-Design of Master and Slave Bus protocols based IPs-Design Metrics, General purpose peripherals (interrupt, timer, clock, DMA etc.) -special purpose peripherals Serial Transmission protocols & Standards-advanced high speed buses-Debugging methodologies.	
Module-4: Emulating SoC Architectures on FPGAs	***15 Hours***
Emulating SoC Architectures on FPGAs-Emphasis on different embedded processors and multiprocessor and architectures-Coprocessor creation, hardware design for System-On-a-Chip-Memory and peripheral interfacing.-System level design Tradeoffs, Power, Energy, Performance and Area.	
Module-5: Analysis and case-studies	***15 Hours***
Exploration of HLS tools, System Modeling-Models of Computation and System Specification Languages, High Level Computation/Behavioral Synthesis-Application case study like FFT, JPEG.	

Learning Resources	1. *R. Sass and A. G. Schmidt. Embedded Systems Design with Platform FPGAs Principles and Practices. Elsevier Inc, USA, 2010.* 2. *The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC, Strathclyde Academic Media , UK ,2014* 3. *S. Hauck and A. DeHon, Reconfigurable Computing: The Theory and Practice of FPGA-Based Computing, Morgan Kaufmann, 2008.* 4. *Cardoso, João M. P.; Hübner, Michael (Eds.), Reconfigurable Computing: From FPGAs to Hardware/Software Codesign, Springer, 2011.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	*-*		*-*		*-*	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Mr.M.K. Martin, Scientist – F & Chief Investigator, NIELIT, Calicut* 2. *Mr. Rajesh. M, Scientist E, NIELIT Calicut*	1. *Dr. M. Gulam Nabi Alsath, Associate Professor, Department of ECE, Anna University, College of Engineering, Guindy, Chennai.* 2. *Dr.S.Kirubaveni, Associate Professor, Department of ECE, Anna University, College of Engineering, Guindy, Chennai.*	*Dr. S. Aditya, Assistant Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	&21ECC574P	Course Name	Computer Vision and Embedded AI	Course Category	C	Professional Core	L	T	P	C
							2	0	2	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*Provide basic understanding on Computer vision.*
CLR-2:	*Familiarize with the different types and process of machine learning*
CLR-3:	*Describe the algorithms based on Deep learning technique*
CLR-4:	*Develop AI based Embedded system*
CLR-5:	*Relate Embedded AI skill in developing real time applications*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*4*
CO-1:	*Review the fundamental concepts in Computer Vision.*	K2	2	-	3	3
CO-2:	*Illustrate the different machine learning algorithms*	K4	2	2	3	3
CO-3:	*Use the concept of Neural Network and related architectures.*	K6	2	3	3	3
CO-4:	*Construct a Machine Learning/ Deep Learning based standalone Embedded AI system.*	K6	3	3	3	3
CO-5:	*Devise the Embedded AI skill in developing real time applications*	K6	3	3	3	3

Module-1: Computer Vision ***15 Hours***

Image – Formation – Processing –Structuring Element – Morphological Operations - Kernel – Blurring and Sharpening – Thresholding – Gradients – Canny Edge Detector – Image Descriptors – Feature Descriptors – Color Histogram – Haralick Texture – Local Binary Pattern – HoG - Feature Detection and Matching.

Practice 1: *Hand Written Digit Classification using Neural Network,* ***Practice 2:*** *Hand Written Digit Classification using CNN,* ***Practice 3:*** *Regression.*

Module-2: Machine Learning ***15 Hours***

Definition – Types – Steps in Machine Learning Process – Performance Metrics - k Nearest Neighbor – k means Clustering – Support Vector Machine – Logistic Regression – Decision Tree – Random Forest – Naïve Bayes – Multilinear Regression – Principal Component Analysis – Tools and Libraries

Practice 4: *Face Detection in Images and Videos,* ***Practice 5:*** *Object Detection and Tracking in Video,* ***Practice 6:*** *Gesture Recognition.*

Module-3: Deep Learning	***15 Hours***
Neural Network - Multilayer Perceptron – Backpropagation Algorithm - Convolutional Neural Network – Parameter Estimation and Optimization – Transfer Learning – Pretrained Models - Recurrent Neural Network – LSTM – GRU – Reinforcement Learning – Tools and Libraries - Transformer architecture. ***Practice 7:*** *Automatic License Plate Recognition,* ***Practice 8:*** *Semantic Segmentation,* ***Practice 9:*** *Text Classification.*	
Module-4: Embedded System Development	***15 Hours***
Open Source Packages and Development Environments - GPU/TPU Supported Boards – Porting OS – Peripheral Interfacing (Input Devices, Output Devices, Sensors, Actuators) – Camera Interface - Porting Machine Learning/Deep Learning Algorithms – Enabling RTOS – Scheduling – GPU Parallel Computing – Computing Strategy. ***Practice 10:*** *Image Captioning,* ***Practice 11:*** *Unauthorized Entry Identifier,* ***Practice 12:*** *Automatic Guided Vehicle.*	
Module-5: Case Studies	***15 Hours***
Hand Written Digit Classification using Neural Network and CNN - Regression – Face Detection in Images and Videos – Object Detection and Tracking in Video – Gesture Recognition – Automatic License Plate Recognition – Semantic Segmentation - Text Classification – Image Captioning Unauthorized Entry Identifier-Automatic Guided Vehicle-IoT based multi-Parameter Monitoring System-Smart Attendance System-Smart Surveillance System ***Practice 13:*** *IoT based multi-Parameter Monitoring System,* ***Practice 14:*** *Smart Attendance System,* ***Practice 15:*** *Smart Surveillance System.*	

Learning Resources	*1. Avimanyu Bandyopadhyay, "Hands-on GPU Computing with Python", Packt Publishing, 2019.* *2. Salman Khan, Hossein Rahmani, Syed Afaq Ali Shah and Mohammed Bennamoun, "A Guide to Convolutional Neural Networks for Computer Vision", Morgan & Claypool Publishers, 2018.* *3. Adrian Rosebrock, "Deep Learning for Computer Vision with Python", PyImageSearch, 2017.* *4. Kevin P. Murphy, "Machine Learning – A Probabilistic Perspective", The MIT Press Cambridge, Massachusetts, London, England, 2012.* *5. Richard Szeliski, "Computer Vision – Algorithms and Applications", Springer – Verlag London Limited, 2011.*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3 (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	*5*	*5*	*5*	*5*	*5*	*5*	*5*	-
Level 2	Understand	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 3	Apply	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 4	Analyze	*15*	*15*	*15*	*15*	*15*	*15*	*15*	-
Level 5	Evaluate	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 6	Create	-	-	-	-	-	-	-	-
	Total	100%		100 %		100 %		100 %	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
Jagadeeshwaran Senthilvelan, CEO, *Protohubs.io, Chennai.*	*Dr. B. Rebekka, Associate Professor* *NIT Tiruchirappalli*	*Dr. S. Aditya, Asst. Professor* *SRMIST Tiruchirappalli*

Course Code	21ECE570T	Course Name	Signal Integrity for High Speed Design	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*Provide basic understanding of signal integrity issues in high-speed PCBs.*
CLR-2:	*Familiarize with the frequency dependent model development*
CLR-3:	*Discover the crosstalk issue in high-speed PCBs*
CLR-4:	*Model the channels and I/O circuits*
CLR-5:	*Classify the noise performance and estimate budgeting*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*Interpret the fundamental concepts of signal integrity in high-speed PCBs*	K2	2	2	3	2
CO-2:	*Develop dielectric and conductor models to account for frequency-dependent properties*	K4	2	2	3	2
CO-3:	*Analyze the reason for crosstalk and devise techniques to minimize the crosstalk issue*	K4	2	2	3	3
CO-4:	*Model the channels and I/O circuits and examine its implications*	K4	3	3	3	3
CO-5:	*Estimate jitter and noise and perform budgeting*	K4	3	3	3	3

Module-1: EM Fundamentals ***9 Hours***

Importance of Signal Integrity – Electromagnetic fundamentals for signal integrity: Maxwell's equations, Wave propagation, Poynting vector, Reflections of Electromagnetic waves – Transmission line fundamentals: Transmission line structure, Transmission line reflections, Time domain reflectometry.

Module-2: Material Modelling ***9 Hours*** *Non ideal conductor models: Signals propagating in unbounded conductive media, Classic conductor model for transmission lines, Transmission line parameters for non-ideal conductors – Electrical properties of Dielectrics: Polarization of dielectrics, Classification of dielectric materials, frequency dependent dielectric behaviour, properties of physical dielectric model, Fiber-weave effect, Environmental variation in dielectric behaviour, Transmission line parameters for lossy dielectrics and realistic conductors*
Module-3: Crosstalk and Its Mitigation Techniques ***9 Hours*** *Mutual inductance and capacitance – Coupled wave equations – Coupled line analysis – Modal Analysis – Crosstalk minimization techniques – Differential signaling: Removal of common mode noise, differential crosstalk, virtual reference plane, propagation of modal voltages, drawbacks – Multilayer PCB stacking and Network connection*
Module-4: Channel And I/O Circuit Modelling ***9 Hours*** *Channel Modelling: Frequency domain effects in time domain analysis – Requirements of a physical channel – Creating a physical transmission line model – Non-ideal return paths – Vias – I/O Circuit Modelling: Design considerations – Push-Pull Transmitters – CMOS receivers – ESD protection circuits – On-Chip termination*
Module-5: JITTER AND NOISE: Modelling and Budgeting ***9 Hours*** *Eye diagram – Bit error rate – Jitter sources and Budgets – Noise sources and Budgets – Peak distortion analysis methods – Mixed signal design considerations*

Learning Resources	*1. Hall Stephen H. and Howard L. Heck, Advanced Signal Integrity for High-Speed Digital Designs, Wiley Publications, 2009* *2. Mike Peng Li, Jitter, Noise, and Signal Integrity at High-Speed, Prentice Hall, 2007* *3. Paul G. Huray, The Foundations of Signal Integrity, Wiley Publications, 2010* *4. Stephen C. Thierauf, Understanding Signal Integrity, Artech House, 2011* *5. Samuel H Russ, Signal Integrity: Applied Electromagnetics and Professional Practice, Springer International publishing, 2016.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
Senthil Rajan Vadivelu,Engineer-II *Rohm Semiconductors India Pvt Ltd Bangalore*	*Dr. S. Moorthi, Professor* *NIT Tiruchirappalli*	*Dr. S. Aditya, Asst. Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	21ECE571T	Course Name	VLSI for Signal Processing	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*identify the basic computation in VLSI Signal Processing*
CLR-2:	*be Familiar with concepts of Iteration Bound, Retiming, Folding*
CLR-3:	*analyze the design efficient pipelining filter design*
CLR-4:	*learn the concept of parallel processing of FIR filter and Bit-level arithmetic architectures*
CLR-5:	*develop the concepts of low power design aspects in VLSI DSP*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Bloom's Level***	***Programme Outcomes (PO)***			***Programme Specific Outcome (PSO)***
		K1-K6	***1***	***2***	***3***	***1***
CO-1:	*apply VLSI design methodology for signal processing systems*	K3	2	3	3	2
CO-2:	*interpret VLSI algorithms and architectures for DSP*	K4	2	3	3	2
CO-3:	*to implement basic architectures for DSP using CAD tools*	K4	3	3	3	2
CO-4:	*develop the design of pipelined and parallel FIR filter*	K4	1	3	3	3
CO-5:	*build low power design concepts of ASICs*	K4	1	3	3	3

Module-1: INTRODUCTION TO DSP SYSTEMS ***9 Hours***

Iteration Bound, Data flow graph representations, loop bound, iteration bound, Various mechanisms for iteration bound computation, Longest path matrix algorithm, Pipelining and Parallel Processing, Pipelining for FIR filter, Pipelining processing for low power, Parallel Processing for Low Power, Introduction to Retiming – Retiming Properties, Sample period Reduction Techniques, Parallel Processing types, Parallel processing standards.

Module-2: SYSTOLIC ARCHITECTURE AND ALGORITHM STRENGTH REDUCTION ***9 Hours***

Algorithmic strength reduction in filters, Transforms, 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge-Sort architecture, Systolic Architecture Design: Introduction,, Systolic Array Design Methodology introduction, FIR Systolic Arrays, Selection of Scheduling Vector, 2D Systolic Array Design, HDL Code for 2-parallel FIR Filter.

Module-3: FAST CONVOLUTION ***9 Hours***
Fast convolution – Cook Toom Algorithm, Modified Cook-Took Algorithm, Pipelining and Parallel recursive and adaptive filters, inefficient/efficient single channel interleaving, Parallel recursive structures, Interleaving mechanism, Look-ahead pipelining in first order IIR filters, Application of Look-ahead pipelining, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining, parallel processing of IIR filters, pipelined adaptive digital filters.
Module-4: BIT-LEVEL ARITHMETIC ARCHITECTURES ***9 Hours***
Scaling and round-off noise, scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, Round-off noise in pipelined first-order filters, Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier tabular form and implementation, Operation description of parallel carry save, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter architecture, CSD multiplication using Horner's rule for precision improvement.
Module-5: HIGH PERFORMANCE ALGORITHM FOR ASIC/SoCs ***9 Hours***
Numerical Strength Reduction, sub -expression elimination, multiple constant multiplications, iterative matching, Linear transformations, Low power Design Techniques, Introduction to wave pipelining, asynchronous pipelining bundled data versus dual rail protocol, Data Vs Dual Rail Protocol, needs for low power VLSI chips, charging and discharging capacitance, CMOS leakage current, Basic principles of low power design, short-circuit current of an inverter, DAA and computation of FFT and DCT, High performance filters using delta-sigma modulators, High Speed Data standards, High Speed Data standard applications.

Learning Resources	*1. Keshab K.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.* *2. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.* *3. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.* *4. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.* *5. Jose E. France, Yannis Tsividis, "Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*		*20%*		*20%*	
Level 2	*Understand*	*20%*		*20%*		*20%*	
Level 3	*Apply*	*30%*		*30%*		*30%*	
Level 4	*Analyze*	*30%*		*30%*		*30%*	
Level 5	*Evaluate*	-		-		-	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Dr. Saravanan Mohan, Principal Researcher, Ericsson, India	*Dr.P.Sakthivel, Professor, Department of ECE, Anna University, College of Engineering, Guindy, Chennai.*	*Dr. V.N.Senthil Kumaran, Associate Professor, Department of ECE, SRMIST, Tiruchirappalli*

Course Code	21ECE572T	Course Name	CMOS RF Circuit Design	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*Provide basic understanding of RF Design and fundamental Transceiver architectures.*
CLR-2:	*Familiarize the concept of Impedance matching and understanding their role in the design of low noise amplifiers*
CLR-3:	*Discover different types of mixers and oscillators used in Transceiver designs*
CLR-4:	*Gain in depth knowledge on the phase locking techniques and review the frequency synthesizer architectures*
CLR-5:	*Design suitable Power amplifiers for transmitter path in transceiver design*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*Identify RF microelectronics parameters through S-parameter analysis*	K2	3	-	3	2
CO-2:	*Model and characterize LNA with impedance matching*	K3	3	2	3	2
CO-3:	*Design up/down conversion mixers and Voltage controlled oscillators*	K4	3	2	3	3
CO-4:	*Design Phase lock loops and Integer-N & Fractional-N frequency synthesizers*	K4	3	2	3	3
CO-5:	*Design Power amplifier with impedance matching*	K4	3	2	3	2

Module-1: RF systems basic architecture ***9 Hours***

Introduction to RF Circuit Design - Basic Concepts in RF Design: General Considerations, Effects of Nonlinearity, Noise, Sensitivity and Dynamic Range, Passive Impedance, Transformation, Scattering Parameters, Analysis of Nonlinear Dynamic Systems, Volterra Series, Transceiver Architectures: General Considerations, Receiver Architectures, Transmitter Architectures

Module-2: Impedance matching & Low-noise amplifiers ***9 Hours***

Impedance Matching: Definition of Q, Impedance Matching using L, PI and T networks, Integrated Inductors, Resistors, Capacitors, Tunable inductors, Transformers, Low-Noise Amplifiers: General Considerations, Problem of Input Matching, LNA Topologies, Gain Switching, Band Switching, High-IP2 LNAs, Nonlinearity Calculations.

Module-3: Mixers and Oscillators ***9 Hours***
Mixers: General Considerations, Passive Down-conversion Mixers, Active Down conversion Mixers, Improved Mixer Topologies, Up-conversion Mixers, Oscillators: Performance Parameters, Basic Principles, Cross-Coupled Oscillator, Three-Point Oscillators, Voltage-Controlled Oscillators, LC VCOs with Wide Tuning Range, Phase Noise, Design Procedure - Low-Noise VCOs, LO Interface, Mathematical Model of VCOs, Quadrature Oscillators
Module-4: Phase-locked loops & Frequency synthesizers ***9 Hours***
Phase-Locked Loops: Basic Concepts, Type-I PLLs, Type-II PLLs, PFD/CP Nonidealities, Phase Noise in PLLs, Loop Bandwidth, Design Procedure Integer-N Frequency Synthesizers: General Considerations, Basic Integer-N Synthesizer, Settling Behavior, Spur Reduction Techniques, PLL-Based Modulation, Divider Design Fractional-N Synthesizers: Basic Concepts, Randomization and Noise Shaping, Quantization Noise Reduction Techniques
Module-5: Power amplifiers & Transceiver design ***9 Hours***
Power Amplifiers: General Considerations, Classification of Power Amplifiers, High Efficiency Power Amplifiers, Cascode Output Stages, Large-Signal Impedance Matching, Basic Linearization Techniques, Polar Modulation, Out phasing, Doherty Power Amplifier, Design Examples CMOS Transceiver Design: System-Level Considerations, Receiver Design, Transmitter Design, Synthesizer Design, case study on single chip transceiver design and consideration.

Learning Resources	*1. B.Razavi, "RF Microelectronics", 2nd Edition, Pearson Education, 2012* *2. Thomas H.Lee, "The Design of CMOS Radio -Frequency Integrated Circuits', 2nd Edition, Cambridge University Press, 2004.* *3. Bosco H Leung "VLSI for Wireless Communication", 2nd Edition, Pearson Education, 2011* *4. Behzad Razavi, " Design of CMOS Analog Integrated Circuits", 2nd Edition, McGraw Hill Publications, 2017.* *5. Hooman Darabi, "Radio Frequency Integrated Circuits and Systems, 1st edition, Cambridge University Press, 2015*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
Dr. Chrisben Gladson, Sr. RF/Wireless Engineer, Renesas Electronics.	*Dr. S. Moorthi, Professor, NIT Tiruchirappalli*	*Dr. S. Aditya, Asst. Professor SRMIST Tiruchirappalli*

Course Code	21ECE573T	Course Name	Multiprocessor Real Time Systems	Course Category	E	Professional Elective	L	T	P	C
							3	1	0	4

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		NIL	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*learn Real Time Systems Basic Concepts*
CLR-2:	*apply Real Time System Design for Embedded Applications*
CLR-3:	*design Optimal Real Time Models and Learn the Uncertainties*
CLR-4:	*analyze the Basic Real Time System Design and Implementation*
CLR-5:	*develop Deep Understanding On Robust Control And Real Time Safety Procedures*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*4*
CO-1:	*illustrate the architecture and communication networks of Real Time systems*	K2	2	2	3	2
CO-2:	*Design Multi Processor models for Real Time applications*	K2	2	2	3	2
CO-3:	*Implement different practical real time systems with minimal supervision*	K4	2	2	3	3
CO-4:	*Develop Deep Understanding on selection of hardware and software's for designing systems*	K4	3	3	3	3
CO-5:	*Compare the cost effective, reliable, robust and feasible designs for real world problems*	K2	3	3	3	2

Module-1: Real Time Systems – Basic Concepts ***12 Hours***

Types Of Real Time Systems, Standard Requirement Classes, Formal Methods In System Specifications, Finite State Machines, Semiformal Methods In System Specifications, Object-Oriented Analysis, Structuring And Composing Requirements, Requirements Validation, Semiformal Methods In System Specification

Module-2: Multiprocessors ***12 Hours***

Microchip PIC18F8720, Intel 8086, Intel Pentium, ARM Processor, Introduction To Interrupts, External interrupts, Design Pattern Of Interrupt Service Routine, Interrupt Response Time, Case Study: ARM Processor Interrupt

Module-3: Real Time Operating Systems ***12 Hours***
Operating System Pseudo Kernels, Interrupt Only Systems, Priority Systems, Theoretical Foundation Of Scheduling, Scheduling Framework, Round Robin Scheduling, Cyclic Code Scheduling, Fixed Priority Scheduling, Dynamic Priority Scheduling, Systems Service For Application Programs, Linear Buffer, Ring Buffer, Deadlock And Starvation Problem, Priority Inversion Problem, Timer And Clock Servers, Memory Management Issues, Swapping Overlaying And Paging.
Module-4: Real Time Unified Modeling Language ***12 Hours***
Real Time Unified Modeling Language Profile, Meta Modeling And Resource Modeling, UML Core Resource Model, UML Stereotype For Protected Resources, Resource Usage And Client Graph, Time Modeling And Timing Mechanism, Time Modeling Stereotypes, Concurrency Modeling In UML, Elicitation Of Timing Constraints, Scheduling Jobs, Stereotype and Subprofile, Worst Case Task Execution and Response Time, Round Robin Architecture, Round Robin Interrupts, Queue Based Architecture, FIFO And Priority Queue.
Module-5: Future Visions on Real Time Systems ***12 Hours***
Real Time Hardwares, Heterogenous Soft Multi Cores, Architectural Issues With Individual Soft Cores, Field bus Networks and Simpler Distributed Nodes, One Coordinating system Task and SLO-2 Multiple Isolated Application Tasks, UML++ Programming Language, Automatic Verification of Software, Conservative Requirements Engineering, Distance Collaboration in Software Projects, Drag-and-Drop Systems, Local Networks of Collaborating Real- SLO Time Systems, Biometric Identification Device with SLO Remote Access, Performance Optimization Techniques, Scaled Numbers for Faster Execution, Look-Up Tables for Functions and Real-Time Device Drivers.

Learning Resources	*1. Phillip A. Laplante , "Real-Time Systems Design and Analysis" John Wiley & Sons, 4th Edition, 2015* *2. Xiaocong Fan, "Real-Time Embedded Systems," Elsevier 2015* *3. Edward D Lamie, "Real Time Embedded Multi Threading" , 2nd Edition, Newnes Elsevier Publication, 2005.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
Senthil Rajan Vadivelu, Engineer-II *Rohm Semiconductors India Pvt Ltd Bangalore*	*Dr. S. Moorthi, Professor,* *NIT Tiruchirappalli*	*Dr. R.Rajasekar, Asst. Professor, SRMIST Tiruchirappalli*

Course Code	21ECE574T	Course Name	Microcontroller Architecture Programming	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1:	learn about the 8051 microcontroller fundamentals
CLR-2:	acquaint with the programming of 8051.
CLR-3:	familiar with the communication buses and protocols in microcontrollers
CLR-4:	learn about the basics of STM32 microcontroller
CLR-5:	interface sensors and actuators to develop applications using STM32 microcontrollers.

Course Outcomes (CO):	At the end of this course, learners will be able to:	Bloom's Level	Programme Outcomes (PO)			Programme Specific Outcome (PSO)
		K1-K6	1	2	3	4
CO-1:	identify the architecture of 8051 and pin diagram and demonstrate addressing modes used in 8051 microcontroller and choose the various types of interrupts	K2	2	3	3	2
CO-2:	infer the data conversion program in 8051 and 8051 Hardware Connection and Intel Hex File	K2	2	3	3	2
CO-3:	apply 8 bit microcontrollers to control AC and DC motors, build applications of traffic light control	K4	3	3	3	2
CO-4:	illustrate the architecture of STM32 microcontroller and pin diagram and distinguish addressing modes	K2	1	3	3	3
CO-5:	develop UART Serial Port Programming and STM Arm Timer Programming	K4	2	3	3	3

Module-1 The 8051 Microcontrollers ***9 Hour***

The 8051 Microcontrollers: Microcontrollers and embedded processors, Overview of the 8051 family. 8051 Assembly Language Programming: Inside the 8051, Introduction to 8051 Assembly programming, Assembling and running an 8051 program, The program counter and ROM space in the 8051, 8051 data types and directives , 8051 flag bits and the PSW register, 8051 register banks and stack.

Module-2 8051 Programming In C ***9 Hour***

Data types and time delay in 805 I C, I/O programming in 8051 C, Logic operations in 8051 C, Data conversion programs in 8051 C, Accessing code ROM space in 8051 C, Data serialization using 8051 C, C Data types for Embedded Systems, Bit-wise Operations in C.

Module-3 Interrupts Programming in C ***9 Hour***

8051 interrupts, Programming timer interrupts, Programming external hardware interrupts, Programming the serial communication interrupt, Interrupt priority in the 8051/52, Interrupt programming in C.

Module-4 STM Arm I/O Programming	***9 Hour***
STM32 Microcontroller, GPIO (General Purpose I/O), Programming and Interfacing, Seven-segment LED interfacing and programming, I/O Port Programming with Assembly Language.	
Module-5 UART Serial Port Programming	***9 Hour***
Basics of Serial Communication, Section, Programming the UART Ports, Using C Library Console I/O.	

Learning Resources	*1. "The 8051 Micro Controller and Embedded Systems" Using Assembly and C SECOND EDITION, Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. McKinlay., Pearson edition.* *2. "STM32 Arm Programming for Embedded Systems", Mazidi, Muhammad Ali; Chen, Shujen; Ghaemi, Eshragh, 1st edtion, Publisher: MicroDigitalEd*	*3. Jonathan W. Valvano, Brookes, Cole, Embedded Microcomputer Systems, Real Time Interfacing, Thomas Learning,1999.* *4. Raj Kamal, Embedded Systems - Architecture Programming and Design, 2/e, Tata Mcgraw Hill, 2008.* *5. Jan Axelson, Embedded Ethernet and Internet Complete, Penram Publications,2003.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member	*Dr. Noor Mahammad, Associate Professor, Department of CSE, IIITDM, Kancheepuram, Chennai.*	*Dr. Anandpushparaj. J, Assistant Professor, Department of ECE, SRMIST, Tiruchirappalli*

Course Code	21ECE575J	Course Name	Sensing and Actuation from Devices	Course Category	E	Professional Elective	L	T	P	C
							2	0	2	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*learn Mechanical and Electromechanical sensor basic working*
CLR-2:	*analyze Thermal sensor design for embedded applications*
CLR-3:	*design optimal real time models and learn the uncertainties using radiation sensor*
CLR-4:	*build the Interface of Smart Sensors with its Applications*
CLR-5:	*interpret the functions of actuators*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	Bloom's Level	*Programme Outcomes (PO)*			Programme Specific Outcome(PSO)
		K1-K6	*1*	*2*	*3*	*4*
CO-1:	*explain the overall sensor characteristics required to make energy conversions*	K2	3	2	3	2
CO-2:	*model and summarize the functionalities of various Thermal Sensors*	K3	3	2	3	3
CO-3:	*explore the various Radiation Sensors and sensing systems for embedded devices.*	K3	3	2	3	3
CO-4:	*implement security, surveillance, energy management systems with minimal supervision using Smart sensors*	K4	3	2	3	3
CO-5:	*interface various sensors and actuators in embedded applications.*	K4	3	2	3	2

Module-1 Mechanical and Electromechanical Sensors ***15 Hours***

Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge –Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors: – Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors.

Practice: Experiments using Resistance Strain Gauge –Semiconductor Strain Gauges – Ultrasonic Sensors

Module-2 Thermal Sensors ***15 Hours***

Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors

Practice: Implementation of Thermal Radiation Sensors in an embedded board

Module-3 Radiation Sensors	***15 Hours***
Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors. Electro analytical Sensors Introduction – The Electrochemical Cell – The Cell Potential - Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization— Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media.	
Practice: Implementation of Radiation Sensors using sensor electrodes	
Module-4 Smart Sensors and its Applications	***15 Hours***
Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation. Sensors –Applications Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring.	
Practice: : IoT devices for monitoring applications and precision farming and Agriculture.	
Module-5 Actuators	***15 Hours***
Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators. Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection. Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors.	
Practice: Interfacing various sensors and actuators in embedded applications*.*	

Learning Resources	*1. D. Patranabis – "Sensors and Transducers" –PHI Learning Private Limited.*	*2. W. Bolton – "Mechatronics" –Pearson Education Limited* *3. D. Patranabis, Sensors and Actuators, 2nd Ed., PHI Learning Private Limited.*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3 (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	*5*	*5*	*5*	*5*	*5*	*5*	*5*	-
Level 2	Understand	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 3	Apply	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 4	Analyze	*15*	*15*	*15*	*15*	*15*	*15*	*15*	-
Level 5	Evaluate	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 6	Create	-	-	-	-	-	-	-	-
	Total	100%		100 %		100 %		100 %	

Course Designers

Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.	*Dr. Noor Mahammad, Associate Professor, Department of CSE, IIITDM, Kancheepuram, Chennai.*	*Dr. Anandpushparaj. J, Assistant Professor, Department of ECE, SRMIST, Tiruchirappalli*

Course Code	21ECE576T	Course Name	Networks On Chip	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*provide the fundamental concepts of various networks with design constraints*
CLR-2:	*utilize different types of networks and their applications*
CLR-3:	*familiarize the evaluation of properties of different routing and flow control*
CLR-4:	*discover the fundamental concepts of quality of service to analyze performance metrics*
CLR-5:	*utilize the evaluation of properties of routing mechanisms*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Blooms Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*design various networks by considering design constrains*	K2	1	2	3	2
CO-2:	*design and analyze the various types of networks*	K3	2	3	3	3
CO-3:	*design the routing and flow control in networks*	K4	3	3	3	3
CO-4:	*analyze the various performance metrics*	K4	1	3	3	3
CO-5:	*design the quality of service and routing mechanisms*	K4	2	3	3	2

Module-1 – Introduction to interconnection networks	***9 Hours***
Uses of interconnection networks, Network basics, A simple interconnection network, Network specifications and constraints, Topology, Routing, Flow control, Router design, Performance analysis. Case study: The SGI Origin 2000	
Module-2 – Types of Networks	***9 Hours***
Butterfly networks, Torus networks mesh networks, Non-blocking networks, Non-interfacing networks, Crossbar networks, Clos networks, Benes networks, Sorting networks. Case study: The BBN Butterfly	
Module-3 – Routing & Flow Control	***9 Hours***
Routing basics, Deterministic routing, Dimension-order routing, Adaptive routing, Adaptive routing basics, Minimal adaptive routing, Fully adaptive routing. Flow control basics, Butterfow control, Buffer management and back pressure, A flit reservation flow control, Deadlock and livelock avoidances, Deadlock and livelock avoidances in adaptive routing	

Module-4 –Quality of service & Router	***9 Hours***
Guaranteed services, Best-effort services, Router datapath components, Input buffer organization, Switches, Output organization, Arbitration, waveform allocator, processor-network interface, Shared memory interface. Case study: ATM service classes	
Module-5 – Performance analysis	***9 Hours***
Features Throughput, Latency, Fault Tolerance, Common measurement pitfalls queueing theory, Probabilistic analysis, Application-driven workloads, Synthetic workloads, Virtual channels, Network size, Injection processes, Prioritization, Stability, Fault tolerance, AHB, SPI. Case study: Efficiency and loss in the BBN Monarch network	

Learning Resources	1. *Santanu kundu Santanu Chattopadhyay, "Network-on-chip – The next generation of system-on-chip integration", CRC Press, Taylor & Francis group, 2015* 2. *Umit Y. Ogras and Radu Marculescu, "Modeling, Analysis and optimization of network-onchip communication architectures", Springer, 2013* 3. *Stavroula N.Ventoura, "NOC switch design and simulation using Matlab's Simulink", Master thesis, National and kapodistrian university of Athens, 2013.* 4. *Sudeep Pasricha and Nikil Dutt, "On-chip communication architectures – system on chip interconnect", Elsevier, 2010.*	5. *Jih-Sheng Shen and Pao-Ann Hsiung, "Dynamic reconfigurable network-on-chip design:Innovations for computational processing and communication", IGI global, 2010* 6. *William James Dally and Brian Patrick Towles, " Principles and practices of interconnection networks", the morgan Kaufmann series in computer architecture and design, 2004*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.* 2. *Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member*	*Dr. V.R. Venkatasubramani, Associate Professor, Department of ECE, Thiagarajar College of Engineering*	*Dr. K. Vaishnavi, Assistant Professor, Department of ECE, SRMIST, Tiruchirappalli*

Course Code	21ECE577J	Course Name	VLSI Architecture For System Design	Course Category	E	Professional Elective	L	T	P	C
							2	0	2	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1:	analyze all the modeling required for verilog hdl
CLR-2:	apply the methods in FPGA and FPAA
CLR-3:	learn the representation of synchronous and asynchronous finite state machines
CLR-4:	describe the controllers
CLR-5:	gain knowledge on FSM designs

Course Outcomes (CO):	At the end of this course, learners will be able to:	Bloom's Level	Programme Outcomes (PO)			Programme Specific Outcome (PSO)
		K1-K6	1	2	3	1
CO-1:	implement the digital design with programmable logic devices	K2	2	2	3	2
CO-2:	analyze the architectural features of FPGA and FPAA	K4	2	3	3	3
CO-3:	make the system level designs using synchronous and asynchronous FSMs	K4	3	3	3	3
CO-4:	design the fundamental mode FSMs using PLDs	K4	3	3	3	3
CO-5:	apply pulse mode approach to FSM design	K4	3	3	3	2

Module-1 - Verilog HDL in system design **12 Hours**

Overview-Evolution of computer- aided digital design- Typical design flow- Basic concepts- Lexical conventions, Data types, system tasks, compiler directives- Gate level modeling- Dataflow modeling – behavioral modeling – Tasks and functions- Design example.

Practice: 8 bit serial and parallel adder and 8 bit multipliers, 8:1 multiplexer using universal gates and realization of full adder using multiplexers, 4 bit code converter and 4 bit magnitude comparator

Module-2 - Programmable logic devices **12 Hours**

Logic implementation options- Technology trends – Design with Field Programmable devices – ROM, PLA, PAL – CPLD – XC9500 family – Erasable Programmable Logic Devices – MAX5000, MAX7000 families.

Practice: 8 bit fixed point arithmetic logical unit, Universal shift registers, Synchronous and asynchronous counters

Module-3 - FPGA and FPAA **12 Hours**

Programming technology, Logic blocks, routing architectures of SRAM- Programmable FPGA Architectures – XC2000, XC3000, XC4000 – Antifuse programmed FPGAs – Routing architecture of the Actel FPGAs – Pro ASIC plus – Design applications – Current FPGA technologies – FPAA architecture and its reconfiguration.

Practice: Finite state machine, Memories, FPGA implementation on fractional order

Module-4 –Synchronous FSM design	***12 Hours***
Choice of components to be considered – architecture centered around nonregistered PLDs – state machine designs – centered around a shift register, centered around a parallel loadable up/down counter – one hot design method – use of algorithmic state machine, application of one hot design to serial 2's complementer, parallel to serial adder/subtractor controller – system level design: controller, data path, and functional partition.	
Practice: Smart watch system using HDL, Traffic light controller using HDL, Washing machine controller using HDL	
Module-5 - Asynchronous state machine design	***12 Hours***
Features and need for asynchronous FSM's – lumped path delay models for asynchronous FSMs – excitation table, state diagrams, K-maps, and state tables – design of the basic cells by using the LPD model – design examples – hazards in asynchronous FSMs – one-hot design of asynchronous state machines – design of fundamental mode FSMs by using PLDs, Chiplet based SoC architecture design, Semiconductor 2D vs 3D packaging techniques, system level modeling using SystemC .	
Practice: Elevator design using HDL, SV - Vending machine design using HDL, SV - Micro oven controller using HDL, SV	

Learning Resources	1. *M.Morris Mano and Michael D.Ciletti, 'Digital Design', Pearson, 6th Edition, 2018* 2. *Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital integrated circuits: A design perspective". Second Edition, Prentice Hall of India, 2016.* 3. *Stephen M.Trimberger, Edr., "Field Programmable Gate Array Technology", Springer Science- Business media, LLC, 2012.* 4. *P.K.Chan & S.Mourad, "Digital Design using Field Programmable Gate Array", Pearson, 2009* 5. *Richard F.Tinder, "Engineering Digital Design, Revised second edition", Academic press, 2000.*	6. *Roger woods, John McAllister, Gaye Lightbody and Ying Yi, "FPGA- based implementation of signal processing systems", A John Wiley and Sons, Ltd., Publication, 2008.* 7. *John V. Oldfield, Richard C.Dorf, "Field Programmable Gate Arrays – Reconfigurable logic for rapid prototyping & implementation of digital systems", John Wiley & Sons, Reprint, 2008* 8. *Samir Palnitkar, "Verilog HDL: A guide to digital design and synthesis", Second Edition, Prentice Hall of India, 2003. Ramalingam. K. K, Steam tables, Sci.Tech Publishers, 2009*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3 (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	*5*	*5*	*5*	*5*	*5*	*5*	*5*	-
Level 2	Understand	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 3	Apply	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 4	Analyze	*15*	*15*	*15*	*15*	*15*	*15*	*15*	-
Level 5	Evaluate	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 6	Create	-	-	-	-	-	-	-	-
	Total	100%		100 %		100 %		100 %	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member* 2. *Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.*	*Dr. V.R. Venkatasubramani, Associate Professor, Department of ECE, Thiagarajar College of Engineering, Madurai.*	*Dr. K. Vaishnavi, Assistant Professor, Department of ECE, SRMIST, Tiruchirappalli.*

Course Code	21ECE578J	Course Name	Soft Computing	Course Category	E	Professional Elective	L	T	P	C
							2	0	2	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*explore the fundamental concepts of soft computing and neural networks*
CLR-2:	*discuss the concepts of fuzzy logic circuits and fuzzy inference systems*
CLR-3:	*explore the basics of genetic algorithm and its applications*
CLR-4:	*classify and illustrate various evolutionary optimization algorithms*
CLR-5:	*introduce methods for handling imprecise and uncertain data using rough sets,*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Bloom's Level***	***Programme Outcomes (PO)***			***Programme Specific Outcome (PSO)***
		K1-K6	***1***	***2***	***3***	***4***
CO-1:	*apply and illustrate soft computing and neural networks to manage data uncertainty*	K3	3	2	3	2
CO-2:	*analyze and design systems using fuzzy logic and fuzzy clustering*	K3	3	2	3	3
CO-3:	*design and develop optimization solutions using genetic algorithms for complex problems*	K4	3	2	3	3
CO-4:	*implement advanced optimization techniques for solving complex problems*	K4	3	2	3	3
CO-5:	*apply and integrate rough set theory for data analysis and clustering*	K4	3	2	3	2

Module-1: Introduction to Soft Computing and Neural Networks ***12 Hours***

Soft Computing Overview – Uncertainty in data, Hard vs Soft Computing, Introduction to Neural Networks, RBF Networks, Self-Organizing Map, Boltzmann Machines, Convolutional Neural Networks

Practice: *Multilayer Perceptron and Application, Implementation of Simple Neural Network (McCulloh-Pitts model), Implementation of Unsupervised Learning Algorithm*

Module-2: Fuzzy Systems and Fuzzy Logic ***12 Hours***

Introduction, Fuzzy Sets, Fuzzy Relations, and Membership functions, Properties of Membership functions, Fuzzification and Defuzzification, Fuzzy Rule based systems, Fuzzy Decision making, Fuzzy Classification, Fuzzy C-Means Clustering

Practice: *Introduction to fuzzy toolbox in MATLAB, Develop Fuzzy Decision-Making for Job Assignment Problem, Implement Fuzzy Inference System for healthcare systems*

Module-3: Genetic Algorithm	***12 Hours***
Difference between traditional algorithms and GA, basic operators, schema theorem, convergence analysis, stochastic models, applications in search and optimization. Encoding, Fitness Function, reproduction, cross over, mutation. Convergency Theory; Applications-Match word finding, Travelling salesman problem ***Practice:*** *Implementation of simple genetic algorithm, Implementation of genetic algorithm for routing in VLSI circuits, Implementation of travelling salesman problem using genetic algorithm,*	
Module-4: Optimization Techniques	***12 Hours***
Genetic Algorithm, Memetic Algorithms, Particle Swarm Optimization, Ant Colony Optimization, Frog-Leaping ***Practice:*** *Binary and Real Coded genetic Algorithms, Study of Derivative-free Optimization, compare different evolutionary algorithms for travelling salesman problem*	
Module-5: Rough Sets	***12 Hours***
Rough Sets – Definition, Upper and Lower Approximations, Boundary Region, Decision Tables, and Decision Algorithms. Properties of Rough Sets. Rough K-means clustering, Rough support, Vector clustering ***Practice:*** *Fault Diagnosis using rough set theory, Software safety analysis using rough sets, Develop a suitable method for Face Recognition System using rough sets*	

Learning Resources	*1. S.N. Sivanandham and S.N.Deepa, "Principles of Soft Computing", 2nd Edition, Wiley Publications.* *2. Simon Haykin "Neural Networks and Learning Machines" Prentice Hall, 2008* *3. Timothy Ross, "Fuzzy Logic with Engineering Applications", Third Edition, Wiley* *4. Samir Roy and Udit Chakraborty: Introduction to Soft Computing Neuro Fuzzy and Genetic Algorithms, 2013, 1st Edition, Dorling Kindersley Licensed by Pearson Education in South Asia*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3 (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	*5*	*5*	*5*	*5*	*5*	*5*	*5*	-
Level 2	Understand	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 3	Apply	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 4	Analyze	*15*	*15*	*15*	*15*	*15*	*15*	*15*	-
Level 5	Evaluate	*10*	*10*	*10*	*10*	*10*	*10*	*10*	-
Level 6	Create	-	-	-	-	-	-	-	-
	Total	100%		100 %		100 %		100 %	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.	*Dr. Dr. V.R. Venkatasubramani, Associate Professor, Department of ECE, Thiagarajar College of Engineering, venthiru@tce.edu.*	*Mr. S.Karthikeyan, Assistant Professor, Department of ECE, SRMIST Tiruchirappalli*
2. Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member		

Course Code	21ECE579T	Course Name	Algorithms for VLSI Design Automation	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		NIL	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*understand all the graph theory concepts required for physical design of a VLSI system IC*
CLR-2:	*learn the methods involved in partitioning and clustering of a design layout*
CLR-3:	*learn the representation used in Floor planning and Placement process*
CLR-4:	*describe the Routing algorithms and Timing Analysis*
CLR-5:	*gain knowledge of practical physical design issues on physical layout*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*analyze and apply algorithms for VLSI physical design challenges*	K3	3	2	3	2
CO-2:	*evaluate and implement partitioning and clustering algorithms in VLSI design*	K3	3	2	3	3
CO-3:	*design a compact IC using floor planning and placement methodologies*	K4	3	2	3	3
CO-4:	*analyze the routing process to achieve the performance of the digital design*	K4	3	2	3	3
CO-5:	*design performance aware VLSI layout*	K4	3	2	3	3

Module-1: Data Structures and Basic Algorithms ***9 Hours***

VLSI Physical design flow, Challenges in VLSI design flow, Basic Graph theory, Complexity analysis, Complexity issues, Analysis in NP hardness, Graph search algorithms, Spanning tree algorithms, Shortest path algorithms, Min- cut and max-cut algorithms, and, Steiner tree algorithms, Computational Geometry Algorithms: Line sweep, Extended line sweep, Basic Graph Structures: Atomic operations of Layout Editors, Basic Graph Structures: Linked list of blocks, Basic Graph Structures: Bin-based, and, Neighbor pointers, Corner Stitching: Introduction, Atomic operations using Corner stitching, Graph problems in Physical design

Module-2: Partitioning And Clustering ***9 Hours***

Introduction to Partitioning, Types of Partitioning, Metrics of Partitioning, Metrics of Clustering, Mathematical Partitioning Formulations, Introduction to Move-based partitioning algorithms, KL algorithm, Problems in KL algorithm, FM Algorithm, Problems in FM algorithm, Challenges in Clustering, Hierarchical Clustering, Agglomerative Clustering, Rajaraman and Wong algorithm, Introduction: Multi-level coarsening algorithm- Edge coarsening, Hyperedge coarsening, Modified Hyperedge coarsening, Practice problems in Clustering

Module-3: Floor planning And Placement	***9 Hours***
Introduction to Floor planning, Floor planning problem formulation and classification, Floorplan topologies, Metrics of Floor planning, Floorplan slicing methods, Algorithms for Slicing floorplan, Floorplan representation: Corner block list, Problems in Corner block list, Non-slicing methods: O-tree, Problems in O-tree, Non-slicing methods: B-tree, Problems in B-tree, Introduction to Placement, Problem formulation and classification, Top –down partition-based placement frame work, Enhancement of Min- cut placement, Placement algorithm using Simulated annealing, Placement algorithm using Genetic algorithm	
Module-4: Routing And Compaction	***9 Hours***
Global Routing, Problem Formulation, Classification of Global Routing, Maze routing algorithm, Lee's algorithm, Line Probe algorithms, Shortest Path algorithms: Steiner Tree based algorithms, Separability Based Algorithm, Detailed Routing: Problem formulation, Classification of Detailed routing, Single layer routing, Single row routing, Two-layer channel routing algorithms: Left, Edge algorithm Dogleg Routing algorithm, Clock routing schemes: H-tree based algorithm, Compaction: Classification and constraint- based compaction, Virtual grid-based compaction and recent trend in Compaction, 3/2 and 2D Compaction	
Module-5: Practical Design Issues	***9 Hours***
Elmore Delay based routing constructions, Examples on Elmore delay, Non-Hunan Interconnect synthesis, Optimization of Non-Hunan, Wire-sizing, Non-tree routing, Van Ginneken's algorithm, Optimization of Van Ginneken's algorithm, Two phase approach & buffer aware tree construction: C algorithm, Buffer aware tree generation, Buffered path with blockage avoidance: Dynamic programming approach, Buffered path with blockage avoidance: Graph-based approach, Buffered tree with blockage avoidance:, Tree adjustment & simultaneous tree and buffer insertion approach Buffered tree with blockage avoidance: Dynamic programming, Graph-based approach, Routabilty driven buffer planning, Noise aware buffer planning, Flip flop & buffer planning, Physical design in 3D circuits.	

Learning Resources	1. *Naveed Sherwani, Algorithms for VLSI physical design Automation, Kluwer Academic Publishers, 2010.* 2. *Sung Kyu Lim, "Practice Problems in VLSI physical design Automation",Springer, 2008* 3. *Charles J . Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, "Hand book of algorithms of Physical design Automation ", CRC press, 2009.* 4. *Sadiq M .Sait, Habib Youssef, "VLSI Physical design automation theory and Practice", World Scientific Publishing 1999*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Santosh Ramachandran, Verification, AI/ML d-Matix,Santa Clara, California.* 2. *Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member.*	*Dr. V.R. Venkatasubramani, Associate Professor of ECE, Thiagarajar College of Engineering, venthiru@tce.edu*	*Mr. V. Rajesh, Assistant Professor, Department of ECE, SRMIST, Tiruchirappalli*

Course Code	21ECE580T	Course Name	CAD Tools for VLSI	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*identify VLSI Design methodologies*
CLR-2:	*apply VLSI design automation tools*
CLR-3:	*analyze the concepts behind the VLSI design rules and routing techniques*
CLR-4:	*discuss strategies for Logical synthesis*
CLR-5:	*perform Hardware and Software Level optimization*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*demonstrate knowledge and understanding of fundamental concepts in CAD for VLSI*	K3	3	2	3	2
CO-2:	*identify and formulate design problems using graphs models for architecture representation*	K3	3	2	3	3
CO-3:	*determine the complexity of floor planning and routing using library binding algorithms*	K6	3	2	3	3
CO-4:	*analyze and implement various logic synthesis to optimize the gate-level net list*	K6	3	2	3	3
CO-5:	*design and transform hardware behavioral description into RTL model*	K6	3	2	3	2

Module-1: Introduction to VLSI Design Flow ***9 Hours***

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization

Practice: *Algorithmic Graph Theory in VLSI Design, Basics of VLSI Design Automation Tools, Combinatorial Optimization in VLSI Design*

Module-2: Layout, Placement and Partitioning	***9 Hours***
Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning ***Practice:*** *Constraint Graph Compaction Algorithms, Partitioning Techniques in VLSI Design, Design Flow Integration with Layout, Placement, and Partitioning*	
Module-3: Floor Planning and Routing	***9 Hours***
Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing ***Practice:*** *Local Routing Problems: Area and Channel Routing, Shape Functions and Floorplan Sizing, Design Flow Integration with Floor Planning and Routing*	
Module-4: Simulation and Logic Synthesis	***9 Hours***
Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis ***Practice:*** *Gate-Level Modeling and Simulation, Switch-Level Modeling and Simulation, Design Flow Integration with Simulation and Logic Synthesis*	
Module-5: High Level Synthesis	***9 Hours***
Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations ***Practice:*** *Hardware Models for High Level Synthesis, High-Level Transformations, Assignment Problem in High-Level Synthesis*	

Learning Resources	*1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.* *2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.* *3. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", World Scientific 1999.* *4. Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing 1987*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California. *2. Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member*	*Dr. V.R. Venkatasubramani, Associate Professor of ECE, Thiagarajar College of Engineering, venthiru@tce.edu*	*Mr. S.Karthikeyan, Assistant Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	$21ECE581T	Course Name	Testing of VLSI Circuits	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1:	provide the fundamental concepts of testing methods to find faults
CLR-2:	utilize fault simulation logic and their applications
CLR-3:	familiarize the evaluation of properties of pure substances and vapor power cycles
CLR-4:	discover the fundamental concepts of ATPG for built-in-self test
CLR-5:	utilize the properties of boundary core standard for testability techniques

Course Outcomes (CO):	At the end of this course, learners will be able to:	Blooms Level	Programme Outcomes (PO)			Programme Specific Outcome (PSO)
		K1-K6	1	2	3	1
CO-1:	design and simulate the fault models	K2	2	2	3	2
CO-2:	apply fault simulation algorithms for circuit under test	K3	2	3	3	2
CO-3:	design test pattern generation circuits for combinational and sequential circuits	K4	3	3	3	3
CO-4:	design built-in-self test for circuit under test	K4	2	3	3	3
CO-5:	analyze the testability techniques for embedded core design	K4	2	3	3	2

Module-1 – Introduction to testing **9 Hours**

Importance of testing- testing during the VLSI life cycle- challenges and levels of abstraction in VLSI testing – VLSI technology trends affecting testing – types of testing. Fault models – defects, errors, faults – Stuck-at faults- fault equivalence, fault collapsing, fault dominance- transistor faults, open and short faults, delay faults, pattern sensitivity and coupling faults, analog fault models- automatic test equipment, UVM methodology, Portable Test and Stimulus Standard (PSS).

Module-2 – Logic and fault simulation **9 Hours**

SCOAP testability analysis – algorithms for true value simulation – compiled-code simulation, event-driven simulation – algorithm for fault simulation – serial fault simulation, parallel fault simulation, deductive fault simulation – concurrent fault simulation Roths TEST-DETECT algorithm

Module-3 – ATPG for combinational and sequential circuits	***9 Hours***
Combinational circuit*: Algorithms and representations, redundancy identification (RID), combinational ATPG algorithms – D- Calculus and D-Algorithm, PODEM and FAN* ***Sequential circuit:*** *ATPG for single-clock synchronous circuits, time-frame expansion method, simulation-based sequential circuit ATPG- CONTEST algorithm, genetic algorithm*	
Module-4 –DFT methods and built-in-self-test	***9 Hours***
DFT methods – Ad Hoc approach, structural approach – scan cell designs – scan architectures – scan design rules – scan design flow, BIST – design rules – test pattern generation – output response analysis – logic BIST architectures – fault coverage enhancement – BIST timing control – logic BIST system design – a design practice – memory MIST	
Module-5 – Boundary scan standard and core-based testing	***9 Hours***
Features Core-based design and test considerations – digital boundary scan – IEEE Std. 1149.1 – test architecture and operations, test access port and bus protocol, data registers and boundary – scan cells, TAP controller – embedded core test standard (IEEE Std. 1500) – architecture, wrapper components and functions – comparisons between 1500 and 1149.1 standards.	

Learning Resources	1. *M.L. Bushnell, V. D. Agarwal, "Essential of electronic testing for digital memory and mixed signal VLSI circuits- Kluwer academic publishers, reprint 2013.* 2. *L.T. Wang, C.W. Wu and X.Wen, VLSI test principles and architectures, Elsevier, 2006.* 3. *Alexander Digital Miczo,"Logic testing and simulation", second edition, A john wiley&sonsINC. Publication,2003.*	4. *Alfred Crouch, "Design for test for digital IC & embedded core systems", prentice hall, 2002.* 5. *Samiha Mourad, Yervant Zorian, " Principles of testing electronic systems" A Wiley interscience publications, 2002.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*	-	*15%*	-	*5%*	-
Level 2	*Understand*	*10%*	-	*15%*	-	*10%*	-
Level 3	*Apply*	*10%*	-	*30%*	-	*10%*	-
Level 4	*Analyze*	*15%*	-	*30%*	-	*15%*	-
Level 5	*Evaluate*	*10%*	-	*10%*	-	*10%*	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member* 2. *Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.*	*Dr. V.R. Venkatasubramani, Associate Professor, Department of ECE, Thiagarajar College of Engineering*	*Dr. K. Vaishnavi, Assistant Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	21ECE582T	Course Name	Hardware - Software Co-Design of Embedded System	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	provide in depth knowledge on Hardware/Software Co-Design.
CLR-2:	familiarize advanced analytical data flow implementation in software and hardware systems.
CLR-3:	discover detailed awareness on fundamental building blocks using hardware/software co-design concepts
CLR-4:	present complete information on modern hardware/software tools for building prototypes of embedded systems with their characterization.
CLR-5:	acquire detailed understanding on the design considerations of the various processors for different applications.

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	analyze the key concepts in hardware/software co-design	4	2	3	3	2
CO-2:	analyze the data flow implementation in software and hardware	4	2	3	3	3
CO-3:	design the fundamental building blocks using hardware/software co-design and related implementation	4	3	3	3	3
CO-4:	design and analyze with modern hardware/software tools for building prototypes of embedded systems	4	2	3	3	3
CO-5:	analyze the various processors	4	2	3	3	3

Module-1 NATURE OF HARDWARE AND SOFTWARE ***9 Hour***

Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph –Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow graph – control flow modeling – Adding time and resources – Transformations.

Module-2 DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE ***9 Hour***

Software Implementation of Data Flow – Converting queues and actors into software, Dynamic Scheduler – Hardware Implementation of Data Flow – single rate SDF graphs into hardware, Pipelining – Analysis of control flow and data flow – construction of control and data flow graph – Translating C into hardware – Designing data path and controller

Module-3 DESIGN SPACE OF CUSTOM ARCHITECTURES	***9 Hour***
Finite state machines with data path – FSMD design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture	
Module-4 HARDWARE / SOFTWARE INTERFACES	***9 Hour***
Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardware interface – Data and control design, programmer's model.	
Module-5 APPLICATIONS	***9 Hour***
Zynq processor-centric platforms-Scalable Processor Architecture, Trivium for 8-bit platforms – AES coprocessor, CORDIC coprocessor – algorithm and implementation.	

Learning Resources	*1. Patrick Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2ndEdition, Springer, 2014.* *2. Louise H. Crockett, "Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC" Strathclyde Academic Media,2014* *3. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice" ,Kluwer Academic Pub, 2013*	*4. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 2010.* *5. Giovanni De Micheli, Rolf Ernst Morgon," Reading in Hardware/Software Co-Design "Kaufmann Publishers, 2002.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*	-	*15%*	-	*5%*	-
Level 2	*Understand*	*10%*	-	*15%*	-	*10%*	-
Level 3	*Apply*	*10%*	-	*30%*	-	*10%*	-
Level 4	*Analyze*	*15%*	-	*30%*	-	*15%*	-
Level 5	*Evaluate*	*10%*	-	*10%*	-	*10%*	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member	*Dr. Noor Mahammad, Associate Professor, Department of CSE, IIITDM, Kancheepuram, Chennai*	*Dr. Anandpushparaj. J Assistant Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	21ECE583T	Course Name	Computer Aided Design Automation	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*analyze and apply control theory fundamentals for system stability*
CLR-2:	*apply electronic fundamentals to design microcomputer-based control systems effectively*
CLR-3:	*apply sensor and actuator principles for automotive engine control systems*
CLR-4:	*implement digital control strategies for efficient powertrain management systems*
CLR-5:	*apply advanced instrumentation and telematics for automotive diagnostics and navigation*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*analyze with the fundamentals of electronic components related to automotive applications*	K3	3	1	3	2
CO-2:	*design automotive sensors, actuators and instrumentations*	K3	3	2	3	3
CO-3:	*analyze the control mechanisms in an automotive system*	K4	3	2	3	3
CO-4:	*analyze the operations of telematics and diagnostic methods*	K4	3	1	3	3
CO-5:	*to be able to understand the complete automotive operation and control mechanisms*	K4	3	2	3	2

Module-1 - Systems Approach to Control and Instrumentation ***9 Hour***

System, Linear system theory, Steady-State sinusoidal frequency response of a system, State variable formulation of models, Control theory, Stability of Control System, Closed-Loop Limit Cycle Control, Instrumentation, Basic Measurement System, Filtering, Digital Subsystem, Sinusoidal Frequency Response, Discrete Time Control System, Closed loop control, Example Discrete Time

Module-2: Fundamentals of Electronics, Microcomputer Instrumentation and Control ***9 Hours***

Semiconductor Devices, Transistors, ICs, Operational Amplifiers, Use of Feedback in Op Amps, Phase-Locked Loop, Digital Circuits, Logic Circuits (Combination and Sequential Circuits), Timers and Counters, Microcomputer fundamentals, Tasks and Operations, CPU Registers, Reading Instructions, Programming Languages, Microcomputer Hardware, Microcomputer Applications in, Automotive Systems, Instrumentation Applications of Microcomputers, Microcomputers in Control Systems

Module-3: Sensors, Actuators and Electronic Engine Control ***9 Hours*** *Motivation for Electronic Engine Control, Exhaust Emissions, Fuel Economy, Test Procedures, Concept of an Electronic Engine Control System, Engine Performance Terms, Exhaust Catalytic, Convertors, Electronic Fuel-Control System, Analysis of Intake Manifold Pressure, Idle Speed Control, Electronic Ignition, Automotive Control System Applications of Sensors and Actuators,, Throttle Angle Sensor, Temperature Sensor, Coolant Sensor, Sensors for Feedback control, Knock Sensors, Automotive Engine Control Actuators, Variable Valve Timing, Electric Motor, Actuators, Ignition System.*
Module-4: Motion and Digital Powertrain Control System ***9 Hours*** *Digital Engine Control, Features, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine, Control System, Summary of Control Modes, Cruise Control System, Cruise Control Electronics, Antilocking Braking System, Electronic Suspension System, Electronic Steering Control, Four-, Wheel Steering*
Module-5: Automotive Instrumentation, Telematics and its Diagnostics ***9 Hours*** *Modern Automotive Instrumentation, Input and Output Signal Generation, Advantages of Computer Based Instrumentation, Display Devices, Flat Panel Display, Fuel Quantity Measurement, Coolant Temperature Measurement, Oil Pressure Measurement, Vehicle Speed Measurement, High- Speed Digital Communication (CAN BUS), Telematics, GPS Navigation, GPS System Structure, Automotive Diagnostics*

Learning Resources	*1. Al. Santini ,"Automotive Electricity and Electronics",Second Edition, Delmar Cengage Learning, 2013.* *2. William B. Ribbens, "Understanding Automotive Electronics- An Engineering Prespective", 7th Edition, Butterworth-Heinemann Publications, 2012.* *3. Robert Bosch," Automotive Hand Book", SAE, 5TH Edition,2000.* *4. Young A.P. & Griffiths, " Automotive Electrical Equipment" , ELBS & New Press,1999.* *5. Bechhold, " Understanding Automotive Electronic", SAE,1998.* *6. Tom Weather Jr. &Cland c. Ilunter, " Automotive computers and control system", Prentice Hall Inc., New Jersey,1984* *7. Crouse W.H., " Automobile Electrical Equipment" , McGraw Hill Co. Inc., New York ,1995*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California. *2. Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member.*	*Dr. V.R. Venkatasubramani, Associate Professor, Department of ECE, Thiagarajar College of Engineering, Madurai. venthiru@tce.edu*	*Mr. V. Rajesh, Assistant Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	21ECE584T	Course Name	Design Of Embedded Control System	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		NIL	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*apply control system design for embedded applications*
CLR-2:	*utilize the Automotive Sensors, Actuators and Instrumentations*
CLR-3:	*design optimal embedded models and learn the uncertainties*
CLR-4:	*utilize the operations of Telematics and Diagnostic methods*
CLR-5:	*apply the basic controllers design and implementation*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*4*
CO-1:	*apply the design of embedded systems with CAN and RTOS integration*	K3	3	2	3	2
CO-2:	*design linear and nonlinear control system models for embedded applications*	K3	3	2	3	3
CO-3:	*validate time domain and frequency domain systems and reduce uncertainties in system design*	K4	3	1	3	3
CO-4:	*design various control elements by understanding pole-zero placement and able to design PID controllers*	K4	3	2	3	3
CO-5:	*apply robust control principles for embedded systems and safety assurance*	K4	3	2	3	3

Module-1: Embedded Systems – Basic Concepts ***9 Hours***

Introduction to Embedded Systems, Architecture, Embedded system model, The Electric Power Level, The Signal Processing Level, Communication Networks in, Embedded Systems, Communication Networks in, Embedded Systems, Introduction to Control Area Networks (CAN), CAN Message Frames, Error Detection and Signaling, CAN Controller Modes, CAN Implementations, Multi-tasking Embedded Control Systems, Introduction to RTOS, RTOS Planning Embedded System and Development

Module-2: Embedded Control System Design ***9 Hours***

Requirements for Control System, Design Safety Requirements, Identification of the System to Be Controlled, Control Device Specification, Control Device Design, Installation and Maintenance, Mathematical Models for Control, Models from Science, Models from Experimental Data, Linearization of Nonlinear Models, Control System's Characteristics, Disturbance Attenuation,, Tracking, Sensitivity to Parameter Variations, Control System's Limitation, Stability and Relative Stability, Performance Specifications for Linear Systems

Module-3: System Identification and Model- Order Reduction ***9 Hours***
Model Building and Model Structures, Model Structures, Input Signal Design for System, Identification Experiments, Requirements Imposed on the Input Signal, Input Signal Design, Model Validation in Time Domain, Model Validation in Frequency Domain, Model-Order Reduction Methods, Nominal Plant and Plant Uncertainties, Multiplicative Uncertainty Model, Additive Uncertainty Model, Additive Uncertainty Model, Practical Examples – System Identification, Brushless d.c. Drive's Identification, Identification of a Fuel Cell
Module-4: Classical Controller Design ***9 Hours***
Controller Design Based on Pole- Zero Cancellation, The Influence of Controller Zero Controller Design for Deadbeat Response, Controller Design Using the Root, Locus Technique, Phase-Lead Controller Design Using the Root Locus, Phase-Lag Controller Design Using the Root Locus, PID Controller Design, Ziegler-Nichols Tuning Formula, Chien-Hrones-Reswick Tuning Formula, The Coefficient Diagram Method, Validation of the Control System,, Representative Sample and Sample Size, Monte Carlo Simulation, Controller Design for Systems withTime Delays, Systems with Time Delays – Smith Predictor, The Coefficient Diagram Method (CDM) for Systems with Time Delays, Handling Jitter in Networked Control System, Controller Design for Disturbance Rejection, Disturbance Observers, Two-Degree-of-Freedom Control Systems (2DOF), Control System Design Verification and Validation
Module-5: Fundamentals of Robust Control and Embedded Safety ***9 Hours***
Norms for Signals and Systems, Internal Stability, Unstructured Plant Uncertainties, Robust Stability for Different, Uncertainty Models, Performance and Robustness Bounds, Design for Robust Performance, Performance Weighting Function, Design for Tracking Control, Performance Weighting Function, Design for Disturbance Rejection, Robust Controller Synthesis Problem, Controller Design, Using Youla Parametrization, Controller Design Using Robust, Control Toolbox, Controller Design with Constraint on the Control Signal, Robust Gain-Scheduled Control, Control Algorithm, Implementation in Real-Time Embedded Safety Loop Development, Risk Assessment and Safety Levels, Classification of Faults, Calculation of Probability of Failure on Demand

Learning Resources	*1. A.Forrai, "Embedded control system design- A model based approach," Springer- Verlag, 2013* *2. Marian Andrzej Adamski,AndreiKaratkevich,MarekWegrzyn, "Embedded Control systems," Springer Science, 2006*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California. *2. Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member.*	*Dr. V.R. Venkatasubramani, Associate Professor, Department of ECE, Thiagarajar College of Engineering, Madurai, venthiru@tce.edu*	*Mr. V. Rajesh, Assistant Professor, Department of ECE, SRMIST Tiruchirappalli.*

Course Code	21ECE670T	Course Name	VLSI for Wireless Communications	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*illustrate the fundamental principles of wireless communication systems, modulation schemes, and channel characteristics.*
CLR-2:	*explore the design and implementation of VLSI architectures for transmitters and receivers.*
CLR-3:	*investigate the design and performance of CMOS mixers.*
CLR-4:	*examine the principles and VLSI implementation of analog-to-digital converters.*
CLR-5:	*analyze the design and functionality of CMOS-based frequency synthesizers.*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*apply the VLSI concepts in wireless communication techniques.*	K3	2	3	3	2
CO-2:	*design and analyze the LNA and Mixers.*	K4	2	3	3	3
CO-3:	*design and analyze PLL for real time applications.*	K4	3	3	3	3
CO-4:	*analyze the characteristics of receivers and frequency synthesizers.*	K4	1	3	3	3
CO-5:	*design and analyze A/D converters.*	K4	1	3	3	2

Module-1: COMMUNICATION CONCEPTS ***9 Hours***

Introduction, Overview of Wireless systems, Standards, Access Methods, Modulation schemes, Classical channel, Wireless channel description, Path loss, Multipath fading.

Module-2: TRANSMITTER AND RECEIVER ARCHITECTURES ***9 Hours***

VLSI Model for Transmitter back end design, Quadrature LO generator, VLSI Model for Receiver front end, Filter design, Non, idealities, Design parameters, Noise figure & Input intercept point. CMOS LNA Introduction, Wideband LNA design. Narrow band LNA design: Impedance matching & Core amplifier.

Module-3: CMOS MIXERS	***9 Hours***
CMOS Active Mixer: Balancing Mixer, Qualitative Description of the Gilbert Mixer, Conversion Gain, Distortion, Noise, A Complete Active Mixer. CMOS Passive Mixer: Switching Mixer, Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer, A Practical Unbalanced Switching Mixer. Sampling Mixer: Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.	
Module-4: ANALOG TO DIGITAL CONVERTERS	***9 Hours***
VLSI implementation: Demodulators, A/D converters used in receivers, Low-pass and bandpass sigma delta modulators and its implementation-I/Q mismatch in converters	
Module-5: FREQUENCY SYNTHESIZERS	***9 Hours***
CMOS based PLL, Phase detector, Dividers, Voltage Controlled Oscillators, LC oscillators, Ring Oscillators, Phase noise, Loop filters & design approaches, A complete synthesizer design	

Learning Resources	*1. BehzadRazavi, "Design of Analog CMOS Integrated Circuits" ,2nd Edition, McGraw-Hill, 2017.* *2. Bosco H Leung "VLSI for Wireless Communication", Second Edition, Springer, 2014.* *3. B.Razavi ,"RF Microelectronics" , Pearson ,2013.* *4. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 2013.* *5. Rappaport,T.S., "Wireless communications", Pearson Education, 3rd Edition, 2010.* *6. Thomas H.Lee, "The Design of CMOS Radio – Frequency Integrated Circuits", Cambridge University Press ,2004.* *7. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI wireless design – Circuits & Systems", Kluwer Academic Publishers, 2000.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*		*20%*		*20%*	
Level 2	*Understand*	*20%*		*20%*		*20%*	
Level 3	*Apply*	*30%*		*30%*		*30%*	
Level 4	*Analyze*	*30%*		*30%*		*30%*	
Level 5	*Evaluate*	-		-		-	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. Dr. Saravanan Mohan, Principal researcher, Ericsson, India *2. Venkat Sunkara, Founder & CEO, ChipEdge Technologies Pvt Ltd, Bengaluru.*	*Dr. Noor Mahammad, Associate Professor, Department of CSE, IIITDM, Kancheepuram, Chennai.*	*Dr.K.Visvaksenan, Professor, Department of ECE, SRMIST, Tiruchirappalli.*

Course Code	21ECE671T	Course Name	Machine Learning for VLSI	Course Category	E	Professional Elective	L	T	P	C
							2	0	2	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*provide concise introduction to the fundamental concepts of Machine Learning*
CLR-2:	*introduce neural networks and its algorithm*
CLR-3:	*focus on the backend design challenges, including mask synthesis and physical verification*
CLR-4:	*study how machine learning can help in physical design*
CLR-5:	*address the energy efficient design of machine learning hardware*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*4*
CO-1:	*analyze and implement supervised and unsupervised machine learning*	K3	3	1	3	2
CO-2:	*develop and explore the applications of neural network algorithms*	K3	3	2	3	3
CO-3:	*apply and demonstrate the machine learning in physical verification and mask synthesis*	K4	3	2	3	3
CO-4:	*apply machine learning to optimize VLSI design and physical verification*	K4	3	2	3	3
CO-5:	*analyze and classify the energy efficient machine learning hardware structures.*	K4	3	2	3	2

Module-1: Introduction to Machine Learning ***12 Hours***

Introduction, Basic Definitions, Types of Learning, Supervised learning: Classification and, Unsupervised Learning: Clustering, Density Estimation, Reinforcement learning, Hypothesis Space, Inductive Bias, Evaluation, Cross-Validation, Linear Regression, Types of Regression Models, Tutorial on supervised vs unsupervised learning, Tutorial on regression, Decision Tree, Example for Decision Tree

Practice: *Supervised Learning - Classification with Decision Trees, Unsupervised Learning - Clustering with K-means, Regression Analysis - Linear Regression*

Module-2: Neural Network, Computational Learning Theory and Clustering ***12 Hours***

Neural Network Introduction, Perceptron, Limitations of Perceptron, Multilayer Neural Network, Back Propagation Algorithm : Learning in epochs stopping, Deep Neural Networks, Training of neural networks, Introduction to computational learning theory, Sample Complexity, Finite hypothesis space, Infinite hypothesis space, Ensemble Learning : Classification, Ensemble Creation and combining, Approaches, Bootstrap Method, Bagging: Bootstrap Aggregation Regression, Boosting: Adaptive Boosting (AdaBoost) Algorithms, Gradient Boosting Algorithms

Practice: *Implementing and Training a Multilayer Neural Network, Ensemble Learning with Bagging and Boosting, Implementing Finite & Infinite hypothesis*

Module-3: Machine Learning in Physical Verification and Mask Synthesis ***12 Hours***

Machine Learning Taxonomy, VLSI CAD Abstraction Levels, ML in Physical Verification, Layout Feature Extraction and Hotspot Detection, ML in Mask Synthesis, Sub-resolution Assist Features, Optical Proximity Correction (OPC), Machine Learning guided OPC, Machine Learning for Clock Optimization, Decision tree induction algorithm, Importance of Lithographic Patterning, Process Representation of Lithographic Patterning, Process Machine Learning for Lithography, Friendly Routing, Image Translation for Lithography,: Bottleneck in Semiconductor, Mask Verification: Bottleneck in IC Manufacturing

Practice: *Hotspot Detection using Machine Learning, Clock Optimization using Machine Learning, Image Translation for Lithography using Deep Learning*
Module-4: Machine Learning Applications in IC Physical Design ***12 Hours*** *Machine Learning for Physical Design: Modern VLSI Layouts, IC Design Flow –Silicon Compiler, Placement and Routing Example: Correlation between Placement and Routing, Challenges for VLSI Design, Datapath Placement: Machine Learning for Placement, Routing, Mask Synthesis and Verification, VLSI Placement and Algorithm, Advances in Deep Learning, Hardware/Software Analogy between NN Training and Placement, DREAM Place Architecture, DREAM Place Architecture flow, MAGICAL Overview, Routing Guidance: Genius Route, Routability - Driven Placement, SRAF Insertion SRAF Image Translation, Challenges for SRAF Insertion* ***Practice:*** *Machine Learning for Placement in VLSI Design, Routing Optimization using Machine Learning, SRAF Insertion using Machine Learning*
Module-5: Energy Efficient Design of Advanced Machine Learning Hardware ***12 Hours*** *Software and Co-design Optimizations, Pruning in Optimization, Weight Sharing, Compact Network Architectures, Hardware–Software Co-design in neural networks, Hardware-Level Techniques, Dataflows for Accelerators, Architectures for Accelerators, Deep CNN Accelerators, Hardware Friendly Strategies for Deep CNN Accelerators, Memory-Efficient Architectures, Hardware Architectural Techniques for Leveraging Sparsity in Neural Networks, Error Resilience Analysis, Energy-Efficient Hardware Accelerator, Design Methodology for Neural Networks, Deep Neural Networks (DNN): Training and model compression, Efficient Machine Learning Architectures: Challenges and the Way Forward Optimizing Memory vs. Computations, Neuromorphic Computing* ***Practice:*** *Pruning and Optimization in Neural Networks, Designing Memory-Efficient Architectures for Deep CNNs, Neuromorphic Computing for Energy-Efficient Machine Learning*

Learning Resources	1. *Lorenzo Rosasco, (2017), Introductory Machine Learning Notes.* 2. *Ethem Alpaydin, Introduction to Machine Learning, Second Edition.* 3. *Ibrahim (Abe) M. Elfadel, Duane S. Boning and Xin Li (2019), Machine Learning in VLSI Computer Aided Design.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. *Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.* 2. *Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member.*	*Dr. V.R. Venkatasubramani, Associate Professor, Department of ECE, Thiagarajar College of Engineering, venthiru@tce.edu*	*Mr. V. Rajesh, Assistant Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	21ECE672T	Course Name	CMOS Analog IC Design	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1:	apply the fundamental concepts of amplifiers
CLR-2:	illustrate different types of mirrors and its applications
CLR-3:	analyze the evaluation of properties of multistage amplifiers
CLR-4:	articulate the fundamental concepts of multistage frequency response
CLR-5:	utilize the evaluation of properties of feedback amplifiers

Course Outcomes (CO):	At the end of this course, learners will be able to:	Blooms Level	Programme Outcomes (PO)			Programme Specific Outcome (PSO)
		K1-K6	1	2	3	4
CO-1:	design CMOS analog IC building blocks	K2	2	2	3	2
CO-2:	apply the various current mirror biasing circuits	K4	2	3	3	3
CO-3:	design various single and multistage differential amplifier architectures	K4	3	3	3	3
CO-4:	Analyze the frequency response of single and multi-stage differential amplifiers	K4	2	3	3	3
CO-5:	Illustrate the design of various feedback amplifiers with compensation	K4	2	3	3	2

Module-1 – Single state amplifiers	**9 Hours**
Review of MOS physics and equivalent circuits and models. Large and small signal analysis CS, CG and source follower, miller effect, frequency response of CS, CG and source follower, inverters, single stage differential amplifiers, CMOS Op Amps, open-loop comparators, data converters.	
Module-2 – Current mirrors	**9 Hours**
Current sources, basic current mirrors, current steering circuits, cascade stages for current mirrors, Wilson current mirror, Wilson current mirror large and small signal analysis of current mirrors	
Module-3 – Multistage differential amplifiers	**9 Hours**
Differential amplifier, large and small signal analysis of the balanced differential amplifier, device mismatches in differential amplifier, small and large signal analysis of the differential pair with current mirror load, $PSRR^+$, $PSRR^-$ and CMRR of differential amplifiers, small signal analysis of telescopic amplifier, two-stage amplifier and folded cascaded amplifier.	

Module-4 – Frequency response of multistage differential amplifiers	***9 Hours***
DFT Frequency response of differential amplifier- transfer function method, miller method, dominant-pole approximation, upper cutoff frequency-zero-value time constant method, UGF- short circuit time constant method, frequency response of telescopic cascaded, folded cascaded and two-stage amplifiers.	
Module-5 – Stability and frequency compensation of feedback amplifiers	***9 Hours***
Features Properties and types of negative feedback circuits, feedback configurations, effect of loading in feedback networks, feedback circuit analysis using return ratio modelling input and output port in feedback network, the relation between gain and bandwidth in feedback amplifiers, phase margin, frequency compensation, compensation of two stage MOS amplifiers.	

Learning Resources	1. *Behzad Razave, "Design of analog CMOS integrated circuits", 2nd edition, Tata McGraw Hill,2017.* 2. *Gray, Hurst, Lewis, Meyar, "Analysis and design of analog integrated circuits" Fifth Edition John Wiley, 2016.* 3. *Phillip E.Allen, Douglas R.Holber, "CMOS analog circuit design", Third edition, Oxford university press, 2011.*	4. *Jacob Baker "CMOS: circuit design, layout, and simulation, third edition", Wiley IEEE press 2010.* 5. *Kenneth William Martin, David johns, "Analog integrated circuit design", Wiley India, 2008.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	***Experts from Higher Technical Institutions***	***Internal Experts***
1. *Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.* 2. *Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member*	*Dr. V.R. Venkatasubramani, Assistant Professor, Department of ECE, Thiagarajar College of Engineering, Madurai.*	*Dr. K. Vaishnavi, Assistant Professor, Department of ECE, SRMIST, Tiruchirappalli.*

Course Code	$21ECE673T	Course Name	Robotics And Control	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*illustrate the fundamentals, evolution and applications of robotics.*
CLR-2:	*learn to model and analyze the motion of robots.*
CLR-3:	*comprehend the behavior of robotic systems and examine different control methods for robotic movement.*
CLR-4:	*design the different types of sensors used in robotics, principles of robotic perception and sensor fusion.*
CLR-5:	*investigate the integration of artificial intelligence in robotics.*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*4*
CO-1:	*discuss the basic principles and concepts of robotics.*	K2	2	3	3	2
CO-2:	*model and analyze the kinematic structure of robotic systems.*	K4	2	3	3	3
CO-3:	*develop motion planning and control algorithms for robotic applications.*	K3	3	3	3	3
CO-4:	*implement principles of robotic perception to process sensory data.*	K3	1	3	3	3
CO-5:	*apply AI techniques to enhance robotic capabilities and develop systems for effective human-robot interaction.*	K3	1	3	3	2

Module-1: Introduction to Robotics	***9 Hours***
Overview of Robotics: Definition and scope of robotics, Historical development and evolution of robots, Classification of robots. Components of a Robotic System: Mechanical structures, Actuators and sensors, Control systems and processors. Applications of Robotics: Industrial robots, Service robots, Medical and healthcare robots.	
Module-2: Kinematics of Robots	***9 Hours***

Introduction to Kinematics: Types of joints and links, Degrees of freedom, Kinematic chains and diagrams. Forward Kinematics: Denavit-Hartenberg (D-H) parameters, Transformation matrices, Position and orientation of end-effectors. Inverse Kinematics: Solving inverse kinematics equations, Analytical and numerical methods, Kinematic redundancy.
Module-3: Dynamics and Control of Robots ***9 Hours***
Introduction to Dynamics: Newton-Euler formulation, Lagrangian mechanics, Equations of motion for robots. Robot Control Systems: PID control, Model-based control, Adaptive and robust control. Motion Planning and Control: Trajectory generation, Path planning algorithms, Feedback control for trajectory tracking.
Module-4: Sensors and Perceptions ***9 Hours***
Introduction to Robotic Sensors: Types of sensors (position, velocity, force, and vision), Sensor characteristics & specifications, Sensor integration in robots. Perception in Robotics: Image processing & computer vision, Object recognition and tracking, Environmental mapping & localization. Sensor Fusion: Principles of sensor fusion, Kalman filter & particle filter, Applications of sensor fusion in robotics.
Module-5: Trends and challenges ***9 Hours***
Artificial Intelligence in Robotics: Machine learning and deep learning for robotics, Reinforcement learning in robotic control, AI-based planning and decision-making. Human-Robot Interaction, Principles of human-robot interaction (HRI), Haptic interfaces and teleoperation, Collaborative robots (cobots), Swarm robotics, Soft robotics, Ethical and societal implications of robotics.

Learning Resources	1. *Mark W. Spong, Seth Hutchinson, and M. Vidyasagar, "Robot Modeling and Control", John Wiley and Sons, 2020.* 2. *Craig, John J, "Introduction to Robotics: Mechanics and Control", Pearson, 2013.* 3. *K. S. Fu, R.C. Gonzalez, C.S.G. Lee," Robotics: Control, Sensing, Vision, and Intelligence", Mcgraw-Hill Book Company, 1987.* 4. *Mikell P. Groover, "Industrial Robotics Technology Programming and publications",McGraw Hill Co., New Delhi, 2012.* 5. *Padhy N. P, "Artificial Intelligence and Intelligent Systems", Oxford University Press, 2005*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*		*20%*		*20%*	
Level 2	*Understand*	*20%*		*20%*		*20%*	
Level 3	*Apply*	*30%*		*30%*		*30%*	
Level 4	*Analyze*	*30%*		*30%*		*30%*	
Level 5	*Evaluate*	-		-		-	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. *Kaarthick Balakrishnan, Research Director, ANCIT Automotive Electronics Consultant, Coimbatore.* 2. *Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.*	*Dr. Noor Mahammad, Associate Professor, Department of CSE, IIITDM, Kancheepuram, Chennai.*	*Dr. S. Amuthameena, Assistant Professor, Department of EEE, SRMIST Tiruchirappalli*

Course Code	$21ECE674T	Course Name	Medical Electronics And Instrumentation	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co- requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1:	comprehend the components of medical instruments and various types of electrodes utilized
CLR-2:	acquire knowledge of the diverse biopotential characteristics and recording techniques employed for different biosignals
CLR-3:	analyze the non-electrical parameter measurements to facilitate recording various physiological parameters
CLR-4:	familiarize oneself with the methods employed for measuring blood flow
CLR-5:	explore the measurement techniques utilized for assessing biochemical parameters

Course Outcomes (CO):	At the end of this course, learners will be able to:	Blooms Level	Programme Outcomes (PO)			Programme Specific Outcomes (PSO)
		K1-K6	1	2	3	1
CO-1:	analyze the principles governing biopotentials and diverse bioelectrode types	K4	2	3	3	2
CO-2:	apply different bio-potential characteristics and recording methods	K4	2	3	3	3
CO-3:	develop measurement systems for non-electrical parameters measurements	K3	2	3	3	3
CO-4:	evaluate different techniques for measuring cardiac output	K4	2	3	3	3
CO-5:	analyze the principles and applications of various biochemical measurement techniques	K4	2	3	3	2

Module-1 - Fundamentals of Bioelectrodes and Biopotentials **9 Hours**

Components of Medical Instrumentation – Origin of Bio-potential: Action Potential - Electrode-electrolyte interface, Half-cell potential, Polarizable and Non-polarizable electrodes - Skin electrode interface – Bio-electrodes: Surface-, Micro-, and Needle electrodes - Equivalent circuits of electrodes – Biochemical and Transcutaneous electrodes: pH, pO2, pCO2

Module-2 - Biopotential Amplification and Signal Recording **9 Hours**

Bioamplifiers- Carrier Amplifier, - Isolation Amplifier - Differential amplifier - Chopper Amplifier - Instrumentation Amplifier - Bioelectric signals (ECG, EMG, EEG, EOG & ERG) and their characteristics - Electrodes for ECG, EEG and EMG - ECG Machine - EMG machine – 10-20 electrodes placement system for EEG - EEG machine - Heart sound and characteristics, PCG

Module-3 - Measurement of Physiological Parameters **9 Hours**

Measurement of Blood pressure – Direct Methods and Indirect Methods - Temperature – Respiration rate - Heart rate measurement - O2 , CO2 measurements, Respiratory volume measurement, BMR Measurement, Plethysmography technique, Detection of various physiological parameters using impedance technique.

Module-4 - Blood Flow Measurement and Cell Counting Techniques	***9 Hours***
Cardiac output Measuring techniques – Dye Dilution method, Thermo dilution method, BP method - Blood Flow measuring Techniques: Electromagnetic Type - Ultrasound Blood Flow meter, Automatic Counting of RBC, WBC and Platelets.	
Module-5 - Biochemical Measurement Techniques	***9 Hours***
Chemical Fibro sensors, Fluorescence sensors - Glucose Sensor - Colorimeter, Spectro photometer, Flame photometer – Chromatography - Mass Spectrometer , auto analyser.	

Learning Resources	1. *Joseph J Carr and John m Brown – Introduction to Biomedical equipment Technology- Pearson Education 4th edition New Delhi 2001* 2. *Leslie Cromwell, Fred J. Weibell, and Erich A. Pfeiffer - Biomedical Instrumentation and Measurements, Prentice-Hall 1990* 3. *Khandpur R.S Hand Book of Biomedical Instrumentation – Tata Mc Graw Hill publication , New Delhi 2nd edition 2003*	4. *Richard S.Cobbold Transducers for Biomedical Measurements; Principle and applications- John Wiley and sons, 1992.* 5. *R. Anand Natarajan - Biomedical Instrumentation and Measurements- PHI Learning, New Delhi, 2nd edition, 2015* 6. *Geddes LA and Baker L.E Principals of Applied Biomedical Instrumentation, 3rd Edition, John Wiley and sons, New york 1989*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*15%*	-	*15%*	-	*15%*	-
Level 2	*Understand*	*25%*	-	*20%*	-	*25%*	-
Level 3	*Apply*	*30%*	-	*25%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	*10%*	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	***Experts from Higher Technical Institutions***	***Internal Experts***
Dr. Saravanan Mohan, Principal researcher, Ericsson, India	*Dr. Noor Mahammad, Associate Professor, Department of CSE, IIITDM, Kancheepuram, Chennai.*	1. *Dr. U. Shajith Ali, Associate Professor, Department of EEE, SRM IST, Tiruchirappalli* 2. *Dr.Dheepanchakkravarthy. A, Associate Professor, Department of EEE, SRM IST, Tiruchirappalli*

Course Code	21ECE675T	Course Name	Embedded Automation Systems	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*apply the Fundamentals of Electronic Components related to automotive applications*
CLR-2:	*discuss on Automotive Sensors, Actuators and Instrumentations*
CLR-3:	*illustrate the Control Mechanisms in an Automotive System*
CLR-4:	*analyze various Telematics and Diagnostic methods*
CLR-5:	*illustrate about various problems in Automotive Industry*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*gain expertise in control theory and instrumentation for system design*	K3	3	-	3	2
CO-2:	*apply advanced electronics principle to microcomputer-based instrumentation and control systems*	K3	3	2	3	3
CO-3:	*analyze and apply sensor and actuator technologies in automotive electronic control*	K4	3	2	3	3
CO-4:	*design and implement advanced digital control systems for automotive powertrain and motion control*	K4	3	2	3	3
CO-5:	*integrate telematics and diagnostics for advanced automotive instrumentation and reliability*	K4	3	2	3	2

Module-1 – Systems Approach to Control and Instrumentation ***9 Hours***

System, Linear system theory, Steady-State sinusoidal frequency response of a system, State variable formulation of models, Control theory, Stability of Control System, Closed-Loop Limit Cycle Control, Instrumentation, Basic Measurement System, Filtering, Digital Subsystem, Sinusoidal Frequency Response, Discrete Time Control System, Closed loop control, Example Discrete Time Control System

Module-2: Fundamentals of Electronics, Microcomputer Instrumentation and Control ***9 Hours***

Semiconductor Devices, Transistors, ICs, Operational Amplifiers, Use of Feedback in Op Amps, Phase-Locked Loop, Digital Circuits, Logic Circuits (Combination and Sequential Circuits), Timers and Counters, Microcomputer fundamentals, Tasks and Operations, CPU Registers, Reading Instructions, Programming Languages, Microcomputer Hardware, Microcomputer Applications in Automotive Systems, Instrumentation Applications of Microcomputers, Microcomputers in Control Systems.

Module-3: Sensors, Actuators and Electronic Engine Control	***9 Hours***
Motivation for Electronic Engine Control, Exhaust Emissions, Fuel Economy, Test Procedures, Concept of an Electronic Engine Control System, Engine Performance Terms, Exhaust Catalytic Convertors, Electronic Fuel-Control System, Analysis of Intake Manifold Pressure, Idle Speed Control, Electronic Ignition, Automotive Control System Applications of Sensors and Actuators, Throttle Angle Sensor, Temperature Sensor, Coolant Sensor, Sensors for Feedback control, Knock Sensors, Automotive Engine Control Actuators, Variable Valve Timing, Electric Motor Actuators, Ignition System	
Module-4: Motion Aad Digital Powertrain Control System	***9 Hours***
Digital Engine Control, Features, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System, Summary of Control Modes, Cruise Control System, Cruise Control Electronics, Antilocking Braking System, Electronic Suspension System, Electronic Steering Control, Four Wheel Steering	
Module-5: Automotive Instrumentation, Telematics and its Diagnostics	***9 Hours***
Modern Automotive Instrumentation, Input and Output Signal Generation, Advantages of Computer Based Instrumentation, Display Devices, Flat Panel Display, Fuel Quantity Measurement, Coolant Temperature Measurement, Oil Pressure Measurement, Vehicle Speed Measurement, High Speed Digital Communication (CAN BUS), Telematics, GPS Navigation, GPS System Structure, Automotive Diagnostics - Reliability Functional Safety, Online Monitoring, Fault tolerance	

Learning Resources	*1. William B. Ribbens, "Understanding Automotive Electronics- An Engineering Prespective", 7th Edition, Butterworth-Heinemann Publications, 2012.* *2. Young A.P. & Griffiths, " Automotive Electrical Equipment" , ELBS & New Press,1999.* *3. Tom Weather Jr. & Cland c. Ilunter, " Automotive computers and control system", Prentice Hall Inc., New Jersey, 1984.* *4. Crouse W.H., " Automobile Electrical Equipment" , Mc Graw Hill Co. Inc., New York ,1995.* *5. Bechhold, " Understanding Automotive Electronic", SAE,1998.* *6. Robert Bosch," Automotive Hand Book", SAE, 5 th Edition,2000.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California. *2. Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member*	*Dr. V.R. Venkatasubramani, Associate Professor, Department of ECE, Thiagarajar College of Engineering, Madurai, venthiru@tce.edu*	*Mr. S.Karthikeyan, Assistant Professor, Department of ECE, SRMIST Tiruchirappalli*

Course Code	21ECE676T	Course Name	MEMS and Micro Systems	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*explore the history, evolution, and applications of MEMS and Microsystems, and understand scaling laws and miniaturization limits.*
CLR-2:	*learn about the materials used in MEMS fabrication and various fabrication processes involved in MEMS manufacturing.*
CLR-3:	*investigate the principles, design considerations, and performance metrics of various sensors and actuators used in MEMS.*
CLR-4:	*explore essential design and packaging considerations for microsystems, focusing on different packaging levels and key technologies.*
CLR-5:	*apply principles of MEMS design to practical applications.*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*4*
CO-1:	*explain the fundamental principles, historical development and significance of MEMS and Microsystems.*	K2	1	3	3	2
CO-2:	*identify the materials used in MEMS fabrication and Understand the processes involved in bulk and surface micromachining.*	K2	2	3	3	3
CO-3:	*design and analyze MEMS sensors and actuators.*	K4	1	3	3	3
CO-4:	*examine packaging techniques and their importance in MEMS.*	K4	1	3	3	3
CO-5:	*apply MEMS design principles to create functional devices.*	K3	2	3	3	3

Module-1: Introduction to MEMS and Microsystems ***9 Hours***

Overview of MEMS and Microsystems: Introduction and historical background, Evolution of MEMS technology, Applications. Microsystems and Microelectronics: Similarities and differences between Microsystems and Microelectronics, Microsystems technology in industrial applications. Scaling Laws in Miniaturization: Scaling in geometry, forces, and electrostatics,Limits of miniaturization.

Module-2: Materials and Fabrication Processes ***9 Hours***

Materials for MEMS: Silicon, polymers, metals, and ceramics.Properties and selection criteria for MEMS materials. Fabrication Techniques: Bulk Micromachining: Etching techniques, isotropic and anisotropic etching. Surface Micromachining: Thin-film deposition, lithography, etching.LIGA Process: Lithography, Electroplating, and Molding. Soft Lithography: PDMS molds, microcontact printing.

Module-3: Sensors and Actuators	***9 Hours***
Sensors: Pressure sensors, inertial sensors, bioMEMS. Principles of operation and design considerations. Actuators: Electrostatic, thermal, piezoelectric, and electromagnetic actuators. Design principles and performance metrics.	
Module-4: Microsystems Packaging	***9 Hours***
Key Design and Packaging Considerations: three levels of microsystem packaging, die level packaging, device level packaging, system level packaging. Interfaces in microsystem packaging, Essential Packaging technologies, Three Dimensional Packaging.	
Module-5: Case Studies	***9 Hours***
Blood Pressure Sensor: Background and History, Device Design Considerations, Commercial Case - NovaSensor BP Sensor. Acceleration Sensors: Design Considerations, Commercial Case - Analog devices and MEMSIC. Gyros: Coriolis Force, MEMS Gyro Design, Single Axis Gyro Dynamics, Commercial case - InvenSense Gyro.	

Learning Resources	1. *Tai - Ran Hsu, "MEMS and Micro Systems: Design, Manufacture and Nano scaleEngineering", 2nd Edition, Tata McGraw Hill, New Delhi, 2008.* 2. *Chang Liu, "Foundations of MEMS", Second Edition, Pearson , 2017* 3. *Eun Sokm Kim, "Fundamentals of Micro electro mechanical Systems (MEMS)" McGraw Hill Professional, 2021* 4. *Stephen D Senturia, "Microsystems Design", 2nd edition Springer Publishers, 2013.* 5. *Marc J. Madou, "Fundamentals of Microfabrication and Nanotechnology", CRC Press, Year: 2011*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*		*20%*		*20%*	
Level 2	*Understand*	*20%*		*20%*		*20%*	
Level 3	*Apply*	*30%*		*30%*		*30%*	
Level 4	*Analyze*	*30%*		*30%*		*30%*	
Level 5	*Evaluate*	-		-		-	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. *Venkat Sunkara, Founder & CEO, ChipEdge Technologies Pvt Ltd, Bengaluru.* 2. *Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.*	*Dr.S.Kirubaveni, Associate Professor, Department of ECE, Anna University, College of Engineering, Guindy, Chennai.*	*Dr. S. Amuthameena, Assistant Professor, Department of EEE, SRMIST Tiruchirappalli*

Course Code	21ECE677T	Course Name	Embedded System Design	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*illustrate the fundamentals on design attributes of functional units of embedded systems*
CLR-2:	*discuss about Hardware, software partitioning in system design*
CLR-3:	*introduce architectural features of 32 bit ARM microcontroller*
CLR-4:	*discuss strategies for embedded firmware design and development*
CLR-5:	*develop an integrated development environment in embedded system*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Bloom's Level*	*Programme Outcomes (PO)*			*Programme Specific Outcome (PSO)*
		K1-K6	*1*	*2*	*3*	*1*
CO-1:	*design embedded systems with hardware-software integration*	K3	3	-	3	2
CO-2:	*proficient in utilizing EDA tools for schematic and PCB design*	K3	3	2	3	3
CO-3:	*discuss and design of advanced programming features using ARM Cortex M3 architecture*	K4	3	2	3	3
CO-4:	*design and develop embedded firmware using RTOS principles*	K4	3	2	3	3
CO-5:	*expertise in writing multiple tasks under RTOS environment*	K4	3	2	3	3

Module-1 – TYPICAL EMBEDDED SYSTEM	***9 Hours***
Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Characteristics and Quality Attributes of Embedded Systems: Hardware, Software Co-Design and Program Modeling, RISC V, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software	
Module-2: Embedded Hardware Design and Development	***9 Hours***
Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning	

Module-3: ARM 32-bit Microcontroller Family	***9 Hours***
Architecture of ARM Cortex M3 –General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register, Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. Advanced Programming Features. Memory Protection. Debug Architecture	
Module-4: Embedded Firmware Design and Development	***9 Hours***
Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis	
Module-5: Embedded System Development Environment	***9 Hours***
Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations	

Learning Resources	*1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009* *2. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier), 2008.* *3. James K Peckol, "Embedded Systems – A contemporary Design Tool", John Weily, 2008.* *4. David. A.Patterson & John L. Hennessy, "Computer Organisation and Design : the Hardware and Software Interface:RISC - V, Morgan Kaufmann, 1st Edition, 2017.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*5%*		*15%*		*5%*	
Level 2	*Understand*	*10%*		*15%*		*10%*	
Level 3	*Apply*	*10%*		*30%*		*10%*	
Level 4	*Analyze*	*15%*		*30%*		*15%*	
Level 5	*Evaluate*	*10%*		*10%*		*10%*	
Level 6	*Create*	-		-		-	
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. *Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.* 2. *Dr.E.Raguvaran, Silicon Architecture Engineer, Intel Corporation, IEEE Senior Member.*	*Dr. V.R. Venkatasubramani, Associate Professor, Department of ECE, Thiagarajar College of Engineering, Madurai, venthiru@tce.edu*	*Mr. S.Karthikeyan, Assistant Professor, Department of ECE, SRMIST,Tiruchirappalli*

Course Code	21ECE678T	Course Name	Embedded C	Course Category	E	Professional Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1:	provide in depth knowledge in design a system with embedded C programming
CLR-2:	demonstrate and implement Peripheral device in microcontroller
CLR-3:	design and develop the hardware and software with design
CLR-4:	acquire the knowledge about the RTOS
CLR-5:	design and develop the Innovative Real Time Systems

Course Outcomes (CO):	At the end of this course, learners will be able to:	Bloom's Level	Programme Outcomes(PO)			PSO
		K1-K6	1	2	3	1
CO-1:	design a system with embedded C programming and debugging skills	K3	3	2	3	2
CO-2:	interface the peripheral device with microcontroller	K3	2	3	3	3
CO-3:	analyze the scheduling strategies and process methods involved in RTOS	K4	2	3	3	3
CO-4:	design and develop the hardware and software	K4	3	2	3	3
CO-5:	explore and develop innovative Real time systems	K4	2	2	3	3

Module-1 – Introduction and Protocols **9 Hour**

Introduction to Embedded C Prog., I/O Port Handling, Parallel I/O Programming, Running LEDs using Program, Arbitration: Arbitration using priority arbiter, Standards: UART, Serial Peripheral Interface, SPI Operations and Interfacing, Universal Serial Bus, Universal Serial Bus interfacing, Inter- Integrated Circuits operation, IEEE802.11Wi-FiStandard, IEEE802.15 Bluetooth Protocol, Bluetooth Protocol Architecture.

Module-2 – Microcontroller and Interfacing Peripherals **9 Hour**

8 bitMicrocontroller-Features-Architecture-MemoryOrganization-I/OPorts-Timers-Watchdog Timers - ADC - Interrupts - RESET - CCP Modules - USART - I2C - SPI - Parallel SlavePort, LED - LCD - Seven Segment Display - Motors (DC, Stepper, Servo) - Relay - Keypad - Keyboard -Sensors -, Global Positioning System - External Serial Buses – RS 232 – RS 422 – RS 485 -USB -CAN –LIN.

Module-3 – RTOS Programming **9 Hour**

RTOS: Tasks and task states, Task Scheduling in RTOS, Priority Inversion ,Priority Ceiling, Priority Inheritance, Shared-Data Problem, Interrupt Latency, Multitasking, Context Switching, Semaphores, Serial Port Programming in assembly language, Serial Port Programming in High level language, Applications of Semaphores, Semaphore synchronization mechanisms, Applications of Semaphores, Process .

Module-4 - Process Communication **9 Hour**

Communication, Process handling in OS, Uni-processor Embedded System, Kernel, Multi-processor Embedded System basics, Introduction to Open MP, Tasking: The task and task stack access, task- wait Constructs, Exceptions and Interrupts.

Module-5 – Device Driver Programming and Case Studies	***9 Hour***
Introduction to Linux Kernel and Porting, The Boot Process, Role of device Driver, Module Basics, Steps to write the module, Implementing System Calls, System Call functions, Task priority, Tasking dependencies, Task Scheduling, Task context, stack and control blocks, Kernel Debugging, OS Debugging functions, USB Driver, USB Driver OS handling, Multitasking in OS, Multitasking Open MP, Linux Kernel module level programming - Case Studies.	

Learning Resources	1. *Mark Sieges mund, "Embedded C Programming- Techniques and Applications of C and PIC MCUs", New nesis an imprint of Elsevier, First Edition,2014.* 2. *Robert Love, Linux System Programming: Talking directly to the kernel and C library: and C Library, 2013, 2nd Edition, Reilly Publication, USA.* 3. *Neil Mathew, Richard stones, Beginning Linux Programming, 2012 reprint, Wrox–Wiley Publishing, USA.* 4. *TimWilmshurst,"Designing Embedded Systems with PIC microcontrollers-Principles and Applications",Newnes Publications,2007.*	5. *Muhammad Ali Mazidi, Rolin Mc Kinlay,Danny Causey,"PIC Microcontroller and Embedded Systems: Using Assembly and C for PIC18", Prentice Hall publications,2007.* 6. *Richard Barnett, LarryO'Cull, SarahCox,"Embedded C Programming with the Microchip PIC",Delmar Learning, adivision of ThomsonLearning, 2004.* 7. *PhillipA.Laplante,"Real- Time System Design and Analysis", AJohn Wiley & Sons, Inc, Third Edition,2004*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*15%*	-	*15%*	-	*15%*	-
Level 2	*Understand*	*25%*	-	*20%*	-	*25%*	-
Level 3	*Apply*	*30%*	-	*25%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*25%*	-	*30%*	-
Level 5	*Evaluate*	-	-	*15%*	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	***Experts from Higher Technical Institutions***	***Internal Experts***
1. *Kaarthick Balakrishnan, Research Director, ANCIT Automotive Electronics Consultant, Coimbatore.* 2. *Santosh Ramachandran, Verification, AI/ML d-Matix, Santa Clara, California.*	1. *Dr. Noor Mahammad, Associate Professor, Department of CSE, IIITDM, Kancheepuram, Chennai.* 2. *Dr. M. Gulam Nabi Alsath, Associate Professor, Department of ECE, Anna University, College of Engineering, Guindy, Chennai.*	1. *Dr. V.N. Senthil Kumaran, Associate Professor, Department of ECE, SRM IST, Tiruchirappalli* 2. *Dr Viseveksenan, Professor, Department of ECE, SRM IST,Tiruchirappalli.*