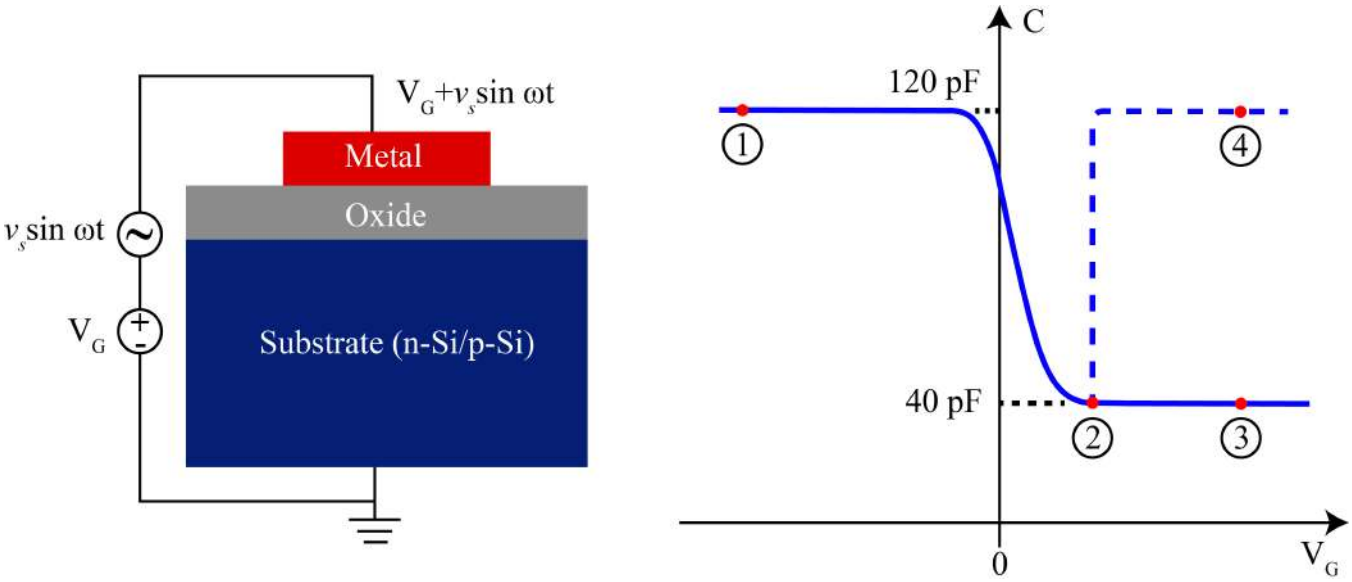
ISD 2023 - Week 8 Assignment

There are 10 questions for a total of 20 marks.

For Q1-Q6: A PG student procures a few identical MOSCAP devices from the market and tries to characterize them in the lab. The basic structure of the MOSCAP is shown below. V_G is the applied dc gate voltage, and v_s is a small signal ac voltage of frequency, ω. The $C-V$ characteristics of one of the MOSCAPs, taken at two different frequencies, is also shown in the figure. Based on the given data, answer the questions that follow.



1. (2 marks) The substrate doping and the type of MOSCAP is _____.

   A. $p-$type and NMOS

   B. $n-$type and PMOS

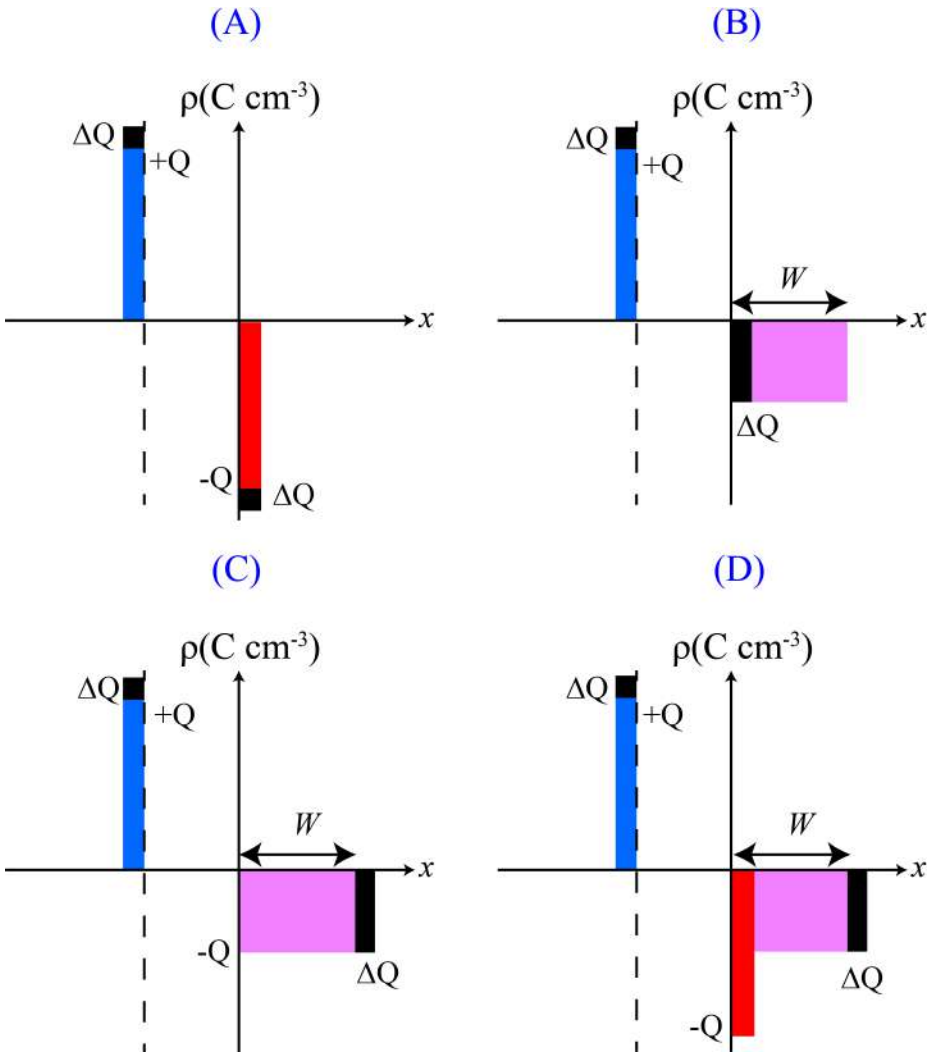
   C. $p-$type and PMOS

   D. $n-$type and NMOS

   E. ambivalent and PMOS

Reflect and remember: The practical way to obtain the "low frequency" or quasi-static CV using a MOS capacitor involves applying a very slow linear-ramp voltage ($< 0.1\ Vs^{-1}$) to the gate and measuring I_G with a very sensitive DC ammeter during the ramp. The capacitance is calculated from $I_G = C\frac{dV_G}{dt}$. This technique provides sufficient time for Q_{inv} to respond to the slowly changing V_G.

2. (2 marks) The charge block diagram corresponding to point 2 in the CV is given in the figure _____ below.



A. A

B. B

C. C

D. D

Reflect and remember: In accumulation (Point 1 in the CV curve), the DC state is characterized by the pileup of majority carriers right at the oxide-semiconductor interface. The state of the system can be changed rapidly as the majority carriers can equilibrate with a time constant on the order of 10^{-10} to 10^{-13} sec. Thus, the charge *accumulated* in a MOSCAP at the edges, when an ac signal is applied, is essentially that of an ordinary parallel plate capacitor.

3. (2 marks) If the area of the MOSCAP is $3 \times 10^{-3}\ cm^2$, then the thickness of the oxide layer is _____ μm. (Use $\epsilon_{ox} = 3.9$, $\epsilon_{Si} = 11.9$, $\epsilon_0 = 8.85 \times 10^{-14}\ Fcm^{-1}$)

   A. 0.263
   B. 103.5
   C. 0.086
   D. 0.345
   E. 28.76

$C_{ox} = \frac{\epsilon_{ox} \times Area}{t_{ox}} \Rightarrow t_{ox} = \frac{3.9 \times 8.85 \times 10^{-14} \times 3 \times 10^{-3}}{120 \times 10^{-12}}$

$\therefore t_{ox} = 8.628 \times 10^{-6}\ cm$

$t_{ox} = 0.086\ \mu m$

4. (2 marks) Invoking delta-depletion approximation, the maximum depletion width (W) in the given MOSCAP is _____ μm.

   (Maximum depletion width occurs at $\phi_S = 2 \times \phi_F$, point 2 in the CV plot. Use $\epsilon_{ox} = 3.9$, $\epsilon_{Si} = 11.9$, $\epsilon_0 = 8.85 \times 10^{-14}\ Fcm^{-1}$)

   A. 0.172
   B. 0.526
   C. 0.26
   D. 0.79
   E. 34.5

Max depletion width occurs when MOSCAP is in depletion

$\Rightarrow C_{dep} = \frac{\epsilon_{Si} \times Area}{W_{max}}$

$\Rightarrow W_{max} = \frac{11.9 \times 8.85 \times 10^{-14} \times 3 \times 10^{-3}}{60 \times 10^{-12}}$

$W_{max} = 0.526\ \mu m$

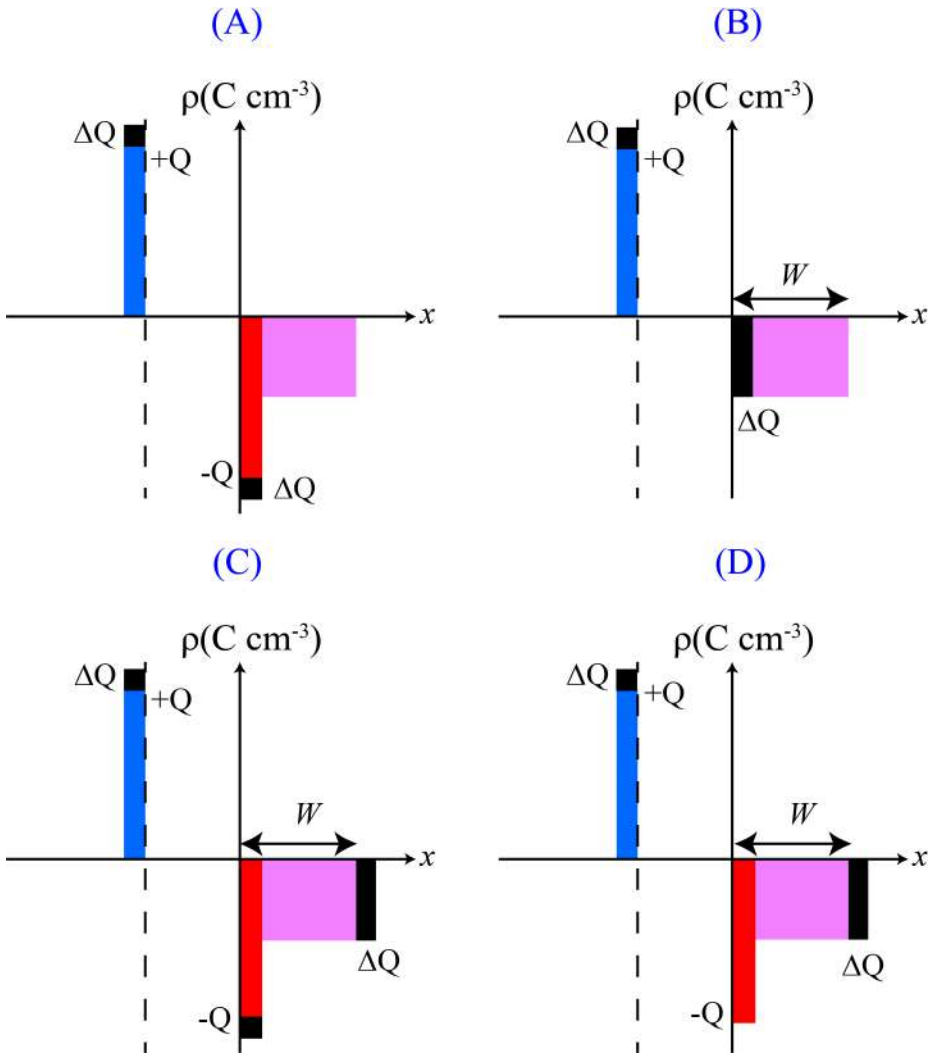
$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$

$\frac{1}{C_{dep}} = \frac{1}{40} - \frac{1}{120}$

$\Rightarrow C_{dep} = 60\ pF$

Reflect and remember: In depletion (Point 2 in the CV curve), the DC state is characterized by a depletion layer charge in the semiconductor. The depletion layer charge is directly related to the withdrawal of the majority carriers from adjacent to the oxide-semiconductor interface. The situation is analogous to two parallel plate capacitors (C_{ox} and C_{dep}) in series.

5. (2 marks) The charge block diagram corresponding to the points 3 and 4 in the CV are _____.



A. ③→ A; ④→ C

B. ③→ A; ④→ D

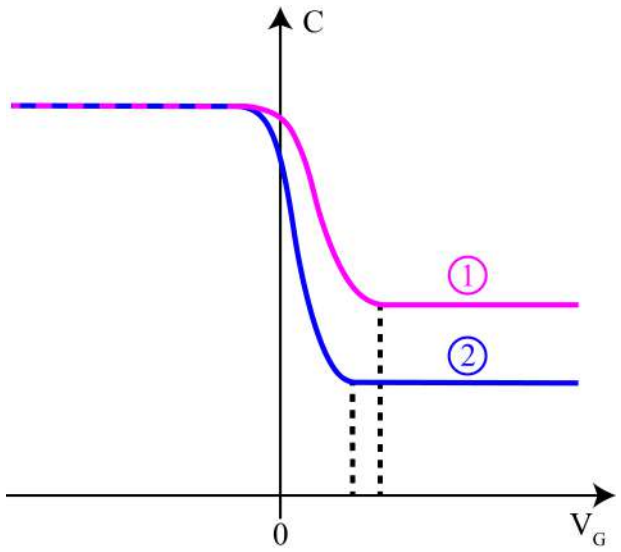
C. ③→ B; ④→ C

D. ③→ D; ④→ A

E. ③→ A; ④→ A

6. (2 marks) In the above experiments, the student finds two sets of CV curves, as shown in the figure below. (Assume the gate area is the same for both the MOSCAPs). Choose the correct option based on the given data, where Na_1 and Na_2 are the doping concentrations of bulk in MOSCAP 1 and 2, respectively.

A. $Na_1 > Na_2$



B. $Na_1 < Na_2$

C. $Na_1 = Na_2$

D. substrate doping doesn't change C_{min}

7. (2 marks) Consider the following statements –

S_1 : The LFCV and HFCV curves of a MOSCAP are identical in the accumulation and depletion regions.

S_2 : Accumulation and Depletion regions are characterized by majority carrier response time, which is much smaller than the applied frequency.

A. S_1 is true and S_2 is false.

B. S_1 is true and S_2 is true, and S_2 is the correct explanation of S_1.

C. S_1 is false and S_2 is true.

D. Both S_1 and S_2 are false.

8. (2 marks) **(EC-GATE 2017)** A MOS capacitor is fabricated on p-type Si (silicon) where the metal work function is $4.1\ eV$, and electron affinity of Si is $4.0\ eV$, and $E_C - E_F = 0.9\ eV$; where E_C and E_F are conduction band minimum and the Fermi energy levels of Si, respectively. If the measured flat band voltage of this capacitor is $-1V$, then the magnitude of the fixed charge at the oxide semiconductor interface, in nC/cm^2, is _____.

(Use $\epsilon_{ox} = 3.9$, $\epsilon_0 = 8.85 \times 10^{-14}\ Fcm^{-1}$, oxide thickness $t_{ox} = 0.1\ \mu m$ and electron charge $q = 1.6 \times 10^{-19}\ C$.)

$\phi_{ms} = 4.1 - (4 + 0.9)$

$= 4.1 - 4.9$

$= -0.8eV$

A. 6.9

$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$

$\Rightarrow -1 = -0.8 - \frac{Q_{ox}}{C_{ox}}$

$Q_{ox} = 0.2 \times C_{ox} = 6.9\,nC/cm^2$

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{0.1 \times 10^{-4}}$

$= 3.4515 \times 10^{-8}\ F/cm^2$

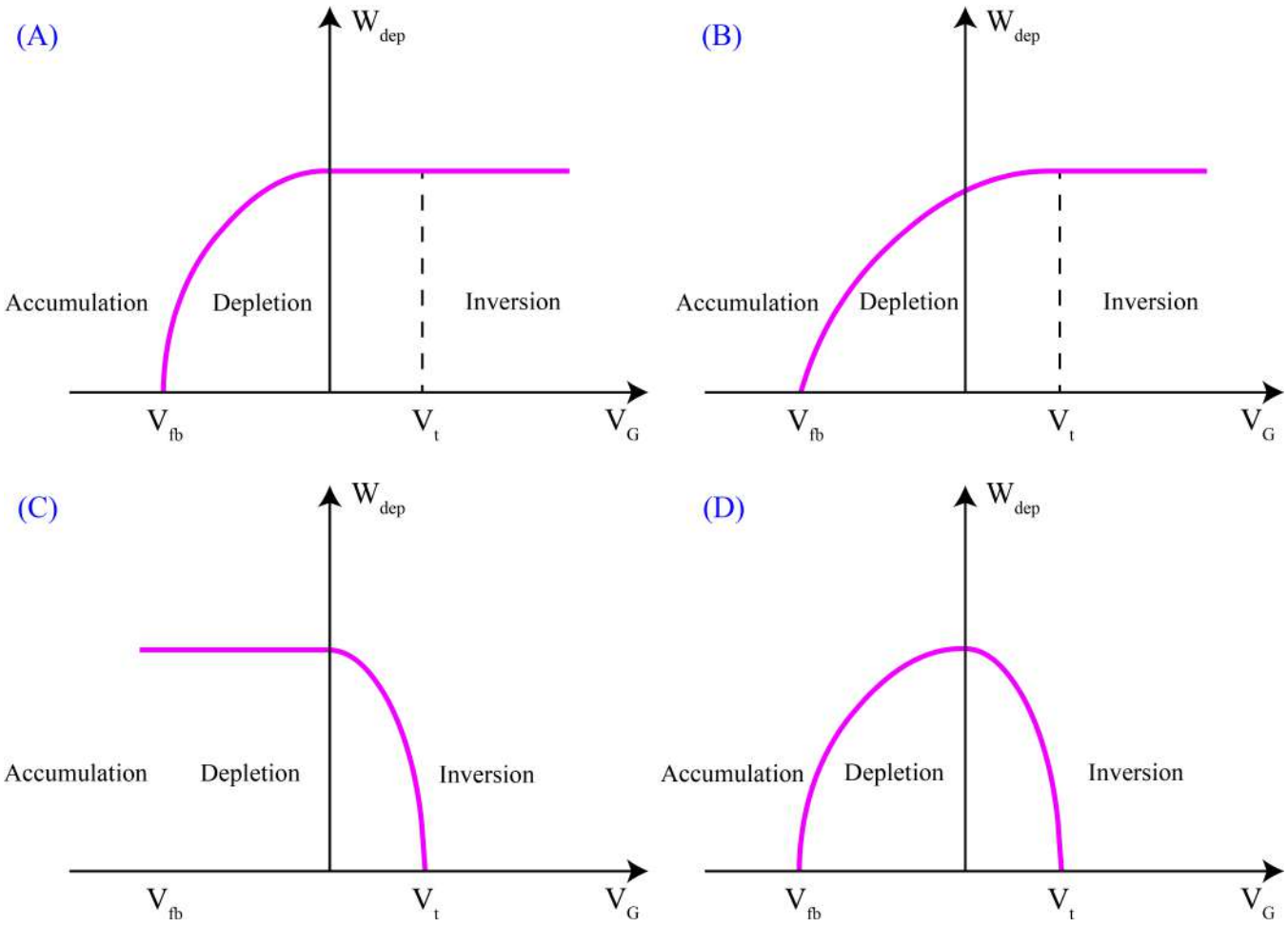
B. 69

C. 0.69

D. 0.069

Reflect and remember: Interface states and fixed oxide charge appear after the oxide is subjected to high electric fields for some time due to the breaking or rearrangement of chemical bonds. This raises a reliability concern because the threshold voltage and transistor current would change with usage and can potentially cause sensitive circuits to fail. Engineers ensure device reliability by controlling the stress field and improving the MOS interface quality, and verifying or projecting the reliability with careful long-term testing.

9. (2 marks) **(EC-GATE 2023)** For a MOSCAP, V_{fb} and V_t are the flat-band voltage and the threshold voltage, respectively. The variation of the depletion width (W_{dep}) for varying gate voltage (V_G) is best represented by –



A. A

B. B

C. C

D. D

Reflect and remember: The surface potential, ϕ_S, is zero at V_{fb} and approximately zero in the accumulation region. As V_G increases from V_{fb} into the depletion regime, ϕ_S increases from zero to $2\phi_F$. When ϕ_S reaches $2\phi_F$, the surface electron concentration becomes so large that the surface is considered inverted. The V_G at that point is called V_T, the threshold voltage. Beyond V_T, the ϕ_S remains constant at $2\phi_F$. The depletion width, W_{dep}, is proportional to $\sqrt{\phi_S}$.

10. (2 marks) In a MOS capacitor, the capacitance at the threshold voltage is due to _____.

A. oxide capacitance

B. depletion capacitance

C. oxide capacitance in series with depletion capacitance

D. oxide capacitance in parallel with depletion capacitance

E. depletion width

F. carrier density