SIMULATION EXPERIMENTS USING LT_SPICE SOFTWARE (VERSION 17)

Exp.No: **VERIFICATION OF THEOREMS**
Date :

Aim:

To verify Kirchhoff's Voltage Law, Kirchhoff's current Law and superposition theorem using LT-SPICE simulation package.

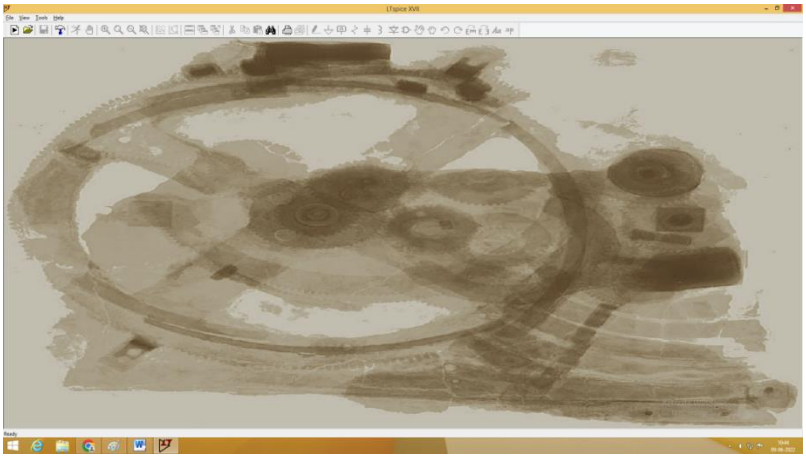
Tools Used: PC/Laptop loaded with LT-SPICE.

Procedure:

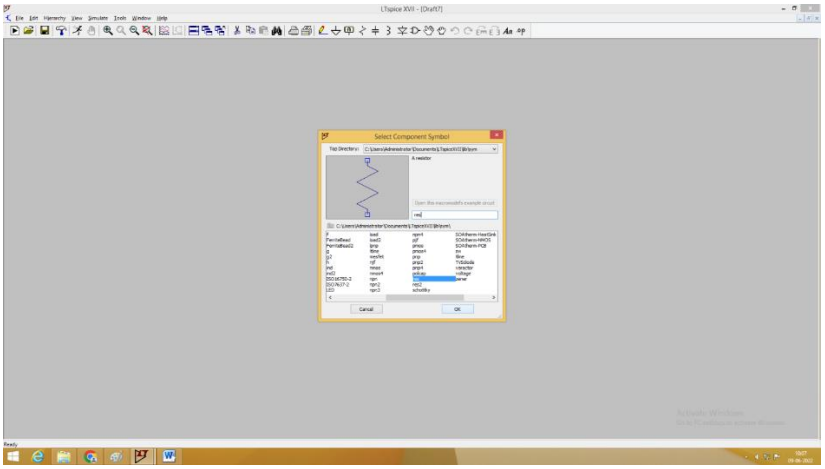
1. Open LTSpice software.
2. Start a new schematic design by clicking File->New schematic.
3. Place the components as per the given circuit to the new schematic page.
4. Save the schematic design inside a user created folder using File-> Save As.
5. Rearrange the components and connect the wires to complete the circuit drawing.
6. Change the values of the components.
7. If necessary, Rename the parts, and add a net name for every node.
8. Setup the simulation command by using simulate-> Edit simulation Cmd.
9. Select any one of the simulation types such as Transient, AC Analysis, DC Sweep or DC op pnt as per the circuit analysis needs.
10. Perform simulation by selecting Run option.
11. Observe the input and output results.

ILLUSTRATION:

1) The latest version of LTSpice Software must be opened.
2) To start a new schematic design,
   Click File->New schematic

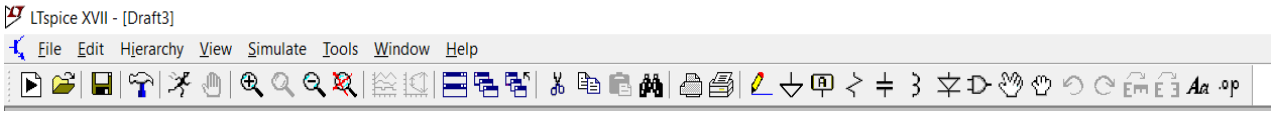


3) To place the components, Use the Component toolbox.



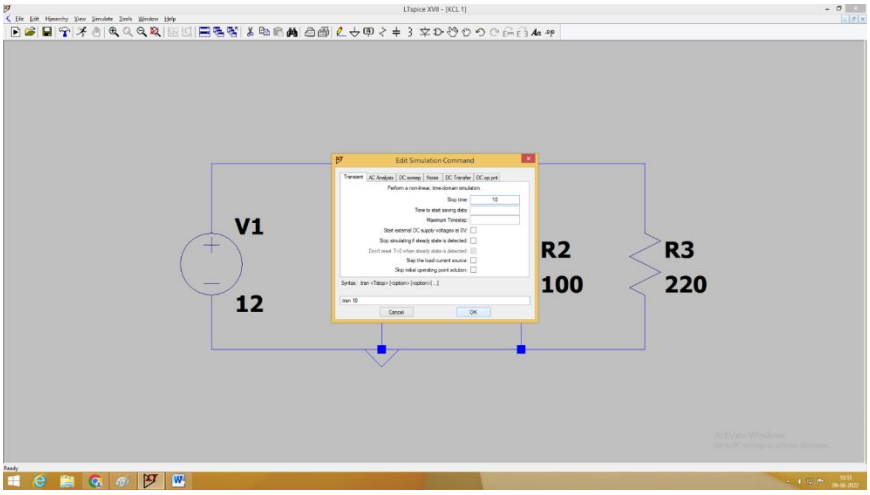
4) Use the shortcut keys or the icons at the toolbar of the schematic.
   Shortcut Keys:

Component selection	:F2	;Ground	:G
Connecting wires	:F3	;Inductor	:L
Diode	:D	;Capacitor	:C
Resistor	:R or r	;Rotate	:Ctrl+R



5) To save the schematic, Click File->Save As and save the schematic in a folder.Rearrange the components using Ctrl+R, and connect the wires as such in the given circuit.

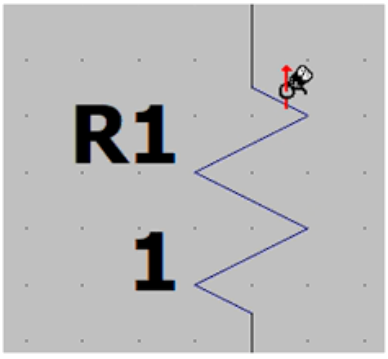
6) Move the cursor to the component, Right click when you see a hand symbol, Enter the values for the respective component.If necessary, Right Click on the name of the component and rename the components, If necessary, Rename a node by Clicking on F4(shortcut for Label Naming).
7) To setup the simulation command, Click Simulate->Edit Simulation Cmd. Select any one of the simulation types such as Transient, AC Analysis, DC Sweep or DC op pnt as per the circuit analysis needs.



8) Perform simulation by clicking on Run option.
9) Observe the input and output results

Measure the voltage of the component in the graph by clicking on the end of the component while the knob - like icon is visible.

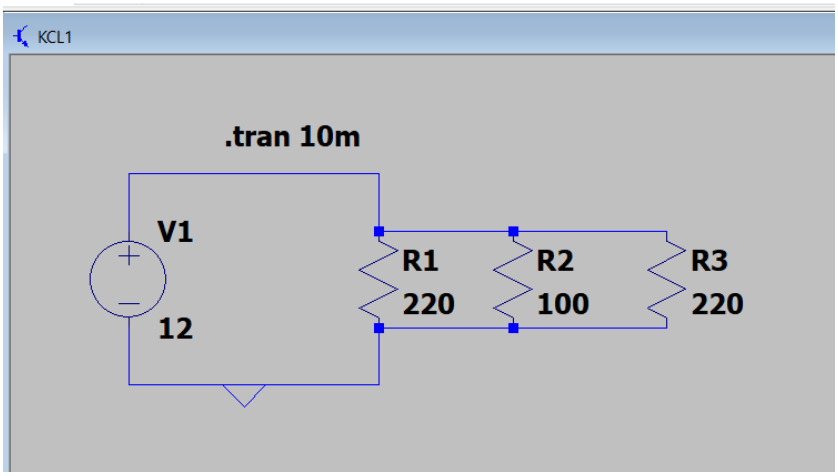
Measure the current of the component in the graph by clicking on the end of the component while the arrow – like icon is visible.



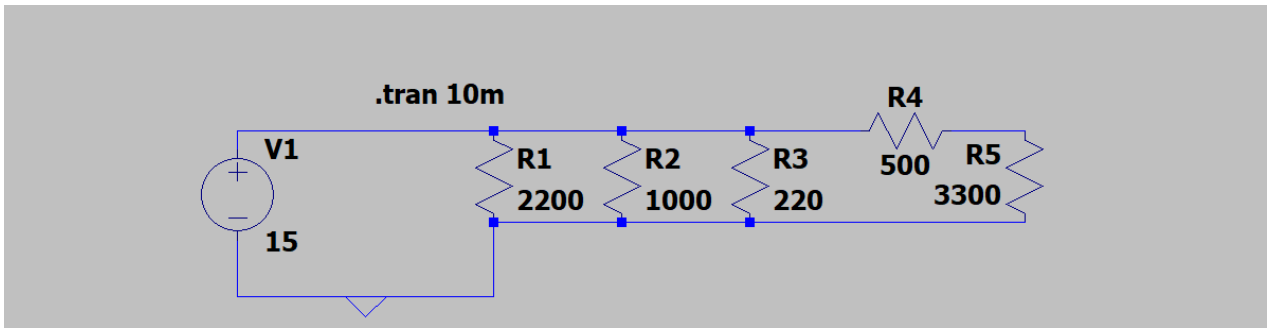
SCHEMATIC CIRCUIT DIAGRAMS

Kirchhoff Current Law:

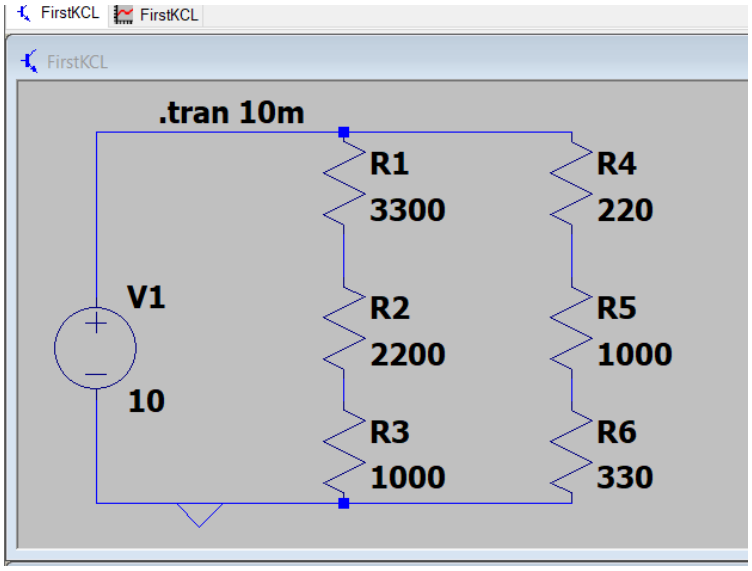
1)



2)

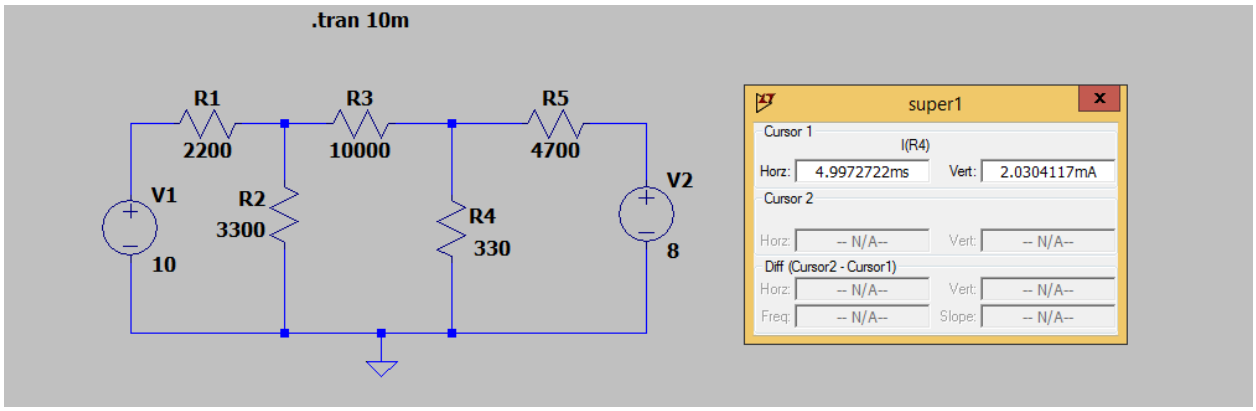


Kirchhoff Voltage Law:

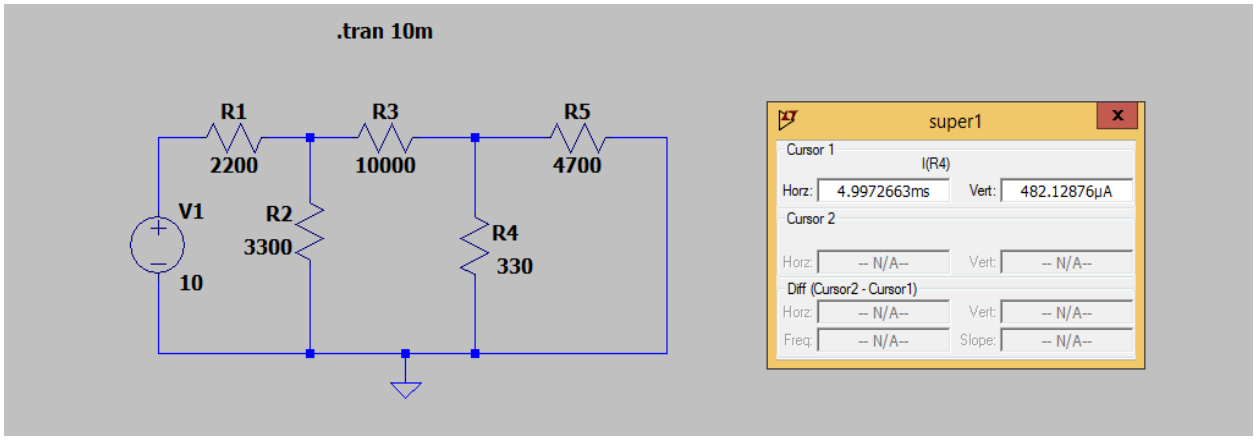


Superposition Theorem:

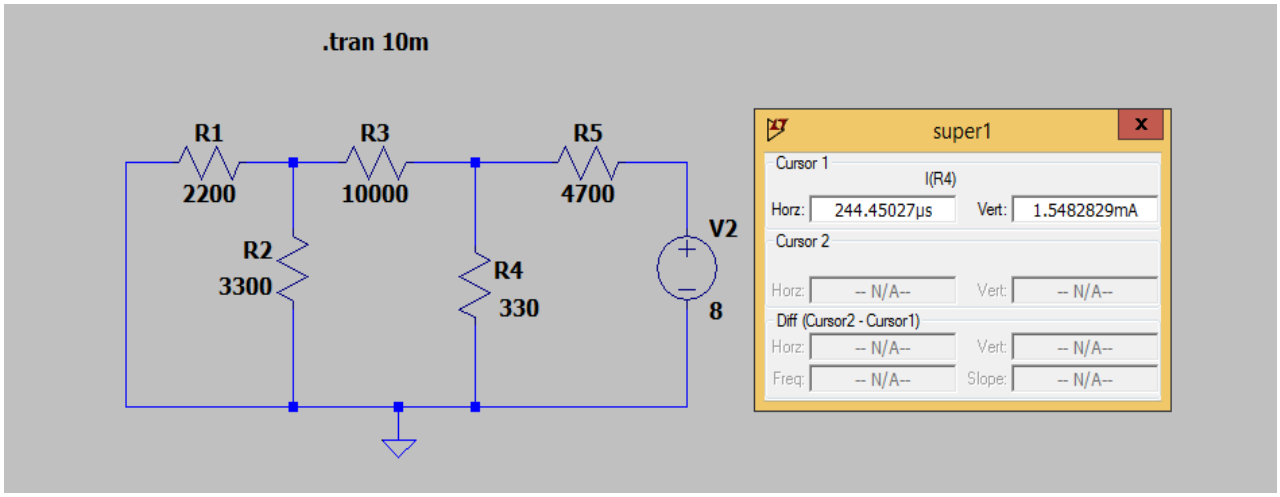
Total:



Keeping V1 and short circuiting V2:

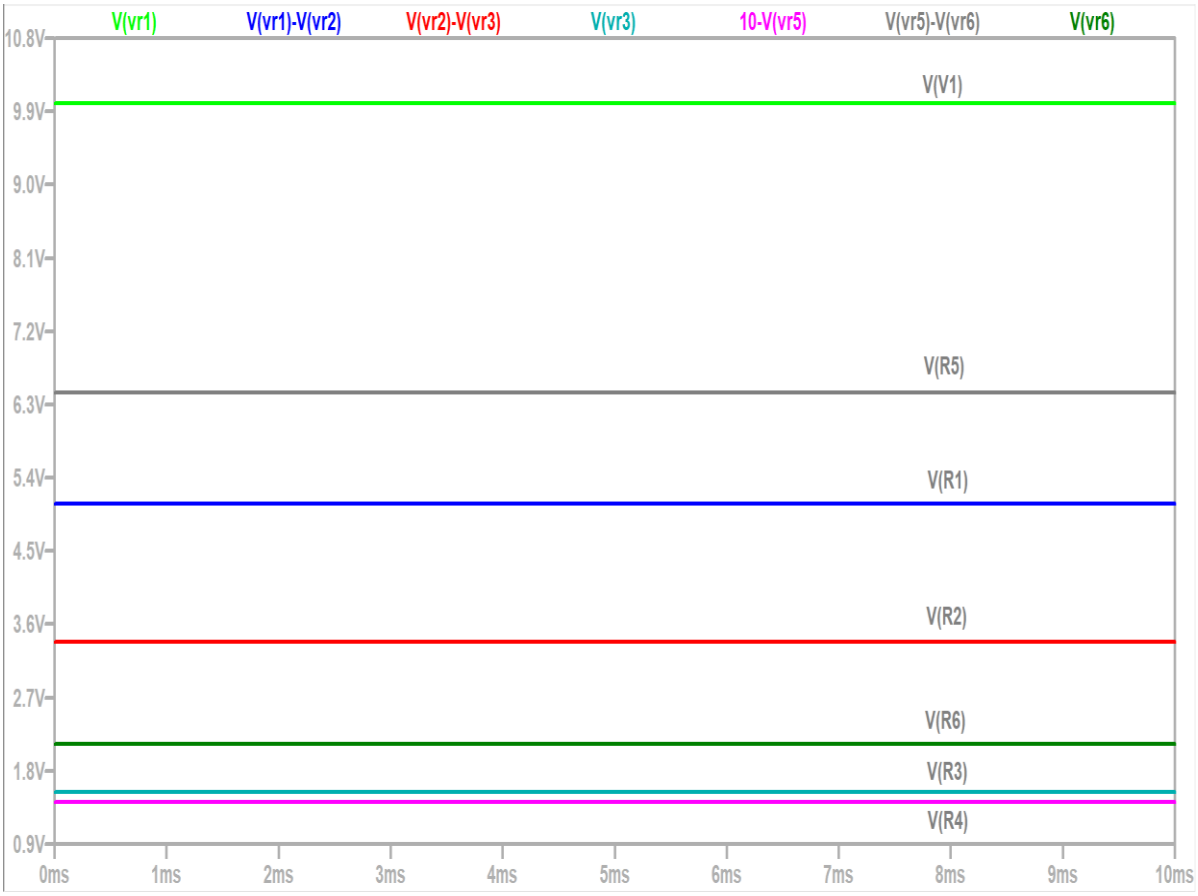


Keeping V2 and short circuiting V1:



OUTPUT RESULTS:

1. KVL VERIFICATION:



The voltage supplied is, V1 = 10V ----------1

Voltage across R1, V(R1) = V(vr1) – V(vr2) = 5.076V

Voltage across R2, V(R2) = V(vr2) – V(vr3) = 3.374V

Voltage across R3, V(R3) = V(vr3) = 1.550V

V(R1) + V(R2) + V(R3) = 10V ----------2

Voltage across R5, V(R4) = 10 – V(vr5) = 1.411V

Voltage across R2, V(R5) = V(vr5) – V(vr6) = 6.459V

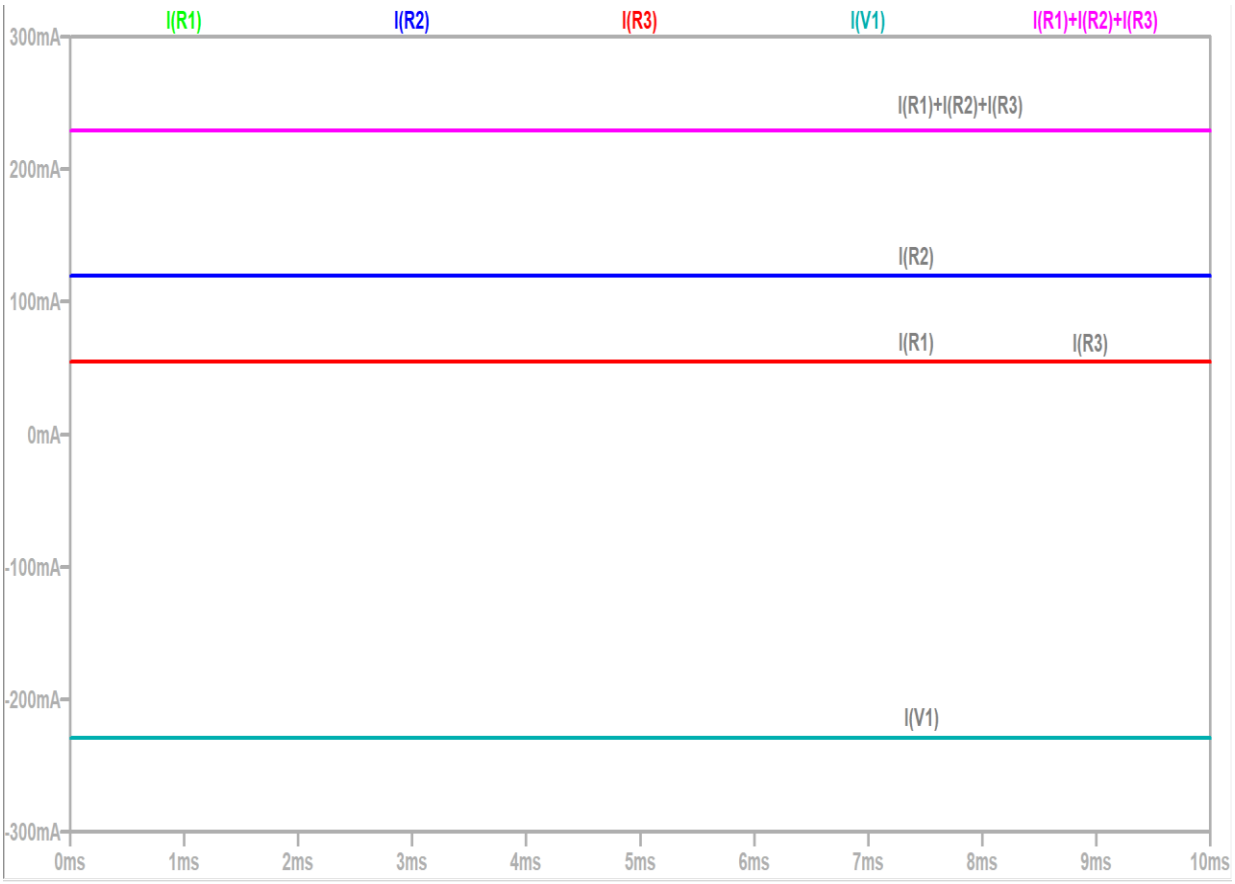
Voltage across R3, V(R6) = V(vr6) = 2.130V

V(R4) + V(R5) + V(R6) = 10V----------3

From 1, 2 and 3, KVL is verified

2. **KCL VERIFICATION**:

1ST CIRCUIT



Current flowing from V1, I(V1) = 229.19mA --------1

Current flowing through R1, I(R1) = 54.78mA

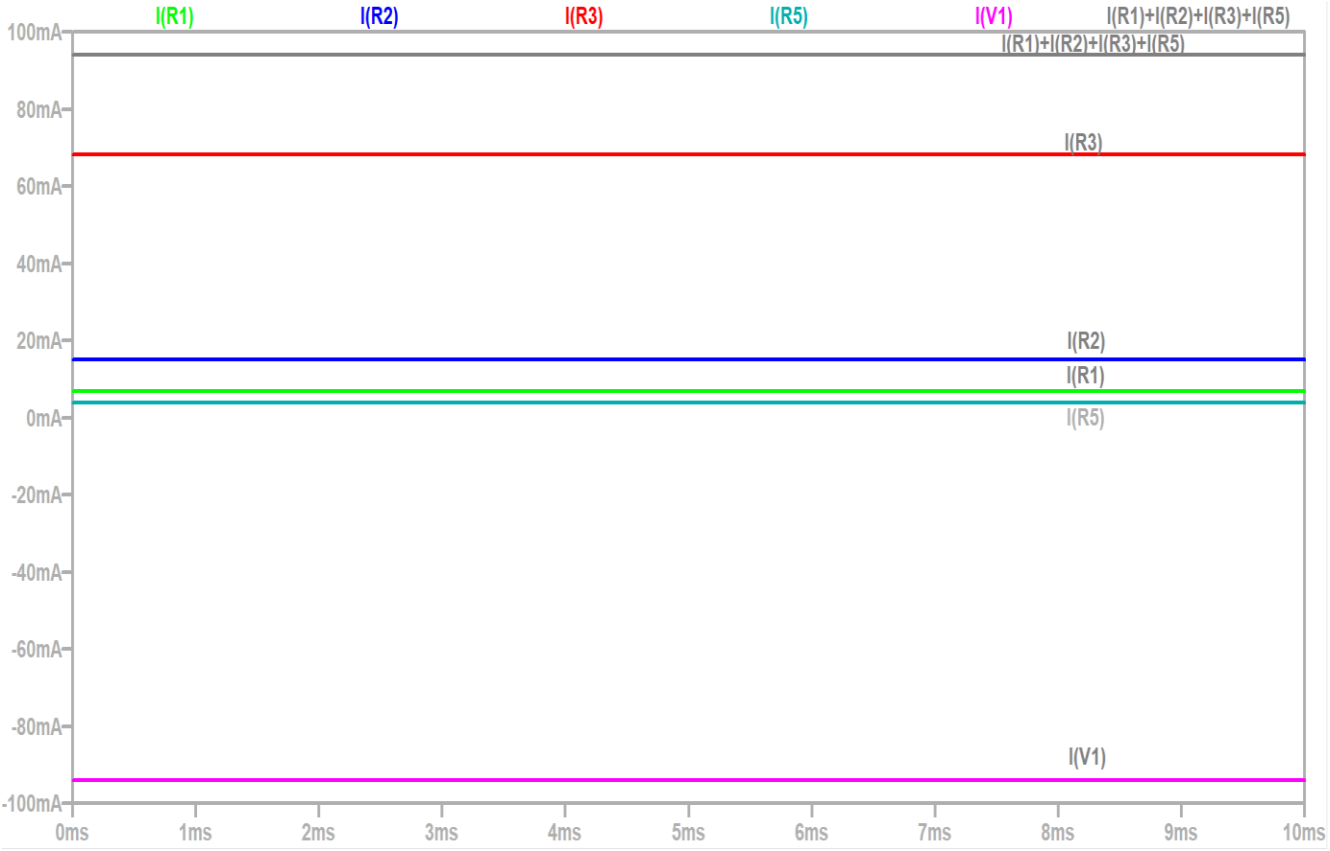
Current flowing through R2, I(R2) = 119.63mA

Current flowing through R3, I(R3) = 54.78mA

I(R1) + I(R2) + I(R3) + = 229.91mA --------2

From 1 and 2, KCL is verified

2ND CIRCUIT



Current flowing from V1, I(V1) = 93.91mA ----------1

Current flowing through R1, I(R1) = 7.08mA

Current flowing through R2, I(R2) = 14.78mA

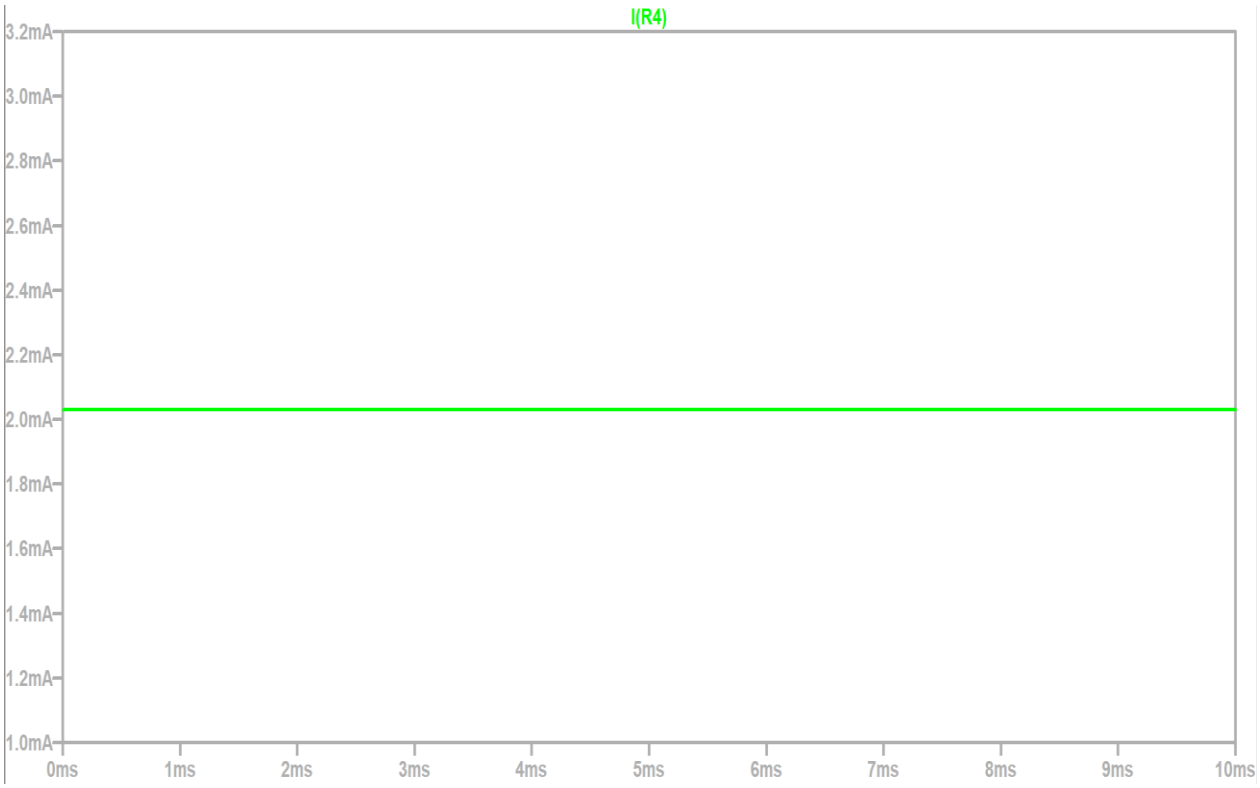
Current flowing through R3, I(R3) = 68.20mA

Current flowing through R5, I(R5) = 3.85mA

I(R1) + I(R2) + I(R3) + I(R5) = 93.91mA ----------2

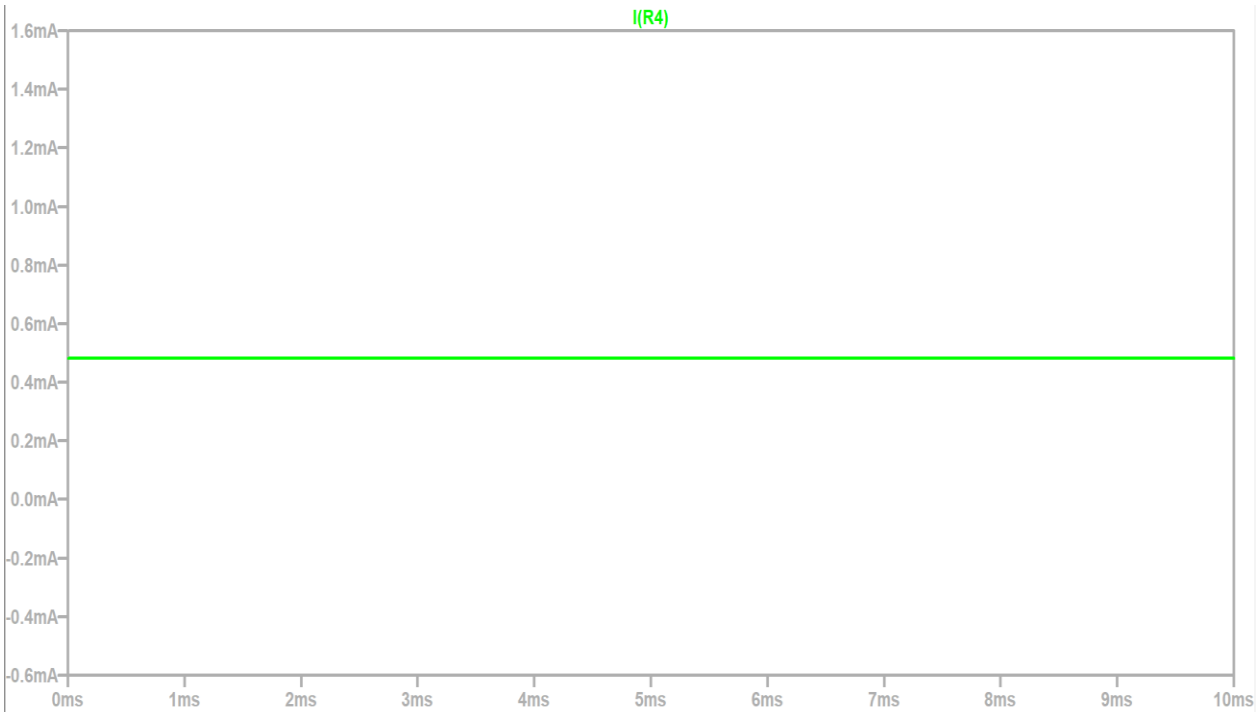
From 1 and 2, KCL is verified

3.SUPERPOSITION THEOREM VERIFICATION:



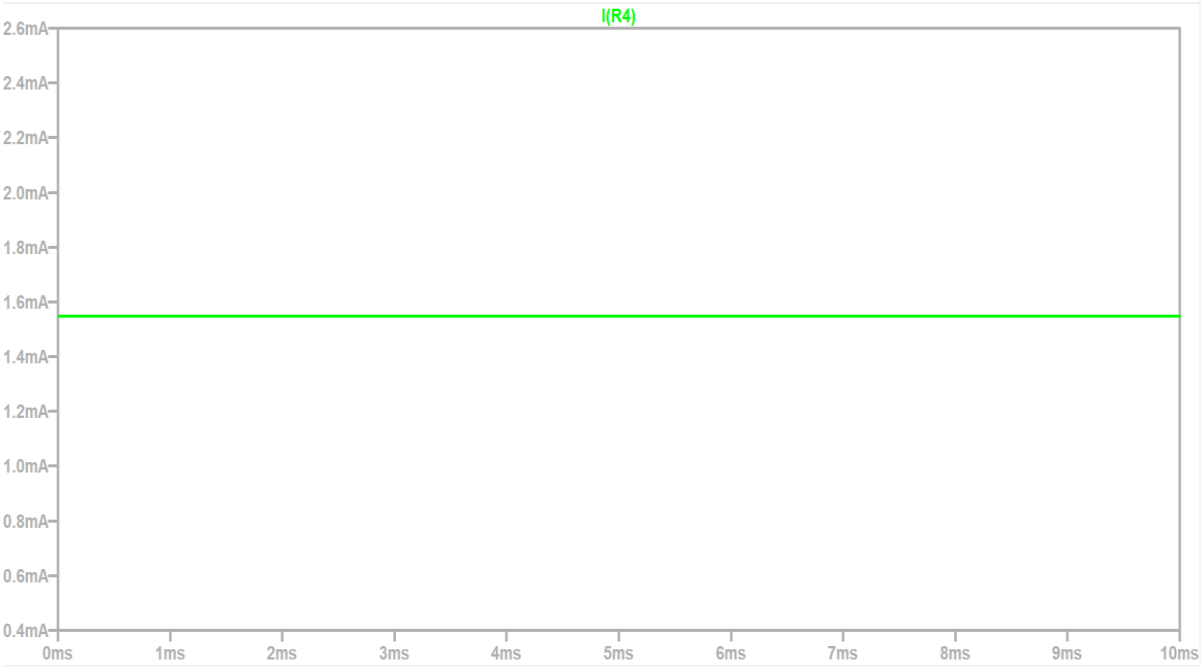
Current through R4, I(R4) = 2.033mA ----------1

After removing the 2nd source(8V),



Current through R4, I(R4) = 0.485mA

After removing 1st source(10V),



Current through R4, I(R4) = 1.548mA

Apply superposition theorem,

I(R4) = 1.548 + 0.485 = 2.033mA ----------2

From 1 and 2, Superposition theorem is verified

RESULT:

Thus the verification Kirchhoff's Voltage Law, Kirchhoff's current Law and superposition theorem was done using LT

Exp. No: **SERIES AND PARALLEL RESONANCE CIRCUITS**
Date:

Aim:

To verify Frequency response of series and parallel resonance circuits using LT-SPICE simulation package.

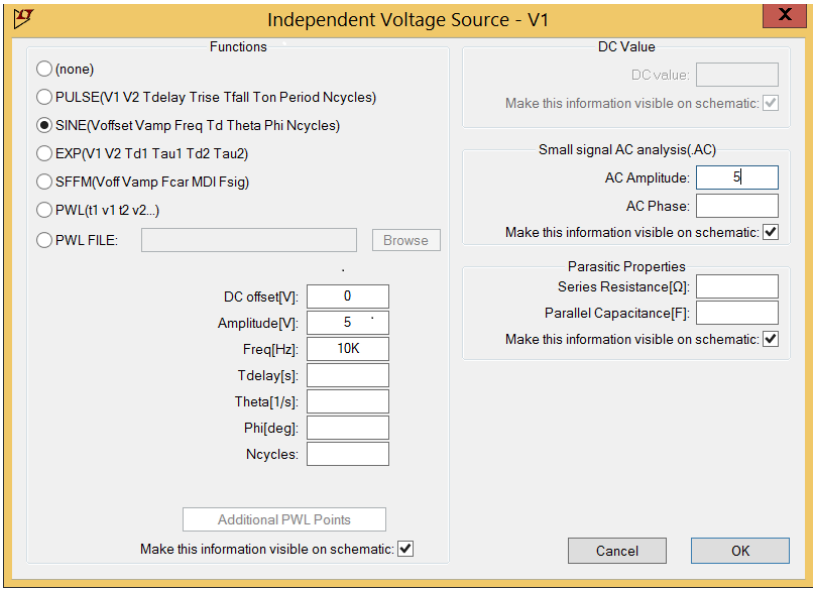
Tools Used: PC/Laptop loaded with LT-SPICE

Keyboard shortcuts:

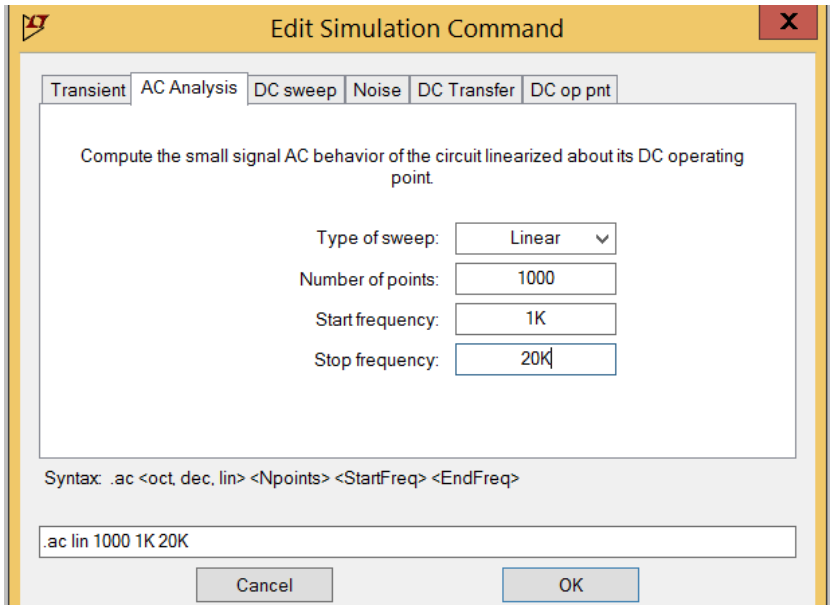
1. Component selection : F2
2. Connecting wire: F3
3. Diode : D
4. Ground : G
5. Resistor: R
6. Inductor: L
7. Capacitor: C

.**Procedure:**

1. Open LTSpice software.
2. Start a new schematic design by clicking File->New schematic.
3. Place the components as per the given circuit to the new schematic page.
4. Save the schematic design inside a user created folder using File-> Save As.
5. Rearrange the components and connect the wires to complete the circuit drawing.
6. Change the values of the components.



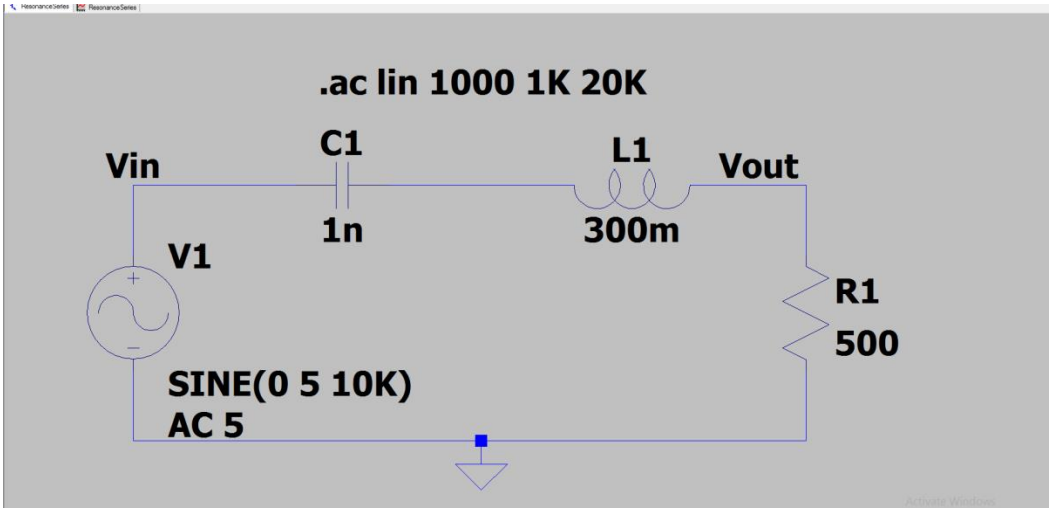
7. If necessary, Rename the parts, and add a net name for every node.
8. Setup the simulation command by using simulate-> Edit simulation Cmd.
9. Select any one of the simulation types such as Transient, AC Analysis, DC Sweep or DC op pnt as per the circuit analysis needs.



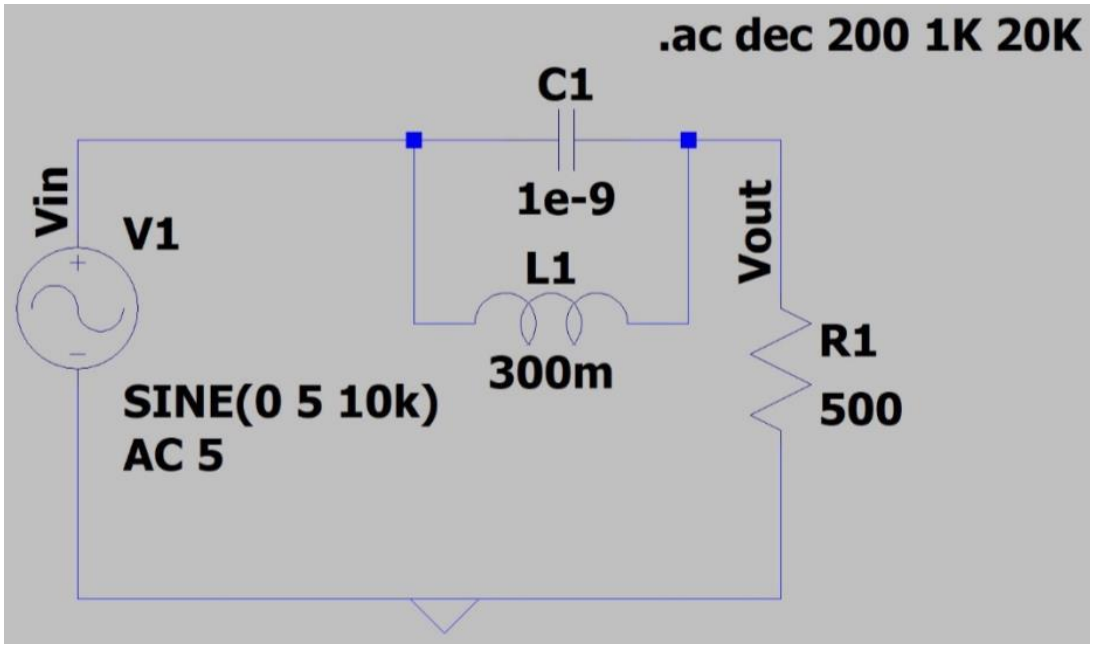
10. Perform simulation by selecting Run option.
11. Observe the input and output results.

SCHEMATIC CIRCUIT DIAGRAMS:

Series resonance circuit:

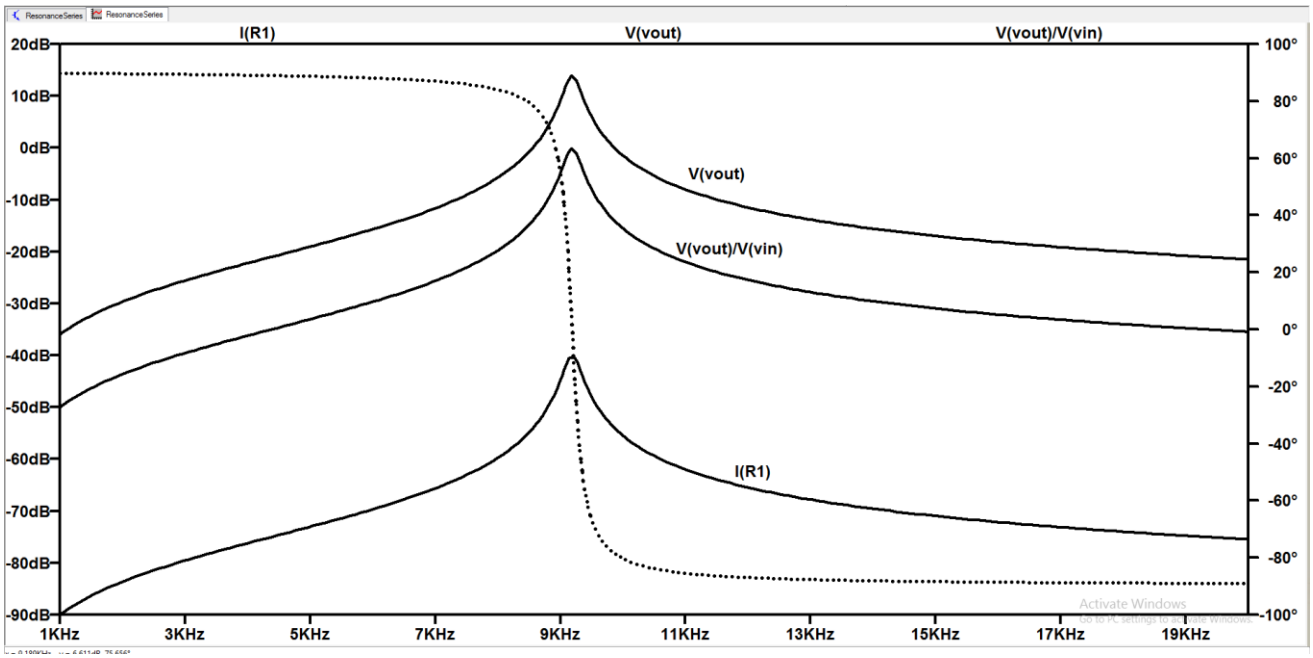


Parallel resonance circuit:

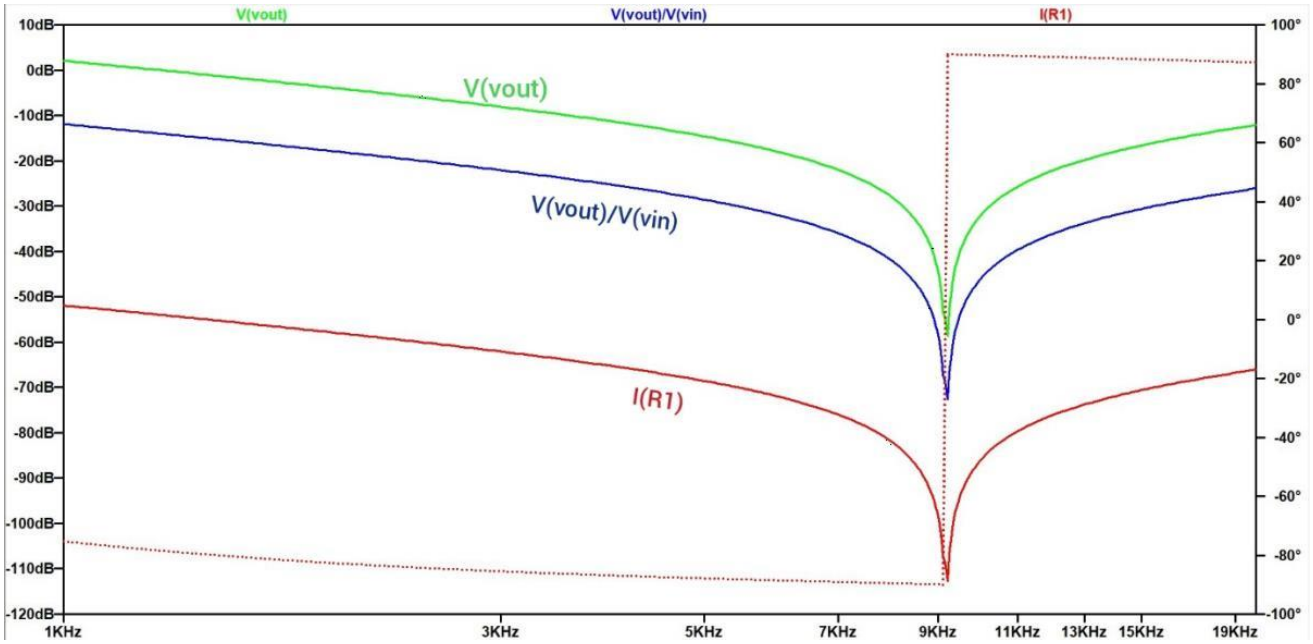


OUTPUT RESULTS:

Series Resonance circuit:



Parallel resonance circuit:



RESULT:

Thus the output waveforms of series and parallel resonance circuits were verified using LT SPICE simulation package.

Exp.No: **TRANSISTOR CHARACTERISTICS**

DATE:

Aim:

To obtain the input and output characteristics of a bipolar junction transistor using LT-SPICE simulation package.

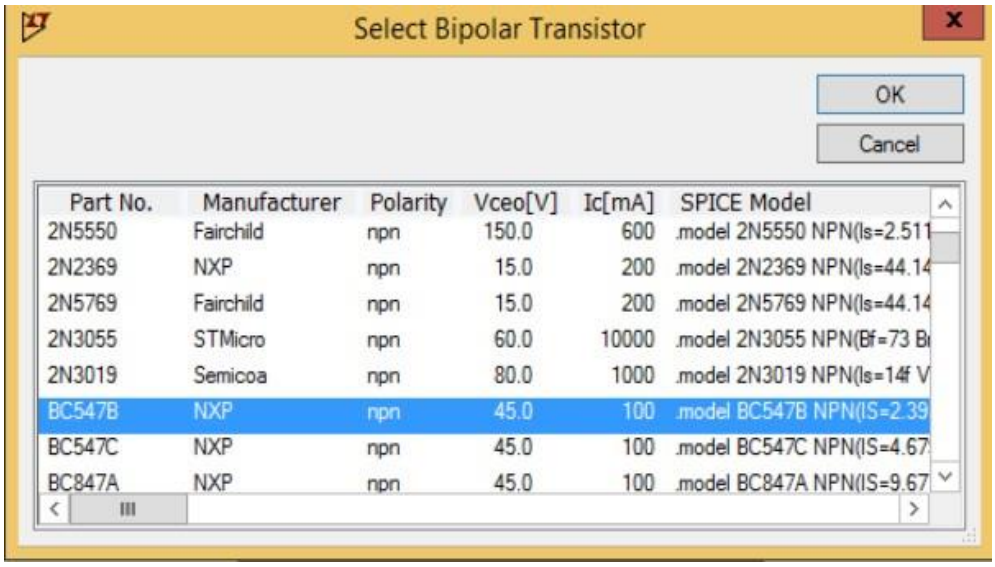
Tools Used: PC/Laptop loaded with LT-SPICE Version 17.

Keyboard shortcuts:

1. Component selection : F2
2. Connecting wire: F3
3. Diode : D
4. Ground : G
5. Resistor: R
6. Inductor: L
7. Capacitor: C

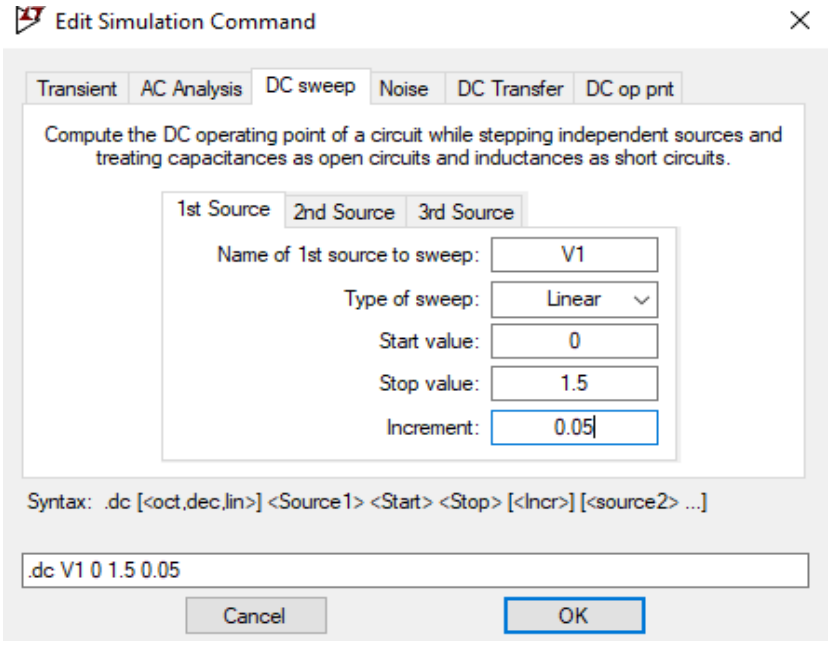
.**Procedure:**

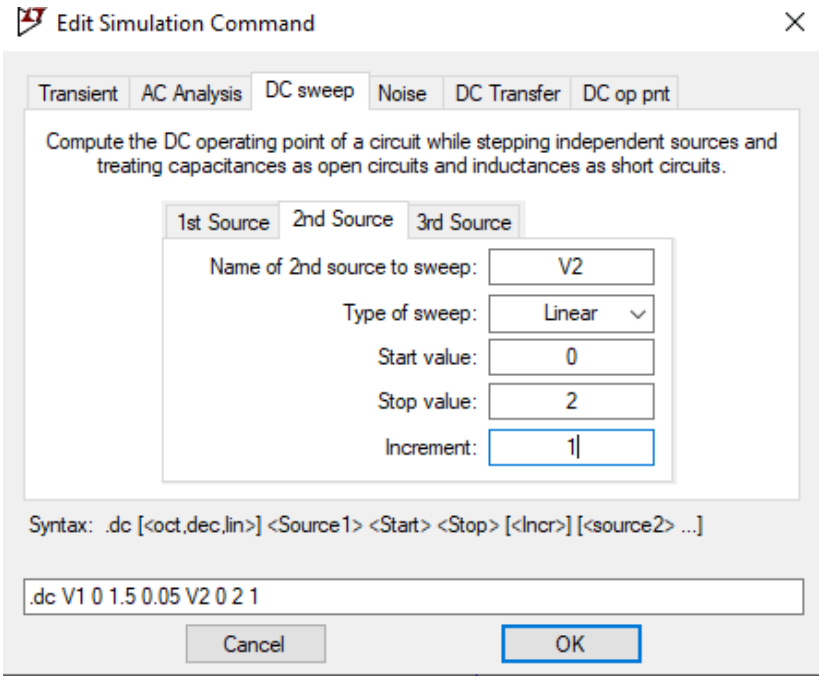
1. Open LTSpice software.
2. Start a new schematic design by clicking File->New schematic.
3. Place the components as per the given circuit to the new schematic page.



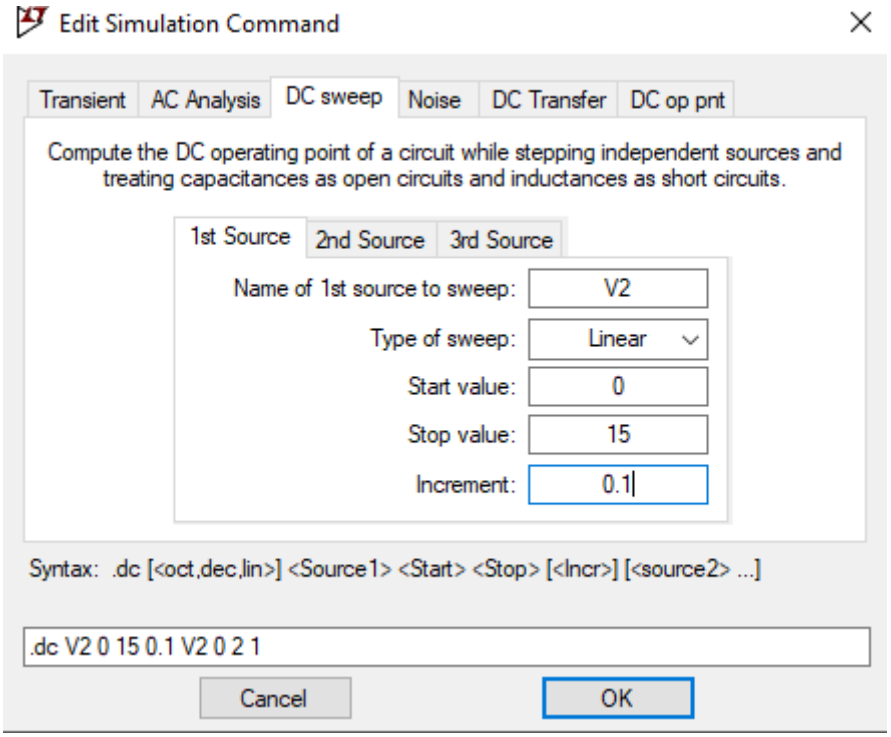
4. Save the schematic design inside a user created folder using File-> Save As.
5. Rearrange the components and connect the wires to complete the circuit drawing.
6. Change the values of the components.
7. If necessary, Rename the parts, and add a net name for every node.
8. Setup the simulation command by using simulate-> Edit simulation Cmd.
9. Select any one of the simulation types such as Transient, AC Analysis, DC Sweep or DC op pnt as per the circuit analysis needs.

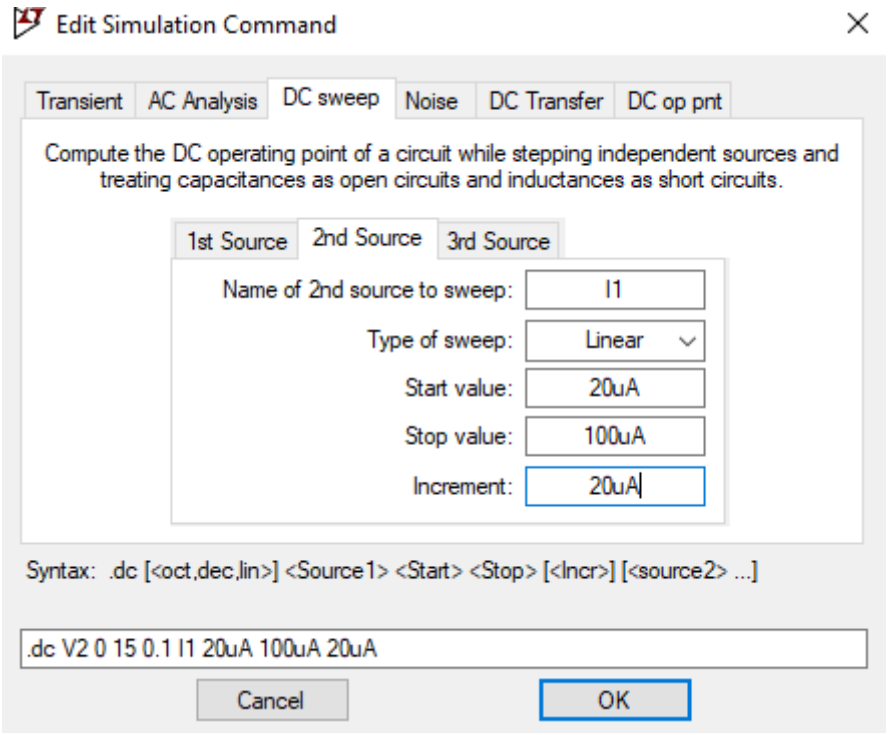
   For input characteristics:





For output characteristics:



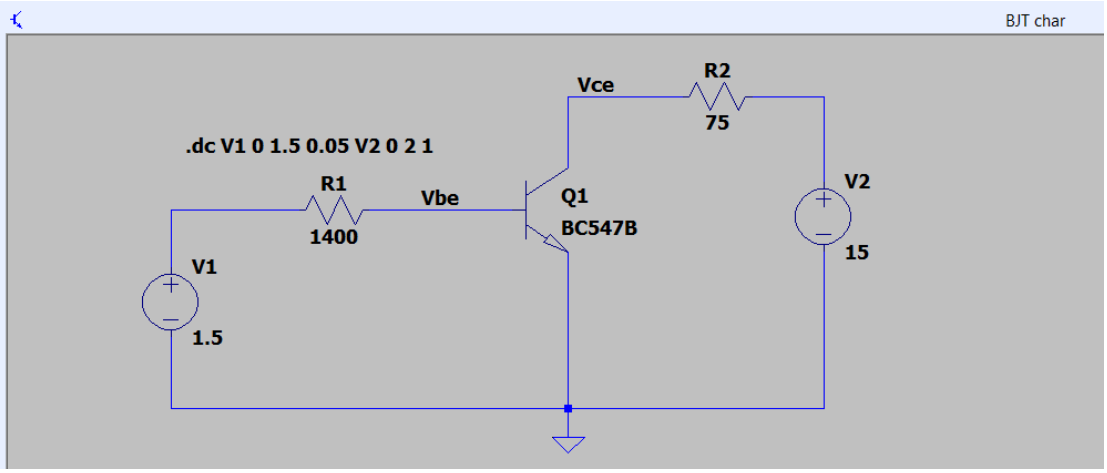


10. Perform simulation by selecting Run option.
11. Observe the input and output results.

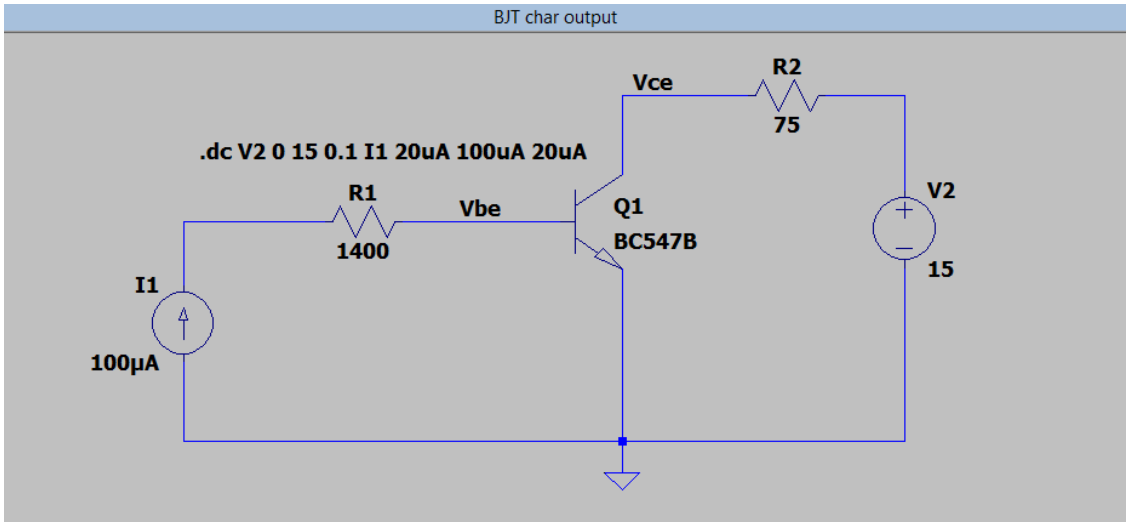
Transistor 1(BC547B):

Schematic circuit diagrams:

Input characteristics:

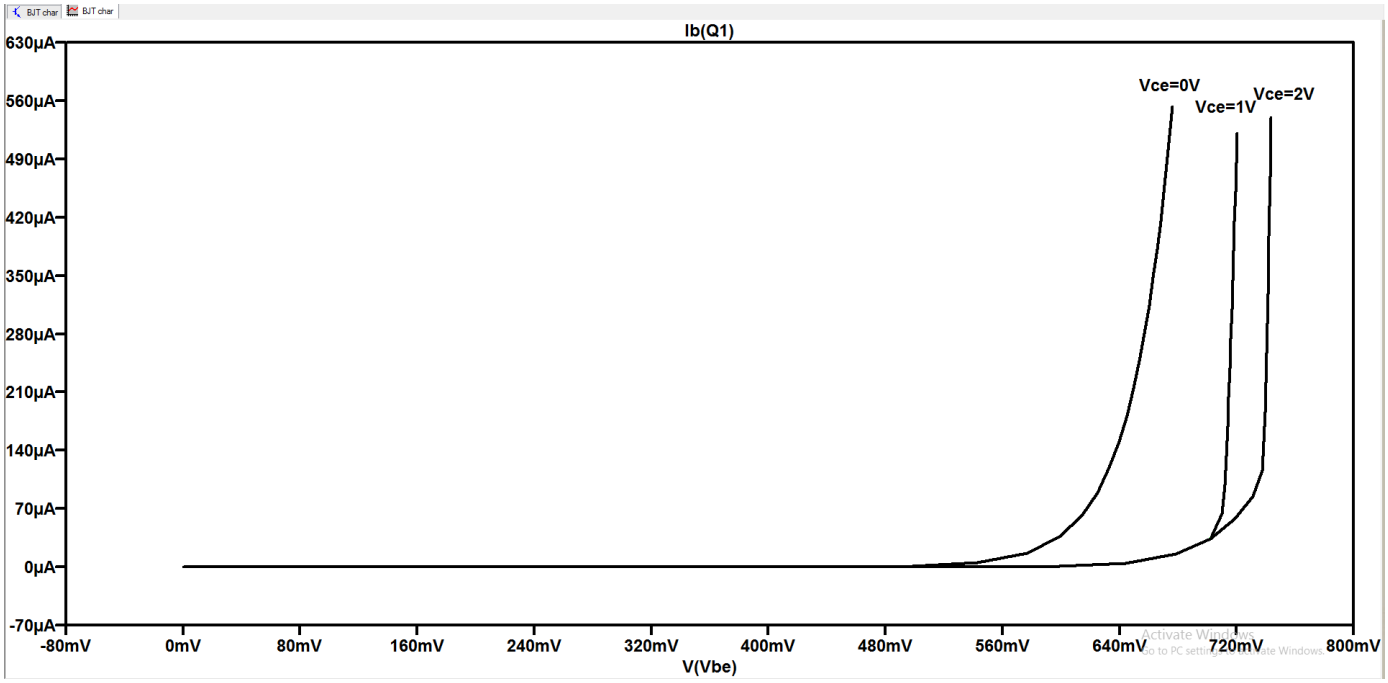


Output Characteristics:

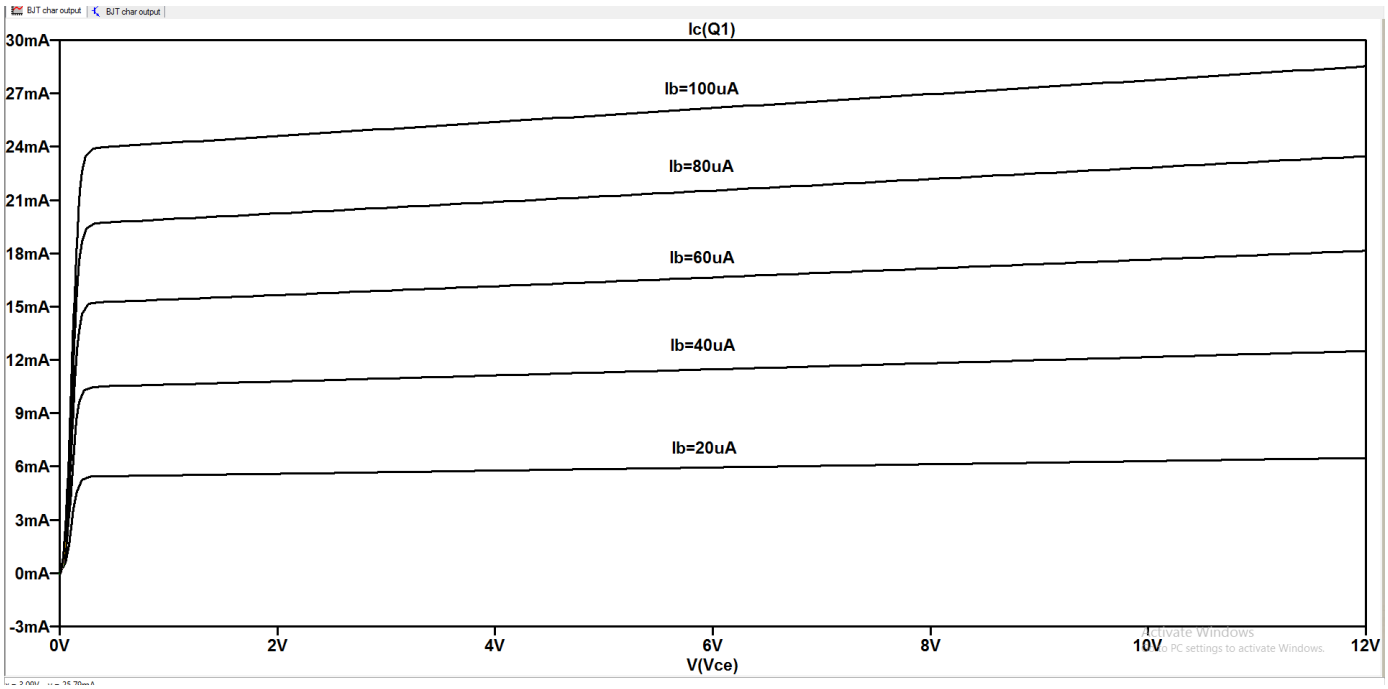


Output result:

Input Characteristics:



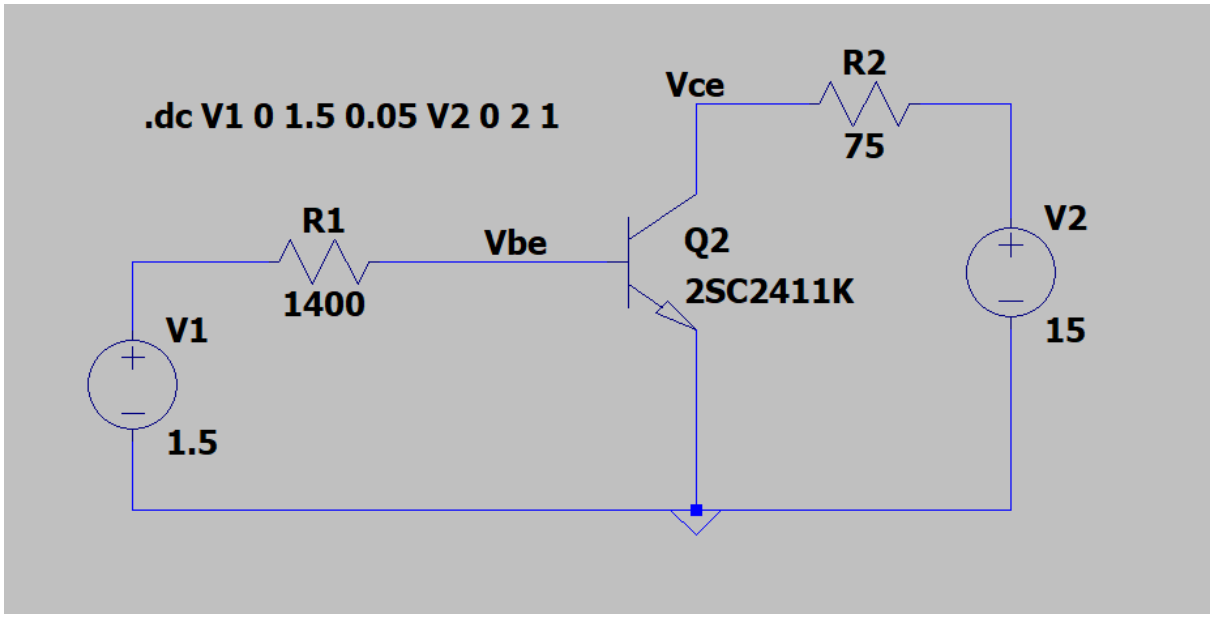
Output characteristics:



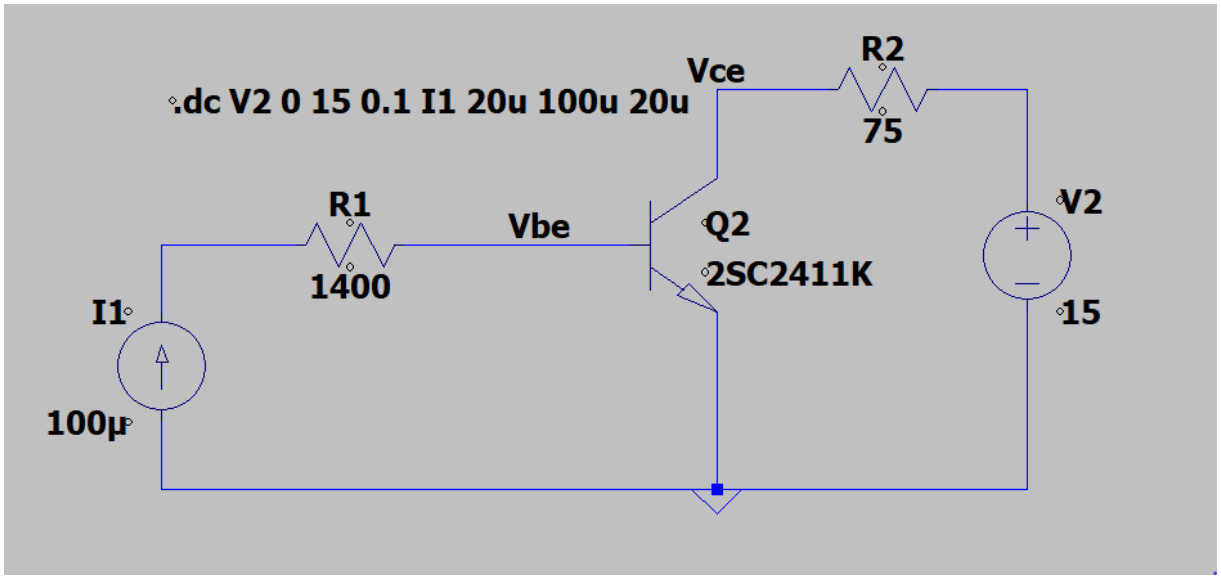
Transistor-2(2SC2411K):

Schematic Circuit Diagrams:

Input Characteristics:

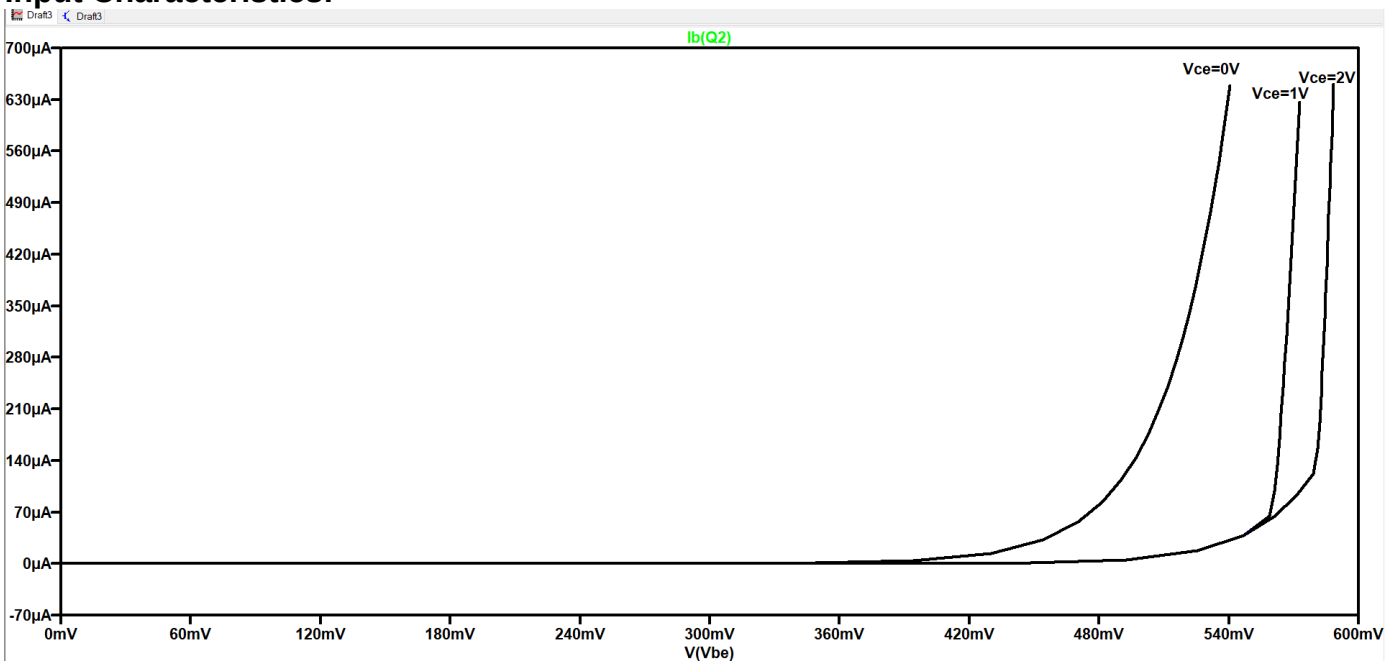


Output Characteristics:

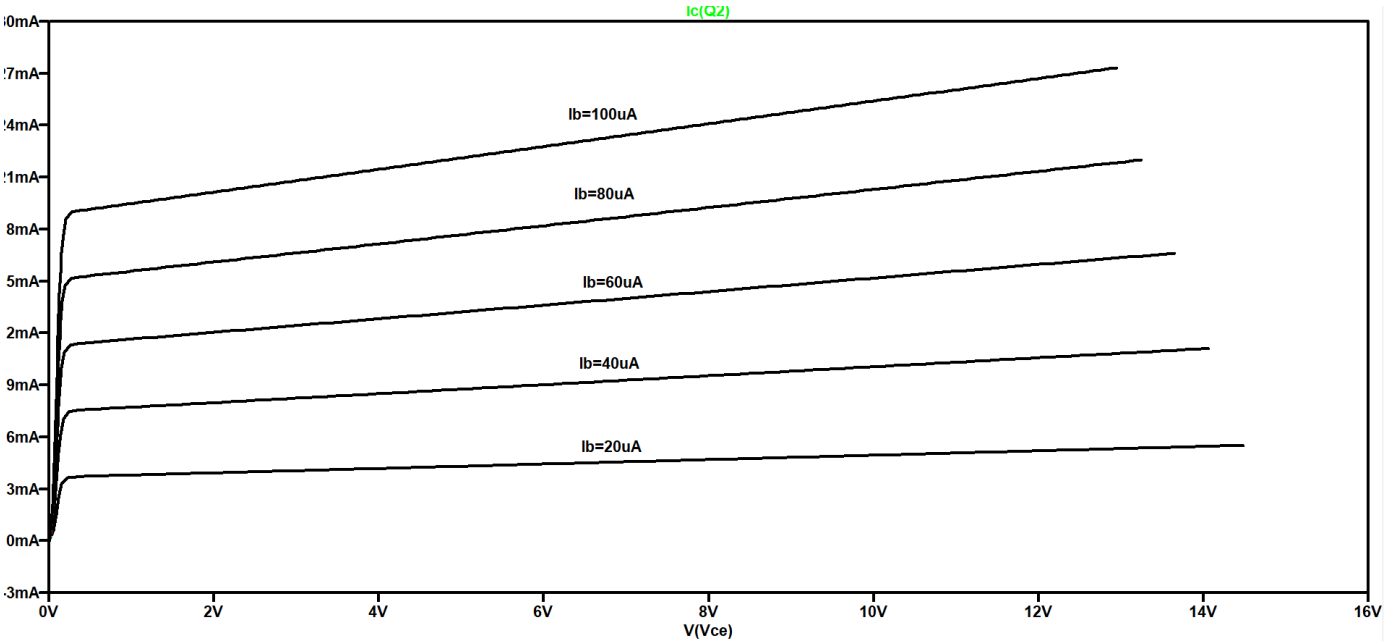


Output Result:

Input Characteristics:



Output Characteristics:



RESULT:

Thus the input and output characteristics of bipolar junction transistor is obtained using LT SPICE simulation package

EXP. NO:
DATE:

N-CHANNEL MOSFET OUTPUT AND TRANSFER CHARACTERISITCS

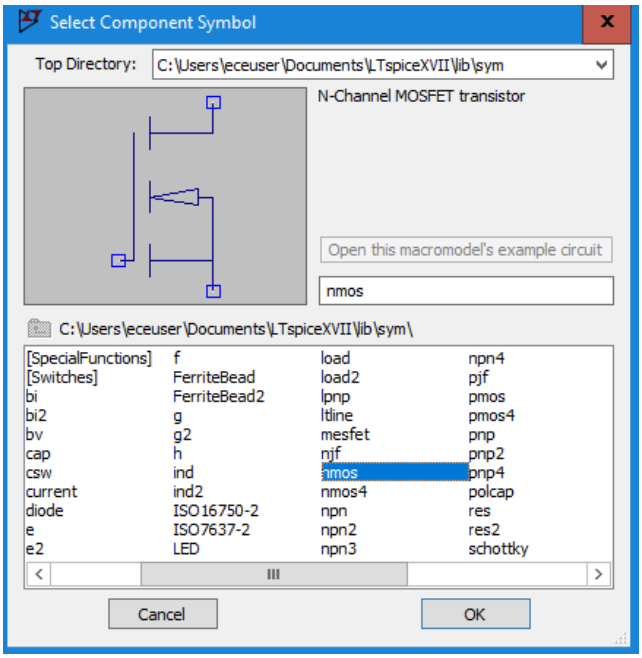
Aim:

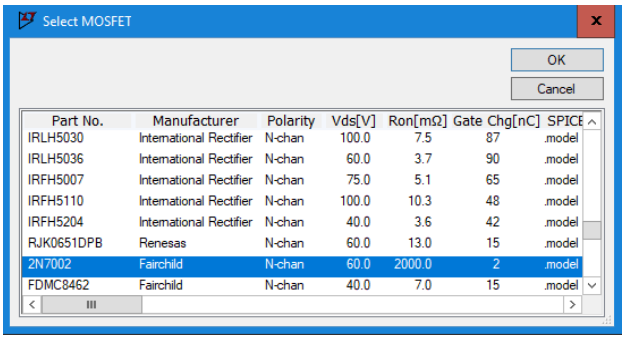
To study the transfer and output characteristics of an n-channel Metal Oxide Semiconductor Field Effect Transistor(MOSFET) in Common – Source Configuration using LT-SPICE simulation package.

Tools Used: PC/Laptop loaded with LT-SPICE.

Procedure:

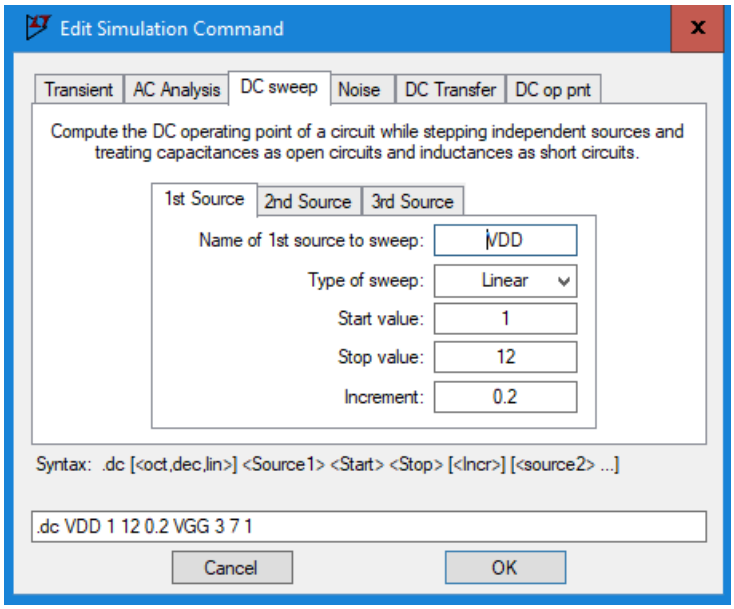
1. Open the Latest version of LTSpice software.
2. Start a new schematic design by clicking File->New schematic.
3. Place the components as per the given circuit to the new schematic page.

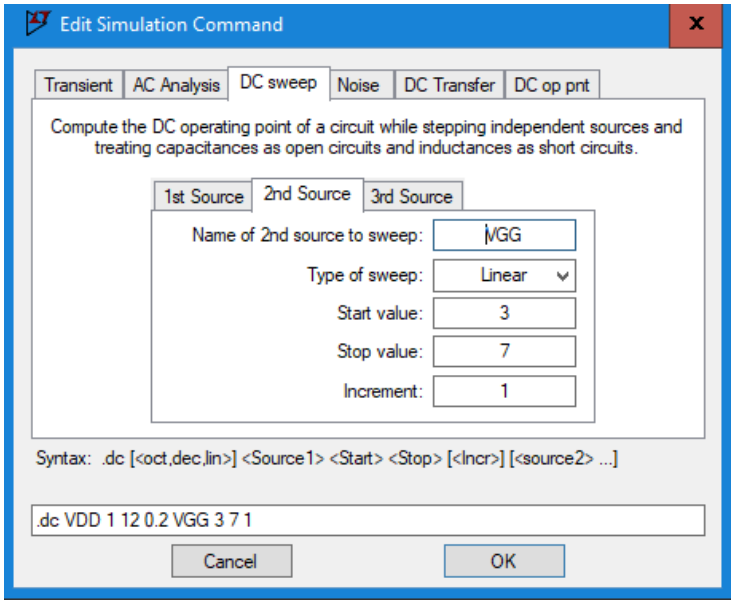




4. Save the schematic design inside a user created folder using File-> Save As.

5. Rearrange the components and connect the wires to complete the circuit drawing.
6. Change the values of the components.
7. If necessary, Rename the parts, and add a net name for every node.
8. Setup the simulation command by using simulate-> Edit simulation Cmd.
9. Select the simulation type DC Sweep.



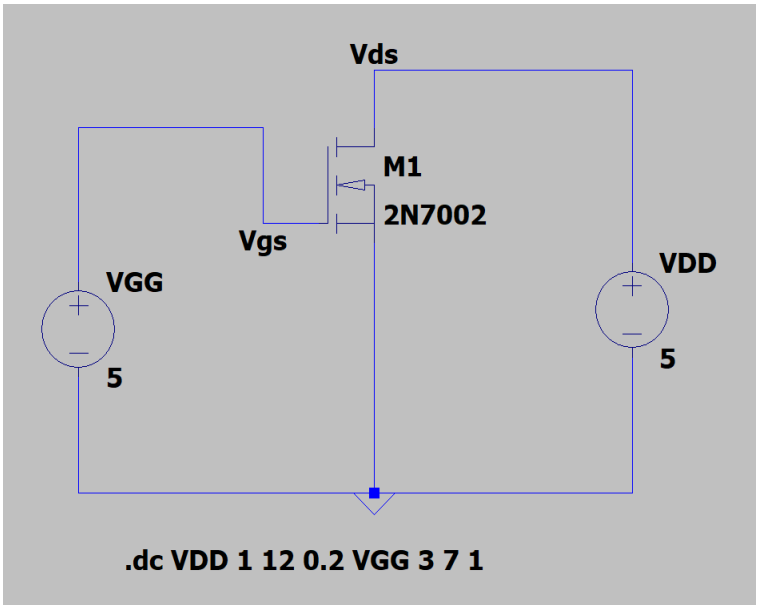


10. Perform simulation by selecting Run option.
11. Observe the input and output results.

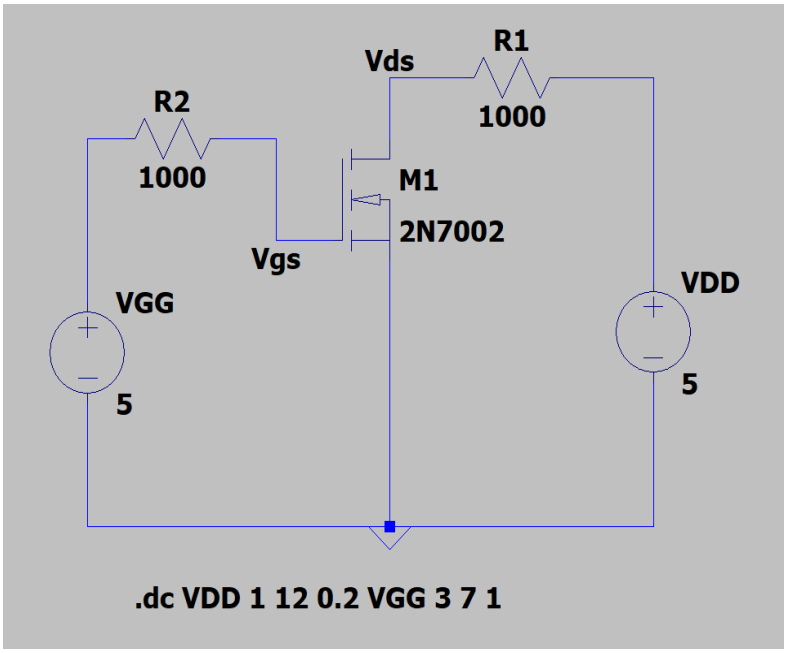
SCHEMATIC CIRCUIT DIAGRAMS

N-CHANNEL MOSFET

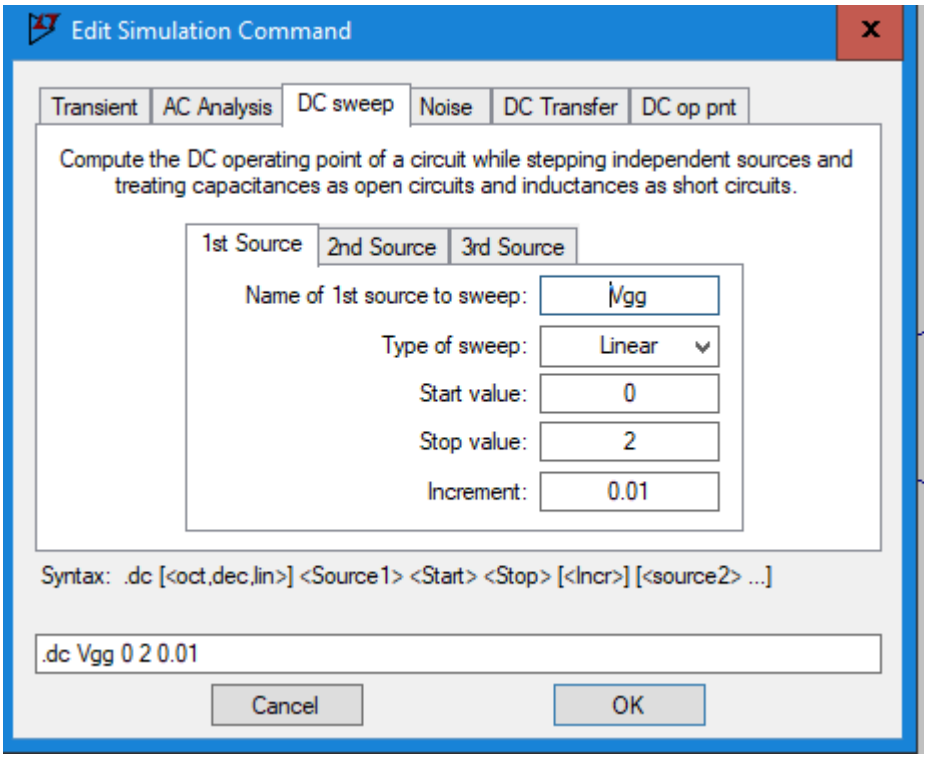
1. DRAIN CHARACTERISTICS

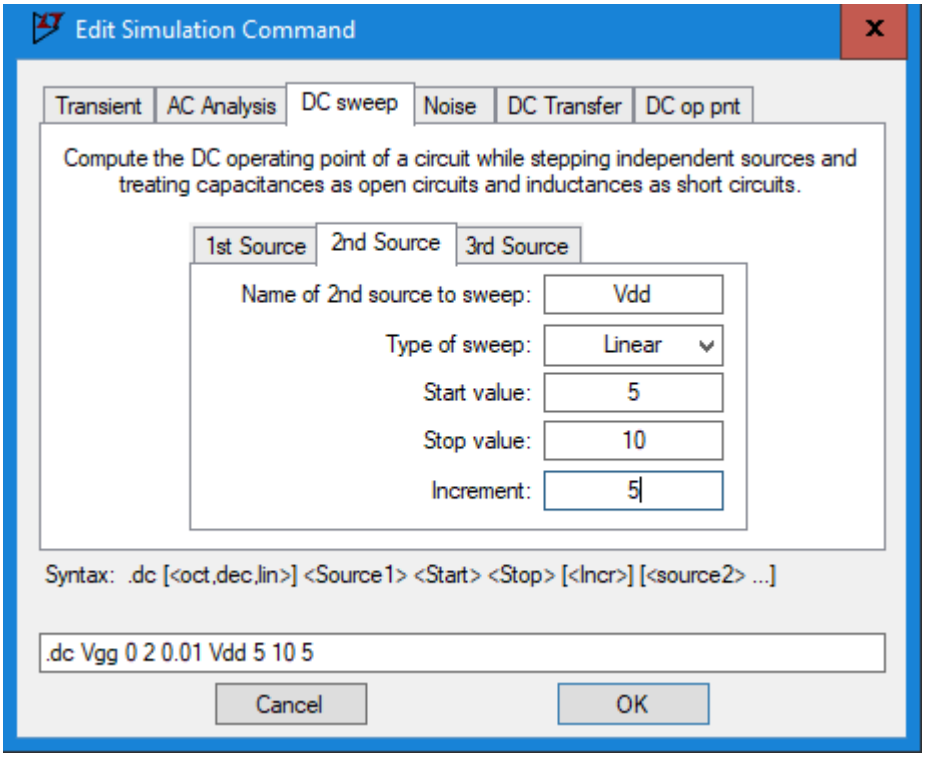


2. TRANSFER CHARACTERISTICS



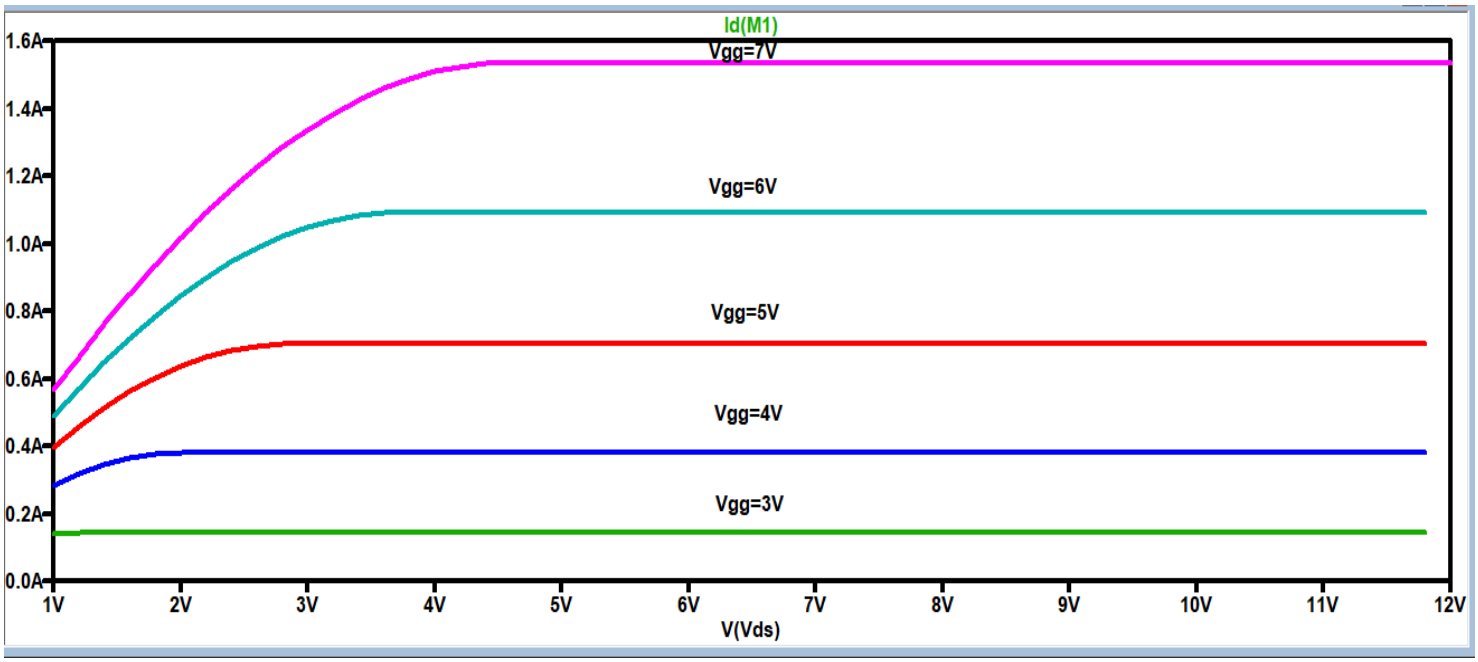
SIMULATION COMMANDS FOR TRANSFER CHARACTERISTICS



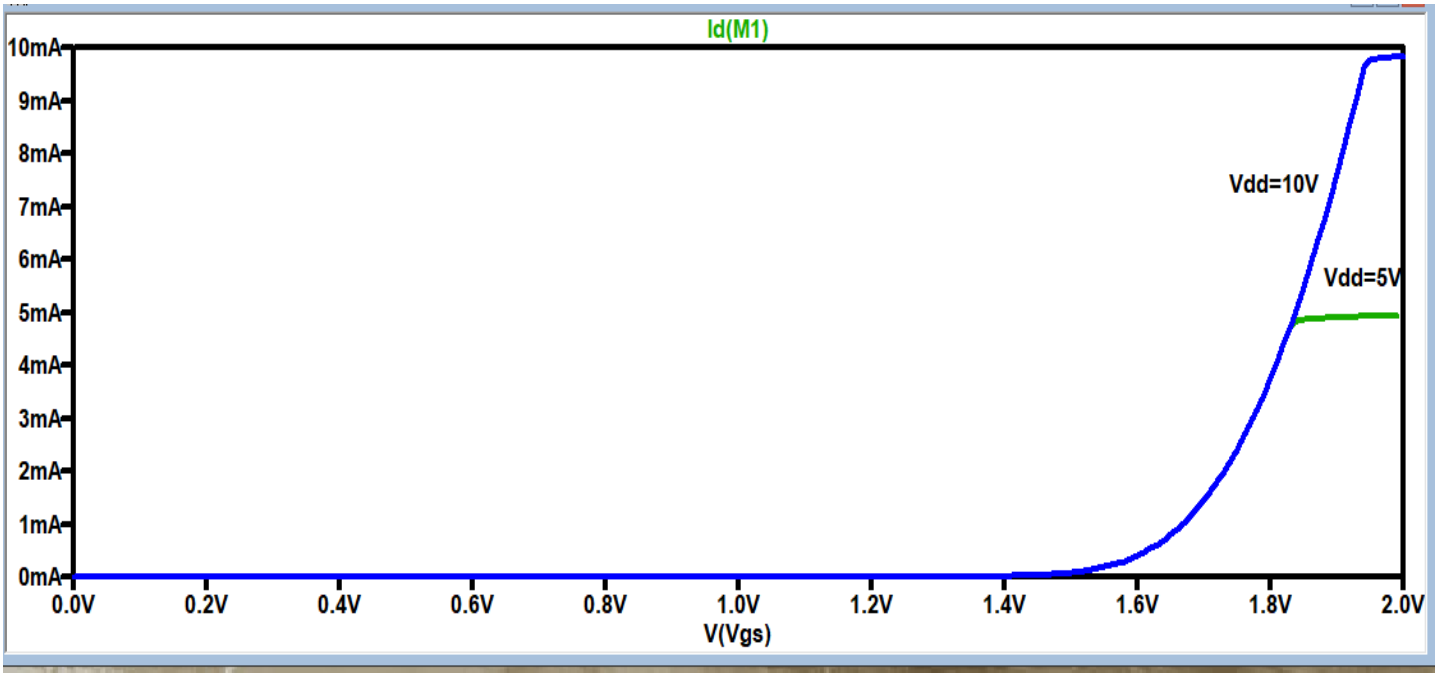


OUTPUT RESULTS

1. DRAIN CHARACTERISTICS OF N-CHANNEL MOSFET



2. TRANSFER CHARACTERISTICS OF N-CHANNEL MOSFET



Result:

Thus the transfer and output characteristics of an n-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in Common – Source Configuration is studied using LT-SPICE simulation package.