SRM INSTITUTE OF SCIENCE AND TECHNOLOGY
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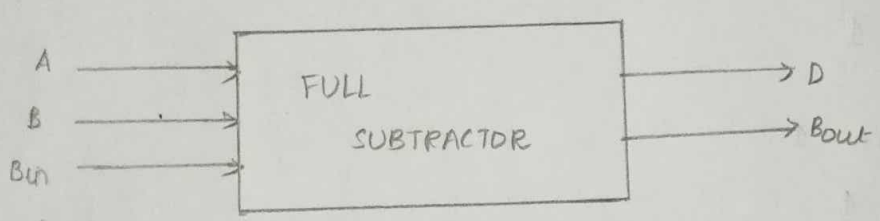
Q1. A, B, Bin, D and Bout are respectively the minuend, the subtrahend, the BORROW-IN, the DIFFERENCE output and the Borrow out in the case of full subtractor. Determine the bit status of D and Bout for the following values of A, B and Bin

Block diagram:

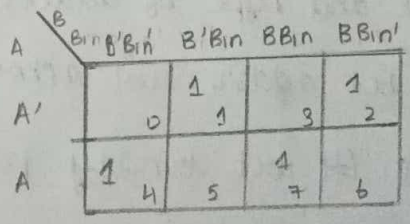


Truth table for full subtractor

Deci	A	B	Bin	D	Bout
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

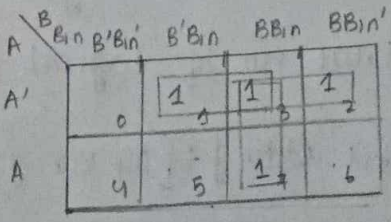
K-MAP

i) Difference



$D = AB'B'in + A'B'Bin + ABBin + ABB'in$

ii) Borrow out



$Bout = A'Bin + A'B + BBin$

$Bout = A'B + Bin(A'+B)$

a) A = 0 ; B = 1 ; B_{in} = 1

D = 0 ; B_{out} = 1

b) A = 1 ; B = 1 ; B_{in} = 0

D = 0 ; B_{out} = 0

c) A = 1 ; B = 1 ; B_{in} = 1

D = 1 ; B_{Out} = 1

d) A = 0 ; B = 0 ; B_{in} = 1

D = 1 ; B_{out} = 1

2) Determine the number of half and full adder circuit blocks required to construct a 64 bit binary parellel adder. Also, determine the number and type of additional logic gates needed to transform this 64 bit adder subtractor

i) An 64 bit binary parellel adder requires 1 half adder and 63 full adder

ii) To transform a 64 bit adder into a 64 bit adder subtractor we need to add 64 XOR gate and 64 AND gate.

- XOR and AND gate = 64
- Total no of logical gate = 128

[64 bit adder] + [64 XOR gate] + [64 AND gate] = 64 bit adder subtractor

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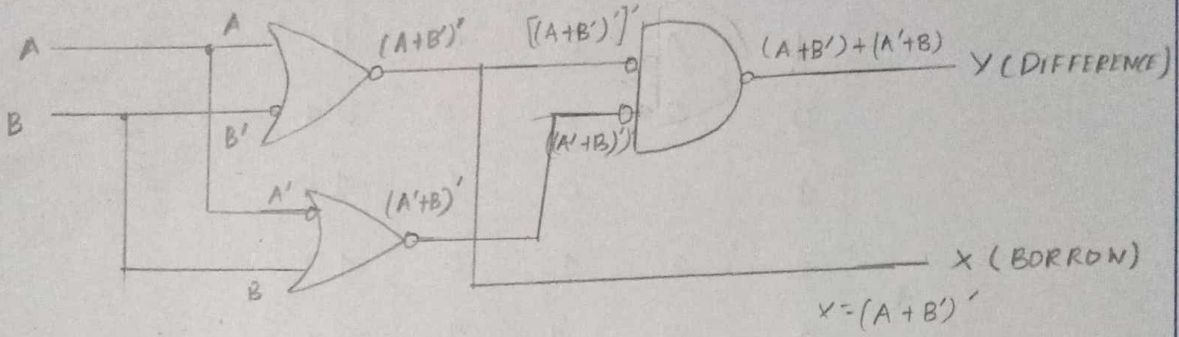
3) Prove that the logic diagram from the figure performs the function of a half-subtractor provided that Y represents the DIFFERENCE output and X- represent the BORROW output

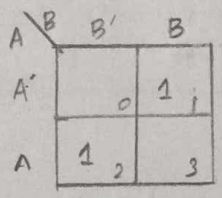


TRUTH TABLE

A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-MAP

A) DIFFERENCE



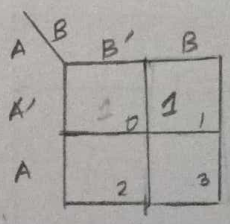
$Y = A'B + AB'$

$Y = A \oplus B$

For Borrow → $A'B$

For Difference → $A \oplus B$

B) BORROW



$X = A'B$

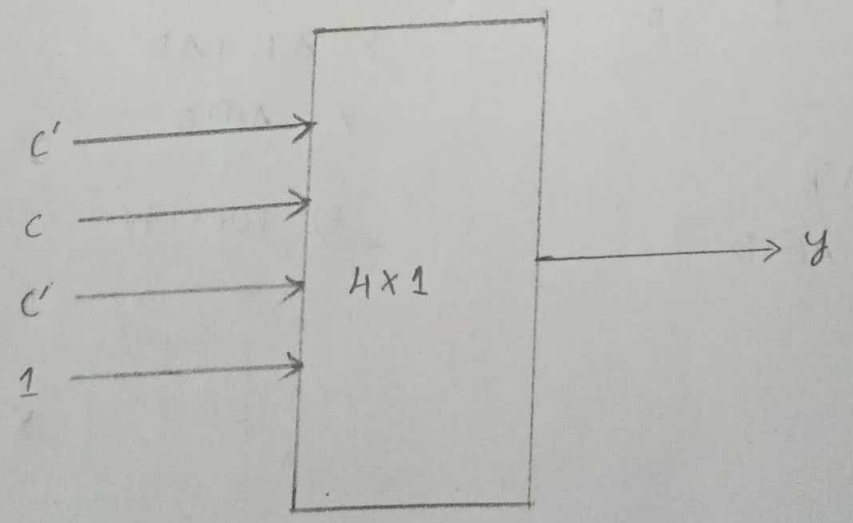
Furom the above logic diagram, it is clear that $y = A \oplus B$ which is EX-OR and x is A'B (AND gate).

Hence it is proved.

4) Implement the Boolean function with a suitable multiplexer

$f(A, B, C) = \pi(1, 2, 3)$

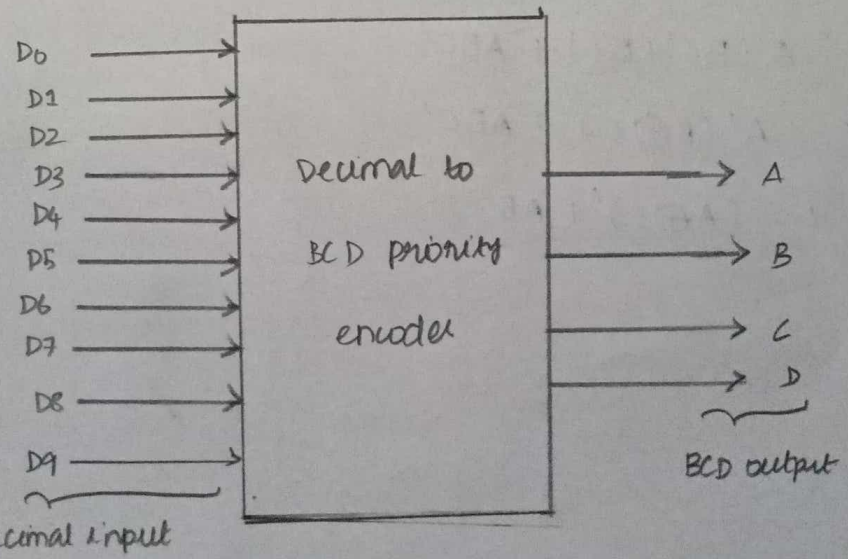
D	A	B	C	y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1



4x1 Multiplexer

Q5. Design a 10 line decimal to BCD priority encoder:

D	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	A	B	C	D
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	x	1	0	0	0	0	0	0	0	0	0	0	0	1
2	x	x	1	0	0	0	0	0	0	0	0	0	1	0
3	x	x	x	1	0	0	0	0	0	0	0	0	1	1
4	x	x	x	x	1	0	0	0	0	0	0	1	0	0
5	x	x	x	x	x	1	0	0	0	0	0	1	0	1
6	x	x	x	x	x	x	1	0	0	0	0	1	1	0
7	x	x	x	x	x	x	x	1	0	0	0	1	1	1
8	x	x	x	x	x	x	x	x	1	0	1	0	0	0
9	x	x	x	x	x	x	x	x	x	1	1	0	0	1



6) A combinational circuit is defined by $F = \Sigma(0, 2, 5, 6, 7)$ Hardware implement the Boolean function F with a suitable decoder and an external OR/NOR gate having the minimum number of inputs

D	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

$Y = A'B'C' + A'BC' + AB'C + ABC' + ABC$

$y = A'C'(B'+B) + ABC(C'+C) + AB'C$

$Y = A'C' + AB + AB'C$

$\boxed{Y = A'C' + A(B+B'C)}$

$Y = A'B'C' + A'(BC'+B'C) + ABC' + ABC$

$Y = A'(BC'+B'C) + ABC'$

$Y = A'(B \oplus C) + ABC'$

$\boxed{Y = (A \oplus C)' + AB}$