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SUB : DIGITAL LOGIC DESIGN

DEPARTMENT : B.TECH. ECE

ASSIGNMENT - II

1. A, B, B_{in}, D and B_{out} are respectively the minuend, the subtrahend, the BORROW-IN, the difference output and the BORROW-OUT in the case of a full subractor. Determine the bit status of D and B_{out} for the following values of A, B and B_{in}

(a) A = 0, B = 1, B_{in} = 1 (b) A = 1, B = 1, B_{in} = 0

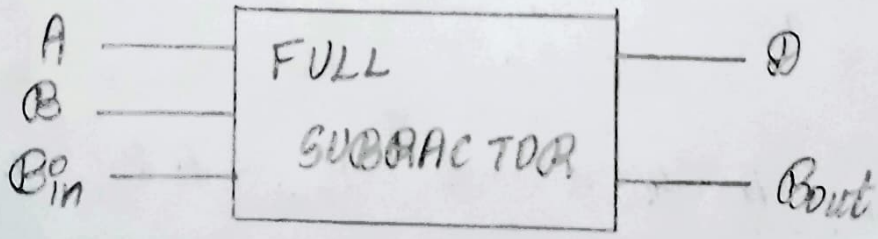
(c) A = 1, B = 1, B_{in} = 1 (d) A = 0, B = 0, B_{in} = 1

Ans: Design of full subractor

(i) Problem statement:

FULL Substractor

(ii) Block diagram

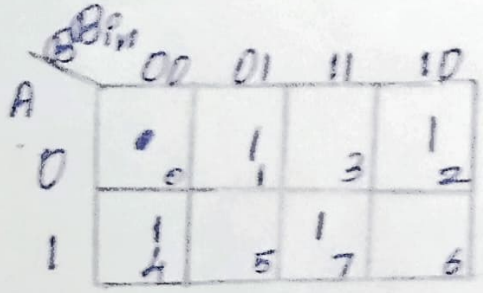


iii) Truth table

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

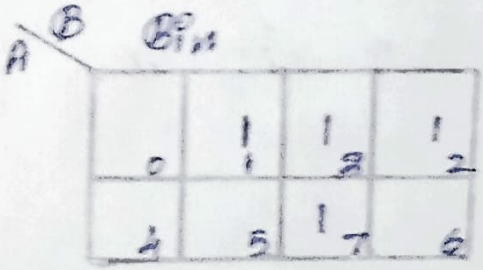
iv) IC - MAP

For Difference



$D = AB'B_{in} + A'B'B_{in} + AB B_{in} + A'B B_{in}$

For Borrow



$B_{out} = A'B_{in} + A'B + B B_{in}$

$= B_{in}(A' + B) + A'B$

(a) $A=0$, $B=1$, $B_{in}=1 \Rightarrow D=0$; $B_{out}=1$

(b) $A=1$, $B=1$, $B_{in}=0 \Rightarrow D=0$; $B_{out}=0$

(c) $A=1$, $B=1$, $B_{in}=1 \Rightarrow D=1$; $B_{out}=1$

(d) $A=0$, $B=0$, $B_{in}=1 \Rightarrow D=1$; $B_{out}=1$

2. Determine the number of half and full adder circuits blocks required to construct a 64-bit binary parallel adder. Also, determine the number and type of additional logic gates needed to transform this 64-bit adder into a 64-bit adder-subractor.

Ans:

For 64 bit:

Half adder = 1; Full adder = 63

For 64 bit adder-subracter-

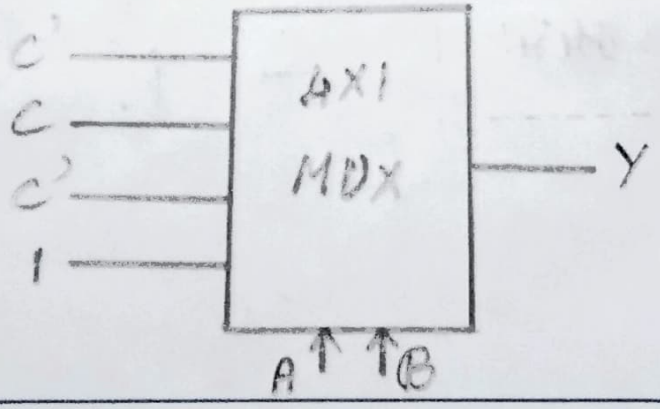
No. of additional logic gates = 64 + 64 = 128 gates

Types of additional logic gates = XOR & AND gate

* From the above logic diagram. It is seen that Y (DIFFERENCE) is A ⊕ B that is EX-OR and X (BORROW) is A'B (AND GATE).

4. Implement the Boolean function with a suitable multiplexer $f(A,B,C) = \Pi(1,2,5)$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



$$Y = A'B'C' + A'BC' + AB'C + ABC' + ABC$$

$$= A'C'(B'+B) + AB(C'+C) + AB'C$$

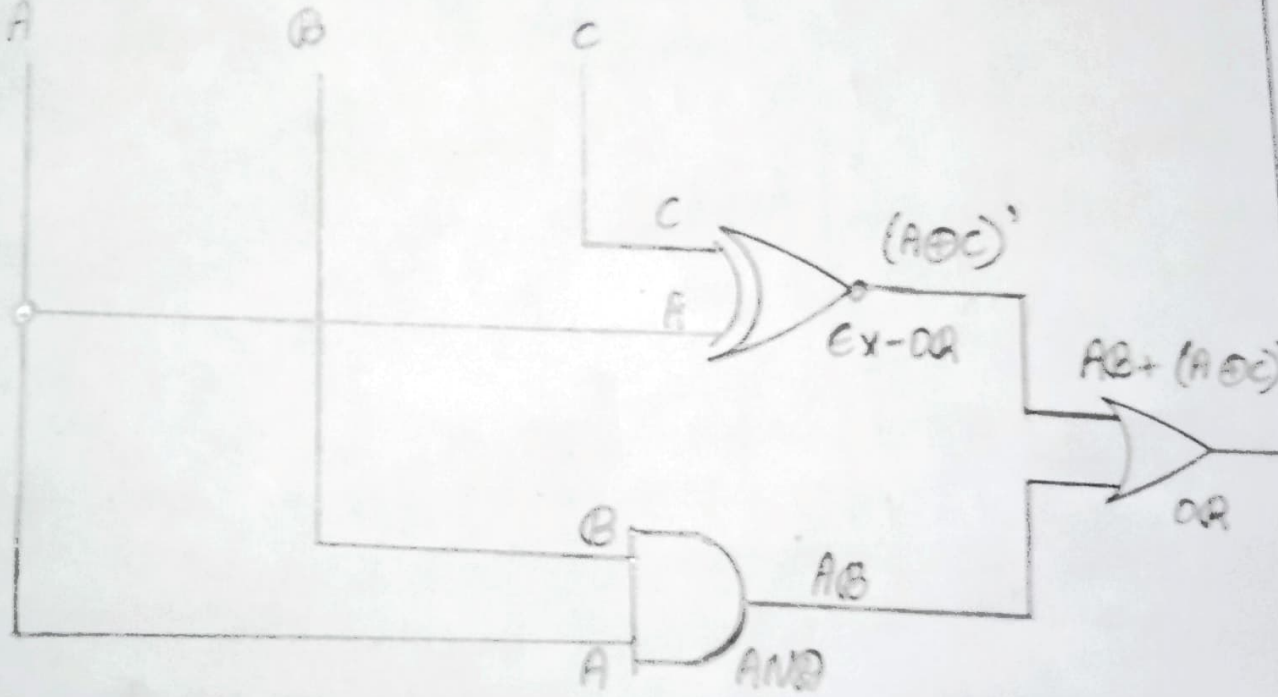
$$= A'C' + AB + AB'C$$

$$= A'C' + A(B+B'+C)$$

$$= A'C' + A(B+C)$$

$$= A'C' + AB + AC$$

$$= (A \oplus C) + AB$$



6. A combinational circuit is defined by $F = \Sigma(0,2,5,6,7)$. Hardware implement the Boolean functions F with a suitable decoder and an external OR/NOR gate having the minimum number of inputs.

Ans:

A	B	C	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1