Workshop Outline

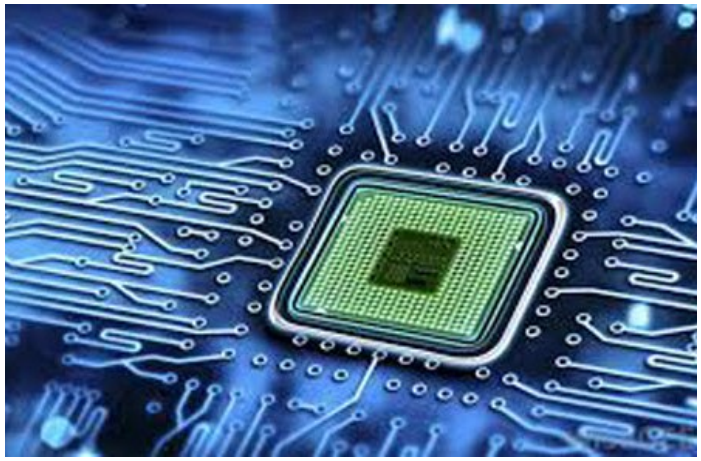
Contents

- Basic of single stage amplifiers and its biasing
- Multistage and differential amplifier design
- Frequency response of amplifiers
- Feedback in amplifiers
- Bandgap references
- PLL

- **Hands-on**
  - Introduction to commercial EDA tools
  - Design and simulation of a 2 stage operational transcon-ductance amplifier
  - Layout design techniques
  - Parasitic extraction
  - Post layout simulation

Objective

The objective of this workshop is typically to impart practical knowledge and skills related to designing, analyzing, and troubleshooting analog electronic circuits. Participants would be able to learn fundamental concepts, circuit topologies and techniques to design circuit from Schematic to GDS-II .



IIT Guwahati
in association with
Ministry of Electronics and Information

ELECTRONICS INDIA
Billion Needs Million Chips

Workshop on "Insights to the Art of Analog Design"

12th – 16th Feb 2024
Conference Hall 3,
Indian Institute of Technology Guwahati

Website:
https://www.iitg.ac.in/proj/ninelabs/analogworkshop/index.html

Contact:
For queries related to accommodation:
Mr. Ravi Dubey
Contact No.: 9893112942/8651976428
For queries related to registration:
Email: piaipgcmeity@iitg.ac.in/ ninelabsIIT@gmail.com
Landline No.:0361-258-3182
Time to contact : 9.00 AM to 6.00 PM

Tentative Speakers

Keynote Speaker

Ms. Sunita Verma

Scientist-G, Meity

Invited Speakers

Prof. Anand Bulusu, IIT Roorkee

Dr. Vinayak Hande, Infineon Tech., Austria

Mr. Nishit Gupta, Scientist-E, MeitY

Dr. Sharayu Jagtap, TUSK IC, Belgium

Outcomes

The workshop on Commercial EDA Design tool for Analog Design, is organized to bring together researchers, developers, and users to discuss advancements, share knowledge, and collaborate on commercial tools for chip design. After completion of this workshop, participants would be able to design analog circuits through VLSI backend flow.

Who can apply?

Students, researchers, faculty members and industry professionals working in the domain of Analog VLSI Design

Participants willing to attend the workshop in the offline mode need to register as early as possible to get on-campus hostel accommodation.

HOW TO APPLY ?

Fees: Student/Research Scholar/Other: Rs. 500

Faculty Member/Industry professional: Rs.1000

Form QR code

For NEFT:

Bank Name: State Bank of India

A/C Name: IIT Guwahati (R&D)

Account No.: 36071160089

IFSC Code: SBIN0014262

Reg. Link: https://forms.gle/GNYfo2nGmr1S1E6X9

Note: Participants have to submit UTR No. as the proof of payment while registering to the workshop.

DETAILS

Workshop Duration: 5 Days

Last Date: 10th Feb 2024

Workshop Mode: Hybrid (Online + Offline)

It is recommended that participants should carry their own laptop having min. 08 GB RAM and Core i3 Processor

Accommodation and food would be made available only for the offline participants.

Organizing Committee

Prof. Mahima Arrawatia (Convenor)

Prof. Harshal B. Nemade (Co-Convenor)

Prof. Gaurav Trivedi (Co-Convenor)

Prof. Aryabartta Sahu

Prof. Prithwijit Guha

Prof. S. Krishnaswamy

Prof. H. S. Shekhawat

Prof. Pratima Agarwal

Prof. John Jose

Prof. Rohit Sinha

Prof. Sukumar Nandi

Volunteers

Rupali Jarwal, Amol Boke, Feroza Haque, Nilutpal Changkakati, Naorem Yaipharenba Meitei, Vikash Prasad, Shailesh Chandra Pandey, Raktim Choudhury, Tina Susan Thomas, Taniya Salotra, Avula Manoj Kumar Reddy, Rushik Parmar, Divya Nakerakanti, Andrew Roobert, Abhyuday Bhardwaj, Akash Dev, Roshan Saras Mani Mishra, Bipul Boro, Parmita Roy, S.S.P. Goswami, Subhadip Poria, Aditi Chakraborty, Nitin M., Sachin Kumar