Solve the following questions for Week 9.

There are 10 questions, for a total of 20 marks.

- 1. (2 marks) For an ideal p-type Depletion MOSFET, choose the correct statement.
 - A. A hole inversion layer is created for an applied bias greater than threshold voltage.
 - B. An electron inversion layer is created for an applied bias greater than threshold voltage.
 - C. A hole inversion layer exists for zero applied bias.
 - D. A hole inversion layer is created for an applied bias less than threshold voltage
 - E. An electron inversion layer exists for zero applied bias.
 - F. An electron inversion layer is created for an applied bias less than threshold voltage
- 2. (2 marks) Consider an n-channel MOSFET with the following parameters: $\kappa = 1 \ mA/V^2$, W/L = 8, and $V_T = 0.4 \ V$. The drain current I_D for $V_{GS} = 0.9 \ V$ and $V_{DS} = 1 \ V$ is ______ (Hint: You are given κ (not κ' !)

 A. $1 \ mA$ So MOSFET operates in saturation sugar E. $1 \ \mu A$ C. $0 \ mA$ D. $0.125 \ \mu A$ $= \frac{1}{2} \left(0.5\right)^2$
 - E. $0.125 \ mA$ F. $1.125 \ mA$
- 3. (2 marks) Consider an ideal long channel n-MOSFET with the following parameters: $\mu_n C_{ox} = 0.18~mA~V^{-2},~W/L = 8,~and~V_T = 0.4~V$. The drain current I_D for $V_{GS} = 0.8~V$ and $V_{DS} = 0.1~V$ is

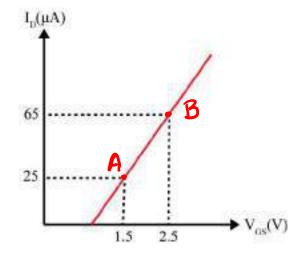
(For Q3-Q4) Answer the following with regards to the subthreshold swing of a MOSFET:

4. (2 marks) The subthreshold swing is defined as:

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- A. The increase in gate voltage necessary to increase the drain current by a factor of 2.
- B. The increase in source voltage necessary to increase the drain current by a factor of 2.
- C. The increase in drain voltage necessary to increase the drain current by a factor of 10.
- D. The increase in drain voltage necessary to increase the drain current by a factor of 2.
- E. The increase in gate voltage necessary to increase the drain current by a factor of 10.
- 5. (2 marks) What is the minimum subthreshold swing of a classical MOSFET (in $mV\ decade^{-1}$) at T=300K?
 - A. 30
 - **B.** 60
 - C. 120
 - D. 26
 - E. 150

(For Q6-Q7) The I_D vs V_{GS} characteristics determined experimentally for an n-channel MOSFET are given below. The width and length of this device is $10~\mu m$ and $1~\mu m$ respectively. Assuming the drain voltage $V_{DS}=0.1~V$, and oxide capacitance $C_{ox}=8\times 10^{-8}~Fcm^{-2}$,



- 6. (2 marks) the mobility of carriers in the inversion region is $\underline{}$ $cm^2 (V-s)^{-1}$ (rounded off to the nearest integer)
 - A. 250
 - **B.** 500

C. 5000 MOSFET is in linear regime.

D. 1450
$$I_0 = \frac{J_n(o_n W)}{2L} \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2 \right]$$

E. 450 At point A, $I_0 = 25 \text{ MA}$ & $V_{GS} = 1.5 \text{ V}$
 $25 \times 10^{-6} = \frac{J_n \times 8 \times 10^{-8} \times 10}{2.5 \times 10^{-6}} \left[2(1.5 - V_T) \cdot 0.1 - 0.1^2 \right]$
 $25 \times 10^{-6} = \frac{J_n \times 8 \times 10^{-8} \times 10}{4.4 \times 10^{-7}} \left[0.3 - 0.2 V_T - 0.01 \right]$

At point B, $I_0 = 65 \text{ MA}$ & $V_{GS} = 2.5 \text{ V}$
 $65 \times 10^{-6} = \frac{J_n \cdot 8 \times 10^{-8} \times 10}{4.4 \times 10^{-7}} \left[0.5 - 0.2 V_T - 0.01 \right]$
 $650 = 0.49 - 0.2 V_T$
 $650 = 0.49 - 0.2 V$

- 7. (2 marks) The threshold voltage for the MOSFET is _____ V. (Hint: Ignore $\frac{V_{DS}^2}{2}$ term for calculating V_T)
 - A. 0.8
 - **B.** 0.875
 - C. 0.75
 - D. 0.32
 - E. 0.625
 - Ignoring $\frac{V_{DS}^{2}}{2}$ them, (wount is given as $I_{D} = \frac{\mu_{h}(0xW)}{L} \left[(V_{4S} V_{T}) V_{PS} \right]$ $25 \times 10^{-6} = 500 \times 8 \times 10^{-8} \times 10 \left[(1.5 V_{T}) 0.1 \right]$ $\frac{25 \times 10^{-6}}{4 \times 10^{-4}} = 0.15 0.1V_{T}$ $0.1V_{T} = 0.0875$ $V_{T} = 0.875 V$

- 8. (2 marks) Given below are two statements regarding I_D in conventional PMOS and NMOS devices.
 - S1: Drain current for a PMOS device $(I_{D,PMOS})<$ Drain current for a NMOS device $(I_{D,NMOS})$ for a particular V_{GS}
 - S2: Mobility of a PMOS device (μ_P) < Mobility of an NMOS device (μ_N) at the interface
 - A. Statement S1 is true and S2 is false
 - B. Statement S1 is false and S2 is true
 - C. Statement S1 is true and S2 is true and S2 is the correct explanation of S1
 - D. Statement S1 is true and S2 is true and S2 is not the correct explanation of S1
 - E. Statement S1 and S2 are false
- 9. (2 marks) Given below are two statements regarding substrate bias in PMOSFET.
 - S1: Source-to-body bias V_{SB} must always be lesser than or equal to zero for a PMOSFET.
 - S2: The source-to-substrate pn junction must be either grounded or reverse biased for normal transistor action.
 - A. Statement S1 is true and S2 is false
 - B. Statement S1 is false and S2 is true
 - C. Statement S1 is true and S2 is true and S2 is not the correct explanation of S1
 - D. Statement S1 and S2 are false
 - E. Statement S1 is true and S2 is true and S2 is the correct explanation of S1

Gate Previous Year Question

10. (2 marks) (EC-GATE 2014) The slope of the I_D vs V_{GS} curve of an n-channel MOSFET in linear region is $0.02~\Omega^{-1}$ at $V_{DS}=0.1~V$. For the same device, neglecting channel length modulation, the slope of the $\sqrt{I_D}$ vs V_{GS} curve $(in \sqrt{A}/V)$ under saturation is approximately _____ (rounded off to one decimal place)

Ans:
$$0.316$$
Range: $0.3-0.4$
 $I_{DS} = K_{N} \left((V_{45} - V_{7}) V_{DS} \right)$, where $K_{A} = M \frac{1}{N} \frac{1}{$