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NEW SILICON PARETO CURVE, EVP: I've debated this problem for a while, and many people have looked at replacing the infamous PPA Pareto curve. I have played with adding interconnects (including the pins) into the equation and 4-letter and 5-letter replacements. After playing with several alternatives, I think EVP is probably the most effortless future transition and more straightforward to pronounce than the alternatives.

First-pass justifications:

- ENERGY, E: because our community should care not only about Performance but the "cost" of Performance, i.e., energy-in and the heat-out. Power really does not show the cost. Yes, time is a function of Performance, but it is also a function of cost. I am concerned that the industry has lost its Moral Imperative on efficiency. Reduction of logic or geometry shrinkage are minor factors in the efficiency game and not very useful ones.

- VOLUME, V: yes, we will be going to physical 3D silicon, no longer caring about 2D floorplans (very 70s). We will choose computational cubes over pancakes. We will care more about making 3D circuits cool enough to drive future computational cubes that avoid thermal nuclear meltdowns.

- PERFORMANCE, P: does not change. Performance is the metric for a satisfied consumer. Again, linked to Energy, but how much is too much? How close can we push modern

computing world towards the Margolus-Levitin limit with the available Energy without destroying the worlds resources in the process.

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