PERSONAL TECH

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Intel shows off near threshold voltage chip wizardry

Full digital radio integration with Atom, too

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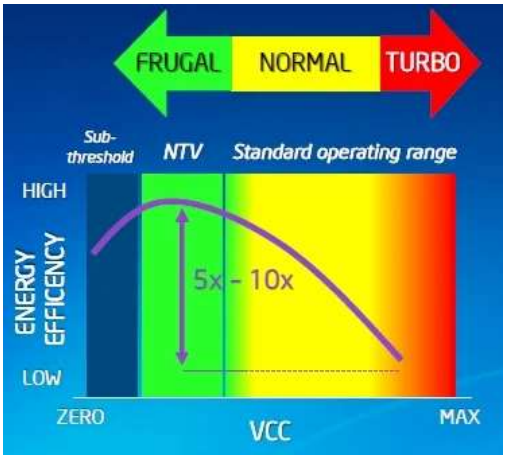
ISSCC The IEEE is hosting its annual International Solid State Circuits Conference in San Francisco this week, and the start of the show will no doubt be the unveiling of some of the features in Intel's forthcoming "Ivy Bridge" processors for PCs, which cram a multicore CPU and a GPU onto the same 22 nanometer Tri-Gate silicon wafer.

Intel is expected to go over some of the features of the Ivy Bridge processors on Monday afternoon. And ahead of the show Justin Rattner, Intel's CTO, trotted out some low-power and digital radio circuitry that the boffins at Intel Labs have been working on so all of these papers would not get stepped on by the presentation of Dadi Perlmutter, chief of Intel's Architecture Group and recently named chief products officer in a management shakeup in January.

In a conference call with journalists ahead of the show, Rattner had two things on his mind: near threshold voltage (NTV) circuit design and full-digital radio electronics and a test project integrating this digital radio on a dual-core Atom processor.

Rattner started talking about near threshold voltage operation and fine-grain power management during last fall's Intel Developer Forum.



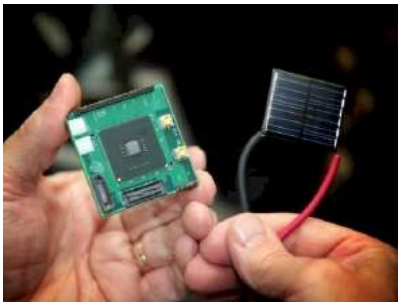
Near threshold voltage: The future of energy-efficient chips?

The threshold voltage is the point at which transistors turn on and conduct electricity. If you can flip bits near this threshold, instead of using much larger swing that is typically many times this threshold voltage to turn zeros into ones and vice versa, then you can save a lot of power.

"VCC has a quadratic impact on power consumption," Rattner explained. "Energy efficiencies peak as you approach the threshold voltage – in fact, you want to be a little over peak."

The idea is to have devices run at low voltages and power consumption rates that would be akin to a sleep mode in today's chips. And NTV techniques are not just limited to processors used in hand-held devices like smartphones and tablets, but to everything all the way up to exascale supercomputers, says Rattner. The important thing is that NTV techniques allow a chip's performance and power to scale as voltage scales up and down, and to do so across a wide dynamic range.

Rattner once again trotted out an original Pentium core from the 1990s re-implemented using NTV techniques. The chip, code-named "Claremont," was shown running off a single solar cell and driving both Windows and Linux back at IDF.



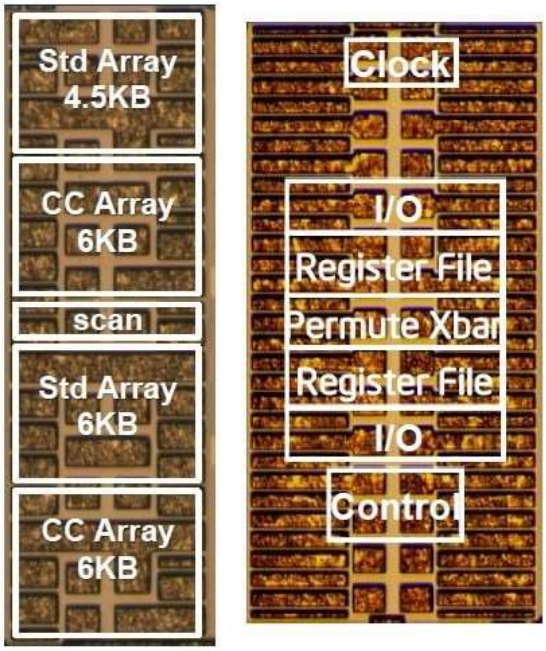
Intel's "Claremont" concept solar-powered IA-32 processor

What Intel will talk about at ISSCC is that the Claremont chip was actually etched in 32 nanometer processes and that the chip can run at a wide range of voltages and clock speeds, from 280 millivolts at 3MHz to 1.2 volts at 915MHz, with power consumption as low as 2 milliwatts in power consumption in a low-power mode where it is still operating, not in sleep mode.

The Pentium chip recast using NTV techniques in 32 nanometer processes was 4.7 times as energy efficient as a Pentium forged using 32 nanometer techniques without the NTV adaptations. If the chip was redesigned to better match the circuits to NTV, it could boost power efficiency by as much as a factor of eight or nine, says Rattner.

Intel Labs is not messing around with NTV techniques, just on old Pentium designs. At ISSCC, Intel's boffins will be showing off a bunch of other circuits using NTV.

One is an eight-transistor SRAM array based on the new 22 nanometer Tri-Gate process that uses the NTV approach. This chip allows for the minimum voltage on the SRAM to scale from 80 millivolts to 140 millivolts, and has the ability to boost the voltage on sensitive writes without the need of a charge pump circuit for the local voltage increase. It has a new "capacitive-coupling wordline boosting" method that Rattner said was "clever and novel," in that it used the intrinsic capacitances of the circuit to do the voltage boosting.



Low-voltage SRAM (left) and low-voltage SIMD graphics engine (right) using NTV techniques

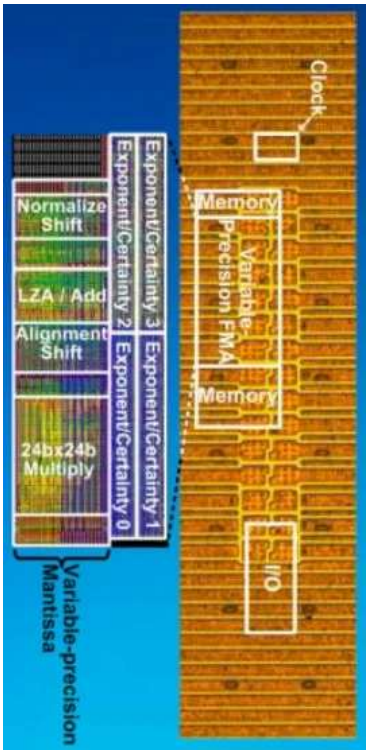
Intel is also showing off a SIMD engine for processor graphics, also implemented in 22 nanometer Tri-Gate processes. In this case, Intel is taking the vector permutation engine of a graphics chip and showing that the design can use NTV techniques and scale the voltage down to 280 millivolts and as high as 1.1 volts. This demonstrates a factor of nine increase in power efficiency over current manufacturing techniques that have a much higher operating voltage when running in low-power mode.

"By any measure, that's a huge improvement in the energy efficiency of these devices," Rattner declared.

Another new circuit that is going to have supercomputer boffins salivating is a variable precision floating point unit, also etched with NTV techniques.

This is a test chip from Intel Labs that sniffs the applications using the FP unit, seeing whether they are doing math for apps or for graphics processing, and figures out what level of precision is necessary then only takes data in that format and only crunches it at that level of bit-ness. This test chip, which runs at 1.45GHz and delivers between 52 and 162 gigaflops of raw number-crunching power, includes a fused multiply-add unit and is etched in 32 nanometer processes.

The FP unit can do 6-bit, 12-bit, and 24-bit precision and, by being smart about doing the math, it can cut energy consumption by as much as 50 per cent and - perhaps more importantly - you can do the math a lot faster because you only operate on the bits you need and don't stuff registers and do calculations on a lot of useless zeros. And, says Rattner, there is no diminished resolution on images processed using this unit, at least not that the human eye can catch.



Intel's variable precision floating point unit

"You can imagine this going into future GPUs and high performance computing designs," said Rattner.

Indeed. I can also imagine Intel actually going back into the discrete graphics card business, too.

By the way, this FP unit did not implement NTV techniques, but used bulk 32 nanometer CMOS processes from Intel. So energy efficiency can be pushed even further, perhaps with as much as a 7X gain in efficiency during low-voltage operation, when NTV techniques are added, said Rattner.

Next page: **What's the frequency, Kenneth?**

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