Standardization of Chiplet Models

Chiplet Summit

January 24-26, 2023, San Jose, California

Tony Mastroianni, Siemens EDA

Chiplet Design Exchange (CDX)

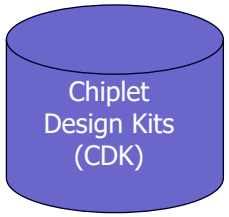
OPEN DOMAIN SPECIFIC ARCHITECTURE

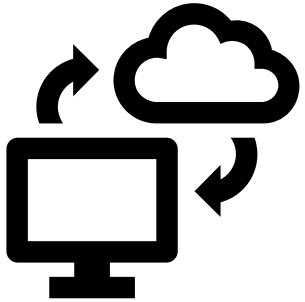
- Charter: Recommend standardized chiplet **models,** workflows and ecosystem
- Members: EDA, chiplet Providers, Assemblers & Integrators
- Other ODSA work groups are working on
  - Die-to-Die (D2D) interfaces
  - Security agents
  - Business models & other related chiplet topics

Open Possibilities.

Standardized Chiplet Models

- Machine readable models





- Industry Standards

JEDEC®
Global Standards for the Microelectronics Industry

OPEN Compute Project®

IEEE
Advancing Technology for Humanity

- Security & Traceability Assurance

- Documentation

Open Possibilities.

Chiplet Design Kits (CDK)

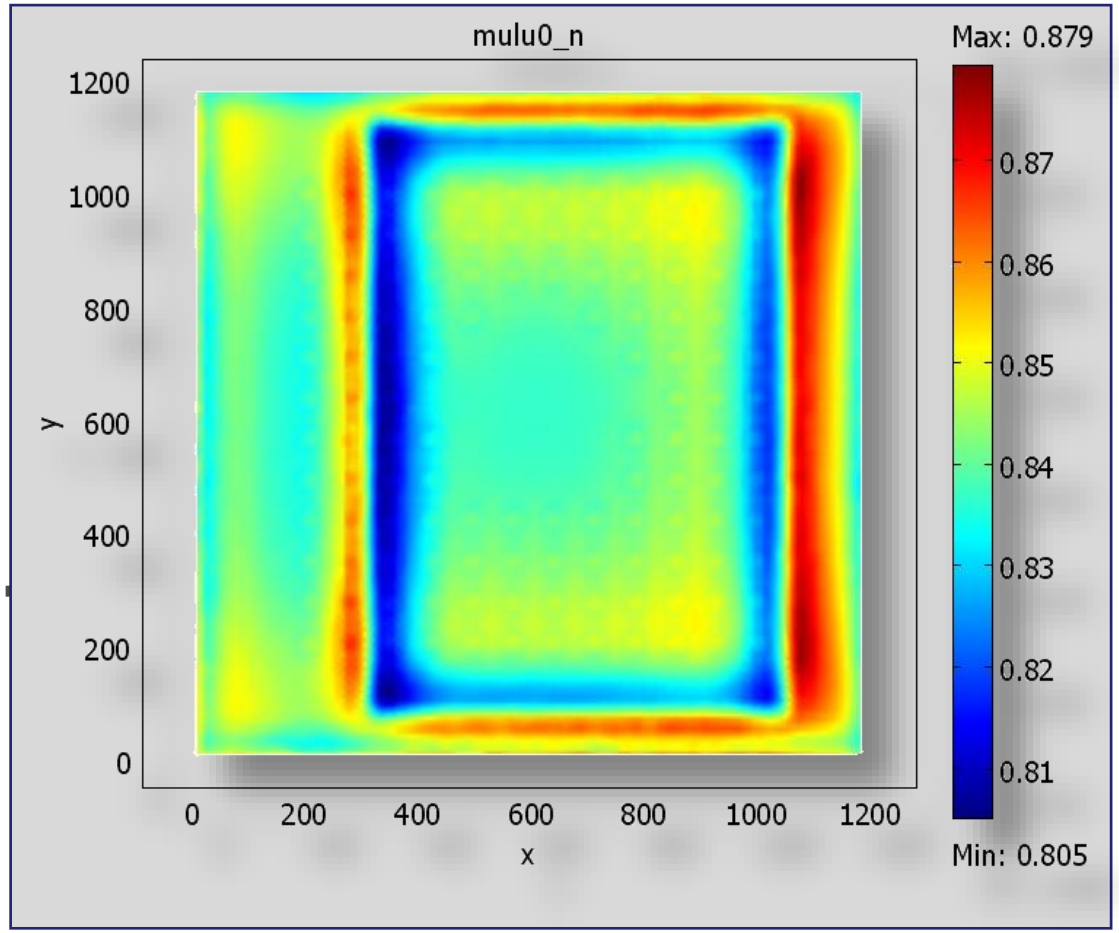
Model	Description
Thermal	• ECXML – JEDEC JEP181
Physical, Mechanical & IO	• Library Exchange Format (LEF) • GDSII or OASIS • SPICE • JEDEC JEP30-P101/CDXML • Optional: Verilog to Physical Pin Mapping file (CSV)
Behavioral	• SystemVerilog IEEE – 1800-2017 • Recommended: Verilog-AMS 2.4 • Optional: SystemC IEEE – 1666-2011 • Optional: Bus Functional Model (BFM)
Power	• Liberty (.LIB) • IEEE2416 Standard for Power Modeling • Optional: UPF – IEEE 1801-2018 or Chip Power Format • Optional: Verilog-AMS 2.4 • Optional: SystemC IEEE – 1666-2011
SI Analysis	• IBIS/IBIS AMI • Optional: Spice netlist (for the IO driver and/or receiver) • Optional: Channel model

Model	Description
PI Analysis	• Chip Power Model (CPM)
Electrical Rules	• JEDEC JEP30-E101/CDXML
Test	• BSDL – IEEE 1149.1/1149.6/1149.7 • ATPG model - Primitive/UDP based Verilog • Recommended: Internal JTAG (IJTAG) IEEE 1687 • Optional: IEEE-1500 Core Test Language (CTL) • Recommended: Gray-box level netlist • ATPG vectors - STIL (IEEE1450.1) or WGL • MBIST/repair vectors - STIL (IEEE1450.1) or WGL • Optional: UPF – IEEE 1801 or Chip Power Format • Optional: IP Firmware (if applicable)
Security/T&T	• Optional: Security Agent • Optional: Trust & Traceability
Documentation and Guidelines	• General Chiplet Documentation • SiP Physical Integration guidelines • SiP Test guidelines • Optional: Firmware (if applicable) • Optional: Security

Thermal

OPEN DOMAIN SPECIFIC ARCHITECTURE

CDX



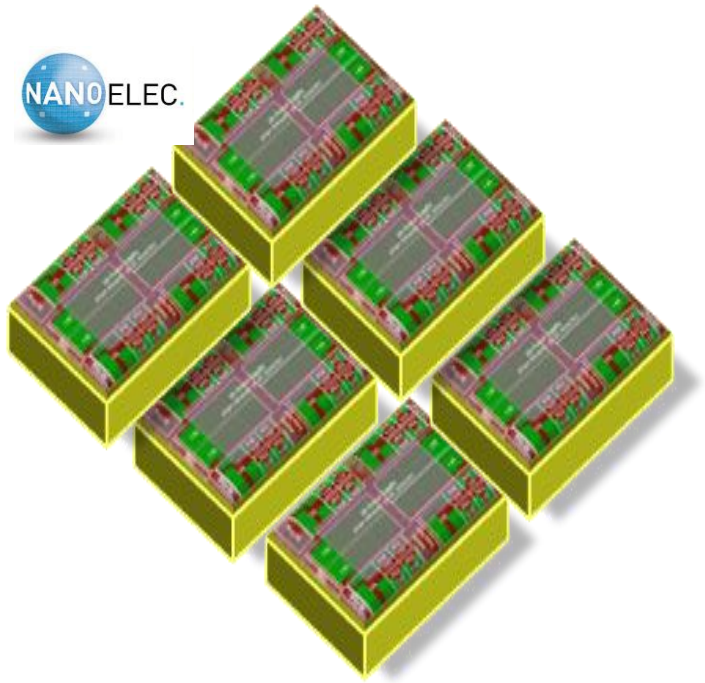
ECXML – JEDEC JEP181

Open Possibilities.

Physical, Mechanical & IO

OPEN DOMAIN SPECIFIC ARCHITECTURE

CDX



Library Exchange Format (LEF)

GDSII or OASIS

SPICE

Optional: Verilog to Physical Pin Mapping file (CSV)

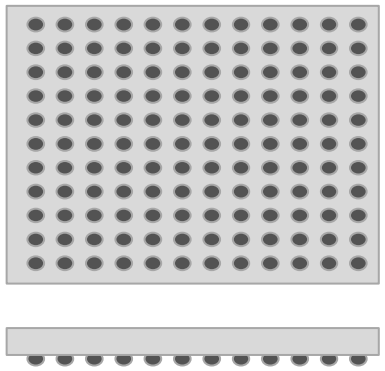
JEDEC JEP30-P101/CDXML (New)

Open Possibilities.

Physical, Mechanical and IO: CDXML File Format

OPEN DOMAIN SPECIFIC ARCHITECTURE

CDX



CDXML is being Developed at CDX Workstream of ODSA in Collaboration with Industry Leaders. CDXML adopted the ZEF opensource model from zGlue.

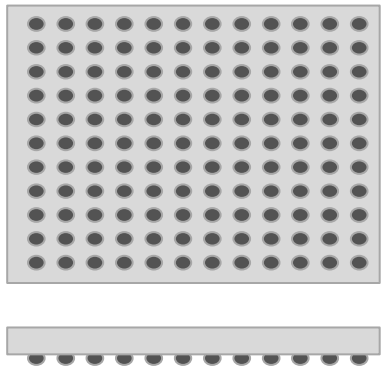
- Mechanical describes all x,y,z, dimensions, tolerance, solder type and material properties
- IO describes pin location, functionality, mode of operation and standardized D2D interface pin names

Open Possibilities.

Electrical Properties

OPEN DOMAIN SPECIFIC ARCHITECTURE

CDX



JEDEC JEP30-E101/CDXML

- Electrical contains overall electrical characteristics information to aid in power scenarios calculations, modes of operation, absolute maximum ratings, recommended operating conditions, and ESD
- EC (Electrical Characteristics), abs max values, operating conditions, allowable RLC, voltage references, temperate based VI (Voltage and Current) pin characteristics

Behavioral

OPEN DOMAIN SPECIFIC ARCHITECTURE

CDX

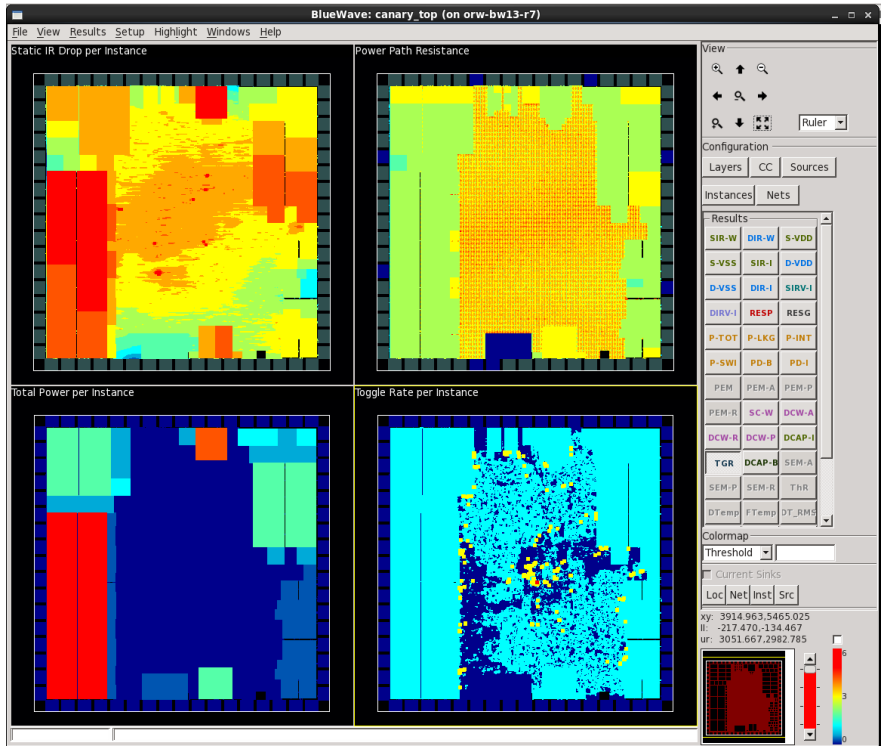
SystemVerilog IEEE – 1800-2017

Recommended: Verilog-AMS 2.4

Optional: SystemC IEEE – 1666-2011

Optional: Bus Functional Model (BFM)

Power



Liberty (.LIB)

IEEE2416 Standard for Power Modeling

Optional: UPF – IEEE 1801-2018 or Chip Power Format

Optional: Verilog-AMS 2.4

Optional: SystemC IEEE – 1666-2011

Signal Integrity Analysis

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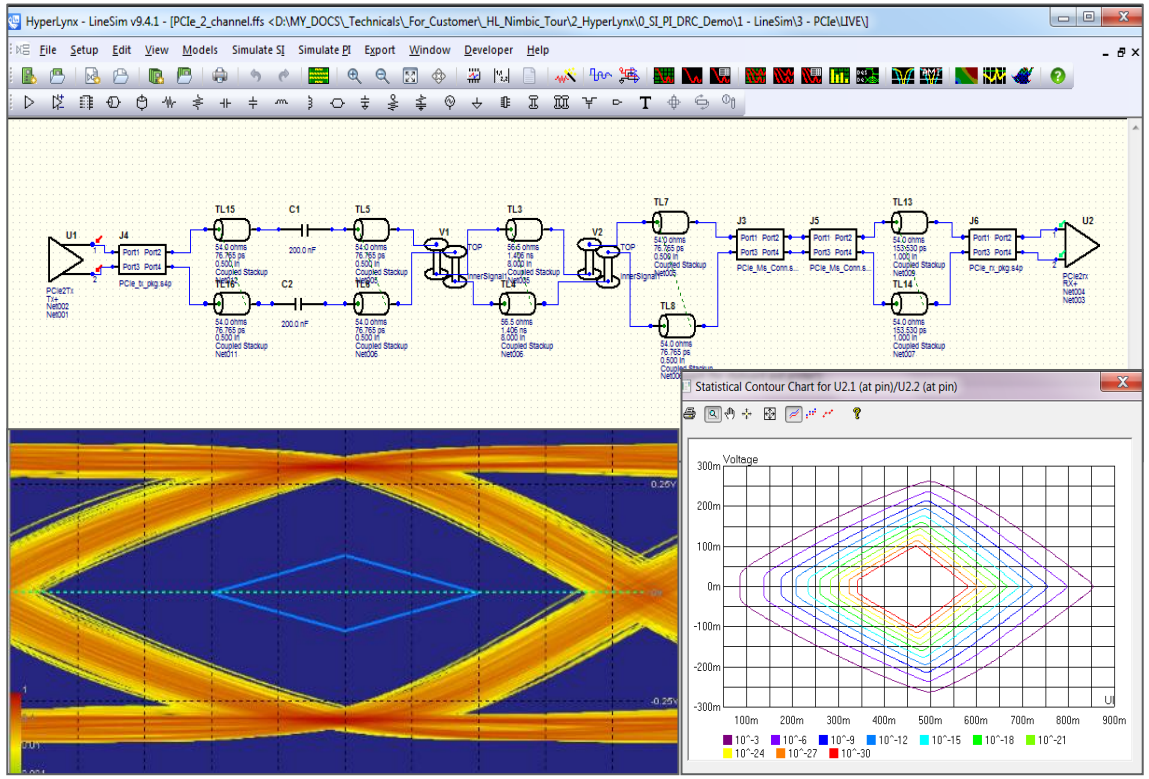
CDX



IBIS/IBIS AMI

Optional: SPICE netlist
(IO driver and/or Transceiver)

Optional: Channel model

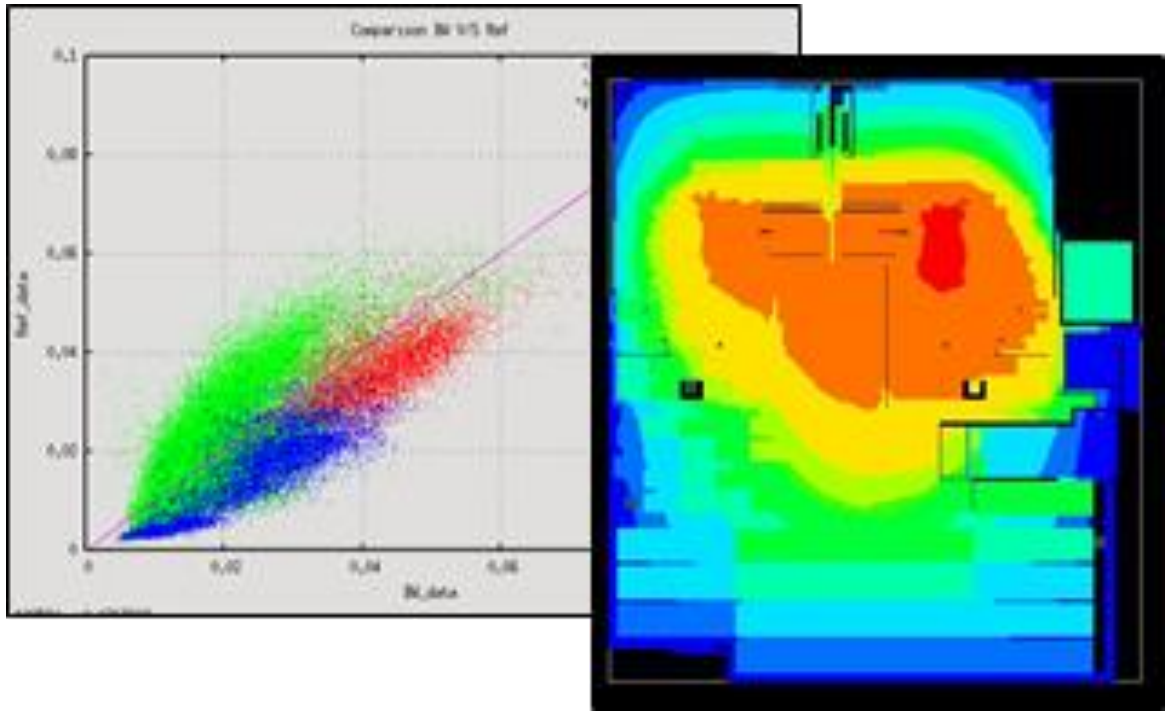
Open Possibilities.

Power Integrity Analysis

OPEN DOMAIN SPECIFIC ARCHITECTURE

CDX

Chip Power Model (CPM)

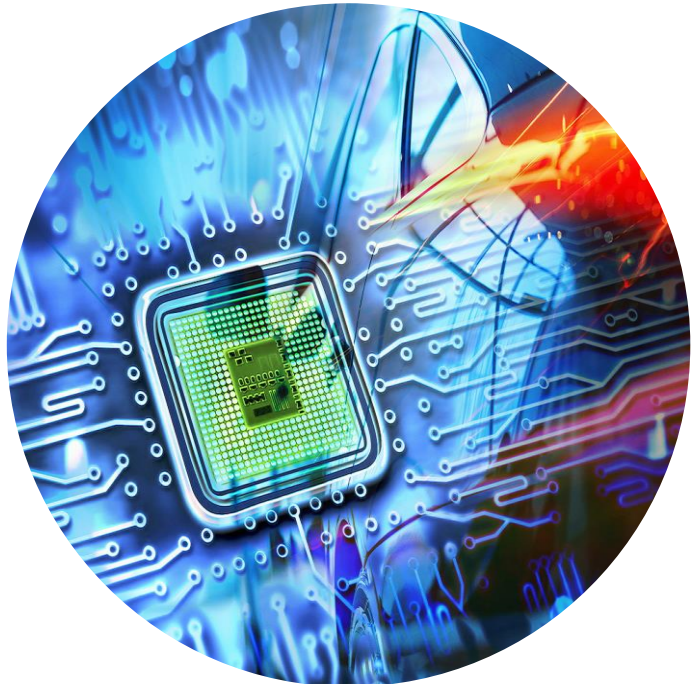


Open Possibilities.

Test

OPEN DOMAIN SPECIFIC ARCHITECTURE

CDX



BSDL – IEEE 1149.1/1149.6/1149.7

ATPG model - Primitive/UDP based Verilog

Recommended: Internal JTAG (IJTAG) IEEE 1687

Optional: IEEE-1500 Core Test Language (CTL)

Recommended: Gray-box level netlist

ATPG vectors - STIL (IEEE1450.1) or WGL

MBIST/repair vectors - STIL (IEEE1450.1) or WGL

Optional: UPF – IEEE 1801 or chip power format

Optional: IP firmware (if applicable)

Open Possibilities.

Security and Trust/Traceability

OPEN DOMAIN SPECIFIC ARCHITECTURE

CDX

Optional: Security agent

Optional: Trust & Traceability

Documentation

OPEN DOMAIN SPECIFIC ARCHITECTURE

CDX

General chiplet documentation

SiP physical integration guidelines

SiP test guidelines

Optional: Firmware (if applicable)

Optional: Security/T&T

Summary

Broad adoption of chiplet based designs requires standardization of chiplet models

CDX whitepapers and CDXML format are a good start towards this standardization:

IEEE 3DIC 2021: November 15-18, 2022

https://ieeexplore.ieee.org/document/9687611

OCP: September 17, 2022

https://www.opencompute.org/documents/ocp-odsa-cdx-proposed-standardization-of-chiplet-models-for-heterogeneous-integration-2-pdf

OCP Global Summit: Oct 18-20, 2022

https://drive.google.com/file/d/1EEwYuEAECPM5Btu4_9Znder-RD4X_Dx-/view

Current CDX areas of focus:

- **HI Workflows White Paper**
- **Defining new CDXML format**

Open Possibilities.

Acknowledgments

CDX Authors

- Anthony Mastroianni (Siemens)
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- Lihong Cao (ASE)
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Open Possibilities.

Call for Participation

Join us to continue our work on chiplet models and SiP workflows and to support the adoption of these recommendations.

- We're looking for volunteers!
- For participation, Email:

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david.ratchkov@thracesystems.com

https://www.opencompute.org/wiki/Server/ODSA

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Thank You