Process and Design Solutions for Exploiting FD-SOI Technology Towards Energy Efficient SOCs

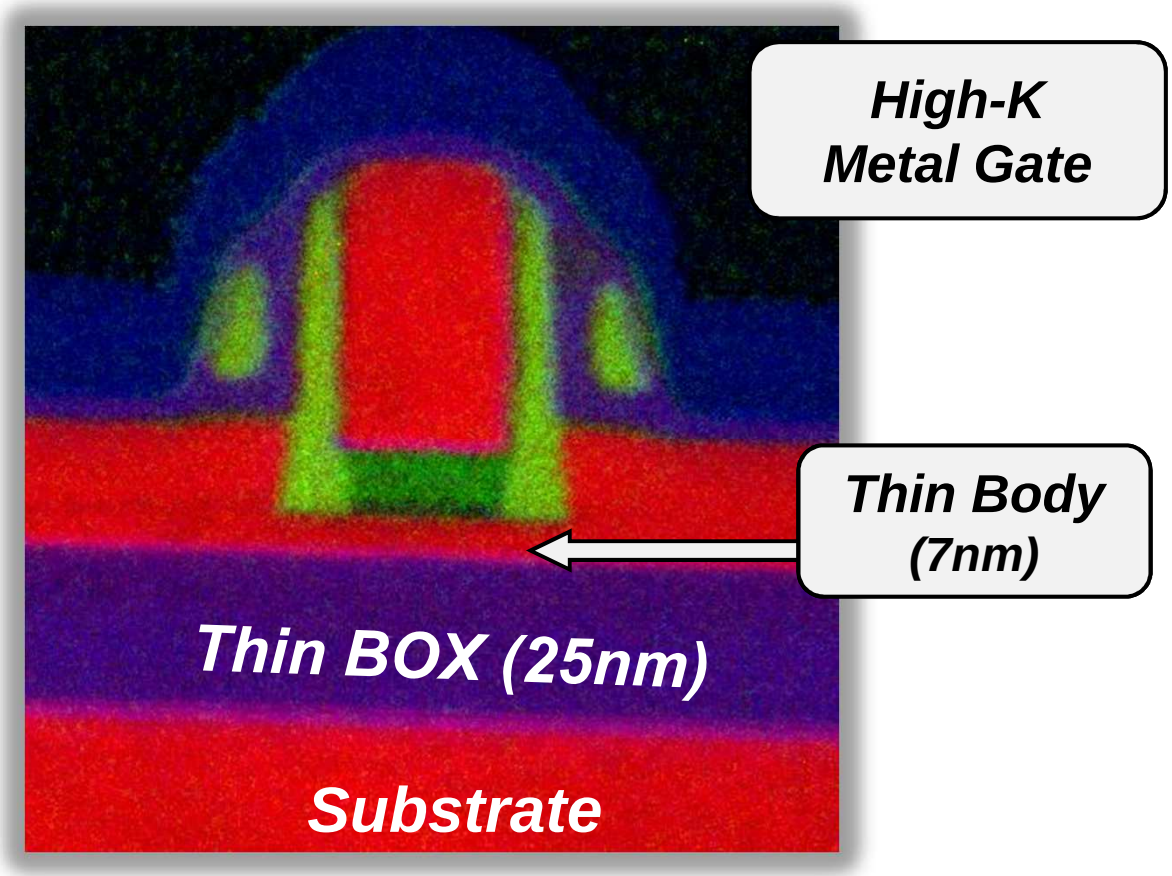
Philippe FLATRESSE

Technology R&D
Central CAD & Design Solutions

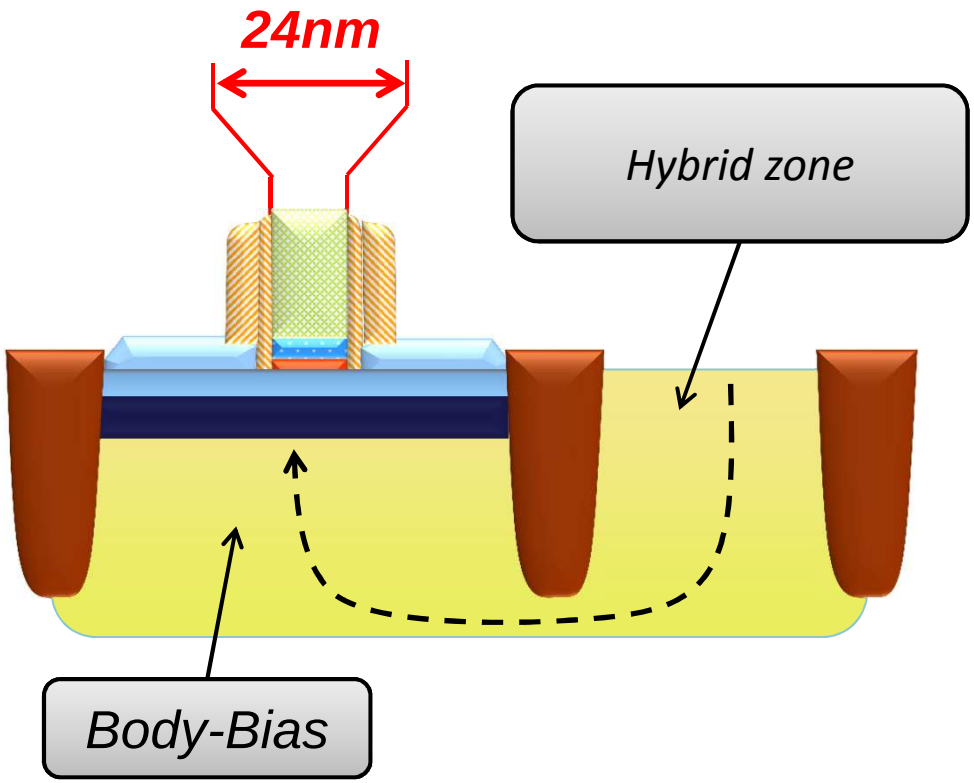
STMicroelectronics

International Symposium on Low Power Electronics and Design

28nm Planar UTBB FD-SOI Transistor



28nm Planar UTBB FD-SOI Advantages

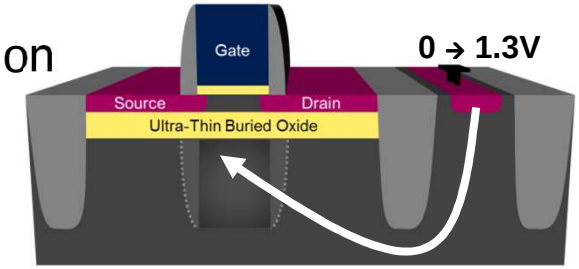


- **Shorter channel length**
  - 24nm technology !
- **Better electrostatics**
  - Faster operation
  - Low voltage
  - Reduced variability
- **Total dielectric isolation**
  - Latch up immunity
- **Lower leakage current**
  - Less sensitive to temperature

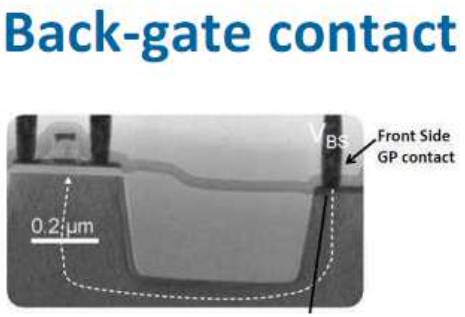
Body Biasing (BB)

A very reasonable effort for extremely worthwhile benefits

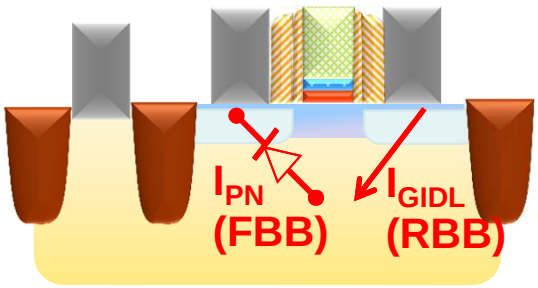
- An **extremely powerful** and flexible concept in FD-SOI to :
  - Boost performance
  - Optimize passive and dynamic power consumption
  - Cancel out process variations and extract optimal behavior from all parts



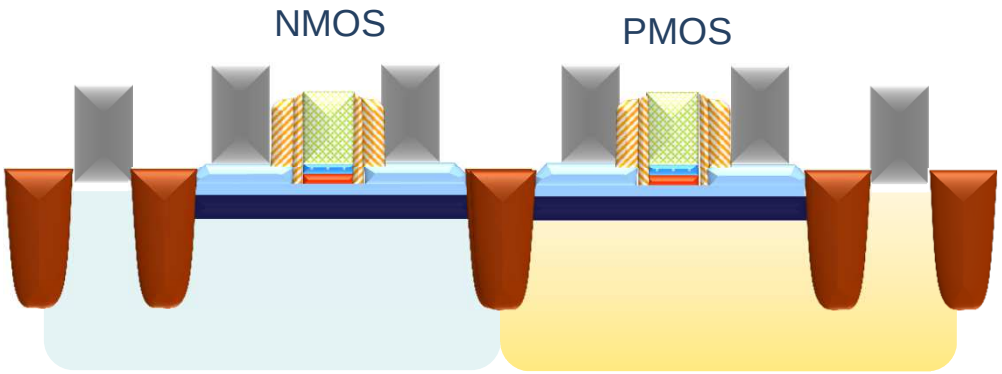
- Comparatively **easy to implement** – if you've ever done DVFS you'll have no difficulty with Body Biasing
  - No area penalty compared to Bulk
  - Reuse of Bulk design techniques
  - Speed/Power control



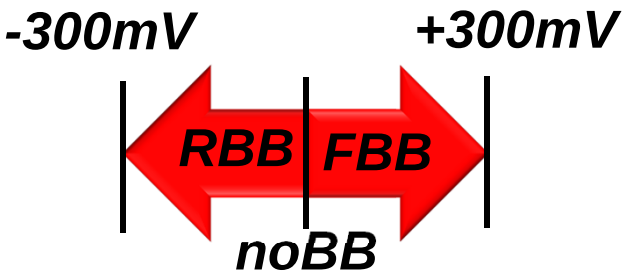
Extended Body Bias Range in UTBB FD-SOI

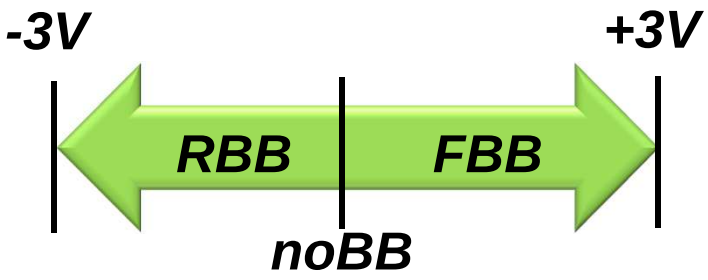


BULK



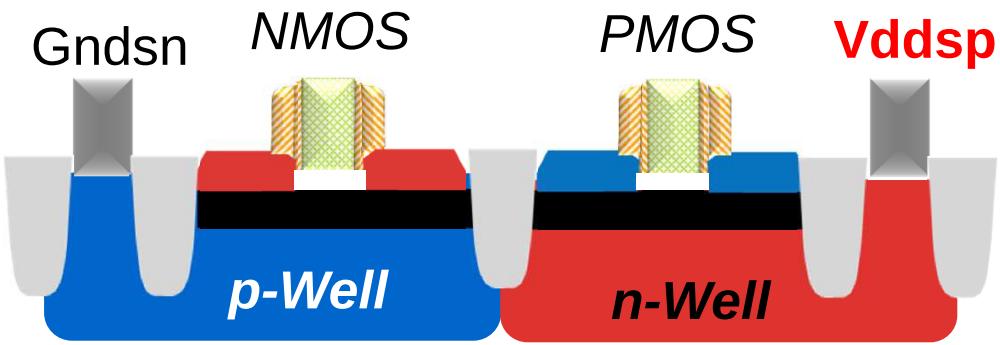
UTBB FD-SOI

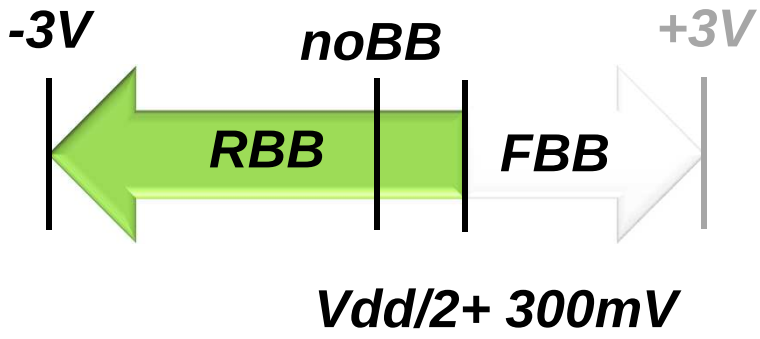




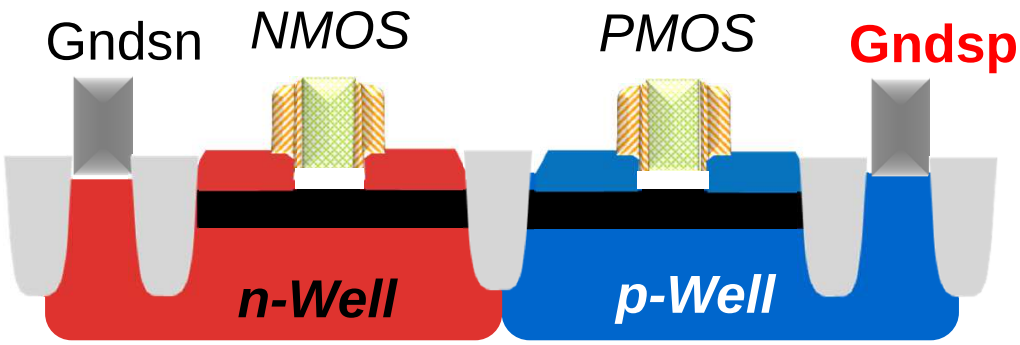
UTBB FD-SOI: Extended Body Voltage Range

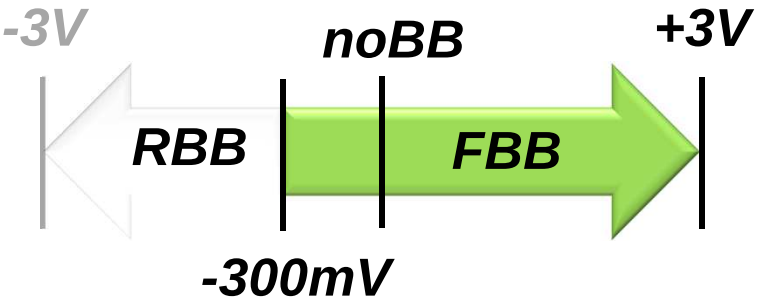
- **Conventional Well (CW) - RBB**





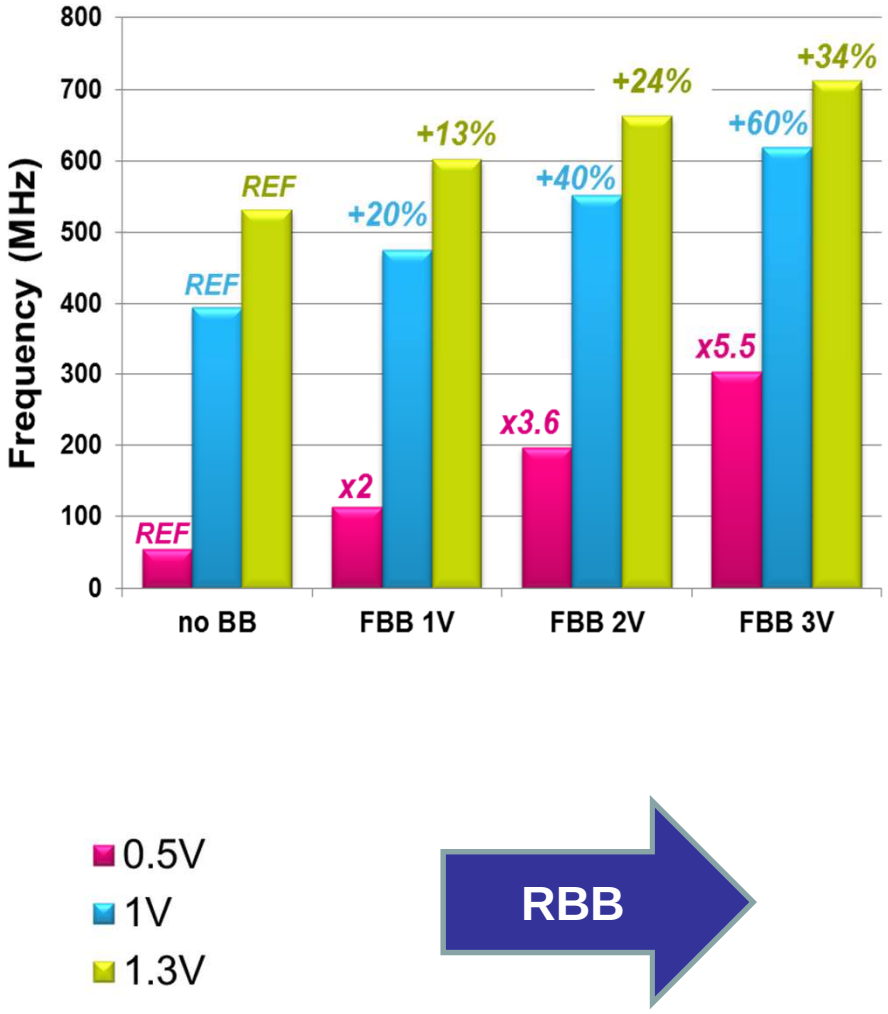
- **Flip Well (FW) - FBB**



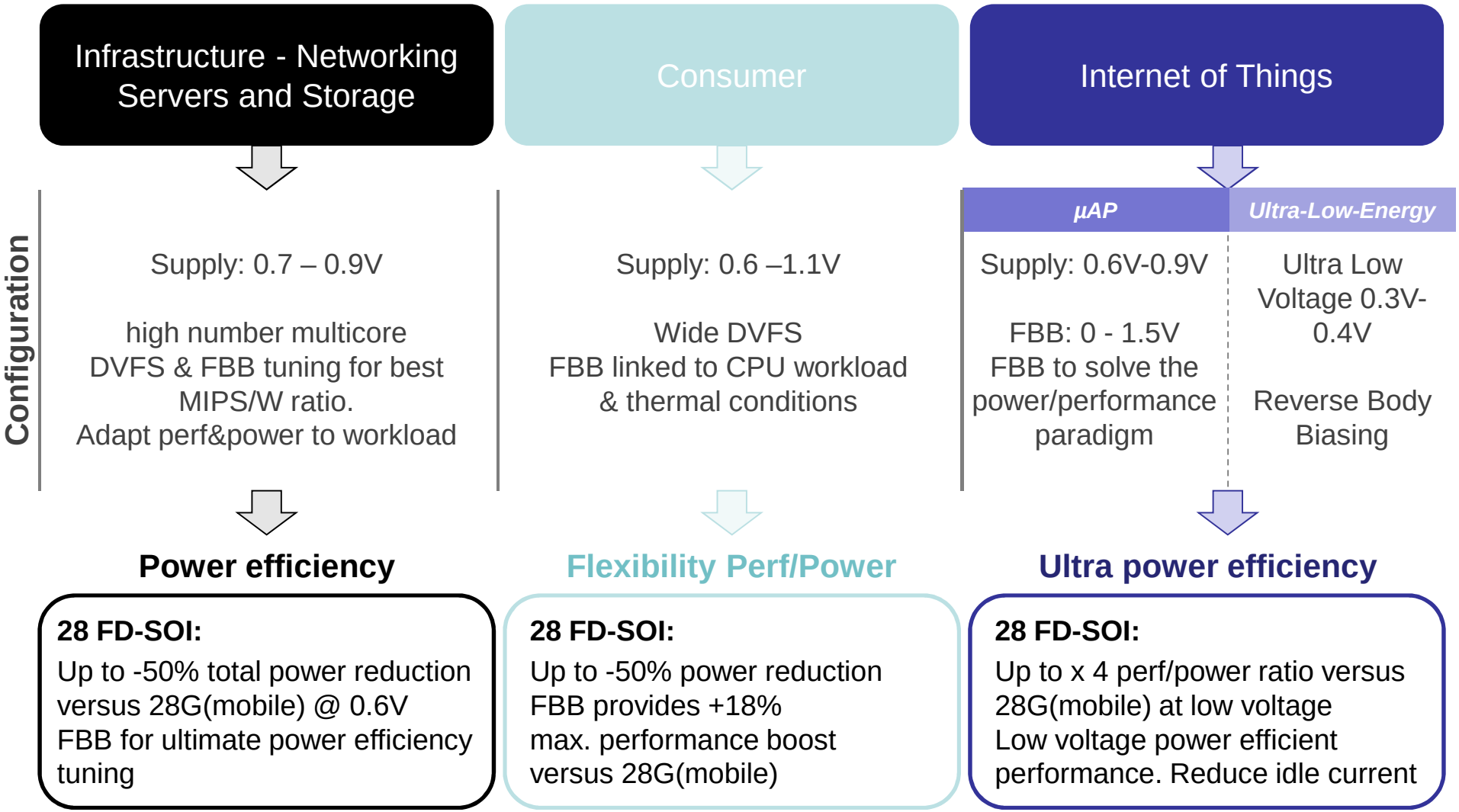


Efficient knob for speed/leakage optimization

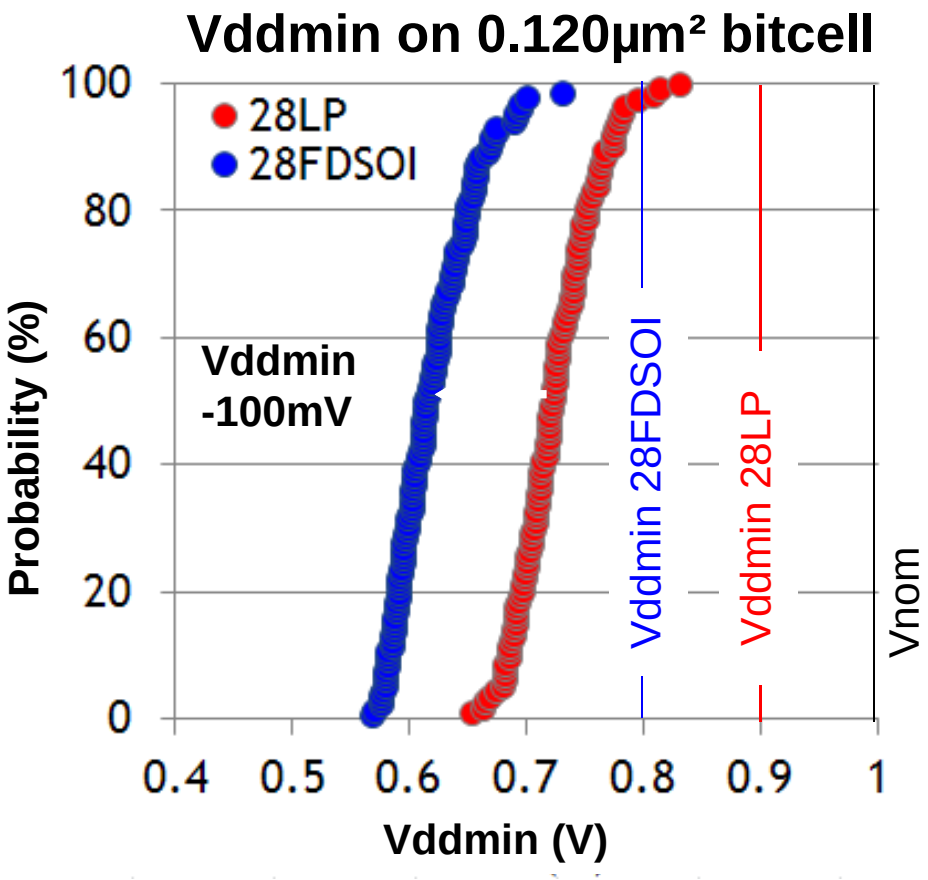
Body Bias Efficiency - Silicon Evidence

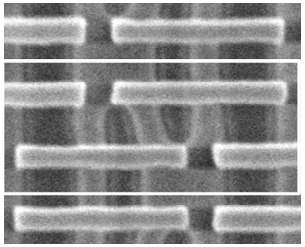


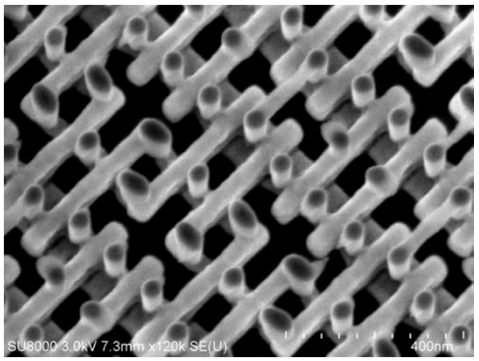
FBB usage per market segment

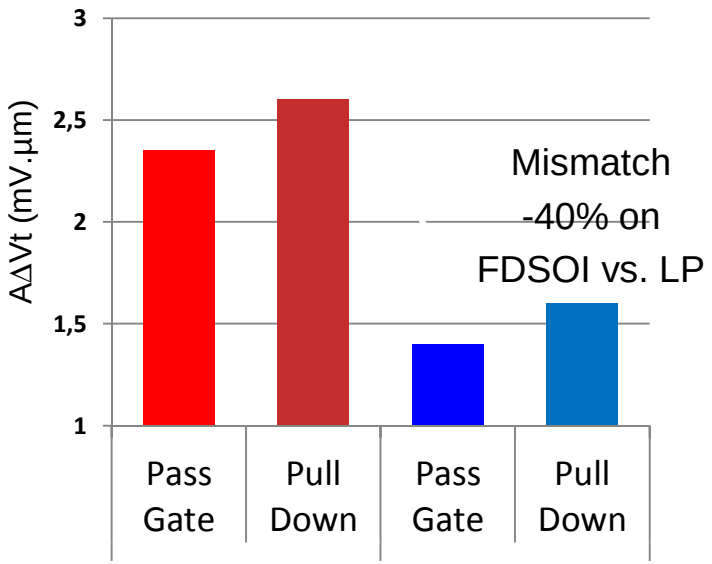


Improved Memory Minimum Voltage





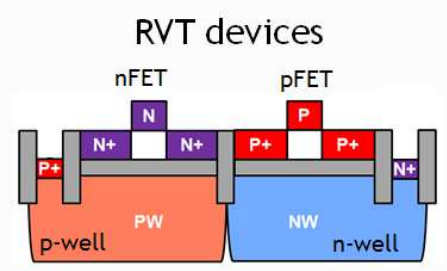




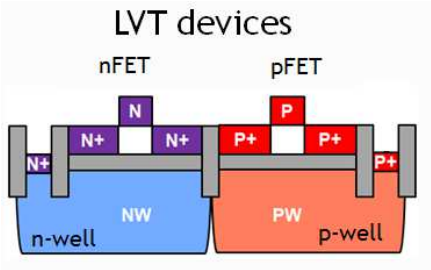
Vmin gain thanks to better mismatch on FD-SOI devices (undoped channel)

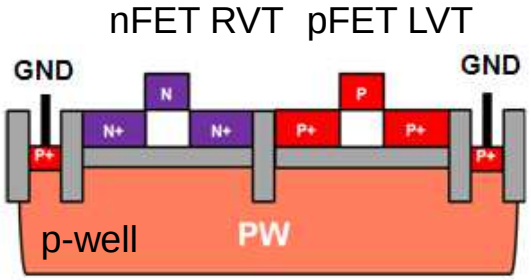
FD-SOI Unique “Single Well” Architecture

SRAM
regular wells



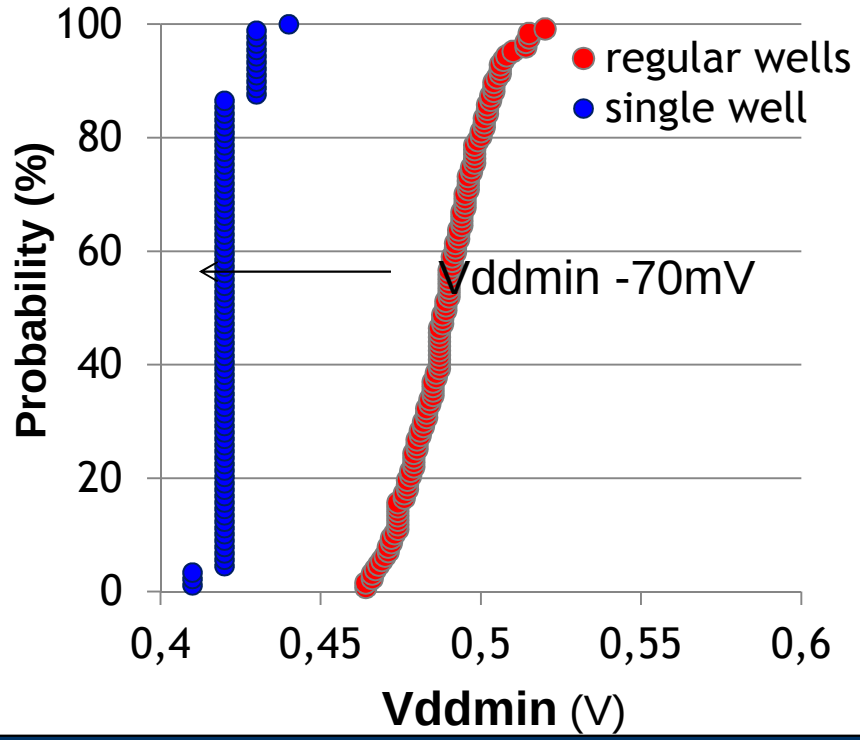
SRAM
flip-well
architecture





ST patented bitcell architecture

SRAM single well

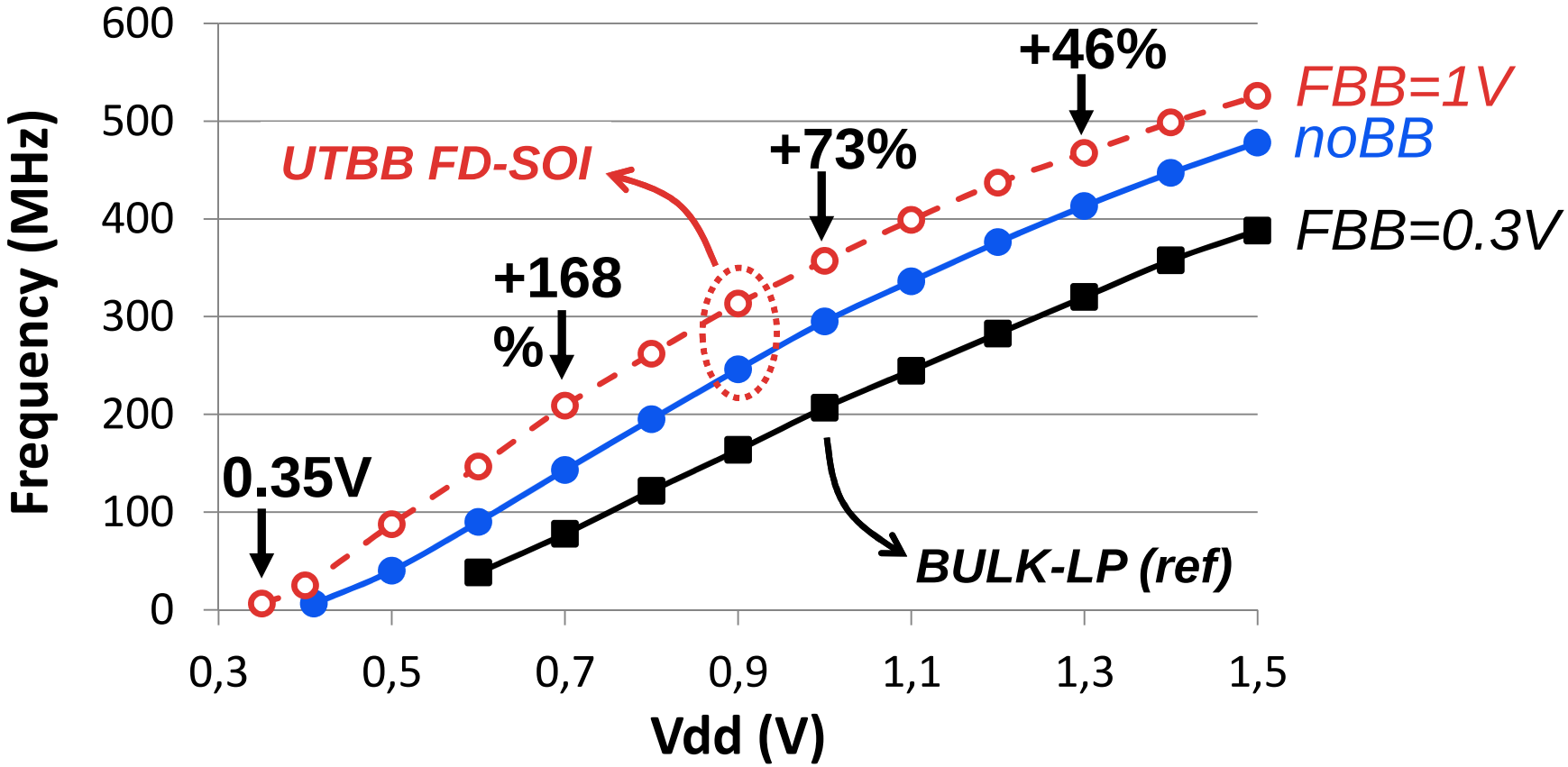


Single Well SRAM

Optimized stability helping behavior at low voltage

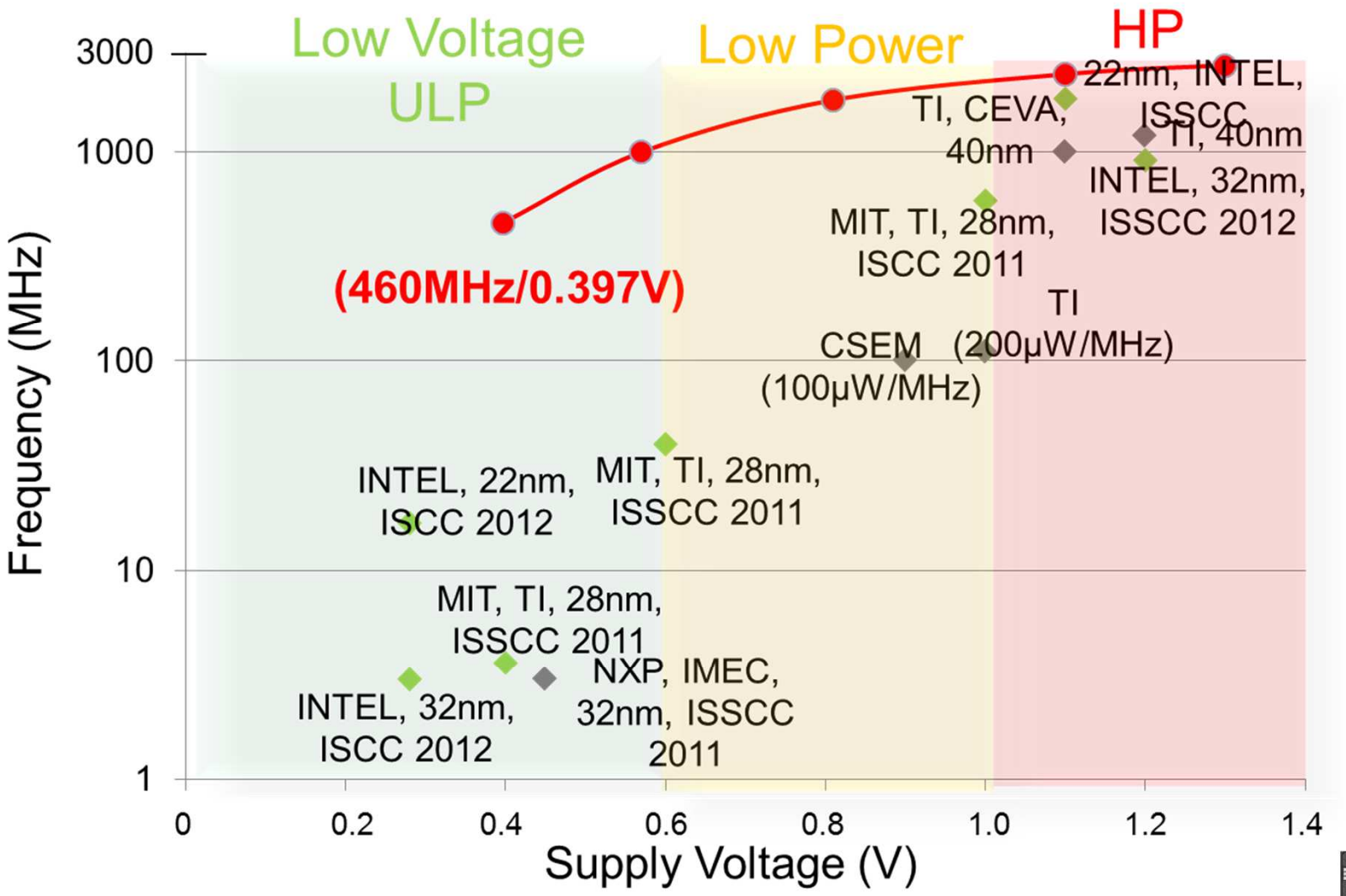
➔ Power efficiency

Si Evidence: LDPC on UTBB FD-SOI

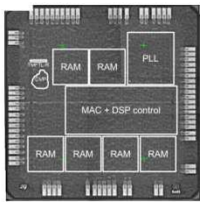


LDPC 6T-SRAM (FBB 1V) functional down to 0.41V

State of the Art UWVR DSP in FDSOI:

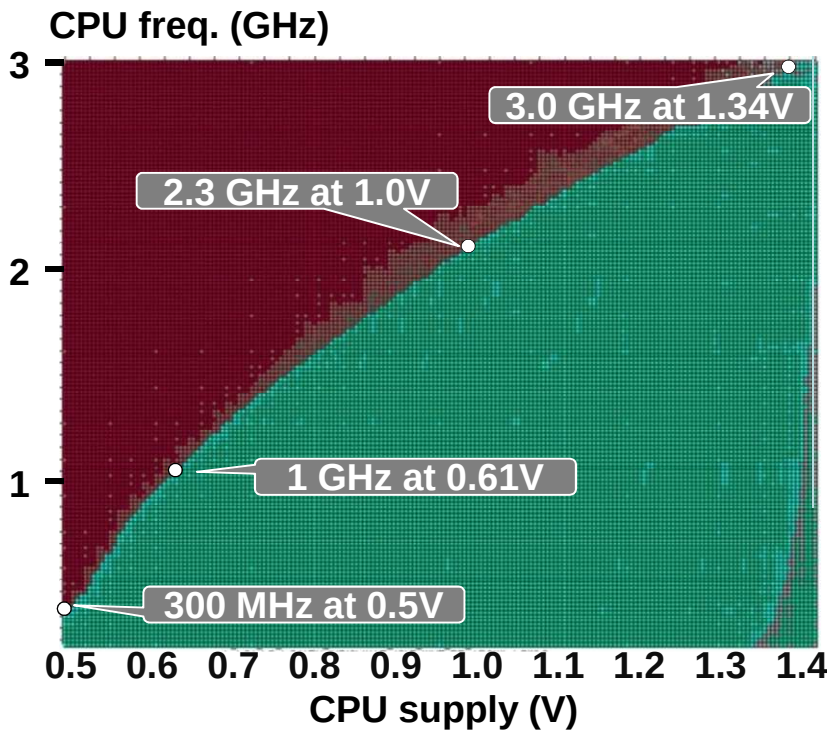


27.1 : A 460MHz@397mV – 2.6GHz@1.3V 32bit VLIW DSP

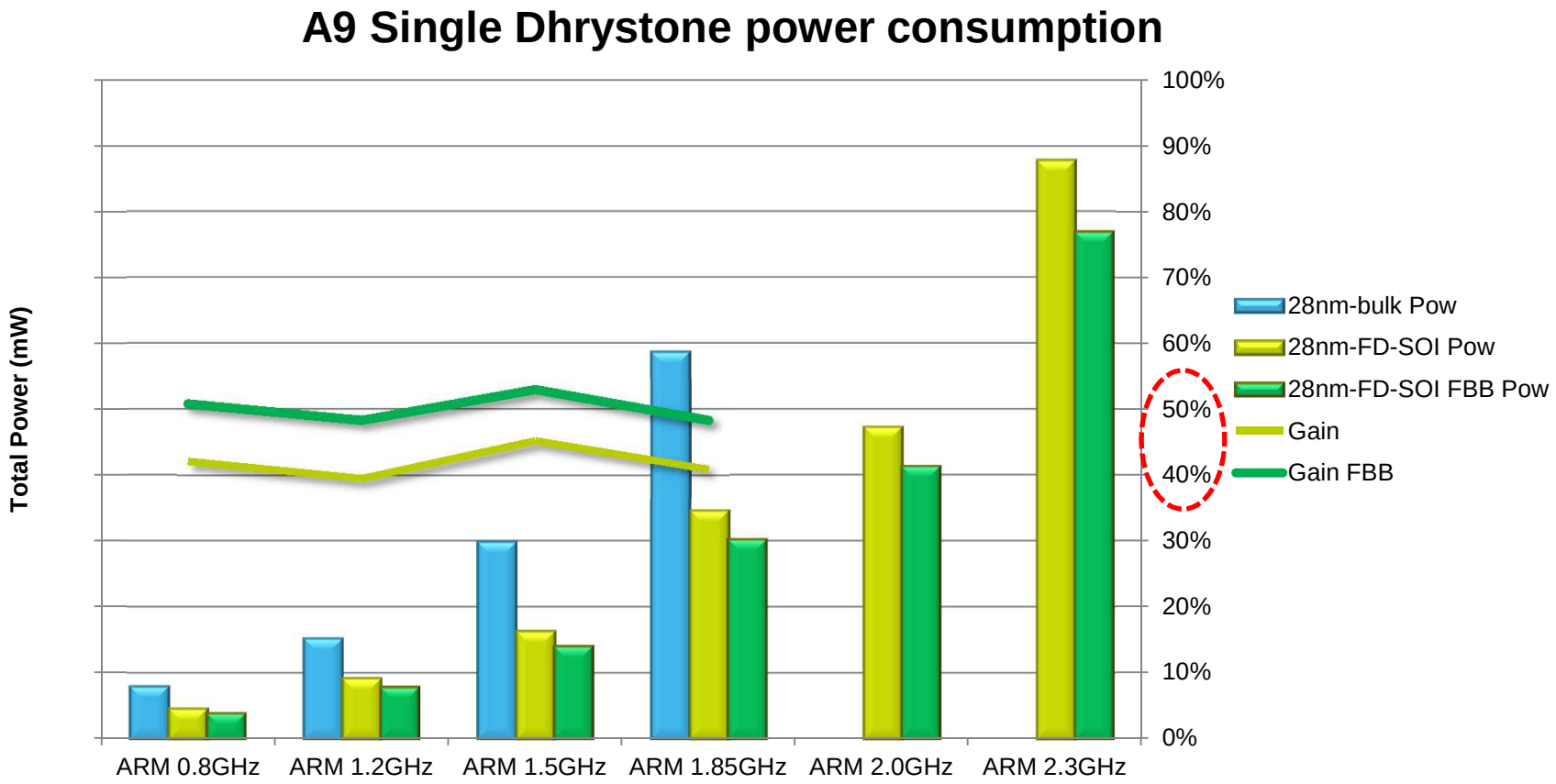


Cortex A9: FD-SOI allowing Ultra-Wide DVFS

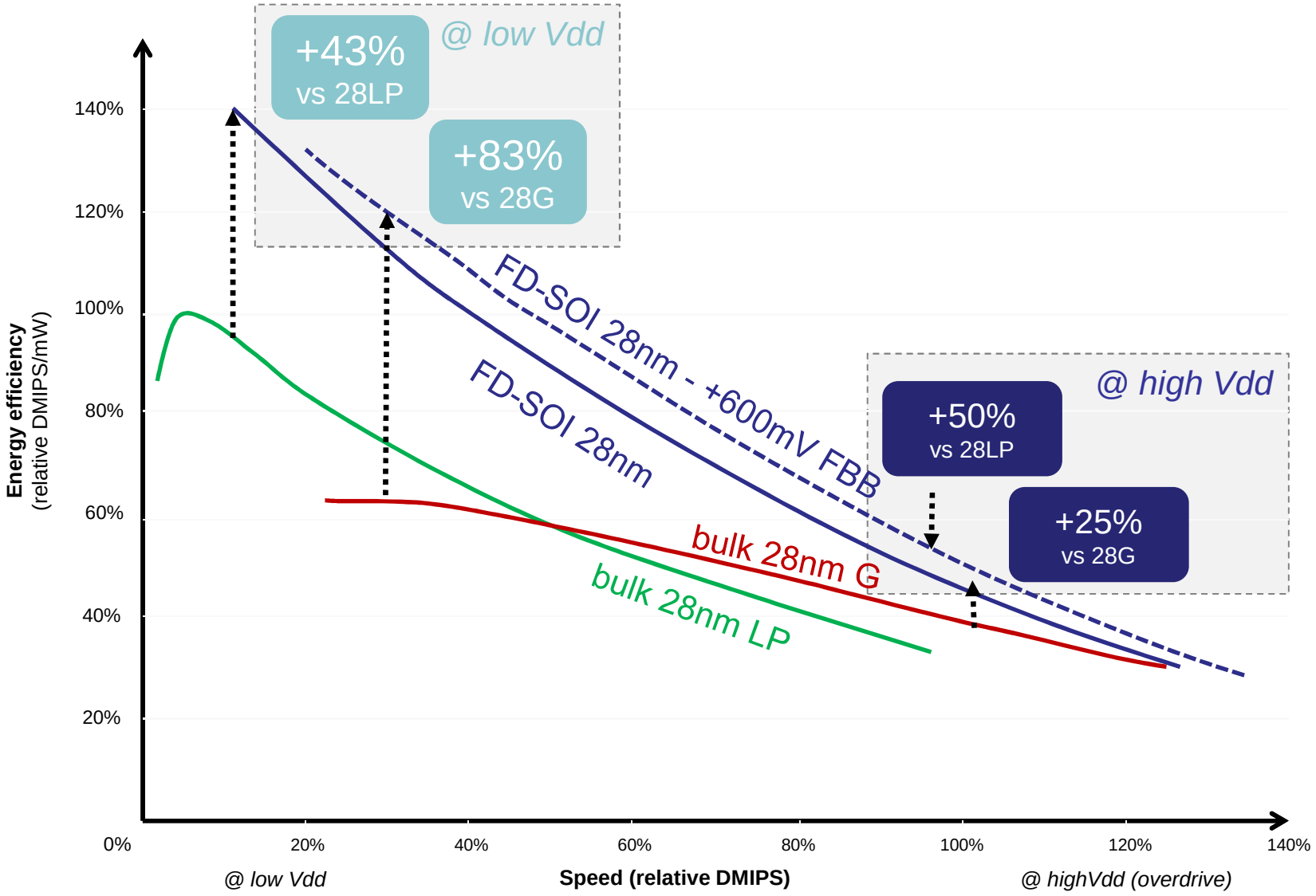
- FD-SOI allows the widest Vdd range for voltage scaling
- Still guaranteeing top notch speeds at very low operating voltage
  - >5x when compared to 28LP technology
  - >35% when compared to 28G technologies
- DVFS energy efficiency optimization is further extended thanks to body bias
  - Allowing to balance and optimize the static and dynamic power consumption components



Cortex A9 Power vs. Performances



28nm FD-SOI Best in class efficiency



FD-SOI

Faster, Cooler, Simpler technology	Enhanced design options	Mature process & ecosystem
• FD-SOI transistors up to 30% faster than bulk • Outstanding power efficiency at every level • Extensive use of existing fab infrastructure	• Back-biasing as a flexible and powerful optimization • Very large operating range for the same design • Ultra-wide range DVFS	• Ecosystem ready at all stage: wafer supply, design and manufacturing • Extended IP offer • Strategic collaboration between Samsung and ST

FD-SOI gives your SOC competitive advantages