JEDEC STANDARD

Double Data Rate (DDR) SDRAM Specification

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DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

(From JEDEC Board Ballot JCB-99-70, and modified by numerous other Board Ballots, formulated under the cognizance of Committee JC-42.3 on DRAM Parametrics.)

Standard No. 79 Revision Log.
Release 1, June 2000
Release 2, May 2002
Release C, March 2003
Release D, January 2004
Release E, May 2004

Scope

This comprehensive standard defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionality, ac and dc parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well.

The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64Mb through 1Gb, X4/X8/X16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

16 M X4 (4 M X4 X4 banks), 8 M X8 (2 M X8 X4 banks), 4 M X16 (1 M X16 X4 banks)
32 M X4 (8 M X4 X4 banks), 16 M X8 (4 M X8 X4 banks), 8 M X16 (2 M X16 X4 banks)
64 M X4 (16 M X4 X4 banks), 32 M X8 (8 M X8 X4 banks), 16 M X16 (4 M X16 X4 banks)
128 M X4 (32 M X4 X4 banks), 64 M X8 (16 M X8 X4 banks), 32 M X16 (8 M X16 X4 banks)
256 M X4 (64 M X4 X4 banks), 128 M X8 (32 M X8 X4 banks), 64 M X16 (16 M X16 X4 banks)

FEATURES

- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8
- CAS Latency: 2 or 2.5, DDR400 also includes CL = 3
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 2.5 V (SSTL_2 compatible) I/O
- VDDQ: +2.5 V ±0.2 V for DDR 200, 266, or 333
  +2.6 ±0.1 V for DDR 400
- VDD:
  +3.3 V ±0.3 V or +2.5 V ±0.2 V for DDR 200, 266, or 333
  +2.6 ±0.1 V for DDR 400

GENERAL DESCRIPTION

The DDR SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:
64 Mb has 67,108,864 bits
128 Mb has 134,217,728 bits
256 Mb has 268,435,456 bits
512 Mb has 536,870,912 bits
1 Gb has 1,073,741,824 bits

The DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW will be referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable read or write burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Initial devices may have a VDD supply of 3.3 V (nominal). Eventually, all devices will migrate to a VDD supply of 2.5 V (nominal). During this initial period of product availability, this split will be vendor and device specific.

This data sheet includes all features and functionality required for JEDEC DDR devices; options not required, but listed, are noted as such. Certain vendors may elect to offer a superset of this specification by offering improved timing and/or including optional features. Users benefit from knowing that any system design based on the required aspects of this specification are supported by all DDR SDRAM vendors; conversely, users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note: This specification defines the minimum set of requirements for JEDEC X4/X8/X16 DDR SDRAMs. Vendors will provide individual data sheets in their specific format. Vendor data sheets should be consulted for optional features or superset specifications.

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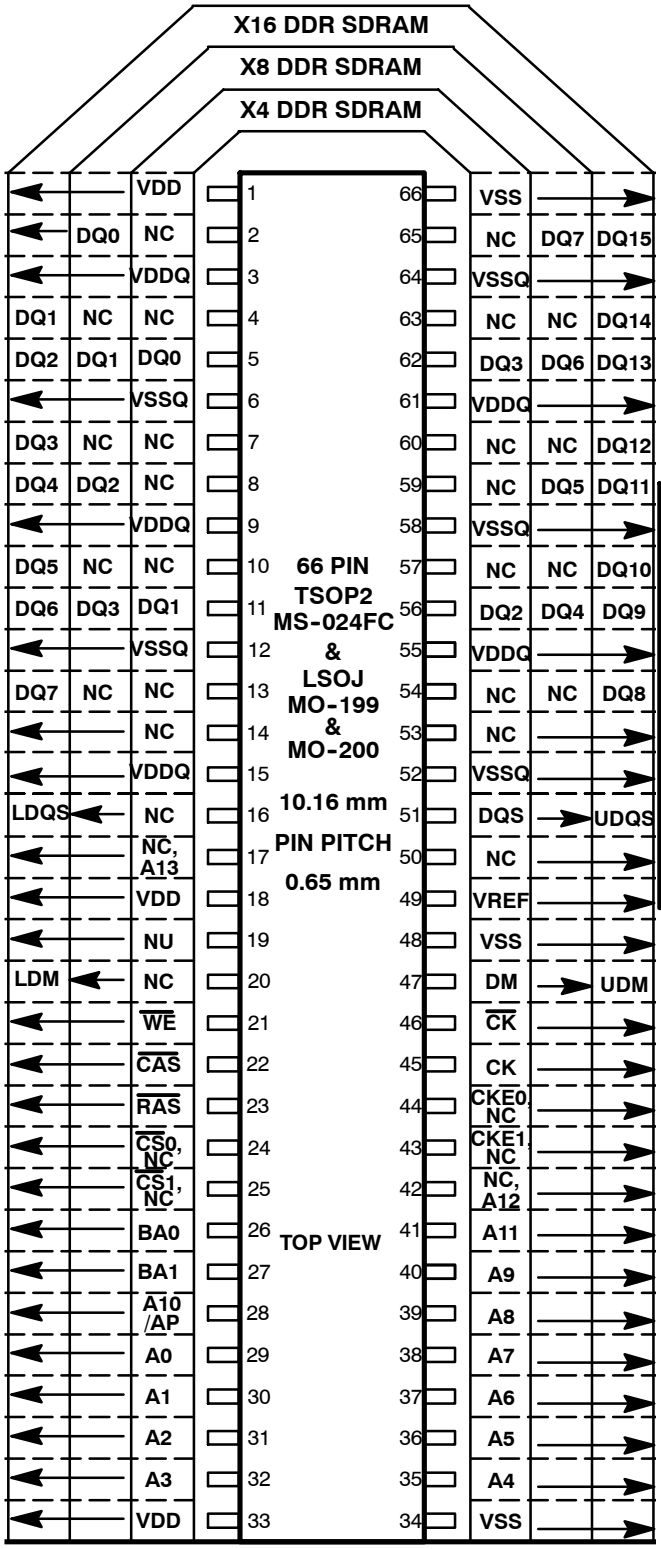


ADDRESS ASSIGNMENT TABLE					
Density	Org.	Bank	Row Addr.	Col Addr	Bank Addr
64 Mb	16M X 4	4	A0⇒A11	A0⇒A9	BA0, BA1
	8M X 8	4	A0⇒A11	A0⇒A8	BA0, BA1
	4M X 16	4	A0⇒A11	A0⇒A7	BA0, BA1
128 Mb	32M X 4	4	A0⇒A11	A0⇒A9, A11	BA0, BA1
	16M X 8	4	A0⇒A11	A0⇒A9	BA0, BA1
	8M X 16	4	A0⇒A11	A0⇒A8	BA0, BA1
256 Mb	64M X 4	4	A0⇒A12	A0⇒A9, A11	BA0, BA1
	32M X 8	4	A0⇒A12	A0⇒A9	BA0, BA1
	16M X 16	4	A0⇒A12	A0⇒A8	BA0, BA1
512 Mb	128M X 4	4	A0⇒A12	A0⇒A9,A11,A12	BA0, BA1
	64M X 8	4	A0⇒A12	A0⇒A9, A11	BA0, BA1
	32M X 16	4	A0⇒A12	A0⇒A9	BA0, BA1
1 Gb	256M X 4	4	A0⇒A13	A0⇒A9,A11,A12	BA0, BA1
	128M X 8	4	A0⇒A13	A0⇒A9,A11	BA0, BA1
	64M X 16	4	A0⇒A13	A0⇒A9	BA0, BA1

TABLE 1a: TSOP2 Device Address Assignment Table

The following pin assignments apply for $\overline{CS}$ and CKE pins for Stacked and Non-stacked devices.

Pin	Non-Stacked	Stacked	
24	$\overline{CS}$	$\overline{CS}$0	
25	NC	$\overline{CS}$1	
43	NC	CKE1	
44	CKE	CKE0	

Figure 1
64 Mb Through 1Gb DDR SDRAM (X4, X8, & X16) IN TSOP2 & LSOJ

(x4)

1	2	3		7	8	9
VSSQ	NC	VSS	A	VDD	NC	VDDQ
NC	VDDQ	DQ3	B	DQ0	VSSQ	NC
NC	VSSQ	NC	C	NC	VDDQ	NC
NC	VDDQ	DQ2	D	DQ1	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DM	F	NC	VDD	A13,NC
	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12,NC	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

X4 Device Ball Pattern

(x8)

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VDD	DQ0	VDDQ
NC	VDDQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VDDQ	NC
NC	VDDQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DM	F	NC	VDD	A13,NC
	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12,NC	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

X8 Device Ball Pattern

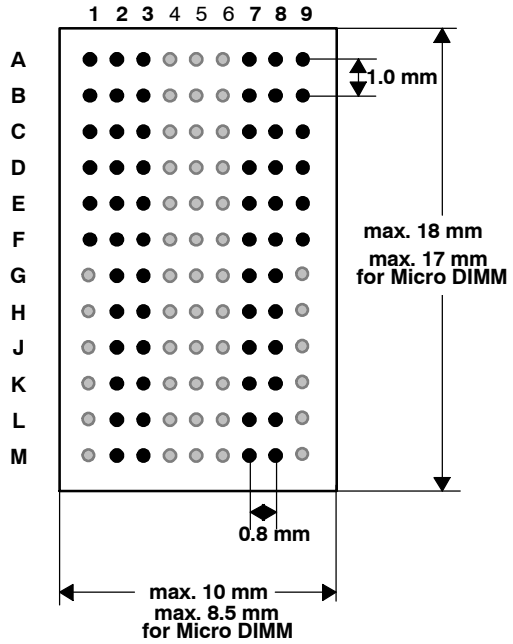
(x16)

1	2	3		7	8	9
VSSQ	DQ15	VSS	A	VDD	DQ0	VDDQ
DQ14	VDDQ	DQ13	B	DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11	C	DQ4	VDDQ	DQ3
DQ10	VDDQ	DQ9	D	DQ6	VSSQ	DQ5
DQ8	VSSQ	UDQS	E	LDQS	VDDQ	DQ7
VREF	VSS	UDM	F	LDM	VDD	A13,NC
	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12,NC	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

X16 Device Ball Pattern

● : Ball Existing **[For Reference Only]**
○ : Depopulated Ball

Top View(See the balls through the Package)

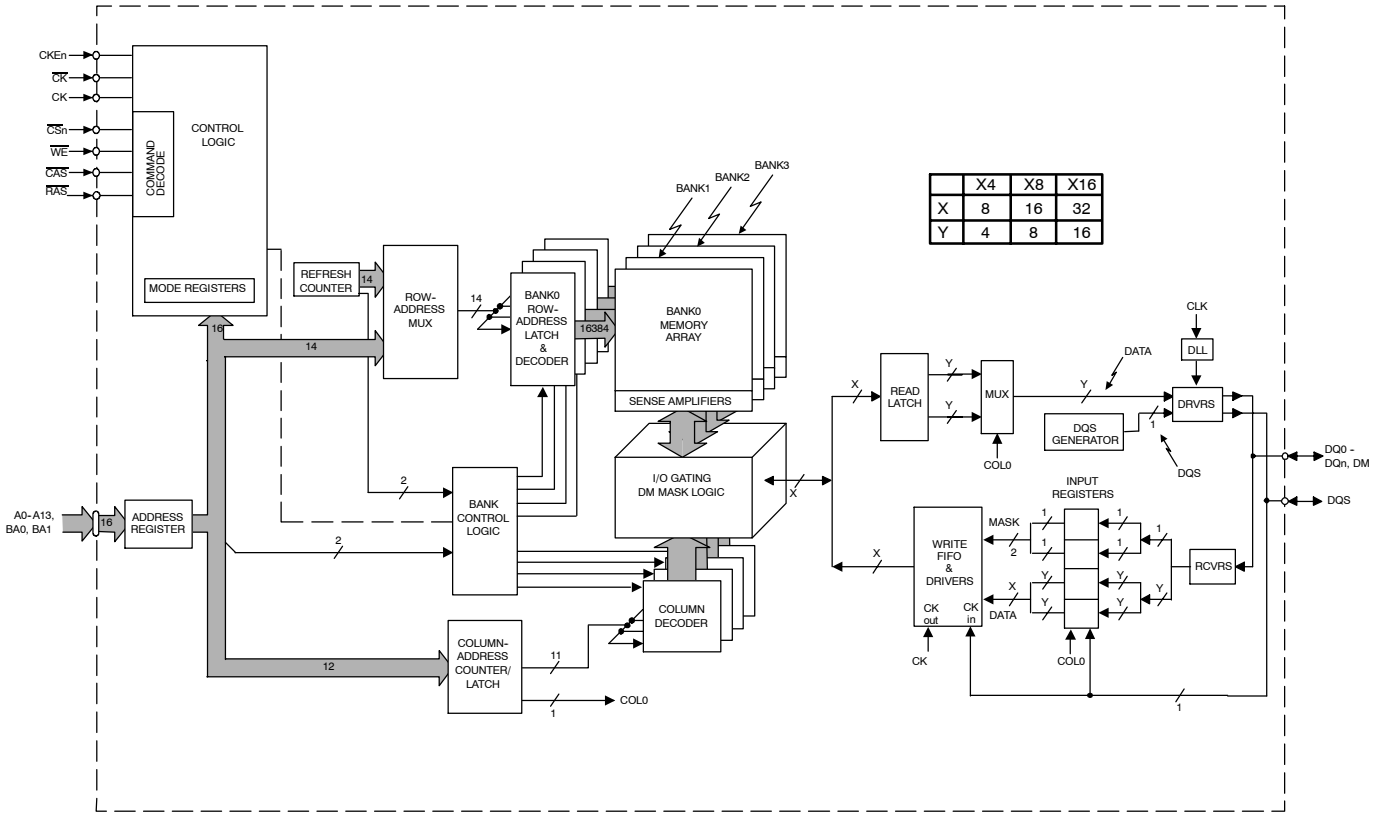


BGA Package Ball Pattern, Top View

Figure 2
128 Mb Through 1Gb DDR SDRAM (X4, X8, & X16) IN BGA

Item	128Mb	256Mb	512Mb	1Gb	Note
Number of banks	4	4	4	4	
Bank Address Pins	BA0, BA1	BA0, BA1	BA0, BA1	BA0, BA1	
Autoprecharge Pins	A10/AP	A10/AP	A10/AP	A10/AP	
Row Addresses	A0-A11	A0-A12	A0-A12	A0-A13	
Column Addresses x4 x8 x16	A0-A9,A11 A0-A9 A0-A8	A0-A9,A11 A0-A9 A0-A8	A0-A9,A11,A12 A0-A9,A11 A0-A9	A0-A9,A11,A12 A0-A9,A11 A0-A9	
H2 pin function	NC	A12	A12	A12	
F13 pin function	NC	NC	NC	A13	
JC11 MO #	MO-233A	MO-233A	MO-233A	MO-233A	
JC11 Variation #	AA	AA	AA	AA	
JC11 Package Name	DSBGA	DSBGA	DSBGA	DSBGA	
Pin Pitch	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	

TABLE 1b: BGA Device Address Assignment and Package Table



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Note 3: Not all address inputs are used on all densities.

FIGURE 3: FUNCTIONAL BLOCK DIAGRAM OF DDR SDRAM

TABLE 2: PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE (CKE0) (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during POWER-DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied upon 1st power up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be maintained to this input The standard pinout includes one CKE pin. Optional pinouts include CKE0 and CKE1 on different pins, to facilitate device stacking.
$\overline{CS}$ ($\overline{CS}$0) ($\overline{CS}$1)	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin. Optional pinouts include $\overline{CS}$0 and $\overline{CS}$1 on different pins, to facilitate device stacking.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (LDM) (UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the X16, LDM corresponds to the data on DQ0-DQ7; UDM corresponds to the data on DQ8-DQ15. DM may be driven high, low, or floating during READs.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0-A13	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS). A12 is used on device densities of 256Mb and above; A13 is used on device densities of 1Gb.
DQ	I/O	Data Bus: Input/Output.
DQS (LDQS) (UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the X16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15.
NC	—	No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: +2.5 V ±0.2 V. for DDR 200, 266, or 333 . . . . . +2.6 ±0.1 V for DDR 400
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply: One of +3.3 V ±0.3 V or +2.5 V ±0.2 V for DDR 200, 266, or 333 . . . . . +2.6 ±0.1 V for DDR 400
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

FUNCTIONAL DESCRIPTION

The DDR SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:
64Mb has 67,108,864 bits
128Mb has 134,217,728 bits
256Mb has 268,435,456 bits
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The DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins. DQ, DQS, & DM may be floated when no data is being transferred

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A13 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. No power sequencing is specified during power up and power down given the following criteria:

- VDD and VDDQ are driven from a single power converter output, AND
- VTT is limited to 1.35 V, AND
- VREF tracks VDDQ/2

OR, the following relationships must be followed:

- VDDQ is driven after or with VDD such that VDDQ < VDD + 0.3 V AND
- VTT is driven after or with VDDQ such that VTT < VDDQ + 0.3 V, AND
- VREF is driven after or with VDDQ such that VREF < VDDQ + 0.3 V.

At least one of these two conditions must be met.

Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 μs delay prior to applying an executable command.

Once the 200 μs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any executable command. A PRECHARGE ALL command should be applied, placing the device in the "all banks idle" state.

Once in the idle state, two AUTO refresh cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

REGISTER DEFINITION

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure NO TAG. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which may be self-clearing).

Mode Register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A13 or (A12 on 256Mb/512Mb, A13 on 1Gb see figure 4) specify the operating mode.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure NO TAG. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

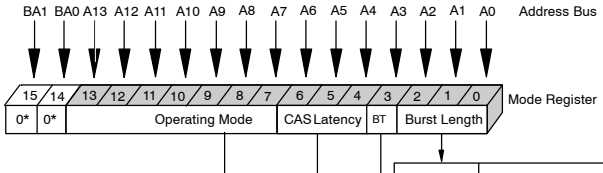
Table 3
BURST DEFINITION

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:
1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data-element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–Ai when the burst length is set to two, by A2–Ai when the burst length is set to four and by A3–Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.



* BA1 and BA0 must be 0, 0 to select the mode register (vs. the extended mode register).

A2	A1	A0	Burst Length A3 = 0	Burst Length A3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

A3	Burst Type
0	Sequential
1	Interleaved

A6	A5	A4	CAS Latency DDR 200 – 333	CAS Latency DDR 400
0	0	0	Reserved	Reserved
0	0	1	Reserved	Reserved
0	1	0	2	2
0	1	1	3 (Optional)	3
1	0	0	Reserved	Reserved
1	0	1	1.5 (optional)	1.5 (optional)
1	1	0	2.5	2.5
1	1	1	Reserved	Reserved

An – A9	A8	A7	A6-A0	Operating Mode
0	0	0	Valid	Normal Operation
0	1	0	Valid	Normal Operation/Reset DLL
0	0	1	VS	Vendor Specific Test Mode
.	.	.		All other states reserved

An = most significant address bit for this device.
VS = Vendor Specific

Figure 4
Mode Register Definition

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 3.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. For DDR200, DDR266, and DDR333, the latency can be set to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors). For DDR400, the latency can be set to 3 clocks (latencies of 2 or 2.5 are optional, and one or both of these optional latencies might be supported by some vendors).

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m.

Reserved states should not be used as unknown operation, or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set command with bits A7–A13 each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9–A13 each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. A Mode Register Set command issued to reset the DLL must always be followed by a Mode Register Set command to select normal operating mode (i.e., with A8=0).

All other combinations of values for A7–A13 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Terminology Definitions.

The following are definitions of the terms DDR200, DDR266, & DDR333, as used in this specification.

DDR200: A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency). The corresponding nominal data rate is *200 MHz.

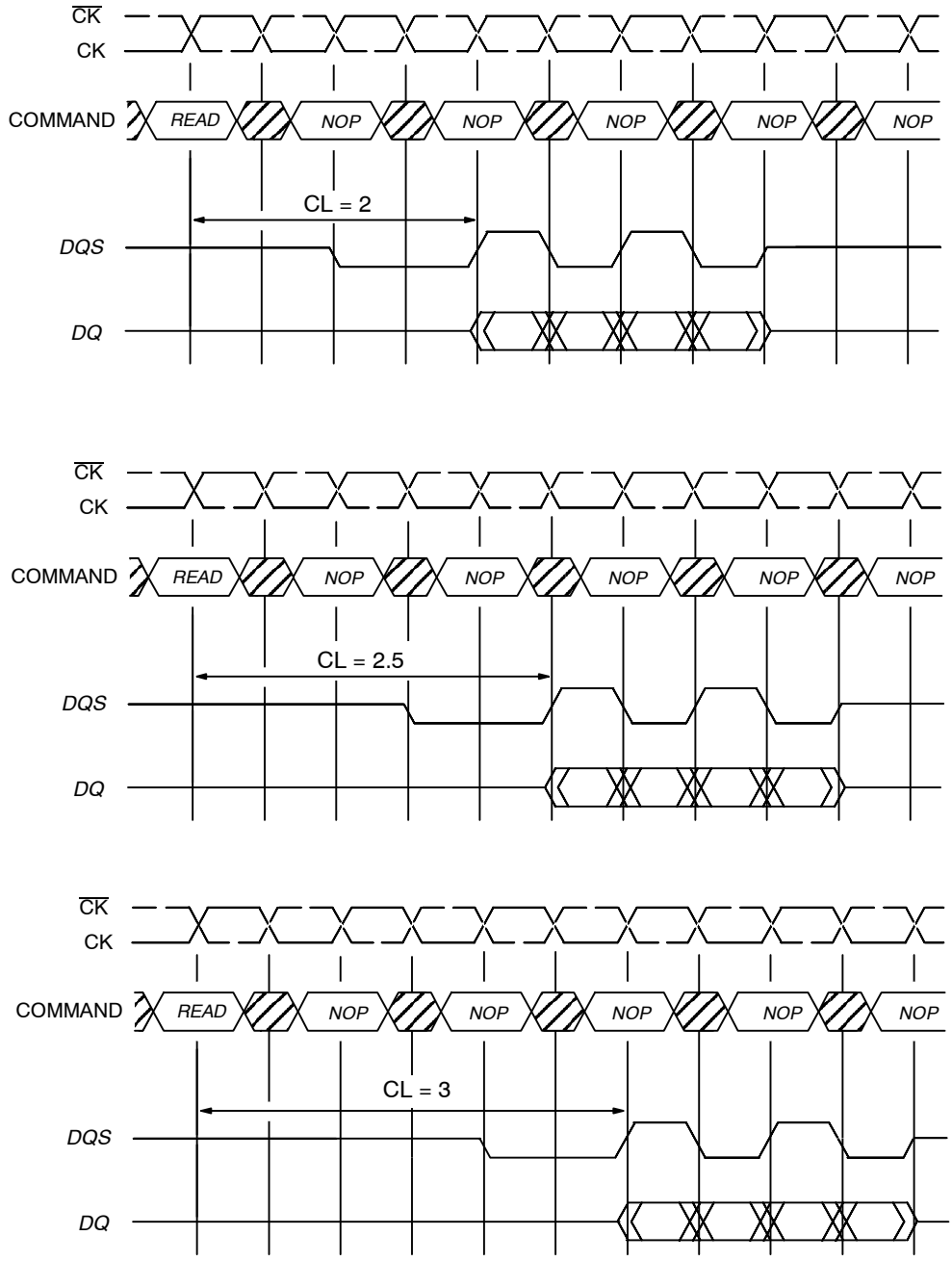
DDR266: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency). The corresponding nominal data rate is *266 MHz.

DDR333: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 167 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 167 MHz clock frequency). The corresponding nominal data rate is *333 MHz.

DDR400: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 200 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 200 MHz clock frequency). The corresponding nominal data rate is *400 MHz.

In addition to the above DDRxxx specification, a letter modifier may be applied to indicate special timing characteristics for these devices in various market applications. For example, DDR266A and DDR266B classifications define distinct sorts for operation as a function of CAS latency. These differences between sorts are described in Table 12, ”AC Timing Variations”.

* In this context, the term MHz is used loosely. A more technically precise definition is ”million transfers per second per data pin”



Burst Length = 4 in the cases shown
Shown with nominal tDQSCK

DON'T CARE

Figure 5
REQUIRED CAS LATENCIES

EXTENDED MODE REGISTER

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output drive strength selection (optional). These functions are controlled via the bits shown in Figure 6. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles must occur before any executable command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Some vendors might also support a weak driver strength option, intended for lighter load and/or point-to-point environments. I-V curves for the normal drive strength and weak drive strength are included in this document.

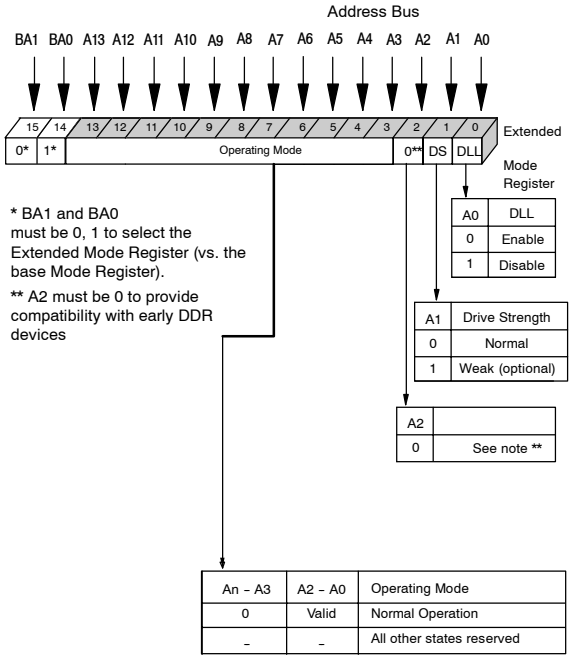


Figure 6
EXTENDED MODE REGISTER DEFINITION

COMMANDS

Truth Table 1a provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1a - Commands

(Notes: 1, 11)

NAME (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7, 12
MODE REGISTER SET	L	L	L	L	Op-Code	2

TRUTH TABLE 1b - DM Operation

NAME (Function)	DM	DQs	NOTES
Write Enable	L	Valid	10
Write Inhibit	H	X	10

NOTE: 1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0-BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A13 provide the op-code to be written to the selected Mode Register.
3. BA0-BA1 provide bank address and A0-A13 provide row address.
4. BA0-BA1 provide bank address; A0-Ai provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0-BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask write data, provided coincident with the corresponding data.
11. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
12. V_{REF} must be maintained during Self Refresh operation.

TRUTH TABLE 2 - CKE

(Notes: 1–4, 6)

CKEn–1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power–Down	X	Maintain Power–Down	
L	L	Self Refresh	X	Maintain Self Refresh	7
L	H	Power–Down	DESELECT or NOP	Exit Power–Down	
L	H	Self Refresh	DESELECT or NOP	Exit Self Refresh	5, 7
H	L	All Banks Idle	DESELECT or NOP	Precharge Power–Down Entry	
H	L	Bank(s) Active	DESELECT or NOP	Active Power–Down Entry	
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Truth Table 3		

NOTE: 1. CKEn is the logic state of CKE at clock edge n; CKEn–1 was the state of CKE at the previous clock edge.

2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.

3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.

4. All states and sequences not shown are illegal or reserved.

5. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSNR or tXSRD period. A minimum of 200 clock cycles is needed before applying any executable command, for the DLL to lock.

6. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

7. V_{REF} must be maintained during Self Refresh operation.

TRUTH TABLE 3 – Current State Bank n – Command to Bank n

(Notes: 1–6, 13; notes appear below and on next page)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start new WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	8, 11

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table is bank–specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and tRP has been met.
   - Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
   - Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the ”row active” state.
   - Read w/Auto-Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
   - Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

NOTE (continued):

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. Once tRFC is met, the DDR SDRAM will be in the ”all banks idle” state.

   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMRD is met, the DDR SDRAM will be in the ”all banks idle” state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with AUTO PRECHARGE enabled and Reads or Writes with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst Terminate must be used to end the READ prior to asserting a WRITE command,
13. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

TRUTH TABLE 4 – Current State Bank n – Command to Bank m

(Notes: 1–6, 10; notes appear below and on next page)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start WRITE burst)	3a, 7, 9
	L	L	H	L	PRECHARGE	
Write (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	3a, 7
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.

NOTE: (continued)

3. Current state definitions: (Continued)

   Read with Auto
   Precharge Enabled: See following text, notes 3a, 3b, and 3c:

   Write with Auto
   Precharge Enabled: See following text, notes 3a, 3b, and 3c:

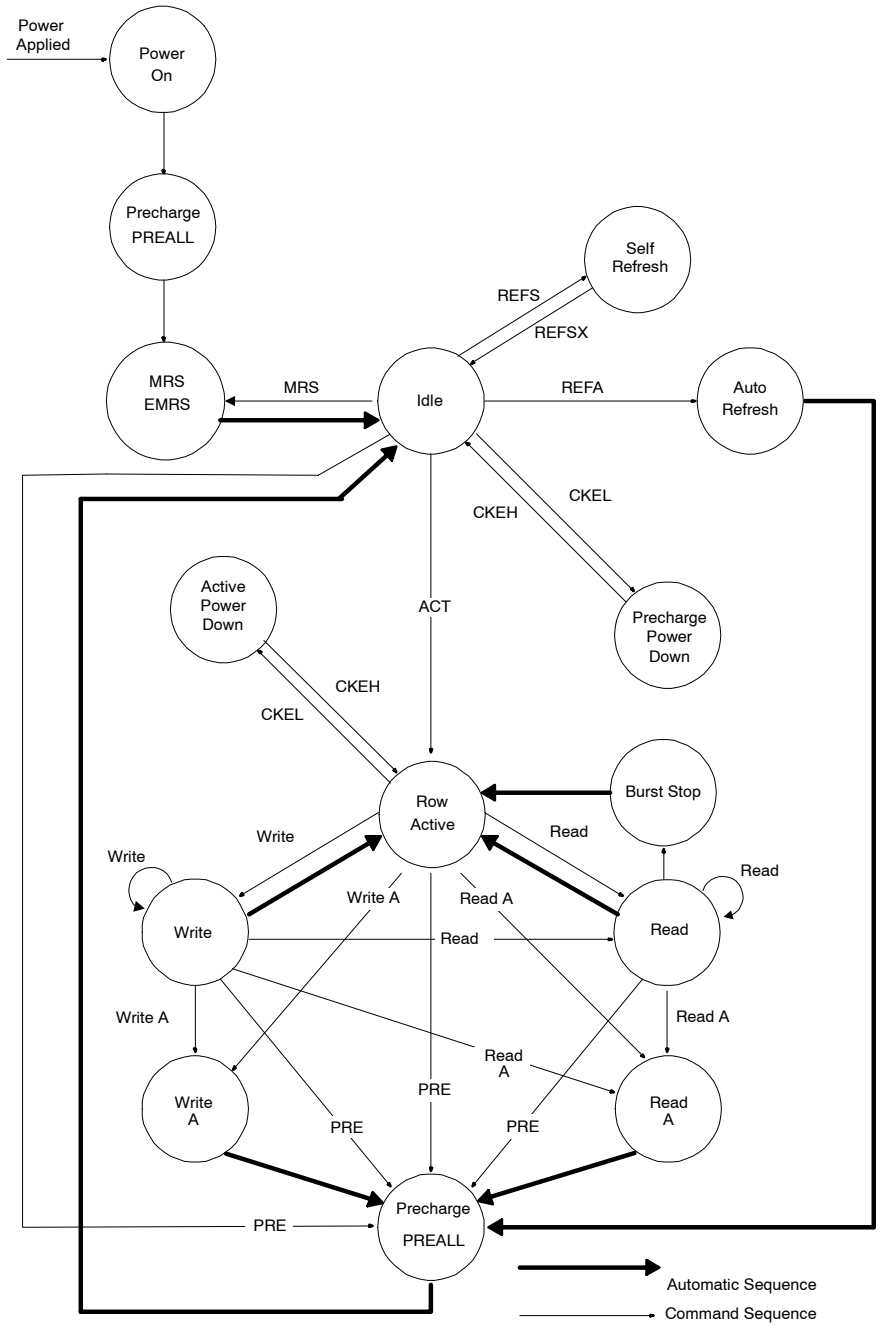
   3a. For devices which *do not support* the optional "concurrent auto precharge" feature, the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).

   3b. For devices which *do support* the optional "concurrent auto precharge" feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided.)

   3c. The minimum delay from a read or write command with auto precharge enable, to a command to a different bank, is summarized below, for both cases of "concurrent auto precharge," supported or not:

From Command	To Command (different bank)	Minimum Delay without Concurrent Auto Precharge Support	Minimum Delay with Concurrent Auto Precharge Support	Units
Write w/AP	Read or Read w/AP	1+(BL/2) + (tWR/tCK) (rounded up)	1+(BL/2) + tWTR	tCK
	Write or Write w/AP	1+(BL/2) + (tWR/tCK) (rounded up)	BL/2	tCK
	Precharge or Activate	1		tCK
Read w/AP	Read or Read w/AP	BL/2		tCK
	Write or Write w/AP	CL (rounded up) + (BL/2)		tCK
	Precharge or Activate	1		tCK

4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of data output, otherwise a Burst Terminate must be used to the READ prior to asserting a WRITE command..
10. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh
CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

Figure 7
SIMPLIFIED STATE DIAGRAM

DESELECT

The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to a DDR SDRAM which is selected ($\overline{CS}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The mode registers are loaded via inputs A0–A13. See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A13 selects the row. This row remains active (or open) for accesses until a precharge (or READ or WRITE with AUTOPRECHARGE) is issued to that bank. A PRECHARGE (or READ or WRITE with AUTOPRECHARGE) command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai, shown in Table 4, selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai, shown in Table 4, selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

Density	Column Address			Row Address
	X16	X8	X4	
64 Mb	A0⇒A7	A0⇒A8	A0⇒A9	A0⇒A11
128 Mb	A0⇒A8	A0⇒A9	A0⇒A9,A11	A0⇒A11
256 Mb	A0⇒A8	A0⇒A9	A0⇒A9,A11	A0⇒A12
512 Mb	A0⇒A9	A0⇒A9,A11	A0⇒A9,A11,A12	A0⇒A12
1 Gb	A0⇒A9	A0⇒A9,A11	A0⇒A9,A11,A12	A0⇒A13

Table 4

ROW-COLUMN ORGANIZATION BY DENSITY

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual Read or Write command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

REFRESH REQUIREMENTS

DDR SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64 ms interval defines the average refresh interval, tREFI, which is a guideline to controllers for distributed refresh timing. For example, a 256 Mb DDR SDRAM has 8192 rows resulting in a tREFI of 7.8 μs. To avoid excessive interruptions to the memory controller, higher density DDR SDRAMs maintain the 7.8 μs average refresh time and perform multiple internal refresh bursts. In these cases, the refresh recovery times, tRFC and tXSNR, are extended to accommodate these internal operations.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS–BEFORE–RAS (CBR) refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of tREFI (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 * tREFI.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH. Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles should occur before a READ command can be issued. Input signals except CKE are "Don't Care" during SELF REFRESH. Since CKE is an SSTL 2 input, V_{REF} must be maintained during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra auto refresh command is recommended.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be ”opened.” This is accomplished via the ACTIVE command (Figure 8), which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been ”closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row–access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

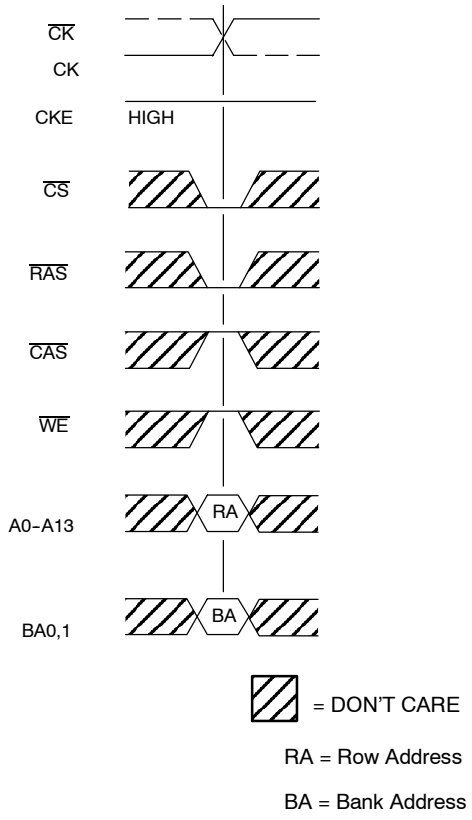


Figure 8
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

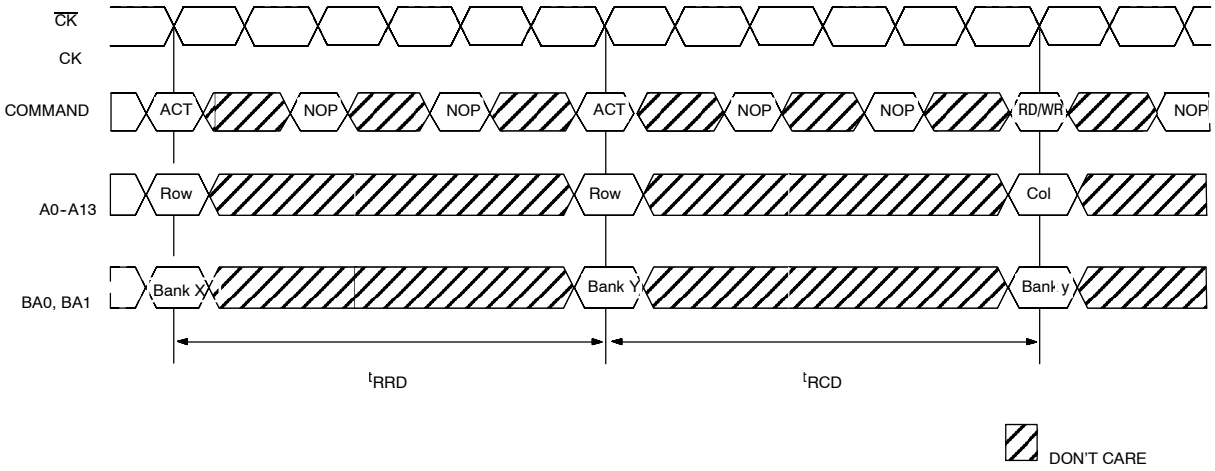


Figure 9
tRCD and tRRD Definition

Reads

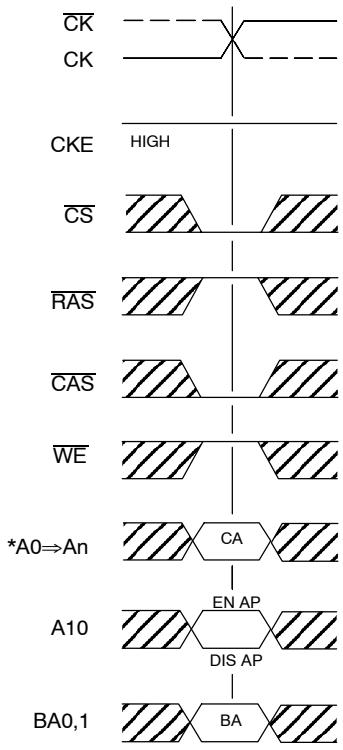
READ bursts are initiated with a READ command, as shown in Figure 10.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row that is accessed will start precharge at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and $\overline{CK}$). Figure 11 shows general timing for each required (CL=2 and CL=2.5 and CL=3) CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 12. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive READ data is shown for illustration in Figure 13. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 14.



= DON'T CARE
CA = Column Address
BA = Bank Address
EN AP = Enable Autoprecharge
DIS AP = Disable Autoprecharge
* See Address tables on PP 3 & 5

Figure 10
READ COMMAND

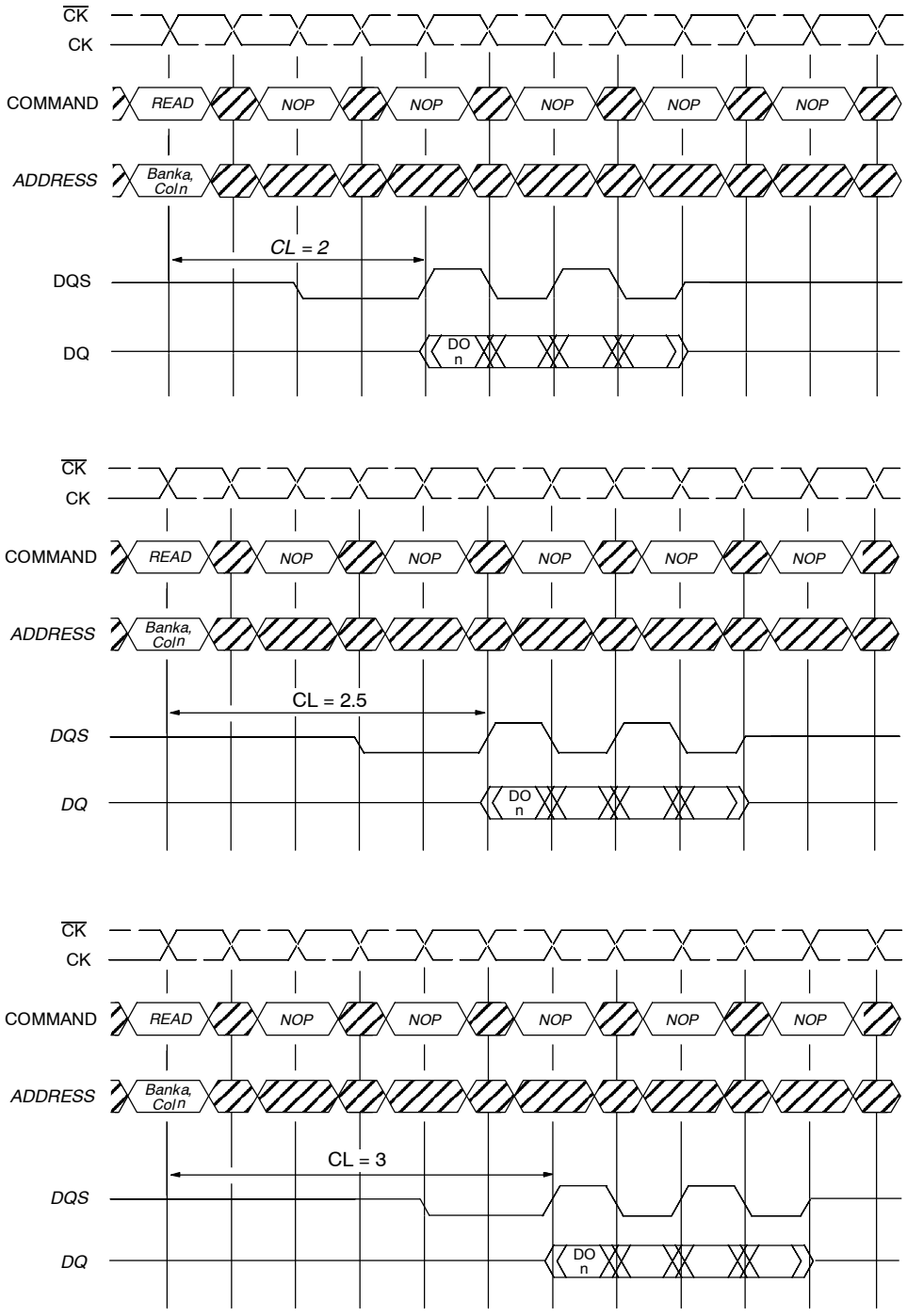
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 15. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command, where X equals the number of desired data element pairs.

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued.

If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 16. The tDQSS MIN case is shown; the tDQSS MAX case has a longer bus idle time (tDQSS MIN and tDQSS MAX are defined in the section on WRITEs).

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 17 for READ latencies of 2 and 2.5. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data elements.

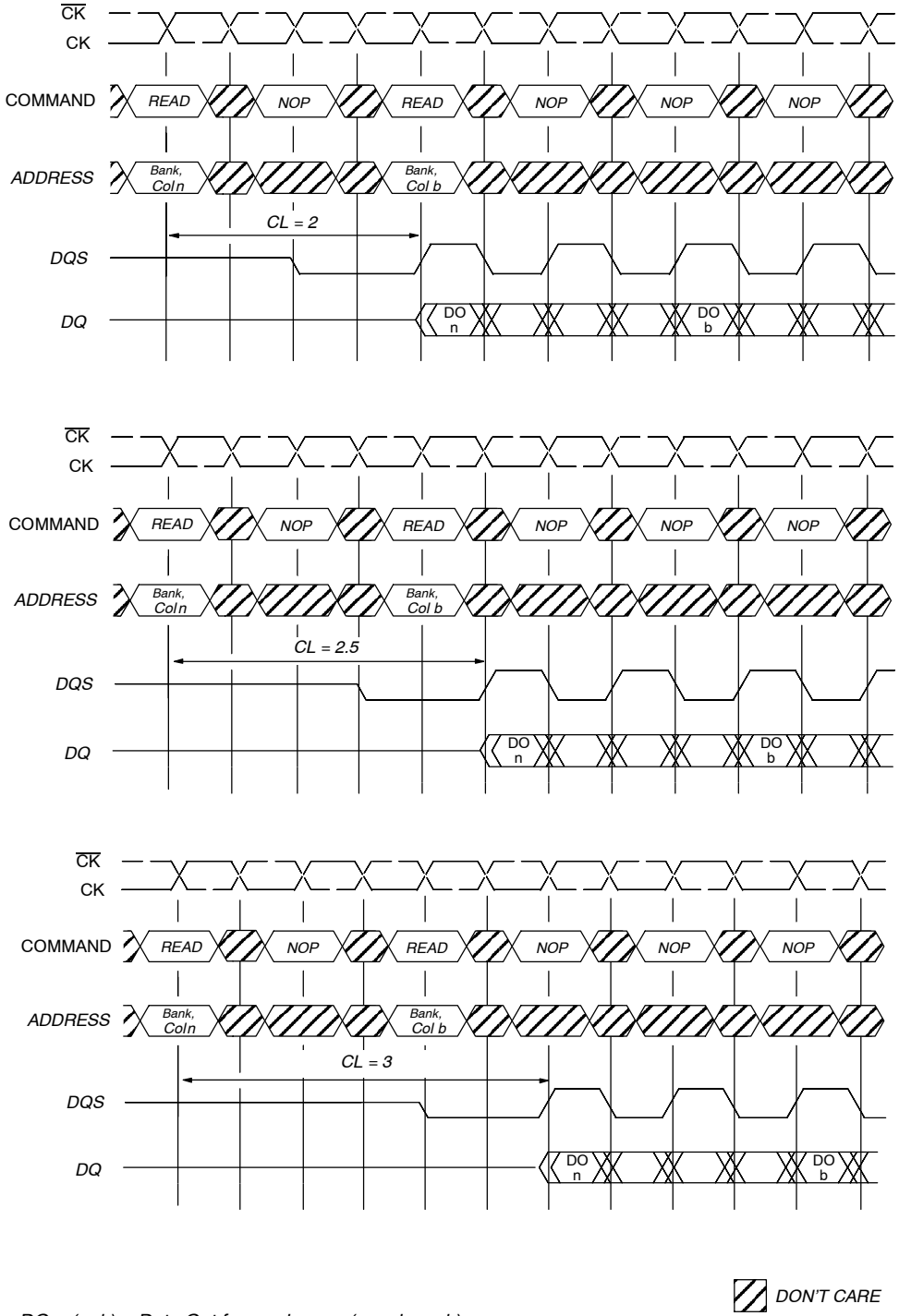
In the case of a READ being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with AUTO PRECHARGE enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.



DO n = Data Out from column n
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n

DON'T CARE

Figure 11
READ BURST - REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)

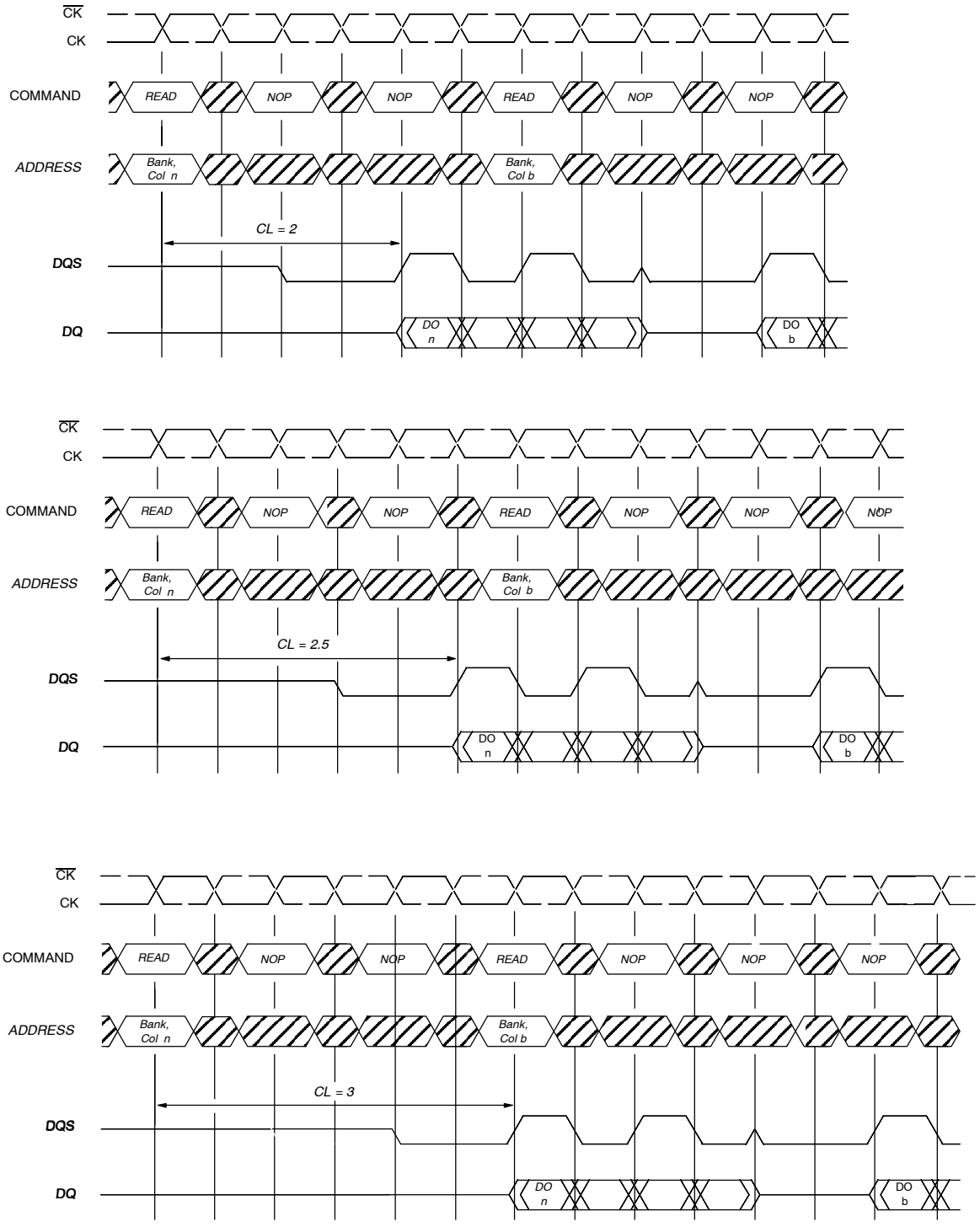
Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)

3 subsequent elements of Data Out appear in the programmed order following DO n

3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b

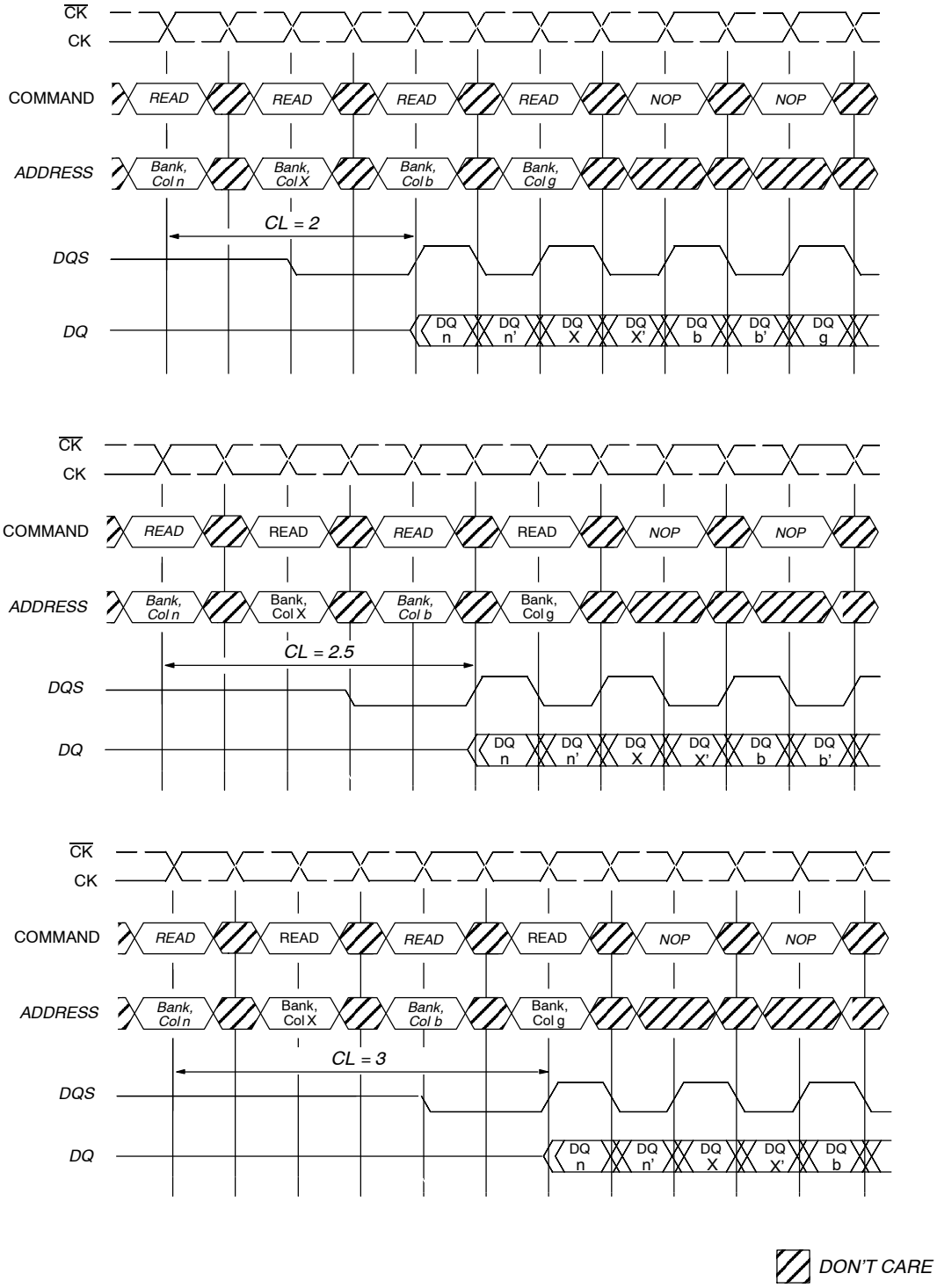
Read commands shown must be to the same device

Figure 12
CONSECUTIVE READ BURSTS - REQUIRED CAS LATENCIES



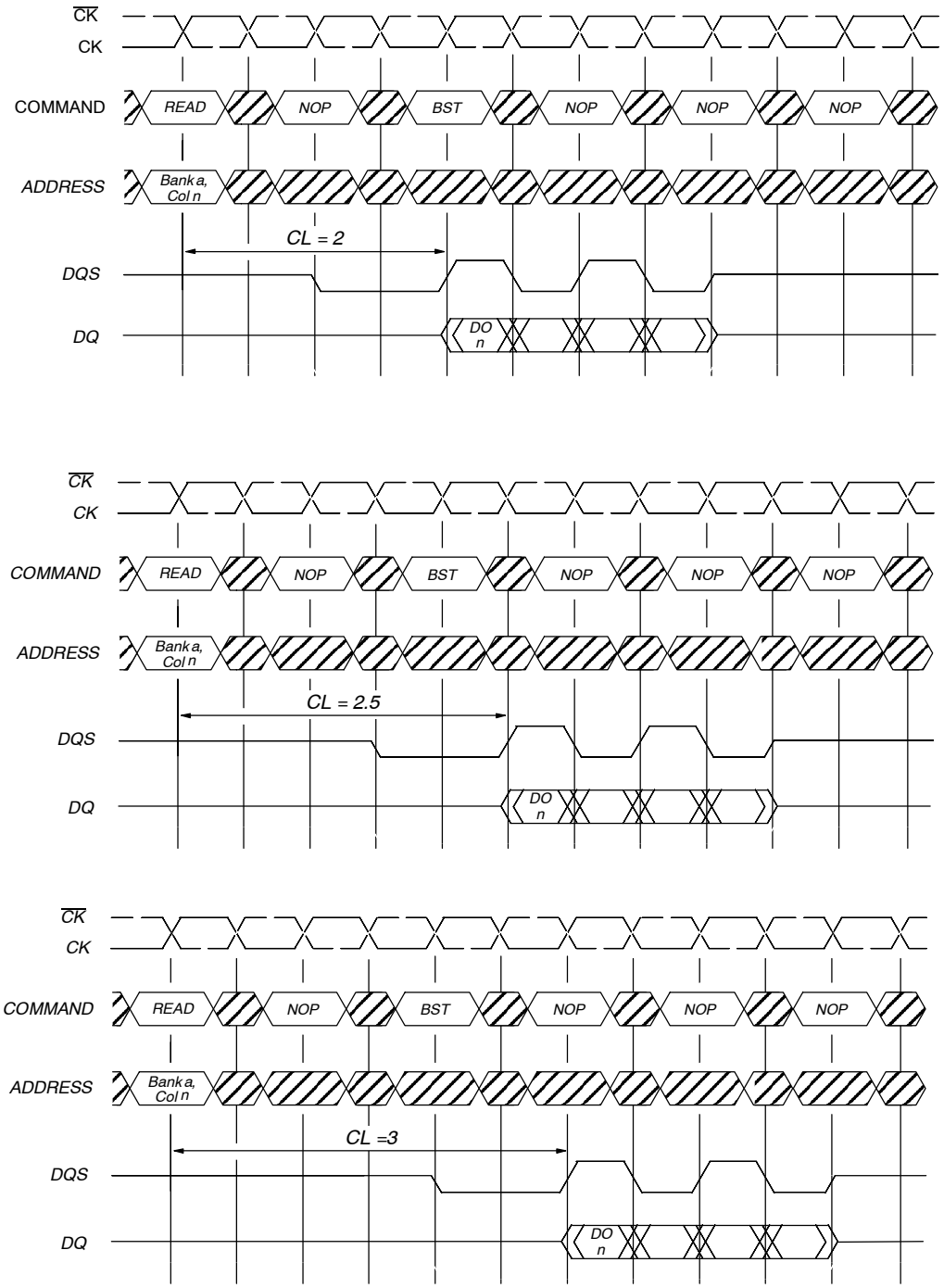
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)

Figure 13
NONCONSECUTIVE READ BURSTS - REQUIRED CAS LATENCIES



DO n, etc. = Data Out from column n, etc.
n' , etc. = the next Data Out following DO n, etc. according to the programmed burst order
Burst Length = 2, 4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted,
Reads are to active rows in any banks

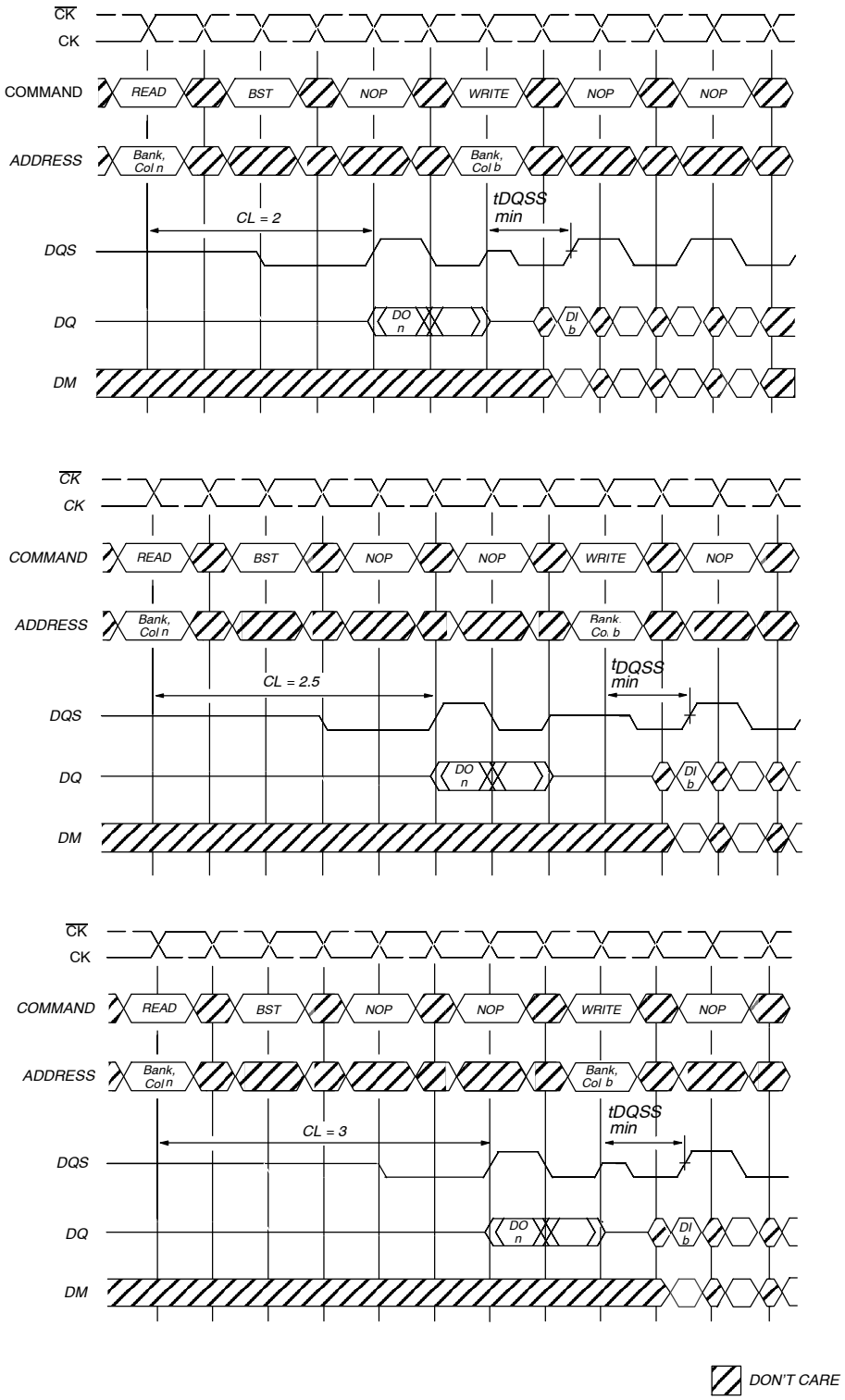
Figure 14
RANDOM READ ACCESSES - REQUIRED CAS LATENCIES



DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n

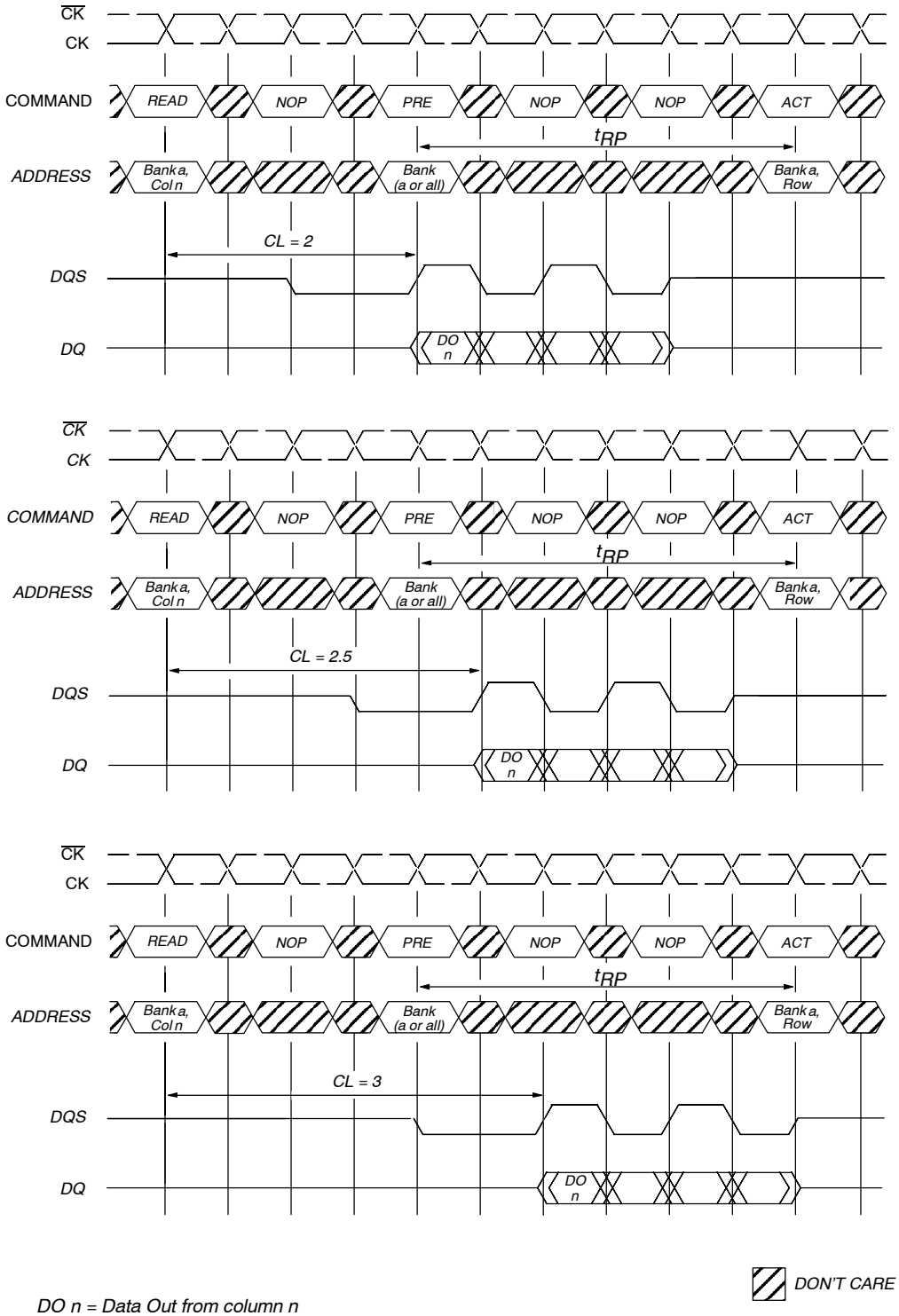
DON'T CARE

Figure 15
TERMINATING A READ BURST - REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
1 subsequent element of Data Out appears in the programmed order following DO n
Data In elements are applied following DI b in the programmed order

Figure 16
READ TO WRITE - REQUIRED CAS LATENCIES



DO n = Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n
Precharge may be applied at (BL/2) tCK after the READ command.
Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
The Active command may be applied if tRC has been met.

Figure 17
READ TO PRECHARGE - REQUIRED CAS LATENCIES

Writes

WRITE bursts are initiated with a WRITE command, as shown in Figure 18.

The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, AUTO PRECHARGE is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the write command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle). Figures 19 and 20 show the two extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Figure 22 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 23. Full-speed random write accesses within a page or pages can be performed as shown in Figure 24.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the write burst, tWTR should be met as shown in Figure 25

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figures 26. and 27 Note that only the data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in must be masked with DM, as shown in Figures 26 and 27.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the write burst, tWR should be met as shown in Figure 28.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figures 29 and 30.

Note that only the data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figures 29 and 30. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

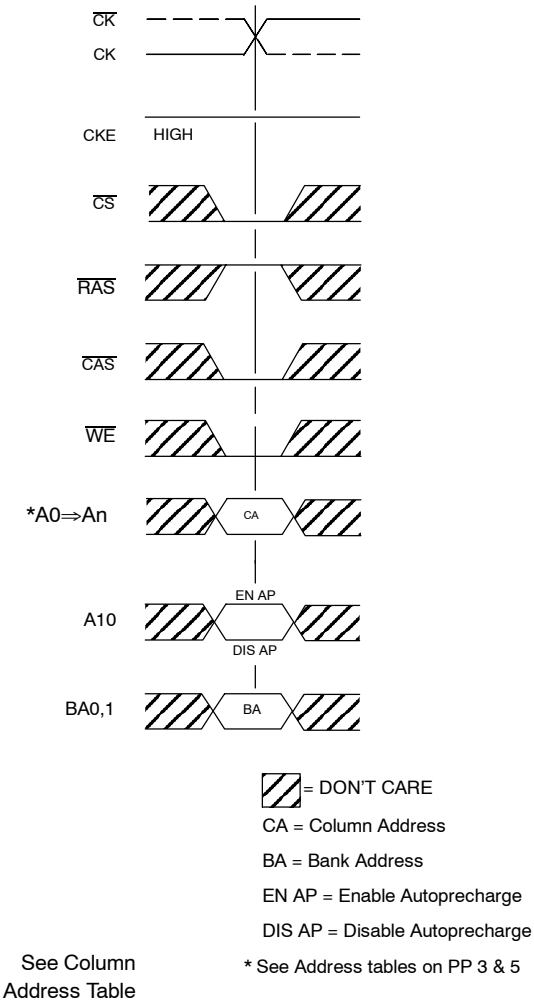
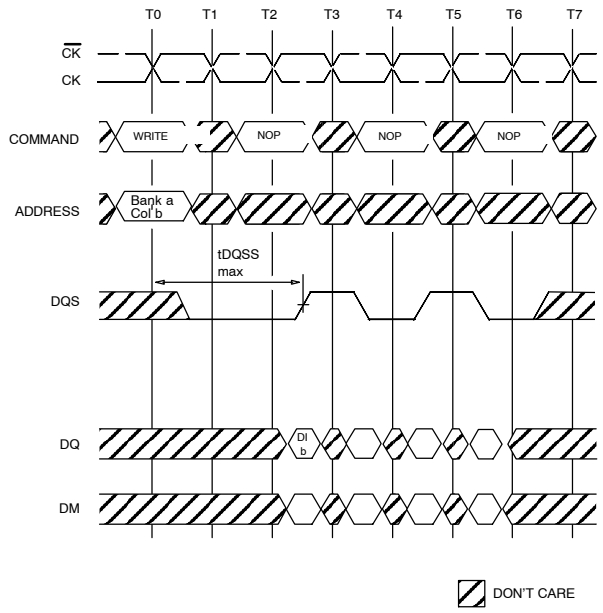
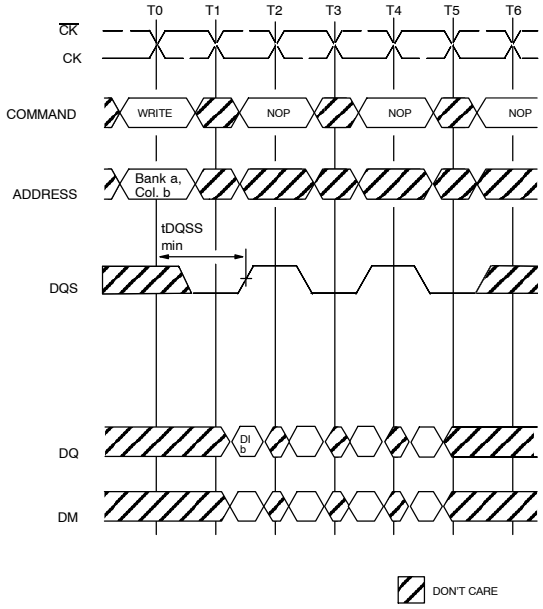


Figure 18
WRITE COMMAND



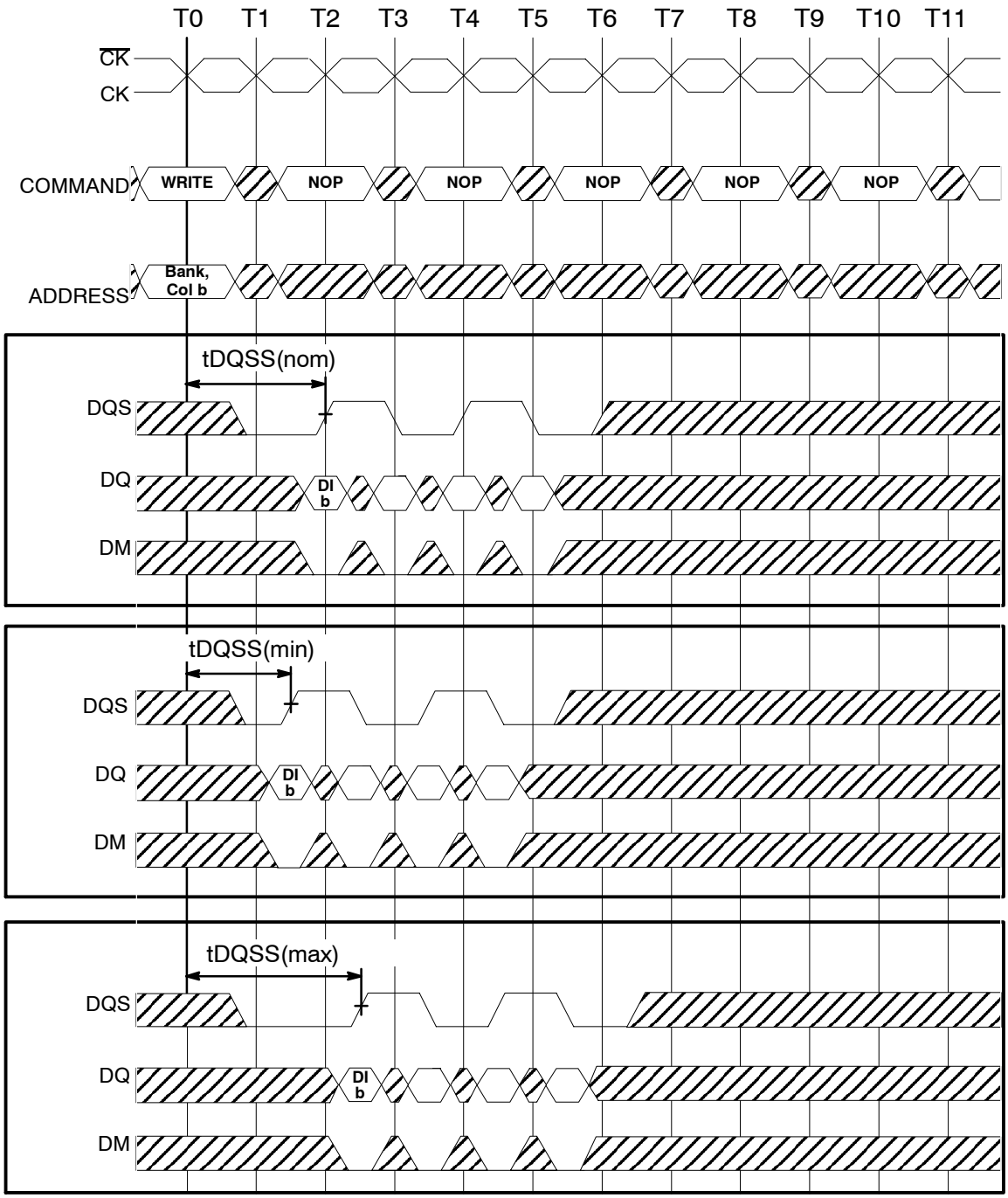
DI b = Data in for column b
3 subsequent elements of Data IN are applied in the programmed order following Di b
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

Figure 19
WRITE - MAX DQSS



DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

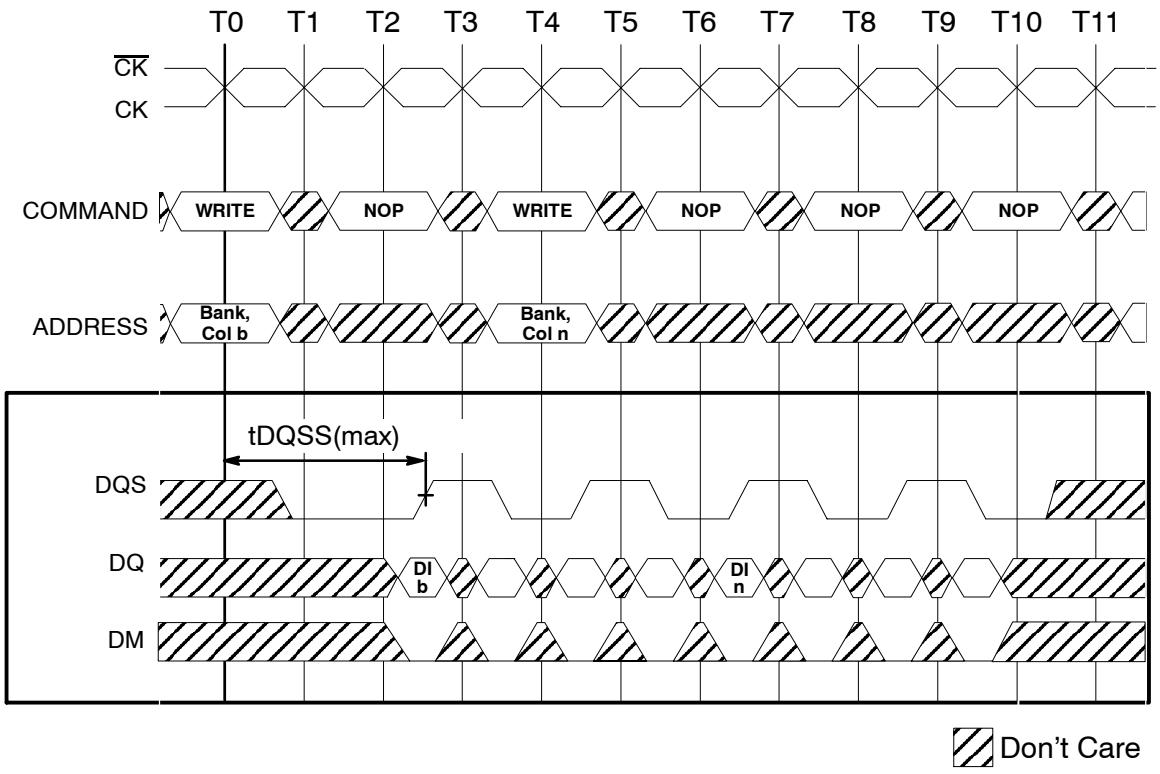
Figure 20
WRITE - MIN DQSS



DI b = Data In for column b
Three elements of data are applied in the programmed order following DI
A noninterrupted burst of 4 is shown
A10 is low with the WRITE command (autoprecharge is disabled)
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

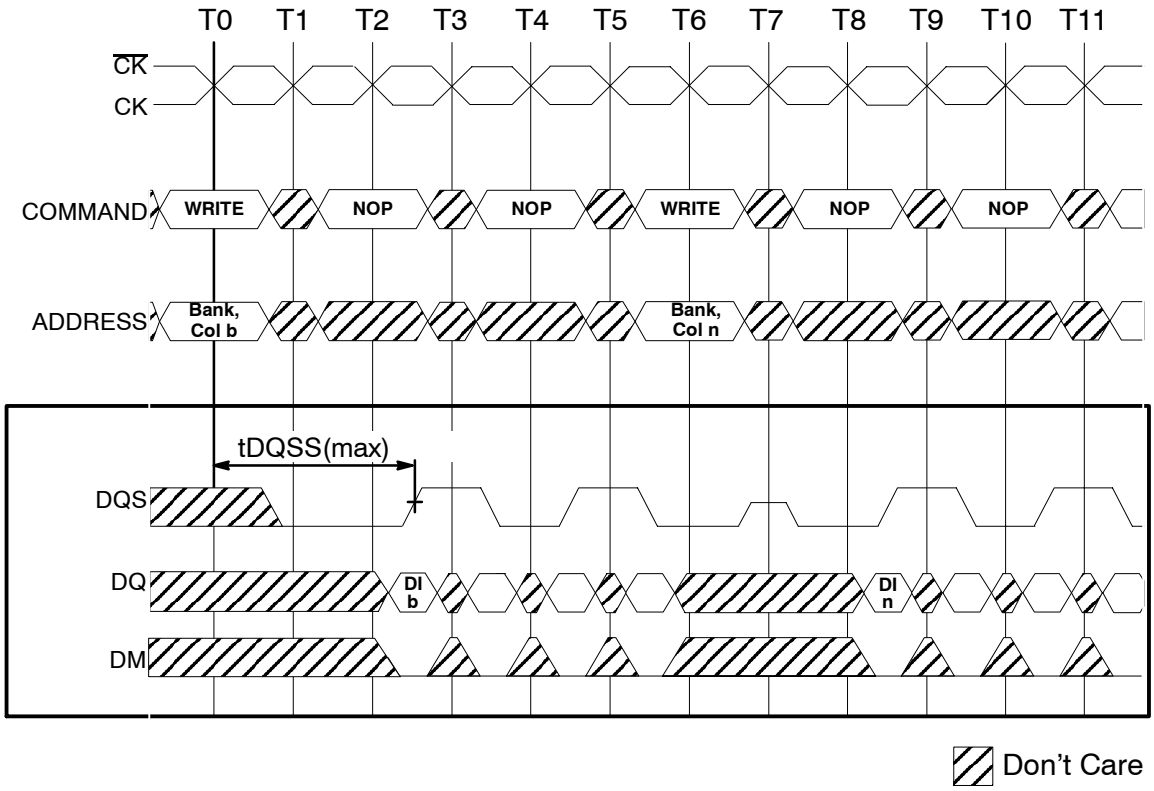
Don't Care

Figure 21
WRITE BURST – Nom., Min., and Max tDQSS



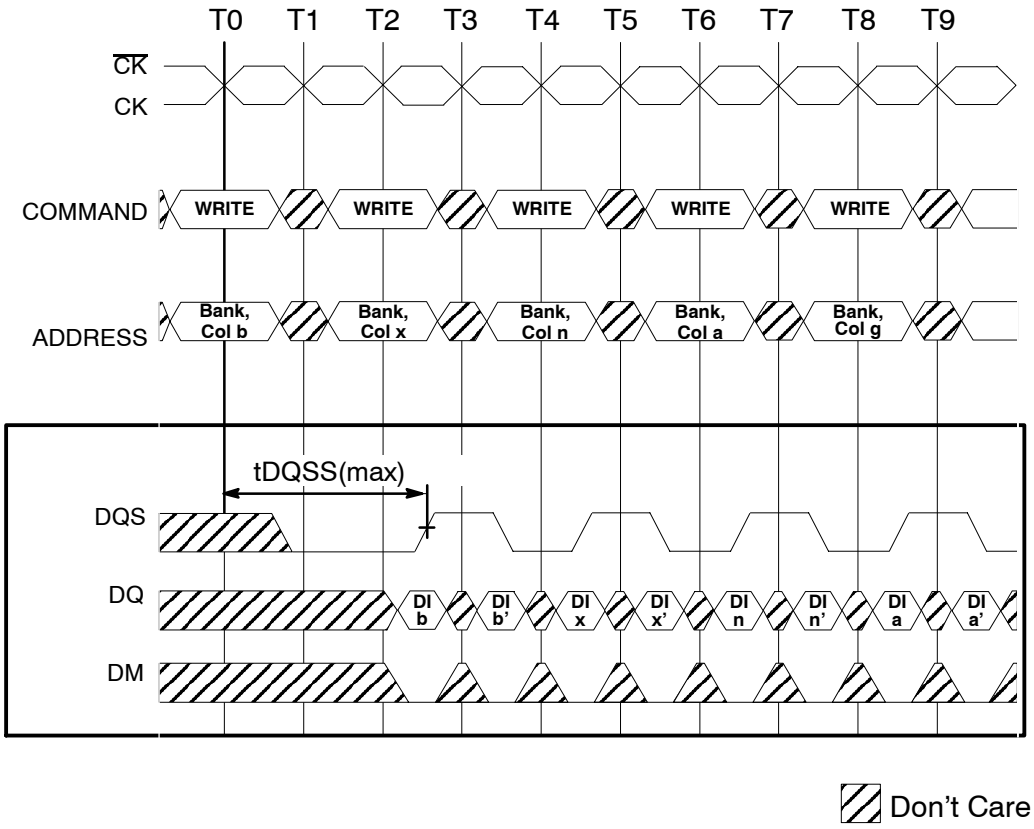
DI b, etc. = Data In for column b, etc.
Three subsequent elements of Data In are applied in the programmed order following DI b
Three subsequent elements of Data In are applied in the programmed order following DI n
Noninterrupted bursts of 4 are shown
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 22
WRITE TO WRITE – Max tDQSS



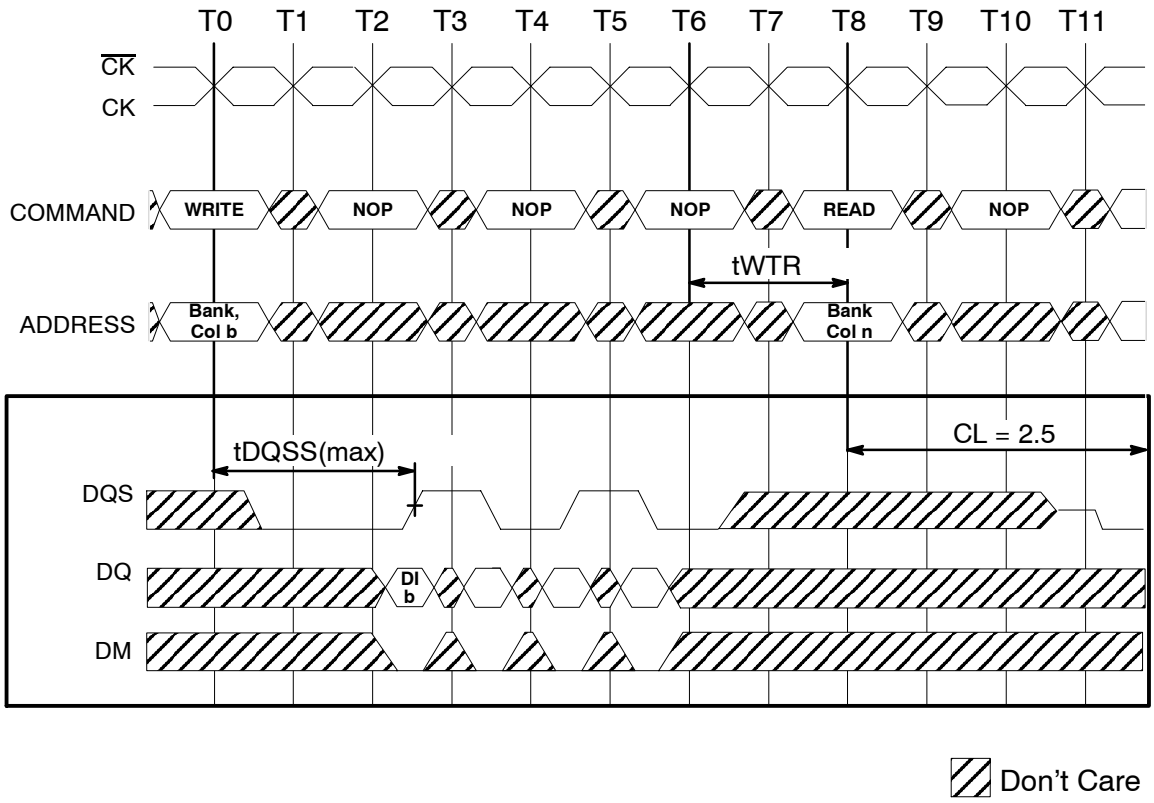
DI b, etc. = Data In for column b, etc.
Three subsequent elements of Data In are applied in the programmed order following DI b
Three subsequent elements of Data In are applied in the programmed order following DI n
Noninterrupted bursts of 4 are shown
Each WRITE command may be to any bank and may be to the same or different devices
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 23
WRITE TO WRITE – Max tDQSS, NON CONSECUTIVE



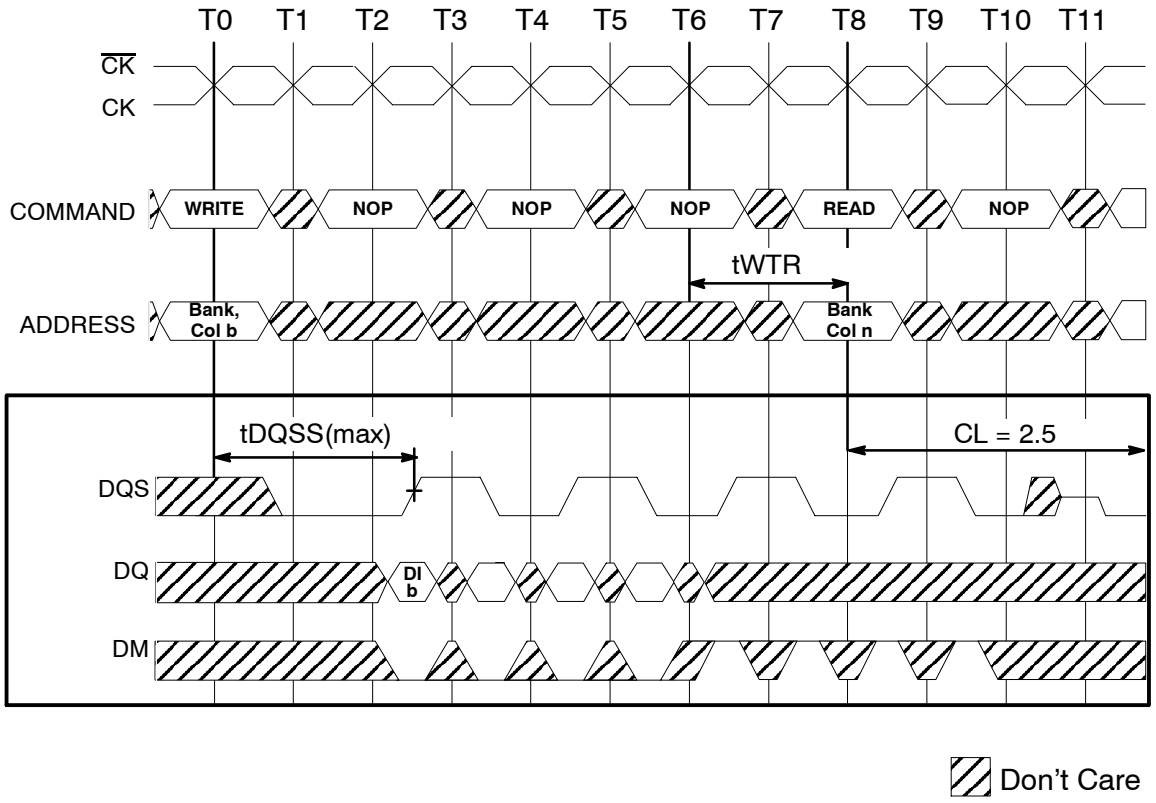
DI b, etc. = Data In for column b, etc.
b', etc. = the next Data In following DI b, etc. according to the programmed burst order.
Programmed Burst Length = 2, 4, or 8 in cases shown.
If burst of 4 or 8, the burst would be truncated.
Each WRITE command may be to any bank and may be to the same or different devices.
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 24
RANDOM WRITE CYCLES - Max tDQSS



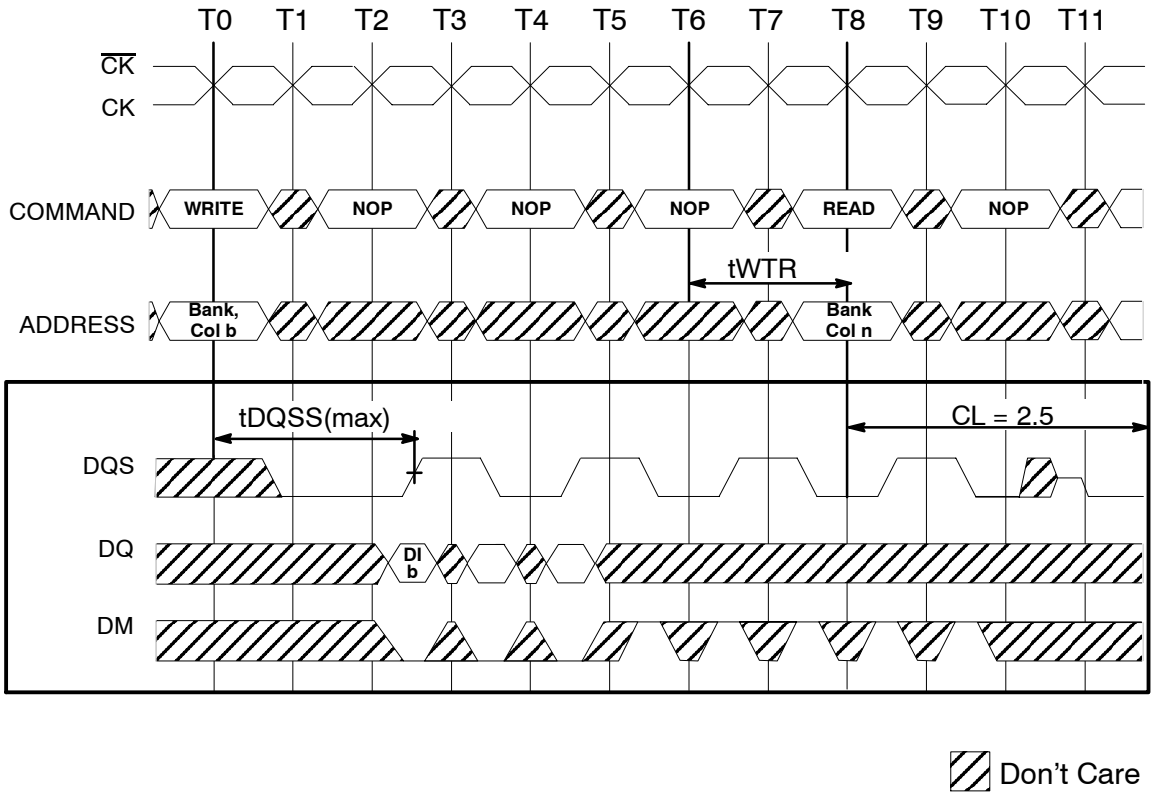
DI b = Data In for column b
Three subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
tWTR is referenced from the first positive CK edge after the last Data In pair
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1tCK)
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device but not necessarily to the same bank
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 25
WRITE TO READ - Max tDQSS, NON-INTERRUPTING



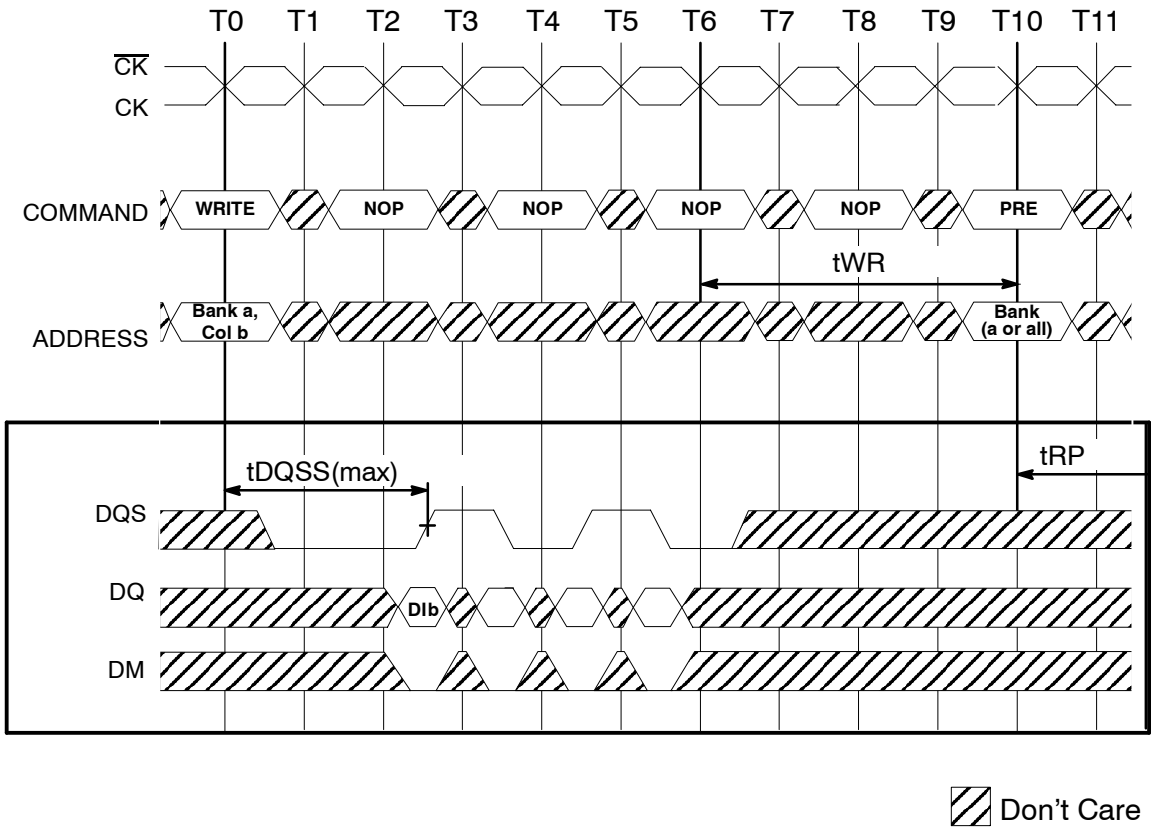
DI b = Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
Three subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last Data In pair
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1tCK)
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device but not necessarily to the same bank
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 26
WRITE TO READ - Max tDQSS, INTERRUPTING



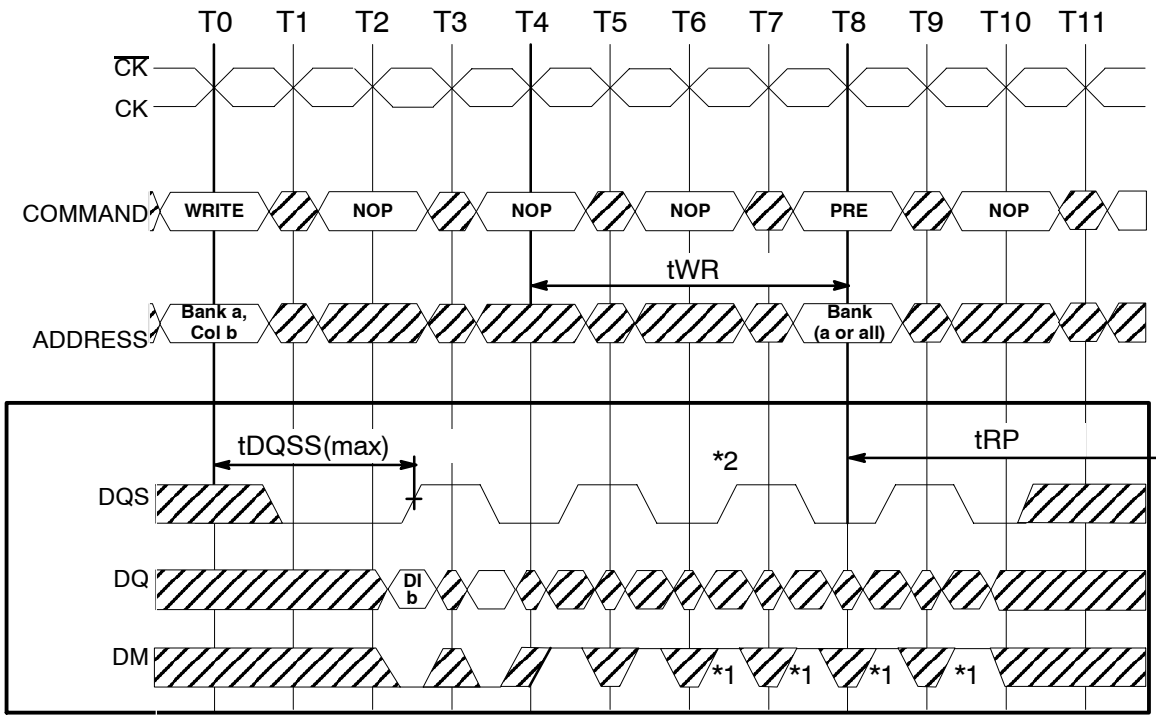
DI b = Data In for column b
An interrupted burst of 8 is shown, 3 data elements are written
Two subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last Data In pair (not the last desired Data In element)
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1tCK)
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
Example is for x4 or x8 devices where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.
The READ and WRITE commands are to the same device but not necessarily to the same bank.

Figure 27
WRITE TO READ - Max tDQSS, ODD NUMBER OF DATA, INTERRUPTING



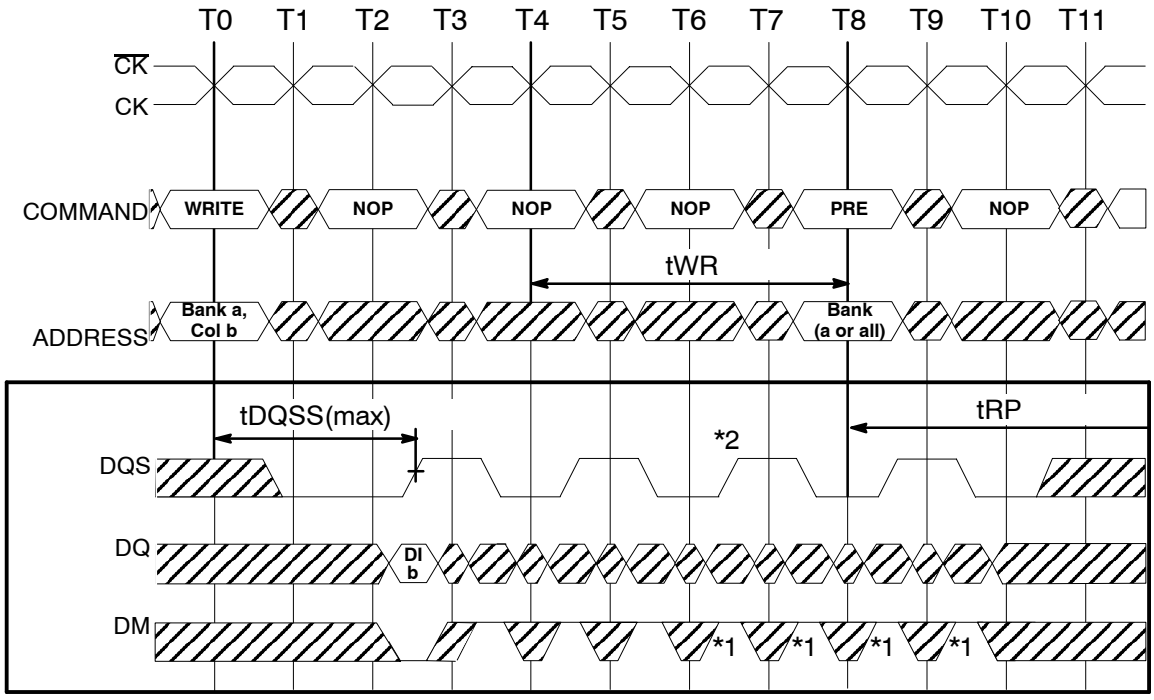
DI b = Data In for column b
Three subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
tWR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 28
WRITE TO PRECHARGE - Max tDQSS, NON-INTERRUPTING



DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
tWR is referenced from the first positive CK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 29
WRITE TO PRECHARGE - Max tDQSS, INTERRUPTING



DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 1 data element is written
tWR is referenced from the first positive CK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 30
WRITE TO PRECHARGE - Max tDQSS,
ODD NUMBER OF DATA, INTERRUPTING

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

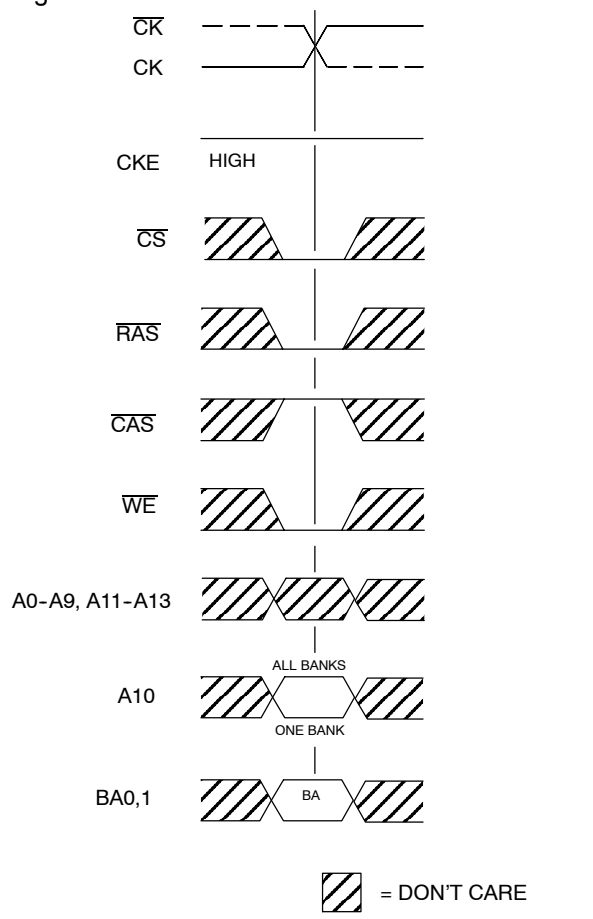


Figure 31
PRECHARGE COMMAND

POWER-DOWN

Power-down is entered when CKE is registered low (no accesses can be in progress and Table 2 criteria must be met). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a READ command can be issued. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self-refresh mode is preferred over the DLL-disabled power-down mode.

In power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are "Don't Care".

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

Input Clock Frequency Change during Precharge Power Down

DDR SDRAM input clock frequency can be changed under following condition:

DDR SDRAM must be in precharged power down mode with CKE at logic LOW level. After a minimum of 2 clocks after CKE goes LOW, the clock frequency may change to any frequency between minimum and maximum operating frequency specified for the particular speed grade. During an input clock frequency change, CKE must be held LOW. Once the input clock frequency is changed, a stable clock must be provided to DRAM before precharge power down mode may be exited. The DLL must be RESET via EMRS after precharge power down exit. An additional MRS command may need to be issued to appropriately set CL etc.. After the DLL relock time, the DRAM is ready to operate with new clock frequency.

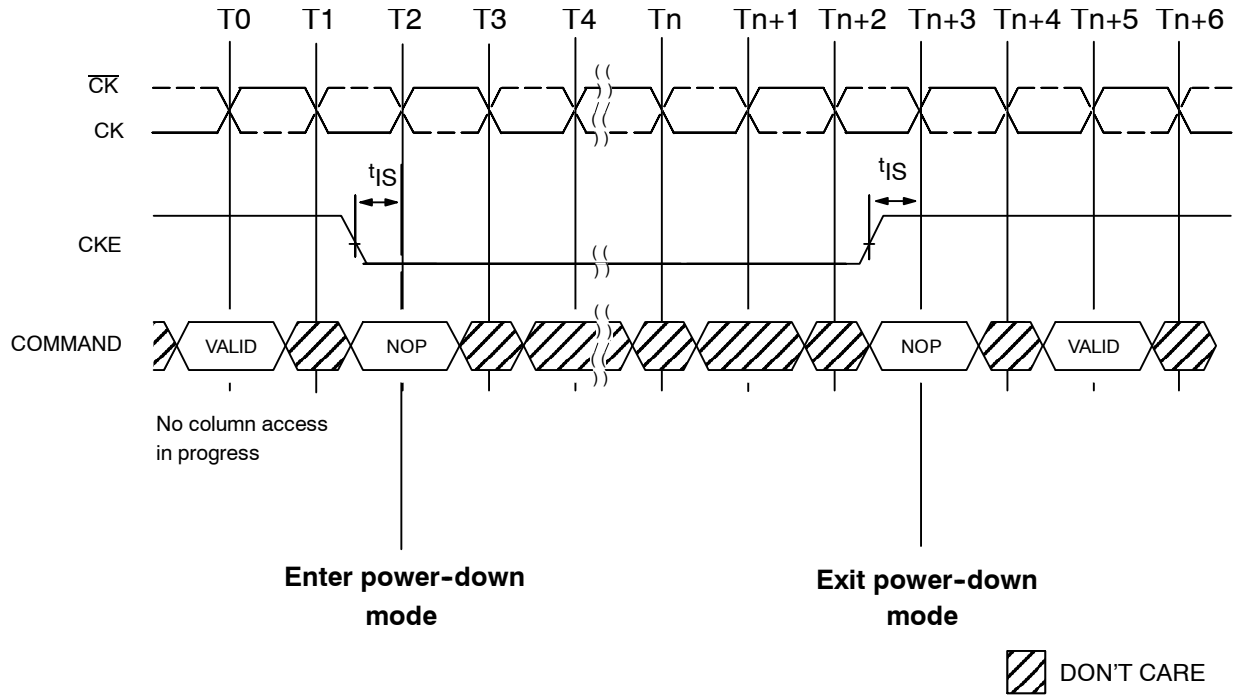


Figure 32
POWER-DOWN

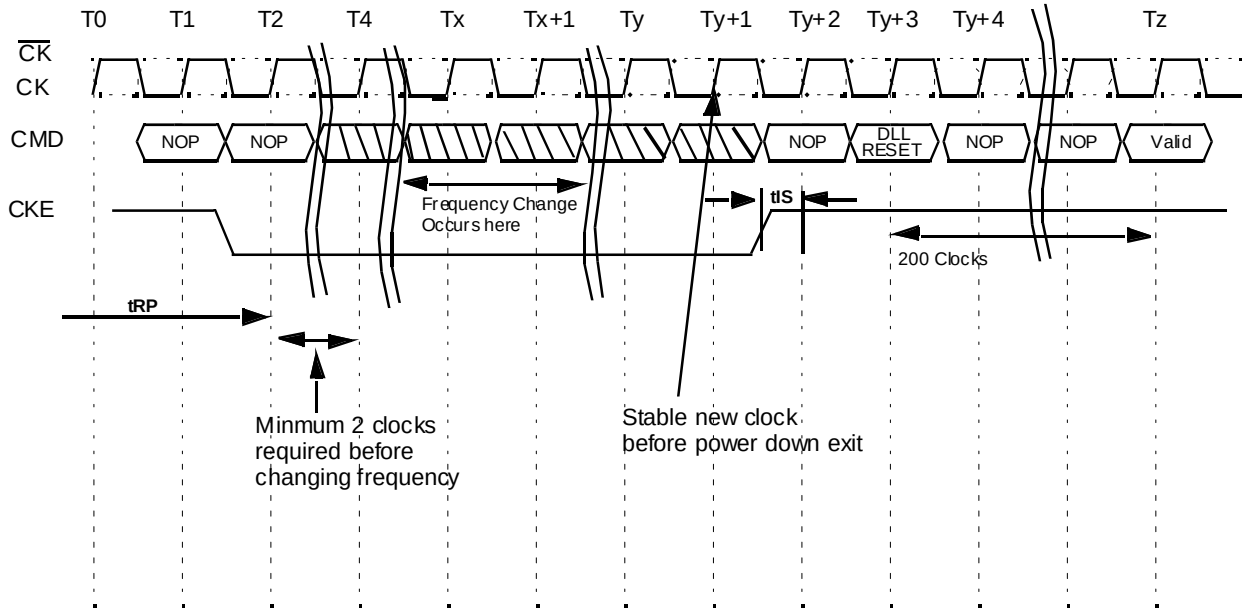


Figure 33
Clock Frequency Change in Precharge
Power Down Mode

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vdd Supply (For devices with nominal Vdd of 3.3 V)
Relative to Vss: -1 V to +4.6 V
Voltage on Vdd Supply (For devices with nominal Vdd of 2.5 V or 2.6 V)
Relative to Vss: -1 V to +3.6 V
Voltage on VddQ Supply Relative to Vss: -1 V to +3.6 V
Voltage on Inputs Relative to Vss: -1 V to +3.6 V
Voltage on I/O Pins Relative to Vss: -0.5 V to VddQ+0.5 V

Operating Temperature, TA (ambient)	0 °C to +70 °C
Storage Temperature (plastic)	-55 °C to +150 °C
Power Dissipation	1 W
Short Circuit Output Current	50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 5: CAPACITANCE

PARAMETER	PACKAGE	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance:CK, $\overline{CK}$	TSOP	Ci1	2.0	3.0	pF	a,d
	BGA		1.5	2.5		a,d
Delta Input Capacitance:CK, $\overline{CK}$	TSOP	Cdi1	-	0.25	pF	a,d
	BGA		-	0.25		a,d
Input Capacitance: All other input-only pins	TSOP	Ci2	2	3	pF	a,d
	BGA		1.5	2.5		a,d
Delta Input Capacitance: All other input-only pins	TSOP	Cdi2	-	0.5	pF	a,d
	BGA		-	0.5		a,d
Input/Output Capacitance: DQ, DQS, DM	TSOP	Cio	4.0	5.0	pF	a,b,c,d
	BGA		3.5	4.5		a,b,c,d
Delta Input/Output Capacitance: DQ, DQS, DM	TSOP	Cdio	-	0.5	pF	a,b,c,d
	BGA		-	0.5		a,b,c,d

a) These values are guaranteed by design and are tested on a sample basis only.
b) Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS, and DM in the system.
c) Unused pins are tied to ground.
d).This parameter is sampled. For DDR 200, 266, and 333, VDDQ = +2.5 V +0.2 V, VDD = +3.3 V +0.3 V or +2.5 V +0.2 V.
For DDR400, VDDQ = +2.6 V ±0.1 V, VDD = +2.6 V ±0.1 V.
For all devices, f = 100 MHz, tA = 25 C, Vout(dc) = VDDQ/2, Vout(peak to peak) = 0.2 V. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
e) The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25 V to 1.0 V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.

TABLE 6: ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1-6, These characteristics are for DDR SDRAM only and obey SSTL_2 class II standard.)
(0°C ≤ TA ≤ 70°C; For DDR 200, 266, and 333, VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V
for DDR400, VDDQ = +2.6 V ±0.1 V, VDD = +2.6 V ±0.1 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
Supply Voltage (for devices with a nominal VDD of 2.6 V)	VDD	2.5	2.7	V	
I/O Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDDQ	2.3	2.7	V	
I/O Supply Voltage (for devices with a nominal VDD of 2.6 V)	VDDQ	2.5	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	7
I/O Termination Voltage (system)	VTT	VREF-0.04	VREF+0.04	V	8
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.15	VDD+0.3	V	
Input Low (Logic 0) Voltage	VIL(DC)	-0.3	VREF-0.15	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	VIN(DC)	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(DC)	0.36	VDDQ+0.6	V	9
V-I Matching: Pullup to Pulldown Current Ratio	VI(Ratio)	0.71	1.4	-	e
INPUT LEAKAGE CURRENT, Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0 V)	IL	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	-5	5	µA	
OUTPUT LEVELS Output High Current (VOUT = 1.95 V) Output Low Current (VOUT = 0.35 V)	IOH IOL	-16.2 16.2		mA mA	

TABLE 7: AC OPERATING CONDITIONS

(Notes: 1–6, These characteristics are for DDR SDRAM only and obey SSTL_2 class II standard.)
(0°C ≤ TA ≤ 70°C; For DDR 200, 266, and 333, VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V; for DDR400, VDDQ = +2.6 V ±0.1 V, VDD = +2.6 V ±0.1 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(ac)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(ac)		VREF - 0.31	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(ac)	0.7	VDDQ + 0.6	V	9
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	VIX(ac)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	10

TABLE 8: Low Power DDR SDRAM Electrical Characteristics

(Note: 1; Recommended Operating Conditions.)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	VDD	1.7	1.9	V	-
I/O Supply Voltage	VDDQ	1.7	1.9	V	-
Address and Command Inputs (A0 - Ai, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)					
Input High Voltage	VIH	0.8 * VDDQ	VDDQ +0.3	V	-
Input Low Voltage	VIL	-0.3	0.2 * VDDQ	V	-
Clock Inputs (CK, CK)					
DC Input Voltage	VIN	-0.3	VDDQ +0.3	V	-
DC Input Differential Voltage	VID(DC)	0.4 * VDDQ	VDDQ +0.6	V	2
AC Input Differential Voltage	VID(AC)	0.6 . VDDQ	VDDQ +0.6	V	2
AC Differential Crosspoint Voltage	VIX	0.4 * VDDQ	0.6 * VDDQ	V	3
Data Inputs (DQ0 - DQ15, UDM, LDM, UDQS, LDQS)					
DC Input High Voltage	VIHD(DC)	0.7 * VDDQ	VDDQ +0.3	V	-
DC Input Low Voltage	VILD(DC)	-0.3	0.3 * VDDQ	V	-
AC Input High Voltage	VIHD(AC)	0.8 * VDDQ	VDDQ +0.3	V	-
AC Input Low Voltage	VILD(AC)	-0.3	0.2 * VDDQ	V	-
Data Outputs (DQ0 - DQ15, UDQS, LDQS)					
DC Output High Voltage (IOH = -0.1mA)	VOH	0.9 * VDDQ	-	V	-
DC Output Low Voltage (IOL = 0.1mA)	VOL	-	0.1 * VDDQ	V	-

Notes:

1. All voltages referenced to VSS. VSS and VSSQ must be the same potential.
2. VID(DC) and VID(AC) are the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
3. The value of VIX is expected to be 0.5 * VDDQ and must track variations in the DC level of the same.

TABLE 9: IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

This table is provided for the users of this Standard so that suppliers use a common format for parameter definitions of their individual IDD specifications. Values will be specific to each supplier.

Conditions	Symbol	Typ	Max
Operating current for one bank active-precharge; $t_{RC} = t_{RC}(min)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333, 5 ns for DDR400; DQ, DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles; $\overline{CS}$ = high between valid commands.	IDD0	-	-
Operating current for one bank operation; one bank open, BL = 4, reads - Refer to the following page for detailed test conditions: $\overline{CS}$ = high between valid commands.	IDD1	-	-
Precharge power-down standby current; all banks idle; power-down mode; CKE $\leq V_{IL}(max)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266A, DDR266B, 6 ns for DDR333, 5 ns for DDR400; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2P	-	-
Precharge floating standby current; $\overline{CS} \geq V_{IH}(min)$; all banks idle; CKE $\geq V_{IH}(min)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333, 5 ns for DDR400; address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2F	-	-
Precharge quiet standby current; $\overline{CS} \geq V_{IH}(min)$; all banks idle; CKE $\geq V_{IH}(min)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333, 5 ns for DDR400; address and other control inputs stable at $\geq V_{IH}(min)$ or $\leq V_{IL}$ (max); $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2Q	-	-
Active power-down standby current ; one bank active; power-down mode; CKE $\leq V_{IL}(max)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333, 5 ns for DDR400; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD3P	-	-
Active standby current; $\overline{CS} \geq V_{IH}(min)$; CKE $\geq V_{IH}(min)$; one bank active; $t_{RC} = t_{RAS}(max)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333, 5 ns for DDR400; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	-	-
Operating current for burst read; burst length = 2; reads; continuous burst; one bank active; address and control inputs changing once per clock cycle; CL = 2 at t_{CK} = 10 ns for DDR200, CL = 2 at t_{CK} = 7.5 ns for DDR266A, CL = 2.5 at t_{CK} = 7.5 ns for DDR266B, 6 ns for DDR333, 5 ns for DDR400; 50% of data changing on every transfer; I_{OUT} = 0 mA	IDD4R	-	-
Operating current for burst write; burst length = 2; writes; continuous burst; one bank active address and control inputs changing once per clock cycle; CL = 2 at t_{CK} = 10 ns for DDR200, CL = 2 at t_{CK} = 7.5 ns for DDR266A, CL = 2.5 at t_{CK} = 7.5 ns for DDR266B, 6 ns for DDR333, 5 ns for DDR400; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every transfer	IDD4W	-	-
Auto refresh current; $t_{RC} = t_{RFC}(min)$ which is 8 * t_{CK} for DDR200 at t_{CK} = 10 ns, 10 * t_{CK} for DDR266 at t_{CK} = 7.5 ns; 12 * t_{CK} for DDR333 at t_{CK} = 6ns; 14 * t_{CK} for DDR400 at t_{CK} = 5ns; IDD5: $t_{RC} = t_{RFC}$ = # of clocks is for 512 Mb devices and smaller. 1Gb devices will require additional clock cycles.	IDD5	-	-
Self refresh current; CKE $\leq$ 0.2 V; external clock on; t_{CK} = 10 ns for DDR200, t_{CK} = 7.5 ns for DDR266, 6 ns for DDR333, 5 ns for DDR400	IDD6	-	-
Operating current for four bank operation; four bank interleaving with BL = 4 - Refer to the following page for detailed test condition	IDD7	-	-
Typical case : For DDR200, 266, and 333: V_{DD} = 2.5 V, T = 25 °C; For DDR400: V_{DD} = 2.6 V, T = 25 °C Worst case : V_{DD} = 2.7 V, T = 10 °C Self refresh: normal/low power respectively Measured values for all items will be averaged from repeated cycles with the above description			

Detailed test conditions for DDR SDRAM IDD1 and IDD7

Typical Case: **For DDR200, 266, and 333:** V_{DD} = 2.5 V, T = 25° C; **For DDR400: V_{DD} = 2.6 V, T = 25 °C**
Worst Case: V_{DD} = 2.7 V, T = 10° C
Legend: A = Active, R = Read, RA = Read with Autoprecharge, P = Precharge, N = DESELECT

IDD1 : Operating current: One bank operation

Only one bank is accessed with $t_{RC}(min)$, Burst Mode, Address and Control inputs change logic state once per Deselect cycle. I_{OUT} = 0 mA

Timing patterns

- DDR200 (100 MHz, CL = 2): t_{CK} = 10 ns, BL = 4, t_{RCD} = 2 * t_{CK}, **t_{RC} = 7 * t_{CK},** t_{RAS} = 5 * t_{CK}
  Setup: A0 N R0 N N P0 N
  Read: A0 N R0 N N P0 N - repeat the same timing with random address changing
  50% of data changing at every transfer

- DDR266B (133 MHz, CL = 2.5): t_{CK} = 7.5 ns, BL = 4, t_{RCD} = 3 * t_{CK}, t_{RC} = 9 * t_{CK}, **t_{RAS} = 6 * t_{CK}**

- DDR266A (133 MHz, CL = 2): t_{CK} = 7.5 ns, BL = 4, t_{RCD} = 3 * t_{CK}, t_{RC} = 9 * t_{CK}, **t_{RAS} = 6 * t_{CK}**
  Setup: A0 N N R0 N N P0 N N
  Read: A0 N N R0 N N P0 N N - repeat the same timing with random address changing 50% of data changing at every transfer
- DDR333B (167 MHz, CL = 2.5): t_{CK} = 6 ns, BL = 4, t_{RCD} = 3 * t_{CK}, t_{RC} = 10 * t_{CK}, t_{RAS} = 7 * t_{CK}
  Setup: A0 N N R0 N N N P0 N N
  Read: A0 N N R0 N N N P0 N N - repeat the same timing with random address changing 50% of data changing at every transfer
- DDR400B (200 MHz, CL = 3): t_{CK} = 5 ns, BL = 4, t_{RCD} = 3 * t_{CK}, t_{RC} = 11 * t_{CK}, t_{RAS} = 8 * t_{CK}
  Setup: A0 N N R0 N N N N P0 N N
  Read: A0 N N R0 N N N N P0 N N - repeat the same timing with random address changing 50% of data changing at every transfer

IDD7 : Operating current: Four bank operation

Four banks are being interleaved with t_{RC}(min), Burst Mode, Address and Control inputs on Deselect edge are not changing. I_{OUT} = 0 mA

Timing patterns

- DDR200 (100 MHz, CL = 2): t_{CK} = 10 ns, BL = 4, t_{RRD} = 2 * t_{CK}, t_{RCD} = 3 * t_{CK}, t_{RAS} = 5 * t_{CK}
  Setup: A0 N A1 RA0 A2 RA1 A3 RA2
  Read: A0 RA3 A1 RA0 A2 RA1 A3 RA2 - repeat the same timing with random address changing 50% of data changing at every transfer
- DDR266B (133 MHz, CL = 2.5): t_{CK} = 7.5 ns, BL = 4, t_{RRD} = 2 * t_{CK}, t_{RCD} = 3 * t_{CK}, t_{RAS} = 6 * t_{CK}
- DDR266A (133 MHz, CL = 2): t_{CK} = 7.5 ns, BL = 4, t_{RRD} = 2 * t_{CK}, t_{RCD} = 3 * t_{CK}, t_{RAS} = 6 * t_{CK}
  Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
  Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 - repeat the same timing with random address changing 50% of data changing at every transfer
- DDR333B (167 MHz, CL = 2.5): t_{CK} = 6 ns, BL = 4, t_{RRD} = 2 * t_{CK}, t_{RCD} = 3 * t_{CK}, t_{RAS} = 7 * t_{CK}
  Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
  Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 - repeat the same timing with random address changing 50% of data changing at every transfer
- DDR400B (200 MHz, CL = 3): t_{CK} = 5 ns, BL = 4, t_{RRD} = 2 * t_{CK}, t_{RCD} = 3 * t_{CK}, t_{RAS} = 8 * t_{CK}
  Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N
  Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N - repeat the same timing with random address changing 50% of data changing at every transfer

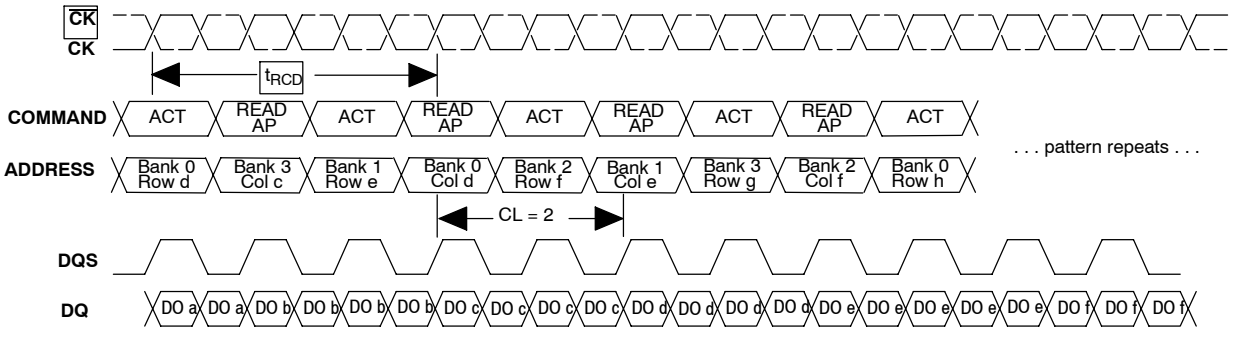


FIGURE 34: Timing waveform for IDD7 measurement at 100 MHz Ck operation

TABLE 10: Low Power DDR SDRAM IDD Specification Parameters and Test Conditions

(IDD values are for full operating range of voltage and temperature; Notes 1 to 3)

Parameter/Condition	Symbol
Operating one bank active-precharge current: $t_{RC} = t_{RCmin}$; $t_{CK} = t_{CKmin}$; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	I_{DD0}
Precharge power-down standby current: all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2P}
Precharge power-down standby current with clock stop: all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2PS}
Precharge non power-down standby current: all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2N}
Precharge non power-down standby current with clock stop: all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2NS}
Active power-down standby current: one bank active, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3P}
Active power-down standby current with clock stop: one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3PS}
Active non power-down standby current: one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3N}
Active non power-down standby current with clock stop: one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3NS}
Operating burst read current: one bank active; BL = 4; CL = 3; $t_{CK} = t_{CKmin}$; continuous read bursts; I_{OUT} = 0 mA address inputs are SWITCHING; 50% data change each burst transfer	I_{DD4R}
Operating burst write current: one bank active; BL = 4; $t_{CK} = t_{CKmin}$; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	I_{DD4W}
Auto-Refresh current: $t_{RC} = t_{RFCmin}$; $t_{CK} = t_{CKmin}$; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD5}
Self refresh current CKE is LOW; $t_{CK} = t_{CKmin}$; Extended Mode Register set to all 0s; address and control inputs are STABLE; data bus inputs are STABLE	I_{DD6}
Self refresh current CKE is LOW; $t_{CK} = t_{CKmin}$; Extended Mode Register set to all 0s; address and control inputs are STABLE; data bus inputs are STABLE	I_{DD6}
Deep Power Down current	I_{DD8}

Notes:

1. IDD specifications are tested after the device is properly intialized.
2. Input slew rate is 1V/ns.
3. Definitions for IDD:

   LOW is defined as $V_{IN} <= 0.1 * V_{DDQ}$;

   HIGH is defined as $V_{IN} => 0.9 * V_{DDQ}$;

   STABLE is defined as inputs stable at a HIGH or LOW level;

   SWITCHING is defined as:

   - address and command: inputs changing between HIGH and LOW once per two clock cycles;
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

TABLE 11: ELECTRICAL CHARACTERISTICS AND AC TIMING
Part A: DDR333, DDR266, DDR200 Devices

All specification parameters are guaranteed by the supplier, but it is not implied that this table represents a test specification.

Absolute Specifications

(Notes: 1-6, 13,1 4, 32) (0°C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

AC CHARACTERISTICS		DDR333		DDR266		DDR200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQ output access time from CK/$\overline{CK}$	tAC	-0.70	+0.70	-0.75	+0.75	-0.8	+0.8	ns	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-0.60	+0.60	-0.75	+0.75	-0.8	+0.8	ns	
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ns	24, 25
Clock cycle time CL = 2.5	tCK	6	12	7.5	12	10	12	ns	30
CL = 2	tCK	7.5	12	7.5	12	10	12	ns	30
DQ and DM input hold time	tDH	0.45		0.5		0.6		ns	j, k, 31
DQ and DM input setup time	tDS	0.45		0.5		0.6		ns	j, k, 31
Control & Address input pulse width (for each input)	tIPW	2.2		2.2		2.5		ns	22
DQ and DM input pulse width (for each input)	tDIPW	1.75		1.75		2		ns	22
DQ & DQS high-impedance time from CK/$\overline{CK}$	tHZ		+0.70		+0.75		+0.8	ns	15
DQ & DQS low-impedance time from CK/$\overline{CK}$	tLZ	-0.70	+0.70	-0.75	+0.75	-0.8	+0.8	ns	15
DQS-DQ Skew (for DQS and associated DQ signals) TSOP Package	tDQSQ		+0.45		+0.5		+0.6	ns	26
BGA Package	tDQSQ		+0.4		+0.5		+0.6	ns	26
DQ/DQS output hold time from DQS	tQH	tHP-tQHS		tHP-tQHS		tHP-tQHS		ns.	25
Data Hold Skew Factor (for DQS and associated DQ Signals) TSOP Package	tQHS		+0.55		+0.75		+1.0	ns	25
BGA Package	tQHS		+0.5		+0.75		+1.0	ns	25
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high pulse width	tDQSH	0.35		0.35		0.35		tCK	
DQS input low pulse width	tDQSL	0.35		0.35		0.35		tCK	
DQS falling edge to CK setup time	tDSS	0.2		0.2		0.2		tCK	
DQS falling edge hold time from CK	tDSH	0.2		0.2		0.2		tCK	
MODE REGISTER SET command cycle time	tMRD	2		2		2		tCK	
Write preamble setup time	tWPRES	0		0		0		ns	17
Write postamble	tWPST	0.40	0.60	0.4	0.6	0.40	0.60	tCK	16
Write preamble	tWPRE	0.25		0.25		0.25		tCK	
Address and Control input hold time (fast slew rate)	tIH	0.75		0.9		1.1		ns	i, 19, 21-23
Address and Control input setup time (fast slew rate)	tIS	0.75		0.9		1.1		ns	i, 19, 21-23
Address and Control input hold time (slow slew rate)	tIH	0.80		1.0		1.1		ns	i, 20-23
Address and Control input setup time (slow slew rate)	tIS	0.80		1.0		1.1		ns	i, 20-23
Read preamble CL=2.5	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	28, 33
CL = 2.0		0.9	1.1	0.9	1.1	0;9	1.1	tCK	28, 33
CL = 1.5		N/A	N/A	N/A	N/A	-	1.1	tCK	28, 33
Read preamble setup time (Optional CL=1.5)	tRPRES		N/A		N/A		1.5	ns	28
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	33
ACTIVE to PRECHARGE command	tRAS	42	70,000	45	120,000	50	120,000	ns	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	60		65		70		ns	
Auto Refresh to Active/Auto Refresh command period 64Mb, 512Mb	tRFC	72		75		80		ns	
1Gb		120		120		120		ns	
ACTIVE to READ or WRITE delay	tRCD	18		20		20		ns	
PRECHARGE command period	tRP	18		20		20		ns	
Active to Autoprecharge Delay	tRAP	tRCD or tRASmin		tRCD or tRASmin		tRCD or tRASmin		ns	
ACTIVE bank A to ACTIVE bank B command	tRRD	12		15		15		ns	
Write recovery time	tWR	15		15		15		ns	
Auto Precharge write recovery + precharge time	tDAL	--		--		--		tCK	27
Internal Write to Read Command Delay CL=2.5	tWTR	1		1		1		tCK	
CL=2.0		1		1		1		tCK	
CL=1.5		N/A		N/A		2		tCK	
Exit self refresh to non-READ command 64Mb to 512 Mb	tXSNR	75		75		80		ns	29
1Gb		126		127.5		130			
Exit self refresh to READ command	tXSRD	200		200		200		tCK	
Average Periodic Refresh Interval 64Mb, 128Mb	tREFI		15.6		15.6		15.6	µs	18, 31
256Mb to 1Gb			7.8		7.8		7.8	µs	18, 31

Part B: DDR400A, DDR400B, DDR400C Devices

All specification parameters are guaranteed by the supplier, but it is not implied that this table represents a test specification.

Absolute Specifications (Notes: 1-6, 13, 14, 32) (0°C ≤ TA ≤ 70 °C; VDDQ = +2.6 V ±0.1 V, VDD = +2.6 V ±0.1 V)

AC CHARACTERISTICS		DDR400A (2.5-3-3)		DDR400B (3-3-3)		DDR400C (3-4-4)			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQ output access time from CK/$\overline{CK}$	tAC	-0.7	+0.7	-0.7	+0.7	-0.7	+0.7	ns	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-0.6	+0.6	-0.6	+0.6	-0.6	+0.6	ns	
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ns	24, 25
Clock cycle time CL = 3	tCK	5	7.5	5	7.5	5	7.5	ns	30
CL = 2.5	tCK	5	12	6	12	6	12	ns	30
CL = 2	tCK	7.5	12	7.5	12	7.5	12	ns	30
DQ and DM input hold time	tDH	0.4		0.4		0.4		ns	31
DQ and DM input setup time	tDS	0.4		0.4		0.4		ns	31
Control & Address input pulse width (for each input)	tIPW	2.2		2.2		2.2		ns	22
DQ and DM input pulse width (for each input)	tDIPW	1.75		1.75		1.75		ns	22
DQ & DQS high-impedance time from CK/$\overline{CK}$	tHZ		+0.7		+0.7		+0.7	ns	15
DQ & DQS low-impedance time from CK/$\overline{CK}$	tLZ	-0.7	+0.7	-0.7	+0.7	-0.7	+0.7	ns	15
DQS-DQ Skew (for DQS and associated DQ signals) TSOP Package	tDQSQ		+0.4		+0.4		+0.4	ns	26
BGA Package	tDQSQ		+0.4		+0.4		+0.4	ns	26
DQ/DQS output hold time from DQS	tQH	tHP-tQHS		tHP-tQHS		tHP-tQHS		ns.	25
Data Hold Skew Factor (for DQS and associated DQ Signals) TSOP Package	tQHS		+0.5		+0.5		+0.5	ns	25
BGA Package	tQHS		+0.5		+0.5		+0.5	ns	25
Write command to first DQS latching transition	tDQSS	0.72	1.25	0.72	1.25	0.72	1.25	tCK	
DQS input high pulse width	tDQSH	0.35		0.35		0.35		tCK	
DQS input low pulse width	tDQSL	0.35		0.35		0.35		tCK	
DQS falling edge to CK setup time	tDSS	0.2		0.2		0.2		tCK	
DQS falling edge hold time from CK	tDSH	0.2		0.2		0.2		tCK	
MODE REGISTER SET command cycle time	tMRD	2		2		2		tCK	
Write preamble setup time	tWPRES	0		0		0		ns	17
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	16
Write preamble	tWPRE	max(0.25* tCK, 1.5 ns)		max(0.25 *tCK, 1.5 ns)		max(0.25 *tCK, 1.5 ns)		ns	
Address and Control input hold time (fast slew rate)	tIH	0.6		0.6		0.6		ns	19, 21-23
Address and Control input setup time (fast slew rate)	tIS	0.6		0.6		0.6		ns	19, 21-23
Address and Control input hold time (slow slew rate)	tIH	0.7		0.7		0.7		ns	20-23
Address and Control input setup time (slow slew rate)	tIS	0.7		0.7		0.7		ns	20-23
Read preamble CL=3	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	28, 33
CL = 2.5		0.9	1.1	0.9	1.1	0.9	1.1	tCK	28, 33
CL = 2.0		0.9	1.1	0.9	1.1	0;9	1.1	tCK	28, 33
CL = 1.5		N/A	N/A	N/A	N/A	N/A	N/A		
Read preamble setup time (Optional CL=1.5)	tRPRES		N/A		N/A		N/A	ns	28
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	33
ACTIVE to PRECHARGE command	tRAS	40	70,000	40	70,000	40	70,000	ns	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	55		55		60		ns	
Auto Refresh to Active/Auto Refresh command period 64Mb, 512Mb	tRFC	70		70		70		ns	
1Gb		120		120		120		ns	
ACTIVE to READ or WRITE delay	tRCD	15		15		18		ns	
PRECHARGE command period	tRP	15		15		18		ns	
Active to Autoprecharge Delay	tRAP	tRCD or tRASmin		tRCD or tRASmin		tRCD or tRASmin		ns	
ACTIVE bank A to ACTIVE bank B command	tRRD	10		10		10		ns	
Write recovery time	tWR	15		15		15		ns	
Auto Precharge write recovery + precharge time	tDAL	--		--		--		tCK	27
Internal Write to Read Command Delay . . . . . CL=3	tWTR	2		2		2		tCK	
CL=2.5		2		2		2		tCK	
CL=2.0		2		2		2		tCK	
CL=1.5		N/A		N/A		N/A			
Exit self refresh to non-READ command 64Mb to 512 Mb	tXSNR	75		75		75		ns	29
1Gb		126		126		126			
Exit self refresh to READ command	tXSRD	200		200		200		tCK	
Average Periodic Refresh Interval 64Mb, 128Mb	tREFI		15.6		15.6		15.6	µs	18, 31
256Mb to 1Gb			7.8		7.8		7.8	µs	18, 31

TABLE 12: AC TIMING VARIATIONS FOR DDR333, DDR266, & DDR200 Devices

This table defines several parameters that differ from those given in Table 11 to establish A & B variants of the primary speed sort specifications for DDR200, DDR266, & DDR333.

	DDR333B		DDR266A		DDR266B		DDR200		DDR200B		Units
Parameter	min	max	min	max	min	max	min	max	min	max	ns
tAC	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	-0.8	0.8	ns
tDQSCK	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	-0.8	0.8	ns
tCK CL = 2.5	6	12	7.5	12	7.5	12	10	12	10	12	ns
tCK CL = 2.0	7.5	12	7.5	12	10	12	10	12	10	12	ns
tRRD	12		15		15		15		20		ns
tWR	15		15		15		15		20		ns

Component Notes

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Figure 34 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

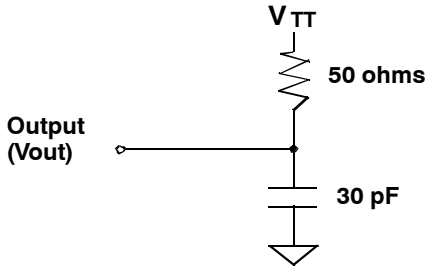


Figure 35: Timing Reference Load

4. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/$\overline{CK}$), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE ≤ 0.2VDDQ is recognized as LOW.
7. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak-to-peak noise on VREF may not exceed +/-2% of the dc value.
8. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF.
9. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
10. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
11. Enables on-chip refresh and address counters.
12. IDD specifications are tested after the device is properly initialized.
13. The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$, is VREF.
14. The output timing reference voltage level is VTT.
15. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving (tHZ), or begins driving (tLZ). Figure 36 shows a method to calculate the point when the device is no longer driving (tHZ) or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
16. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

17. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
18. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
19. For command/address input slew rate $\geq$1.0 V/ns
20. For command/address input slew rate $\geq$0.5 V/ns and $<$1.0 V/ns
21. For CK & $\overline{CK}$ slew rate $\geq$1.0 V/ns (single-ended)
22. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
23. Slew Rate is measured between VOH(ac) and VOL(ac).
24. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
25. tQH = tHP - tQHS, where:
    tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
26. tDQSQ
    Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
27. tDAL = (tWR/tCK) + (tRP/tCK)
    For each of the terms above, if not already an integer, round to the next highest integer.
    Example: For DDR266B at CL=2.5 and tCK=7.5 ns
    tDAL = ((15 ns / 7.5 ns) + (20 ns / 7.5 ns)) clocks
    = ((2) + (3)) clocks
    = 5 clocks
28 Optional CAS Latency, 1.5, is only defined for DDR200 speed grade
29 In all circumstances, tXSNR can be satisfied using tXSNR = tRFCmin + 1*tCK
30 The only time that the clock frequency is allowed to change is during self-refresh mode.
31 If refresh timing or tDS/tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
32 Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
33 tRPST end ;point adn tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Figure 36 shows a method to calculate the point when the device is no longer driving (tRPST) or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

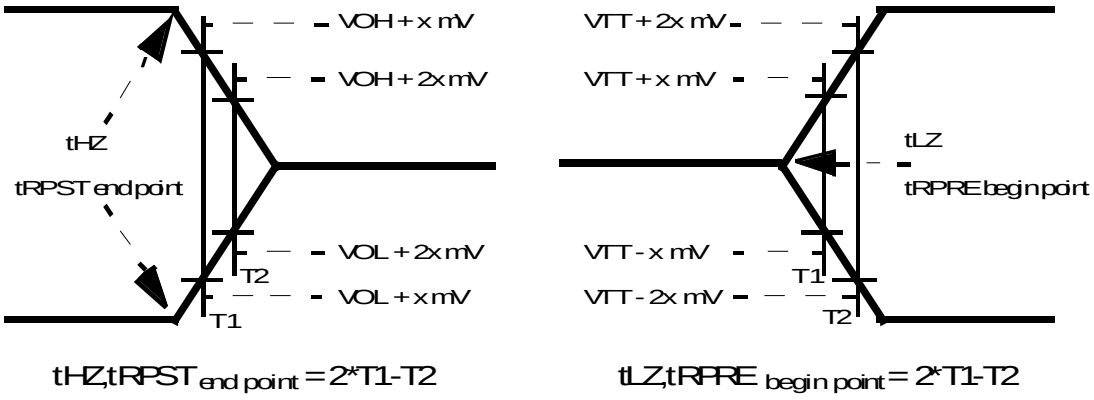


Figure 36: Method for Calculating Transitions and Endpoints

SYSTEM CHARACTERISTICS for DDR SDRAMS

The following specification parameters are required in systems using DDR333, DDR266 & DDR200 devices to ensure proper system performance. These characteristics are for system simulation purposes and are guaranteed by design.

Table 13: Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR400		DDR333		DDR266		DDR200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	V/ns	a, m

Table 14: Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	ΔtIS	ΔtIH	UNITS	NOTES
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Table 15: Input/Output Setup & Hold Time Derating for Slew Rate

I/O Input Slew Rate	ΔtDS	ΔtDH	UNITS	NOTES
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Table 16: Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	ΔtDS	ΔtDH	UNITS	NOTES
±0.0 ns/V	0	0	ps	j
±0.25 ns/V	+50	+50	ps	j
±0.5 ns/V	+100	+100	ps	j

Table 17: Output Slew Rate Characteristics (X4, X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 - 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown Slew Rate	1.2 - 2.5	1.0	4.5	b,c,d,f,g,h

Table 18: Output Slew Rate Characteristics (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 - 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown Slew Rate	1.2 - 2.5	0.7	5.0	b,c,d,f,g,h

Table 19: Output Slew Rate Matching Ratio Characteristics

Slew Rate Characteristic	DDR266A		DDR266B		DDR200		
PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	NOTES
Output Slew Rate Matching Ratio (Pullup to Pulldown)	-	-	-	-	0.71	1.4	e,m

Table 20: AC Overshoot/Undershoot Specification for Address and Control Pins
This specification is intended for devices with no clamp protection and is guaranteed by design

Parameter	Specification	
	DDR333	DDR200/266
Maximum peak amplitude allowed for overshoot (See Figure 37):	TBD	1.5 V
Maximum peak amplitude allowed for undershoot (See Figure 37):	TBD	1.5 V
The area between the overshoot signal and VDD must be less than or equal to (See Figure 37):	TBD	4.5 V-ns
The area between the undershoot signal and GND must be less than or equal to (See Figure 37):	TBD	4.5 V-ns

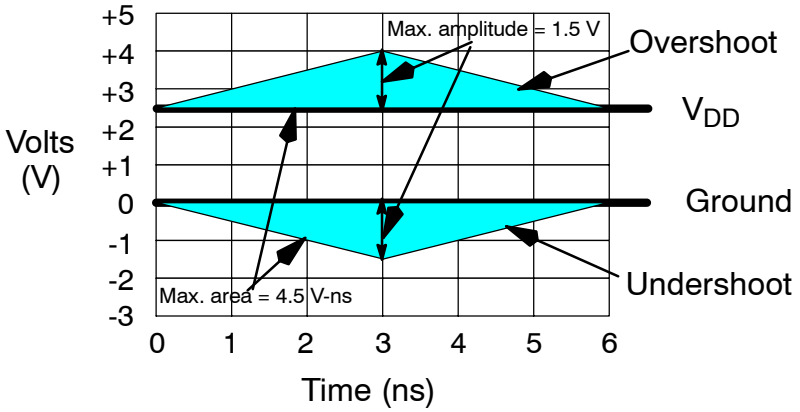


Figure 37: Address and Control AC Overshoot and Undershoot Definition

TABLE 21: Overshoot/Undershoot Specification for Data, Strobe, and Mask Pins

Parameter	Specification	
	DDR333	DDR200/266
Maximum peak amplitude allowed for overshoot (See Figure 38):	TBD	1.2 V
Maximum peak amplitude allowed for undershoot (See Figure 38):	TBD	1.2 V
The area between the overshoot signal and VDD must be less than or equal to (See Figure 38):	TBD	2.4 V-ns
The area between the undershoot signal and GND must be less than or equal to (See Figure 38):	TBD	2.4 V-ns

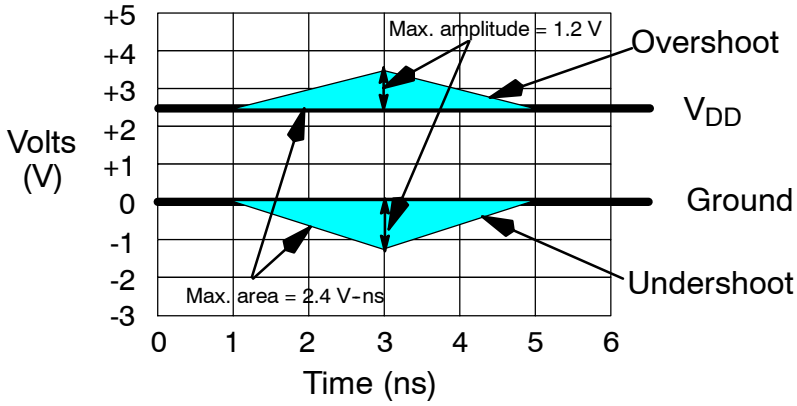


Figure 38: DQ/DM/DQS AC Overshoot and Undershoot Definition

TABLE 22. Clamp V-I Characteristics for Address, Control and Data Pins

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0.1
0.8	0.1	0.6
0.9	1.0	1.8
1.0	2.5	3.4
1.1	4.7	5.6
1.2	6.8	7.6
1.3	9.1	10.0
1.4	11.0	13.0
1.5	13.5	15.4
1.6	16.0	18.0
1.7	18.2	21.6
1.8	21.0	25.0
1.9	23.3	28.0
2.0	26.0	31.0
2.1	28.2	34.4
2.2	31.0	38.0
2.3	33.0	42.0
2.4	35.0	46.0
2.5	37.0	50.0

Power & Ground Clamp V-I Characteristics

System Notes:

a. Pullup slew rate is characterized under the test conditions as shown in Figure 39.

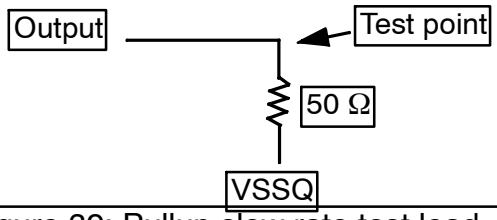


Figure 39: Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 40.

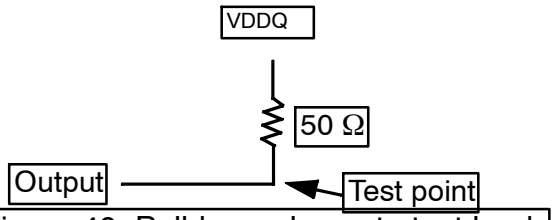


Figure 40: Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 – 320 mV ± 250 mV)
Pulldown slew rate is measured between (VDDQ/2 + 320 mV ± 250 mV)
Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example: For typical slew rate, DQ0 is switching
For minimum slew rate, all DQ bits are switching worst case pattern
For maximum slew rate, only one DQ is switching from either high to low, or low to high.
The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions
Typical: 25 °C (T Ambient), VDDQ = nominal, typical process
Minimum: 70 °C (T Ambient), VDDQ = minimum, slow–slow process
Maximum: 0 °C (T Ambient), VDDQ = maximum, fast–fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOPII package devices only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns as shown in Table 14. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions. A derating factor applies to speed bins DDR200, DDR266, and DDR333.

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 15 & 16. Input slew rate is based on the larger of AC–AC delta rise, fall rate and DC–DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
The delta rise/fall rate is calculated as:
{1/(Slew Rate1)}–{1/(slew Rate2)}
For example: If Slew Rate 1 is 0.5 V/ns and Slew Rate 2 is 0.4 V/ns, then the delta rise,fall rate is –0.5 ns/V. Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps. A derating factor applies to speed bins DDR200, DDR266, and DDR333.

k. Table 15 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC–AC slew rate and the DC–DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(AC) or VIH(DC) to VIL(DC), and similarly for rising transitions. A derating factor applies to speed bins DDR200, DDR266, and DDR333.

m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

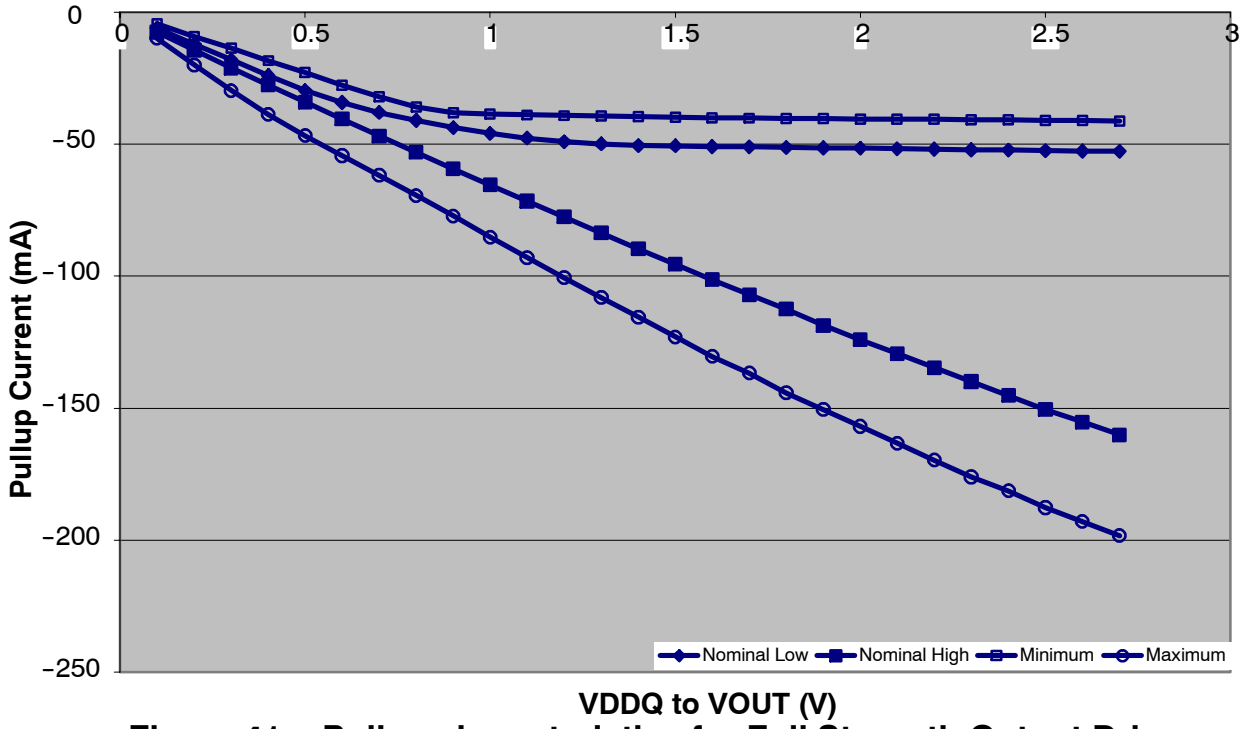


Figure 41a: Pullup characteristics for Full Strength Output Driver

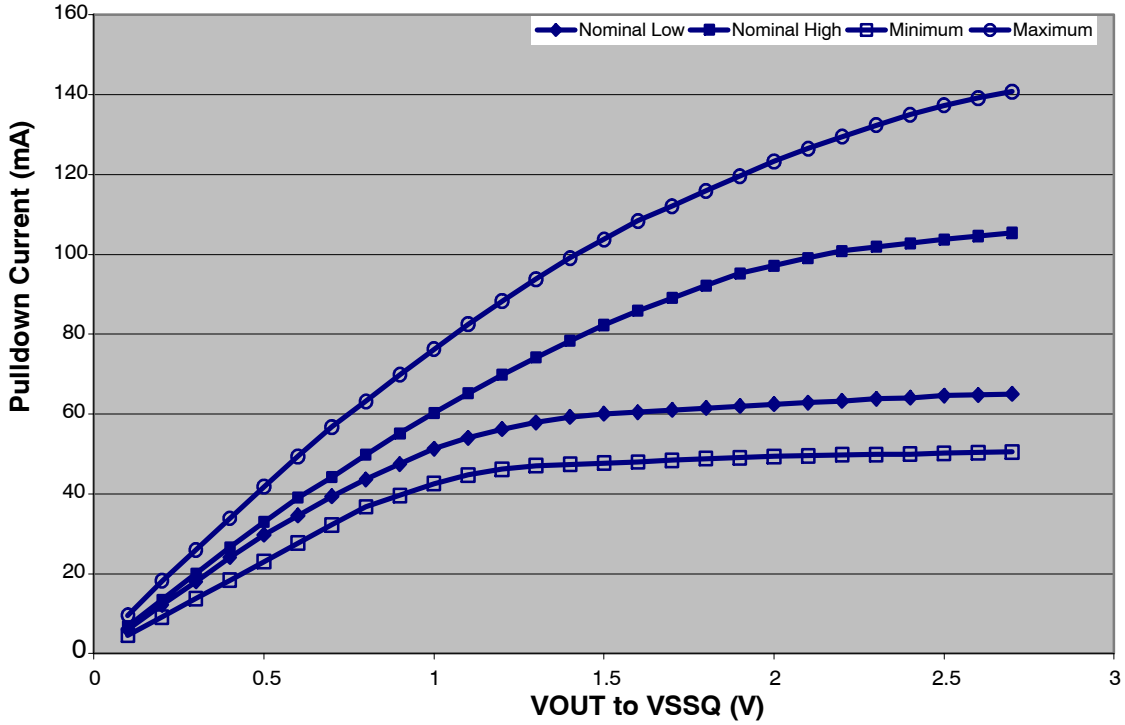


Figure 41b: Pulldown characteristics for Full Strength Output Driver

FIGURE 41: FULL STRENGTH OUTPUT DRIVER CHARACTERISTIC CURVES

TABLE 23: Full Strength Driver Characteristics

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Minimum	Maximum	Nominal Low	Nominal High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	160.1	-41.2	-198.2

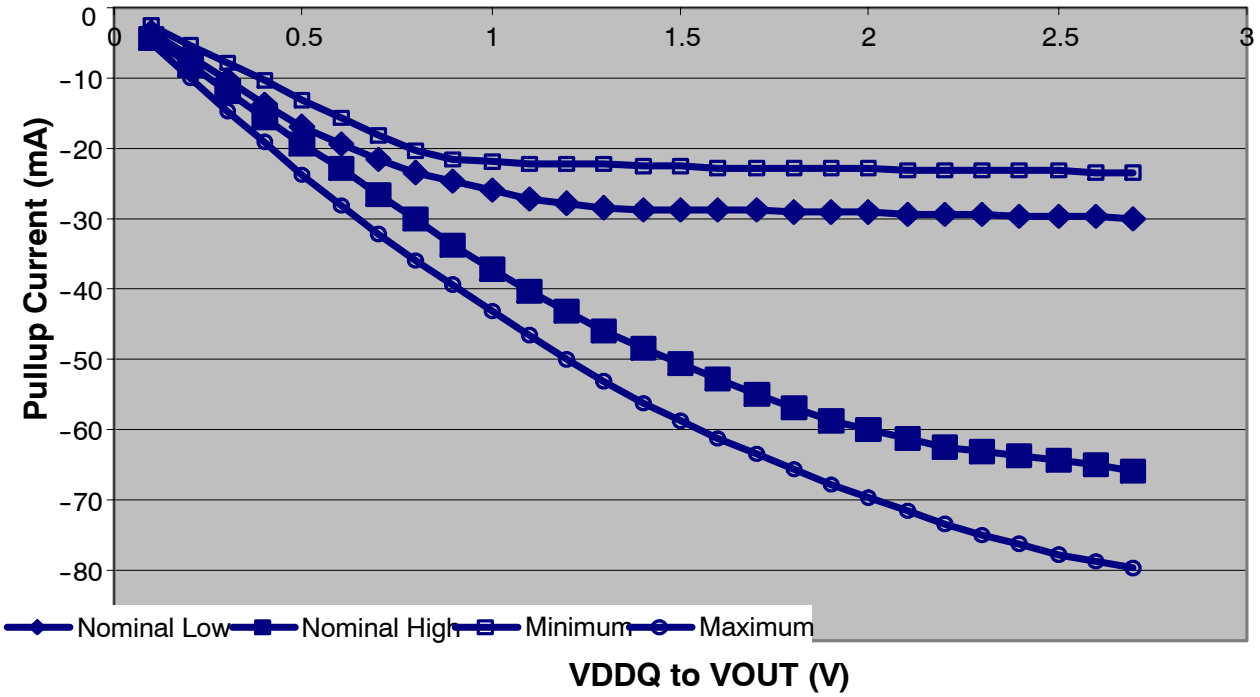


Figure 42a: Pullup Characteristics for Weak Output Driver

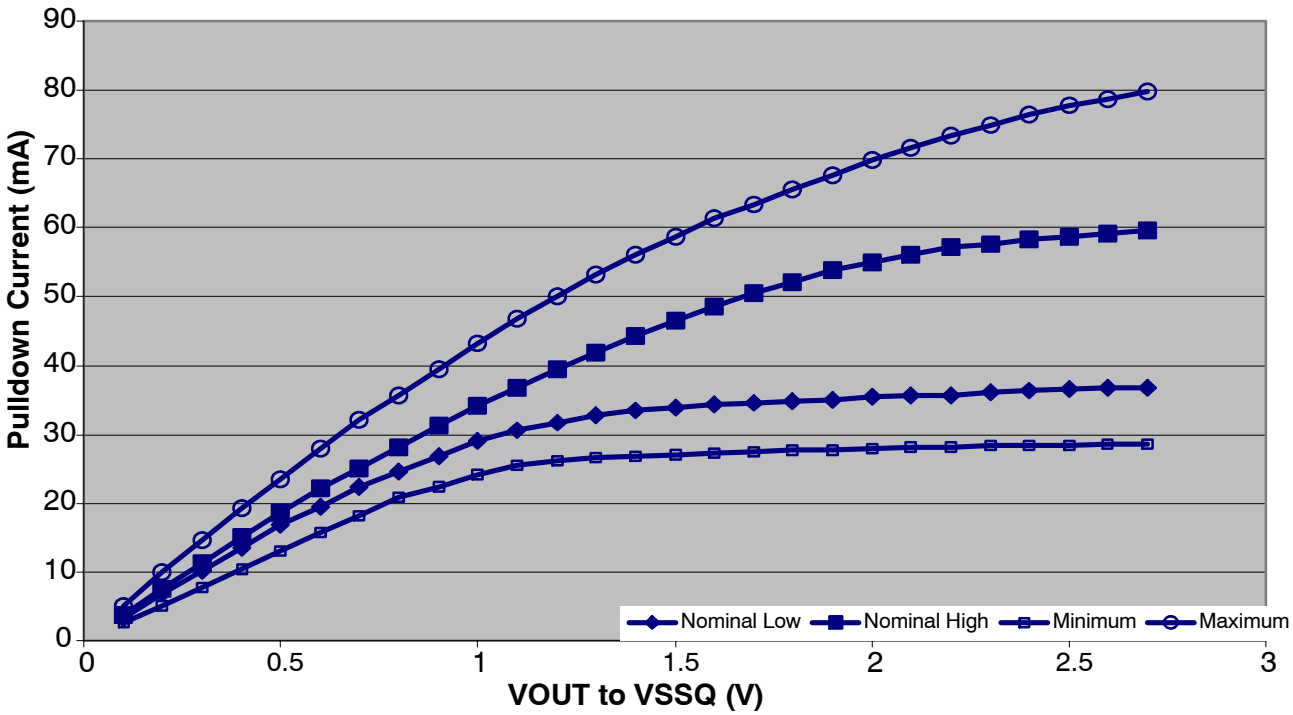


Figure 42b: Pulldown Characteristics for Weak Output Driver

FIGURE 42: WEAK OUTPUT DRIVER CHARACTERISTIC CURVES

TABLE 24: Weak Driver Characteristics

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	3.4	3.8	2.6	5	-3.5	-4.3	-2.6	-5
0.2	6.9	7.6	5.2	9.9	-6.9	-8.2	-5.2	-9.9
0.3	10.3	11.4	7.8	14.6	-10.3	-12	-7.8	-14.6
0.4	13.6	15.1	10.4	19.2	-13.6	-15.7	-10.4	-19.2
0.5	16.9	18.7	13	23.6	-16.9	-19.3	-13	-23.6
0.6	19.6	22.1	15.7	28	-19.4	-22.9	-15.7	-28
0.7	22.3	25	18.2	32.2	-21.5	-26.5	-18.2	-32.2
0.8	24.7	28.2	20.8	35.8	-23.3	-30.1	-20.4	-35.8
0.9	26.9	31.3	22.4	39.5	-24.8	-33.6	-21.6	-39.5
1	29	34.1	24.1	43.2	-26	-37.1	-21.9	-43.2
1.1	30.6	36.9	25.4	46.7	-27.1	-40.3	-22.1	-46.7
1.2	31.8	39.5	26.2	50	-27.8	-43.1	-22.2	-50.0
1.3	32.8	42	26.6	53.1	-28.3	-45.8	-22.3	-53.1
1.4	33.5	44.4	26.8	56.1	-28.6	-48.4	-22.4	-56.1
1.5	34	46.6	27	58.7	-28.7	-50.7	-22.6	-58.7
1.6	34.3	48.6	27.2	61.4	-28.9	-52.9	-22.7	-61.4
1.7	34.5	50.5	27.4	63.5	-28.9	-55	-22.7	-63.5
1.8	34.8	52.2	27.7	65.6	-29	-56.8	-22.8	-65.6
1.9	35.1	53.9	27.8	67.7	-29.2	-58.7	-22.9	-67.7
2	35.4	55	28	69.8	-29.2	-60	-22.9	-69.8
2.1	35.6	56.1	28.1	71.6	-29.3	-61.2	-23	-71.6
2.2	35.8	57.1	28.2	73.3	-29.5	-62.4	-23	-73.3
2.3	36.1	57.7	28.3	74.9	-29.5	-63.1	-23.1	-74.9
2.4	36.3	58.2	28.3	76.4	-29.6	-63.8	-23.2	-76.4
2.5	36.5	58.7	28.4	77.7	-29.7	-64.4	-23.2	-77.7
2.6	36.7	59.2	28.5	78.8	-29.8	-65.1	-23.3	-78.8
2.7	36.8	59.6	28.6	79.7	-29.9	-65.8	-23.3	-79.7

DDR SDRAM Output Driver V-I Characteristics

DDR SDRAM output driver characteristics are defined for full and half strength operation as selected by the EMRS bit A1. Figures 39 and 40 show the driver characteristics graphically, and tables 21 and 22 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

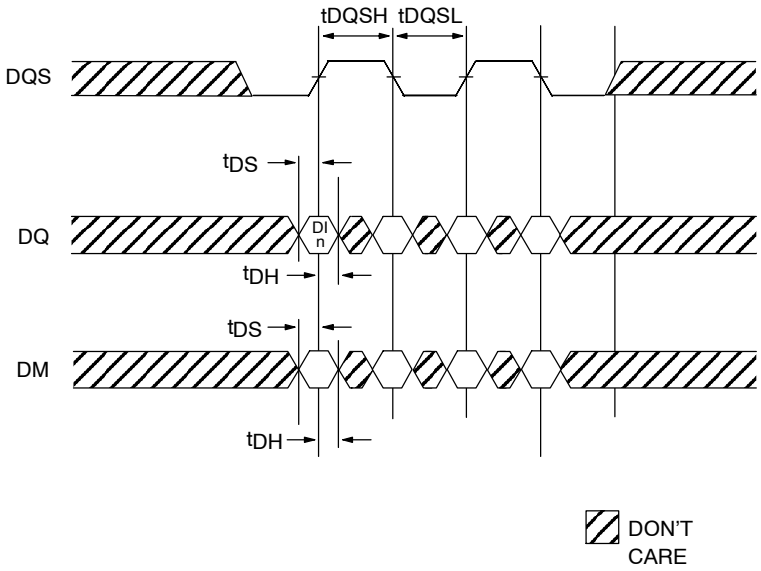
Typical	25 ^{o}C (T ambient),	VDDQ = nominal, typical process
Minimum	70 ^{o}C (T ambient),	VDDQ = minimum, slow-slow process
Maximum	0 ^{o}C (T ambient),	VDDQ = maximum, fast-fast process

Output Driver Characteristic Curves Notes:

1) The full variation in driver current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V-I curve of Figures 41 and 42.

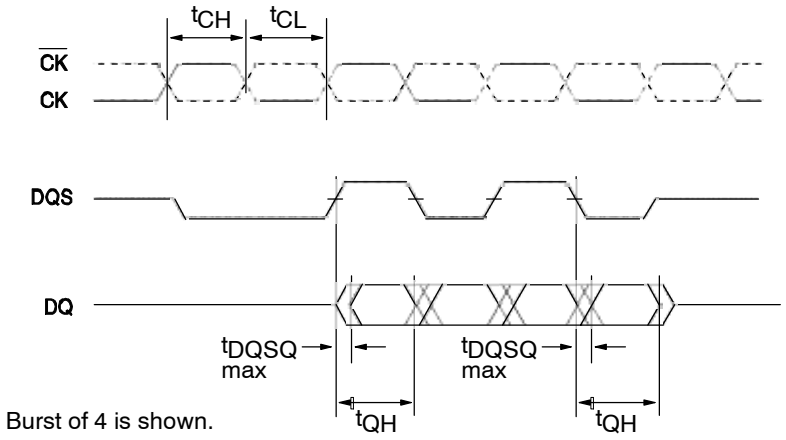
2) It is recommended that the "typical" IBIS V-I curve lie within the inner bounding lines of the V-I curves of Figures 41 and 42.

3) The full variation in the ratio of the "typical" IBIS pullup to "typical" IBIS pulldown current should be unity $\pm$ 10%, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.



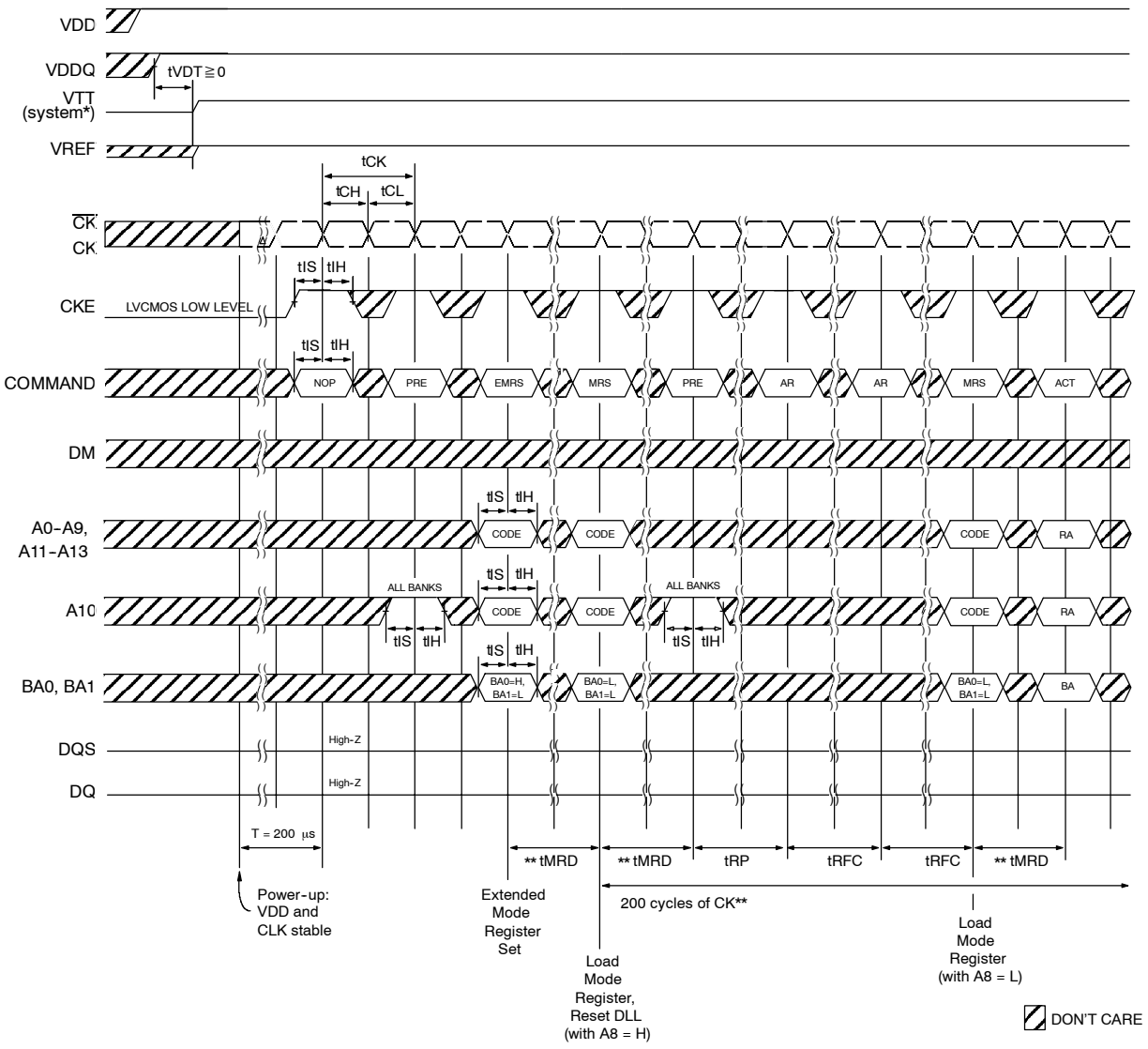
DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n

Figure 43 – DATA INPUT (WRITE) TIMING



Burst of 4 is shown.

Figure 44 – DATA OUTPUT (READ) TIMING

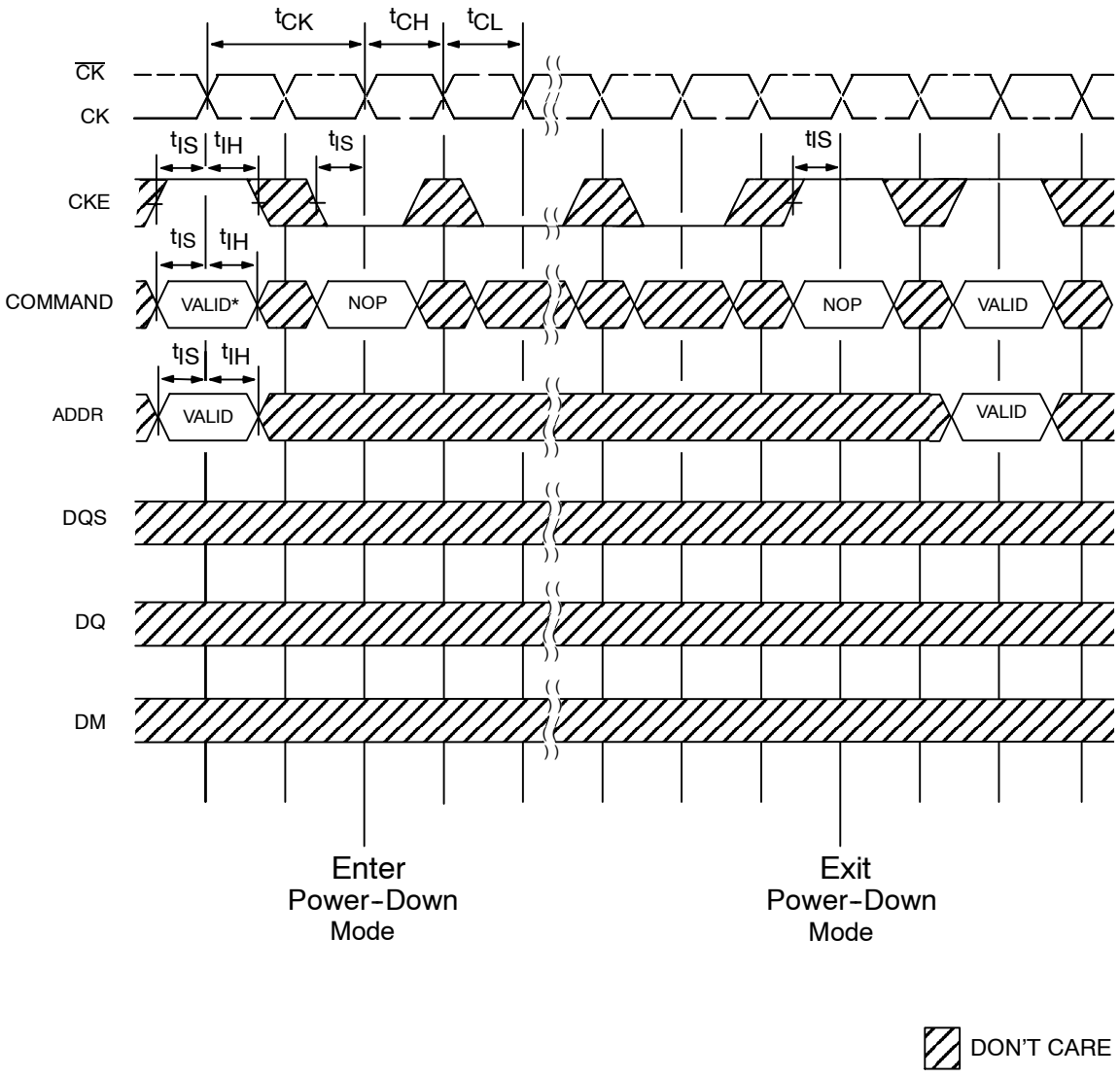


* = VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch-up.

** = tMRD is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied

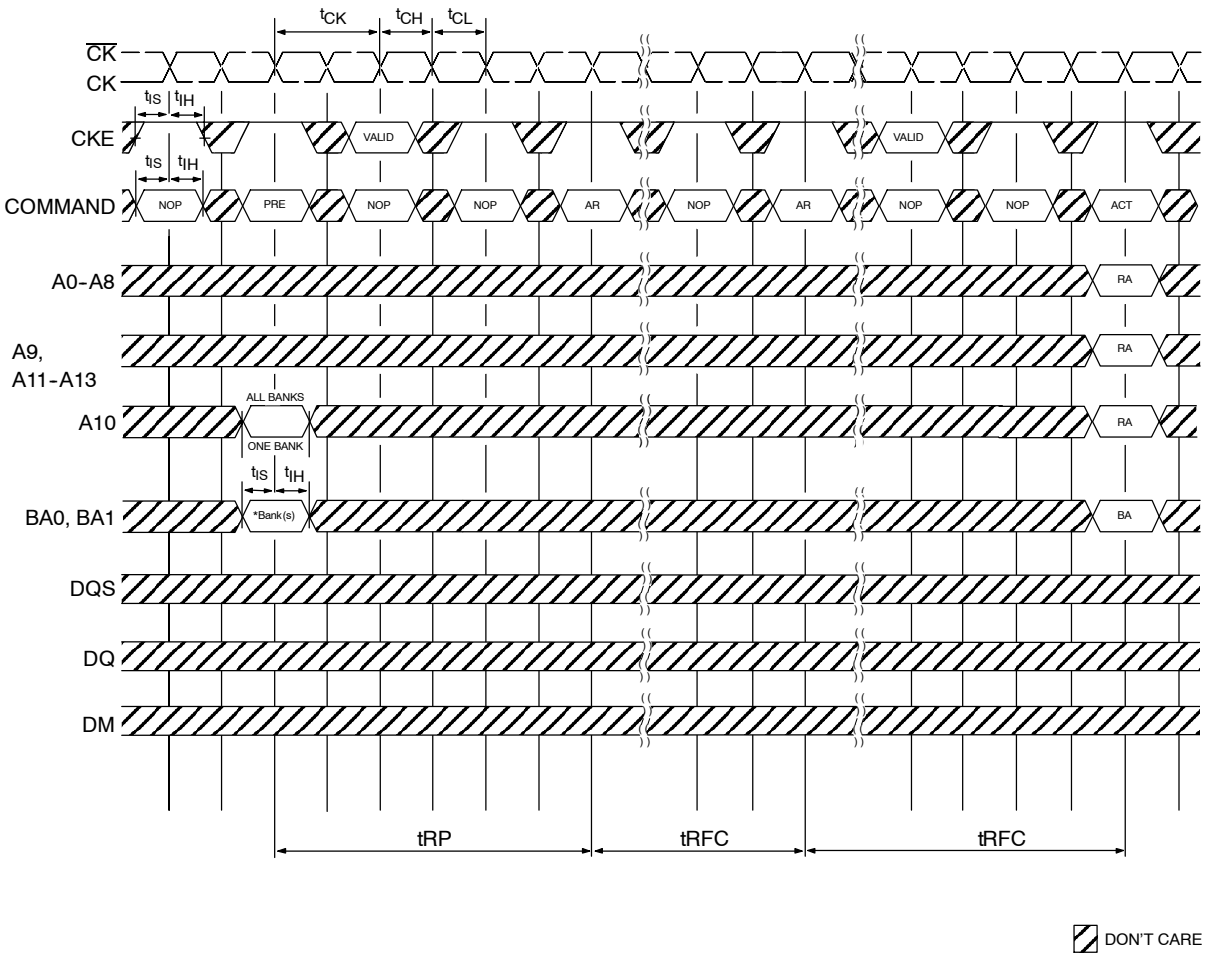
The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

Figure 45 – INITIALIZE AND MODE REGISTER SETS



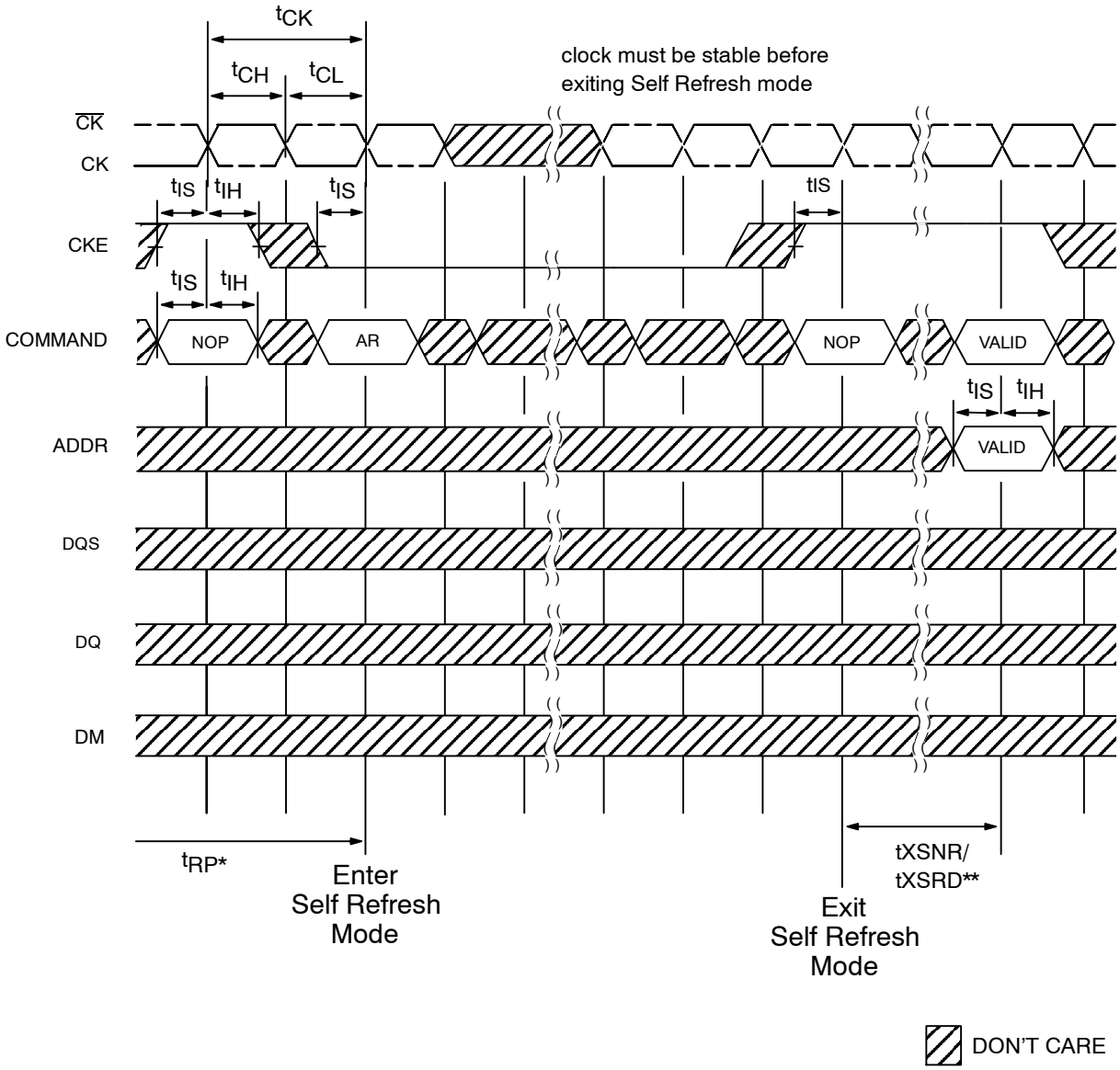
No column accesses are allowed to be in progress at the time Power-Down is entered
* = If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is Active Power Down.

Figure 46 - POWER-DOWN MODE



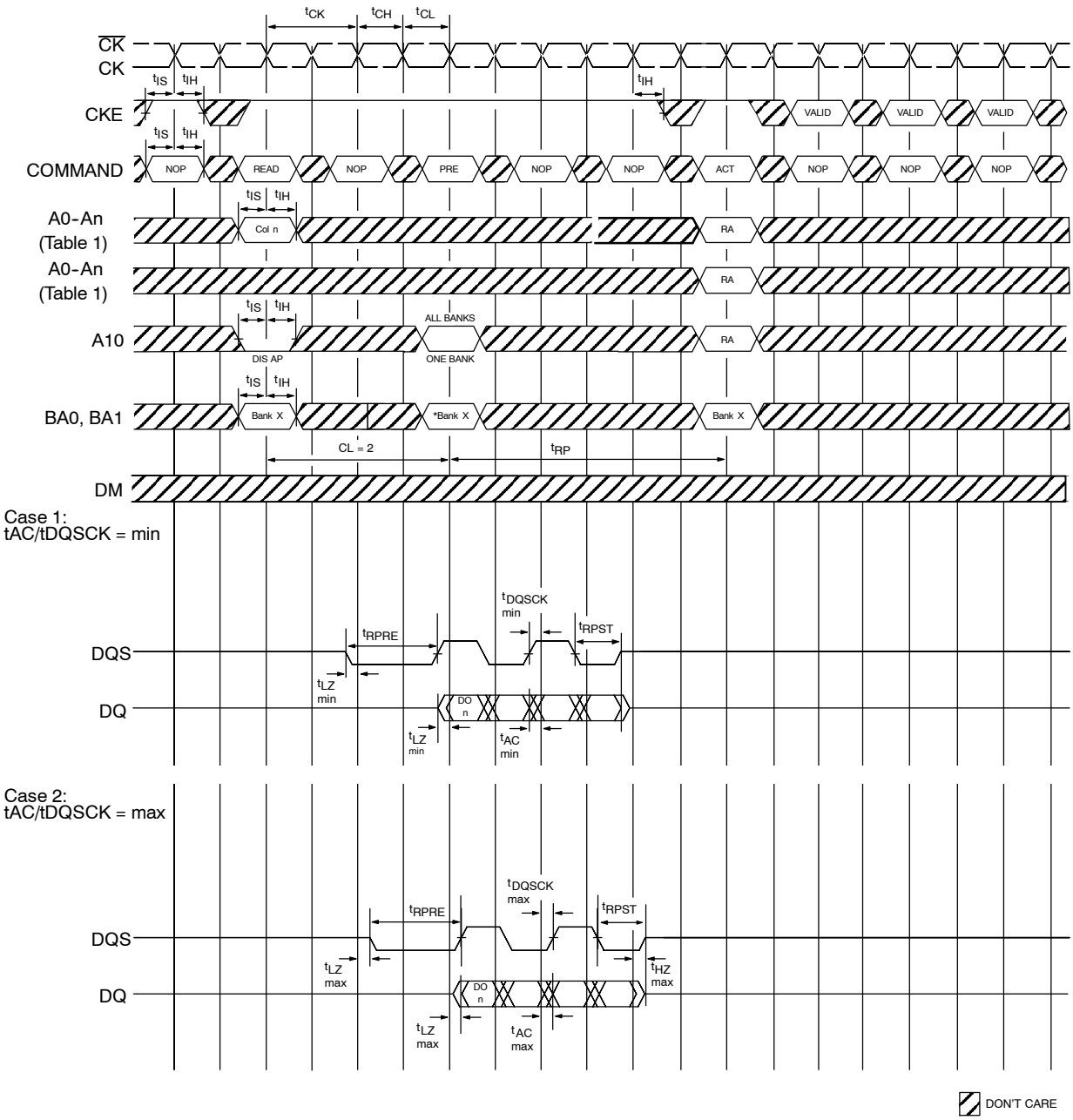
* = ”Don’t Care”, if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks)
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH
NOP commands are shown for ease of illustration; other valid commands may be possible after tRFC.
DM, DQ and DQS signals are all ”Don’t Care”/High-Z for operations shown

Figure 47 - AUTO REFRESH MODE



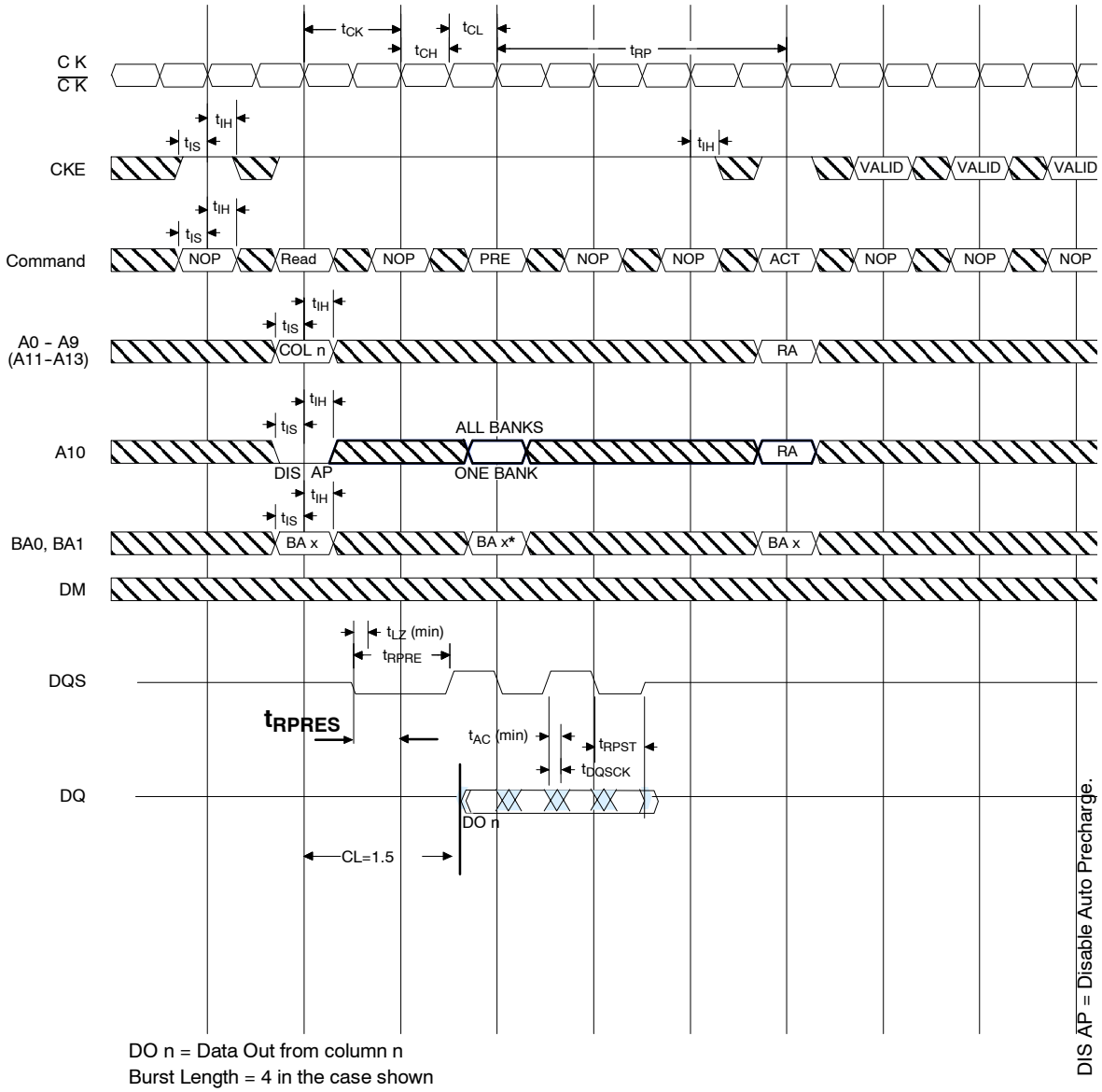
* = Device must be in the "All banks idle" state prior to entering Self Refresh mode
** = tXSNR is required before any non-READ command can be applied, and tXSRD (200 cycles of CK) is required before a READ command can be applied.

Figure 48 - SELF REFRESH MODE



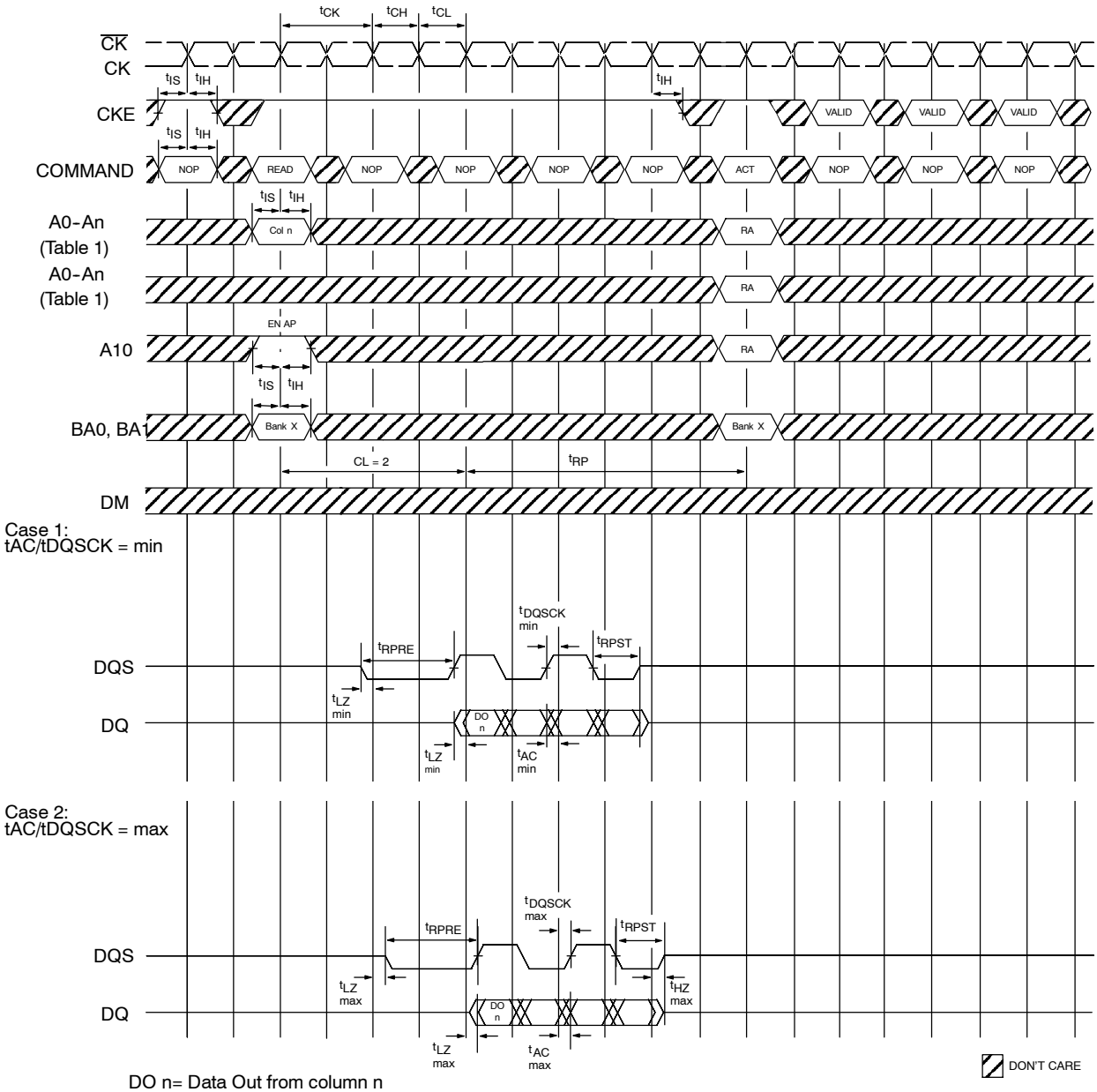
DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

Figure 49 - READ - WITHOUT AUTO PRECHARGE



DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
***** = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

Figure 50 - READ WITHOUT AUTOPRECHARGE (CL=1.5, BL=4)



DO n= Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

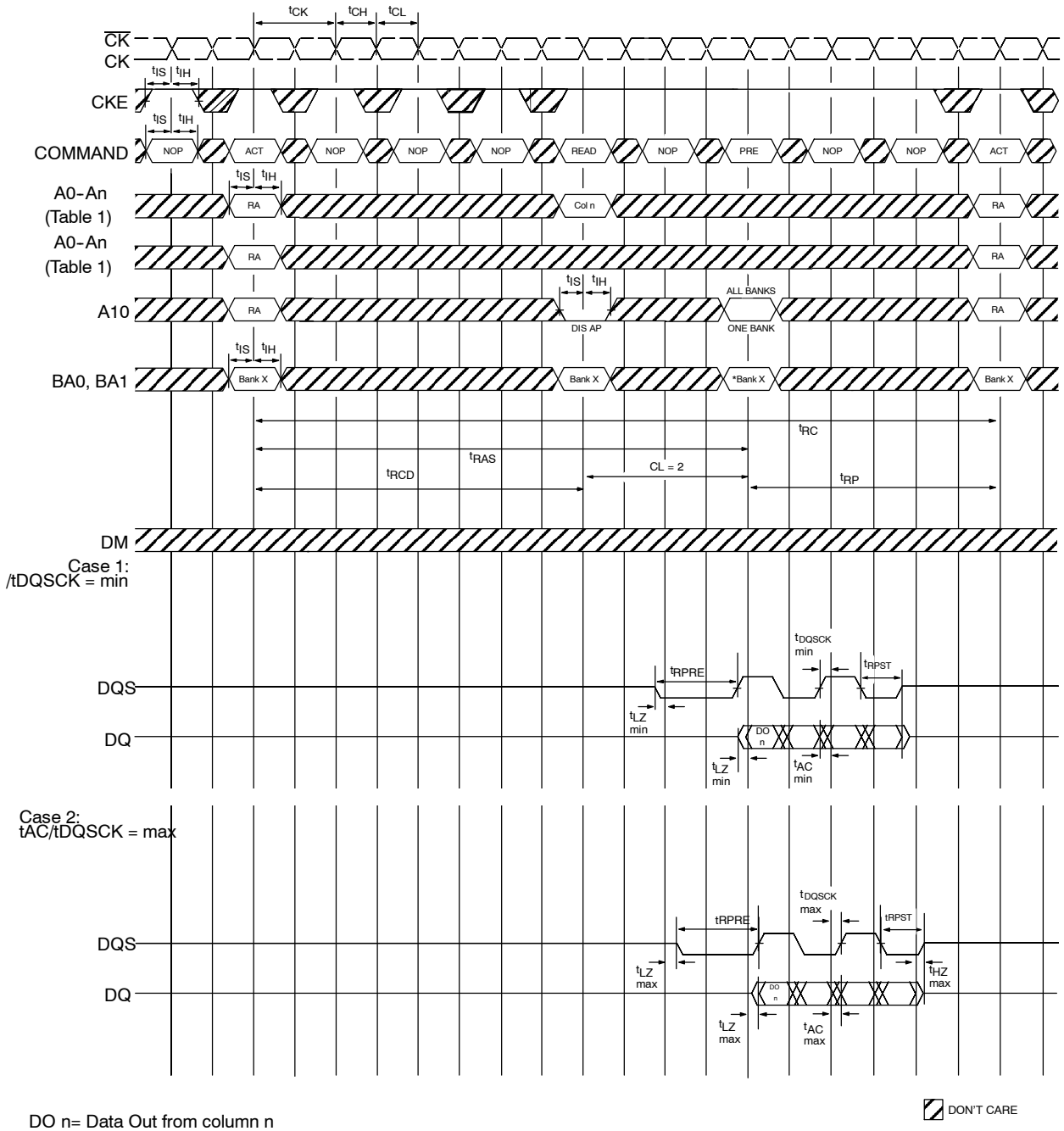
EN AP = Enable Autoprecharge

ACT = ACTIVE, RA = Row Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

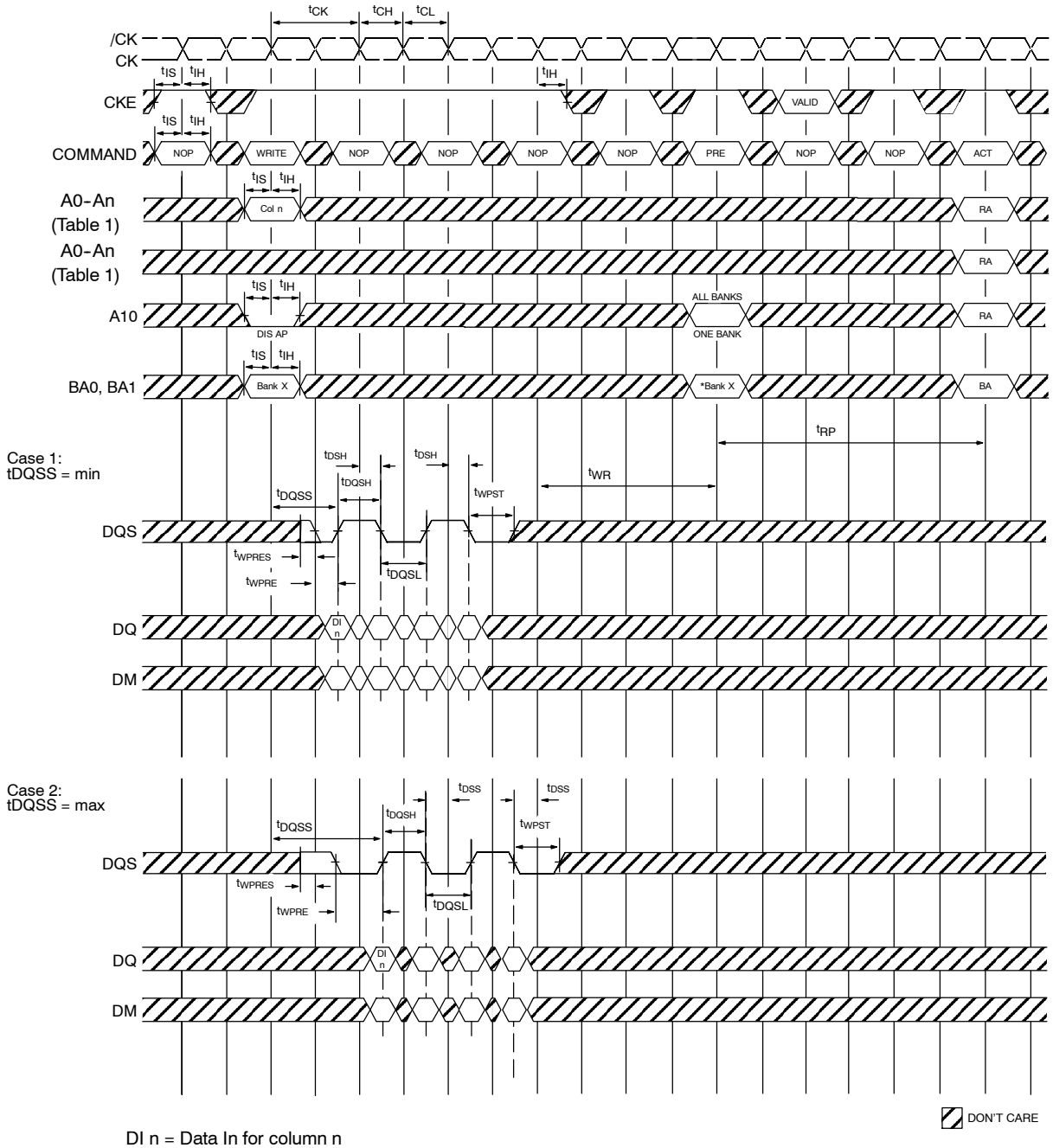
The READ command may not be issued until tRAP has been satisfied. If Fast Autoprecharge is supported, tRAP = tRCD, else the READ may not be issued prior to tRASmin - (BL*tCK/2).

Figure 51 - READ - WITH AUTO PRECHARGE



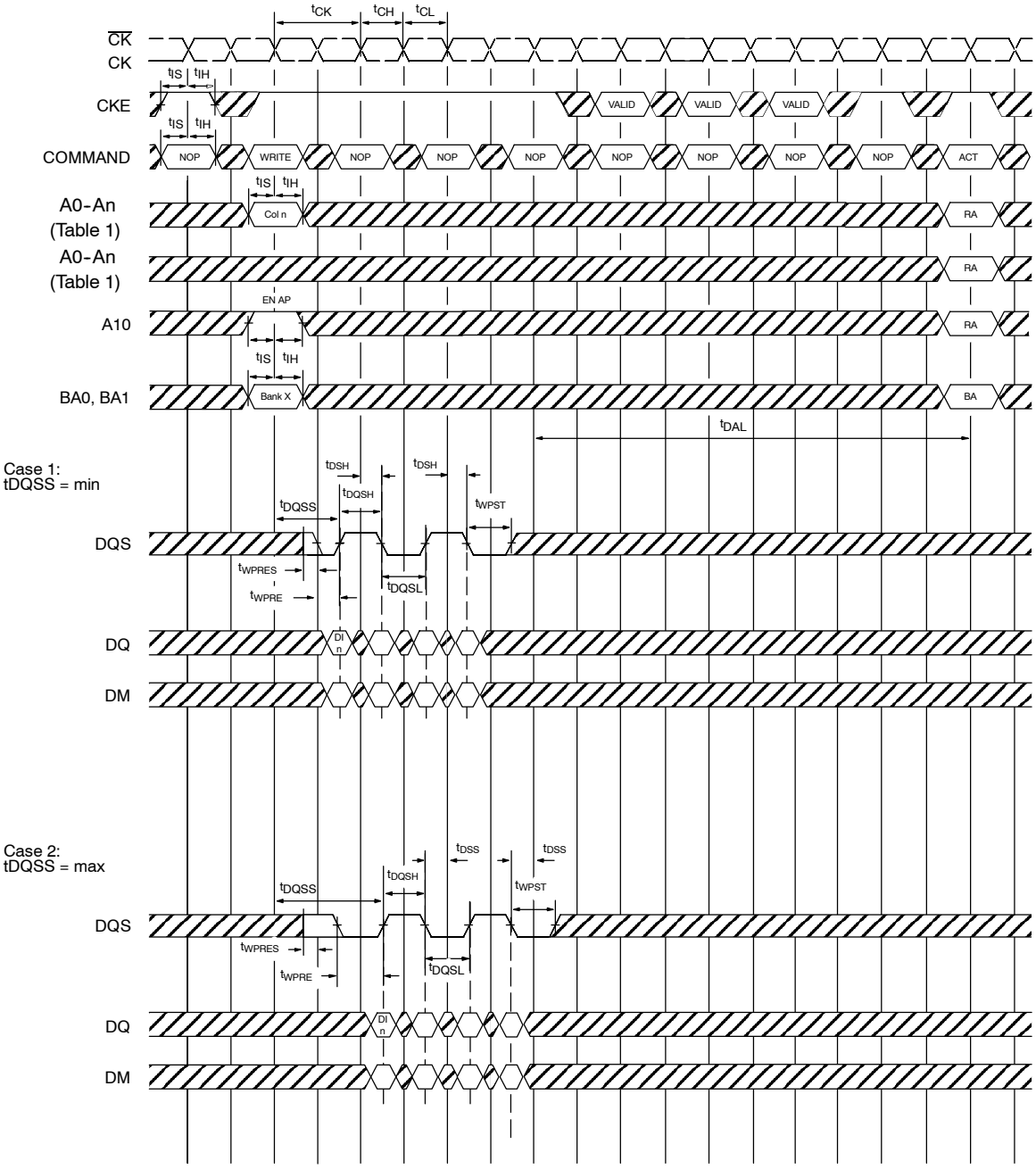
DO n= Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that tRCD > tRCD MIN so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

Figure 52 - BANK READ ACCESS



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge.
Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

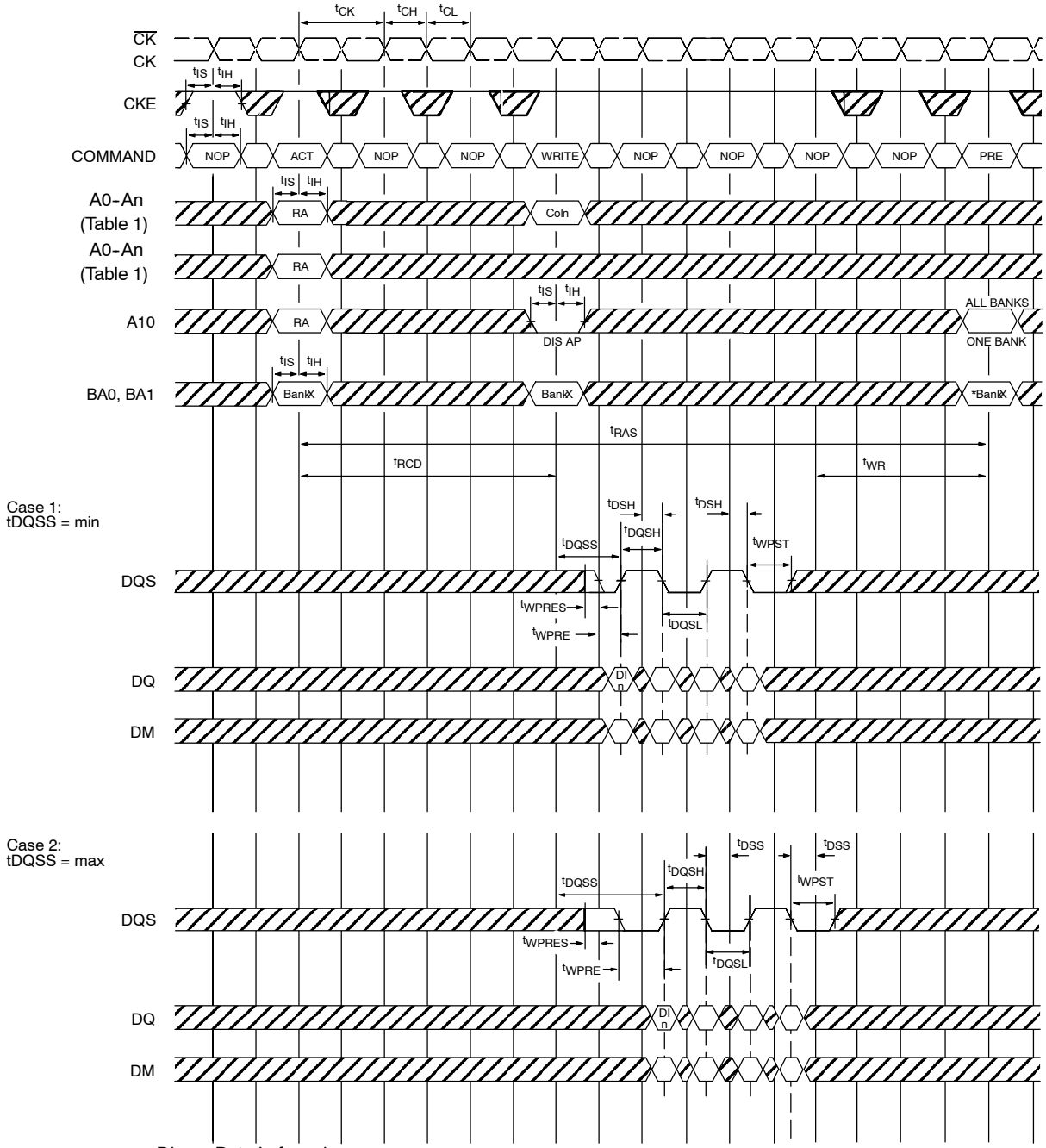
Figure 53 - WRITE - WITHOUT AUTO PRECHARGE



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
EN AP = Enable Autoprecharge
ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge.

DON'T CARE

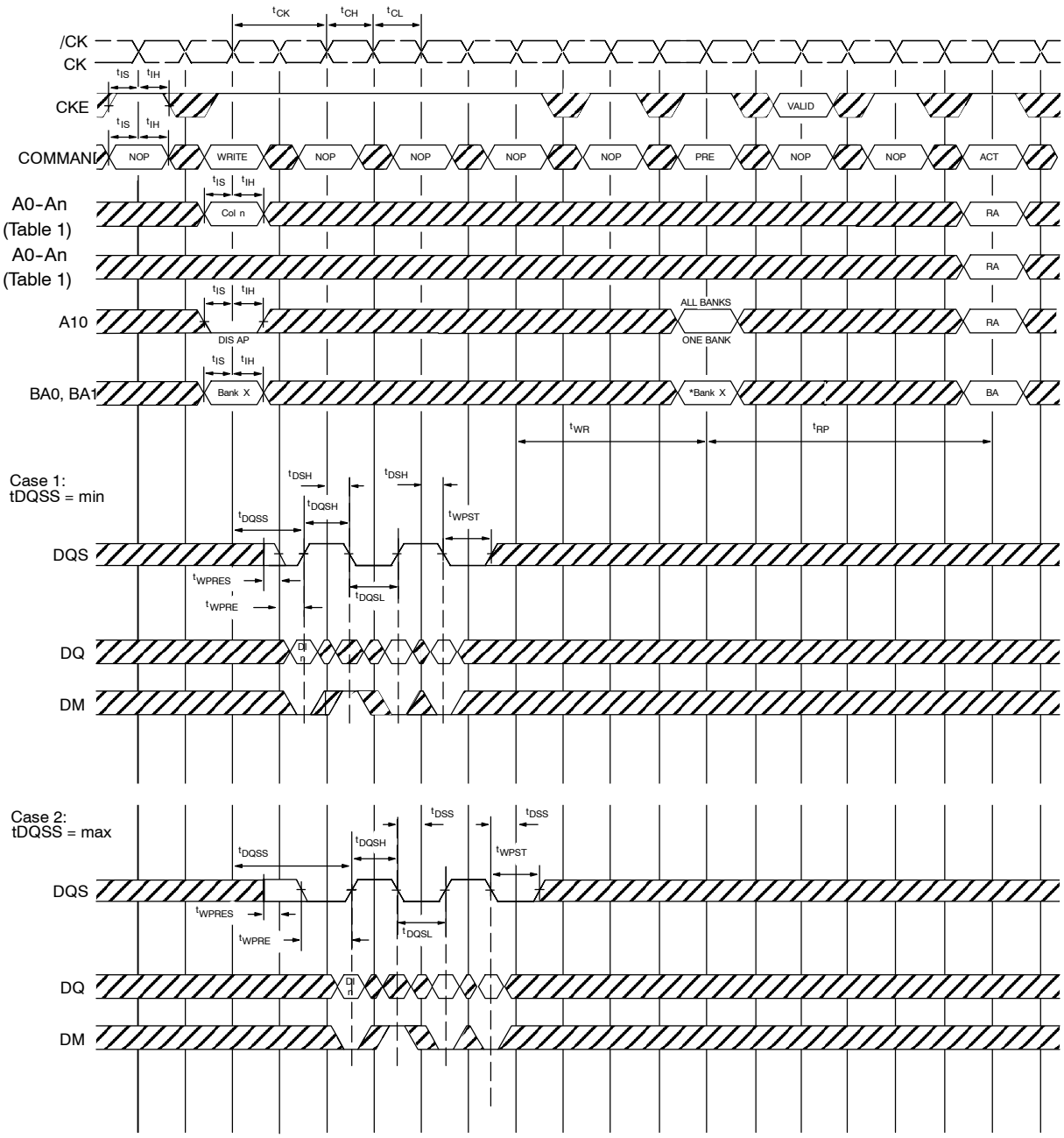
Figure 54 – WRITE – WITH AUTO PRECHARGE



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge.
Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

DON'T CARE

Figure 55 - BANK WRITE ACCESS



DI n= Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n (the second element of the four is masked)
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge.
Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

Figure 56 – WRITE – DM OPERATION

Annex A (informative) Differences between JESD79E and JESD79D

This table briefly describes most of the changes made to this standard, JESD79E, compared to its predecessor, JESD79D (January 2004). Some punctuation changes are not included.

Page	Description of Change
6	Per JCB-04-028 In **Table 2 – Pin Descriptions** – In the description for Clock Enable, added two lines of explanatory text before the last sentence.
12	Per JCB-04-028 In **Truth Table 1a – Commands** – Added Note 12. – For Auto Refresh, added a reference to Note 12 .
13	Per JCB-04-028 In **Truth Table 2 – CKE** – Added Note 7. – For Self Refresh, added a reference to Note 7.
20	Per JCB-04-028 Under the heading **Self Refresh** – Added one line of text to the end of the first paragraph.
43	Per JCB-04-031 – New section, **Input Clock Frequency Change During Precharge Power Down**.
44	Per JCB-03-031 – Added **Figure 33. Clock Frequency Change in Precharge Power Down Mode**. – Subsequent figures renumbered .
50	In **Table 11, Electrical Characteristics and AC Timing, Part a, DDR333, DD266, DDR200** Per JCB-04-015 – For tRPRE and tRPST, added a reference to Note 33.
51	In **Table 11, Electrical Characteristics and AC Timing, Part B, DDR400A, DD400B, DDR400C** Per JCB-04-008 – For tCK, where CL=3, changed the Max from 8 ns to 7.5 ns. Per JCB-00-015 – For tRPRE and tRPST, added a reference to Note 33.
52	Per JCB-04-015 – Added explantory text to Note 15.
53	Per JCB-04-015 – Added Note 33 – Added **Figure 36. Method for Calculating Transitions and Endpoints**. – Subsequent figures renumbered .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