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SOC Implementation of Soft-Error Tolerance in Asynchronous Burst Mode Circuits

Chandu Kumari, T. Ravi Sekhar

Abstract*— The problem of soft errors in asynchronous burst-mode machines (ABMMs), and we propose the solution is an error tolerance approach, which leverages the inherent functionality of Muller C- elements, along with a variant of duplication, to suppress all transient errors. The proposed method is more robust and less expensive than the typical triple modular redundancy error tolerance method and often even less expensive than previously proposed concurrent error detection methods, which only provide detection but no correction The solution is an error tolerance approach, which leverages the inherent functionality of Muller C-elements, along with a variant of duplication, to suppress all transient errors, which leverages a newly devised soft- error susceptibility assessment method for ABMMs, along with partial duplication, to suppress a carefully chosen subset of transient errors. Progressively more powerful options for partial duplication select among individual gates, complete state/output logic cones or partial state/output logic cones and enable efficient exploration of the tradeoff between the achieved soft- error susceptibility reduction and the incurred area overhead. Furthermore, a gate-decomposition method is developed to leverage the additional soft-error susceptibility reduction opportunities arising during conversion of a two-level ABMM implementation into a multilevel one. Extensive experimental results on benchmark ABMMs assess the effectiveness of the proposed methods reducing soft-error susceptibility, and their impact on area, performance, and offline testability.

Index Terms*— Asynchronous burst-mode circuits, soft errors, soft-error mitigation, soft-error susceptibility, soft-error tolerance.

I. INTRODUCTION

When high-energy neutrons (present in terrestrial cosmic radiation) or alpha particles (which originate from impurities in the packaging materials) strike a sensitive region in a semiconductor device, the resulting single-event upset (SEU) can alter the state of the system resulting in a soft error. Although soft errors cause no permanent damage, they can severely limit the reliability of electronic systems. Soft errors in memories (both static and dynamic) have traditionally been a much greater concern than soft errors in combinational logic circuits (for the same minimum feature size) since memories contain by far the largest number and density of bits susceptible to particle strikes. In the next decade, technology trends, smaller feature sizes, lower voltage levels, higher operating frequencies, and reduced logic depth—are projected to cause an increase in the soft error failure rate in core combinational logic in integrated circuits [5], [7]. In [9], it has been shown that propagated SEUs will constitute an important failure mode in integrated circuits. Soft errors are emerging as a serious threat to the reliable operation of integrated circuits (ICs). When high-energy neutrons or alpha particles strike a sensitive region in a semiconductor device, they generate a single-event transient (SET) that may alter the state of the system, resulting in a soft error. The projected increase in the Soft-Error failure Rate (SER) of near-future CMOS technologies has sparked numerous efforts to develop error protection mechanisms for digital ICs [1]–[4]. Since the majority of commercial ICs available in the marketplace follow the clocked design paradigm, most of these efforts target synchronous circuits. Yet, clock less design has recently received increased attention, and several advanced asynchronous design styles have been carving an increasing niche in the market [5].Moreover, due to their low power consumption and electromagnetic noise emission, asynchronous circuits are gaining a particularly strong foothold in mission- critical applications, wherein reliability is key. Soft- error protection techniques can be divided into *error tolerance* and *error mitigation* approaches. The former take an expensive holistic approach and attempt to tolerate all SETs in the circuit, while the latter aim to explore the tradeoff between the provided protection and the incurred cost. Unfortunately, tolerance and mitigation methods developed for synchronous circuits are not directly portable to the asynchronous domain. Moreover, and while a few soft-error analysis, tolerance, and design hardening methods have been developed for the class of quasi-delay-insensitive (QDI) circuits, their utility is limited in other classes, each of which presents its own challenges This paper aims to provide an array of solutions for coping with soft errors in the class of asynchronous burst-mode machines (ABMMs). Specifically, the contributions of this paper include the following.

A duplication-based soft-error-tolerant ABMM design methodology, which leverages the inherent functionality of C-elements to reduce the cost and improve the robustness of the triple modular redundancy (TMR) approach. A soft-error susceptibility assessment methodology for ABMMs, based on an enhanced version of a previously developed asynchronous-circuit fault simulator. A soft-error mitigation solution, based on the newly developed soft-error susceptibility assessment methodology. Three alternative partial duplication options, which select judiciously among individual gates, complete cones of state/output logic, or partial cones of state/output logic, are proposed in order to explore the tradeoff between area overhead and SER reduction in ABMMs.

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A gate-decomposition strategy, which maximizes the ability of the decomposed structure to suppress soft errors when a two-level ABMM is converted into a multilevel equivalent. Formulated as an integer linear program (ILP), the proposed method aims at maximizing *logic masking* through efficient distribution of the input signals of each decomposed gate to its constituents. A halting- based test generation method that retains offline testability for most faults in a soft-error-tolerant ABMM, based on an extension of a previously developed test generation tool.

II. RELATED WORK

ABMMs constitute a class of *Huffman* circuits, which consist of a set of combinational functions, computing the next state and output of the circuit, and a set of feedback lines, storing the state of the circuit. No clock and no state registers are used in these circuits; however, delay elements are often added to eliminate *essential hazards*1. Given the absence of a clock, *communication protocols* are needed to ensure correct interaction between an asynchronous circuit and its environment. These protocols define the properties of the stimuli (response) that the environment (circuit) is allowed to provide to the circuit (environment). Based on these protocols, various classes of asynchronous circuits are defined.TMR employs three copies of a given circuit and a majority vote to decide the final output. Thus, any error(s) affecting only one of the copies is tolerated. As has been done for tolerating soft errors in both synchronous and in asynchronous circuits, the majority voter module can be substituted by a C- element. A C-element generates a rising (falling) transition when rising(falling) transitions have occurred on all of its inputs. Thus, when the inputs to a three-input C-element are nominally identical signals, a transient error in one of them will be suppressed and will not change the output of the C- element. The latter remains in its previous state until all three inputs to the C-element make the same transition, after which the output of the C-element follows.

III. PROPOSED WORK

A. TMR based soft-error tolerance

TMR employs three copies of a given circuit and a majority voter to decide the final output. Thus, any error(s) affecting only one of the copies is tolerated. As has been done for tolerating soft errors in both synchronous and in asynchronous circuits, the majority voter module can be substituted by a C-element. A C-element generates a rising (falling) transition when rising (falling) transitions have occurred on all of its inputs. Thus, when the inputs to a three-input C-element are nominally identical signals, a transient error in one of them will be suppressed and will not change the output of the C- element. The latter remains in its previous state until all three inputs to the C-element make the same transition, after which the output of the C-element follows. The TMR-based soft-error-tolerant design method for ABMMs is shown below.

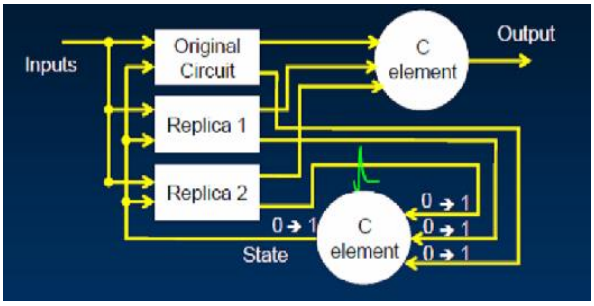

Fig.1:TMR based soft error tolerance in ABMMs

The original circuit is triplicated, and C-elements are inserted at the state/output lines. When an SET strikes in any one of the three replicas, these C-elements prevent its effect from propagating to a state line or output. However, transient errors in the newly introduced C-elements cannot be tolerated. Specifically, a transient error that temporarily changes the state of a C-element driving an output may result in a hazard that can jeopardize communication of the circuit with its environment. Moreover, a transient error that temporarily changes the output of a C- element on a state line may propagate through the combinational feedback back to it. The Proposed solution for cross-coupled structure of C-element

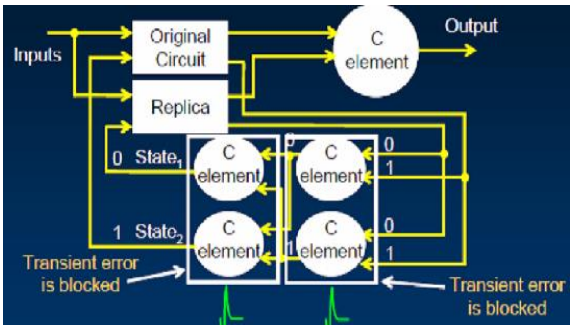

Fig.2:Tolerating Error on state-line C- Element

Hence, all inputs of the C-element will agree on the erroneous value, forcing an incorrect permanent change in the state of the three copies and, by extension, the state/output of the circuit. In other words, an SET in a C-element driving a state line is far worse than an SET in a C-element driving an output since it results in a chain reaction of erroneous states, outputs, and, by extension, miscommunication between the ABMM and the environment. This limitation, along with the excessive cost incurred, makes TMR a rather non appealing option for designing soft-error-tolerant ABMMs.

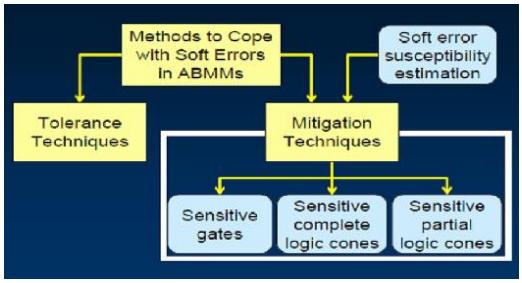

Fig.3: Coping with soft error in ABMMs

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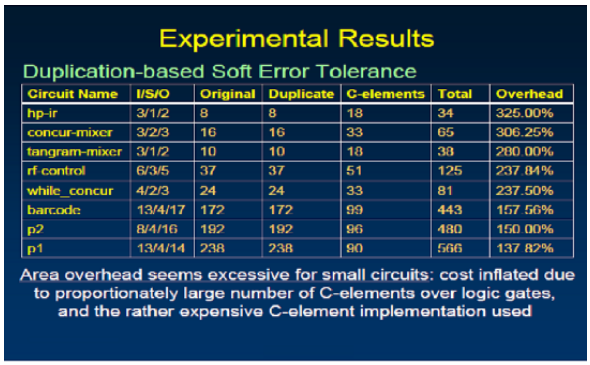
IV. RESULTS

Soft-Error Tolerance Results The results for duplication-based soft-error tolerance are presented including the following details of the circuits that were used: name, number of inputs (I), number of states (S), number of state bits (Bits), and number of outputs (O). The fourth major heading summarizes the total literal and gate count of the soft-error- tolerant AB MM. While for small circuits the area overhead may seem excessive (i.e., over 300%), we raise caution that this cost is significantly inflated due to the proportionately large number of C-elements over logic gates. Indeed, in larger circuits, such as and, this proportion changes, and the percentile overhead reduces drastically (i.e., less than 150%).



Circuit Name	I/S/O	Original	Duplicate	C-elements	Total	Overhead
hp-ir	3/1/2	8	8	18	34	325.00%
concur-mixer	3/2/3	16	16	33	65	306.25%
tangram-mixer	3/1/2	10	10	18	38	280.00%
rf control	6/3/5	37	37	51	125	237.84%
while_concur	4/2/3	24	24	33	81	237.50%
barcode	13/4/17	172	172	99	443	157.56%
p2	8/4/16	192	192	96	480	150.00%
p1	13/4/14	238	238	90	566	137.82%

Table.1 Showing experimental results

Thus, we anticipate the area overhead be even lower for larger and more complex ABMMs. More importantly, assessing the overhead of the proposed duplication-based soft-error-tolerant ABMM design method should not be done in absolute terms but rather in comparison to the best known alternative for these circuits. The area cost of TMR and the minimum- cost CED method. For each circuit, the solution with the lowest area cost is shown in boldface. The area cost of duplication-based tolerance is, on average,24% less than that of TMR. We also note that, for 8 out of the 13 benchmark circuits, duplication-based soft-error tolerance incurs lower overhead, even in comparison to the CED methods in [8] With respect to performance, the duplicate circuit utilized in the soft-error tolerance approach, or the partial duplicate in the mitigation methods, operates in parallel with the original circuit. However, and similar to that when majority voters are employed in a typical soft-error-tolerant TMR design, the addition of C-elements at the output/state functions increases the delay of the circuit and equivalently reduces the performance of the controller.

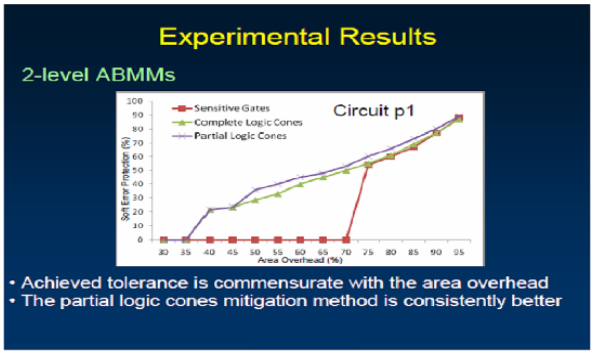


Fig.4 Graph representing Experimental results

A. Synthesis Report

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
Total no. of paths / destination ports: 16 / 16

Offset: 8.003ns (Levels of Logic = 1)
Source: instance1/txdp (FF)
Destination: dp (PAD)
Source Clock: clk rising
Data Path: instance1/txdp to dp

Cell:in->out fanout Delay Delay Logical Name (Net Name)

FDE:C->Q 13 1.085 2.250 instance1/txdp(instance1/txdp)
OBUF:I->O 4.668 dp_OBUF (dp)

Total 8.003ns (5.753ns logic, 2.250ns route) (71.9% logic, 28.1% route)

==========

CPU : 8.47 / 8.92 s | Elapsed : 8.00 / 8.00 s

Total memory usage is 96900 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings: 0 (0 filtered)
Number of infos : 0 (0 filtered)

V.CONCLUSION

Careful examination of the impact of transient errors in ABMMs reveals the limitations of traditional error tolerance methods, such as the standard TMR approach, in protecting these circuits. Toward soft- error-tolerant ABMMs, the solution proposed herein leverages the inherent functionality of C-elements and extends a duplication-based error tolerance method to withstand more soft errors than the typical TMR method. At the same time, the proposed solution incurs less area overhead, even when compared to previous CED methods. Furthermore, based on a newly developed soft-error susceptibility assessment method for ABMMs, soft-error solutions can also be devised. Indeed, as demonstrated experimentally, partial duplication through careful selection of individual gates, complete state/output logic cones, or partial state/output logic cones enables efficient exploration of the tradeoff between the incurred overhead and the achieved soft-error susceptibility reduction.

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