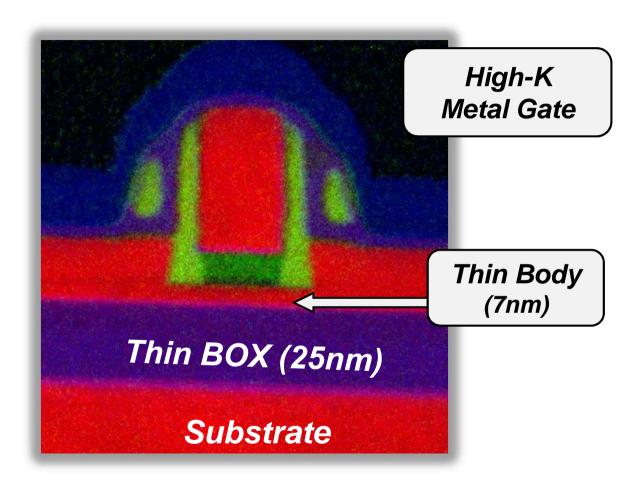
# Process and Design Solutions for Exploiting FD-SOI Technology Towards Energy Efficient SOCs

## Philippe FLATRESSE

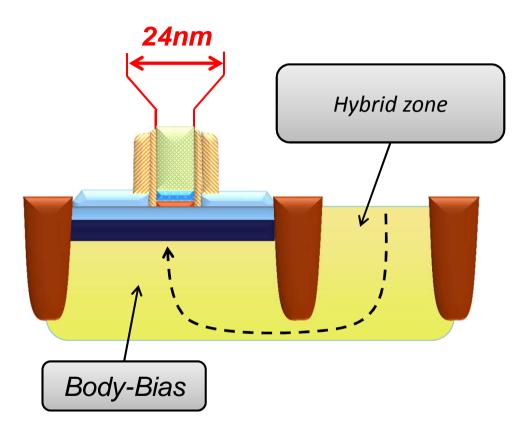
Technology R&D
Central CAD & Design Solutions

**STMicroelectronics** 

## 28nm Planar UTBB FD-SOI Transistor



## 28nm Planar UTBB FD-SOI Advantages

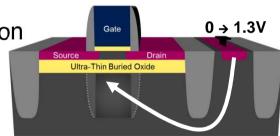


- Shorter channel length
  - 24nm technology!
- Better electrostatics
  - Faster operation
  - Low voltage
  - Reduced variability
- Total dielectric isolation
  - Latch up immunity
- Lower leakage current
  - Less sensitive to temperature

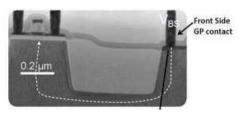
# **Body Biasing (BB)**

#### A very reasonable effort for extremely worthwhile benefits

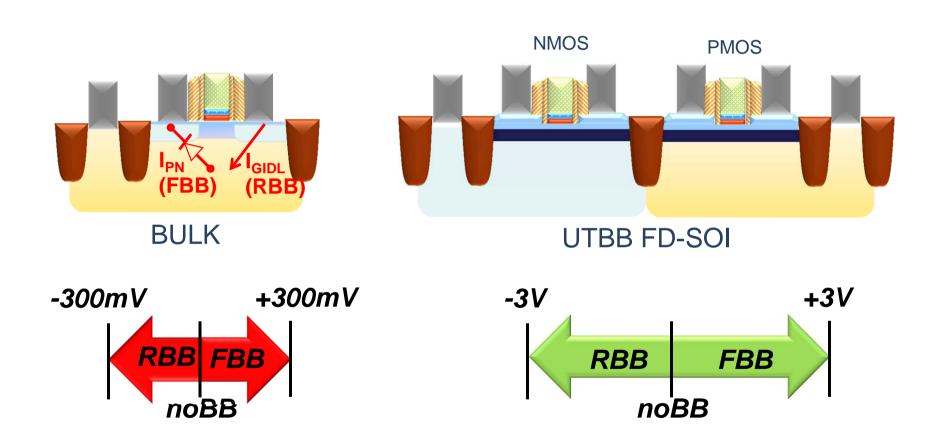
- An extremely powerful and flexible concept in FD-SOI to:
  - Boost performance
  - Optimize passive and dynamic power consumption
  - Cancel out process variations and extract optimal behavior from all parts



- Comparatively easy to implement if you've ever done DVFS you'll have no difficulty with Body Biasing
   Back-gate contact
  - No area penalty compared to Bulk
  - Reuse of Bulk design techniques
  - Speed/Power control

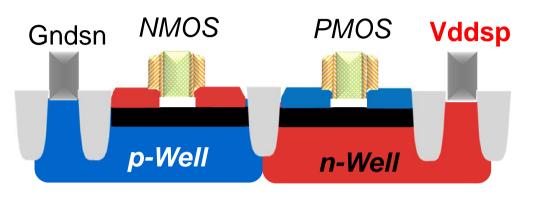


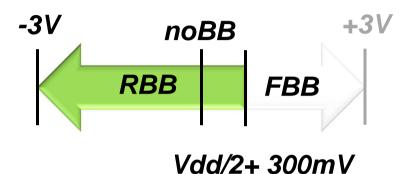
## **Extended Body Bias Range in UTBB FD-SOI**



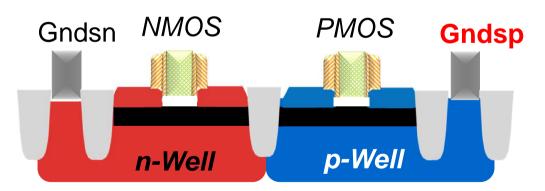
## **UTBB FD-SOI: Extended Body Voltage Range**

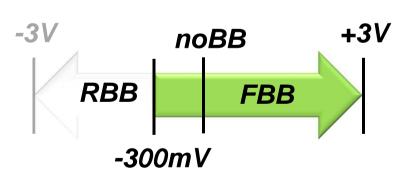
Conventional Well (CW) - RBB





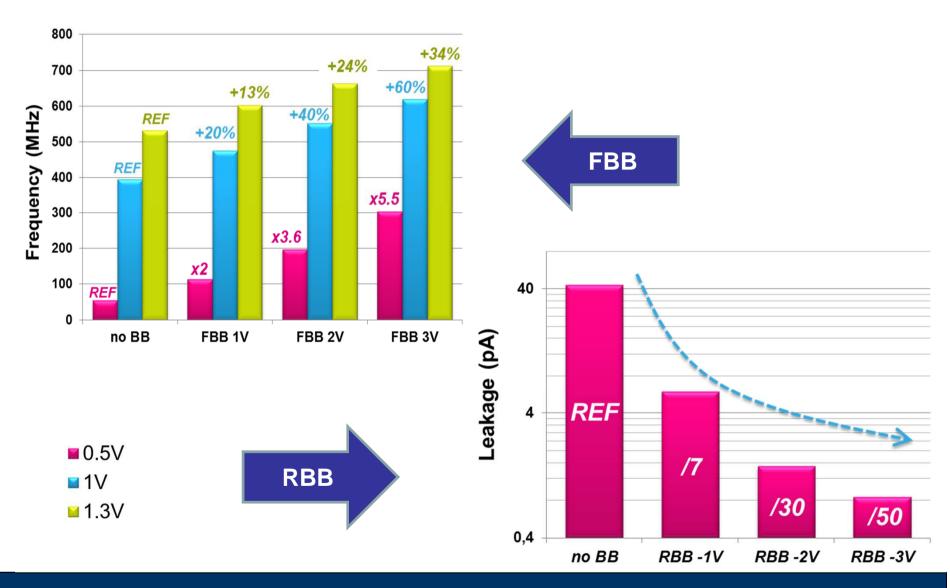
Flip Well (FW) - FBB





Efficient knob for speed/leakage optimization

## **Body Bias Efficiency - Silicon Evidence**



## FBB usage per market segment

Infrastructure - Networking Servers and Storage



Supply: 0.7 - 0.9V

high number multicore
DVFS & FBB tuning for best
MIPS/W ratio.
Adapt perf&power to workload



#### **Power efficiency**

#### **28 FD-SOI:**

Configuration

Up to -50% total power reduction versus 28G(mobile) @ 0.6V FBB for ultimate power efficiency tuning

#### Consumer



Wide DVFS
FBB linked to CPU workload
& thermal conditions



#### **Flexibility Perf/Power**

#### **28 FD-SOI:**

Up to -50% power reduction FBB provides +18% max. performance boost versus 28G(mobile)

#### Internet of Things

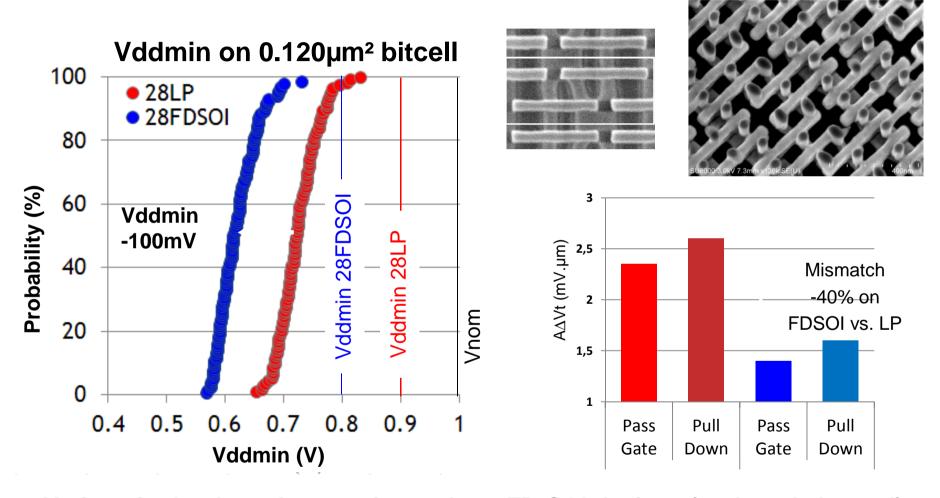
# Supply: 0.6V-0.9V FBB: 0 - 1.5V FBB to solve the power/performance paradigm Ultra-Low-Energy Ultra-Low-Energy Voltage 0.3V0.4V Reverse Body Biasing

#### Ultra power efficiency

#### 28 FD-SOI:

Up to x 4 perf/power ratio versus 28G(mobile) at low voltage Low voltage power efficient performance. Reduce idle current

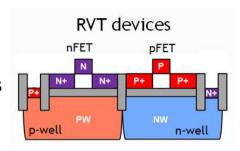
## **Improved Memory Minimum Voltage**



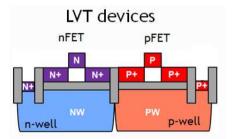
Vmin gain thanks to better mismatch on FD-SOI devices (undoped channel)

## FD-SOI Unique "Single Well" Architecture

SRAM regular wells



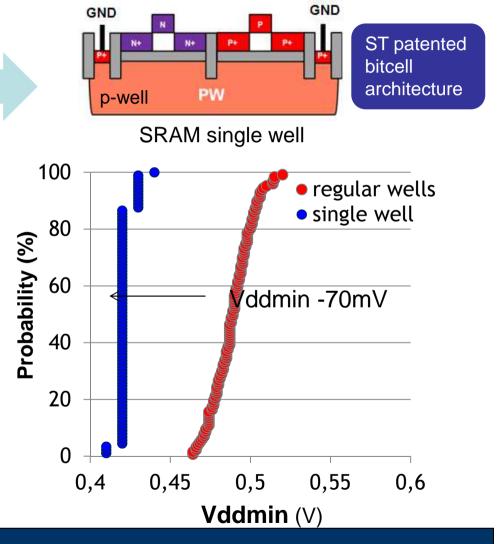
SRAM flip-well architecture



### Single Well SRAM

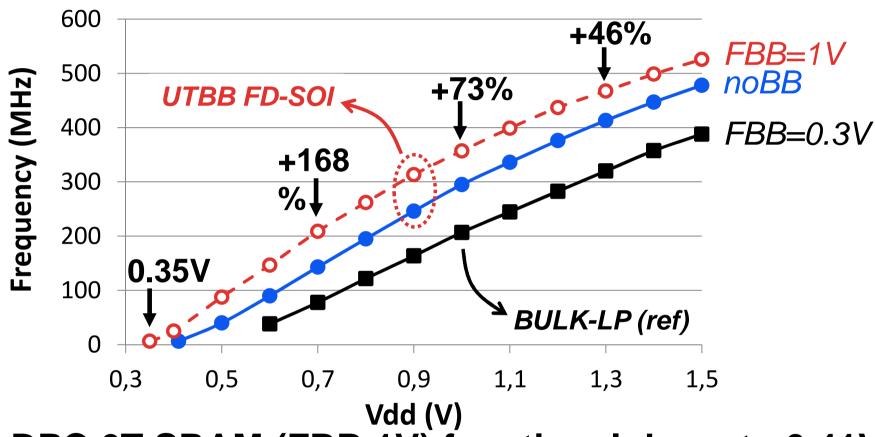
Optimized stability helping behavior at low voltage

→ Power efficiency



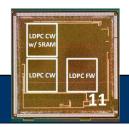
nFET RVT pFET LVT

### Si Evidence: LDPC on UTBB FD-SOI

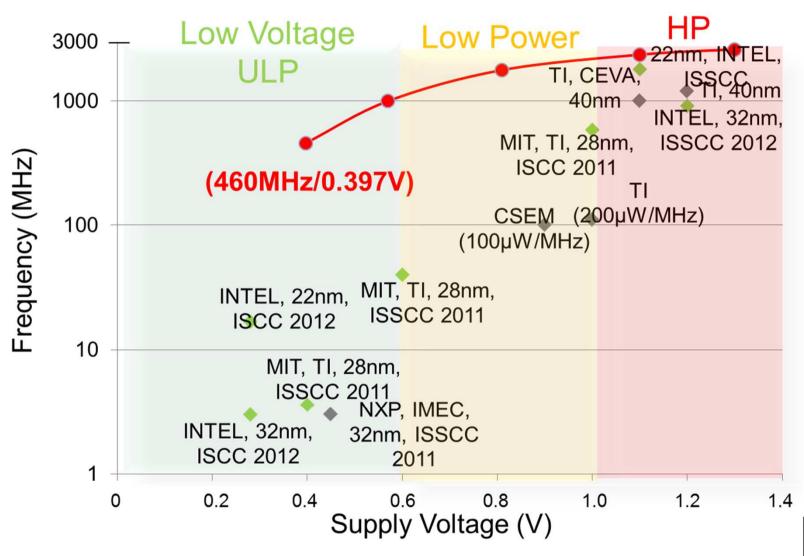


LDPC 6T-SRAM (FBB 1V) functional down to 0.41V

© 2013 IEEE - International Solid-State Circuits Conference Ultra-Wide Body-Bias Range LDPC Decoder in 28nm UTBB FD-SOI



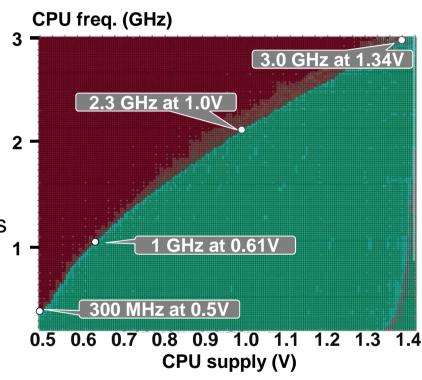
## State of the Art UWVR DSP in FDSOI:



© 2014 IEEE - International Solid-State Circuits Conference 27.1: A 460MHz@397mV - 2.6GHz@1.3V 32bit VLIW DSP

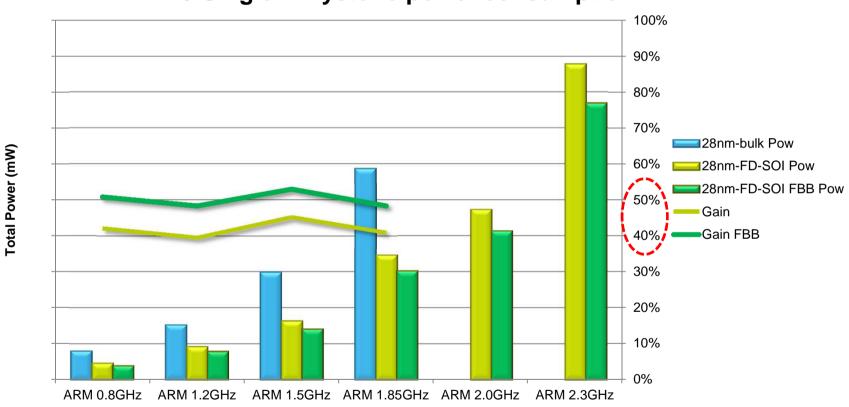
## Cortex A9: FD-SOI allowing Ultra-Wide DVFS

- FD-SOI allows the widest Vdd range for voltage scaling
- Still guaranteeing top notch speeds at very low operating voltage
  - >5x when compared to 28LP technology
  - >35% when compared to 28G technologies
- DVFS energy efficiency optimization is further extended thanks to body bias
  - Allowing to balance and optimize the static and dynamic power consumption components

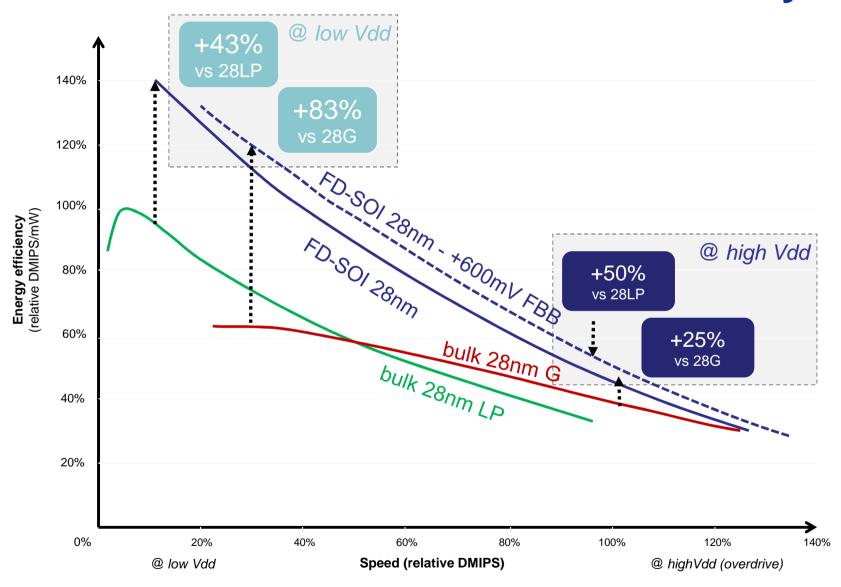


## **Cortex A9 Power vs. Performances**

#### **A9 Single Dhrystone power consumption**



## 28nm FD-SOI Best in class efficiency





# Faster, Cooler, Simpler technology

- FD-SOI transistors up to 30% faster than bulk
- Outstanding power efficiency at every level
- Extensive use of existing fab infrastructure

# Enhanced design options

- Back-biasing as a flexible and powerful optimization
- Very large operating range for the same design
- Ultra-wide range DVFS

# Mature process & ecosystem

- Ecosystem ready at all stage: wafer supply, design and manufacturing
- Extended IP offer
- Strategic collaboration between Samsung and ST

FD-SO gives your SOC competitive advantages