



Intel Details Digital Radios, Solar-Powered CPUs

by [Joel Hruska](#) — Sunday, February 19, 2012, 04:53 PM EDT

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The last Intel unveil we'll be focusing on is the company's new variable-precision floating point unit (FPU). The FPU handles all math involving a decimal (floating point); conventional x86 CPUs have an FPU that's capable of performing single (32-bit) and double (64-bit) precision operations. Current CPUs utilize the entire FPU address space for performing operations. The unit assumes, by default, that it must be as accurate as it possibly *can* be. If you're calculating spacecraft trajectory or measuring subatomic particles, such accuracy is vital. If you're rendering Skyrim or updating Facebook, it isn't.

Variable Precision Floating Point Unit

(10.3) A 1.45GHz 52-to-162GFLOPS/W Variable-Precision Floating-Point Fused Multiply-Add Unit With Certainty Tracking in 32nm CMOS

- 1st reported variable-precision floating point unit with accuracy tracking for multiply-add
- Today's floating-point math wastes energy, time, and storage by using worst-case precision everywhere
- Using variable precision (24-bit→12-bit→6-bit) as needed can cut energy by 50%
- Uses NTV circuits for up to 7x further efficiency gain

The variable-precision FPU Intel is showing off is capable of adjusting how precise it is depending on the needs of the software in question. Because it only uses full precision when it's necessary, the FPU uses up to 50% less energy than a conventional unit without sacrificing performance or accurate results. Again, this isn't a logic unit that's intended for a near-term shipping product, but it's an interesting example of how power efficiency can be improved by ensuring that workloads are optimally distributed and managed. Back when FPUs were first designed and implemented, there was no way to tell what sort of work was being performed. The only safe option was to assume a universal worst-case scenario. Now, that's no longer the case.

Intel's other presentations at ISSCC this year will discuss Ivy Bridge and additional products that use the company's [22nm Tri-Gate transistor technology](#), new SRAM designs that use NTV to lower operating voltages, and an NTV SIMD implementation that shows how that technology can be applied to graphics units. NTV is at the heart of much of what Intel is working on as far as next-generation power optimization, but the company isn't betting everything on a single technology. Their discussion of digital radio implementation and the use of a variable-precision FPU is evidence of how improved power efficiency is being chased from every angle.

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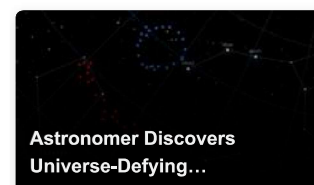


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