COEN/ELEN 921c
Homework 4

Prob 1

Again, use the circuit diagram from P2.24 (Text Prob 2.24, Fig P2.24). Answer the following:

a) Assuming the propagation delay through all the gates is identical and equal to "t". What is the propagation delay through this circuit?

4t

b) Assuming the propagation delay through the gates is not equal, it is:

INVERTER = 5 ns NAND = 10 ns NOR = 12 ns OR = 8 NS

What is the propagation delay through this circuit (in ns)?

c) What is the worst case (slowest) signal path through this circuit, ie. starting at which input, through which gates, getting to the output?

A → NOT → NAND → OR → NAND → output

Prob 2

Given the following set of electrical and switching specs for the 3 gates show:

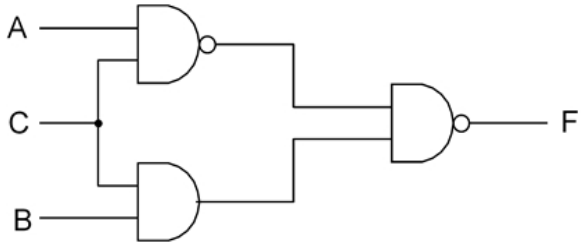
	NAND 74xx	NAND 74LSxx	AND 74xx	Units
Voh	2.4	2.7	2.4	V
Vol	0.4	0.5	0.4	V
Vih	2.0	2.0	2.0	V
Vil	0.8	0.8	0.8	V
Iih	40	20	40	uA
Iil	1.6	0.4	1.6	mA
Ioh	0.4	0.4	0.8	mA
Iol	16	8	16	mA
Icch	8	1.6	21	mA
Iccl	22	4.4	33	mA
t_{PHL}	14	21	17	ns
t_{PLH}	7	8	9	ns

a. What is the maximum fan-out for a 74xx AND gate driving 74LSxx NAND gates?

min. ($I_{OH}/I_{ih} = 40$; $I_{OL}/I_{IL} = 16/0.4 = 40$)

b. What is the average power consumption of the 74xx AND gate package?

c. What is the propagation delay of the circuit shown. Calculate average propagation delay for each gate, and use those to determine delay of complete circuit.



Prob 3. Consider text problem 2.22, ie. the "alarm" problem. It has 4 inputs (A – D) as described in problem 2.22. Label the output as Z (rather than F(A,B,C,D).

Z = AB' + C'D + AD'

a) Write a VHDL behavioral module called "alarm" with an architecture called "alarm_behav".

b) Using AND gates, OR, gates, and INVERTERs, rewrite the architecture description as a structural architecture called "alarm_struc". You can assume components AND2, OR2 and INV have been defined previously, and available for your use.

Prob 4. Text Problem 3.1 (a & b)

Prob 5. Text Problem 3.2 (a & b)

Prob 6. Text Problem 3.3 (a & b)

Prob 7. Text Problem 3.12 (a only)