

COEN 921c
Homework 4 Solution

Prob 1

Again, use the circuit diagram from P2.24 (Text Prob 2.24). Answer the following:

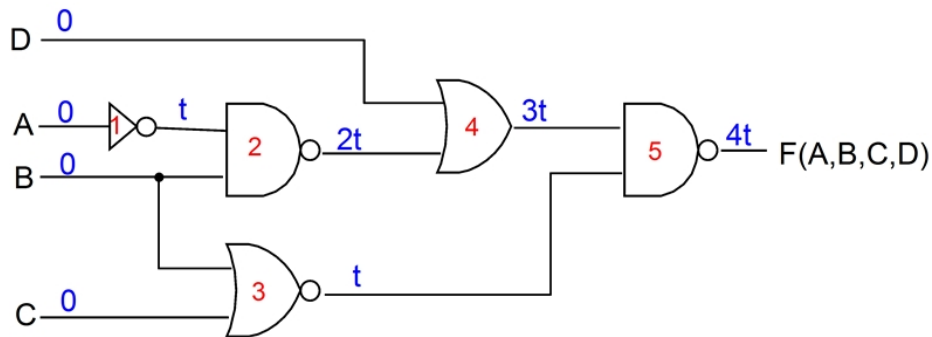


Figure P2.24

- a) Assuming the propagation delay through all the gates is identical and equal to "t". What is the propagation delay through this circuit?

Using $\max(t_1, t_2, \dots, t_n) + t_{pd}$ for the delay at each gate output results in the delay at NAND gate 5 is 4t.

- b) Assuming the propagation delay through the gates is not equal, it is:

INVERTER = 5 ns NAND = 10 ns NOR = 12 ns OR = 8 ns

What is the propagation delay through this circuit (in ns)?

The path from input A through INV 1, NAND 2, OR 4, and NAND 5 is the delay of the circuit. Since the delay is NOT uniform 't', we must add up the individual delays

5 ns + 10 ns + 8 ns + 10 ns = 33 ns So, the delay through the circuit is **33 ns**.

- c) What is the worst case (slowest) signal path through this circuit, ie. starting at which input, through which gates, getting to the output?

It is from: Input A through INV 1, NAND 2, OR 4, and NAND 5

Prob 2

Given the following set of electrical and switching specs for the 3 gates show:

	NAND 74xx	NAND 74LSxx	AND 74xx	Units
V _{oh}	2.4	2.7	2.4	V
V _{ol}	0.4	0.5	0.4	V
V _{ih}	2.0	2.0	2.0	V
V _{il}	0.8	0.8	0.8	V
I _{ih}	40	20	40	uA
I _{il}	1.6	0.4	1.6	mA
I _{oh}	0.4	0.4	0.8	mA
I _{ol}	16	8	16	mA
I _{cch}	8	1.6	12	mA
I _{ccl}	22	4.4	33	mA
t _{PHL}	14	21	17	ns
t _{PLH}	7	8	9	ns

a. What is the maximum fan-out for a 74xx AND gate driving 74LSxx NAND gates?

$$I_{oh} / I_{ih} = 0.8 \text{ ma} / 20 \text{ ua} = 40$$

$$I_{ol} / I_{il} = 16 \text{ ma} / 0.4 \text{ ma} = 40$$

Must choose the smaller of the two (ie. the worst case). Since both are the same, it doesn't matter and the fan out is 40.

$$\text{Fan Out} = 40$$

b. What is the average power consumption of the

74xx AND gate package?

$$P = (I_{cch} + I_{ccl}) / 2 * V_{CC} = (21 \text{ ma} + 33 \text{ ma}) / 2 * 5 \text{ v} = 135 \text{ mW}$$

c. What is the propagation delay of the circuit shown. Calculate average propagation delay for each gate, and use those to determine delay of complete circuit.

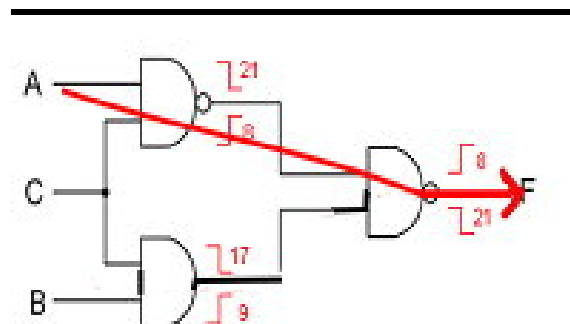
Delay through NAND gates are $(21+8)/2 \text{ ns} = 14.5 \text{ ns}$

Delay through AND gate is $(17+9)/2 \text{ ns} = 13 \text{ ns}$

Total delay Path A-F = $14.5 + 14.5 = 29 \text{ ns}$

Total delay Path B-F = $13 + 14.5 = 27.5 \text{ ns}$

So, worst cast delay is path A-F = 29 ns



Prob 3

Consider text problem 2.22, ie. the “alarm” problem from HW 3. It has 4 inputs (A – D) as described in problem 2.22. Label the output as Z (rather than F(A,B,C,D)).

$$Z = AB' + C'D + AD'$$

- a) Write a VHDL behavioral module called “alarm” with an architecture called “alarm_behav”.

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entity alarm is
    Port ( A, B, C, D : in bit;    -- primary input signals
          Z : out bit );
end alarm;

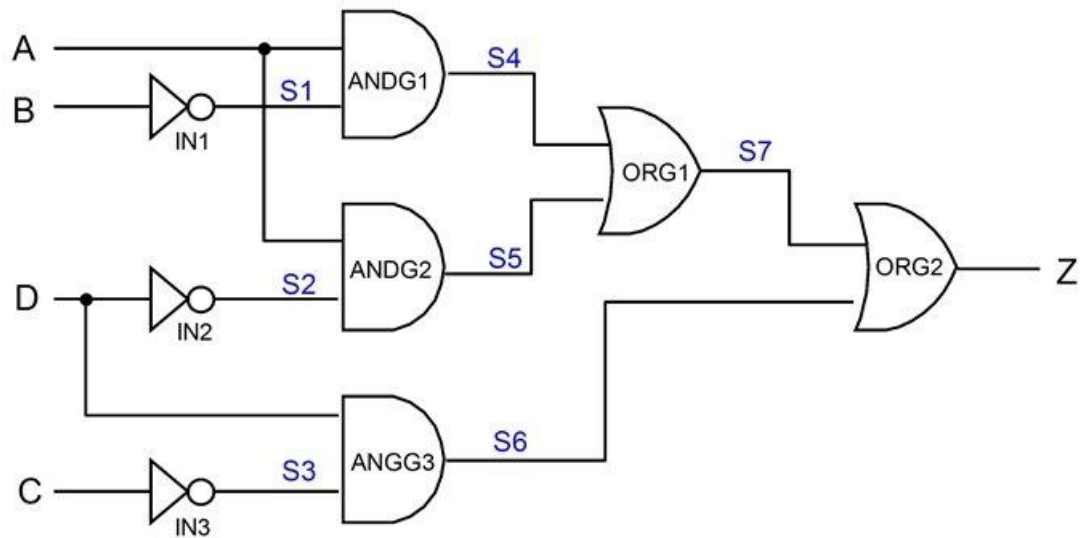
architecture alarm_behav of alarm is
begin
    Z = (A AND (not B)) OR ((not C) AND D) OR (A AND (not D));
end alarm_behav;

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- b) Using AND gates, OR gates, and INVERTERS, rewrite the architecture description as a structural architecture called “alarm_struc”. You can assume components AND2, OR2 and INV have been defined previously, and available for your use.

Note: I meant to assume a component named OR3, not OR2. If you assumed it should have been OR3, that's fine. I wrote the solution though using OR2, utilizing 2 of them to make a 3 input OR gate.

First, draw the circuit labeling all signals and gates:



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architecture alarm_struct of alarm is
    signal S1, S2, S3, S4, S5, S6, S7 : bit;

    component AND2 port ( a, b : in bit;          -- a previously defined 2-input AND gate
                        a_and_b : out bit);

    component OR2 port ( a, b : in bit;          -- a previously defined 2-input OR gate
                       a_or_b : out bit);

    component INV port ( a : in bit;             -- a previously defined INVERTER gate
                       a_inv : out bit);

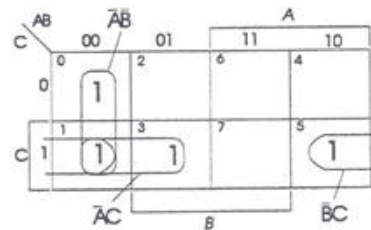
begin
    IN1 : INV port map (B, S1);
    IN2 : INV port map (D, S2);
    IN3 : INV port map (C, S3);
    ANDG1 : AND2 port map (A, S1, S4);
    ANDG2 : AND2 port map (A, S2, S5);
    ANDG3 : AND2 port map (A, S3, S6);
    ORG1 : OR2 port map (S4, S5, S7);
    ORG2 : OR2 port map (S6, S7, Z);
end alarm_struct;

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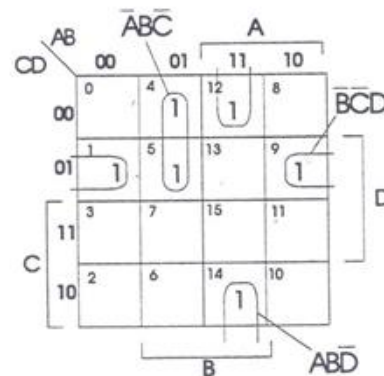
Prob 4 Text Problem 3.1 (a & b)

3.1 Plot the following functions on the Karnaugh map:

(a) $f(A, B, C) = \bar{A}\bar{B} + \bar{B}C + \bar{A}C$



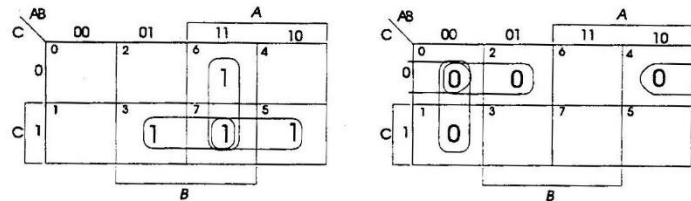
(b) $f(A, B, C, D) = \bar{B}\bar{C}D + \bar{A}B\bar{C} + AB\bar{D}$



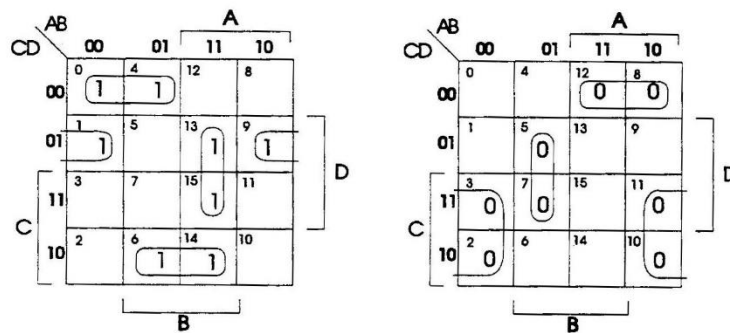
Prob 5. Text Problem 3.2 (a & b)

3.2 Minimize the following functions via the K-map:

$$\begin{aligned} \text{(a)} \quad f(A, B, C) &= \sum m(3, 5, 6, 7) \\ &= AB + BC + AC \\ &= (A + C)(B + C)(A + B) \end{aligned}$$



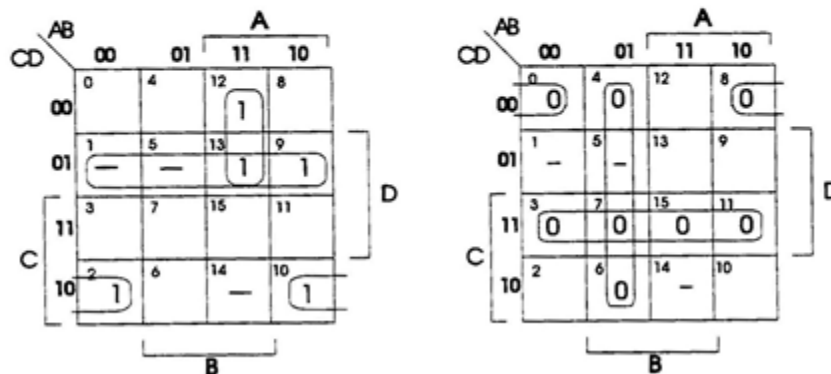
$$\begin{aligned} \text{(b)} \quad f(A, B, C, D) &= \sum m(0, 1, 4, 6, 9, 13, 14, 15) \\ &= \bar{A}\bar{C}\bar{D} + \bar{B}\bar{C}D + ABD + BC\bar{D} \\ &= (\bar{A} + C + D)(A + \bar{B} + \bar{D})(B + \bar{C}) \end{aligned}$$



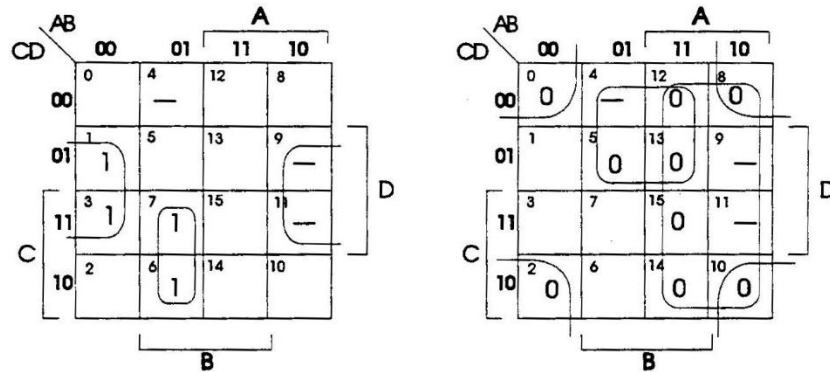
Prob 6. Text Problem 3.3 (a & b)

3.3 Minimize the following functions containing don't cares via the K-map:

$$\begin{aligned} \text{(a)} \quad f(A, B, C, D) &= \sum m(2, 9, 10, 12, 13) + d(1, 5, 14) \\ &= \bar{C}D + \bar{B}C\bar{D} + AB\bar{C} \\ &= \bar{C}D + \bar{B}C\bar{D} + AB\bar{D} \\ &= (\bar{C} + \bar{D})(A + \bar{B})(B + C + D) \end{aligned}$$



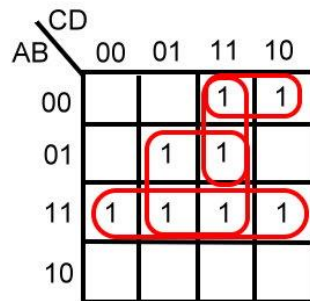
$$\begin{aligned}
 (b) \quad f(A, B, C, D) &= \sum m(1, 3, 6, 7) + d(4, 9, 11) \\
 &= \bar{B}D + \bar{A}BC \\
 &= (\bar{A})(\bar{B} + C)(B + D)
 \end{aligned}$$



Prob 7. Text Problem 3.12 (a only)

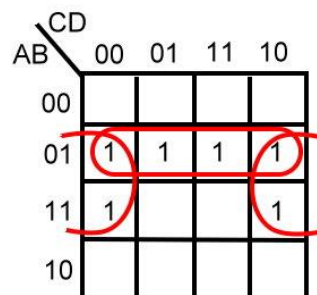
List all prime implicants for the indicated functions:

$$f_a = AB + BD + A'B'C$$



Prime Implicants
 $\{AB\}$
 $\{BD\}$
 $\{A'B'C\}$
 $\{A'CD\}$

$$f_b = A'B + BD'$$



Prime Implicants
 $\{A'B\}$
 $\{BD'\}$

For function f_a can you also list all the “Implicants”? Can you list all the “Essential Prime Implicants”? Hint: There are 19 implicants in all. 3 of them are essential prime implicants.