GENERAL INFORMATION FOR COEN/ELEN 921c

Introductory Logic Design

Fall 2018

office hour; on class, mail

Boolean functions and their minimization. Analysis and design of combinational circuits, adders, multipliers, multiplexers, decoders. Switching characteristics, noise margin, propagation delay. Bussing. Memory elements: latches and flip-flops; timing; registers; counters. Programmable logic: ROM, PLD, and FPGA. HDL in conjunction with FPGAs.

Instructor: Carl Fussell, Email: cafussell@scu.edu

Text: Nelson, Nagle, et.al., Digital Logic Circuit Analysis & Design

Class: Tuesday 1710 - 1900 O'Connor 106

Grading: Generally curved with the following weights

Quizes (2)	20%	(10% ea) → announced.
Midterm	35%	→ half
Final	45%	

Note: Homework is assigned but not turned in. Solutions are provided for the student to check the accuracy of their work. Students need to do the problems to do well on quizzes and exams.

Makeup exams will be given **ONLY** if notice is given to the instructor prior to exam day.

Honor Code: All students taking courses in the School of Engineering agree, individually and collectively, that they will neither give nor receive unauthorized aid in examinations or other course work that is to be used by the instructor as a basis of grading.

Expectations: Basic electrical knowledge: power, voltage, current, ohms law.

References:

Wakerly, John, Digital Design Principles and Practices, Prentice Hall
Roth, Charles, Fundamentals of Logic Design, West
Katz, Randy, Contemporary Logic Design, Benjamin Cummings

Google Search of **"Combinational Logic Design"** will yield web references.

Of course, there are many other references beyond these.

Postings and Class Materials:

http://camino.scu.edu

Tentative Syllabus for COEN/ELEN 921c

Introductory Logic Design

no lab

1. Introduction — 1.1-1.4

   - Read chapter 0
   - Number systems, radices, arithmetic, number representations

2. Boolean Algebra — 2.1-2.3

   - Boolean Operators
   - Postulates and Theorems
   - Switching Functions, Truth tables, Canonical form
   - Logic Devices (SSI)

3. Analysis and Synthesis of Logic Circuits — 2.4-2.7

   basic gate.

   - AND, OR, NOT, NAND, NOR, XOR, Tri-State
   - Two level circuits, DeMorgan's theorem
   - HDL intro

   → start to design circuit
   make it smaller is good

4. Nasty realities

   frequently.

   - Propagation delays
   - Electrical Characteristics — Handout
   - Switching Characteristics/Noise margins — 2.4.2

5. Simplification of Switching Functions — 3.1-3.9

   - K-Maps, Sum-of-Products / Product-of-Sums
   - Incompletely specified functions
   - Hazards
   - Exclusive OR functions
   - Quine-McCluskey

6. Modular Combinational Logic Elements (MSI) — 4.1-4.7, 4.9.2

   - Decoders, Encoders, Multiplexers, Demultiplexers
   - Tri-State, Bussing

6. Programmable Logic Devices — 5.1-5.5

   - Gate arrays, PROMs, PLDs, PLAs, PALs, FPGAs

7. Sequential Circuits and Devices (SSI)

   - Sequential Model, Combinational vs. Sequential, State tables and diagrams — 6.1-6.2
   - Latches and Flip Flops: D, RS, JK, T — 6.3-6.4
   - Timing: setup, hold times, edge trigger, master/slave
   - Other devices: One-shots, timers — 6.5-6.7

8. Modular Sequential Logic (MSI)

   - Registers, Shift Registers, Counters, Mod-N Counters — 7.1-7.4