# Test Document
# TIPS CHIP
# 1.0

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# 작업사항

- 측정 시나리오 적기 - doc
- **메인 시나리오 적기**
  - 동작하는 기능들은 독립적인 시나리오로 동작한다고 하면 부가적인 시나리오로 작성할 것
- 대표성 있는 것을 측정
- Random test 도 같이 추가할 것
  - Such as input signal change
- 문서 버전 컨트롤! – rivision history

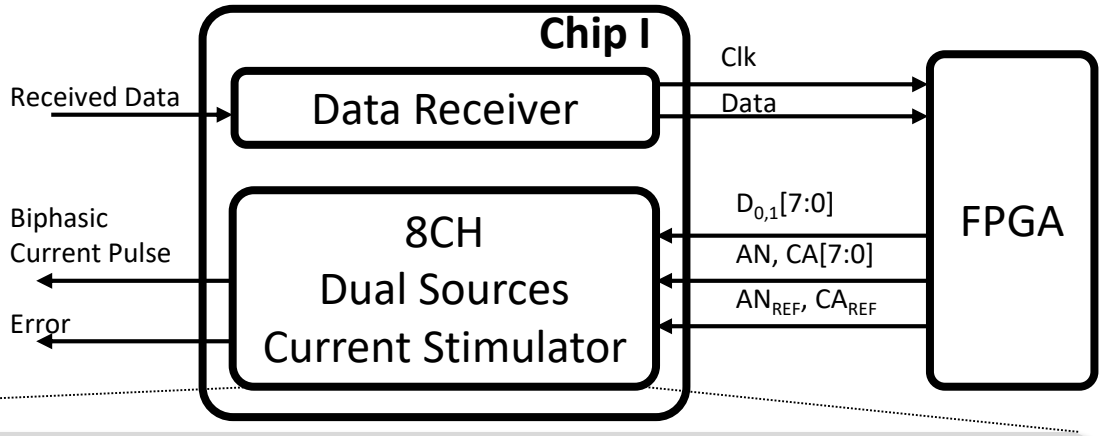
# Push Pull Stimulator version 1.0
# (P-P Stimulator 1.0)

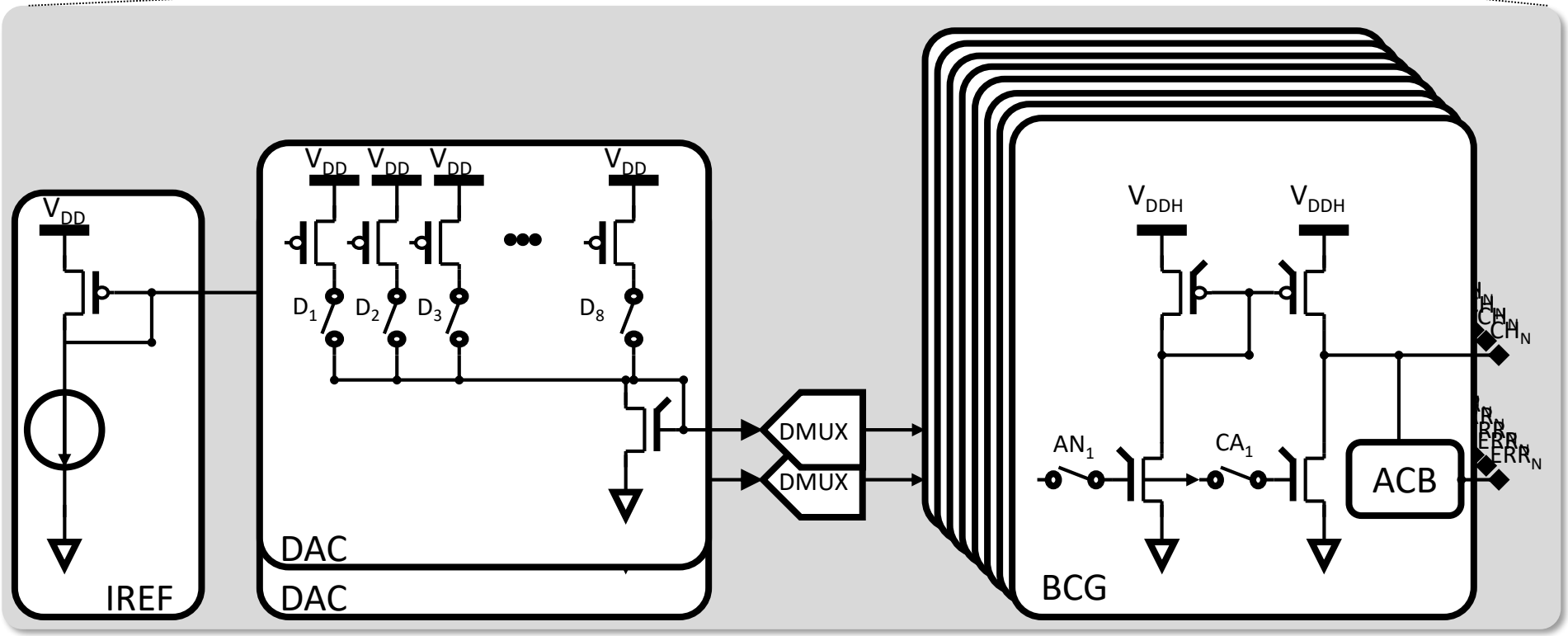
# Push Pull Stimulator version 1.0 (P-P Stimulator 1.0)

| Chip I | Description |
|---|---|
| Block | Current stimulator with dual current supplies and a data receiver |
| Supply Voltage | $V_{DD}$ = 1.8 V, $V_{BIAS}$ = 5 V, 10 V, $V_{DDH}$ = 20 V |
| # of Channels | 8 |
| # of Current Source | 2 |
| Current Level | 2.55 mA (8-bit) |
| Continuous Interleaved Sampling (CIS) | Yes |
| Simultaneous Analog Stimulation (SAS) | Yes |
| Active Charge balancer (ACB) | Yes |

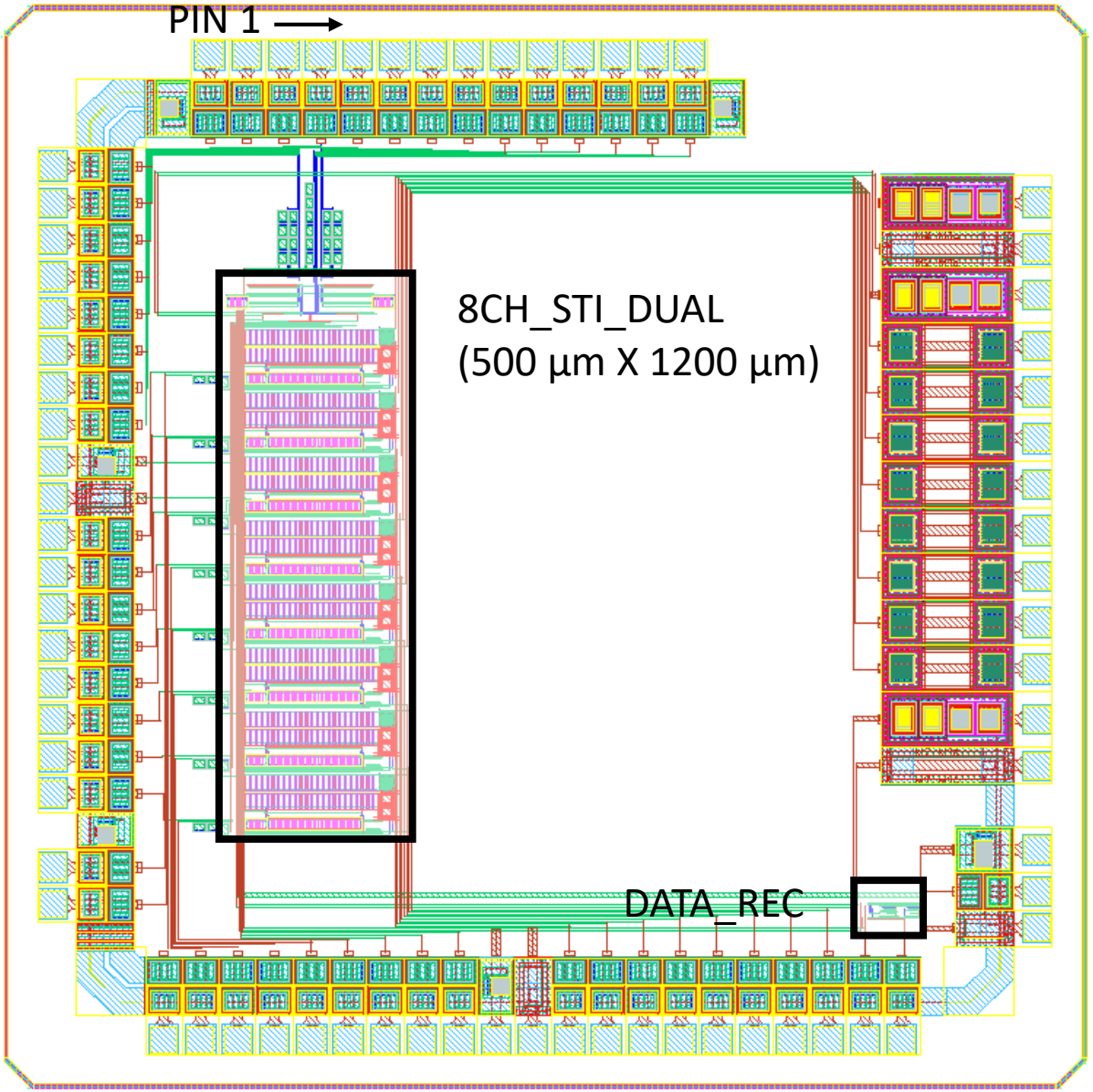
# P-P Stimulator 1.0

- Reference Generator (IREF)
  - 기준 전류원 생성 (2 μA)
- Digital to Analog Converter (DAC)
  - 디지털신호로 조절하여 자극 전류원을 생성 (8-bit level)
- 1:8 Analog Demultiplexer (DMUX)
  - DAC에서 생성된 신호를 8채널 BCG 중 하나로 선택하여 전달함.
- Biphasic Current Generator (BCG)
  - biphasic current pulse 로 변환
- Active Charge Balancer (ACB)
  - 디지털신호로 Cathodic 자극 전하량와 Anodic 자극 전하량을 비교하여 알려줌



# PAD Allocation




Size: 2350 µm (W) X 2350 µm (H)

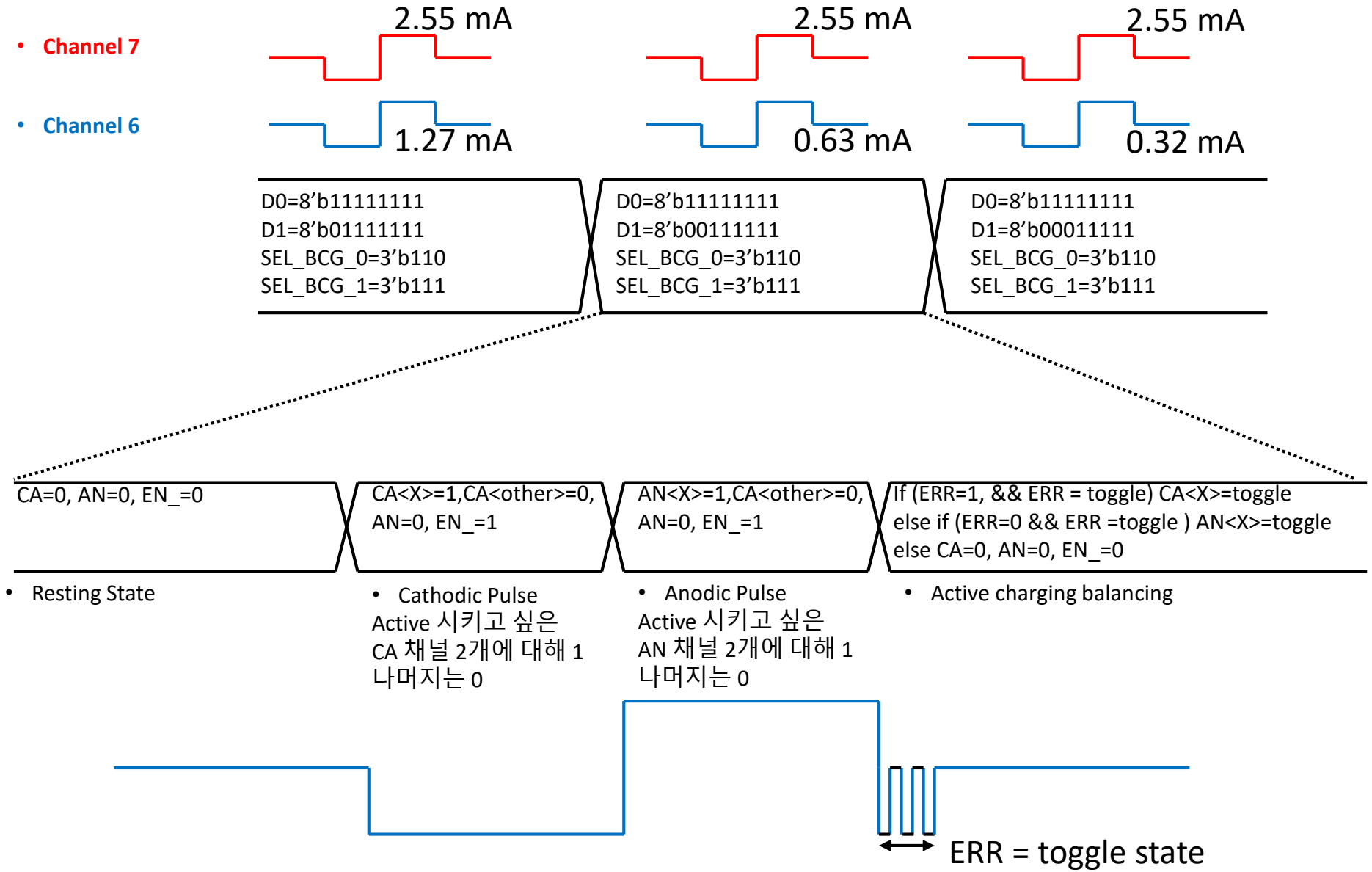
# PAD Description

| # | Type | NAME | Description |
|---|---|---|---|
| 29 | Analog | DR_IN | Inductive link에서 들어오는 data 입력 |
| 31 | Analog | DATA | 출력하는 Data |
| 32 | Analog | CLK | 출력하는 Clock |
| 43 | Analog | VB0P526 | $V_B$ = 0.526 V |
| 44 | Analog | VB0P9 | $V_B$ = 0.9 V |
| 18-25 | Analog | CH<7:0> | 7번에서 0번 BCG 채널 자극파형출력 |
| 45 | Digital | EN_ | 자극파형이 chip에서 생성될 때, 0 resting = 1, Active charge balancer 부분의 comparator 입력부분 전압 초기화 |
| 1-8 | Digital | D1<0:7> | D1 DAC의 level을 결정 ('1'= ON) |
| 9-11 | Digital | SEL_BCG_0<0:2> | D0에서 생성된 전류를 BCG로 복사해줄 채널을 선택 (111 = 7번채널 선택, D0와 D1은 다른 값을 가져야 함) |
| 12-14 | Digital | SEL_BCG_1<0:2> | D1에서 생성된 전류를 BCG로 복사해줄 채널을 선택 (111 = 7번채널 선택, D0와 D1은 다른 값을 가져야 함) |
| 33-40 | Digital | ERR<7:0> | 7번부터 0번까지의 BCG가 생성한 자극파형의 charge balancing을 측정하기위해 비교값을 출력하는 디지털 신호 |
| 46-53 | Digital | CA<7:0> | Cathodic Current pulse 생성시 1 |
| 54- 61 | Digital | AN<7:0> | Anodic Current pulse 생성시 1 |
| 64-71 | Digital | D0<0:7> | D0 DAC의 level을 결정 ('1'= ON) |
| 15,17,26 | Power | VDD20P0 | $V_{DD}$ = 20 V |
| 16,27,30,41,62 | Power | VSS | $V_{SS}$ = 0 V |
| 28 | Power | VDD5P0 | $V_{DD}$ = 5V |
| 42,63 | Power | VDD1P8 | $V_{DD}$ = 1.8 V |



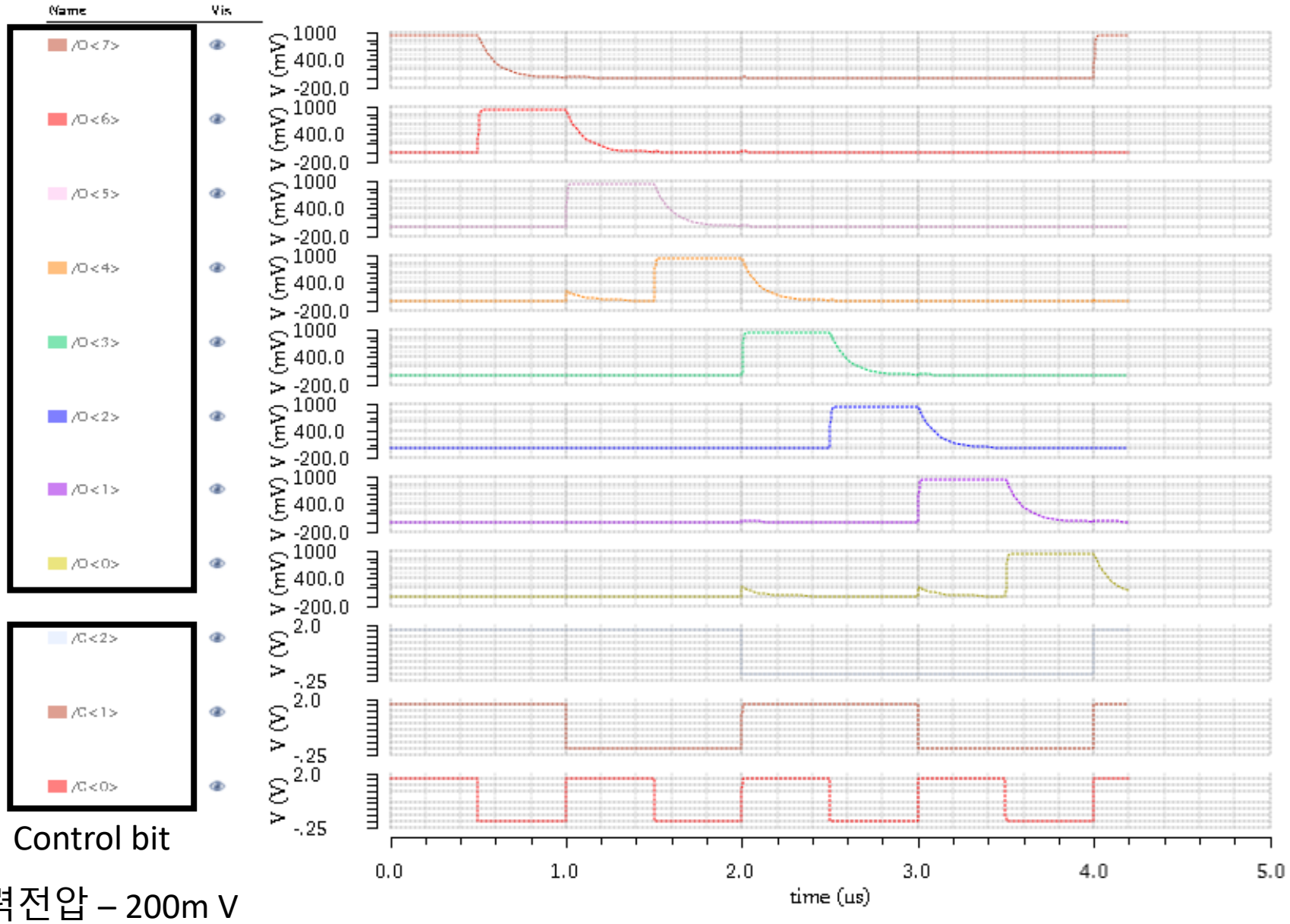
- BCG: biphasic current generator

# Input Signal Flow



# DMUX_1T8 – Simulation Result Load R=100k C=1pF

출력 신호

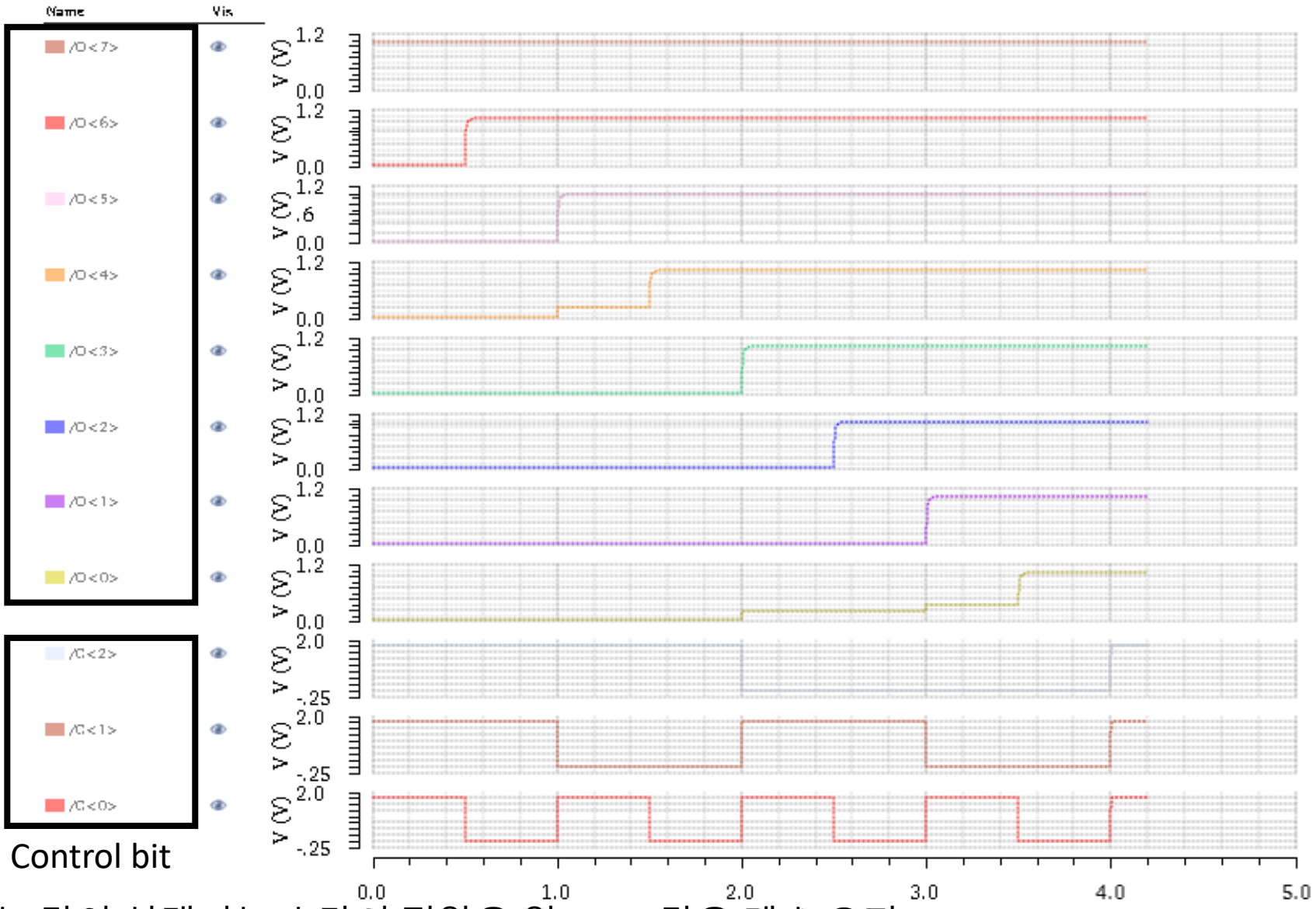



Control bit

입력전압 – 200m V

# DMUX_1T8 – Simulation Result R=10G C=1pF

출력 신호

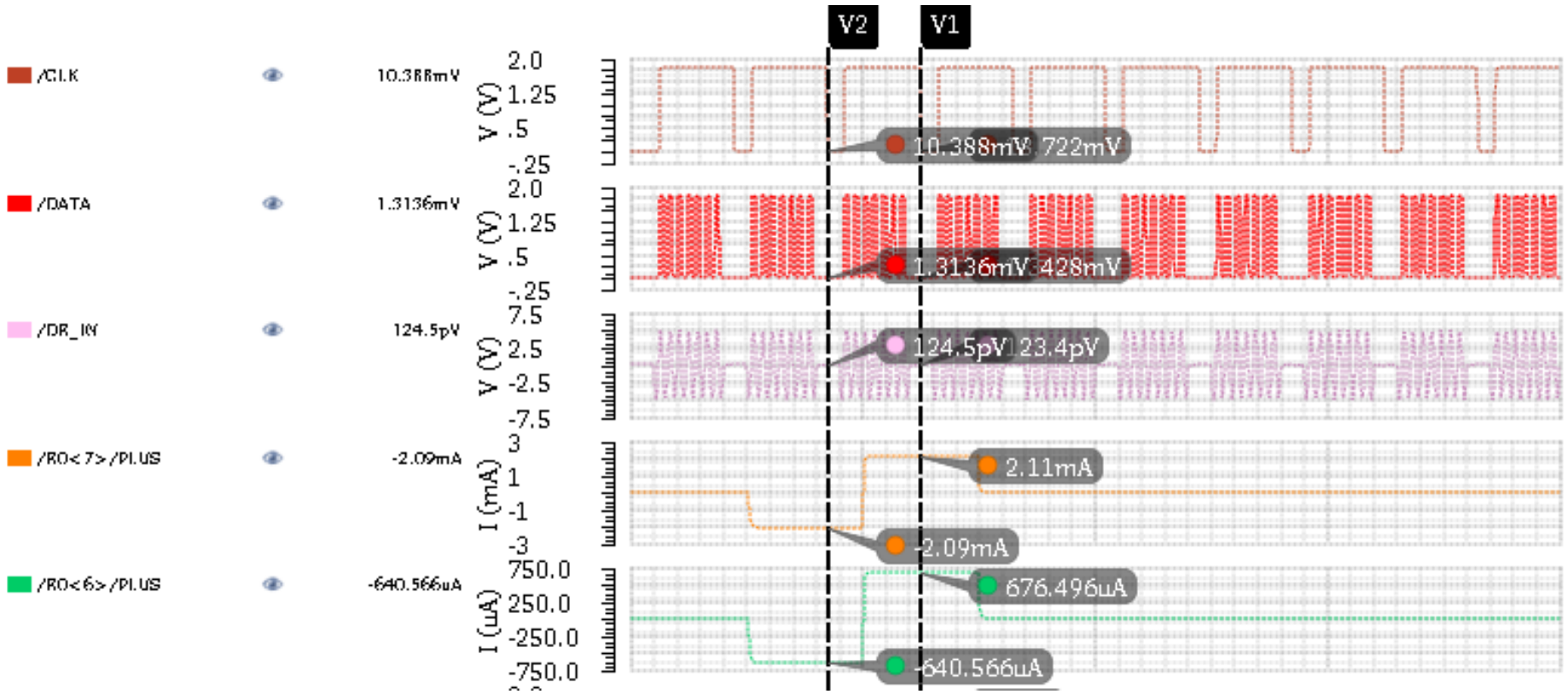



Control bit

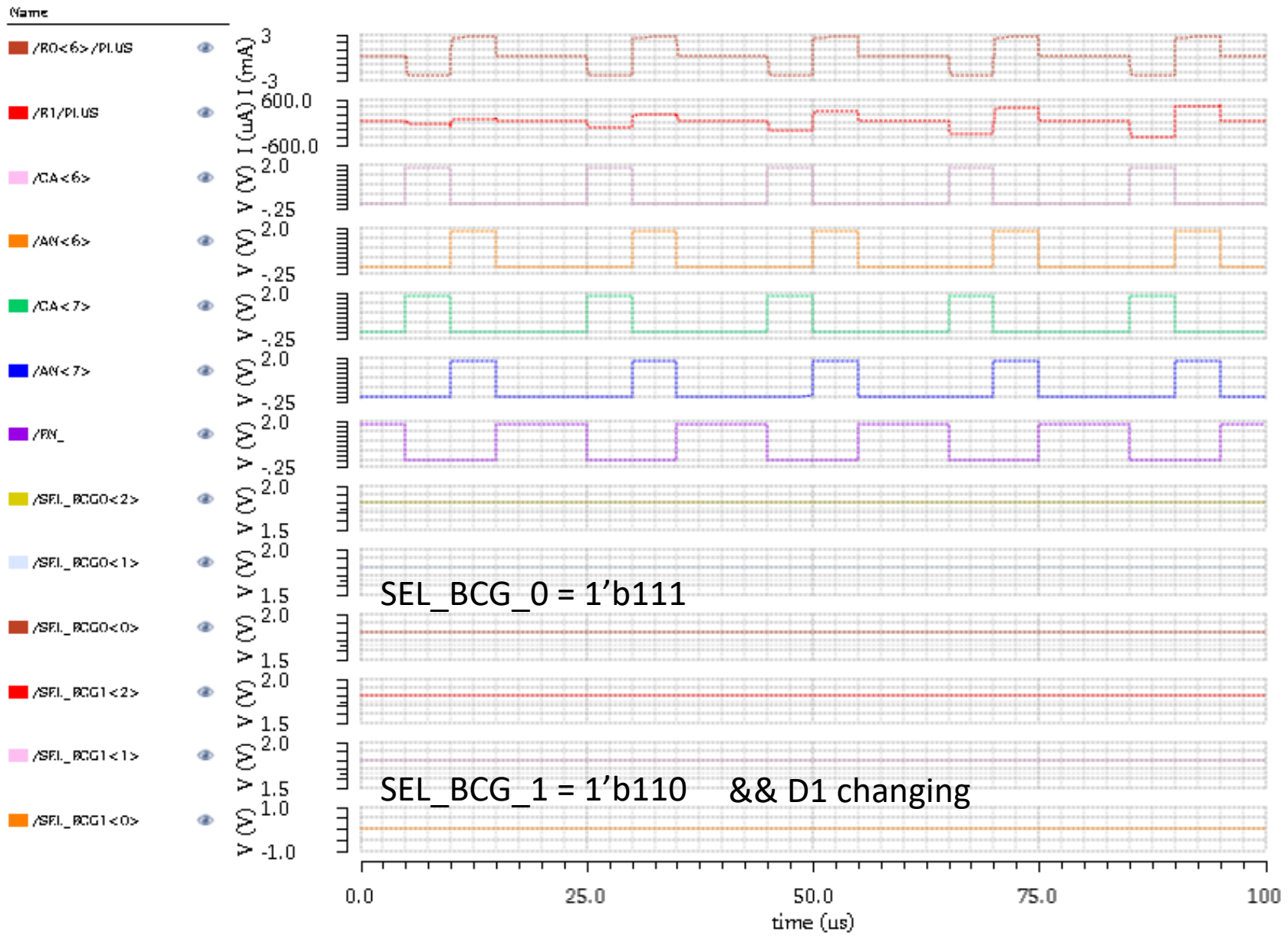
실재로는 값이 선택되는 순간의 전압을 읽고, 그 값을 계속 유지

# BCG_DUAL – Simulation Result 0

- Simultaneous Stimulation with Clock and Data Recovery

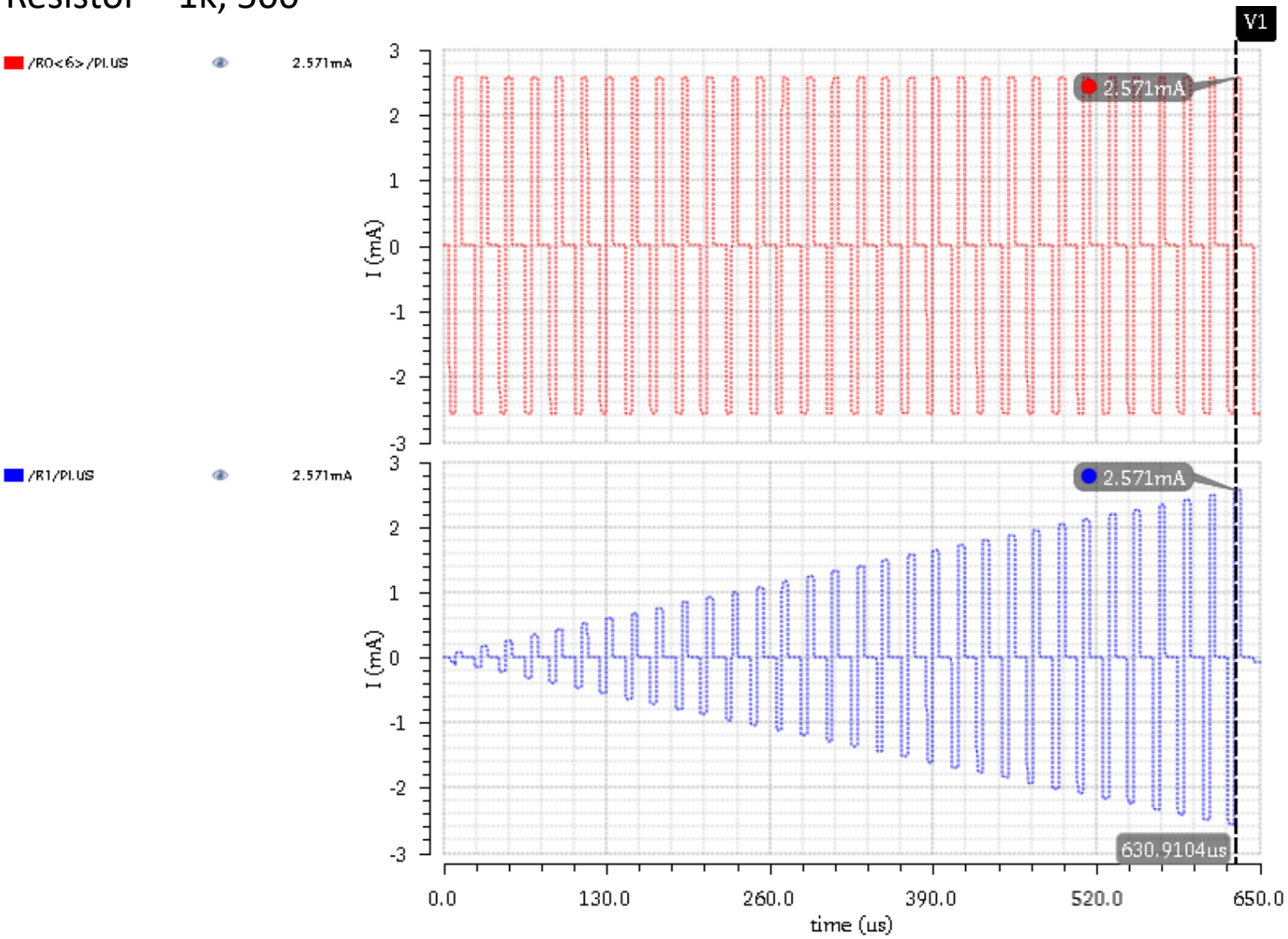


# BCG_DUAL – Simulation Result 0



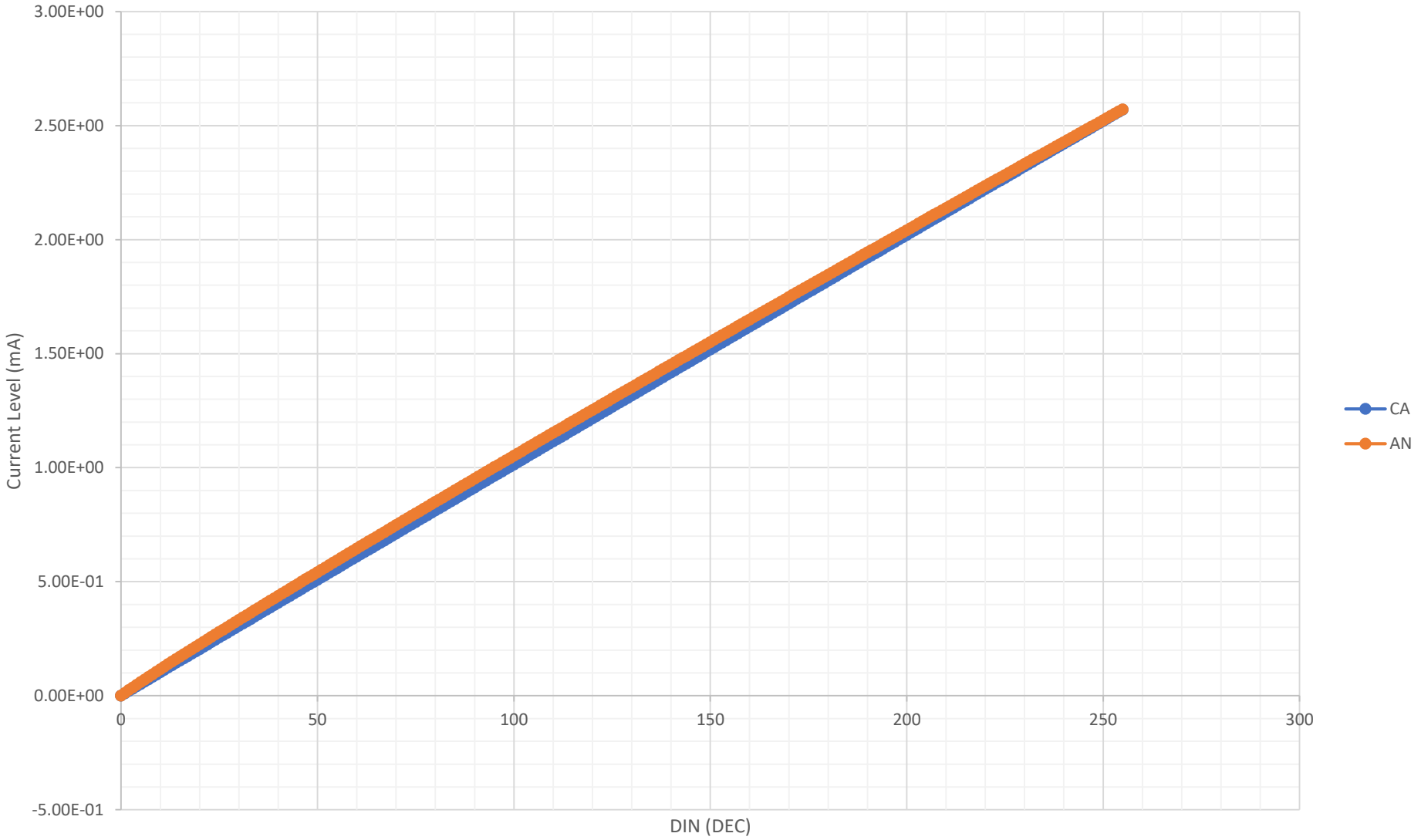
# BCG_DUAL – Simulation Result 1

- Simultaneous Stimulation
  - Resistor – 1k, 500



# BCG_DUAL – Simulation Result 2

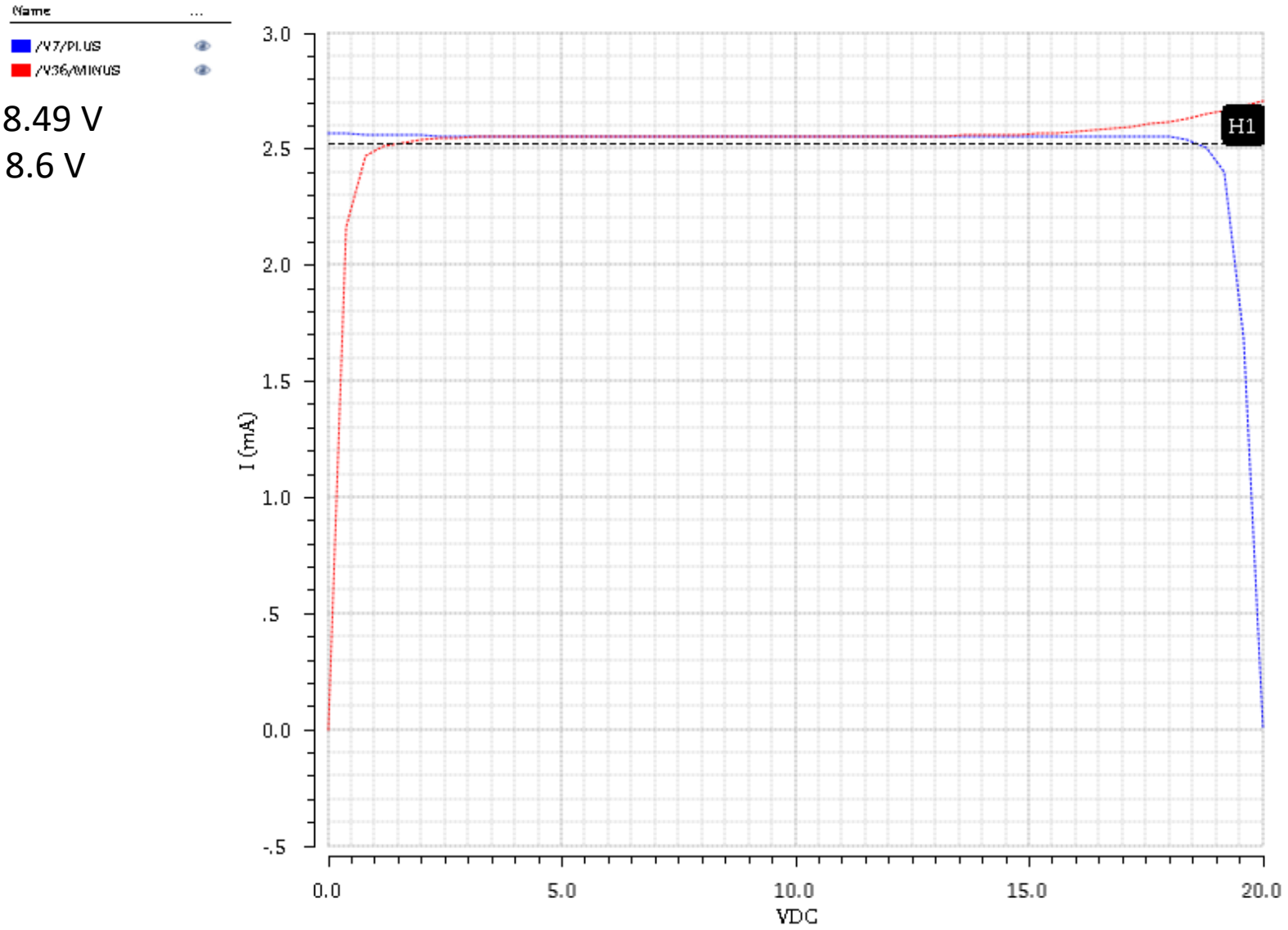
- Current Level



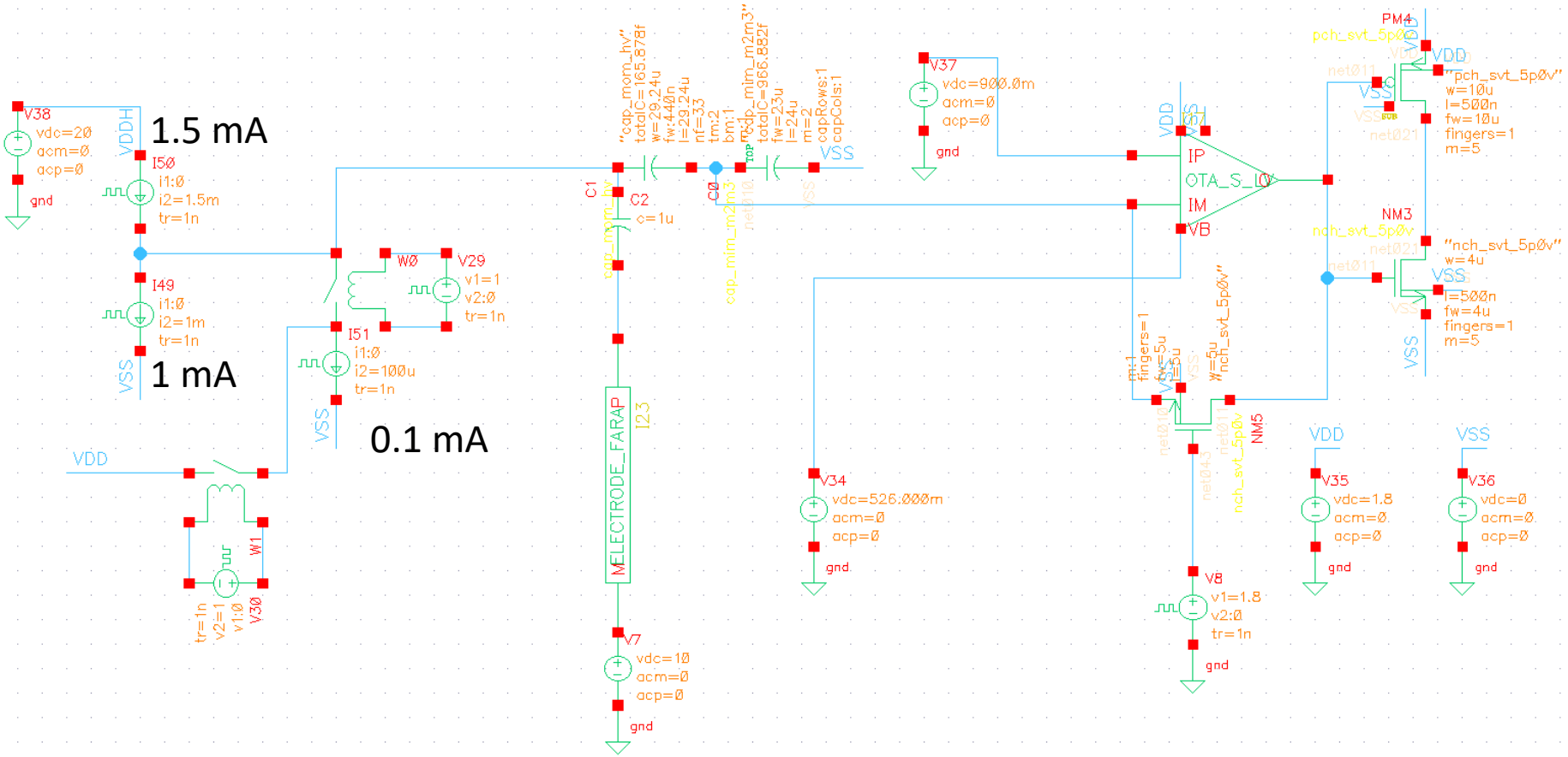
# BCG_DUAL – Simulation Result 3

- Voltage Compliance ($V_{COMP}$)

$V_{COMP, CA}$ - 8.49 V
$V_{COMP, AN}$ - 8.6 V

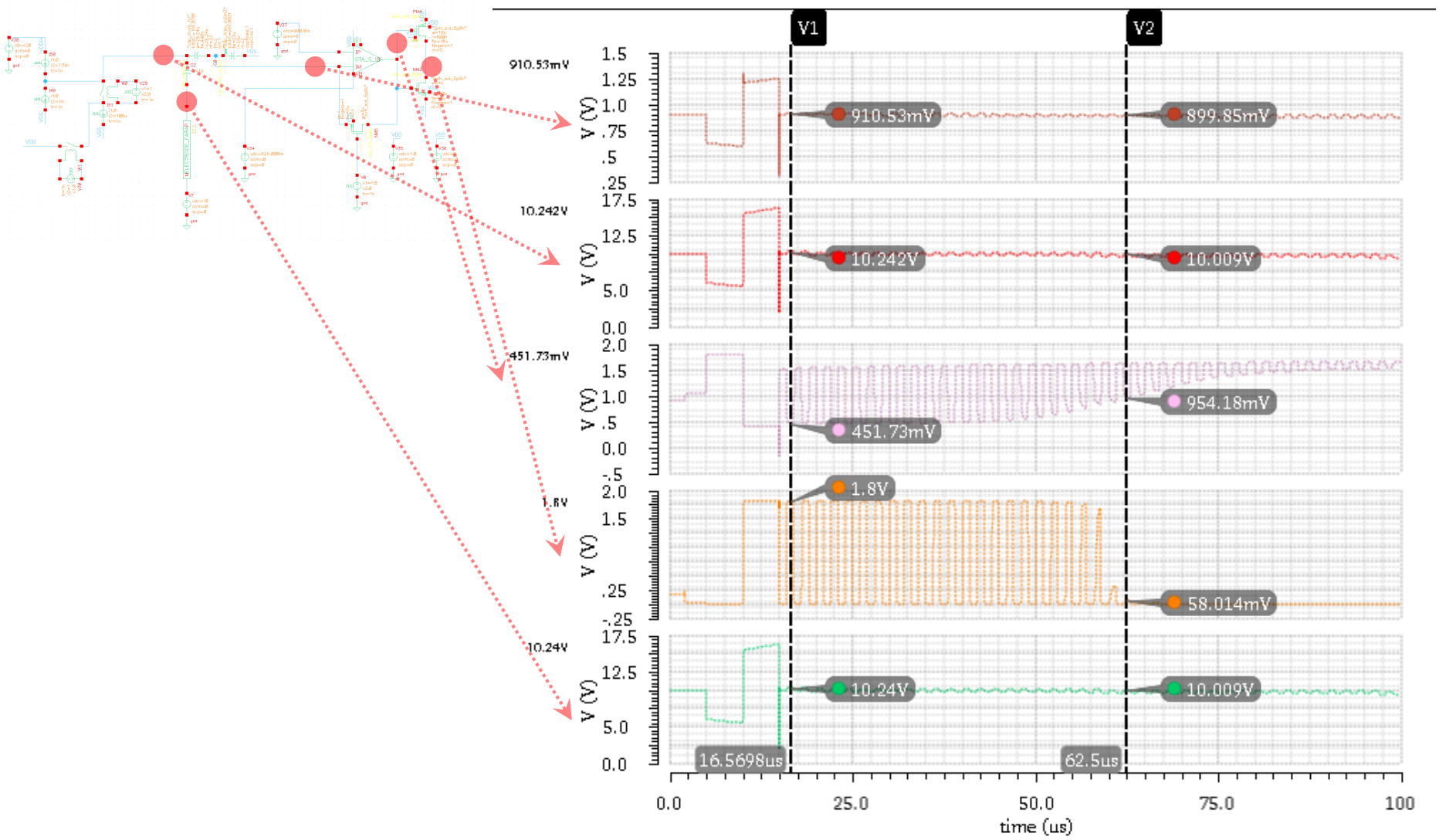


# BCG_DUAL – Test Bench Error



# BCG_DUAL – Simulation Result 1

- Biphasic Current Pulse with Error Output
  - 10.24 V → 10.009 V



# Measurement lists

- Current Level - 255 level
- Voltage Compliance
- Simultaneous Analog Stimulation (SAS)
  - Change R1: R2 ratio

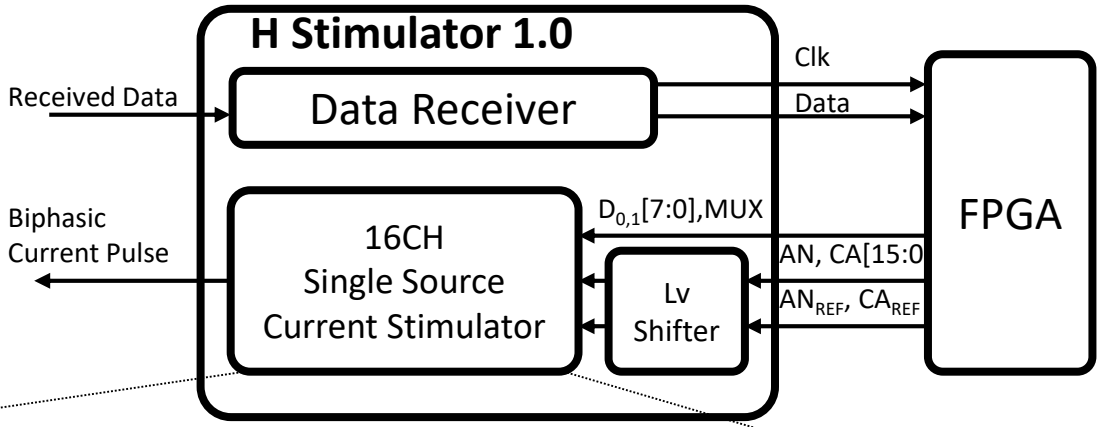
# H-bridge Stimulator version 1.0 (H Stimulator 1.0)

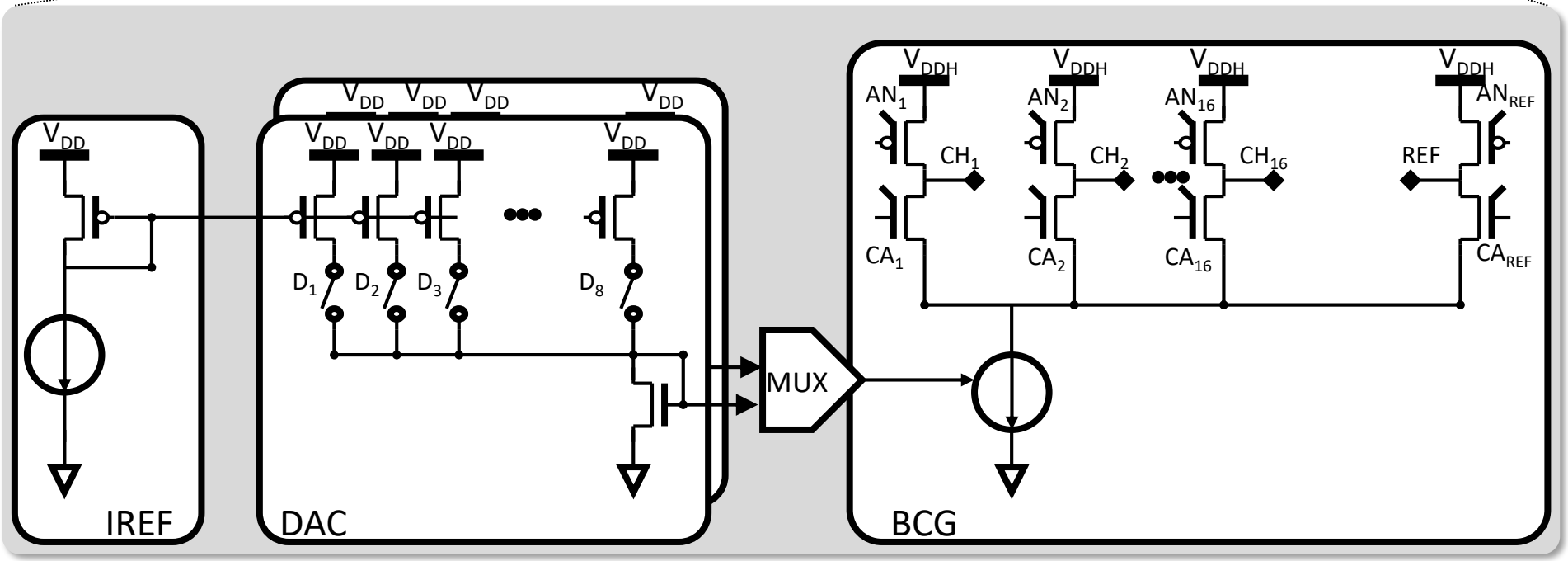
# Spec.

| Chip II | Description |
|---|---|
| Block | Current stimulator with a single current supply and a data receiver |
| Supply Voltage | $V_{DD}$ = 1.8 V, $V_{BIAS}$ = 5 V, $V_{DDH}$ = 10 V |
| # of Channels | 16 |
| # of Current Source | 2 |
| Current Level | 2.55 mA (8-bit) |
| Continuous Interleaved Sampling (CIS) | Yes |
| Simultaneous Analog Stimulation (SAS) | No |
| Active Charge balancer (ACB) | No (passive charge balancer included) |

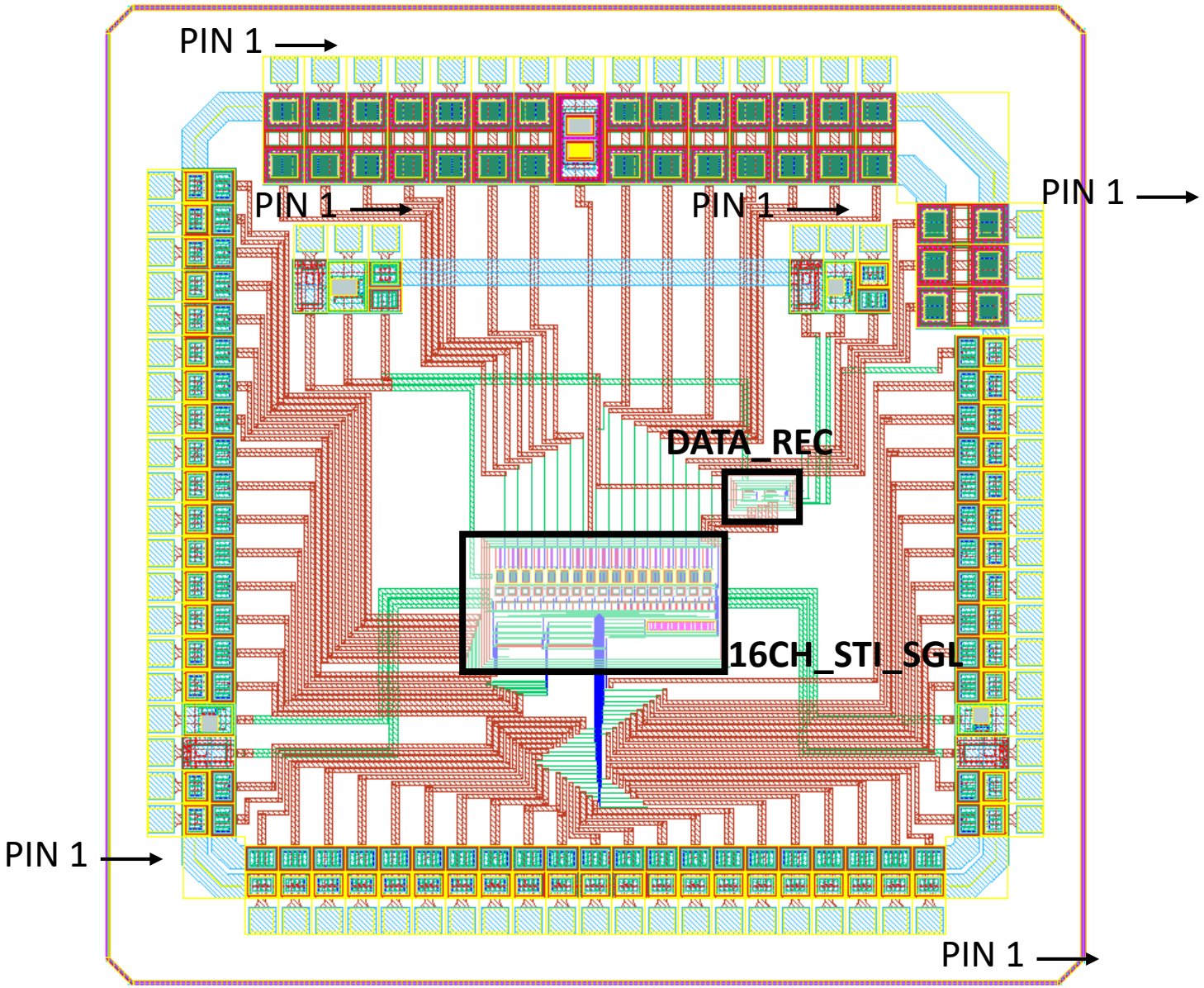
# H Stimulator 1.0 Block Diagram

- Reference Generator (IREF)
  - Reference current generator (2 μA)
- Digital to Analog Converter (DAC)
  - Digitally controllable current generation (8-bit level)
- 2:1 Analog Multiplexer (MUX)
- Biphasic Current Generator (BCG)
  - Conversion of DC current into biphasic current pulse



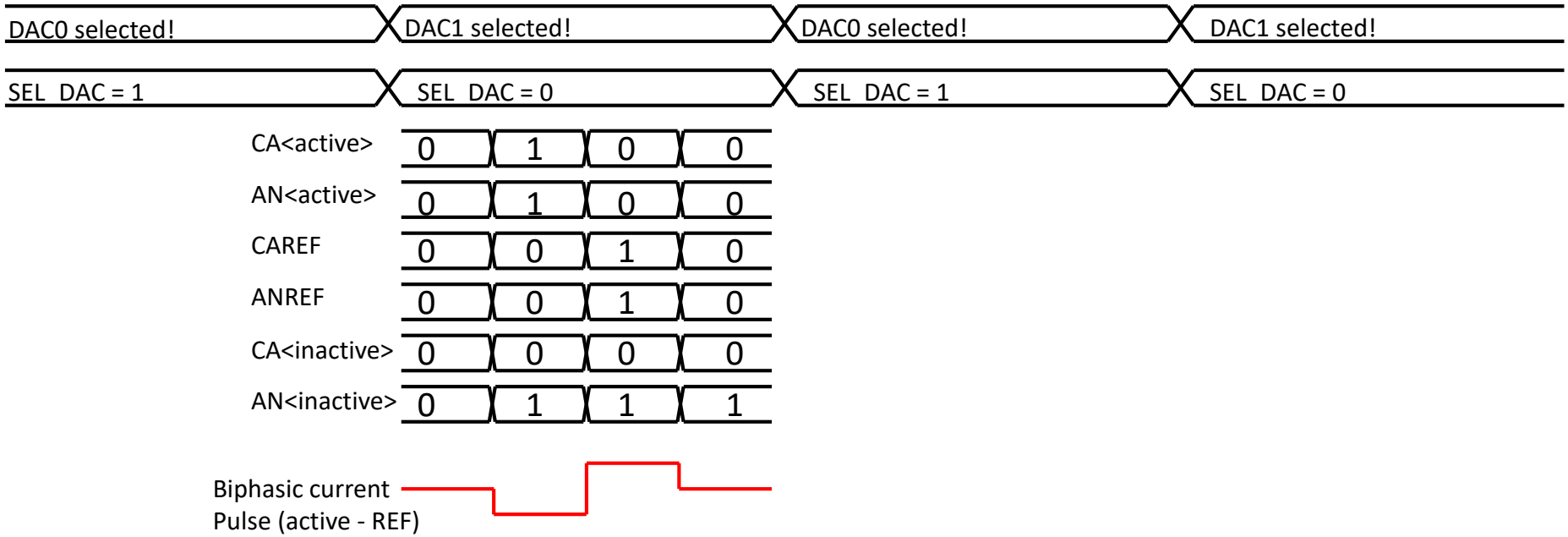
# PAD Allocation



# PAD Allocation

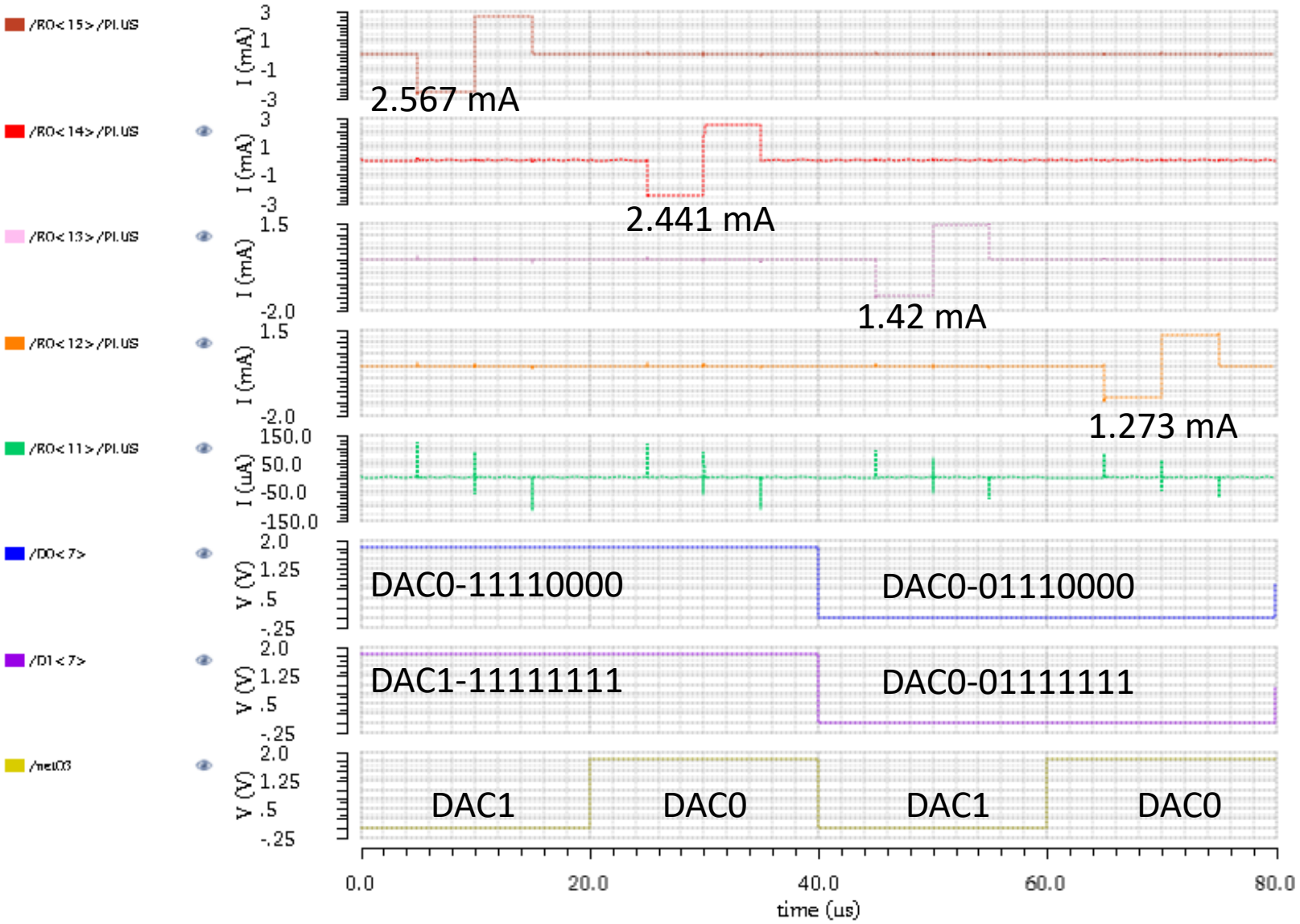
| # | Type | NAME | Description |
|---|---|---|---|
| 20 | In | SEL_DAC | • 2개의 DAC중 하나를 선택함. 자극파형생성시 SEL_DAC 에 따라 DAC0,1 중 하나를 선택하여 자극파형의 크기를 결정함. (1àDAC0, 0à DAC1) |
| 77 | In | IN | • Data receiver의 입력단 |
| 21-55 | In | CAREF, CA<15:0> | • 20 페이지 참조, H bridge 아랫쪽 스위치 NMOS 이기 때문에 1=ON, 0=OFF,<br>• 핀번호 (이름) - 21(REF), 23(<15>), 25(<14>), 27(<13>), 29(<12>), 33(<11>), 35(<10>), 37(<9>), 39(<8>), 41(<7>), 43(<6>), 45(<5>), 47(<4>), 49(<3>), 51(<2>), 53(<1>), 55(<0>) |
| 22-56 | In | ANREF, AN<15:0> | • 20 페이지 참조, H bridge 위쪽 스위치 PMOS 이기 때문에 1=OFF, 0=ON,<br>• 핀번호 (이름) - 22(REF), 24(<15>), 26(<14>), 28(<13>), 32(<12>), 34(<11>), 36(<10>), 38(<9>), 40(<8>), 42(<7>), 44(<6>), 46(<5>), 48(<4>), 50(<3>), 52(<2>), 54(<1>), 56(<0>) |
| 59-66 | In | D1<7:0> | • DAC1 의 자극파형 크기를 결정 ( 10 µA 간격, 2.55 mA) |
| 67-74 | In | D0<7:0> | • DAC0 의 자극파형 크기를 결정 ( 10 µA 간격, 2.55 mA) |
| 18 | Out | REF | • Stimulator Reference 자극파형 출력 |
| 19 | Out | Data | • Data receiver 에서 Data out |
| 80 | Out | CLK | • Data receiver 에서 Clock out |
| 1-7,9-17 | Out | CH<0:15> | • Stimulator Channel 자극파형 출력 |
| 8 | Power | VDDH | • 10 V power supply |
| 76 | Power | VDD5P0 | • 5 V power supply |
| 30,58,79 | Power | VDD | • 1.8 V power supply |
| 31,57,75,78 | Power | VSS | • 0 V power supply |

# Input Signal Flow



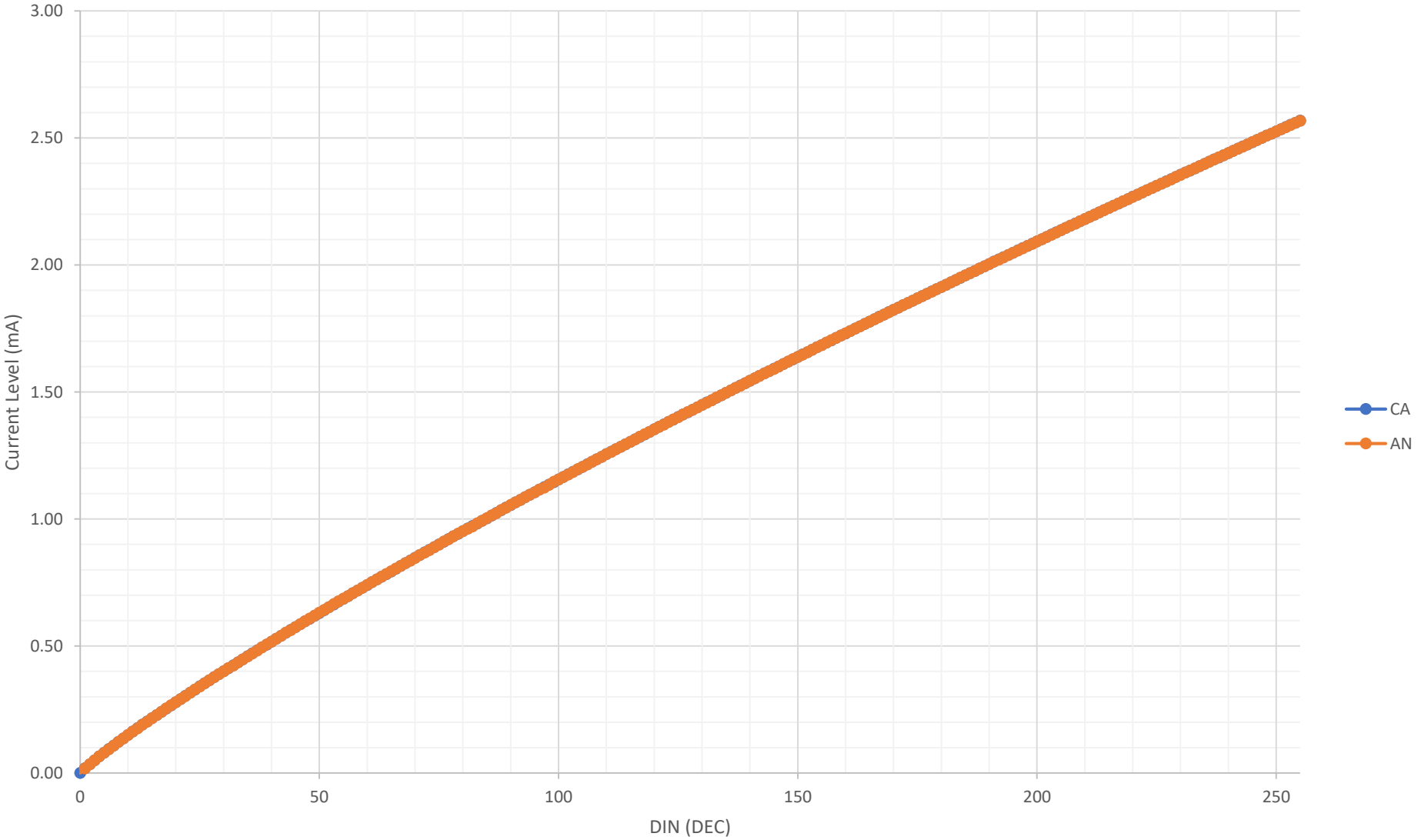
# 16CH_STI_SGL – Simulation Result 1

- CIS Stimulation



# 16CH_STI_SGL – Simulation Result 2

- Current Level



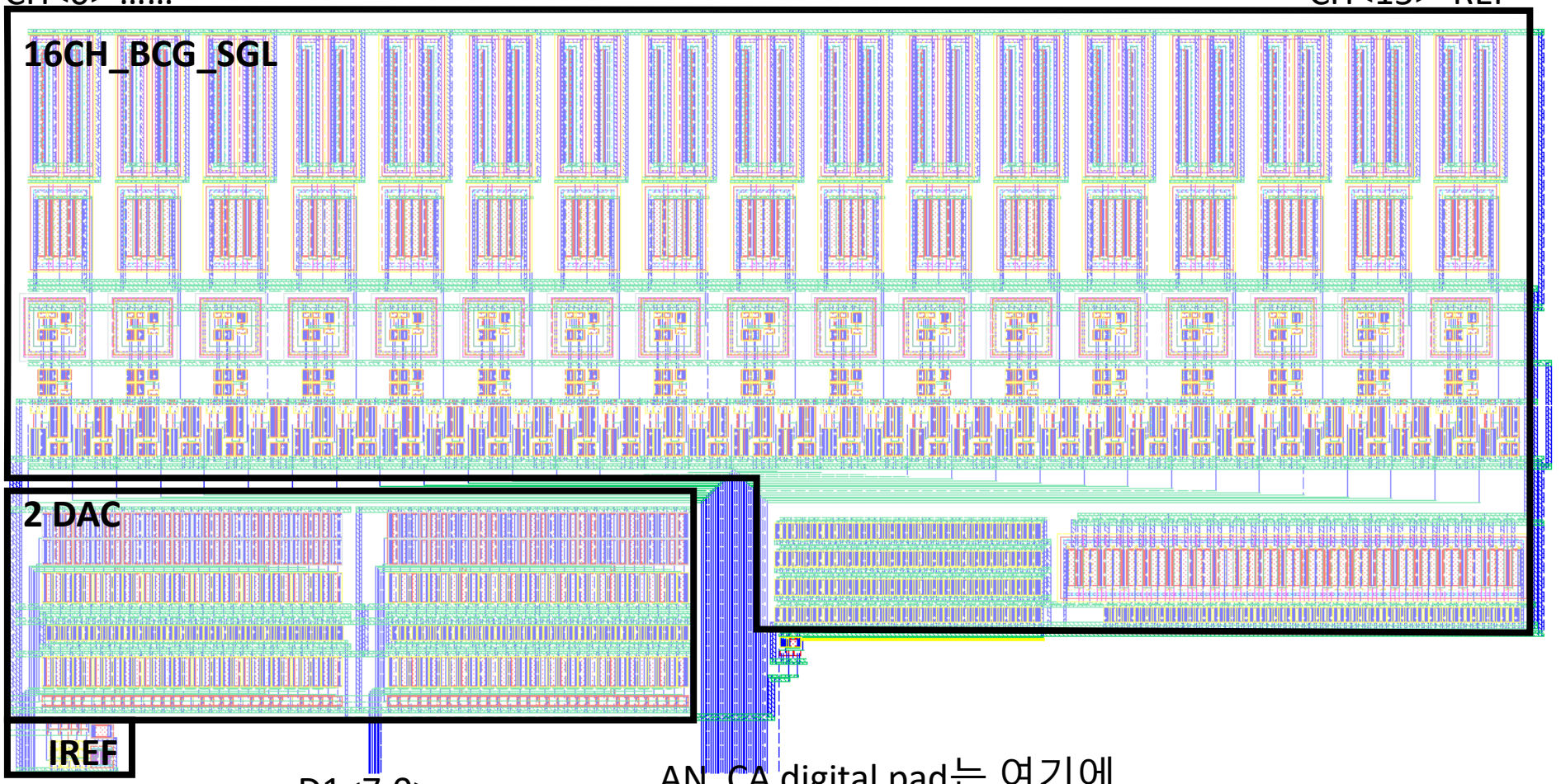
# 16CH_STI_SGL – Layout

540 µm (W) X 260 µm (H)

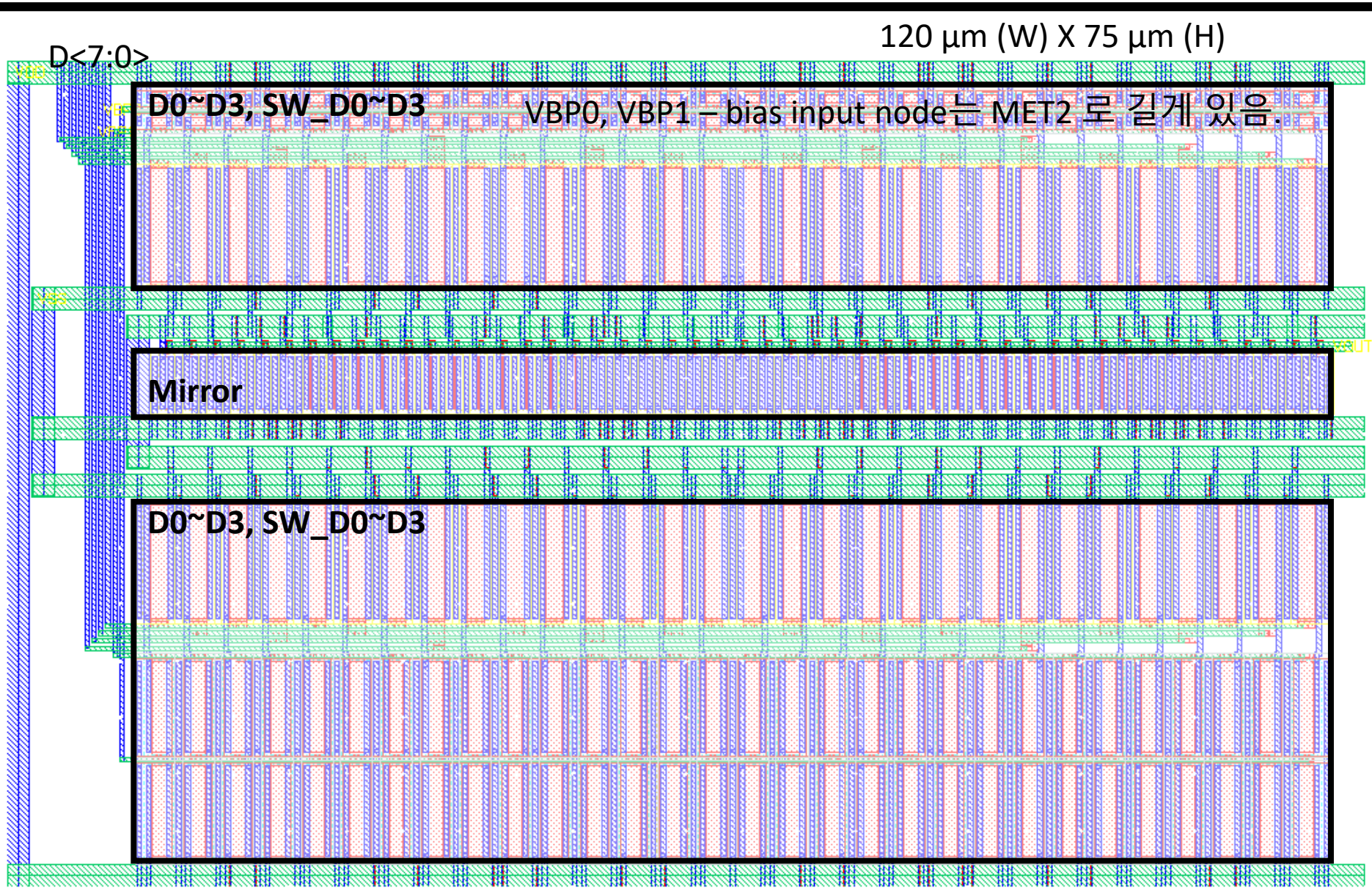
자극파형 출력패드는 위쪽라인에 있음.

CH<0> ……

CH<15> REF



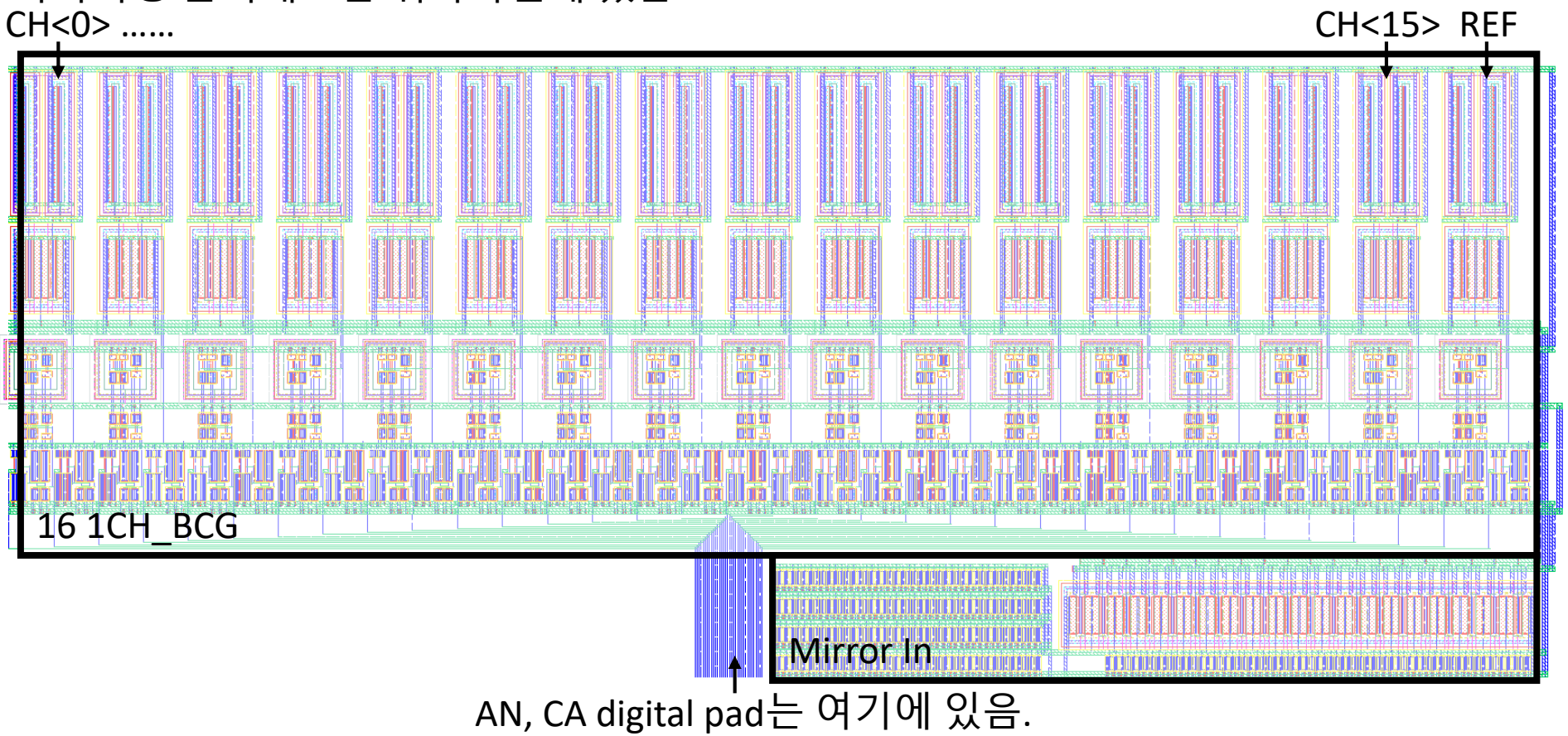
# DAC -Layout


120 μm (W) X 75 μm (H)
D<7:0>
D0~D3, SW_D0~D3
VBP0, VBP1 – bias input node는 MET2 로 길게 있음.
Mirror
D0~D3, SW_D0~D3

# 16CH_BCG - Layout

540 µm (W) X 220 µm (H)

자극파형 출력패드는 위쪽라인에 있음.



# Measurement List

- Current Level - 255 level
- Voltage Compliance