Altera Quartus II를 이용한 설계 구현

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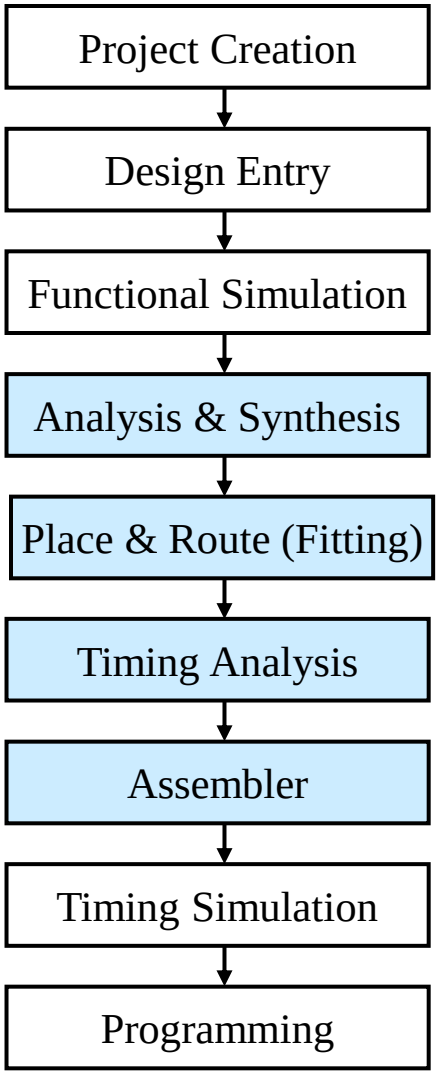
Quartus II 설계 흐름

Front End(합성)
Back End(P&R)
모두 수행

full compile (합성+P&R)
후에 실제 **Gate delay** 정보 산출



functional
RTL 시뮬레이션

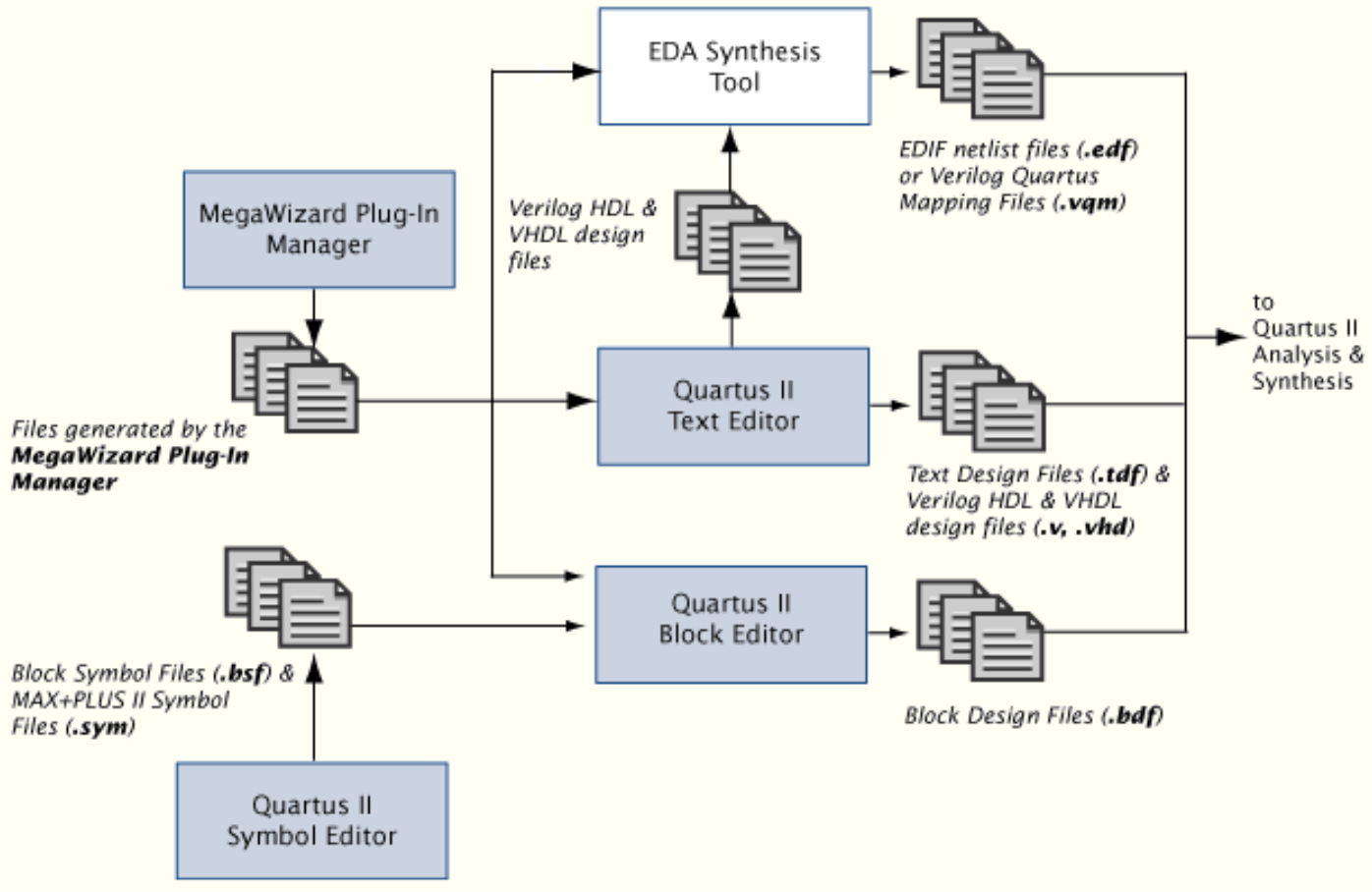
Gate 의 **delay** 는
고려 없이
function 만 검증

Quartus II Compiler modules

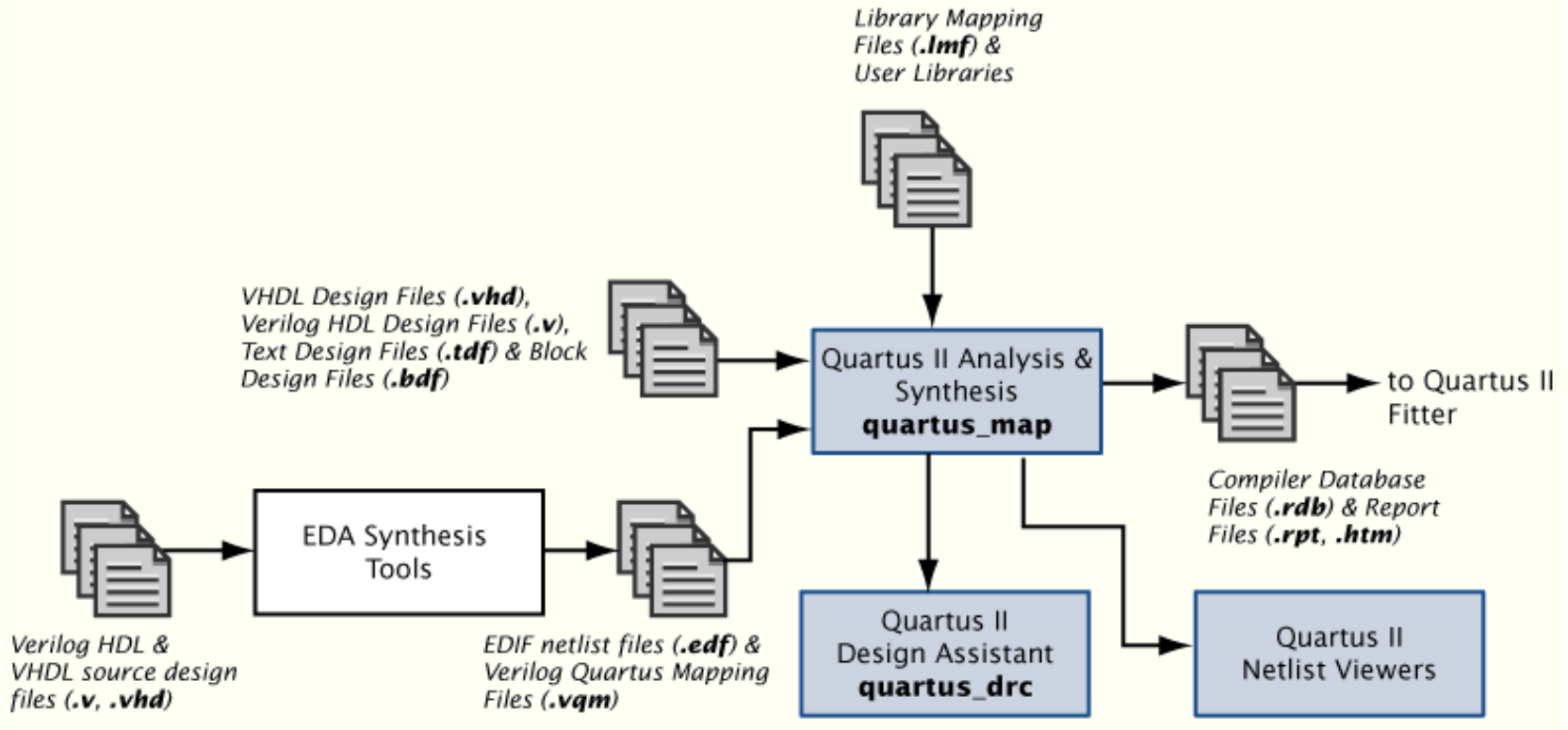
Gate level
시뮬레이션

Gate 의 실제**delay** 를
고려하여 실제 동작이
FPGA 에서 동작가능한지를
검증

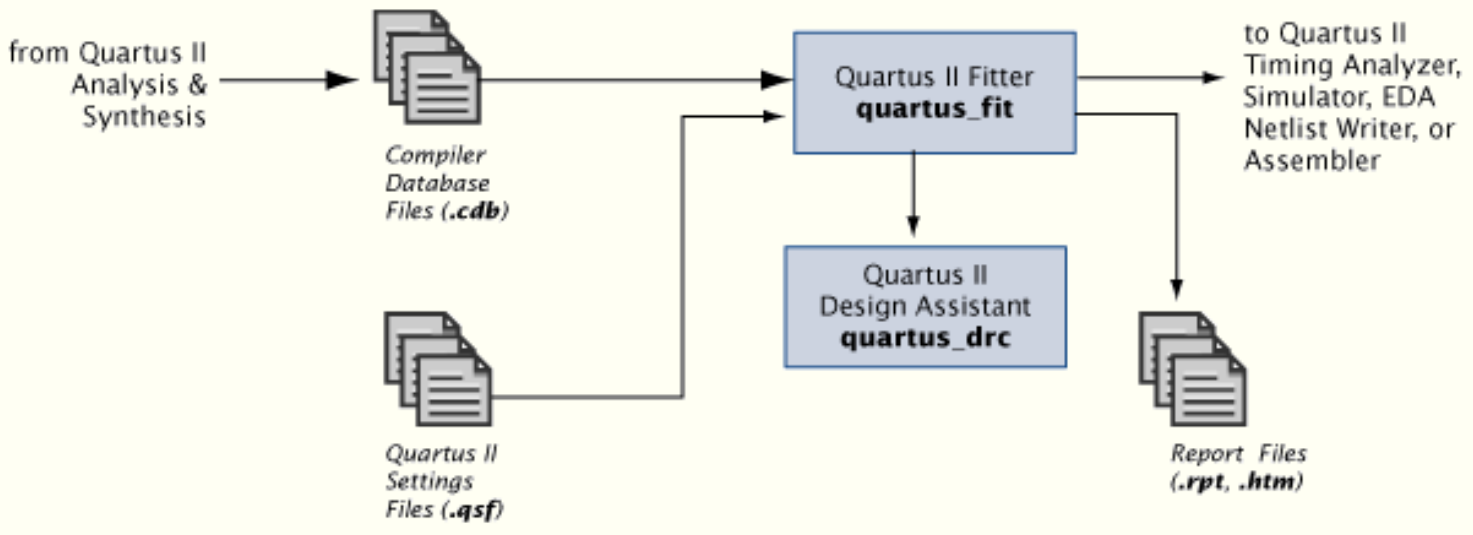
Quartus II 설계입력



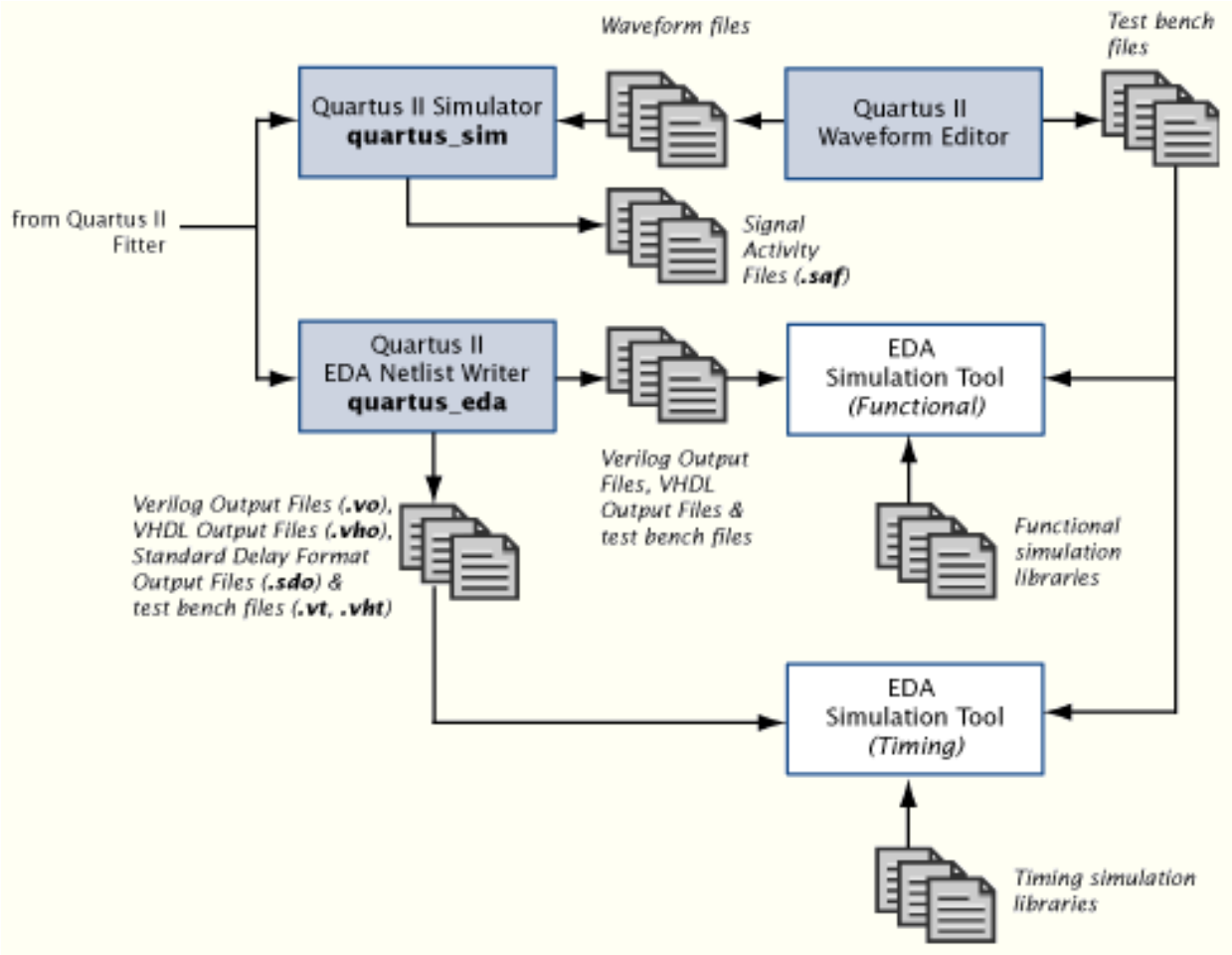
Quartus II 설계합성



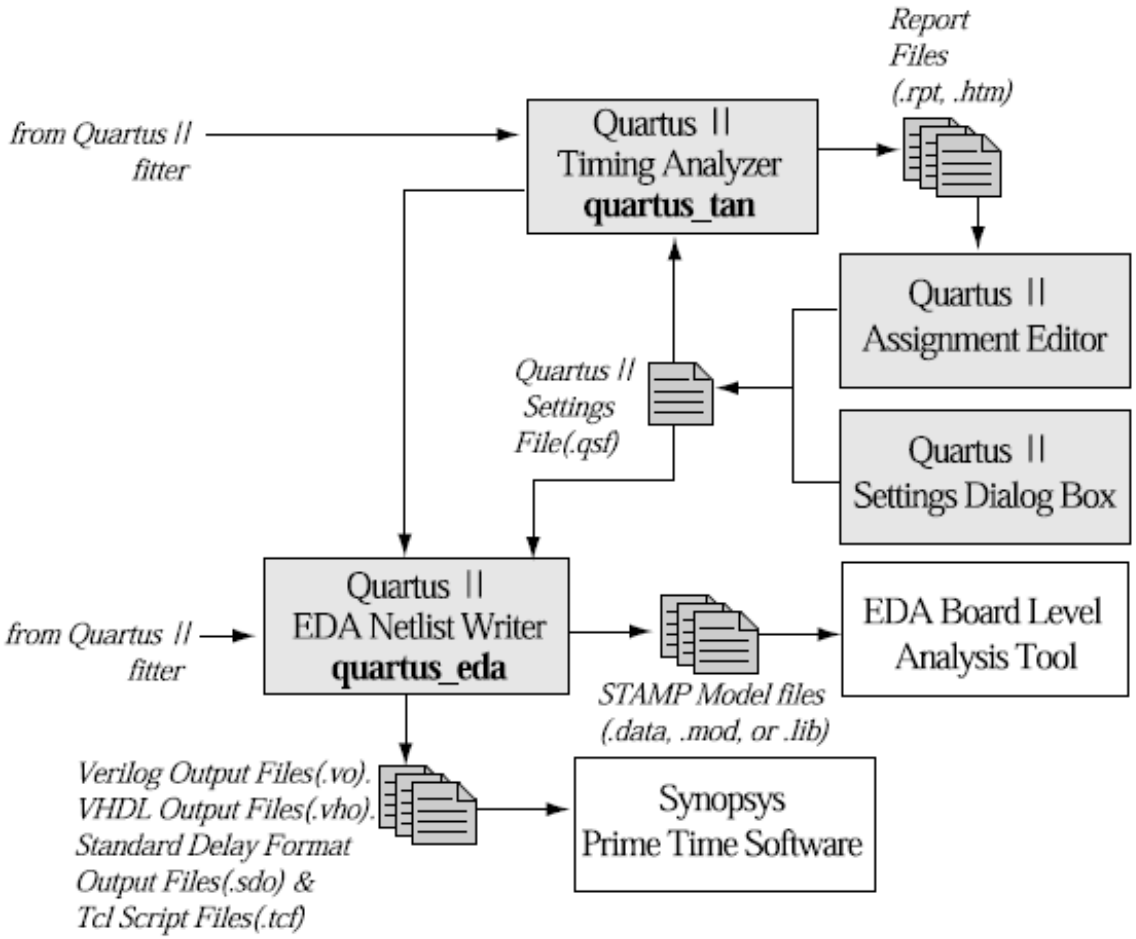
Quartus II Place & Route



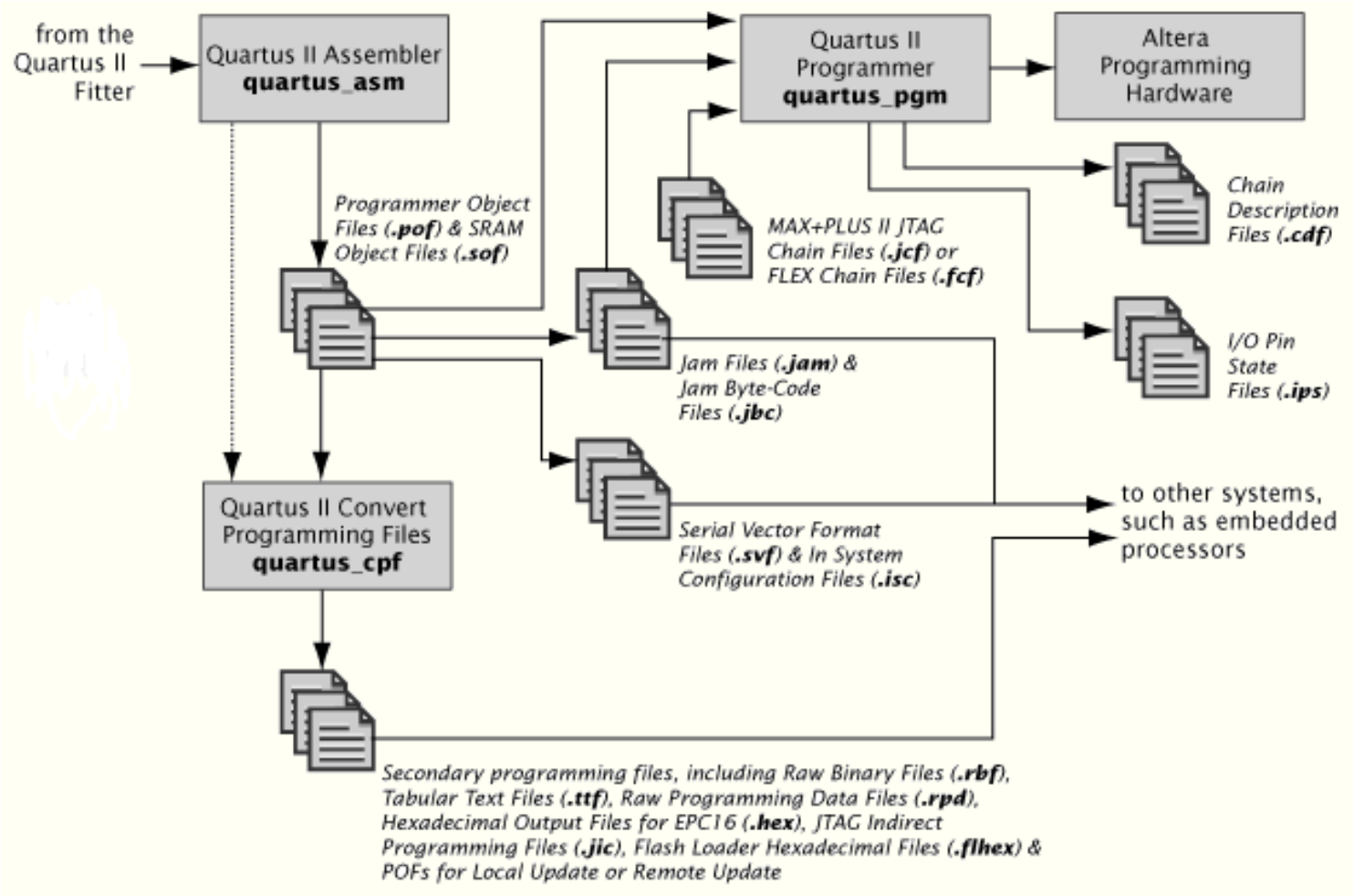
Quartus II 시뮬레이션



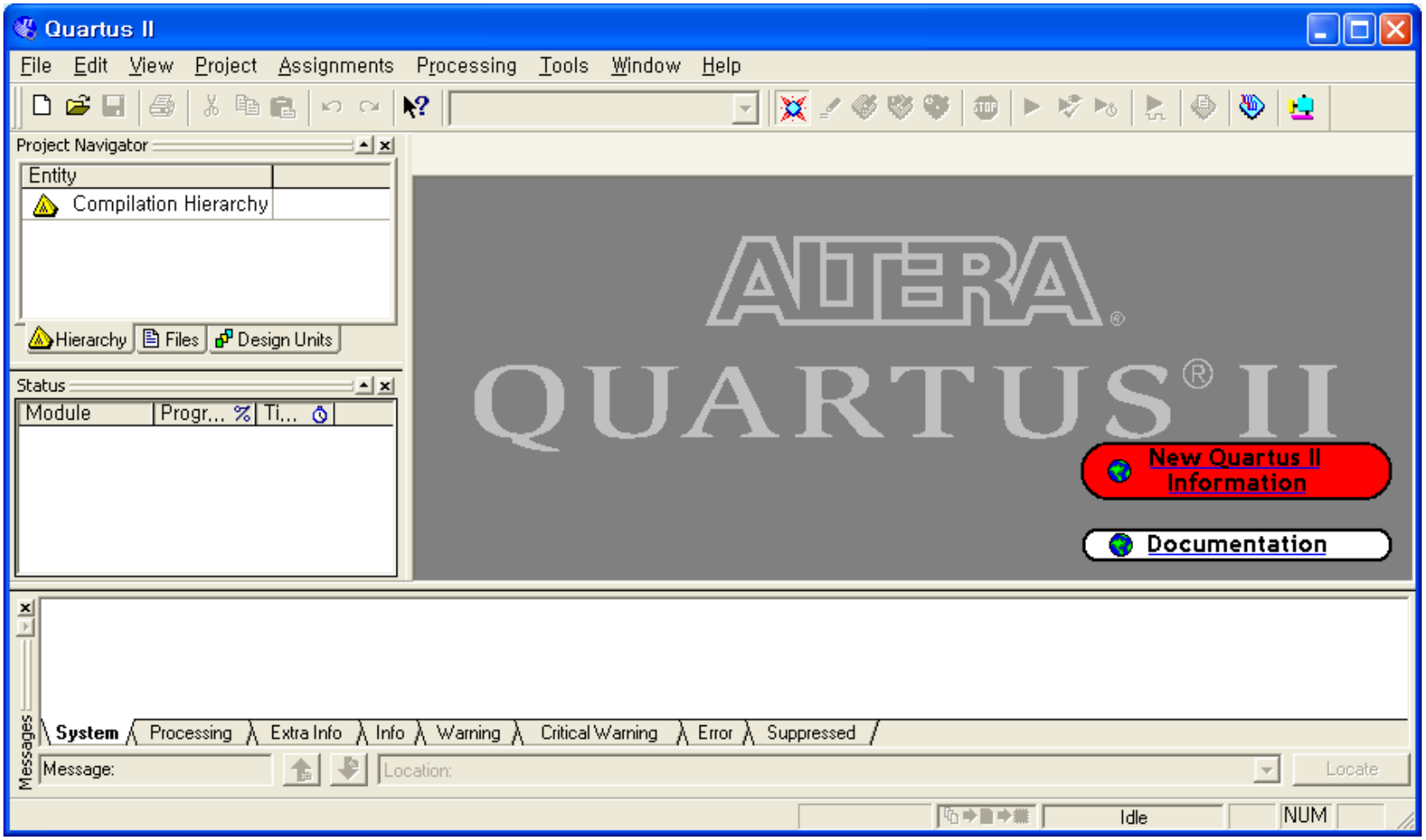
Quartus II 타이밍 분석



Quartus II 디바이스 프로그래밍



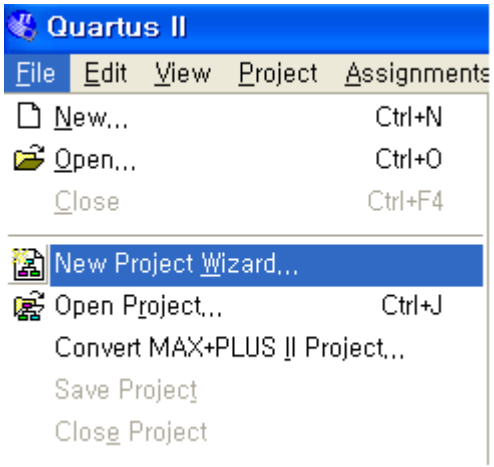
Quartus II 메인 화면

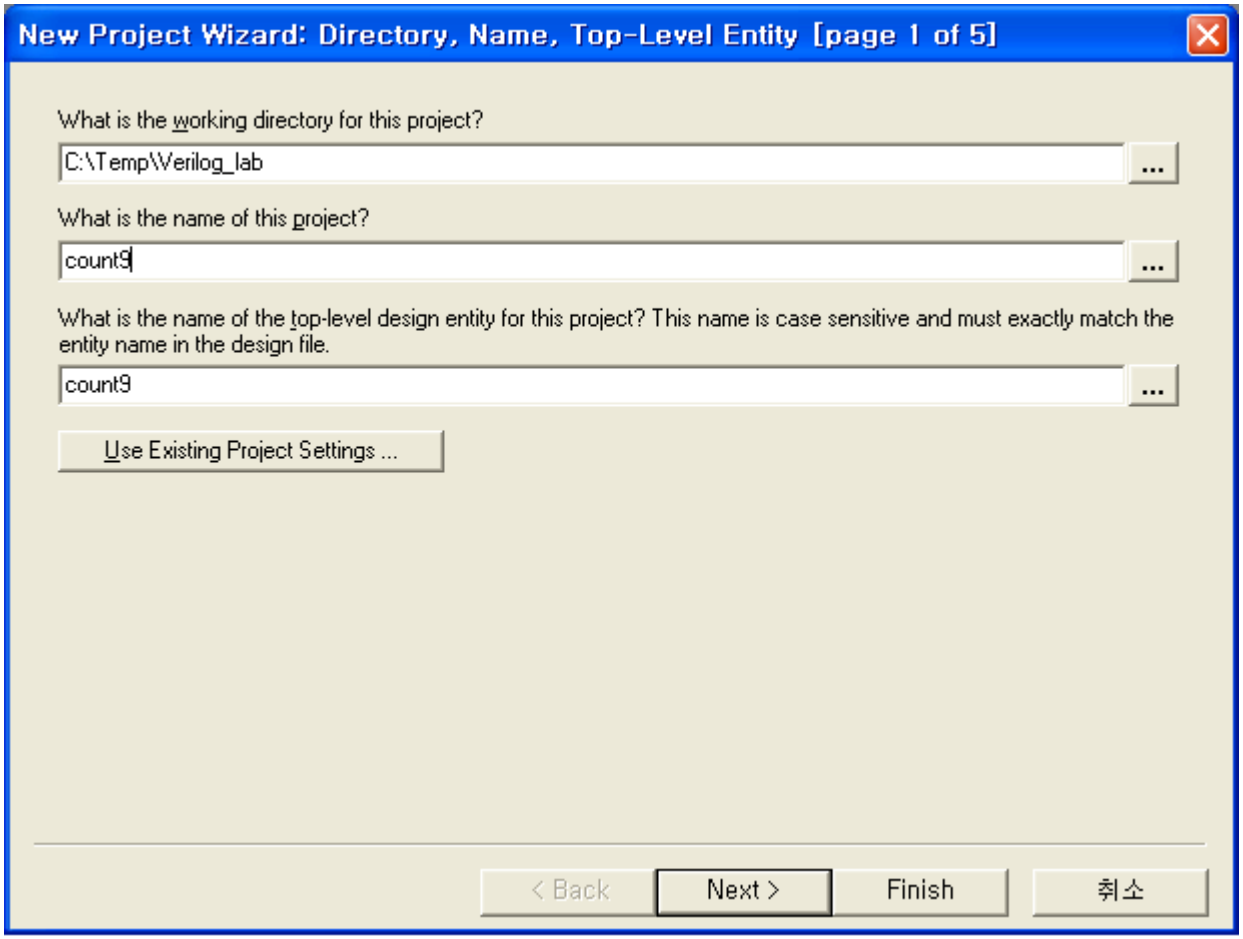


프로젝트 생성

File -> New Project Wizard를 선택

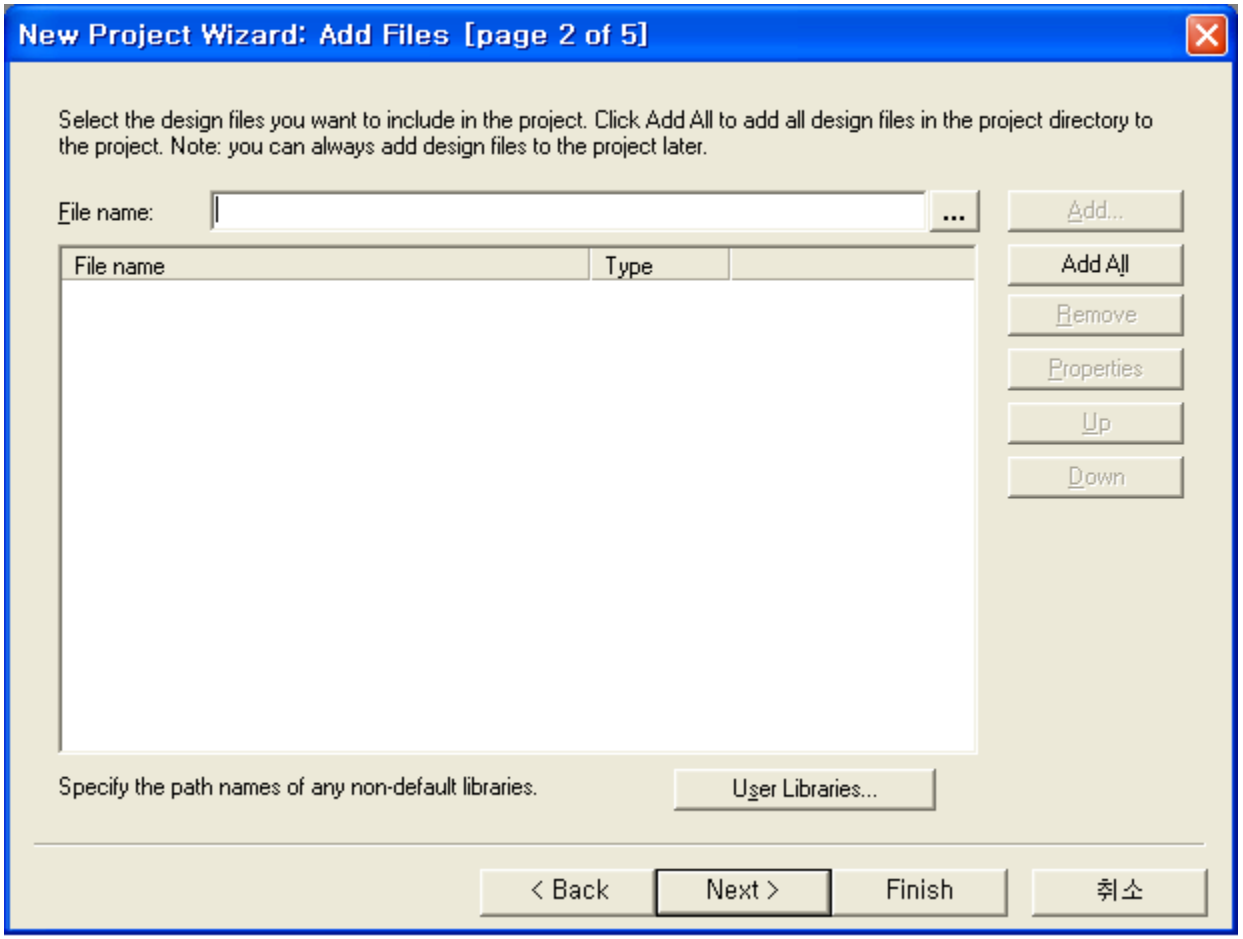
- Working directory, Project Name, Top-Level Design entity 등을 설정





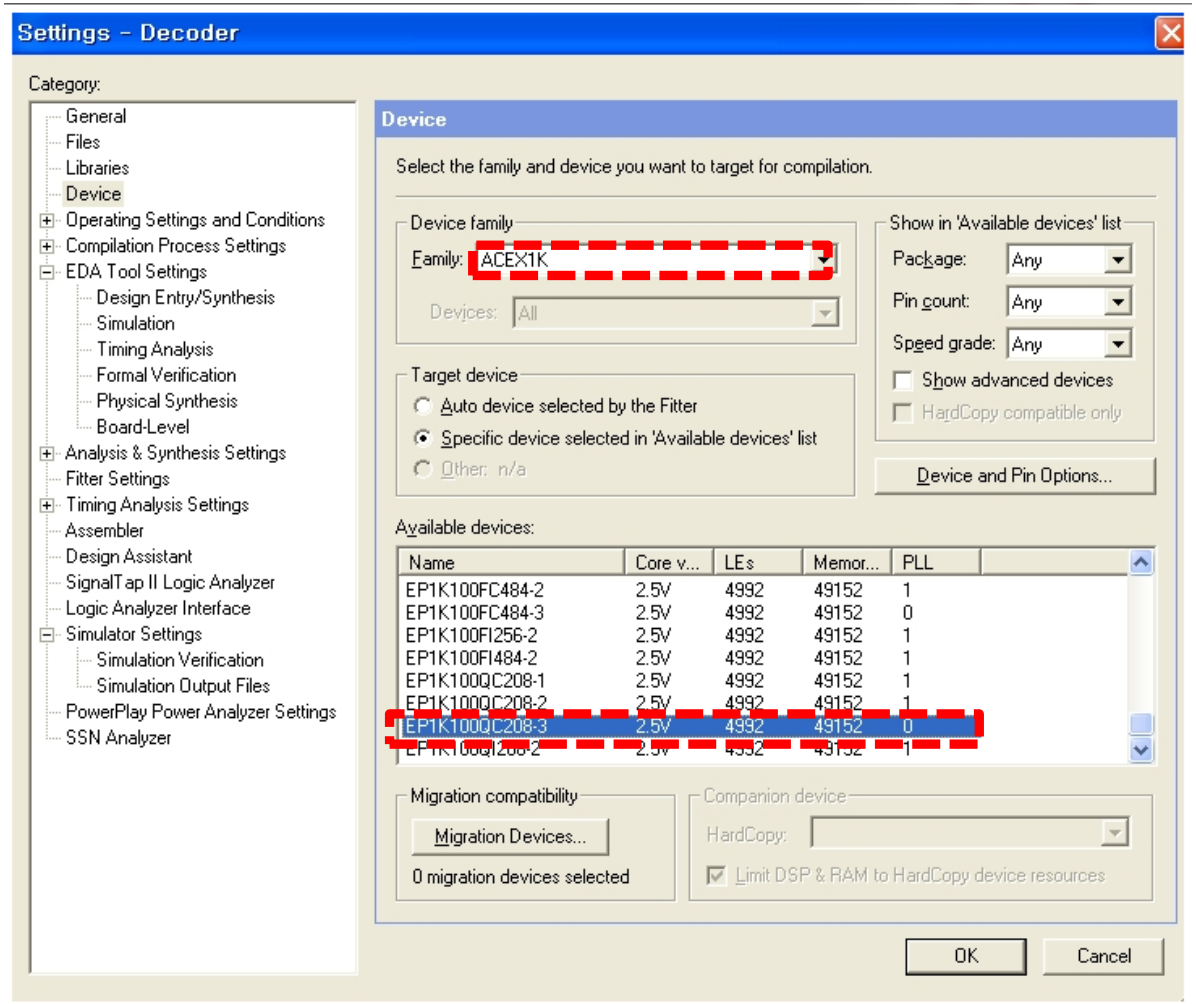
프로젝트 생성

- Add Files **대화창**



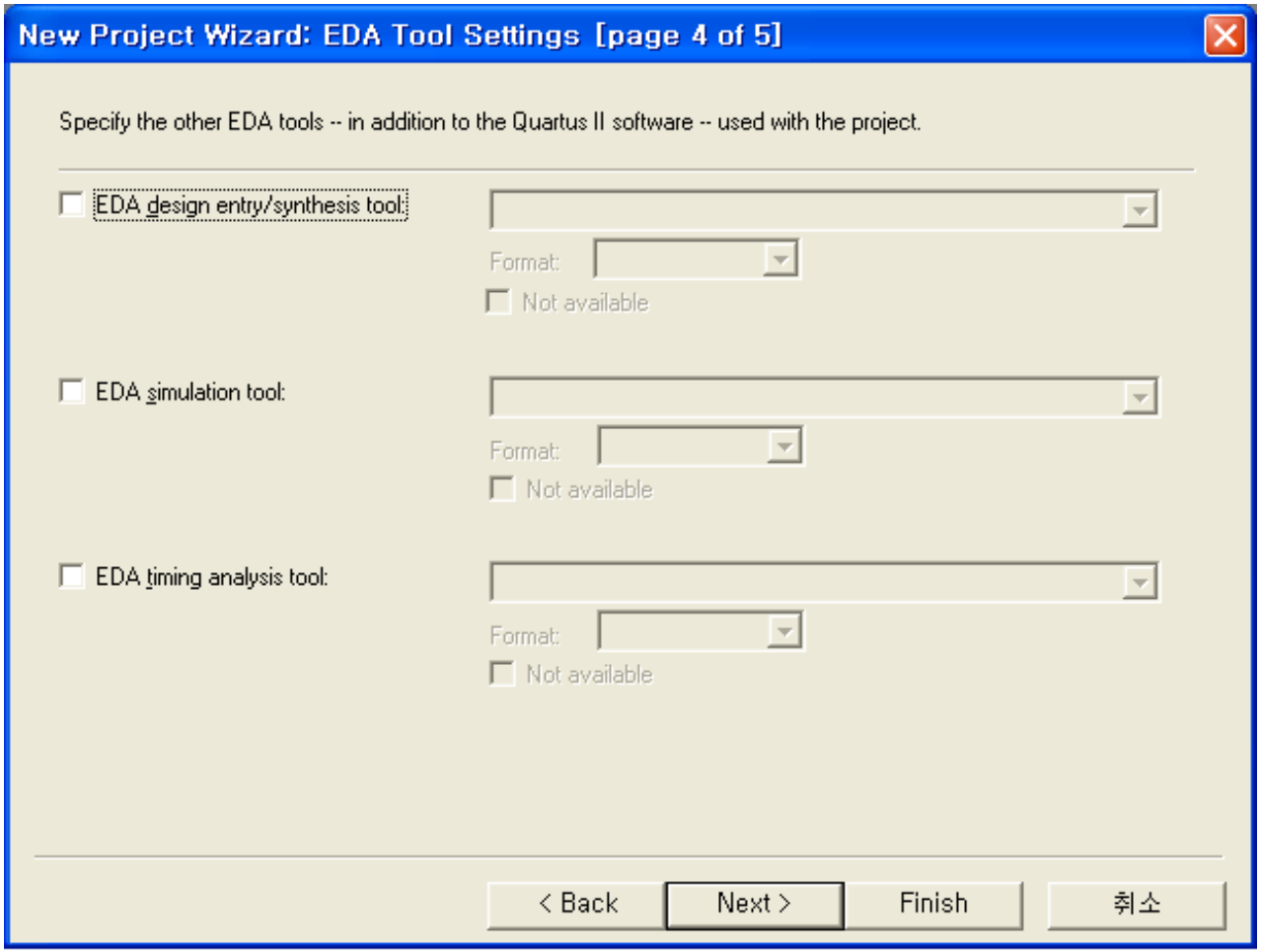
프로젝트 생성

- Family & Device Settings **대화창**



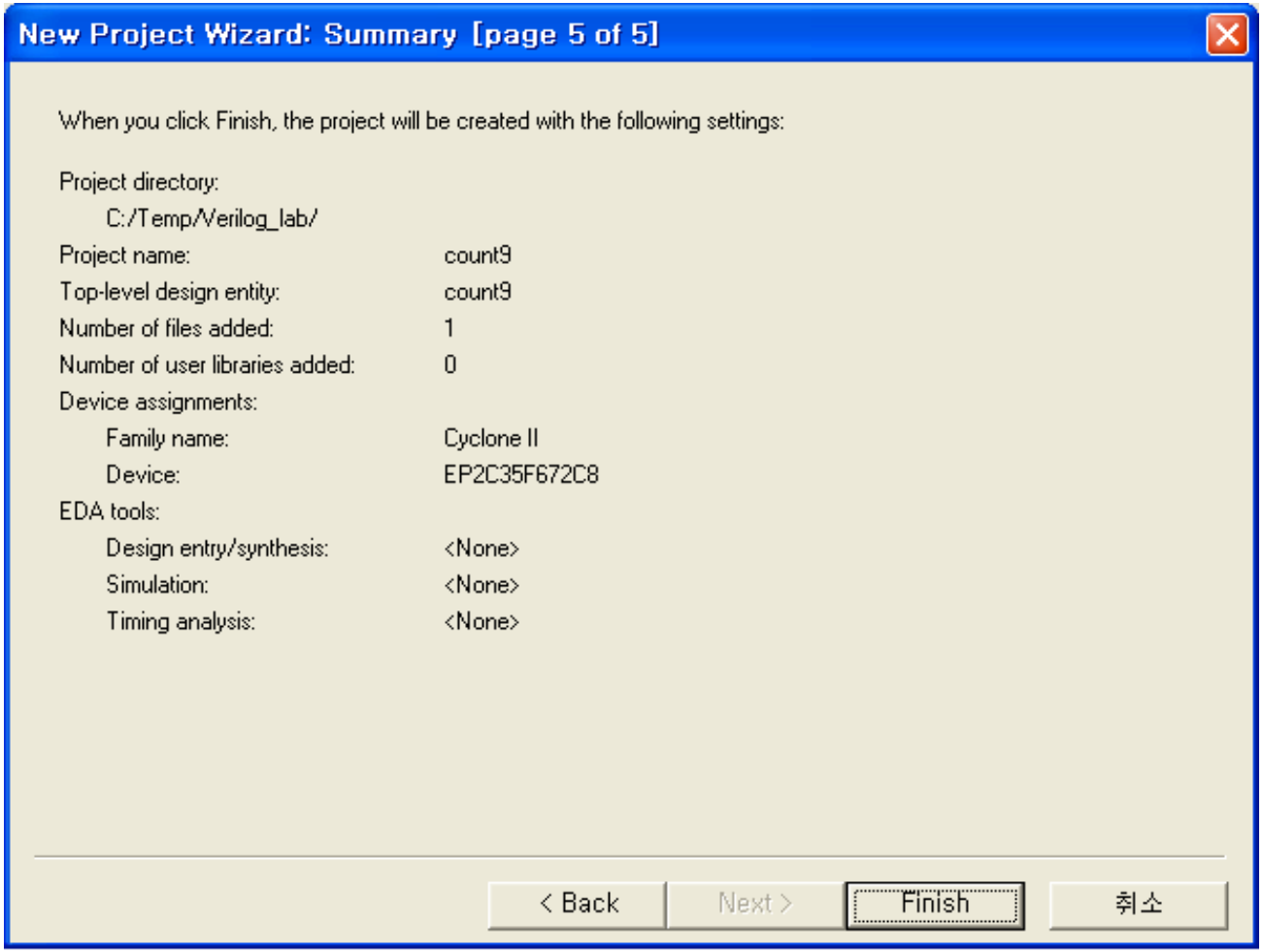
프로젝트 생성

- EDA Tools Settings **대화창**



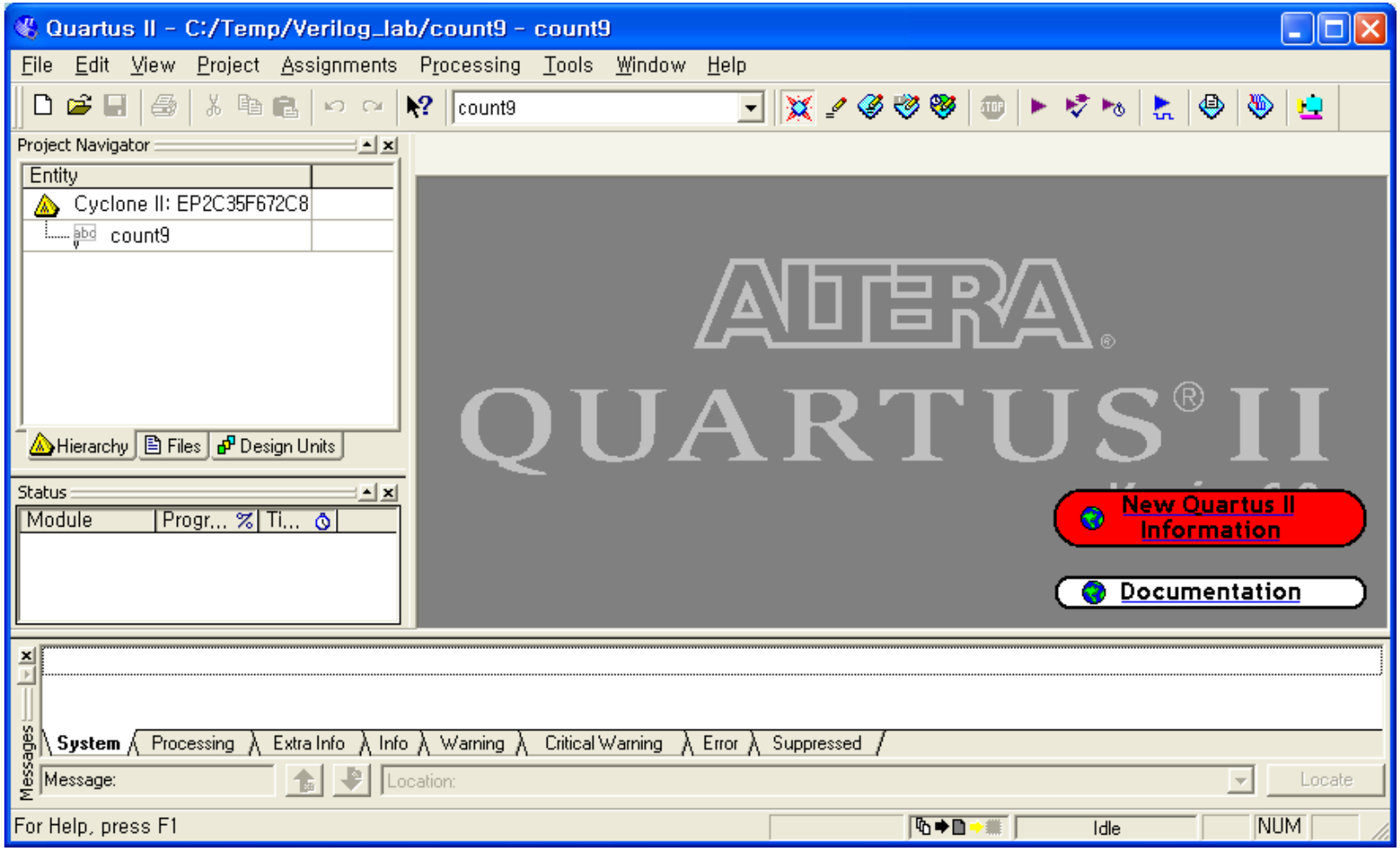
프로젝트 생성

- Summary **대화창**



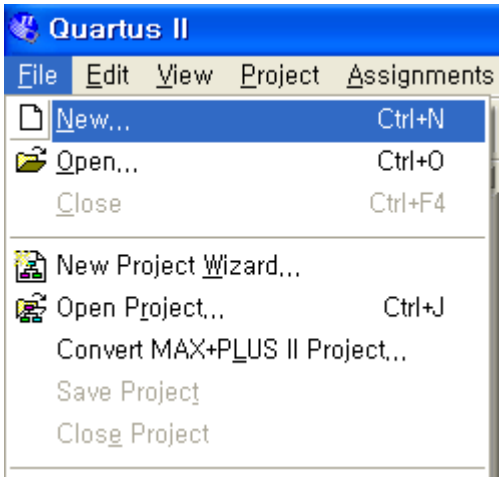
프로젝트 생성

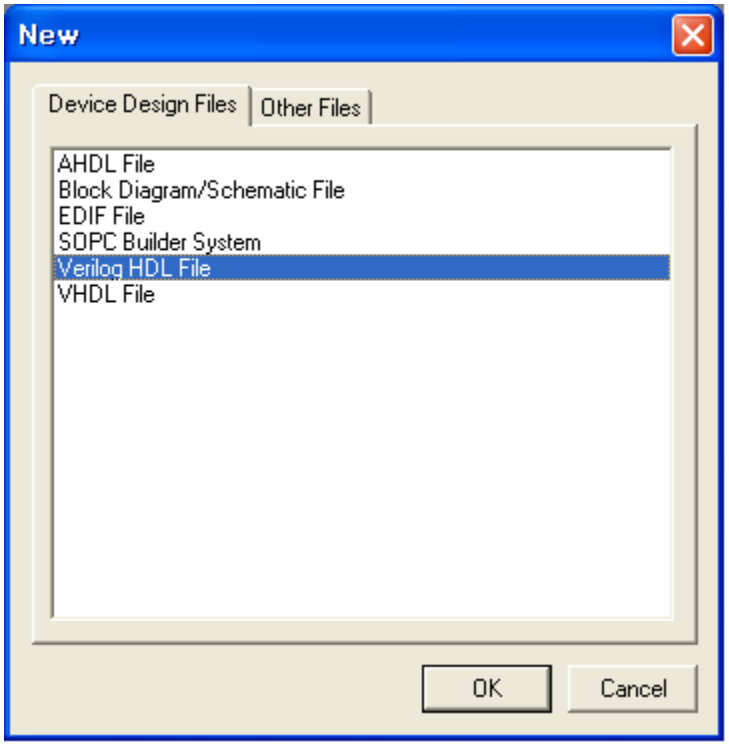
- 프로젝트 생성이 완료된 상태



설계 입력

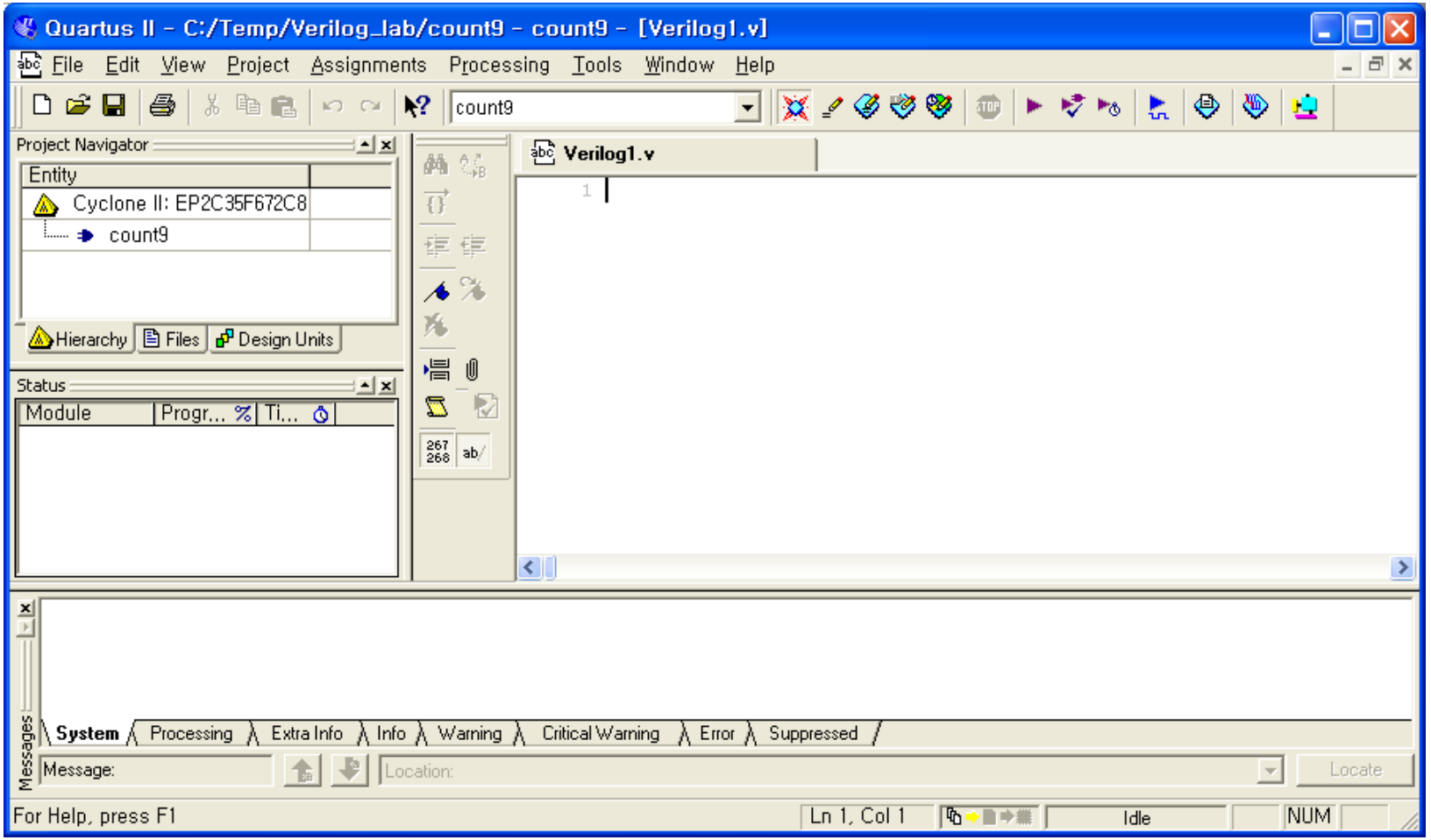
- File -> New를 선택
- New 대화창에서 Verilog HDL File을 선택





설계 입력

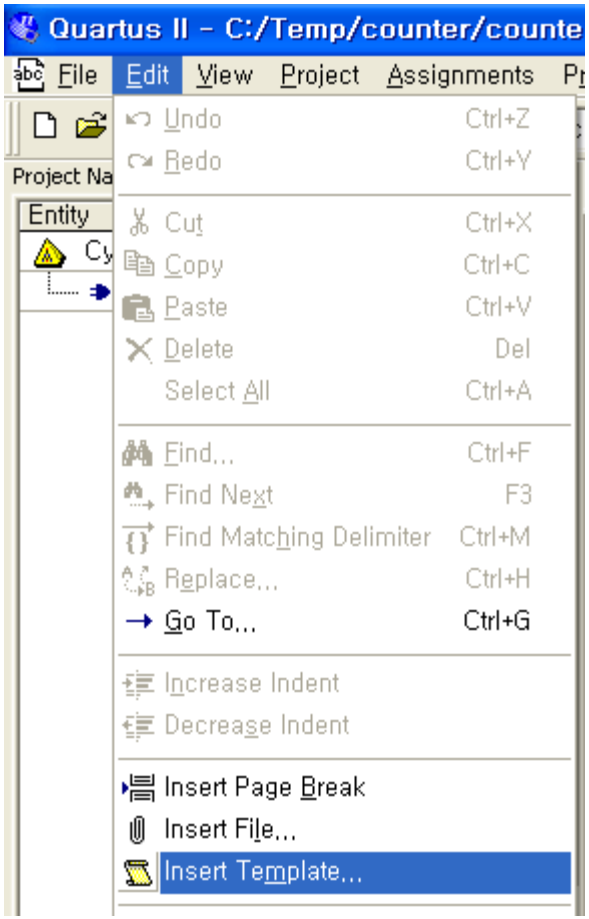
- 문서 편집기가 활성화된 상태

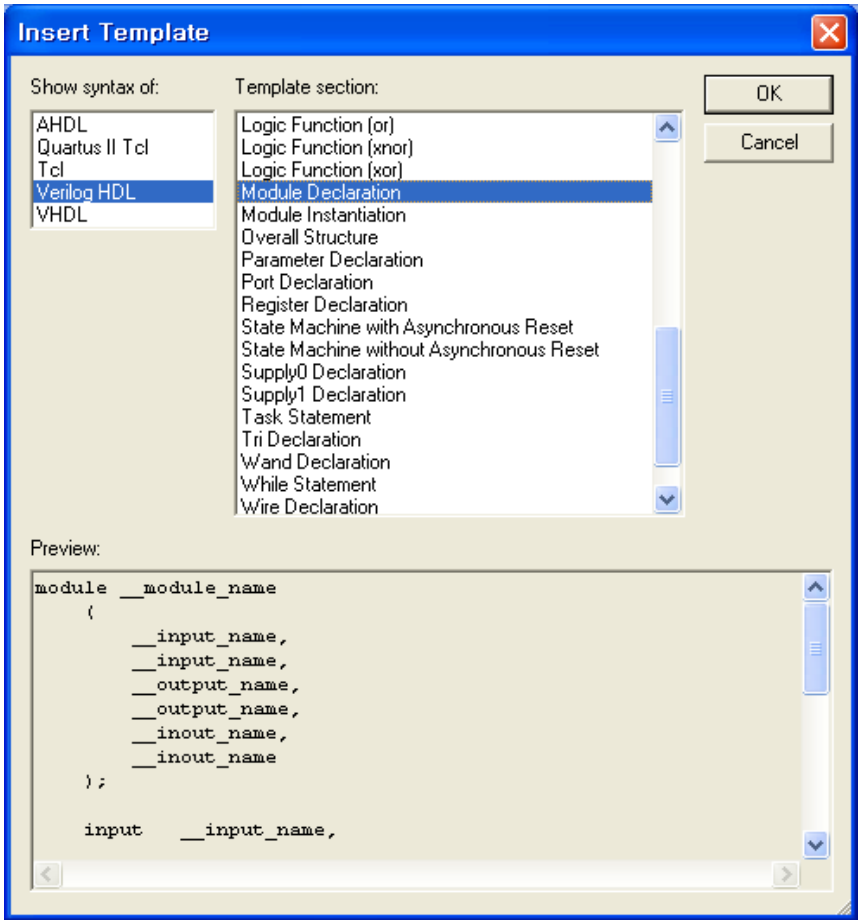


설계 입력

HDL Template를 이용한 설계 입력

- Edit -> Insert Template

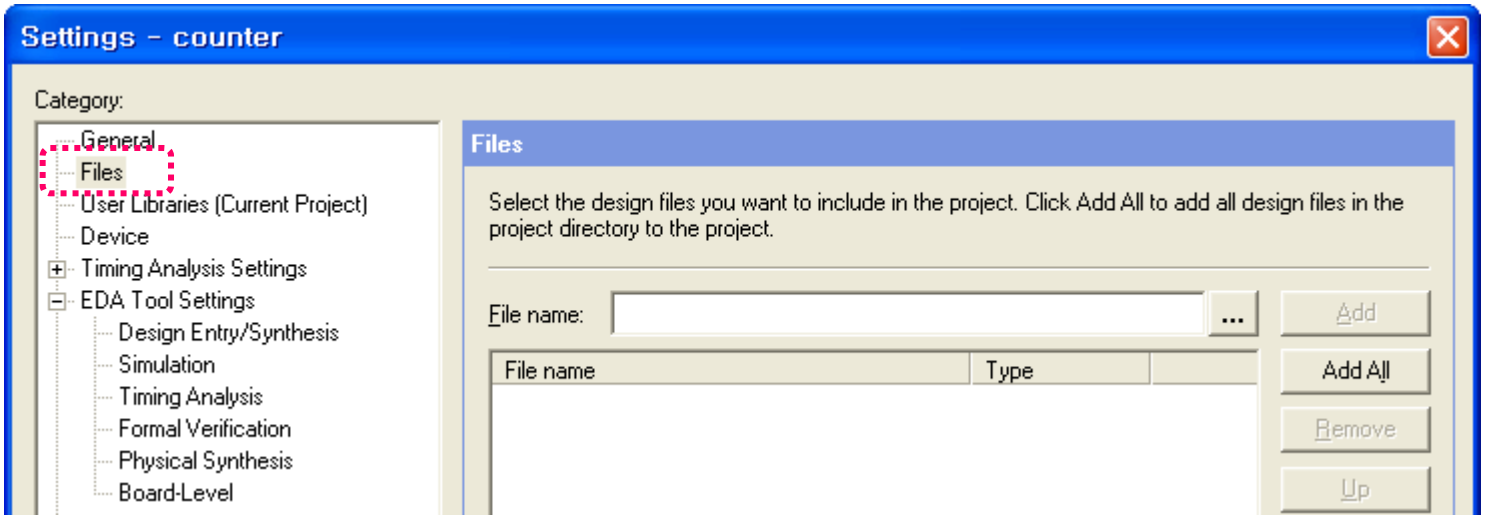




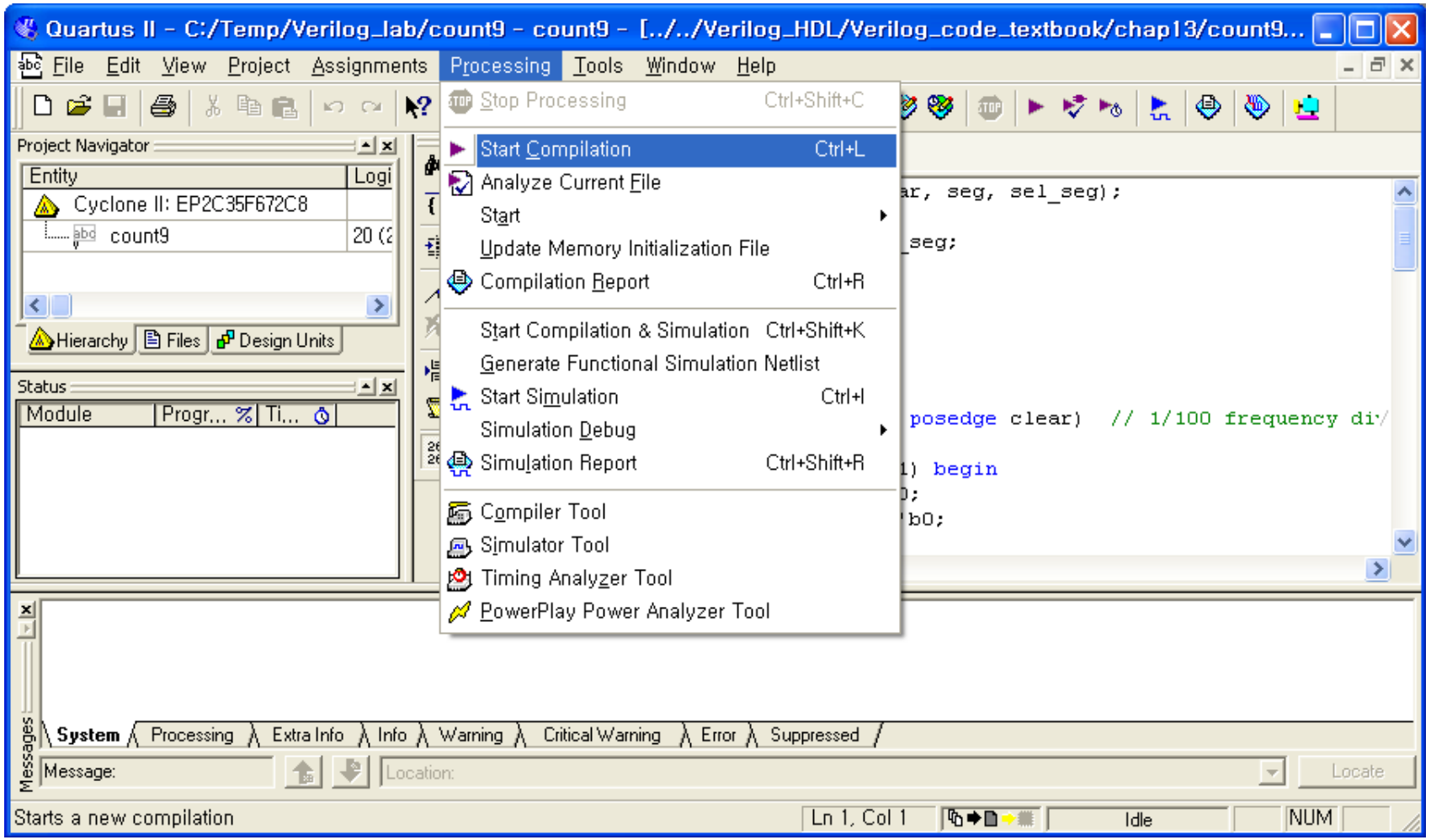
설계 입력

HDL 소스파일 추가

- Project -> Add/Remove Files

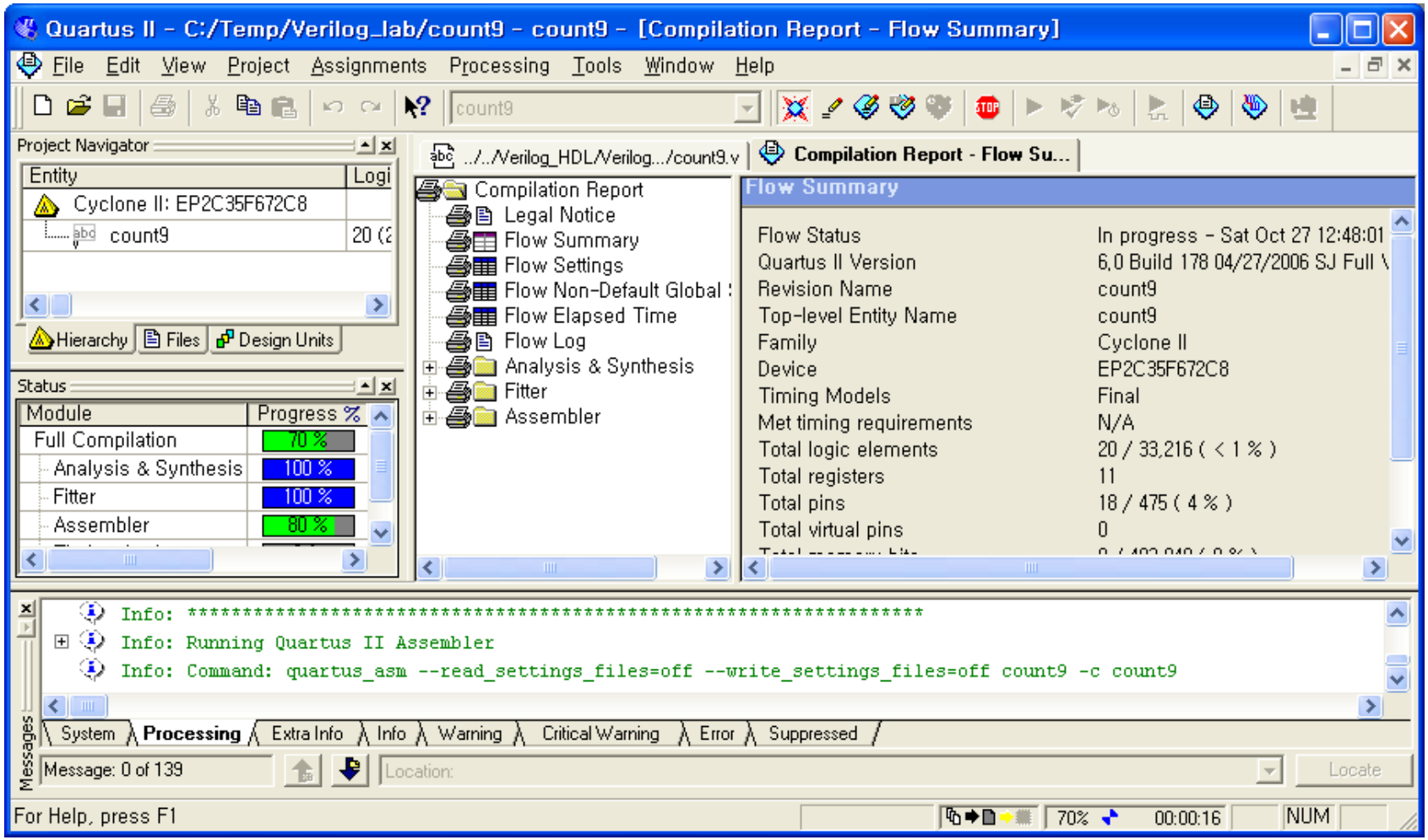


컴파일


Quartus II - C:/Temp/Verilog_lab/count9 - count9 - [../../Verilog_HDL/Verilog_code_textbook/chap13/count9...
File Edit View Project Assignments Processing Tools Window Help
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report Ctrl+R
Start Compilation & Simulation Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation Ctrl+I
Simulation Debug
Simulation Report Ctrl+Shift+R
Compiler Tool
Simulator Tool
Timing Analyzer Tool
PowerPlay Power Analyzer Tool
Project Navigator
Entity
Cyclone II: EP2C35F672C8
count9
Hierarchy Files Design Units
Status
Module
System Processing Extra Info Info Warning Critical Warning Error Suppressed
Message:
Location:
Locate
Starts a new compilation
Ln 1, Col 1
Idle
NUM

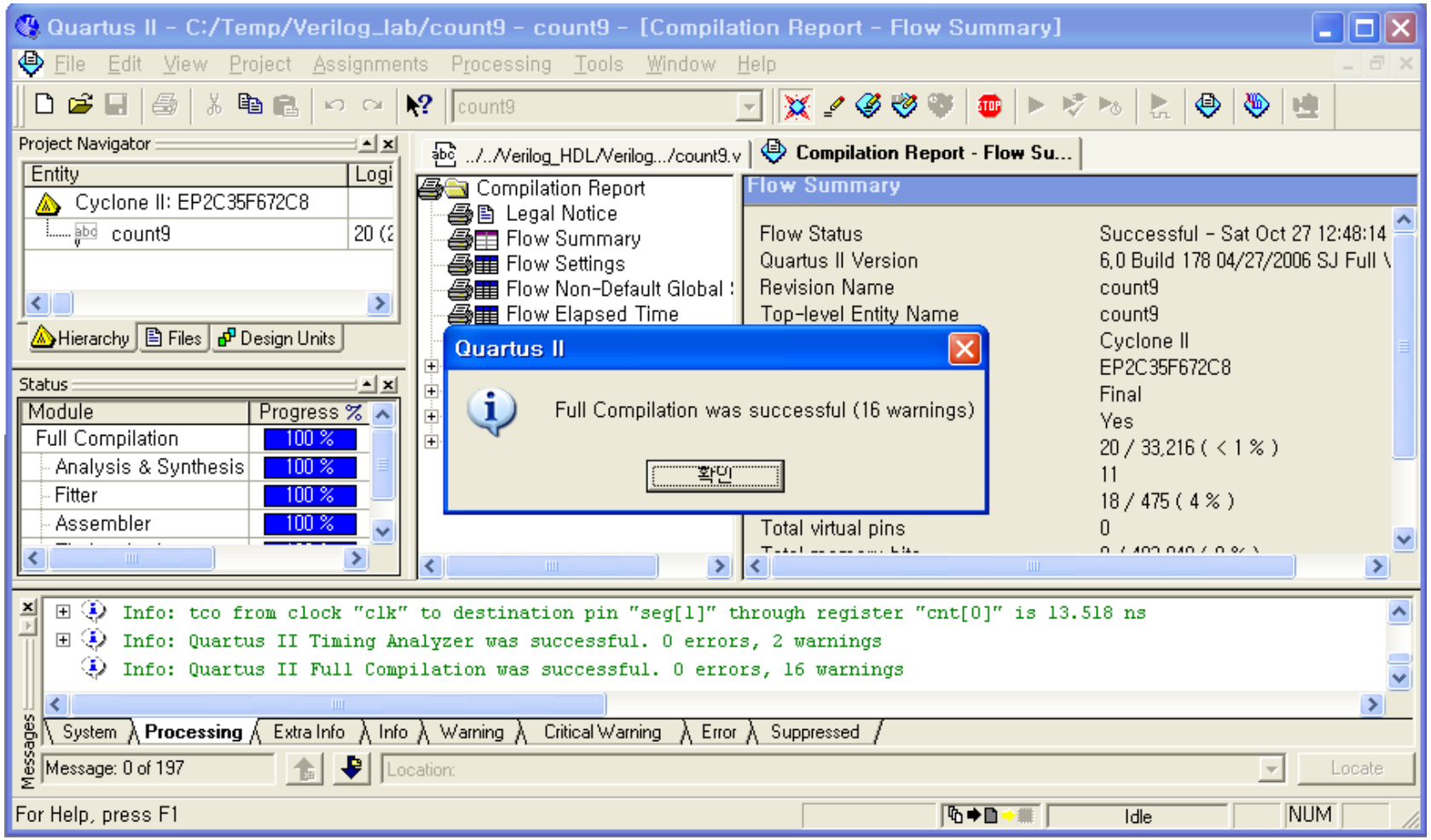
컴파일

◆ 컴파일 진행 과정


Quartus II - C:/Temp/Verilog_lab/count9 - count9 - [Compilation Report - Flow Summary]
File Edit View Project Assignments Processing Tools Window Help
count9
Project Navigator
Entity
Cyclone II: EP2C35F672C8
count9
Hierarchy Files Design Units
Status
Module Progress %
Full Compilation 70 %
Analysis & Synthesis 100 %
Fitter 100 %
Assembler 80 %
../../Verilog_HDL/Verilog.../count9.v
Compilation Report - Flow Su...
Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Global
Flow Elapsed Time
Flow Log
Analysis & Synthesis
Fitter
Assembler
Flow Summary
Flow Status In progress - Sat Oct 27 12:48:01
Quartus II Version 6.0 Build 178 04/27/2006 SJ Full
Revision Name count9
Top-level Entity Name count9
Family Cyclone II
Device EP2C35F672C8
Timing Models Final
Met timing requirements N/A
Total logic elements 20 / 33,216 (< 1 %)
Total registers 11
Total pins 18 / 475 (4 %)
Total virtual pins 0
Info: ********
Info: Running Quartus II Assembler
Info: Command: quartus_asm --read_settings_files=off --write_settings_files=off count9 -c count9
Messages
System Processing Extra Info Info Warning Critical Warning Error Suppressed
Message: 0 of 139
Location:
Locate
For Help, press F1
70%
00:00:16
NUM

컴파일

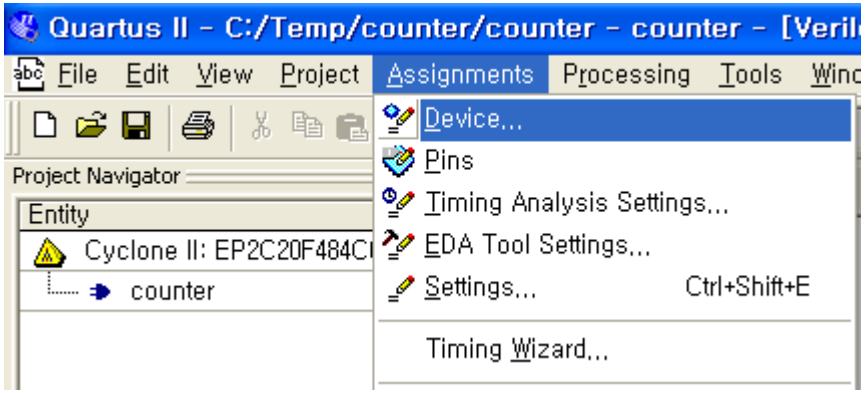
◆ 컴파일 완료 상태


Quartus II - C:/Temp/Verilog_lab/count9 - count9 - [Compilation Report - Flow Summary]
File Edit View Project Assignments Processing Tools Window Help
count9
Project Navigator
Entity
Cyclone II: EP2C35F672C8
count9
Hierarchy Files Design Units
Status
Module Progress %
Full Compilation 100 %
Analysis & Synthesis 100 %
Fitter 100 %
Assembler 100 %
../../Verilog_HDL/Verilog.../count9.v
Compilation Report - Flow Su...
Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Global
Flow Elapsed Time
Flow Summary
Flow Status Successful - Sat Oct 27 12:48:14
Quartus II Version 6.0 Build 178 04/27/2006 SJ Full
Revision Name count9
Top-level Entity Name count9
Cyclone II
EP2C35F672C8
Final
Yes
20 / 33,216 (< 1 %)
11
18 / 475 (4 %)
Total virtual pins 0
Quartus II
Full Compilation was successful (16 warnings)
확인
Info: tco from clock "clk" to destination pin "seg[1]" through register "cnt[0]" is 13.518 ns
Info: Quartus II Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 16 warnings
System Processing Extra Info Info Warning Critical Warning Error Suppressed
Messages
Message: 0 of 197
Location:
Locate
For Help, press F1
Idle
NUM

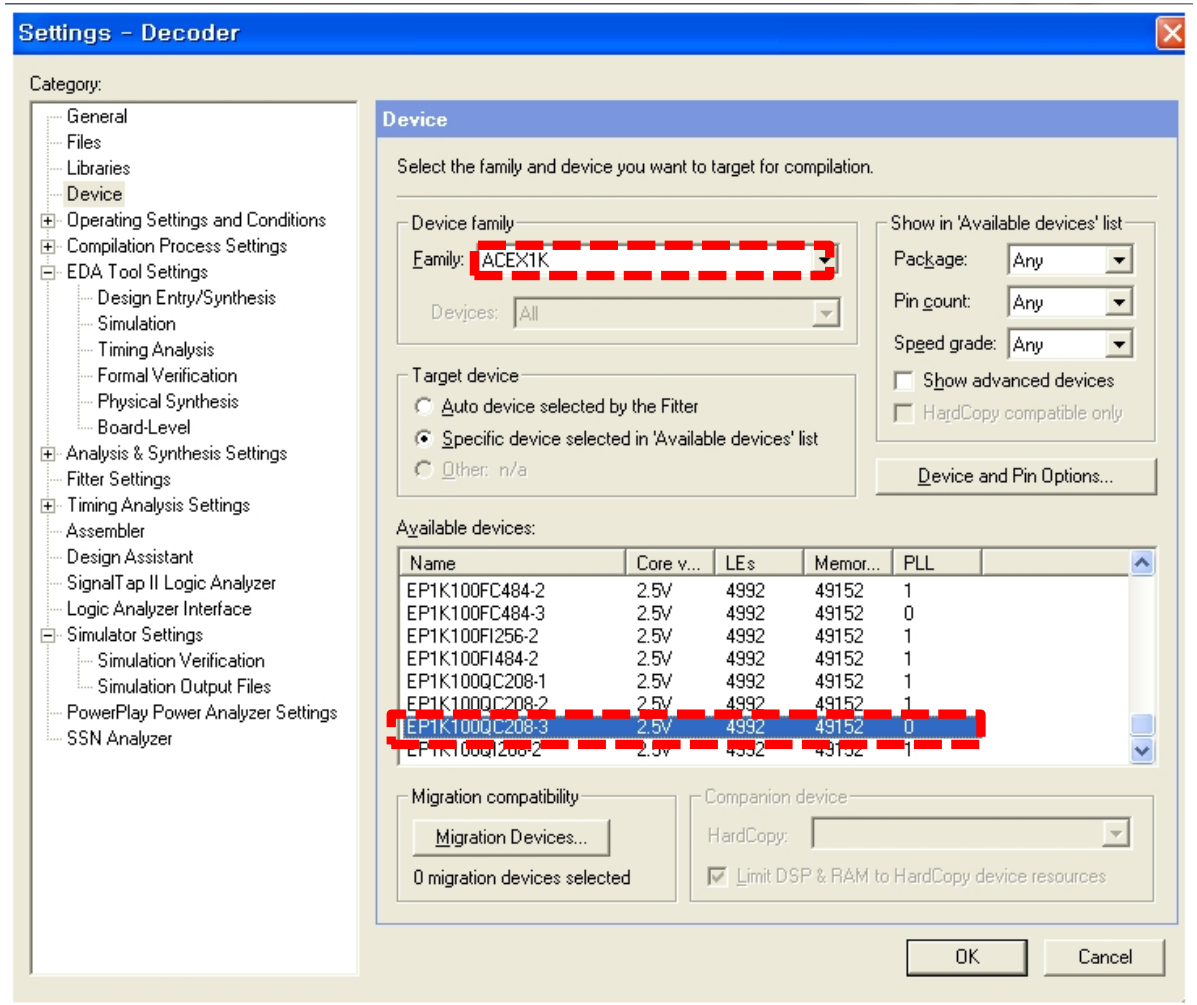
디바이스 및 핀 할당

Target device 지정

- Assignments -> Device



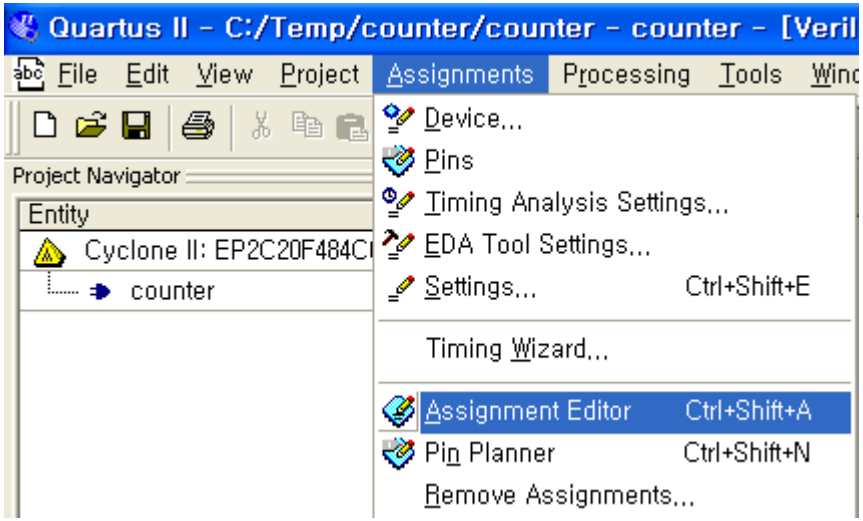
디바이스 및 핀 할당


Settings - Decoder
Category:
General
Files
Libraries
Device
Operating Settings and Conditions
Compilation Process Settings
EDA Tool Settings
Design Entry/Synthesis
Simulation
Timing Analysis
Formal Verification
Physical Synthesis
Board-Level
Analysis & Synthesis Settings
Fitter Settings
Timing Analysis Settings
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
Simulator Settings
Simulation Verification
Simulation Output Files
PowerPlay Power Analyzer Settings
SSN Analyzer
Device
Select the family and device you want to target for compilation.
Device family
Family: ACEX1K
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Show advanced devices
HardCopy compatible only
Device and Pin Options...
Available devices:
Name Core v... LEs Memor... PLL
EP1K100FC484-2 2.5V 4992 49152 1
EP1K100FC484-3 2.5V 4992 49152 0
EP1K100FI256-2 2.5V 4992 49152 1
EP1K100FI484-2 2.5V 4992 49152 1
EP1K100QC208-1 2.5V 4992 49152 1
EP1K100QC208-2 2.5V 4992 49152 1
EP1K100QC208-3 2.5V 4992 49152 0
Migration compatibility
Migration Devices...
0 migration devices selected
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
OK
Cancel

디바이스 및 핀 할당

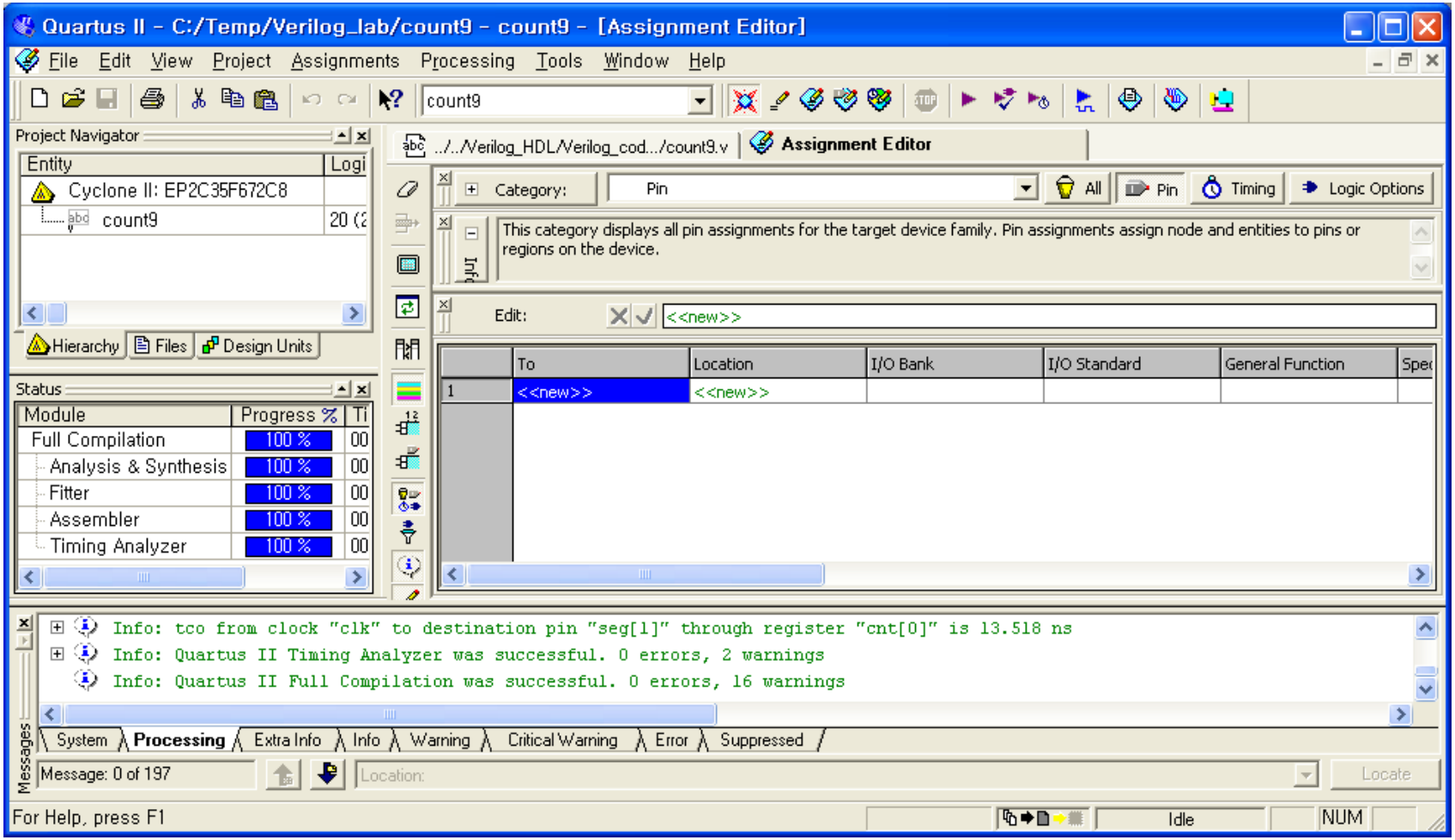
Device Pin 할당

- Assignments -> Assignment Editor



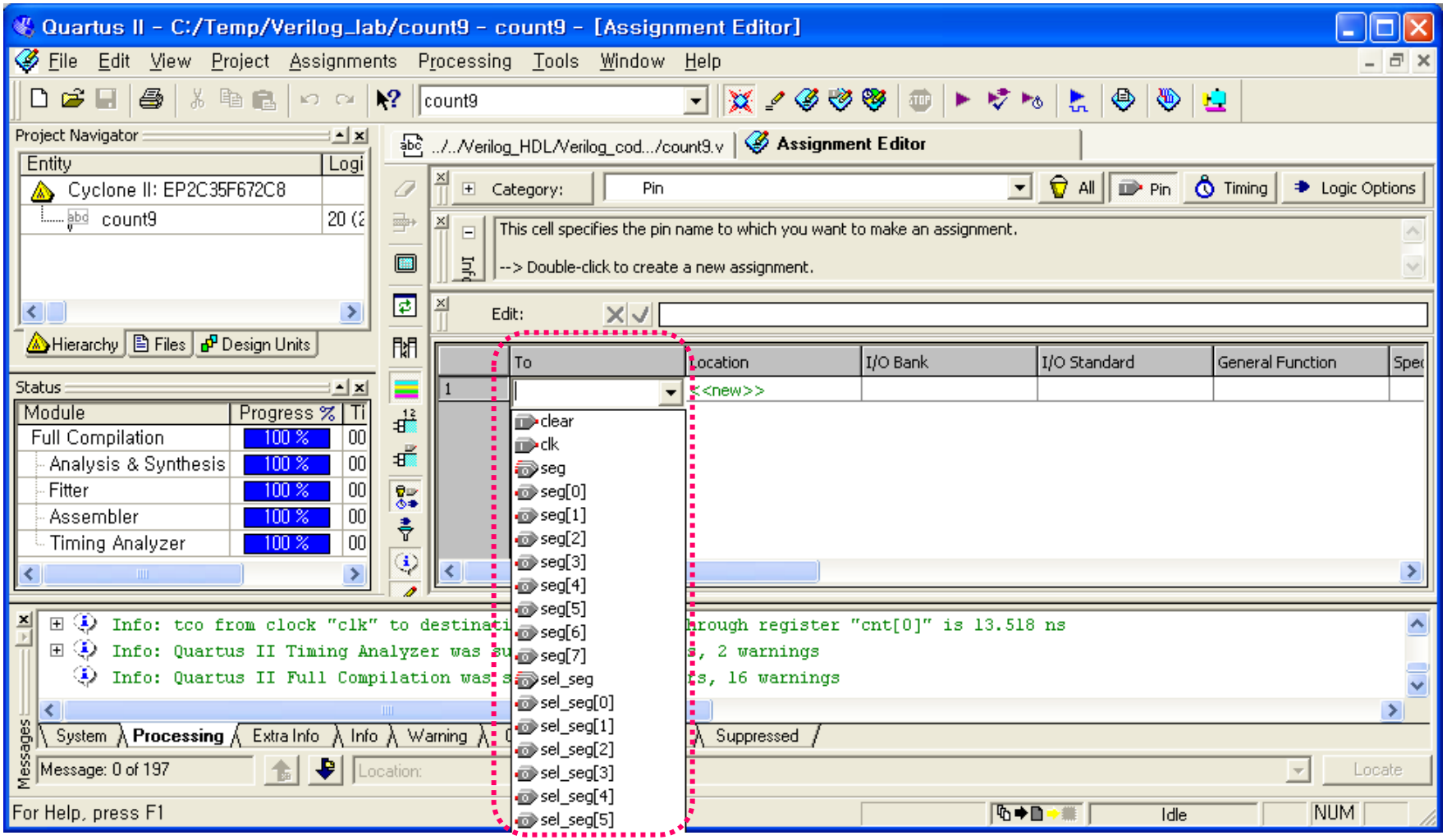
디바이스 및 핀 할당

- Assignment Editor



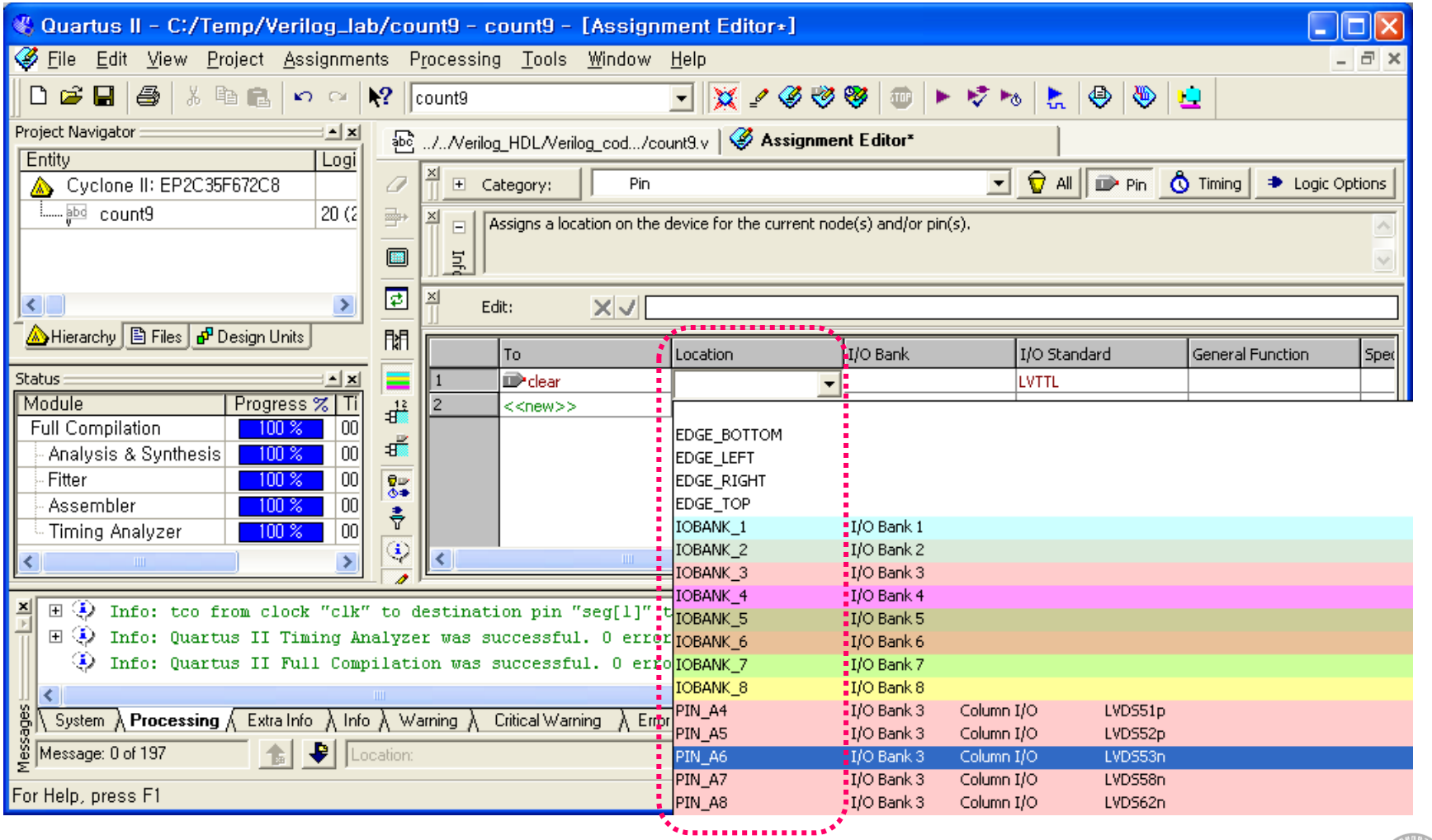
디바이스 및 핀 할당

- Port 선택



디바이스 및 핀 할당

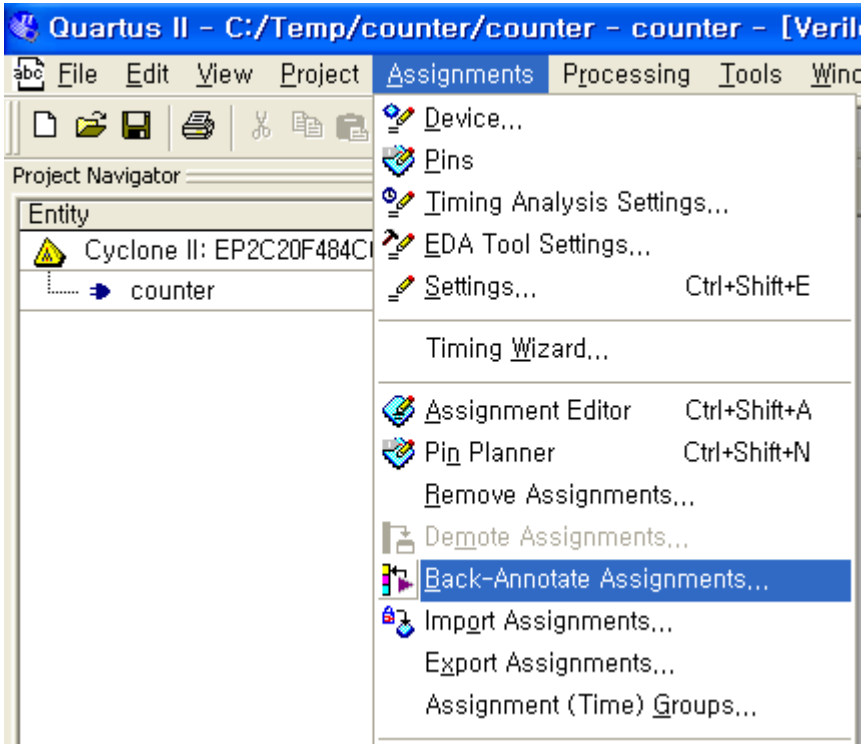
- Pin 할당



디바이스 및 핀 할당

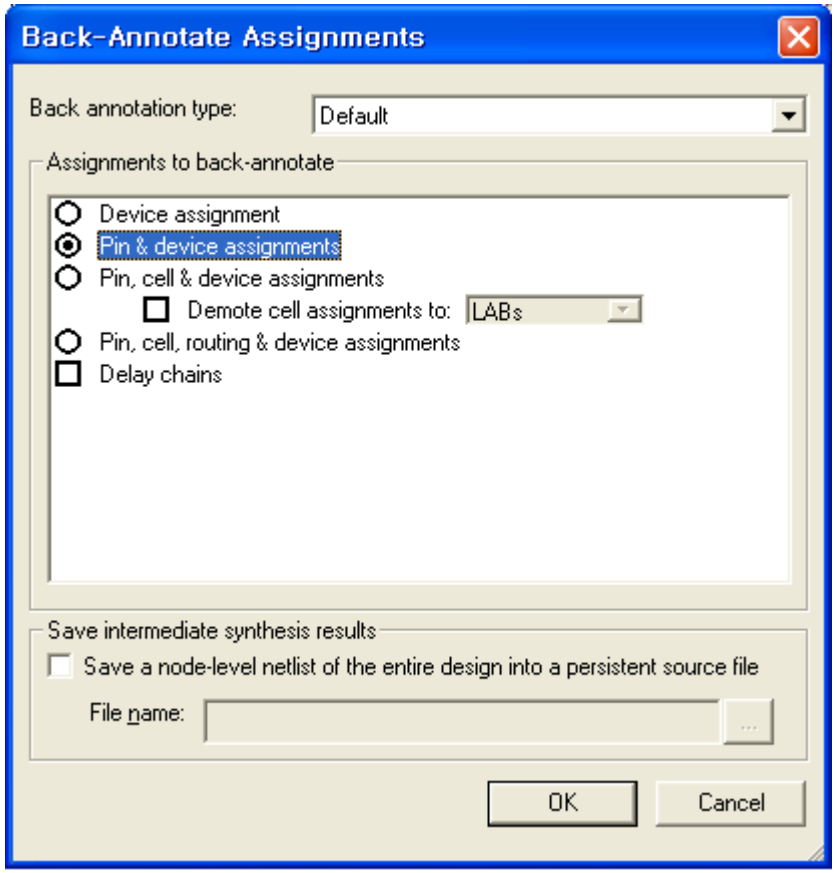
Back-Annotate Assignments를 이용한 핀 할당

- 사전에 full compile이 완료되어야 함.



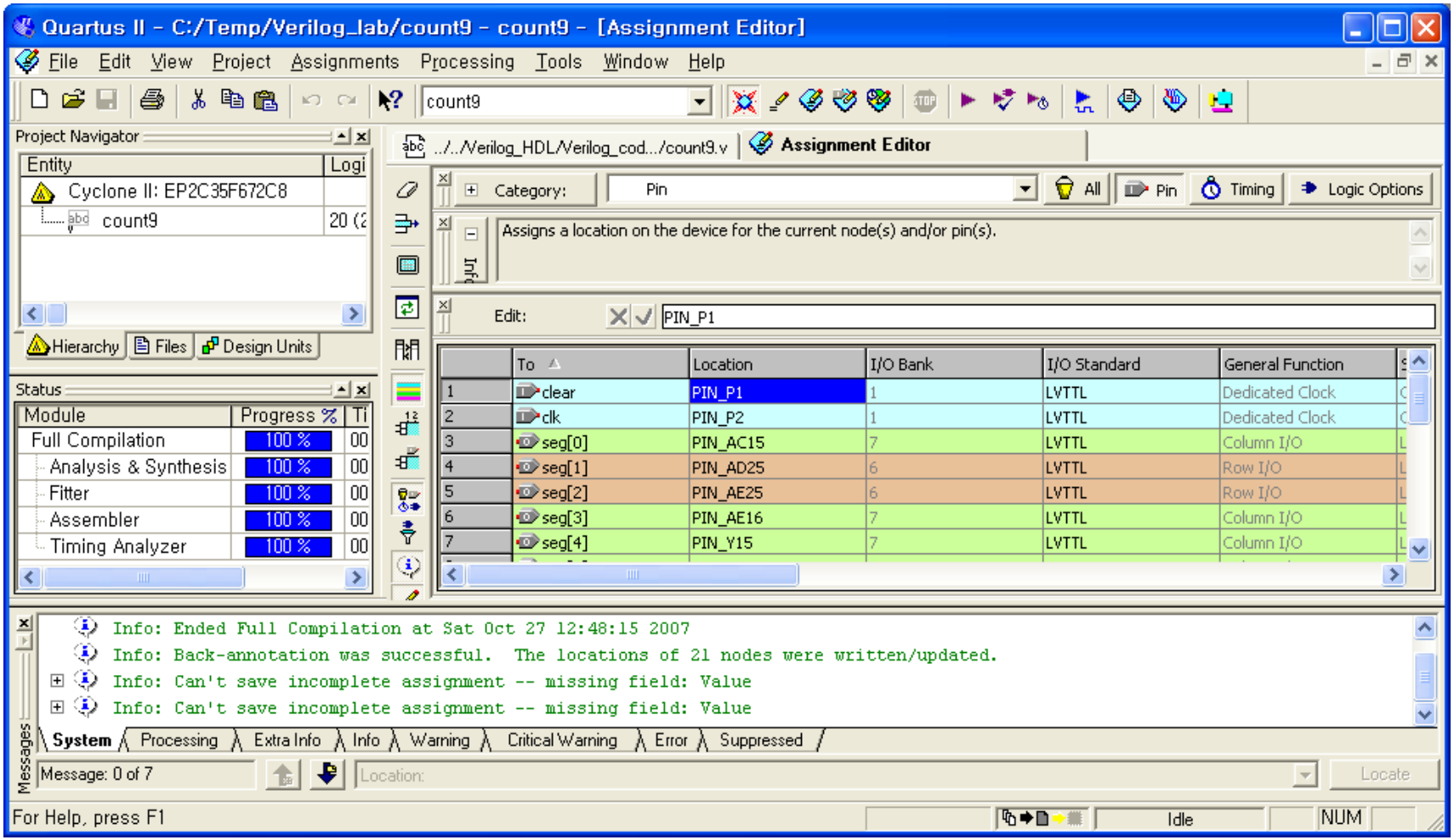
디바이스 및 핀 할당

▣ Back-Annotate Assignments를 이용한 핀 정보 불러오기



디바이스 및 핀 할당

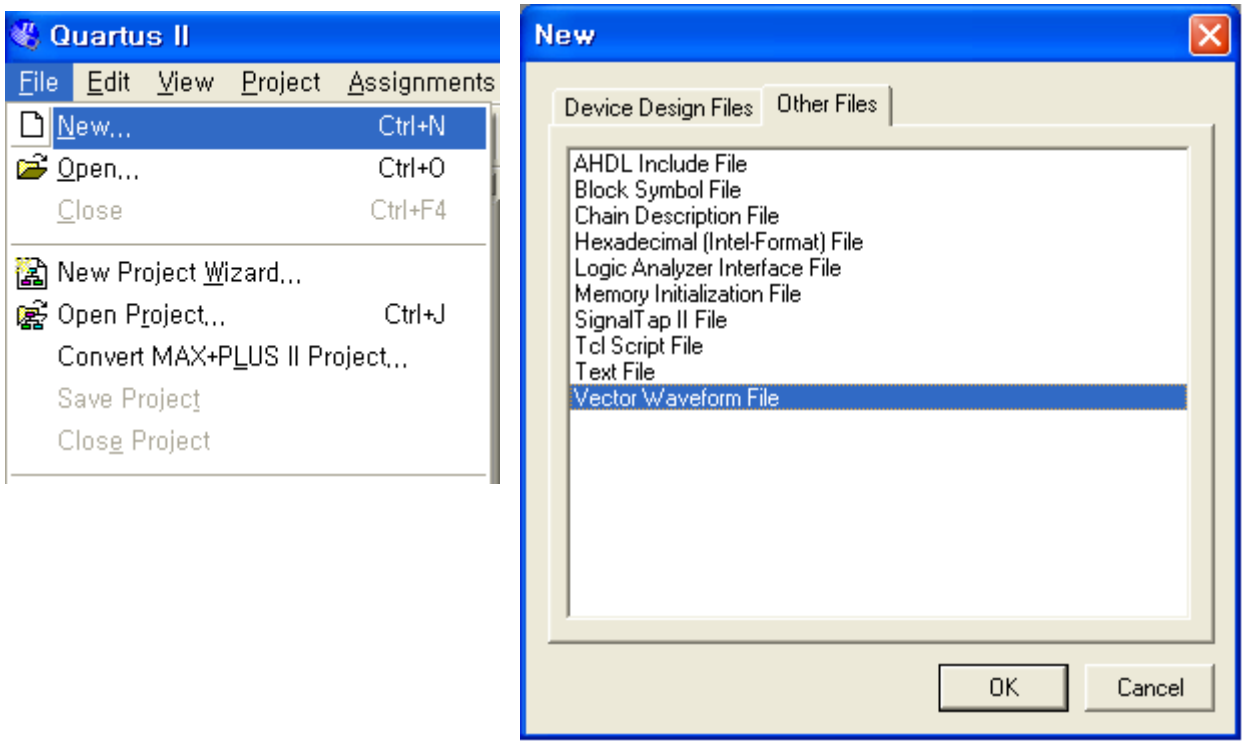
- Assignment Editor를 사용하여 Pin 정보를 수정



시뮬레이션

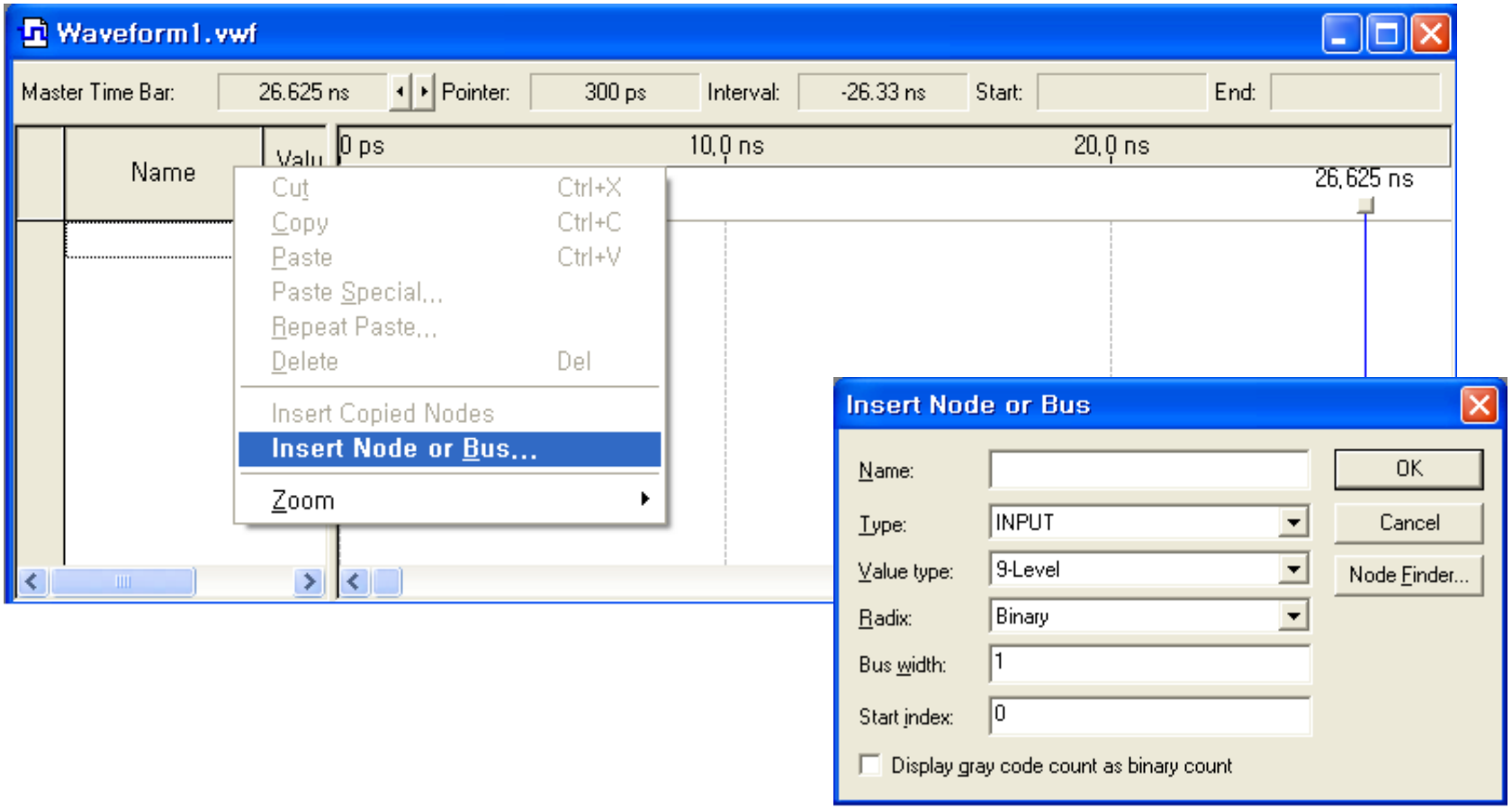
Quartus II Simulator를 사용한 시뮬레이션

- File -> New
- Vector Waveform File



시뮬레이션

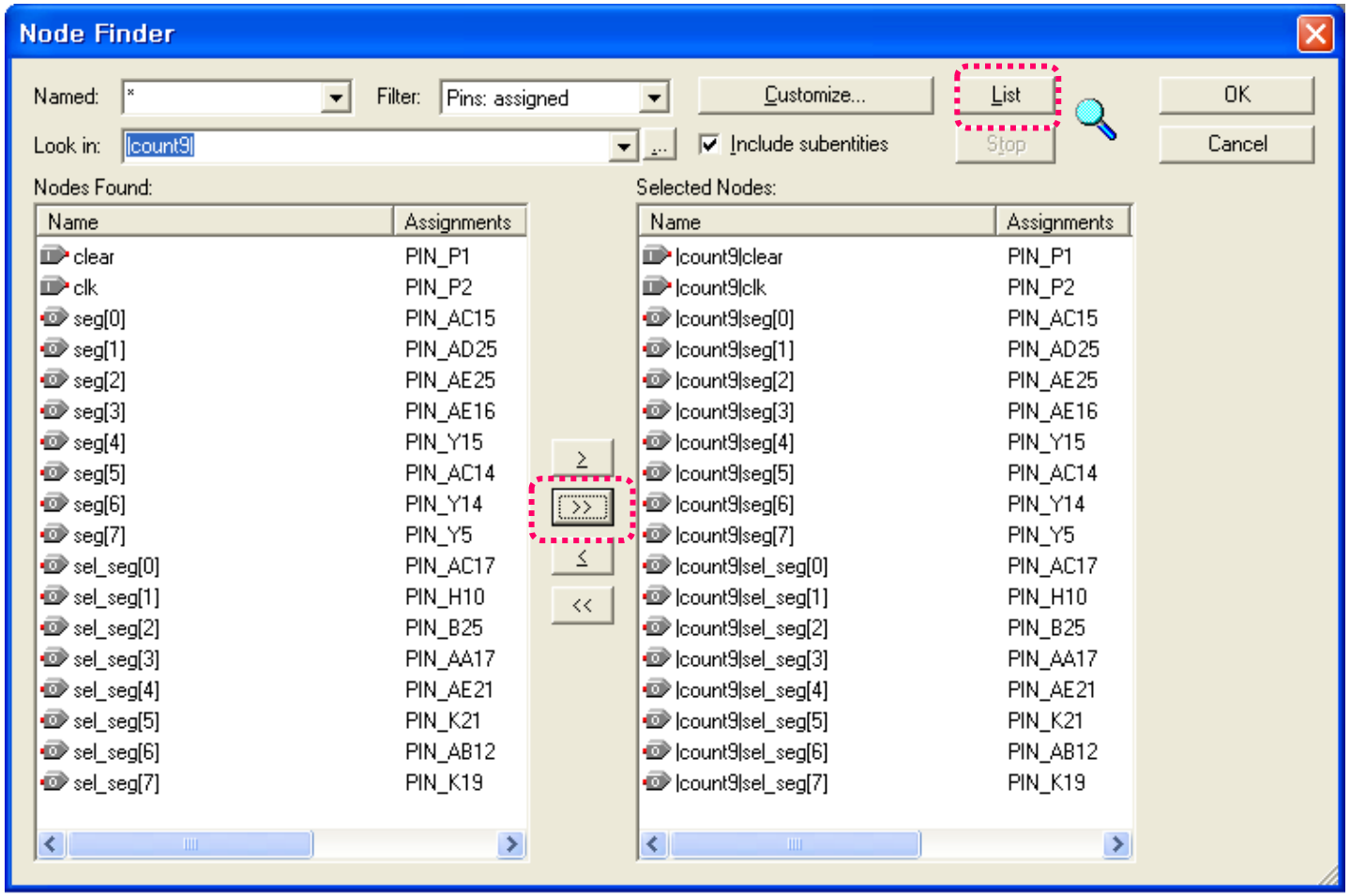
▣ 시뮬레이션 입력파형 생성



시뮬레이션

▣ 시뮬레이션 입력파형 생성

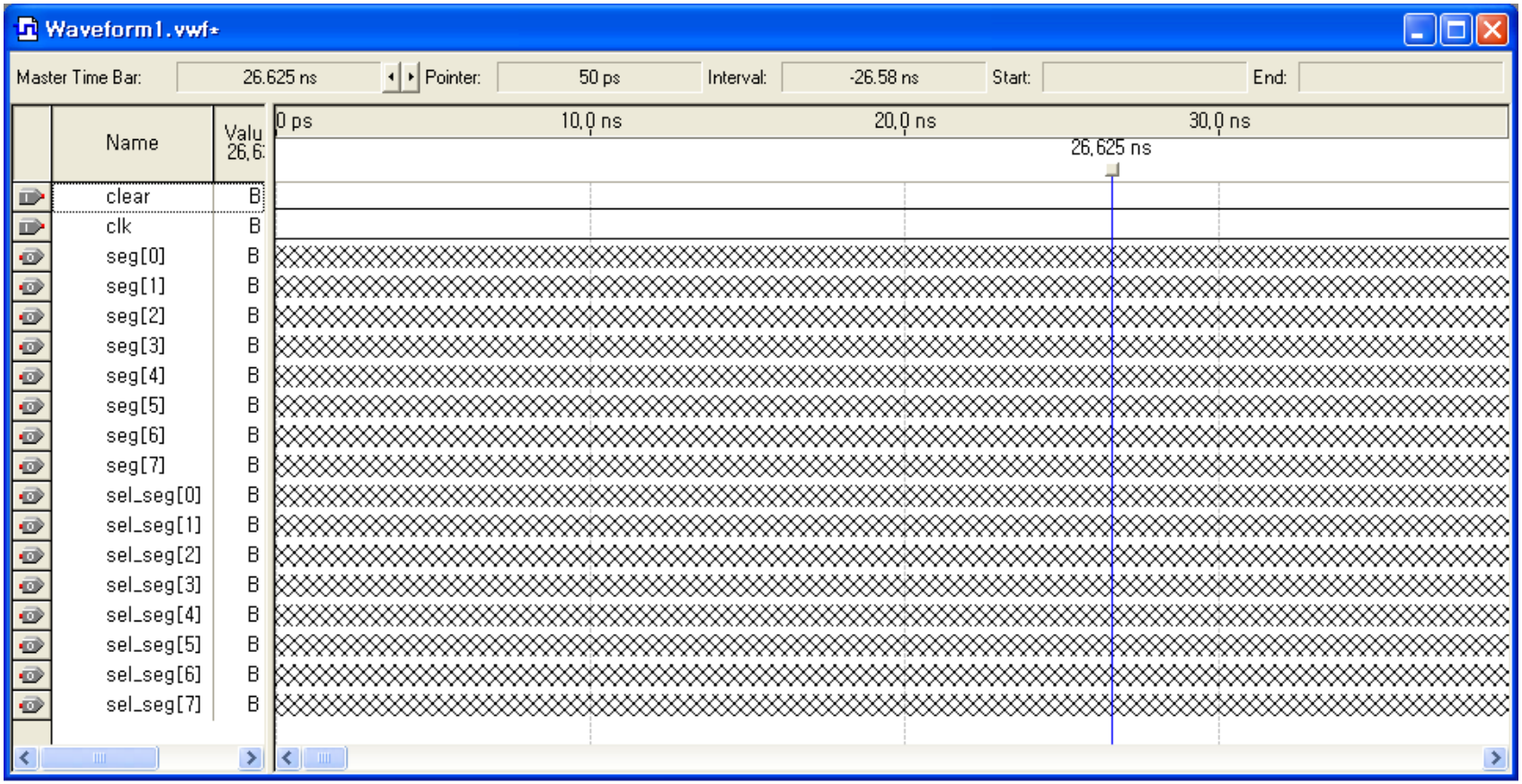
◆ Node Finder 창



시뮬레이션

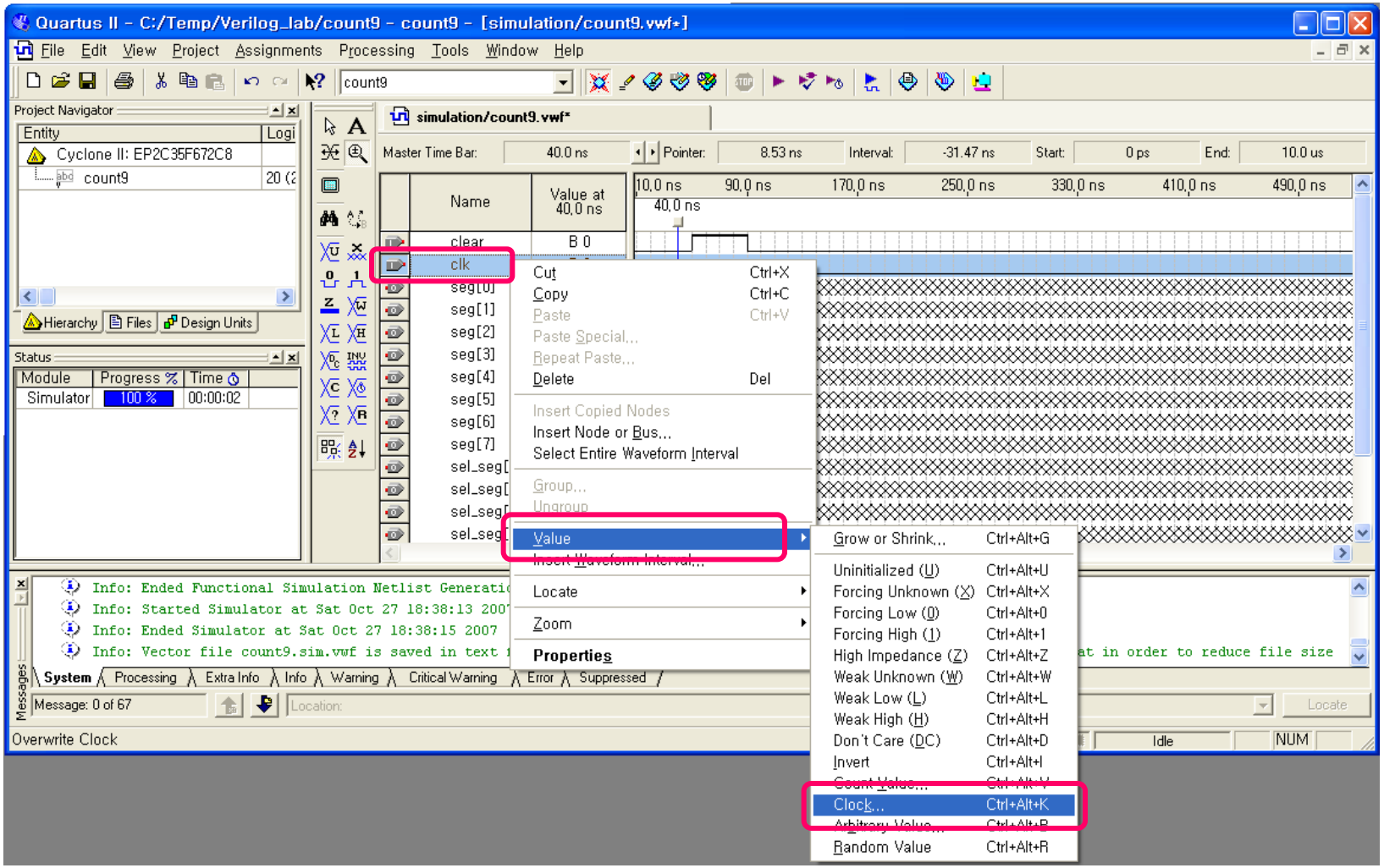
▣ 시뮬레이션 입력파형 생성

◆ 입출력 포트의 로드가 완료된 상태



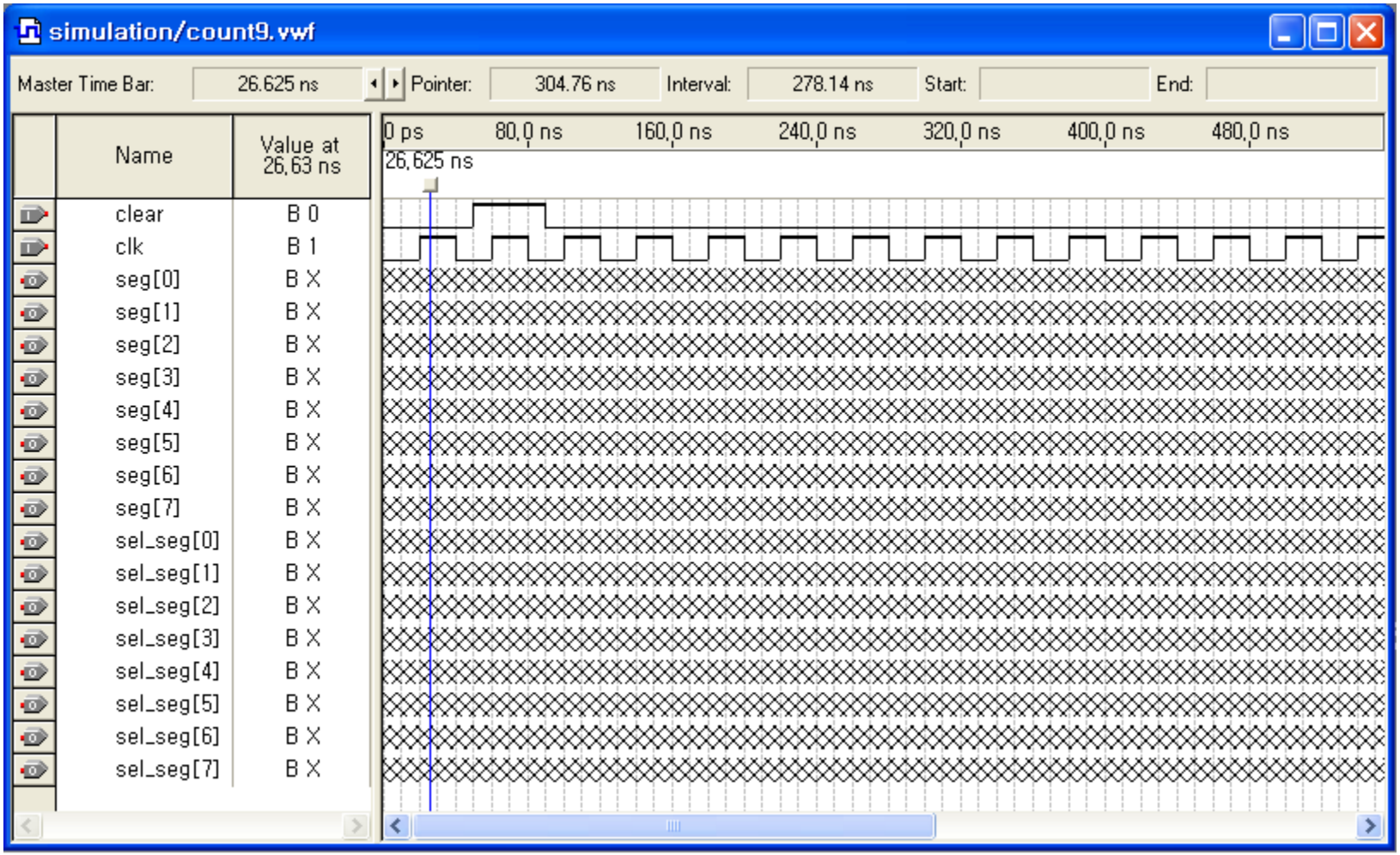
시뮬레이션

◆시뮬레이션 파형 설정



시뮬레이션

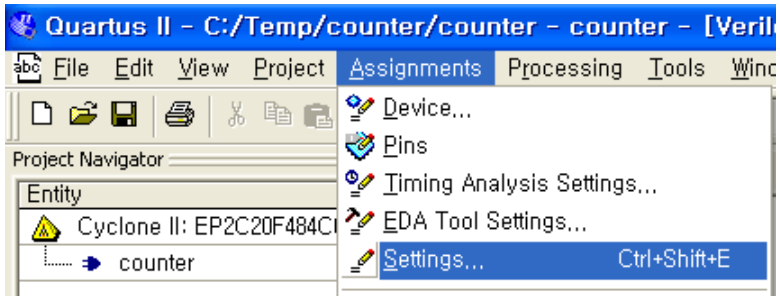
- 시뮬레이션 파형 설정이 완료된 상태

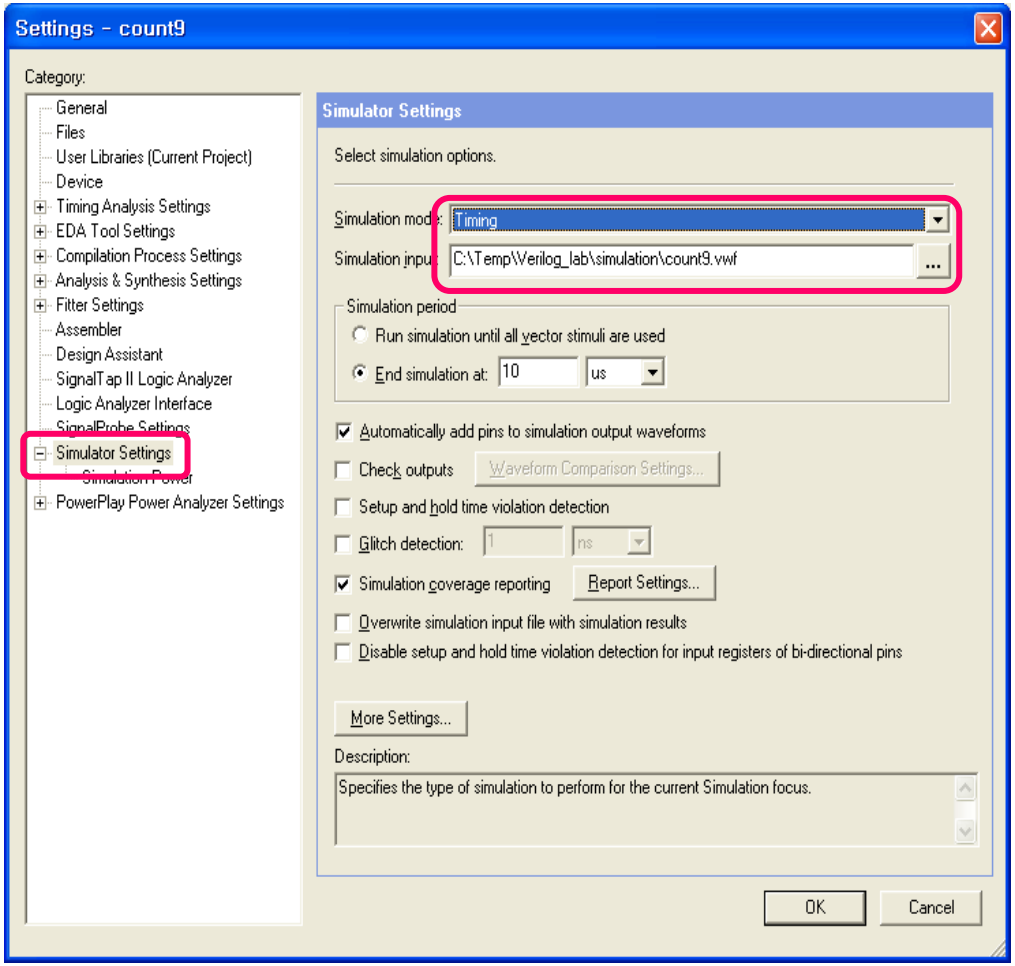


시뮬레이션

▣ 타이밍 시뮬레이션 설정

- ◆ Assignments -> Settings

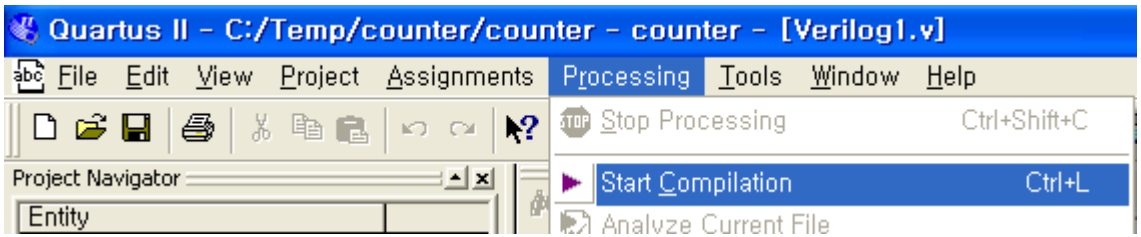




시뮬레이션

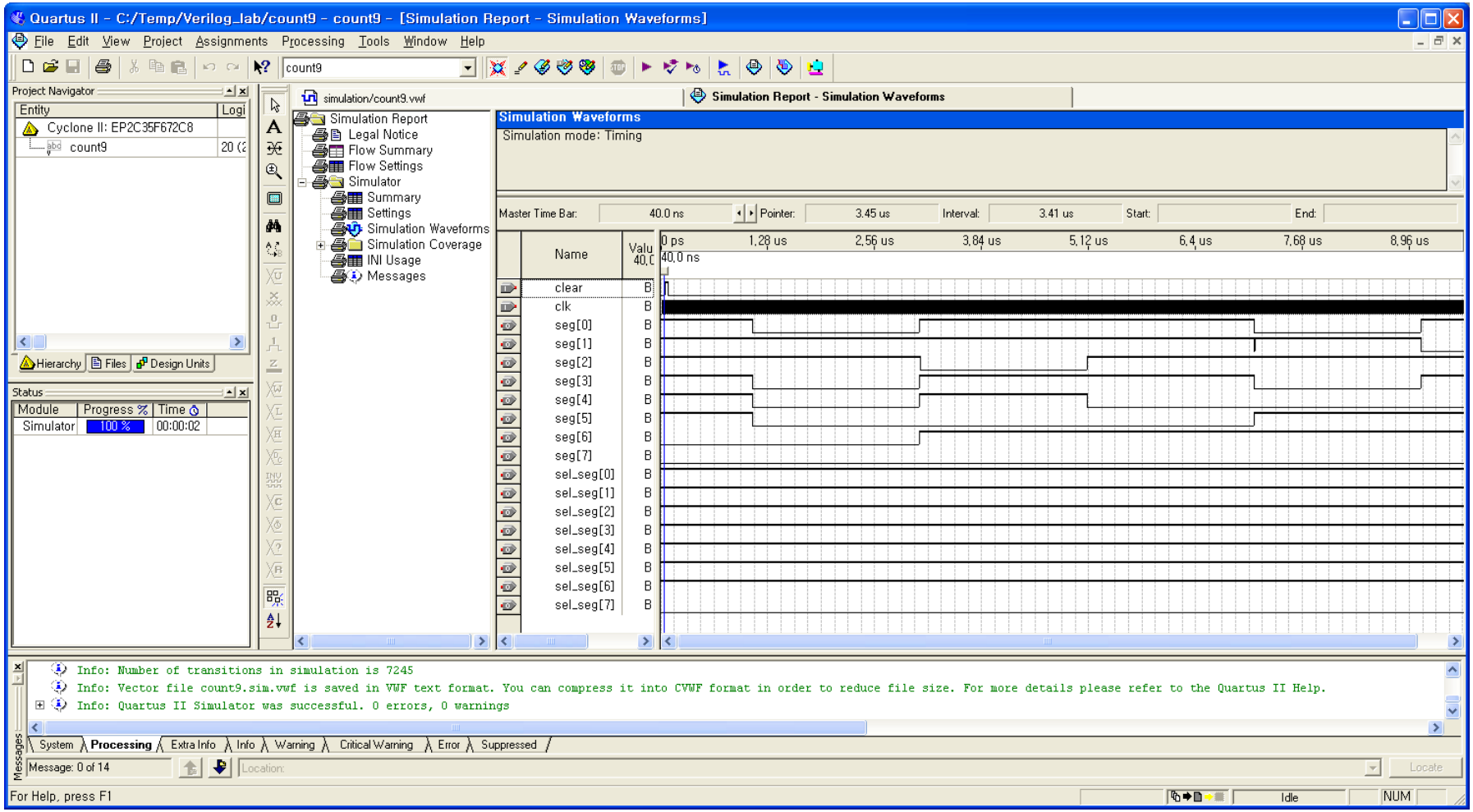
시뮬레이션 실행

- Processing -> Start Simulation



시뮬레이션

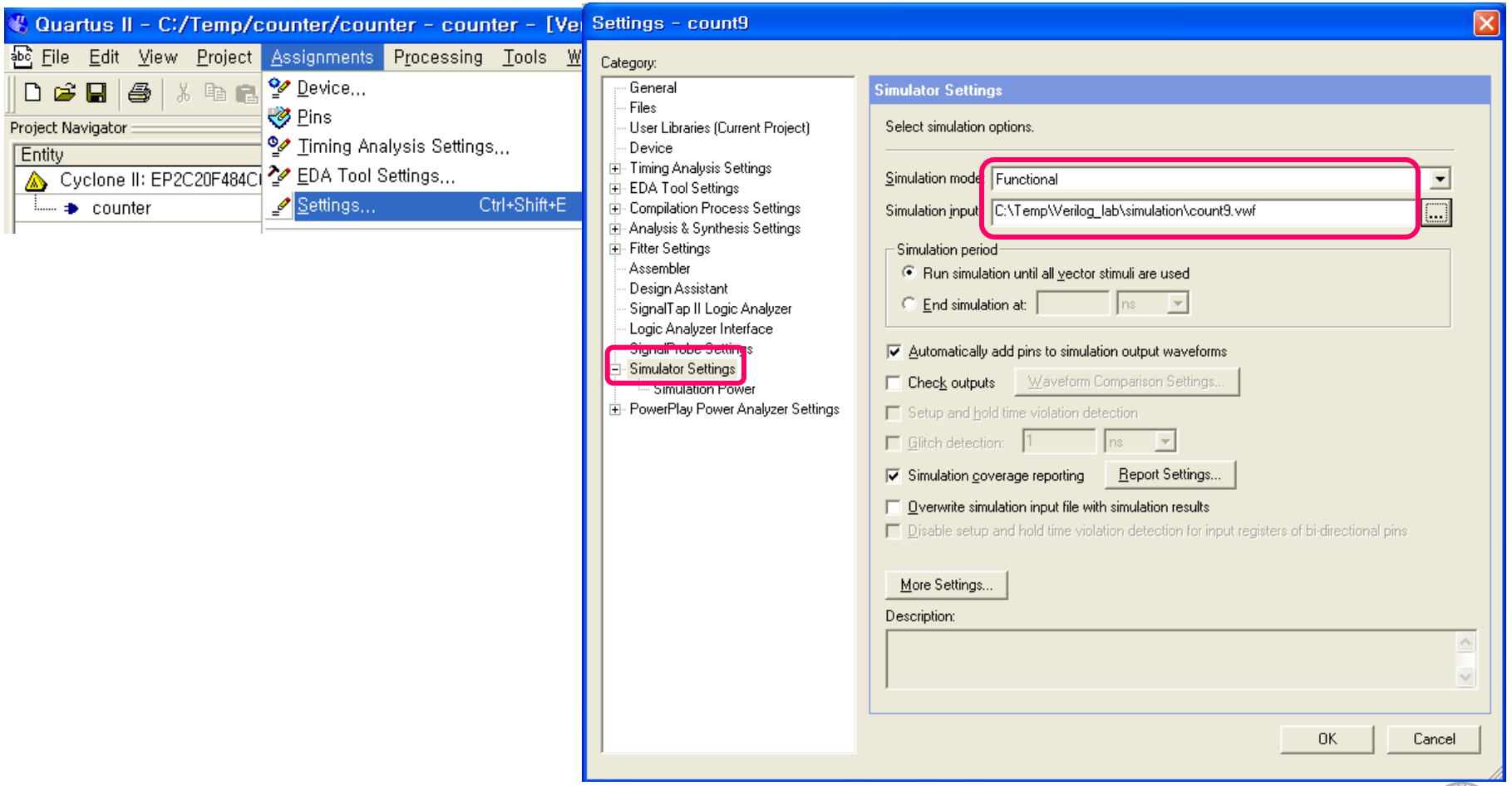
◆시뮬레이션 결과



시뮬레이션

▣ 기능 시뮬레이션 설정

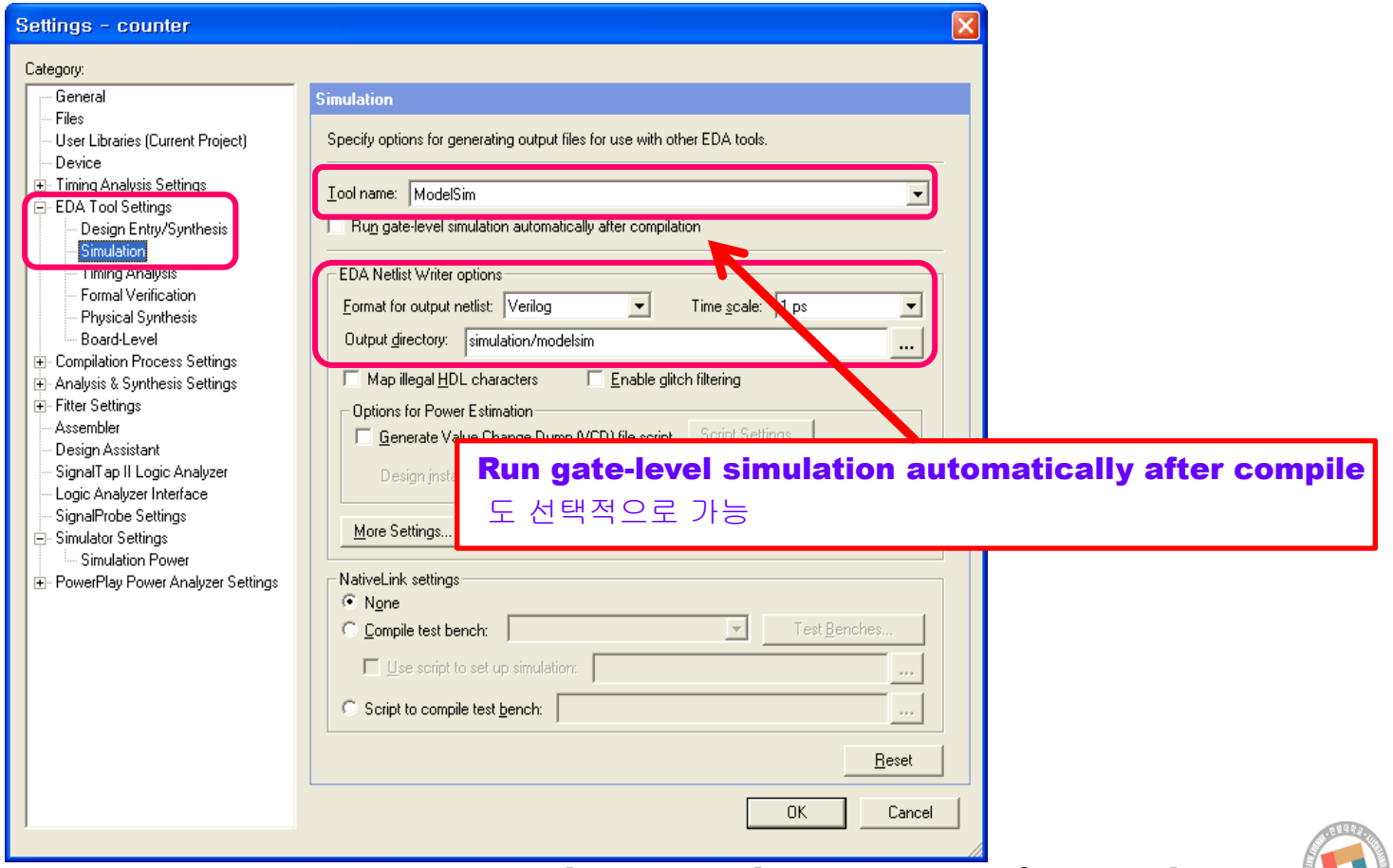
- ◆ Assignments -> Settings



ModelSim을 이용한 시뮬레이션

▣ 시뮬레이터 설정

- ◆ Assignments -> Settings
- ◆ EDA Tool Settings -> Simulation

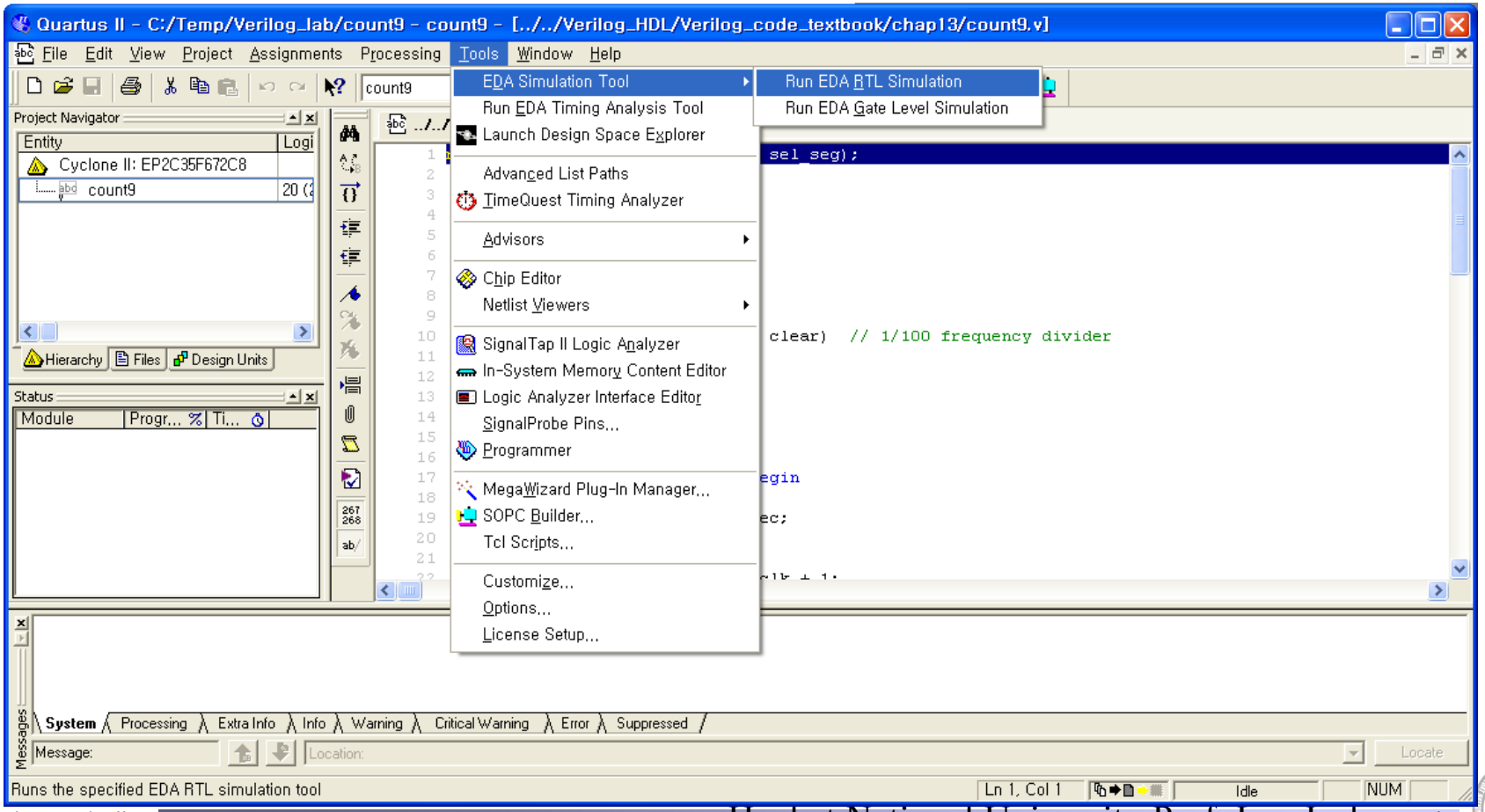


ModelSim을 이용한 시뮬레이션

▣ 시뮬레이터 실행

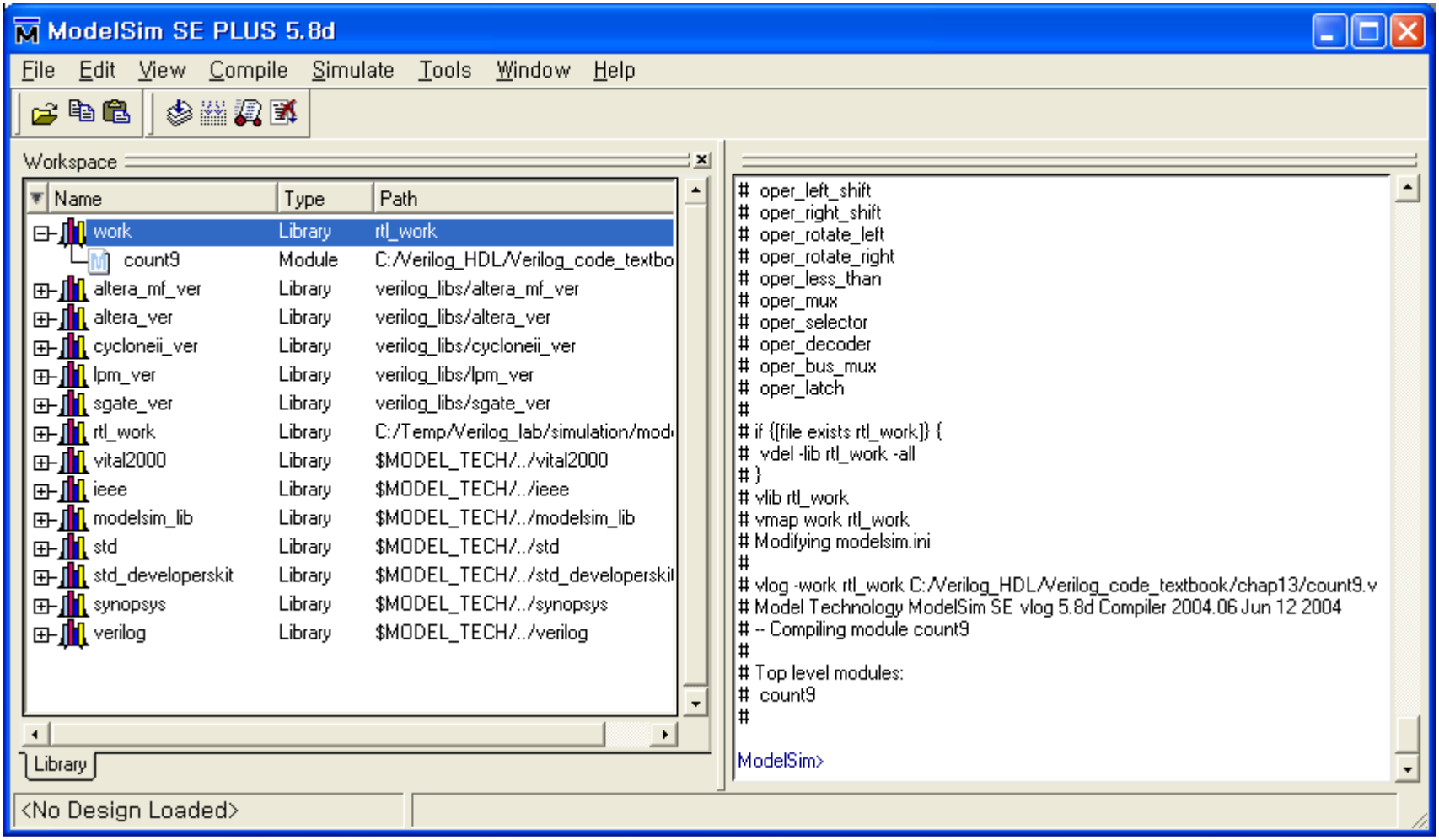
◆ Tools -> EDA Simulation Tool -> Run EDA RTL Simulation

-> Run EDA Gate Level Simulation



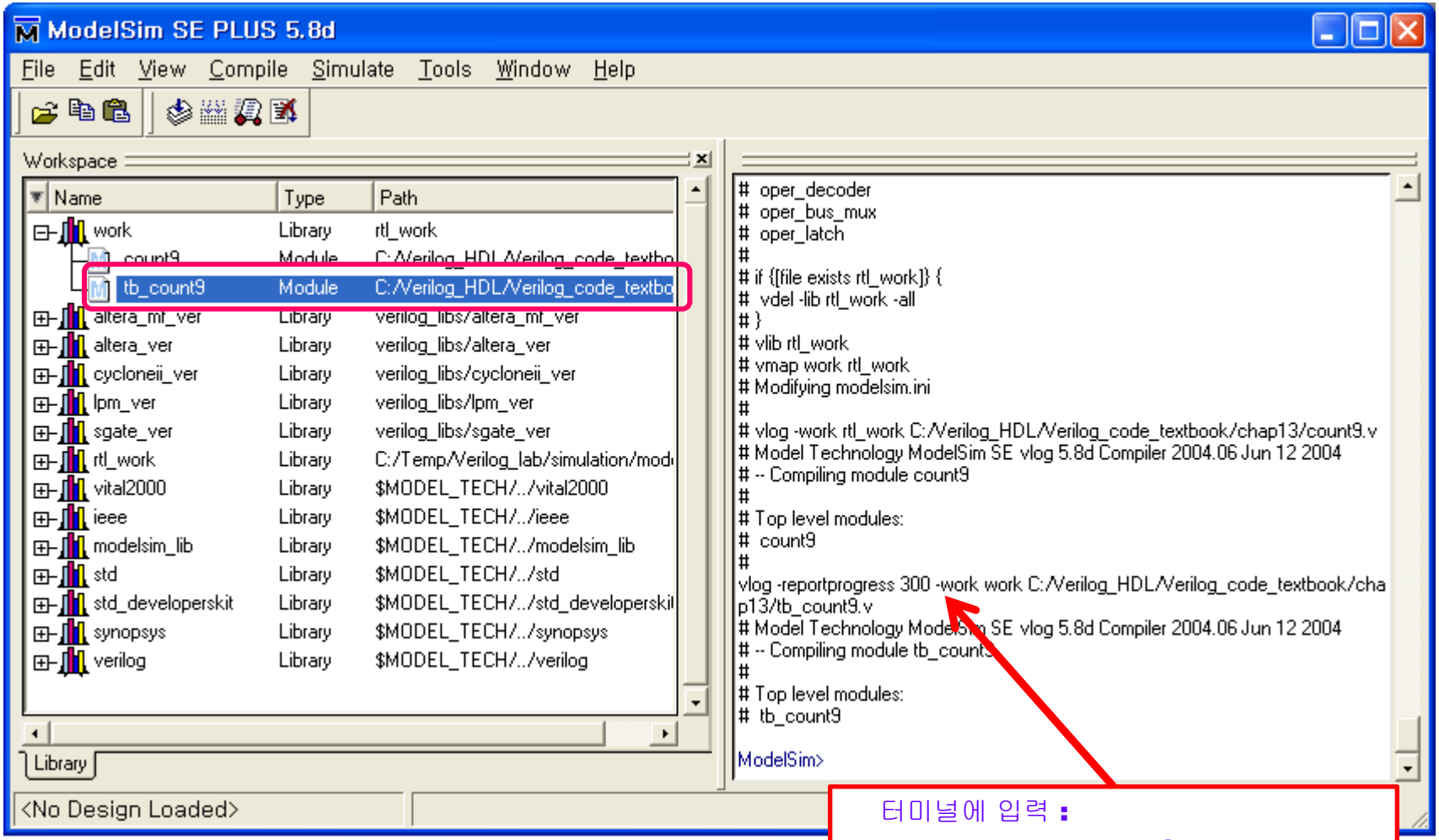
ModelSim을 이용한 시뮬레이션

- ModelSim이 실행된 상태



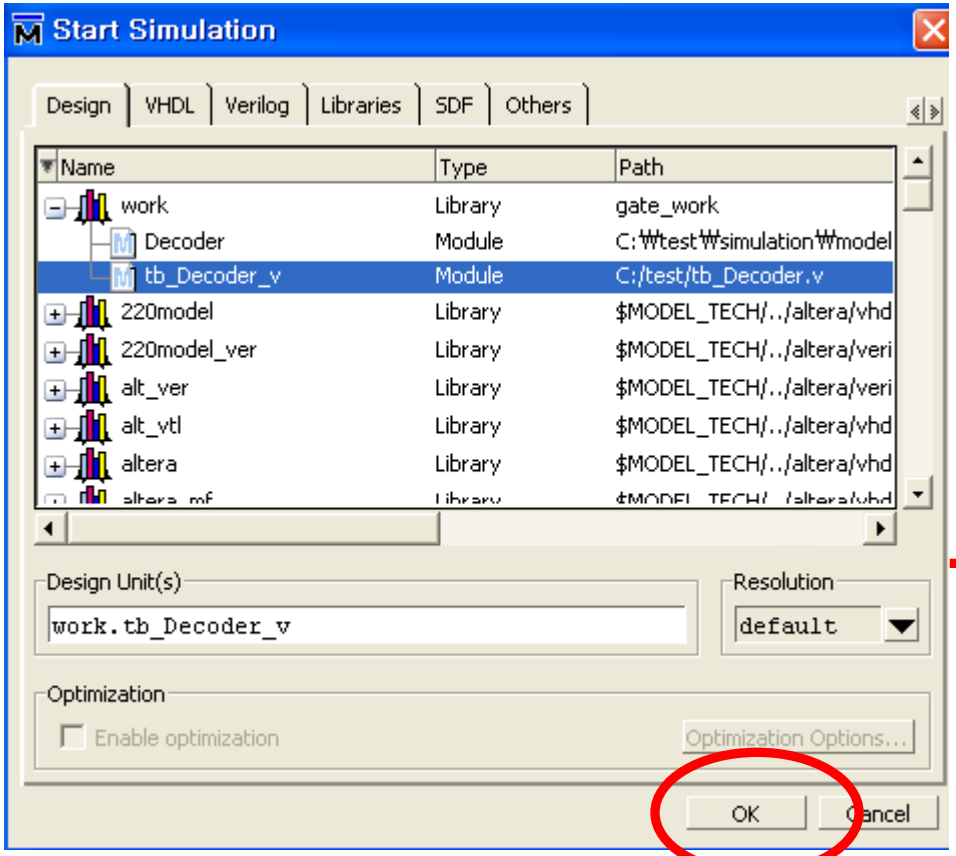
ModelSim을 이용한 시뮬레이션

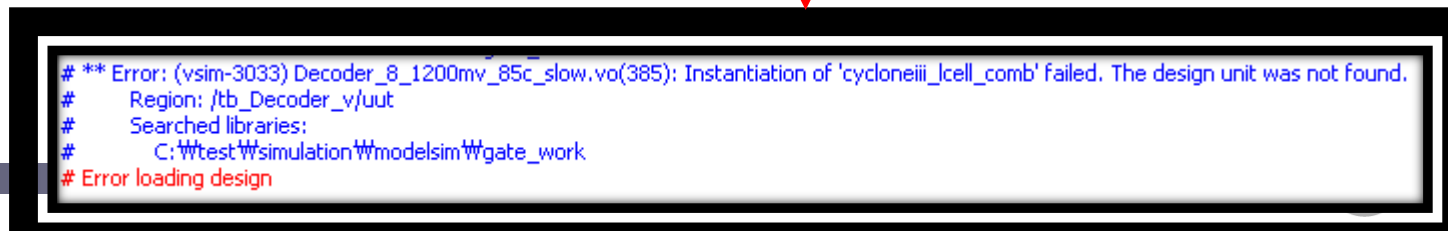
◆기존에 없던 테스트벤치 파일이 컴파일 되어 추가된 상태



Gate Level 시뮬레이션 시 문제 해결

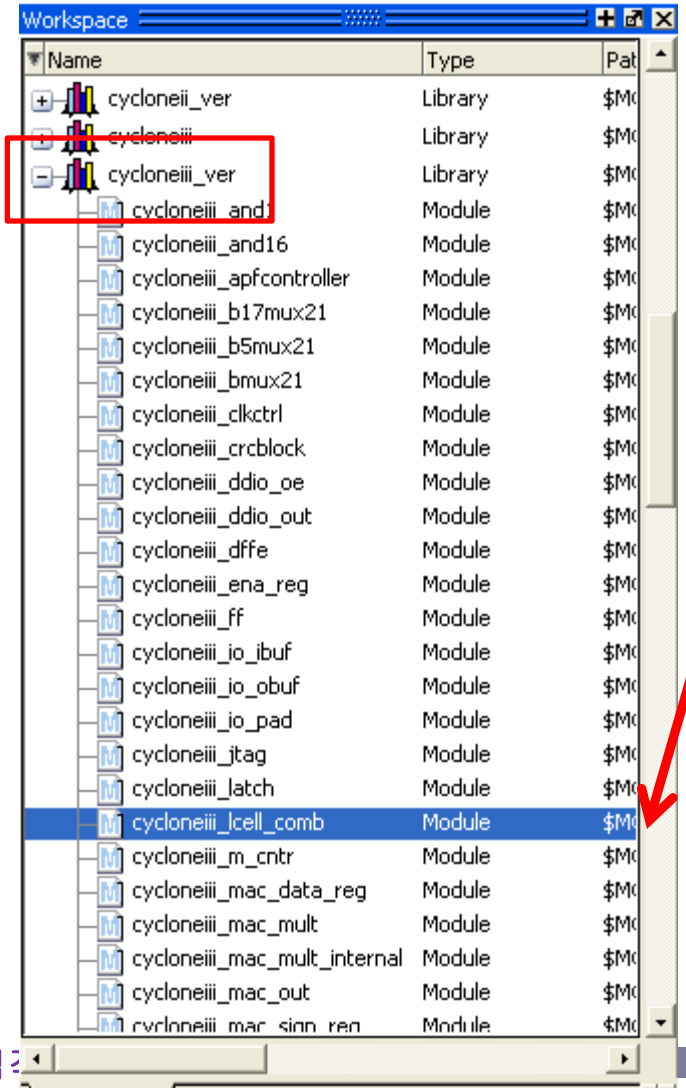
▣ 라이브러리 찾지 못하는 에러 발생



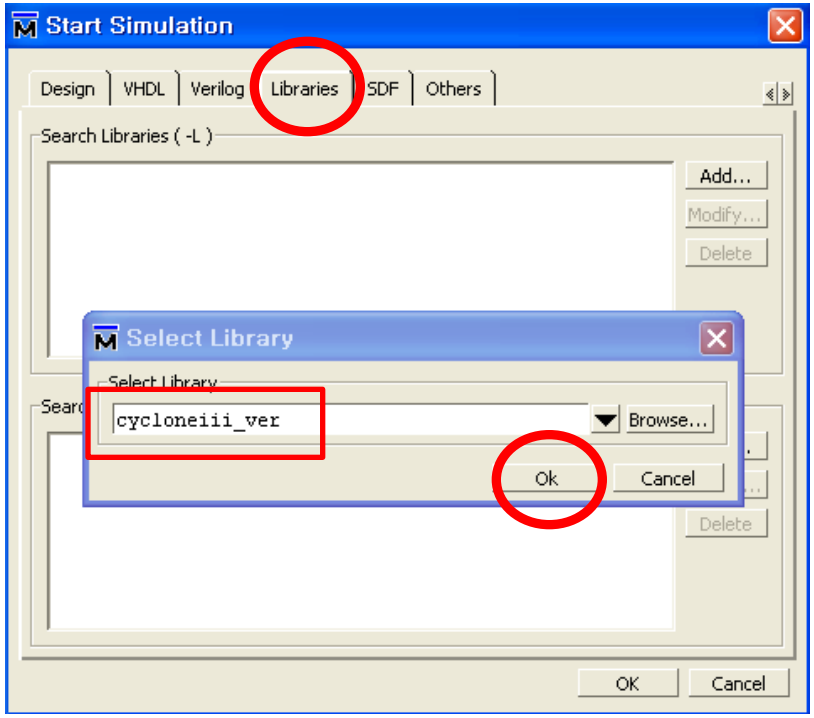


Gate Level 시뮬레이션 시 문제 해결

▣ 라이브러리 찾지 못하는 에러 발생

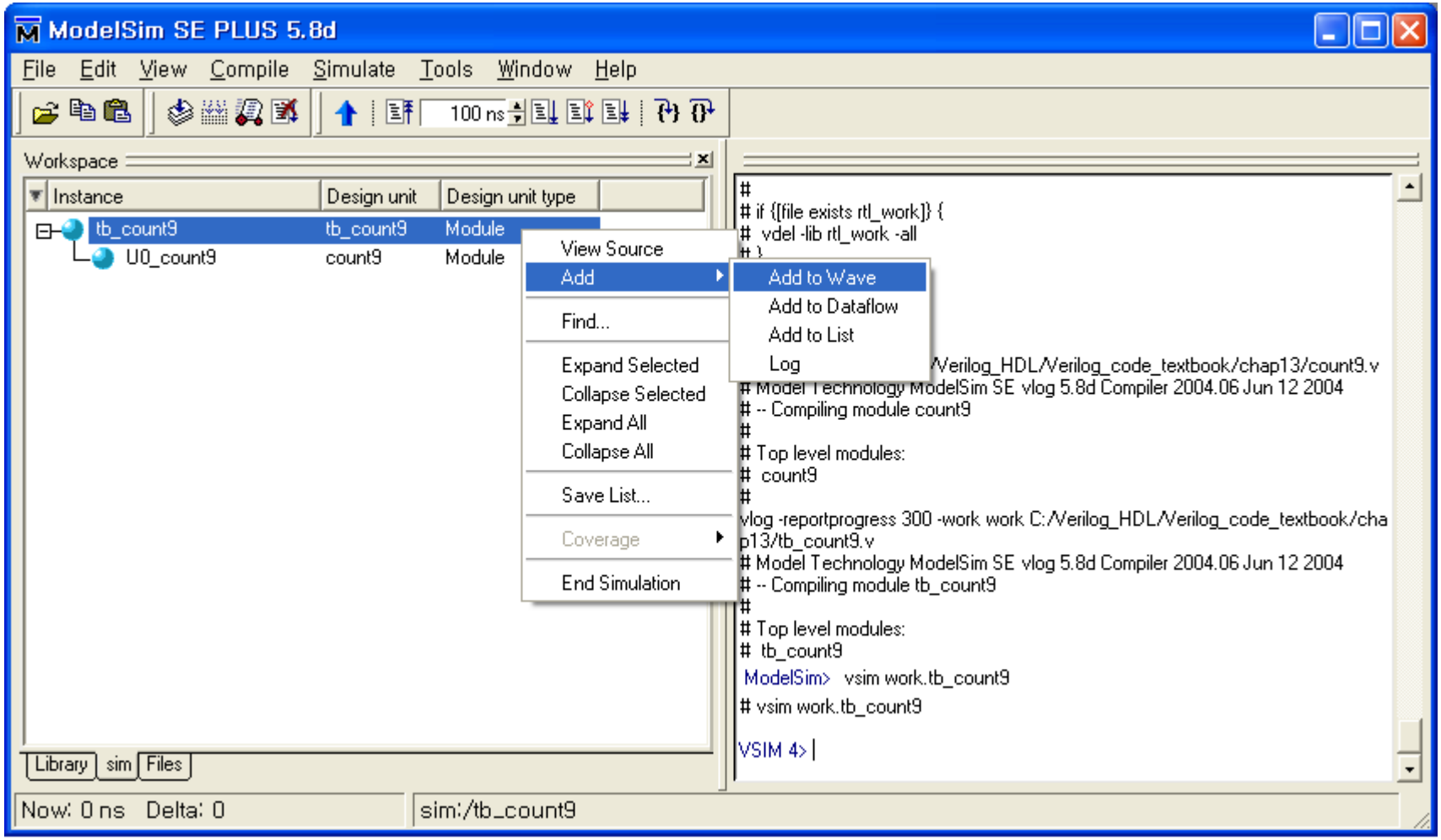


그럼 처럼 **work space**에서
해당 라이브러리 존재함을 확인



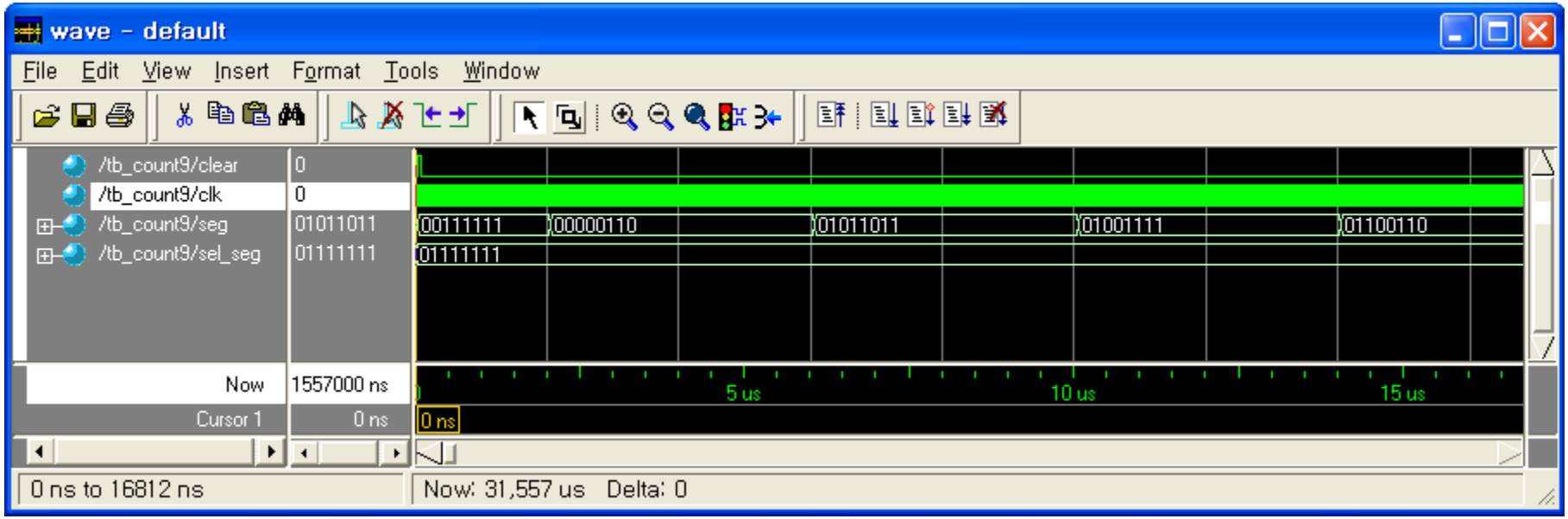
ModelSim을 이용한 시뮬레이션

- Waveform 창에 신호 추가하기



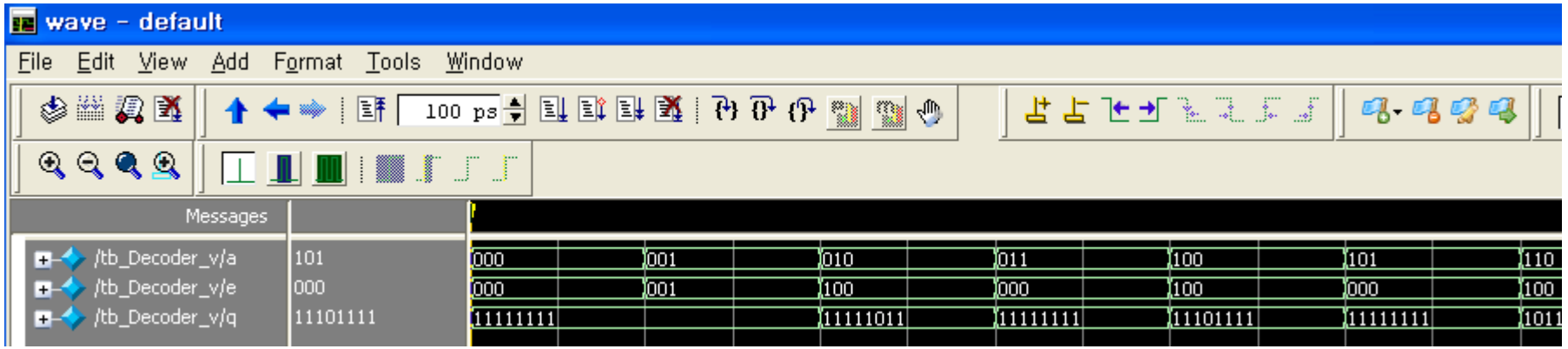
ModelSim을 이용한 시뮬레이션

- ModelSim 시뮬레이션 결과

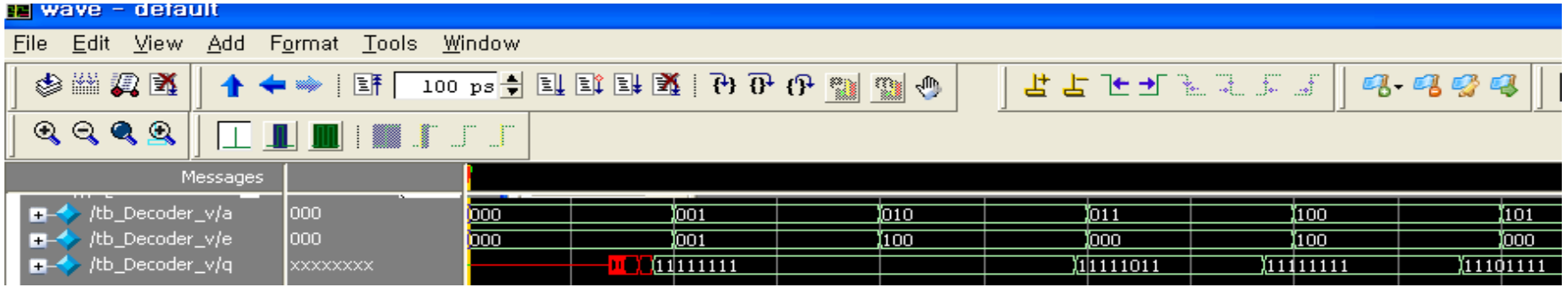


ModelSim을 이용한 시뮬레이션

- Functional 한 RTL 시뮬레이션 결과



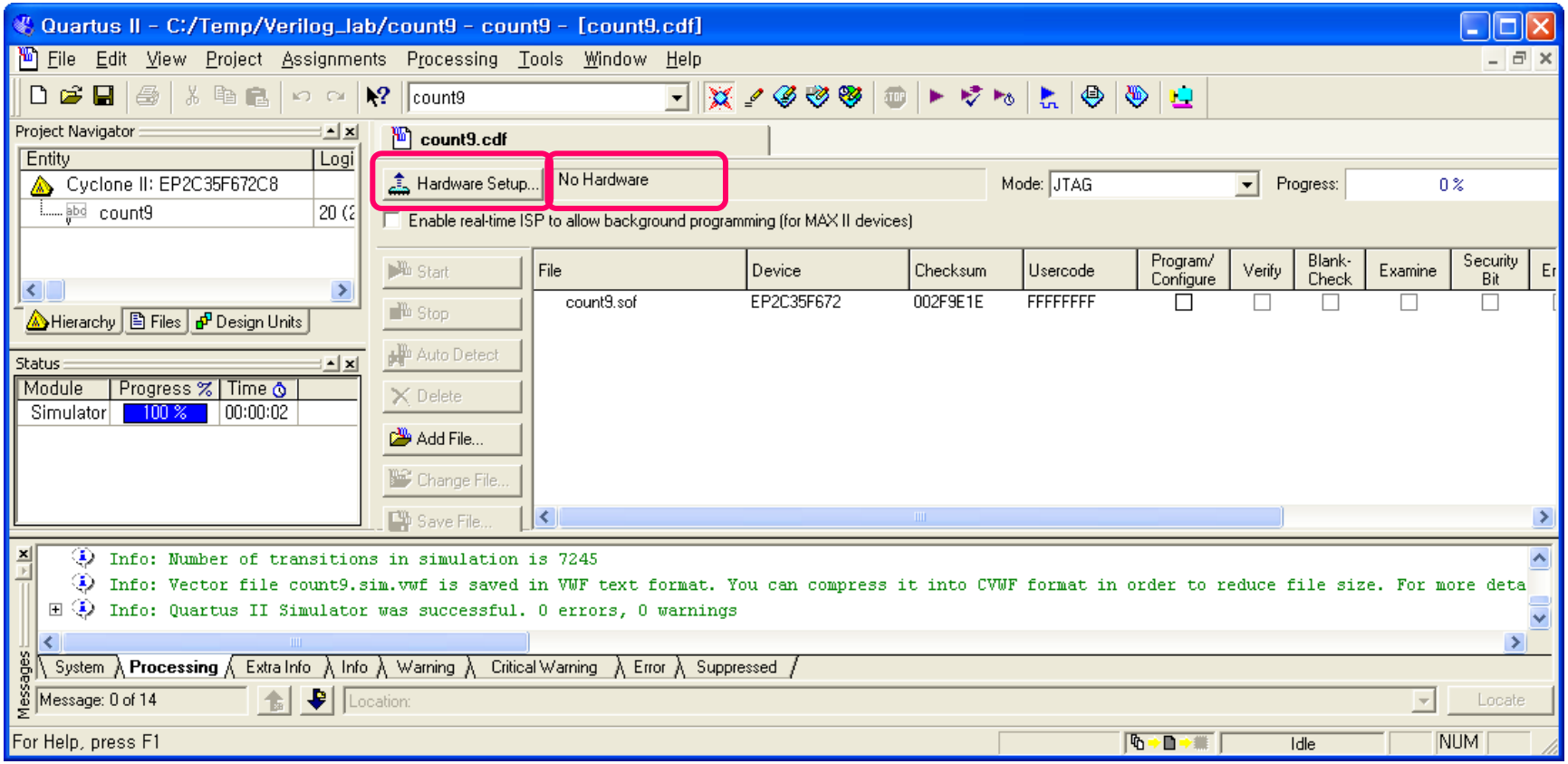
- Gate-level 시뮬레이션 결과 : 실제 Gate 의 계산 결과 시간을 확인 가능



디바이스 프로그래밍

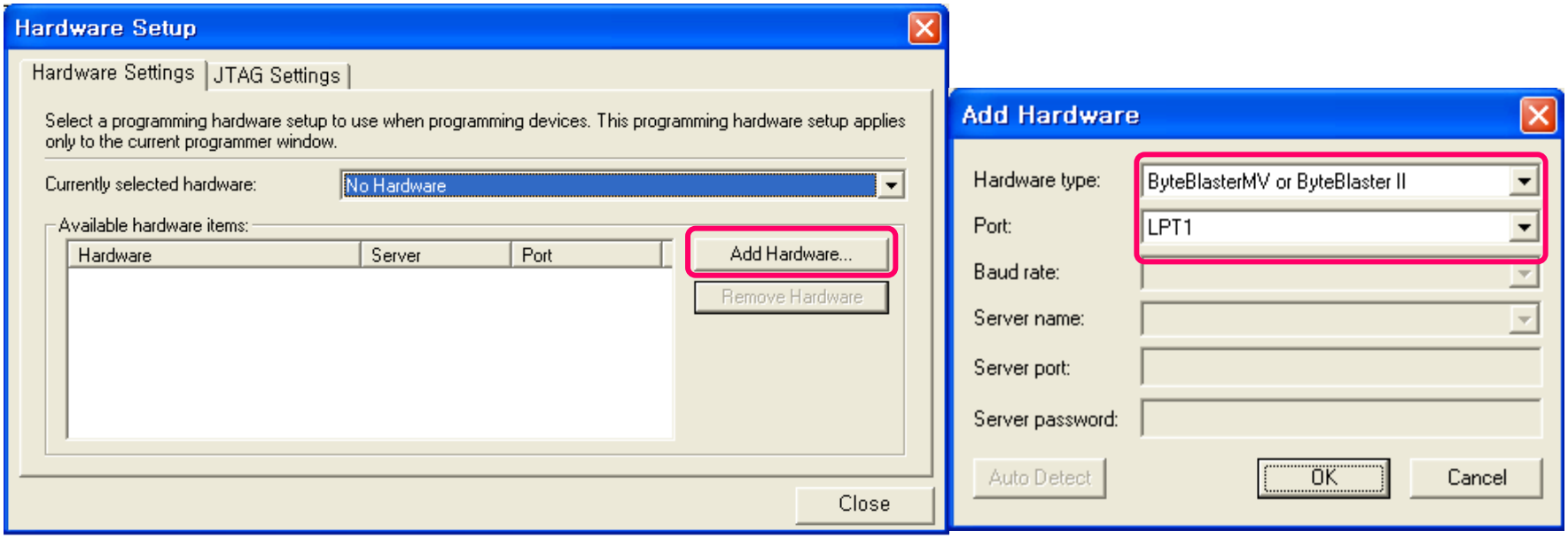
▣ 프로그래밍 하드웨어 설정

- ◆ Tools -> Programmer -> Hardware Setup



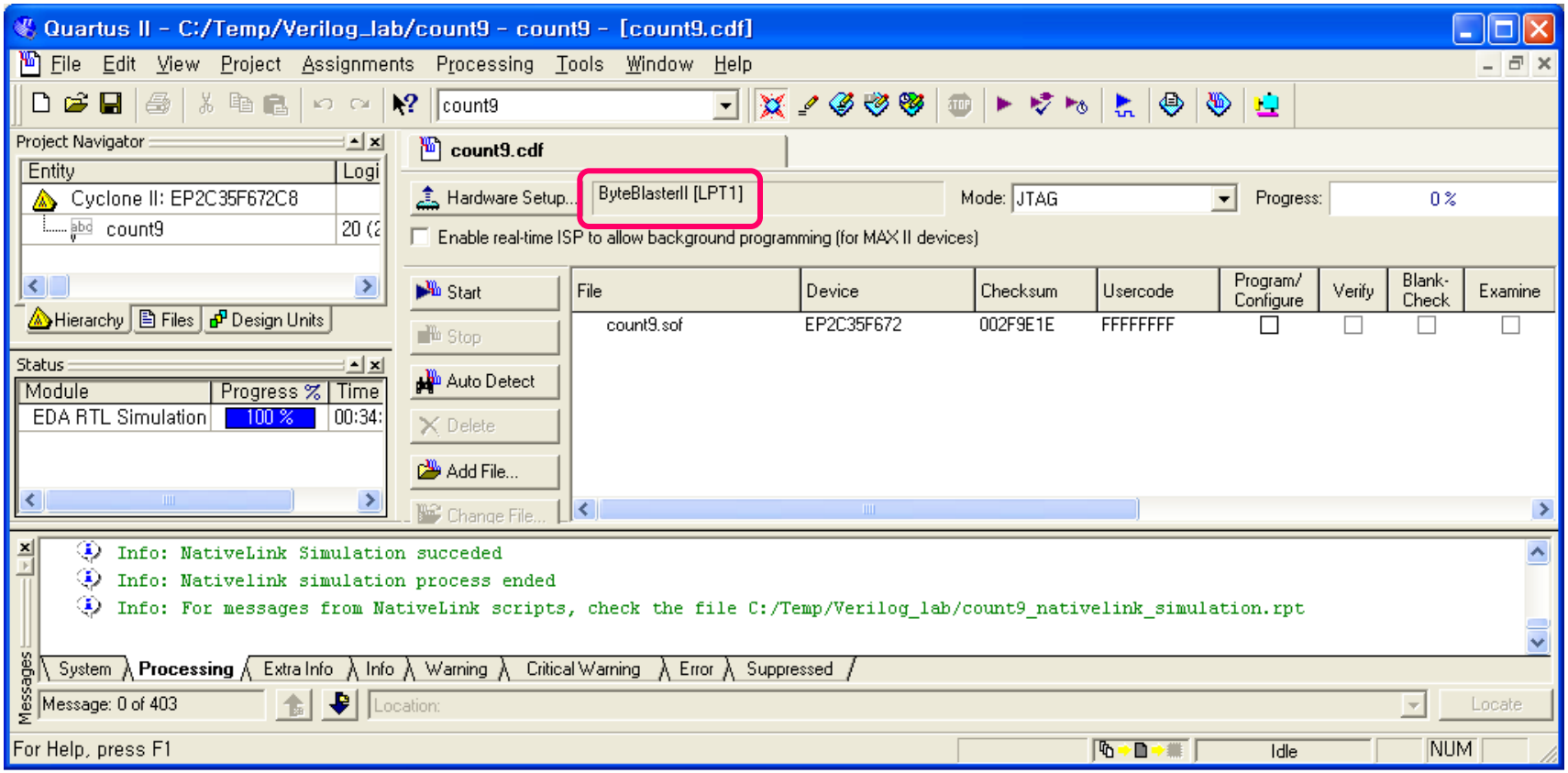
디바이스 프로그래밍

▣ 프로그래밍 하드웨어 설정



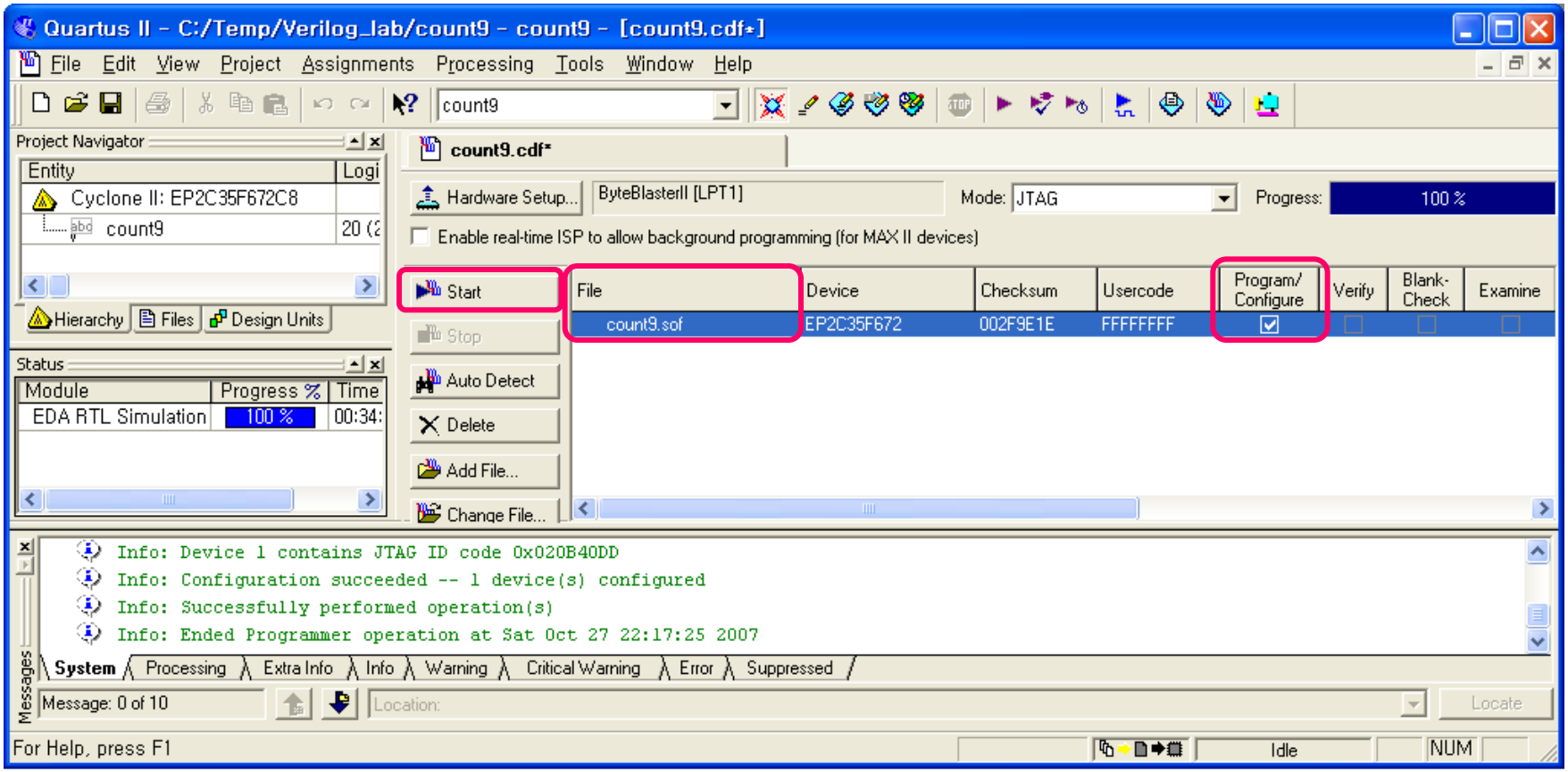
디바이스 프로그래밍

▣ 프로그래밍 하드웨어 설정이 완료된 상태



디바이스 프로그래밍

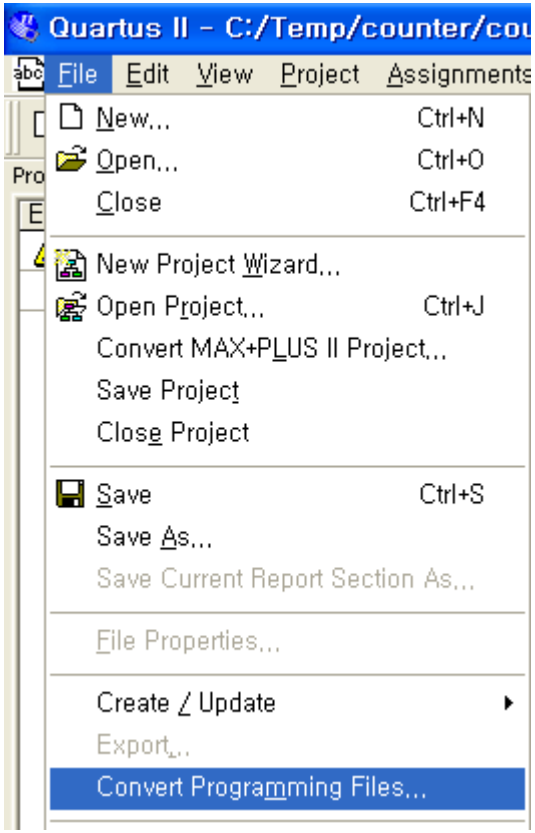
▣ 디바이스 프로그래밍



디바이스 프로그래밍

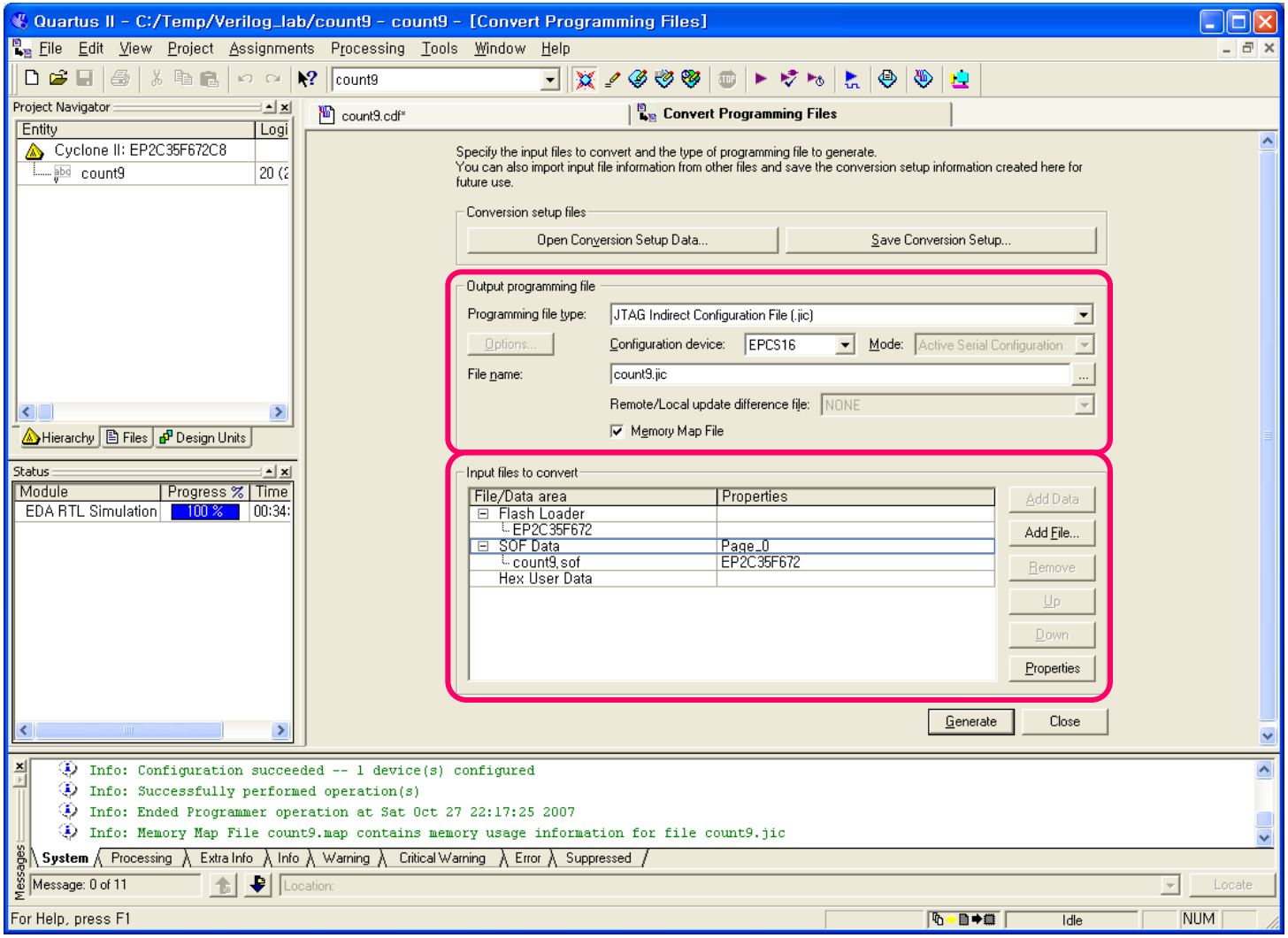
▣ PROM 프로그래밍

- ◆ File -> Convert Programming Files



디바이스 프로그래밍

- .sof 파일을 .jic 파일로 변환



디바이스 프로그래밍

- PROM 프로그래밍