



Altera Quartus II를 이용한 설계 구현

한밭대학교 반도체 설계실

Sun, Hye-Seung



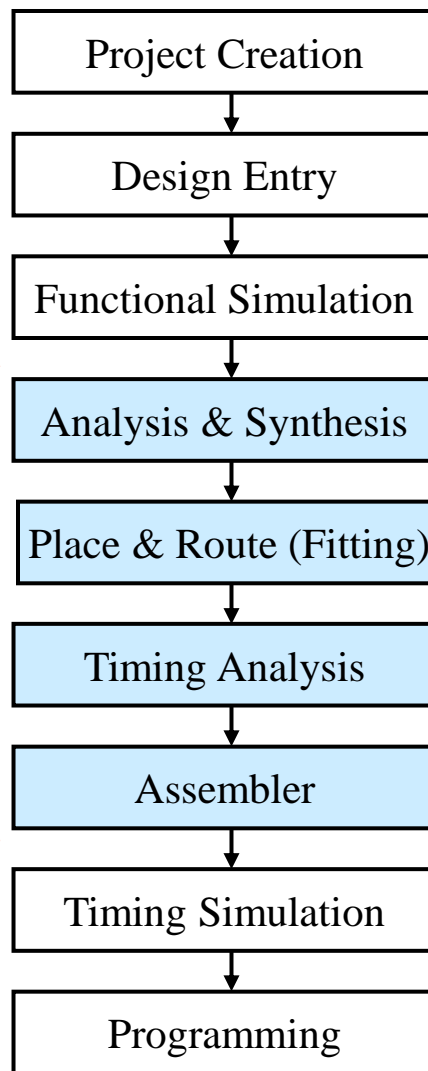


Quartus II 설계 흐름

Front End(합성)
Back End(P&R)
모두 수행

full compile (합성+P&R)

후에 실제 **Gate delay** 정보 산출



functional
RTL 시뮬레이션



Quartus II
Compiler
modules



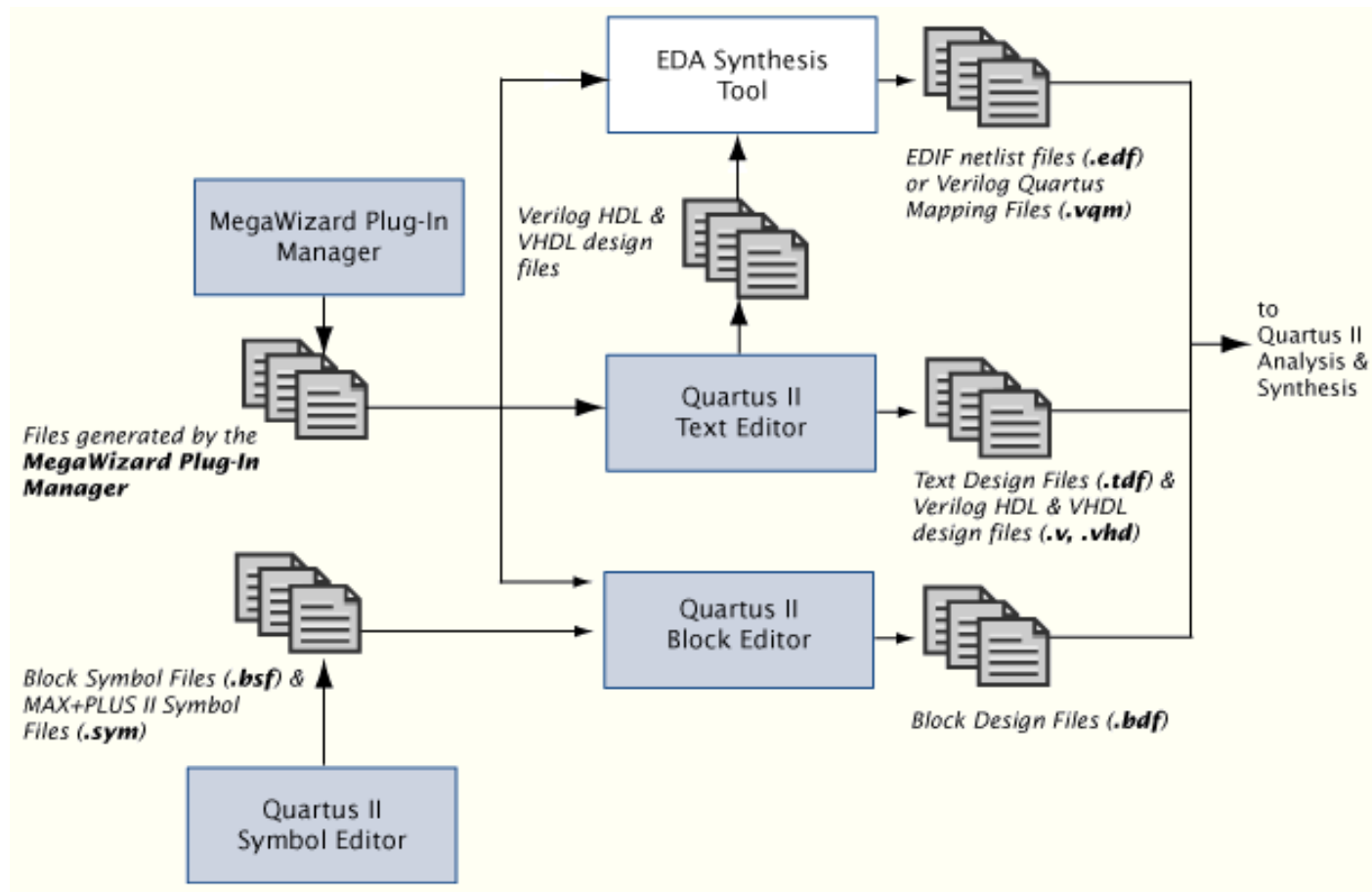
Gate level
시뮬레이션

Gate의 **delay**는
고려 없이
function만 검증

Gate의 실제**delay**를
고려하여 실제 동작이
FPGA에서 동작가능한지를
검증

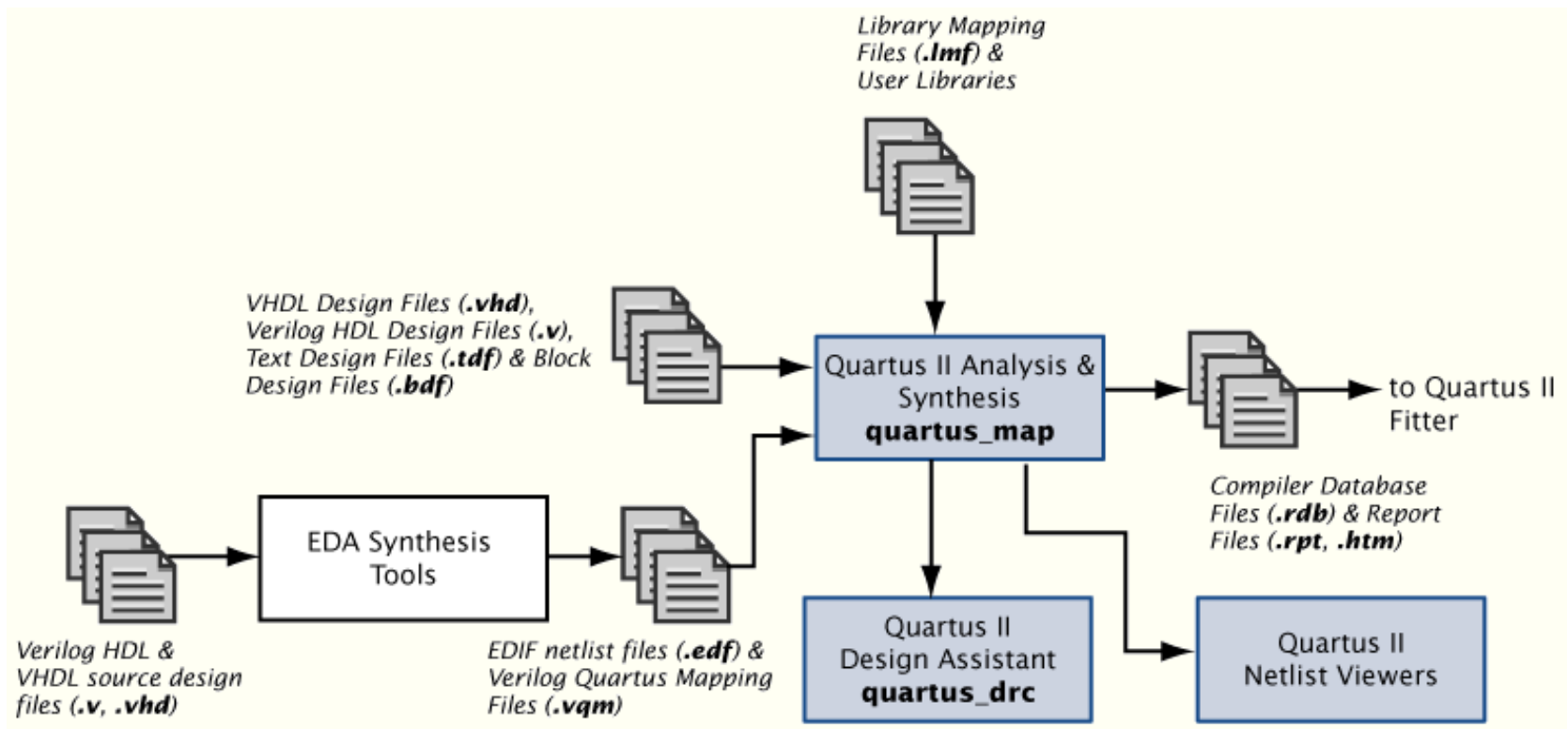


Quartus II 설계입력



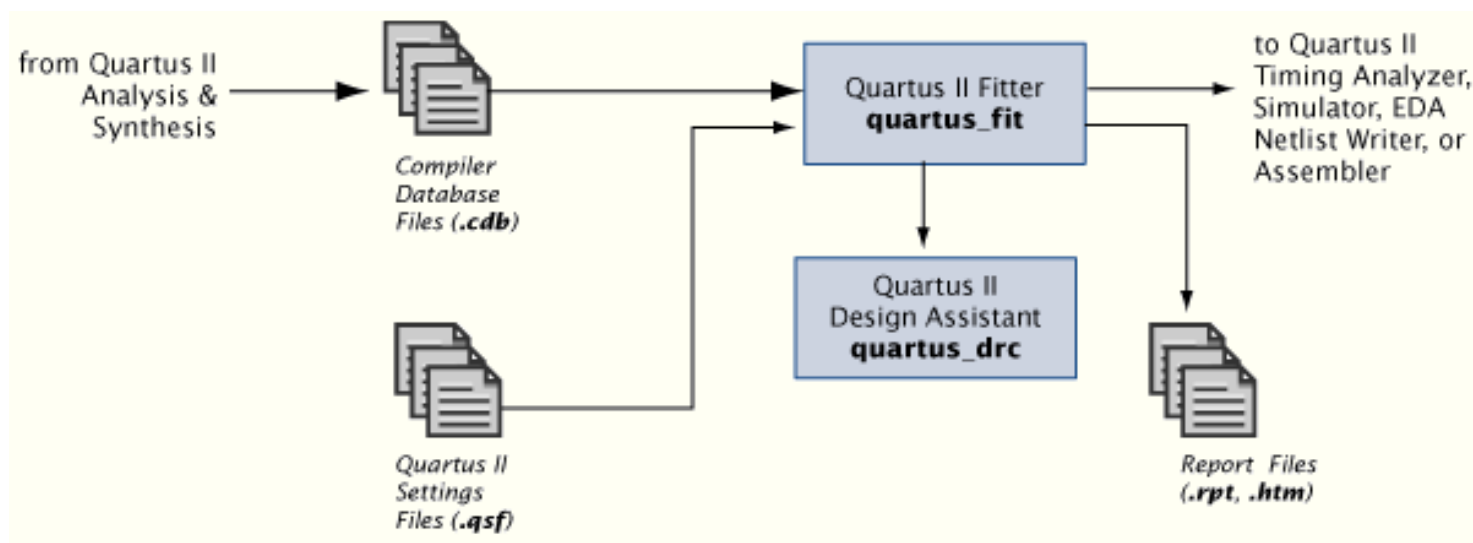


Quartus II 설계합성



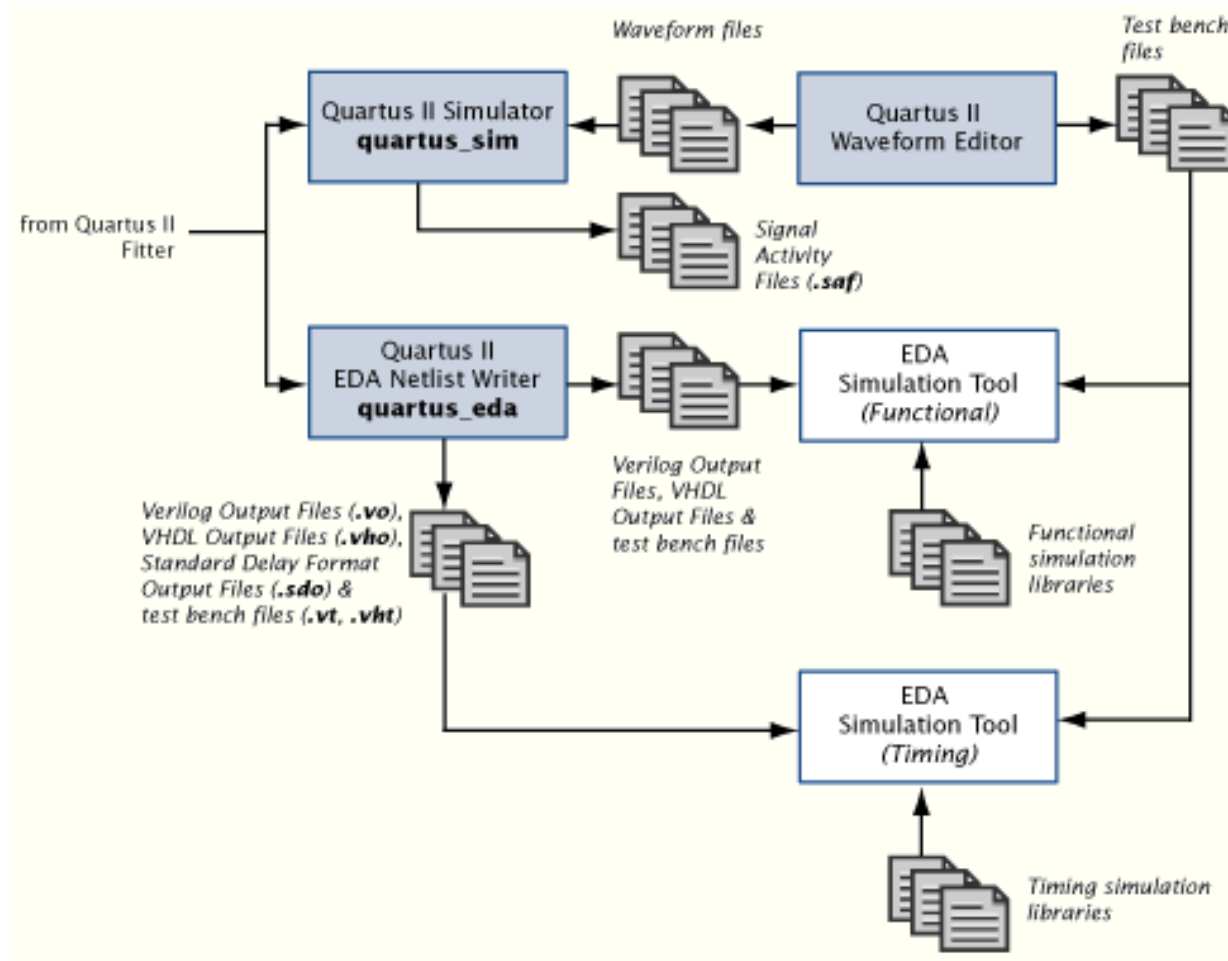


Quartus II Place & Route



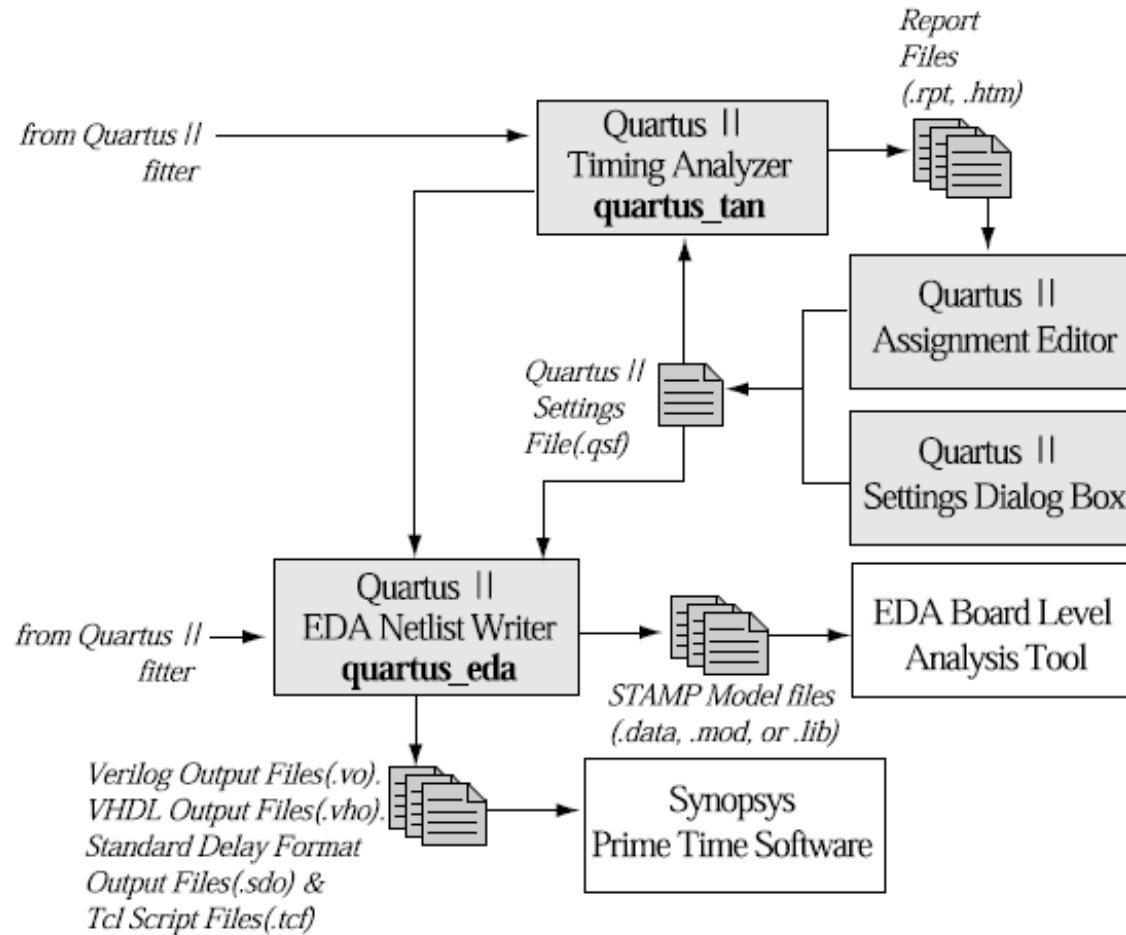


Quartus II 시뮬레이션



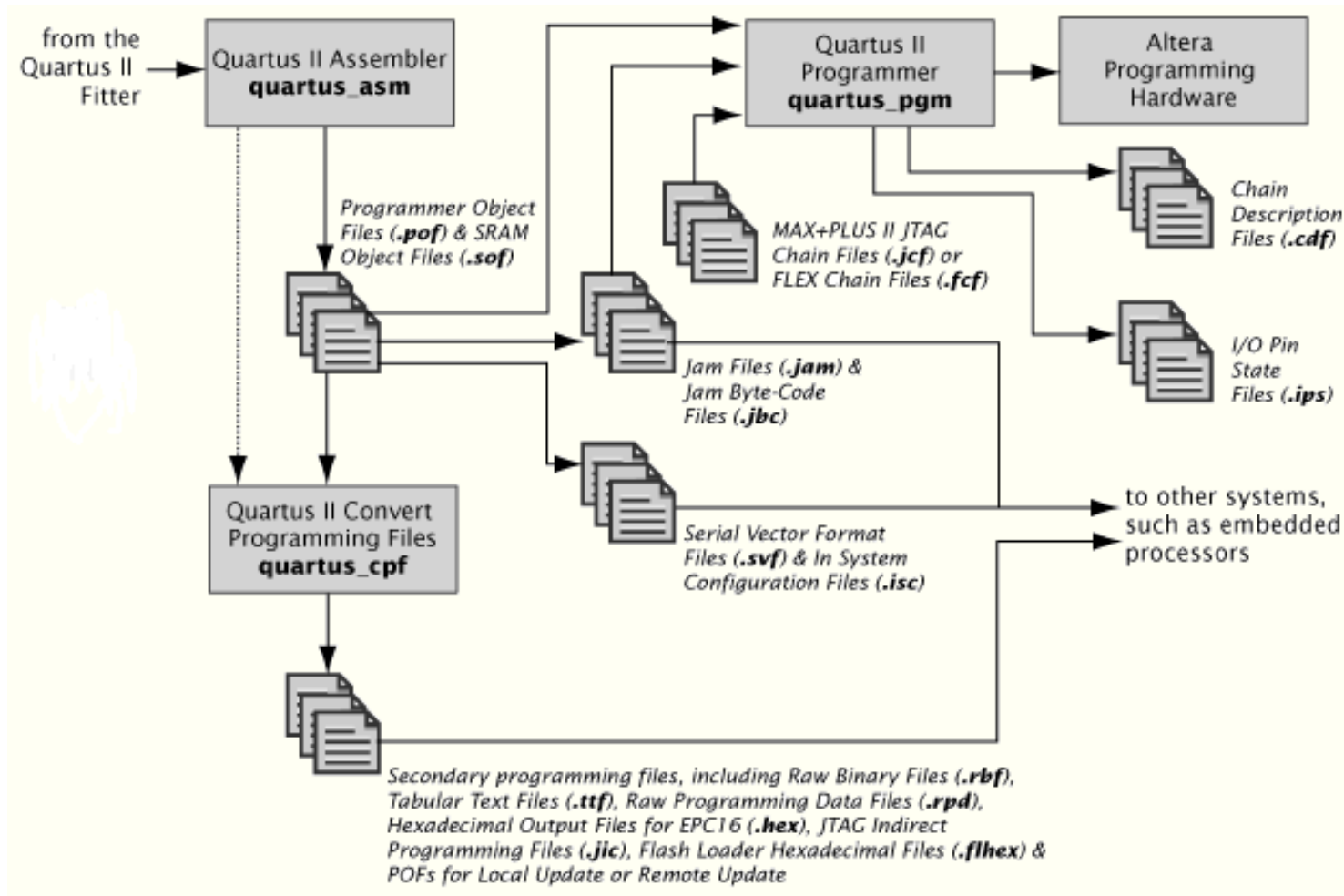


Quartus II 타이밍 분석



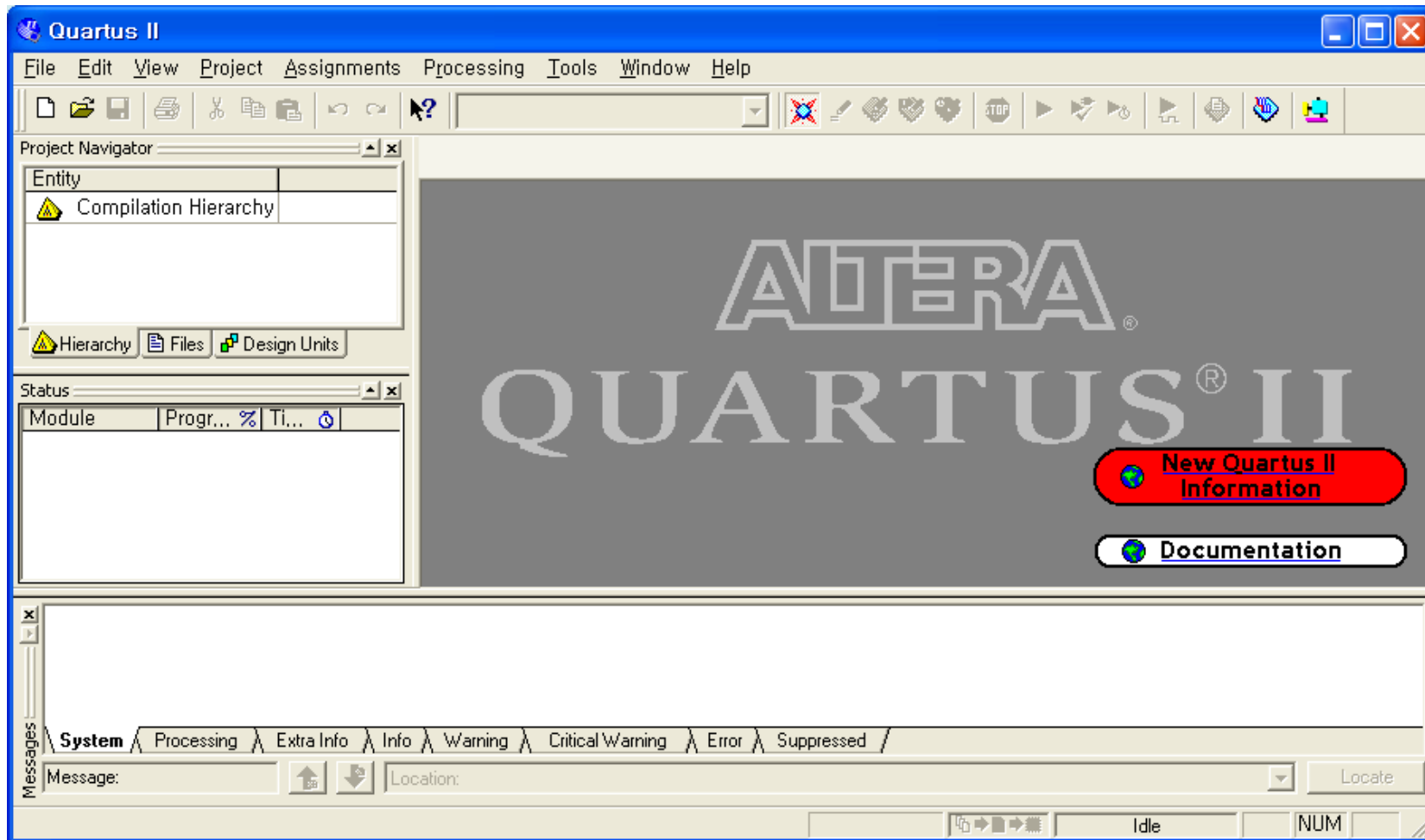


Quartus II 디바이스 프로그래밍





Quartus II 메인 화면

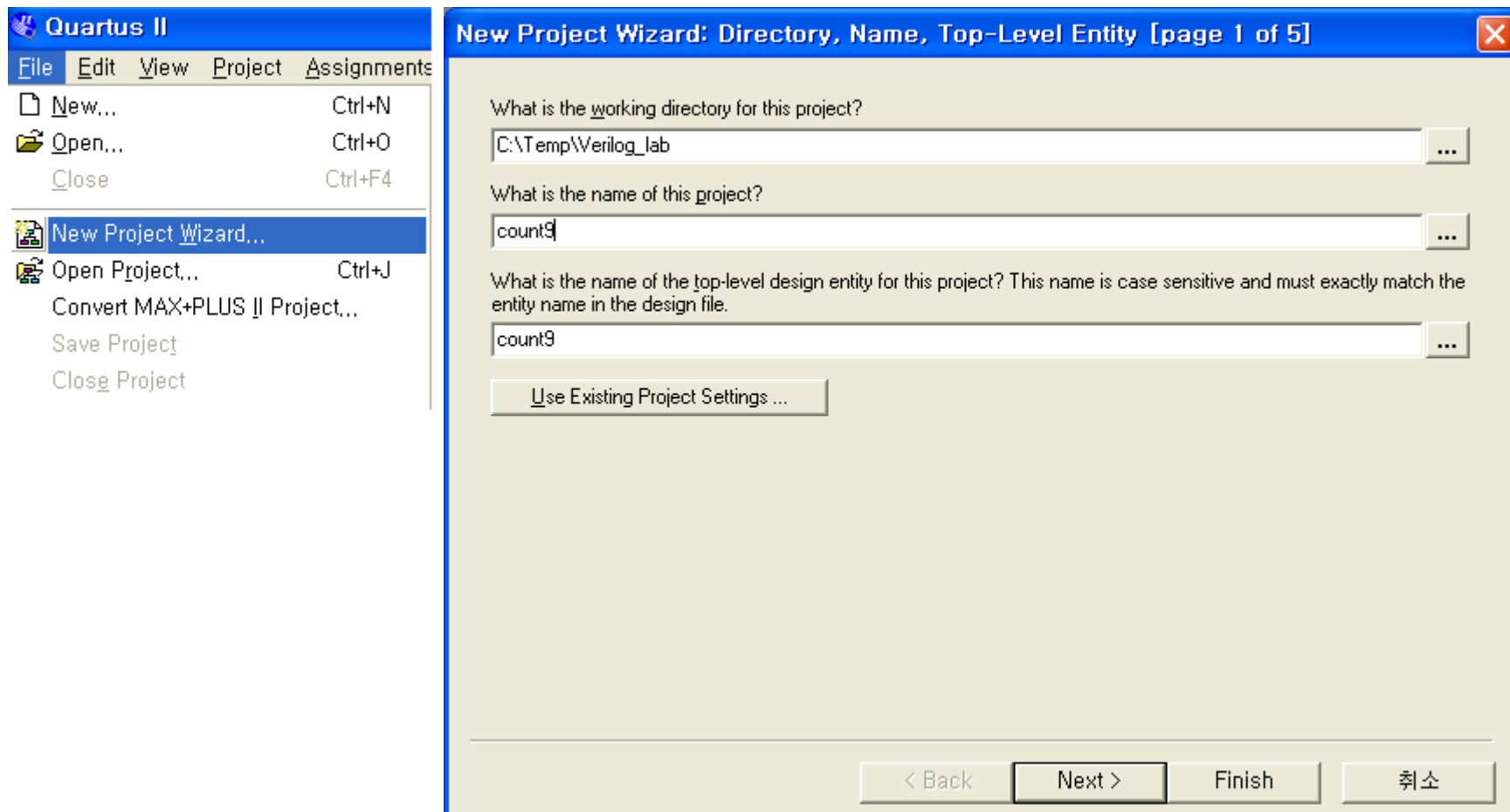




프로젝트 생성

□ File -> New Project Wizard를 선택

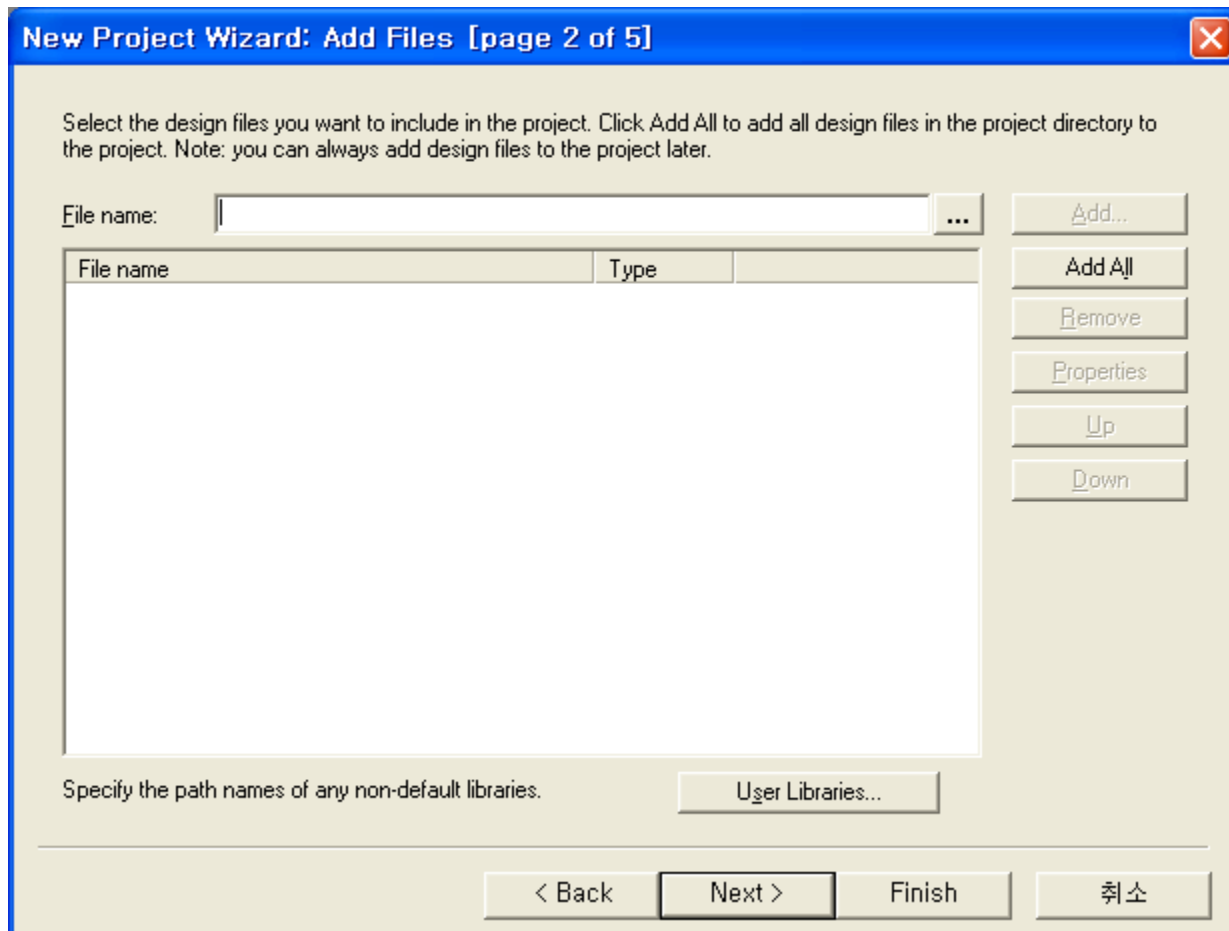
◆ Working directory, Project Name, Top-Level Design entity 등을 설정





프로젝트 생성

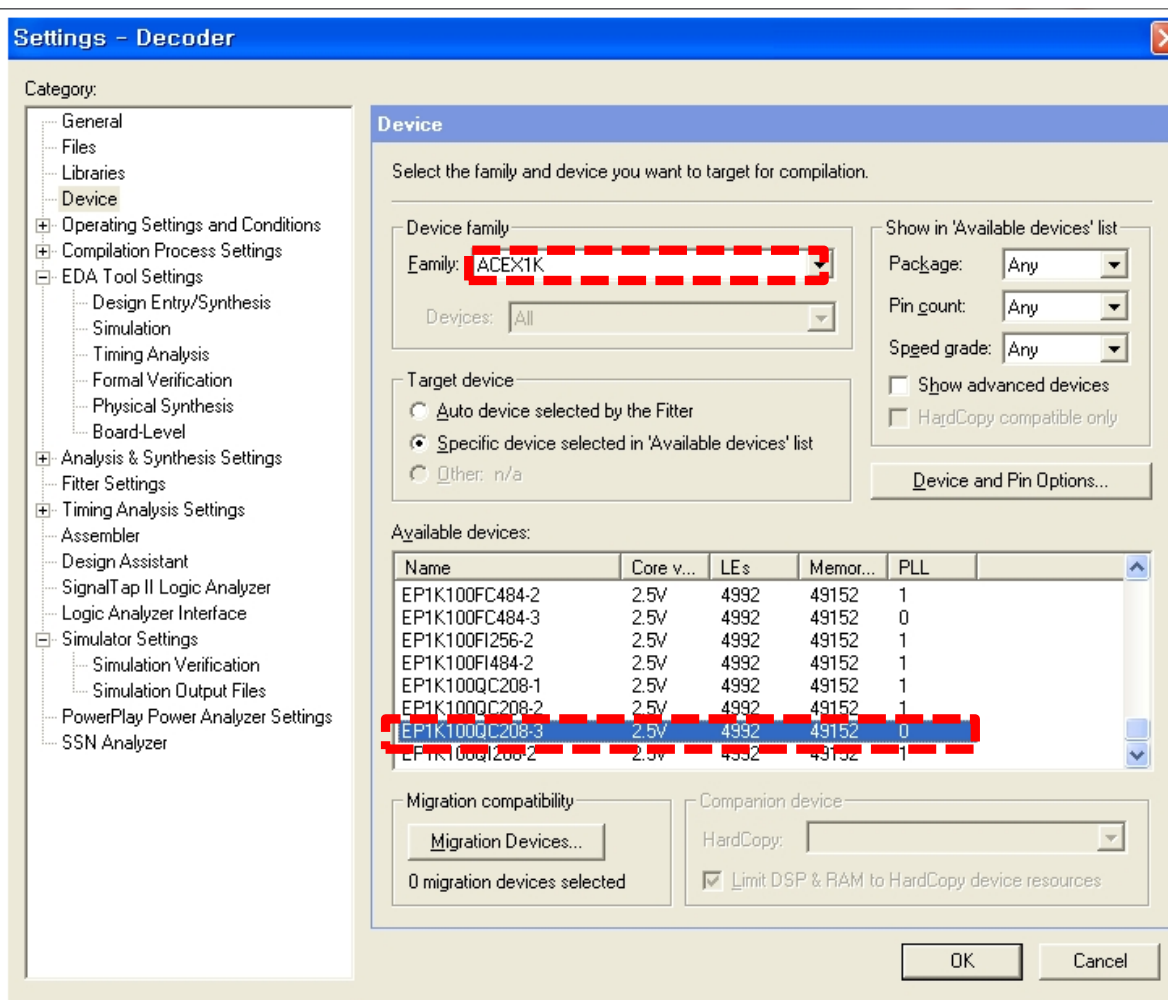
◆ Add Files 대화창





프로젝트 생성

◆ Family & Device Settings 대화창





프로젝트 생성

◆ EDA Tools Settings 대화창

New Project Wizard: EDA Tool Settings [page 4 of 5]

Specify the other EDA tools -- in addition to the Quartus II software -- used with the project.

☐ EDA design entry/synthesis tool: Format: ☐ Not available

☐ EDA simulation tool: Format: ☐ Not available

☐ EDA timing analysis tool: Format: ☐ Not available

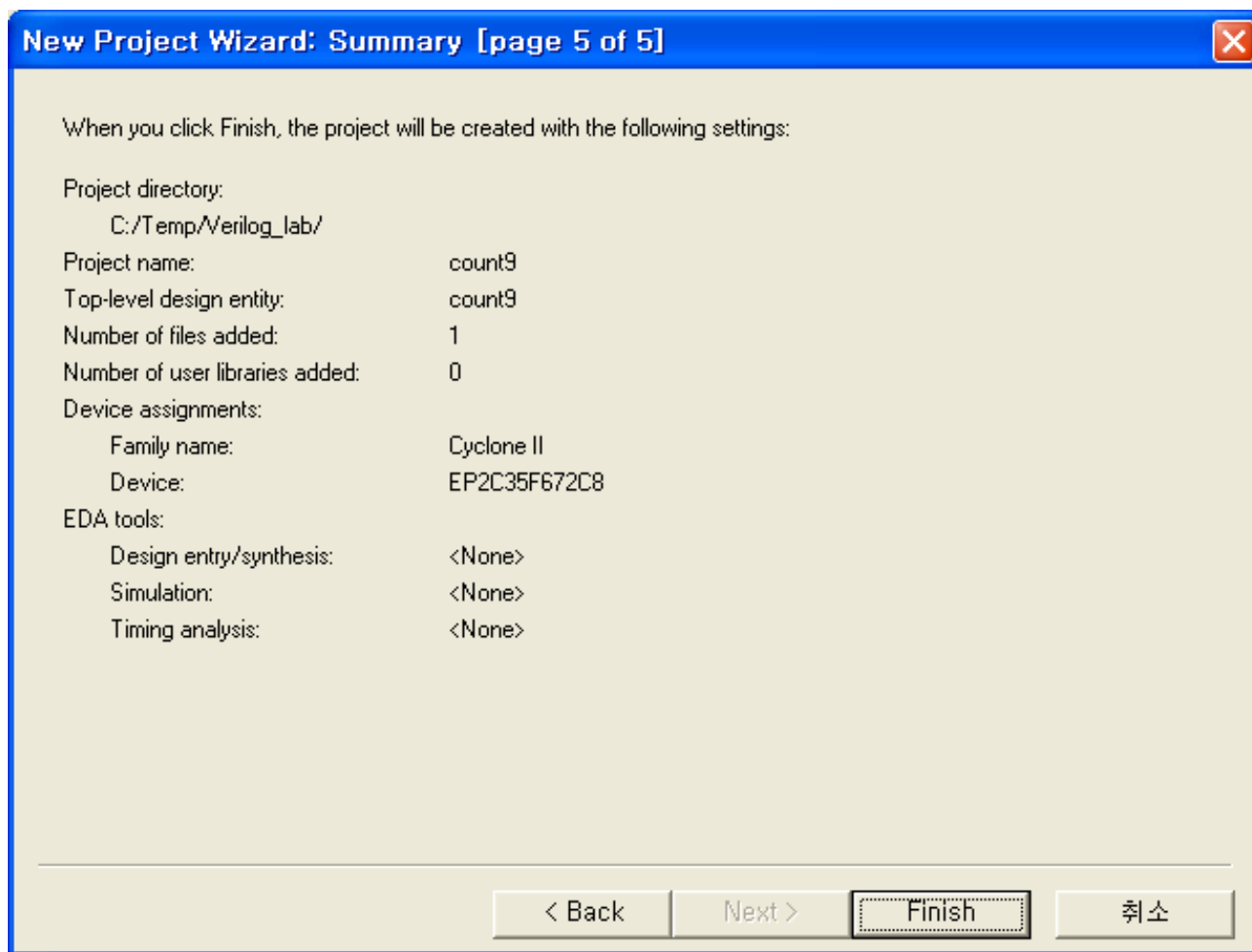
< Back Next > Finish 취소





프로젝트 생성

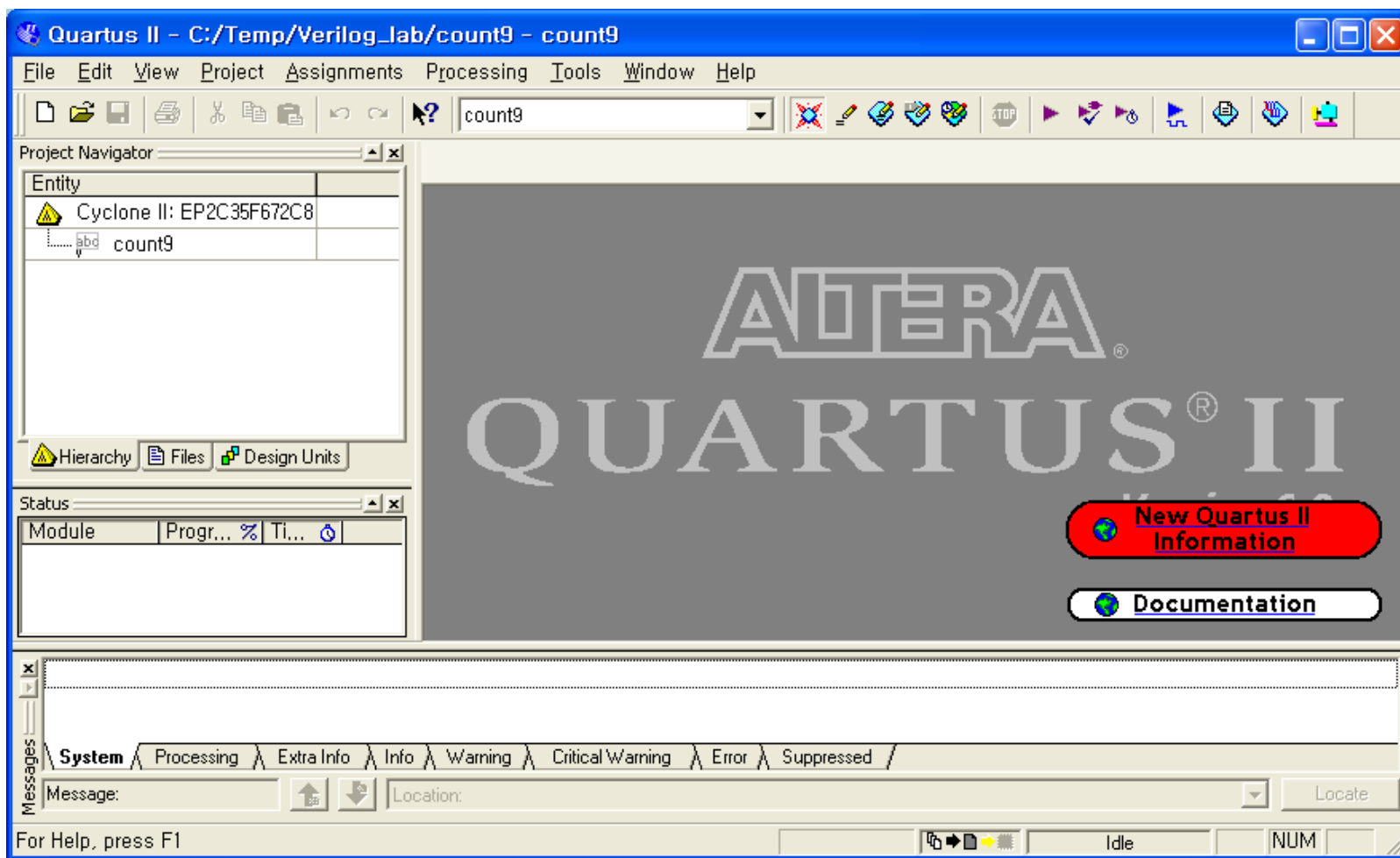
◆ Summary 대화창





프로젝트 생성

◆ 프로젝트 생성이 완료된 상태

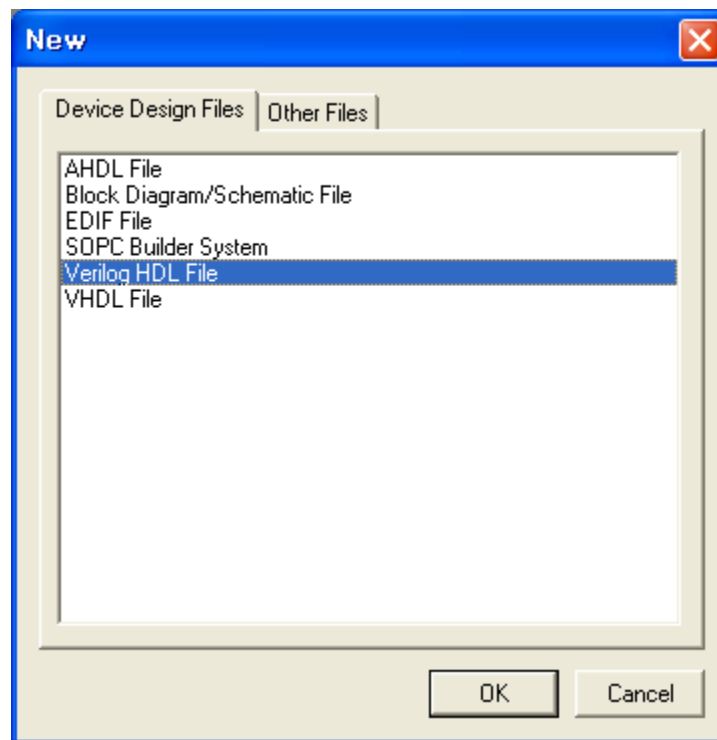
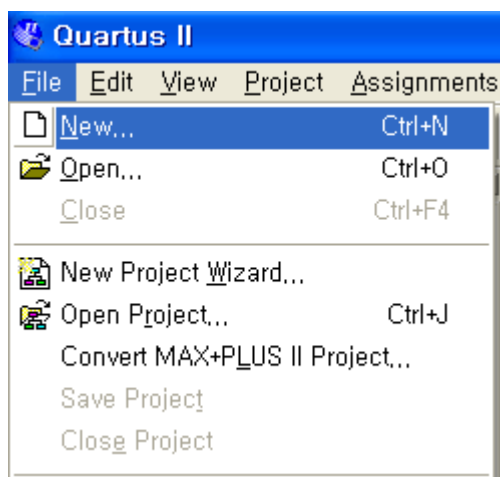




설계 입력

□ File -> New를 선택

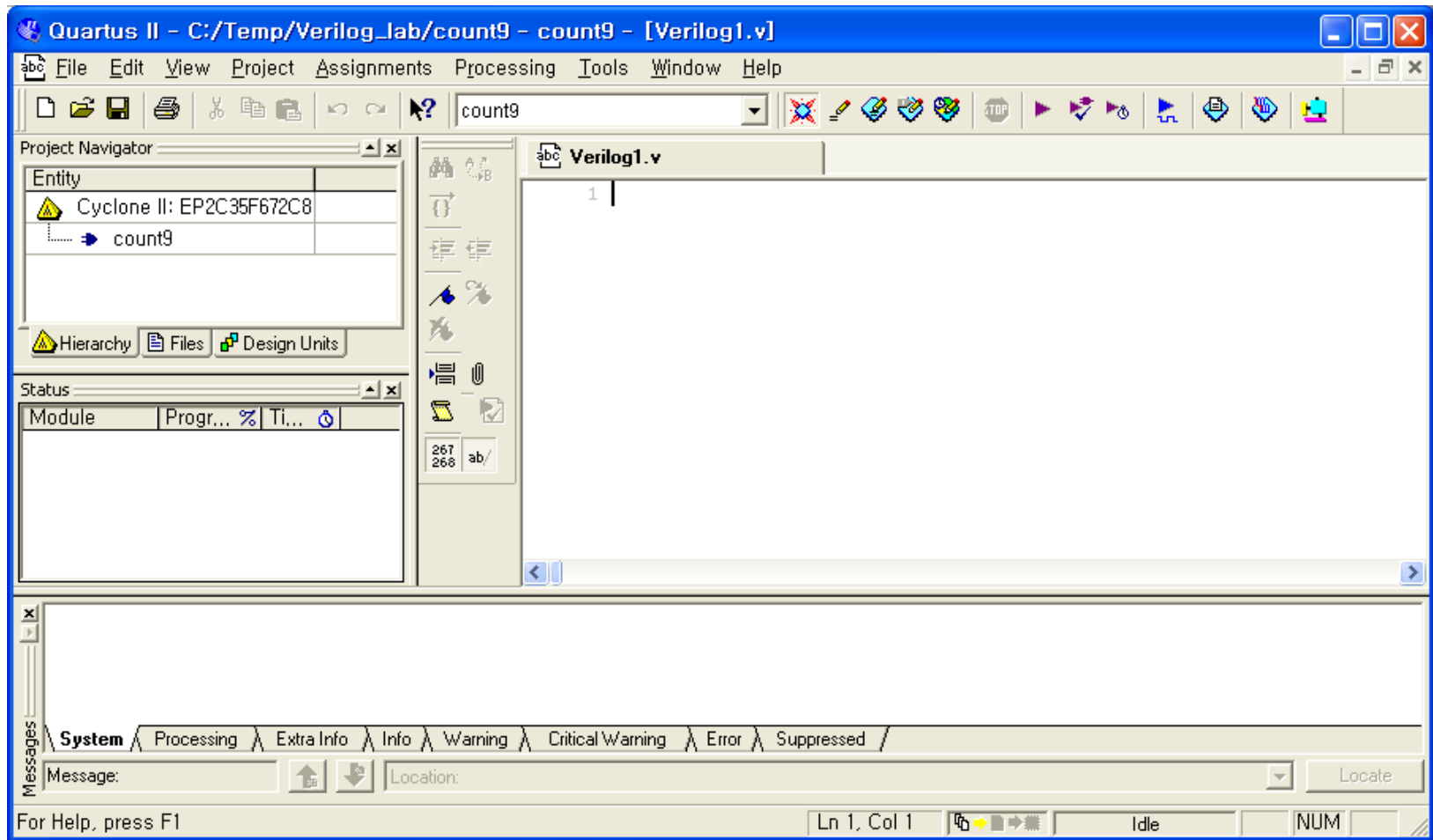
□ New 대화창에서 Verilog HDL File을 선택





설계 입력

◆ 문서 편집기가 활성화된 상태

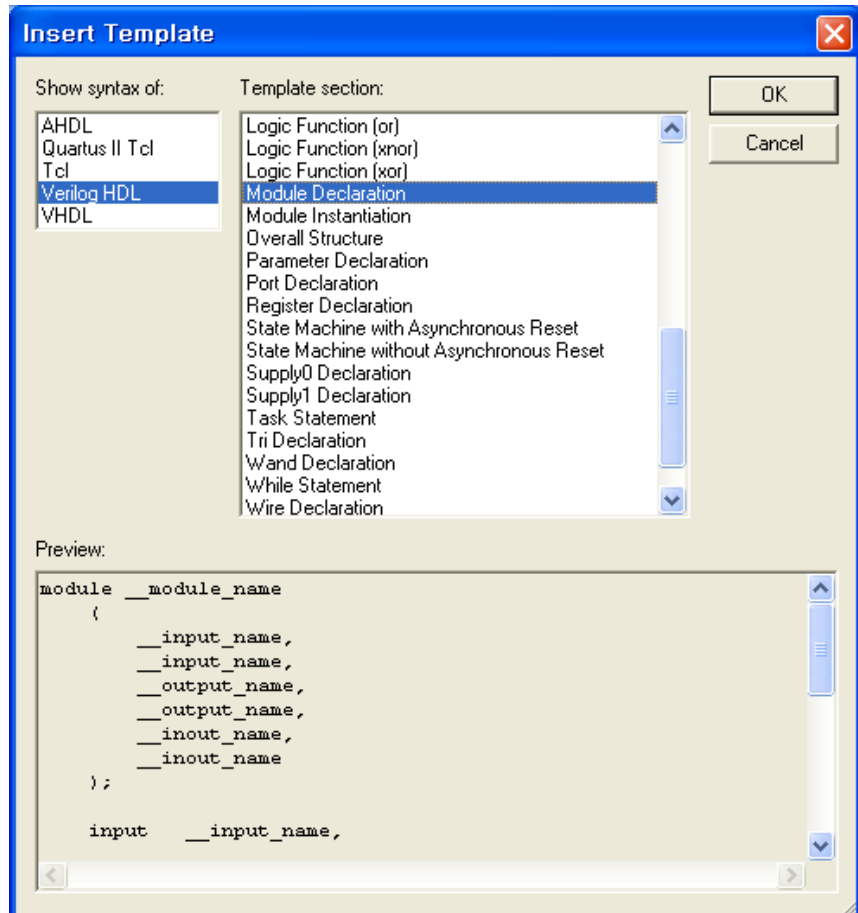
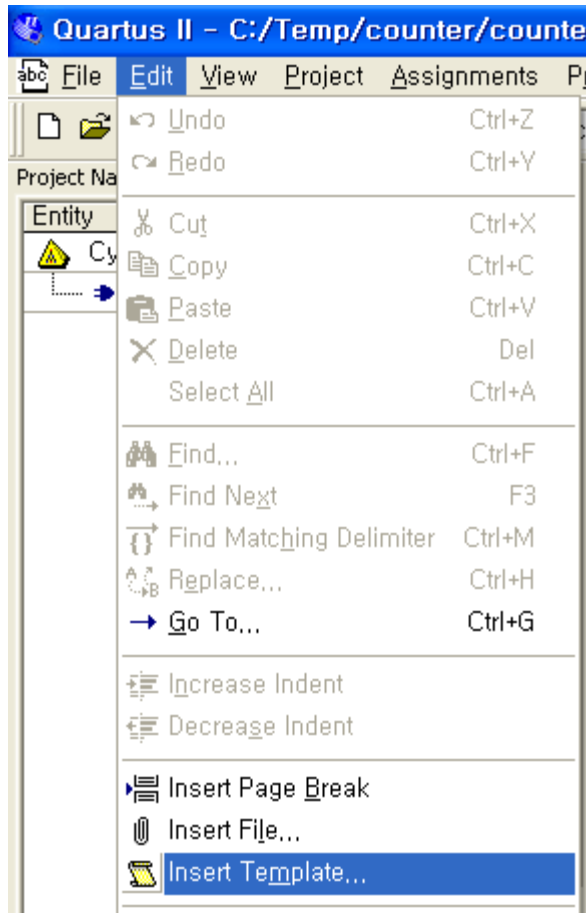




설계 입력

□ HDL Template를 이용한 설계 입력

◆ Edit -> Insert Template

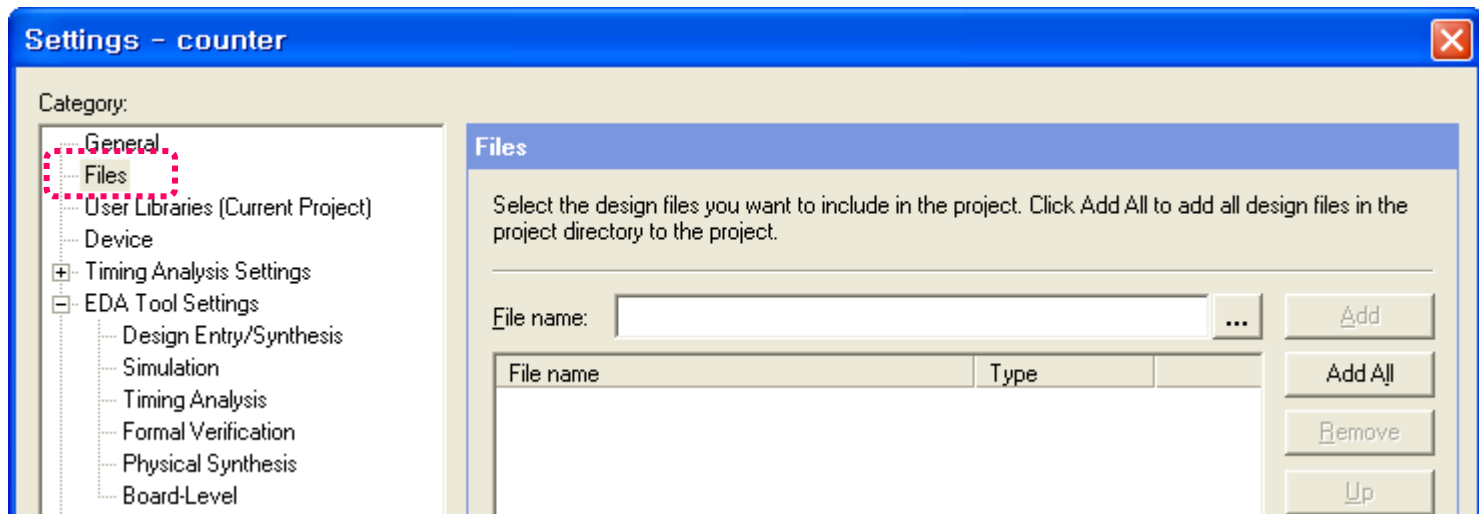




설계 입력

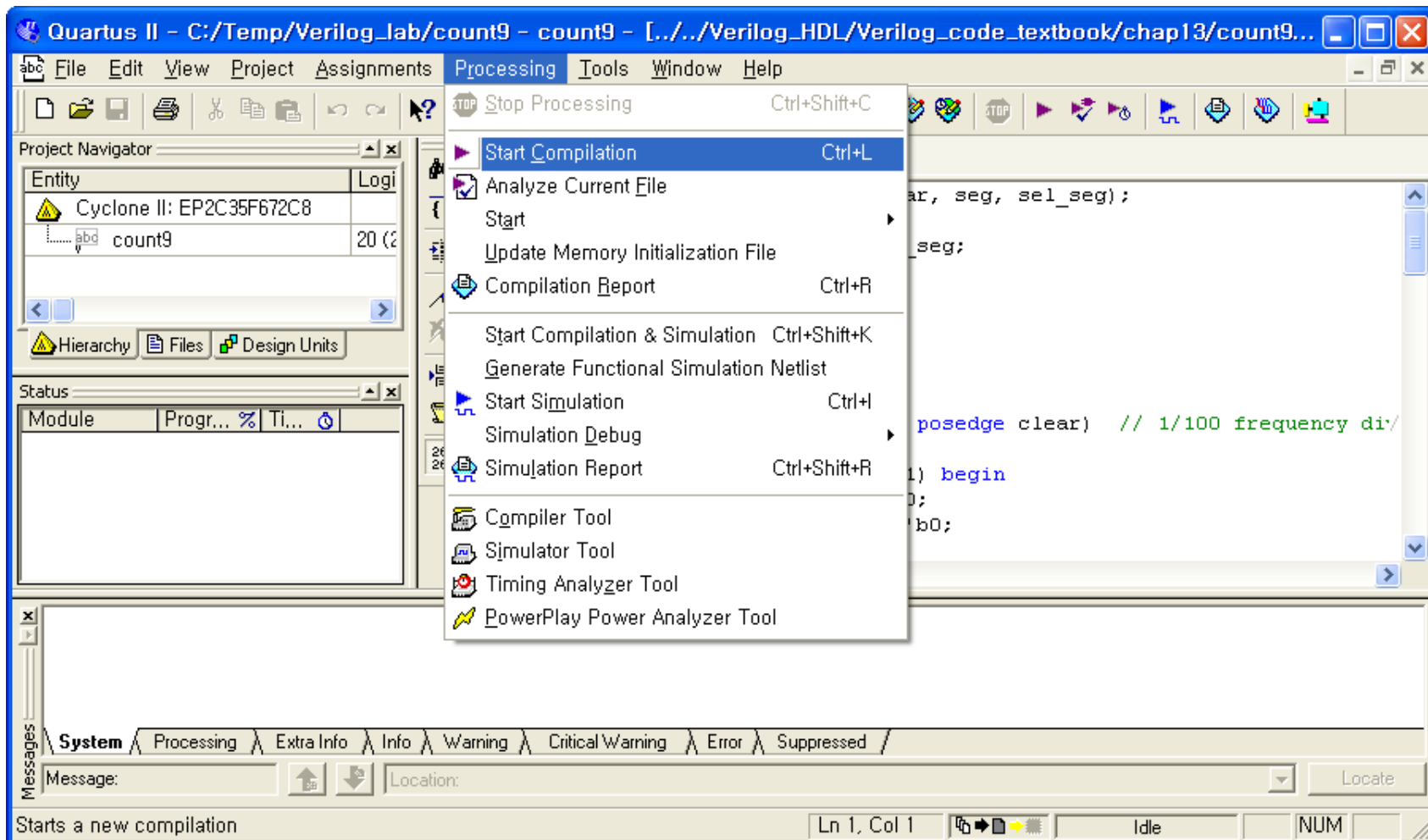
▣ HDL 소스파일 추가

◆ Project -> Add/Remove Files





컴파일





컴파일

◆ 컴파일 진행 과정

The screenshot displays the Quartus II software interface during the compilation of a Verilog project named 'count9'. The title bar indicates the project path: 'C:/Temp/Verilog_lab/count9 - count9 - [Compilation Report - Flow Summary]'. The interface is divided into several panes:

- Project Navigator:** Shows the project hierarchy with 'Cyclone II: EP2C35F672C8' and 'count9' listed.
- Status:** A table showing the progress of various compilation steps:

Module	Progress %
Full Compilation	70 %
Analysis & Synthesis	100 %
Fitter	100 %
Assembler	80 %
- Compilation Report - Flow Summary:** A detailed report on the right side of the window, listing various compilation parameters and results.

Flow Summary	
Flow Status	In progress - Sat Oct 27 12:48:01
Quartus II Version	6.0 Build 178 04/27/2006 SJ Full \
Revision Name	count9
Top-level Entity Name	count9
Family	Cyclone II
Device	EP2C35F672C8
Timing Models	Final
Met timing requirements	N/A
Total logic elements	20 / 33,216 (< 1 %)
Total registers	11
Total pins	18 / 475 (4 %)
Total virtual pins	0
Total memory bits	0 / 402,048 (0 %)
- Messages:** A log window at the bottom showing the command used to run the assembler: 'quartus_asm --read_settings_files=off --write_settings_files=off count9 -c count9'.





컴파일

◆ 컴파일 완료 상태

The screenshot shows the Quartus II software interface with the title bar "Quartus II - C:/Temp/Verilog_lab/count9 - count9 - [Compilation Report - Flow Summary]". The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The toolbar contains various icons for file operations and compilation. The Project Navigator on the left shows the project structure with "count9" selected. The Status window shows the progress of the compilation steps: Full Compilation (100%), Analysis & Synthesis (100%), Fitter (100%), and Assembler (100%). The Messages window at the bottom displays the following information:

- Info: tco from clock "clk" to destination pin "seg[1]" through register "cnt[0]" is 13.518 ns
- Info: Quartus II Timing Analyzer was successful. 0 errors, 2 warnings
- Info: Quartus II Full Compilation was successful. 0 errors, 16 warnings

A "Quartus II" dialog box is displayed in the center, stating "Full Compilation was successful (16 warnings)" with an "확인" (OK) button. The "Flow Summary" window on the right provides details about the compilation process:

Flow Summary	
Flow Status	Successful - Sat Oct 27 12:48:14
Quartus II Version	6.0 Build 178 04/27/2006 SJ Full
Revision Name	count9
Top-level Entity Name	count9
Cyclone II	EP2C35F672C8
Final	Yes
20 / 33,216 (< 1 %)	11
18 / 475 (4 %)	
Total virtual pins	0
Total parameters	0 / 400,000 (0 %)

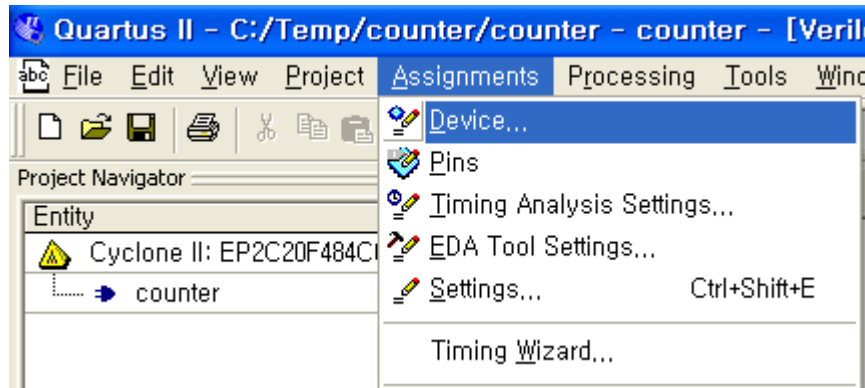




디바이스 및 핀 할당

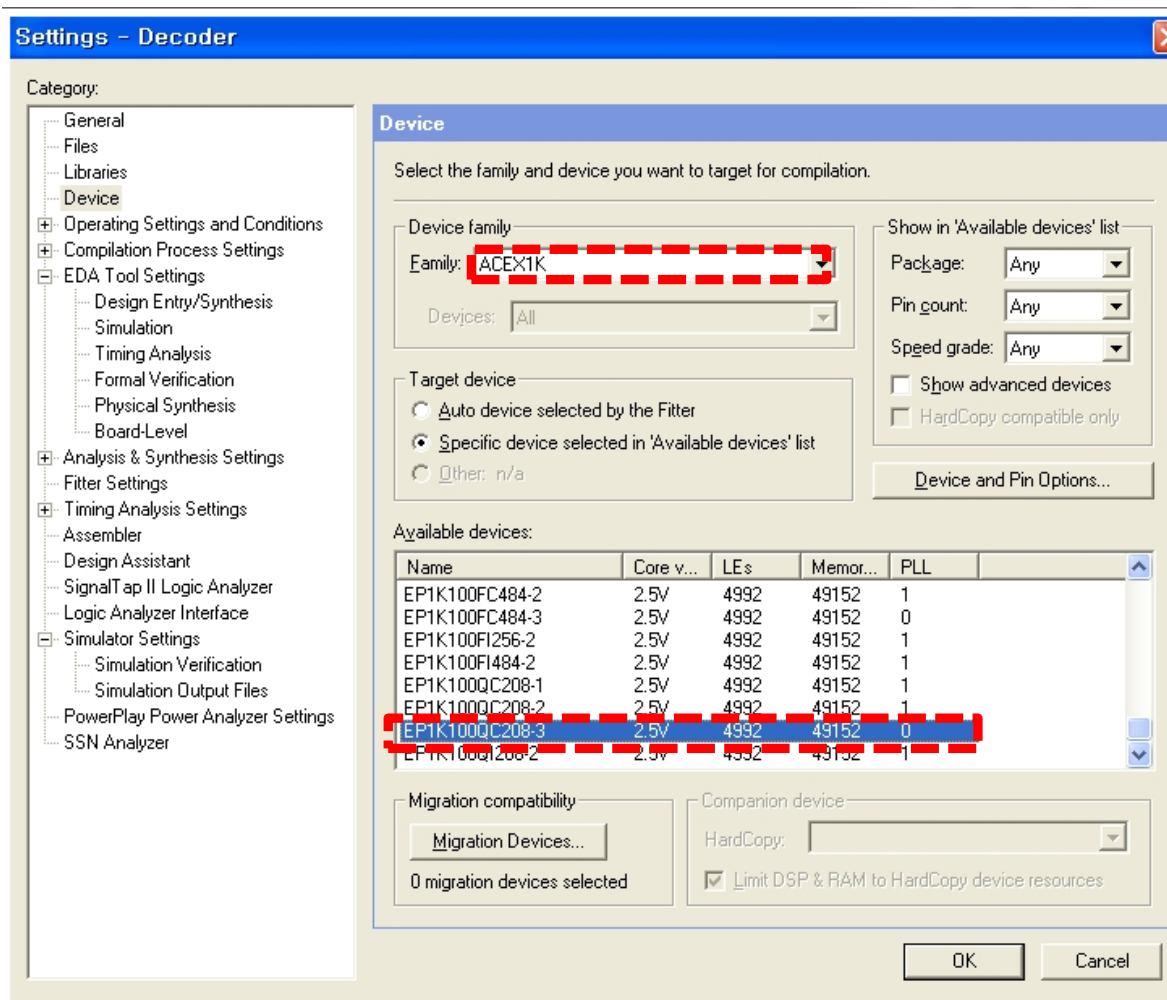
□ Target device 지정

◆ Assignments -> Device





디바이스 및 핀 할당

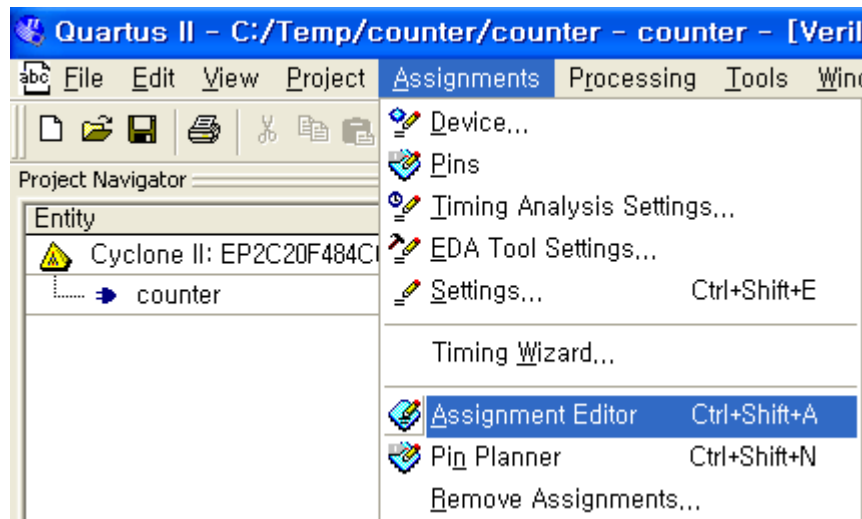




디바이스 및 핀 할당

■ Device Pin 할당

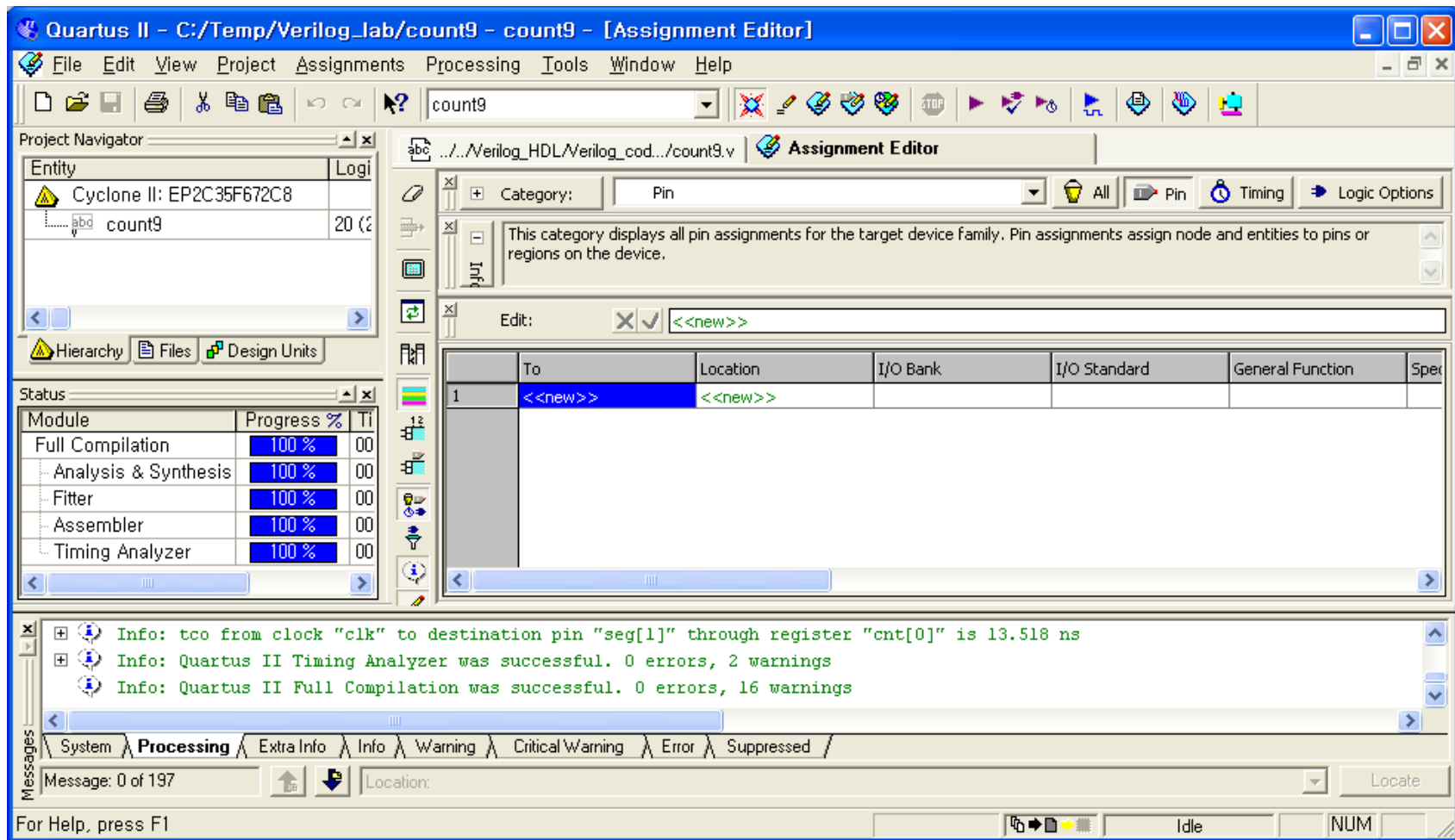
◆ Assignments -> Assignment Editor





디바이스 및 핀 할당

◆ Assignment Editor





디바이스 및 핀 할당

◆ Port 선택

The screenshot shows the Quartus II Assignment Editor for a project named 'count9'. The 'Pin' category is selected, and the 'Edit' window is open. A red dashed box highlights the 'To' column of the pin assignment table, which contains a list of pins: 'clear', 'clk', 'seg', 'seg[0]', 'seg[1]', 'seg[2]', 'seg[3]', 'seg[4]', 'seg[5]', 'seg[6]', 'seg[7]', 'sel_seg', 'sel_seg[0]', 'sel_seg[1]', 'sel_seg[2]', 'sel_seg[3]', 'sel_seg[4]', and 'sel_seg[5]'. The 'Location' column shows '<new>'. The 'I/O Bank', 'I/O Standard', 'General Function', and 'Speed' columns are empty.

To	Location	I/O Bank	I/O Standard	General Function	Speed
1	<new>				

Below the table, a list of pins is shown, including 'clear', 'clk', 'seg', 'seg[0]', 'seg[1]', 'seg[2]', 'seg[3]', 'seg[4]', 'seg[5]', 'seg[6]', 'seg[7]', 'sel_seg', 'sel_seg[0]', 'sel_seg[1]', 'sel_seg[2]', 'sel_seg[3]', 'sel_seg[4]', and 'sel_seg[5]'. The 'Messages' pane at the bottom shows information about the compilation process, including 'Info: tco from clock "clk" to destination', 'Info: Quartus II Timing Analyzer was successful', and 'Info: Quartus II Full Compilation was successful'.





디바이스 및 핀 할당

◆ Pin 할당

Quartus II - C:/Temp/Verilog_lab/count9 - count9 - [Assignment Editor*]

File Edit View Project Assignments Processing Tools Window Help

count9

Project Navigator

Entity	Logi
Cyclone II: EP2C35F672C8	
count9	20 (2

Hierarchy Files Design Units

Status

Module	Progress %	TI
Full Compilation	100 %	00
Analysis & Synthesis	100 %	00
Fitter	100 %	00
Assembler	100 %	00
Timing Analyzer	100 %	00

Messages

System Processing Extra Info Info Warning Critical Warning Error

Message: 0 of 197 Location:

For Help, press F1

Assignment Editor*

Category: Pin

Assigns a location on the device for the current node(s) and/or pin(s).

Edit:

To	Location	I/O Bank	I/O Standard	General Function	Spec
1 clear			LVTTL		
2 <<new>>					

EDGE_BOTTOM
EDGE_LEFT
EDGE_RIGHT
EDGE_TOP
IOBANK_1 I/O Bank 1
IOBANK_2 I/O Bank 2
IOBANK_3 I/O Bank 3
IOBANK_4 I/O Bank 4
IOBANK_5 I/O Bank 5
IOBANK_6 I/O Bank 6
IOBANK_7 I/O Bank 7
IOBANK_8 I/O Bank 8
PIN_A4 I/O Bank 3 Column I/O LVD551p
PIN_A5 I/O Bank 3 Column I/O LVD552p
PIN_A6 I/O Bank 3 Column I/O LVD553n
PIN_A7 I/O Bank 3 Column I/O LVD558n
PIN_A8 I/O Bank 3 Column I/O LVD562n

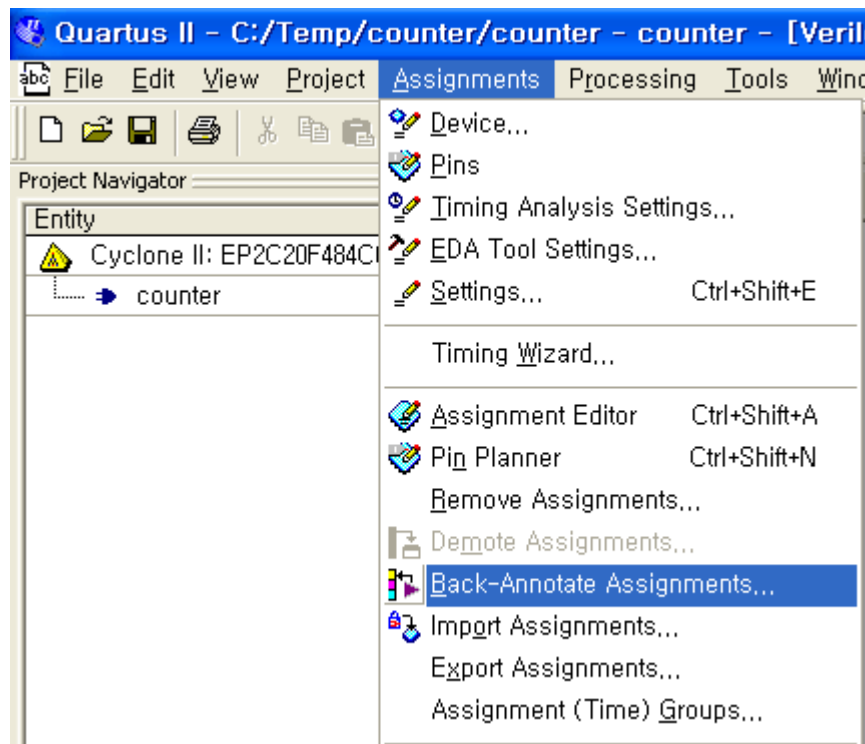




디바이스 및 핀 할당

■ Back-Annotate Assignments를 이용한 핀 할당

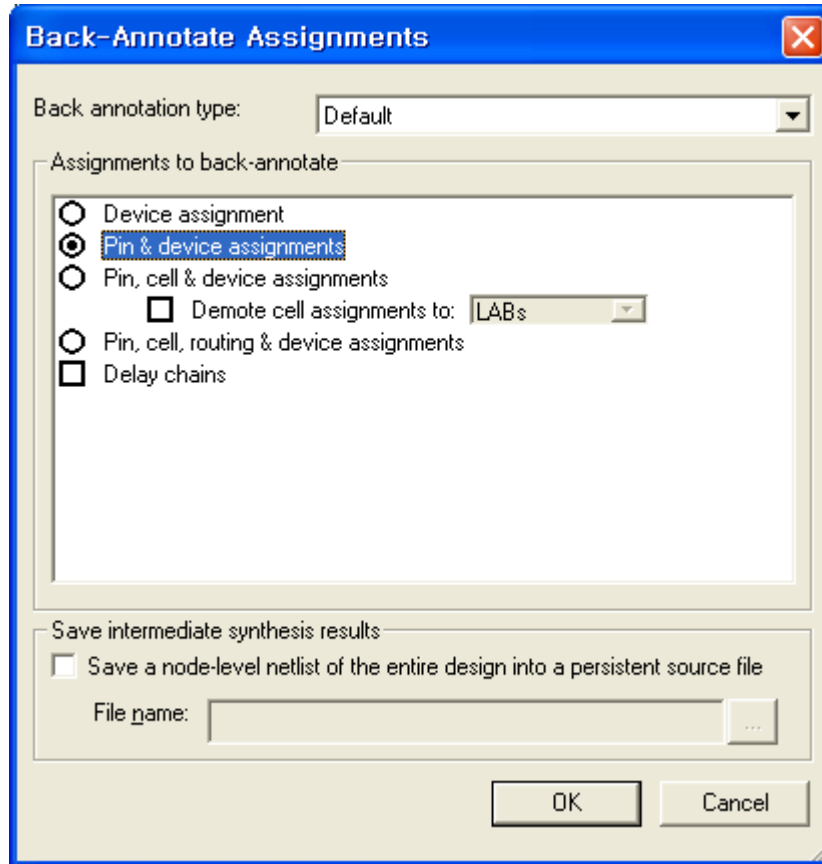
◆사전에 full compile이 완료되어야 함.





디바이스 및 핀 할당

■ Back-Annotate Assignments를 이용한 핀 정보 불러오기





디바이스 및 핀 할당

◆ Assignment Editor를 사용하여 Pin 정보를 수정

Quartus II - C:/Temp/Verilog_lab/count9 - count9 - [Assignment Editor]

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity Logi
Cyclone II: EP2C35F672C8
count9 20 (2)

Status

Module	Progress %	TI
Full Compilation	100 %	00
Analysis & Synthesis	100 %	00
Fitter	100 %	00
Assembler	100 %	00
Timing Analyzer	100 %	00

Assignment Editor

Category: Pin

Assigns a location on the device for the current node(s) and/or pin(s).

Edit: PIN_P1

To	Location	I/O Bank	I/O Standard	General Function
clear	PIN_P1	1	LVTTL	Dedicated Clock
clk	PIN_P2	1	LVTTL	Dedicated Clock
seg[0]	PIN_AC15	7	LVTTL	Column I/O
seg[1]	PIN_AD25	6	LVTTL	Row I/O
seg[2]	PIN_AE25	6	LVTTL	Row I/O
seg[3]	PIN_AE16	7	LVTTL	Column I/O
seg[4]	PIN_Y15	7	LVTTL	Column I/O

Messages

Info: Ended Full Compilation at Sat Oct 27 12:48:15 2007
Info: Back-annotation was successful. The locations of 21 nodes were written/updated.
Info: Can't save incomplete assignment -- missing field: Value
Info: Can't save incomplete assignment -- missing field: Value

System Processing Extra Info Info Warning Critical Warning Error Suppressed

Message: 0 of 7

Location:

For Help, press F1

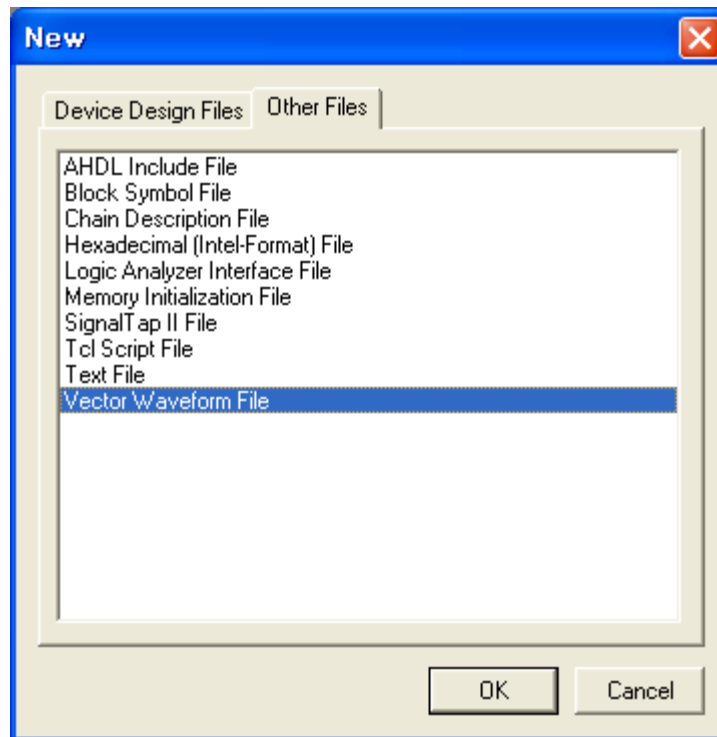
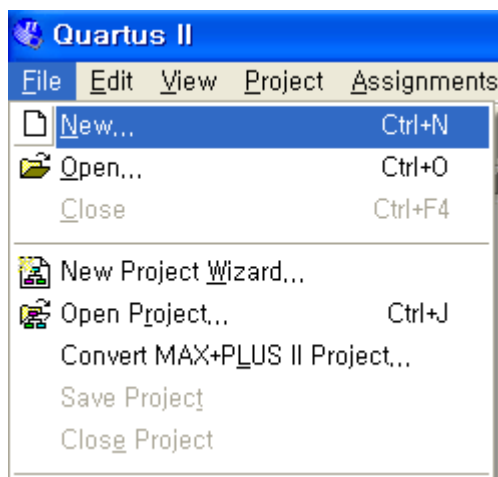




시뮬레이션

■ Quartus II Simulator를 사용한 시뮬레이션

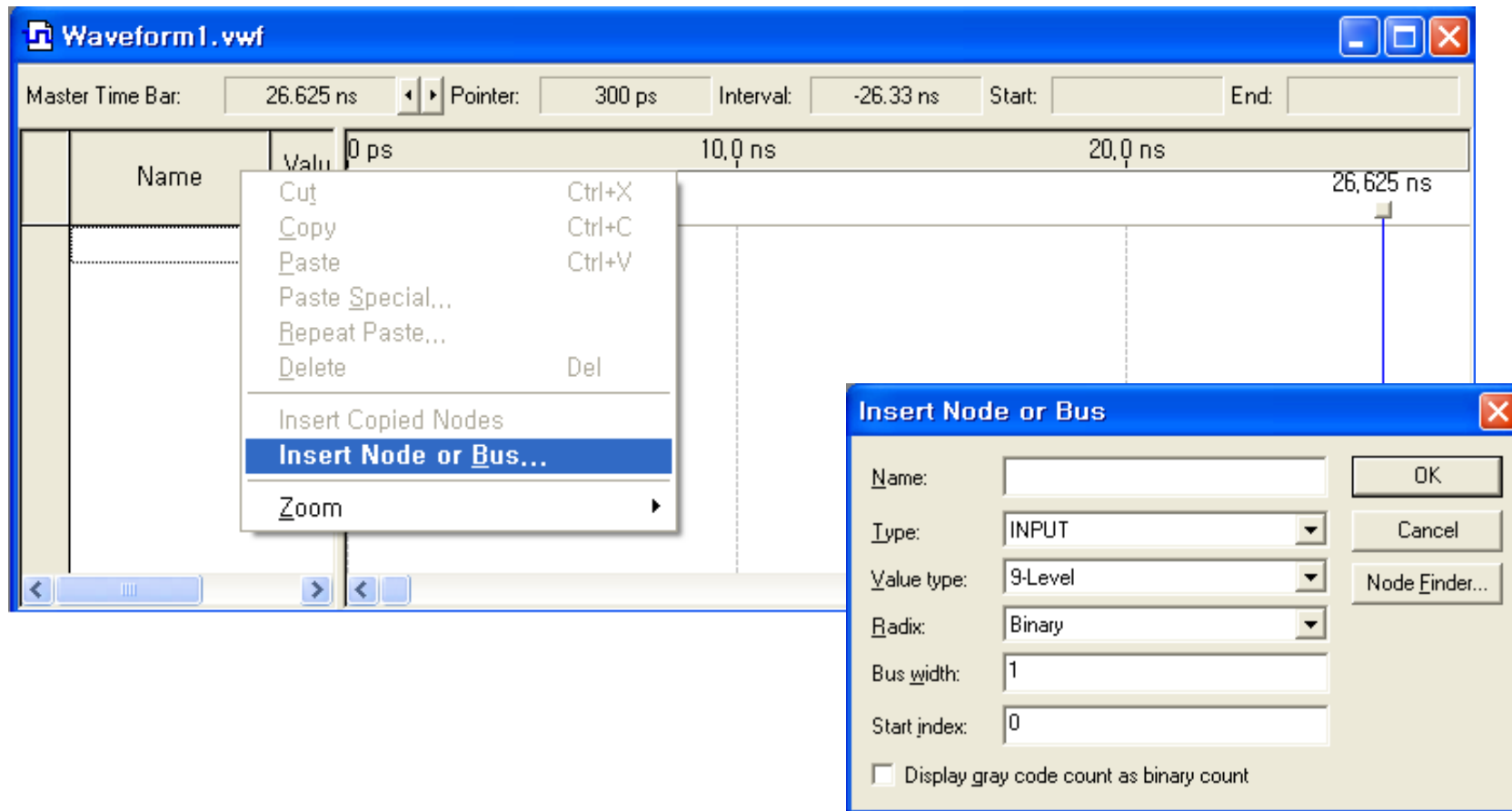
- ◆ File -> New
- ◆ Vector Waveform File





시뮬레이션

□ 시뮬레이션 입력파형 생성

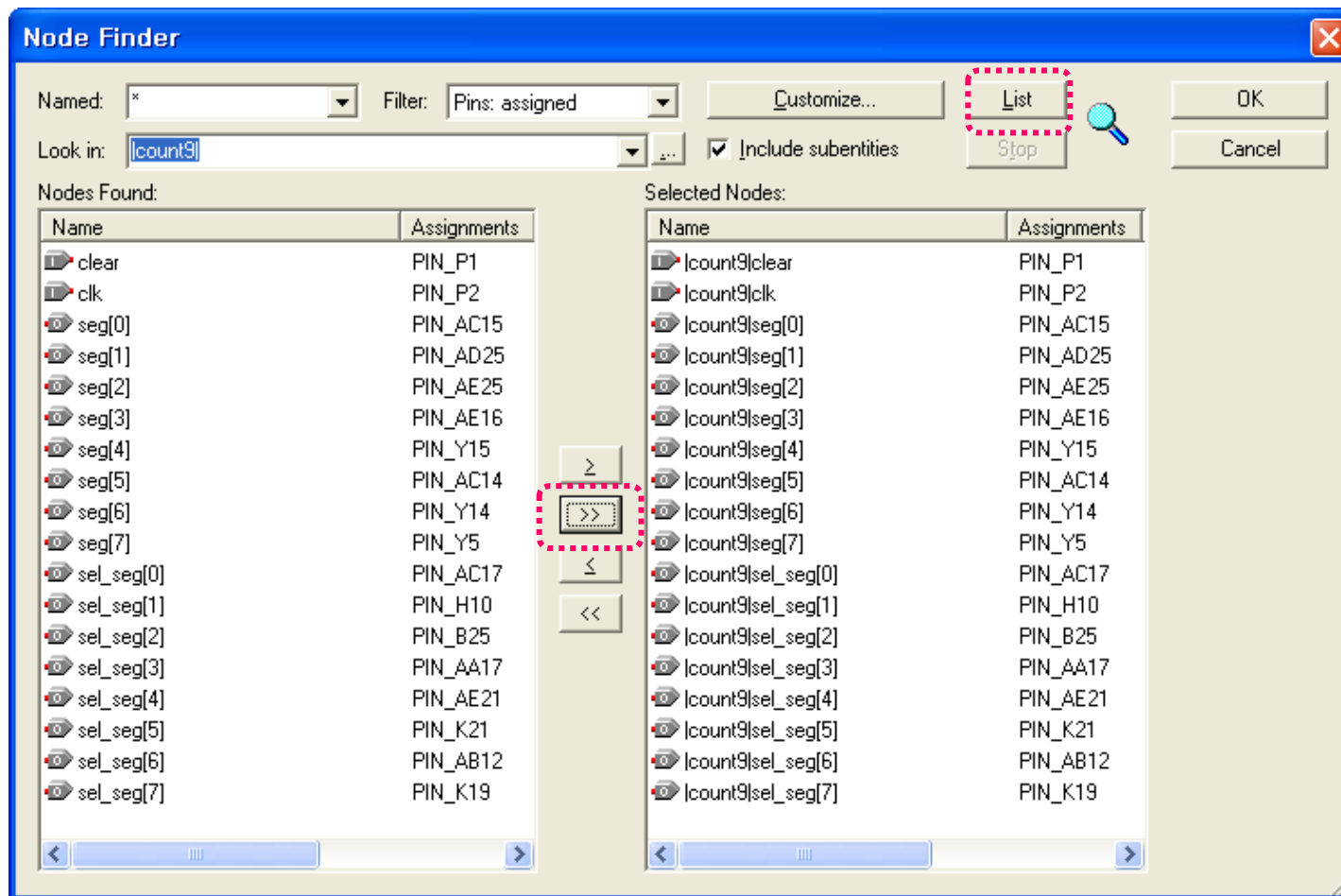




시뮬레이션

□ 시뮬레이션 입력파형 생성

◆ Node Finder 창

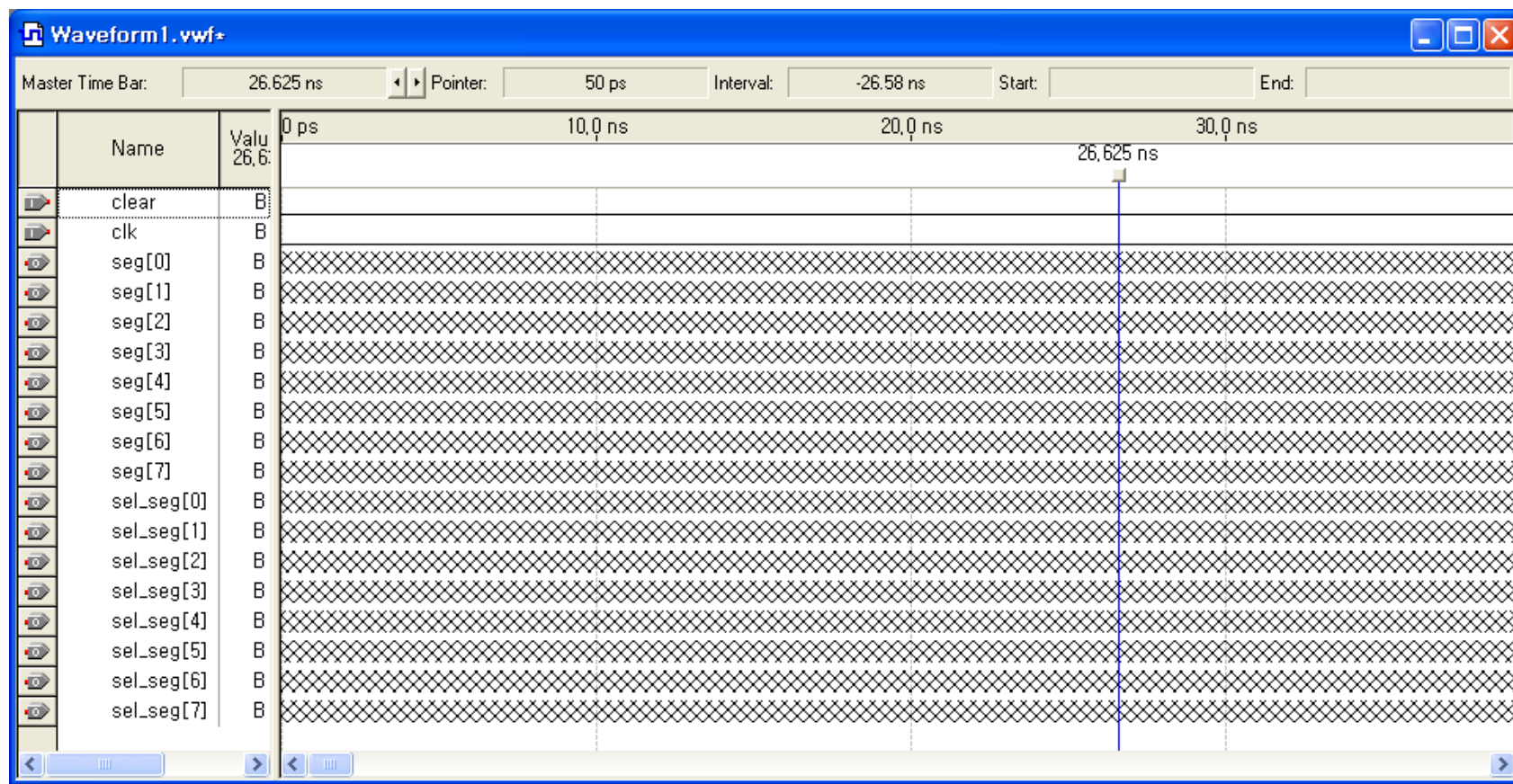




시뮬레이션

□ 시뮬레이션 입력파형 생성

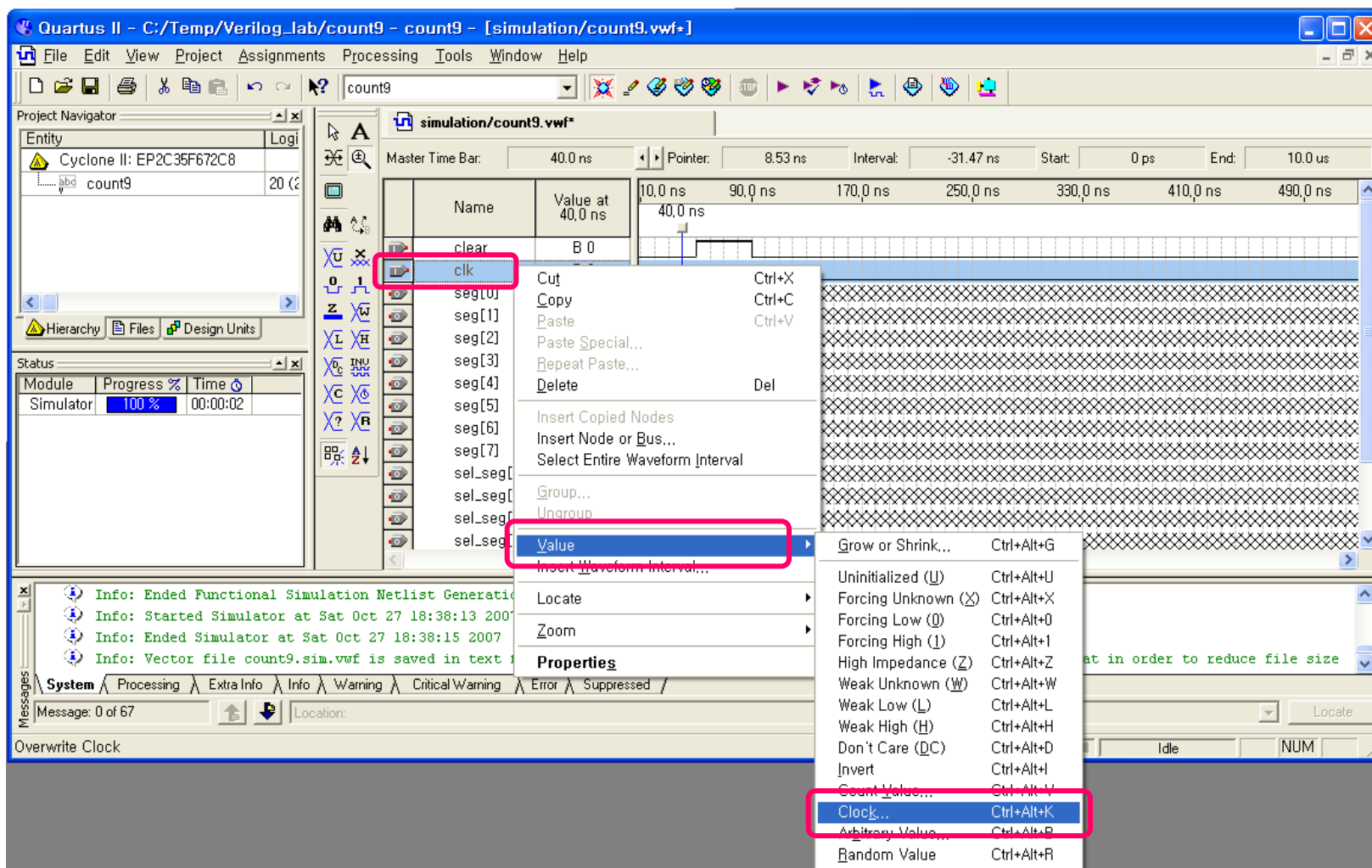
◆ 입출력 포트의 로드가 완료된 상태





시뮬레이션

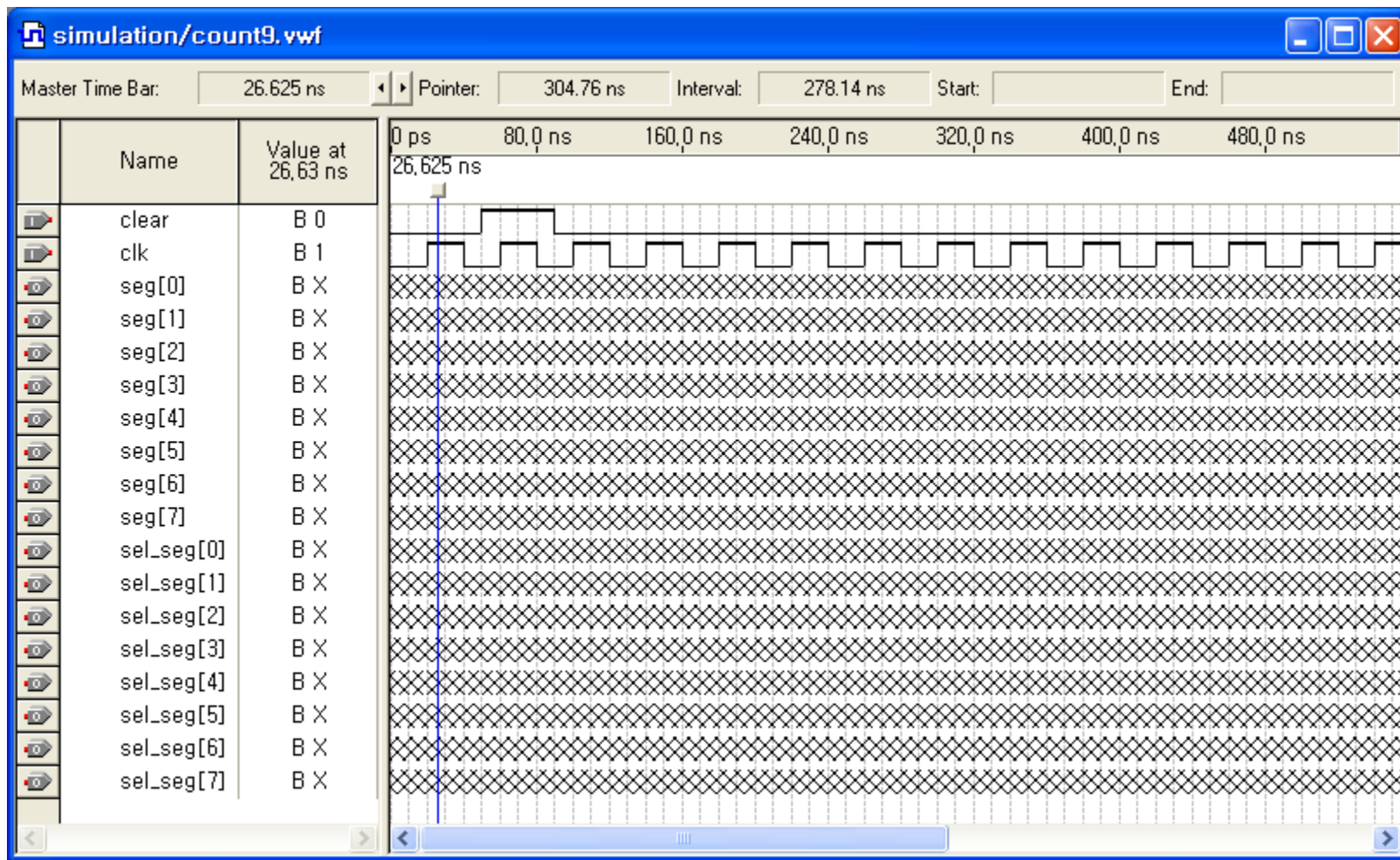
◆ 시뮬레이션 파형 설정





시뮬레이션

◆ 시뮬레이션 파형 설정이 완료된 상태

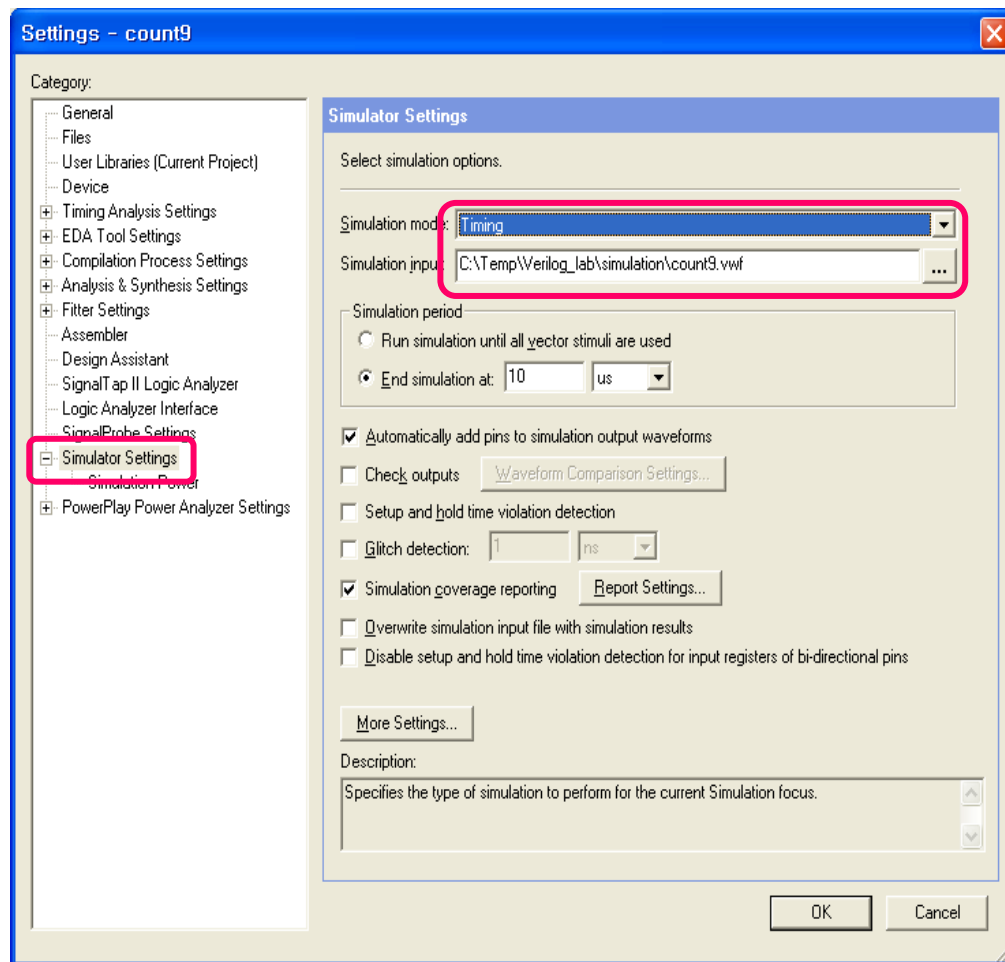
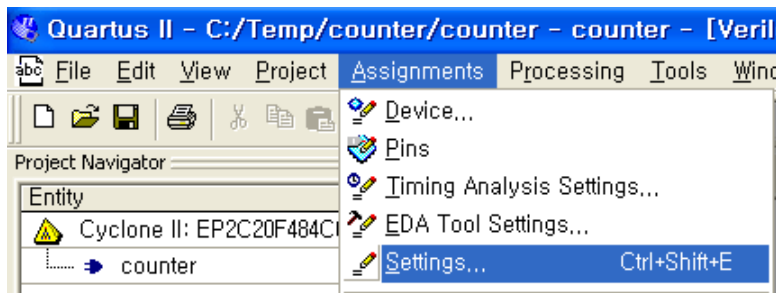




시뮬레이션

□ 타이밍 시뮬레이션 설정

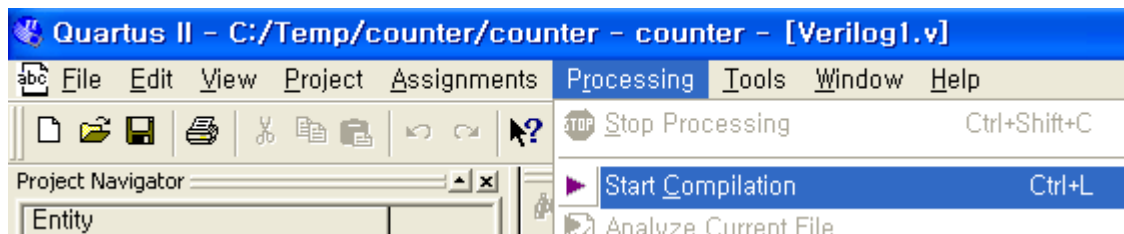
◆ Assignments -> Settings



시뮬레이션

▣ 시뮬레이션 실행

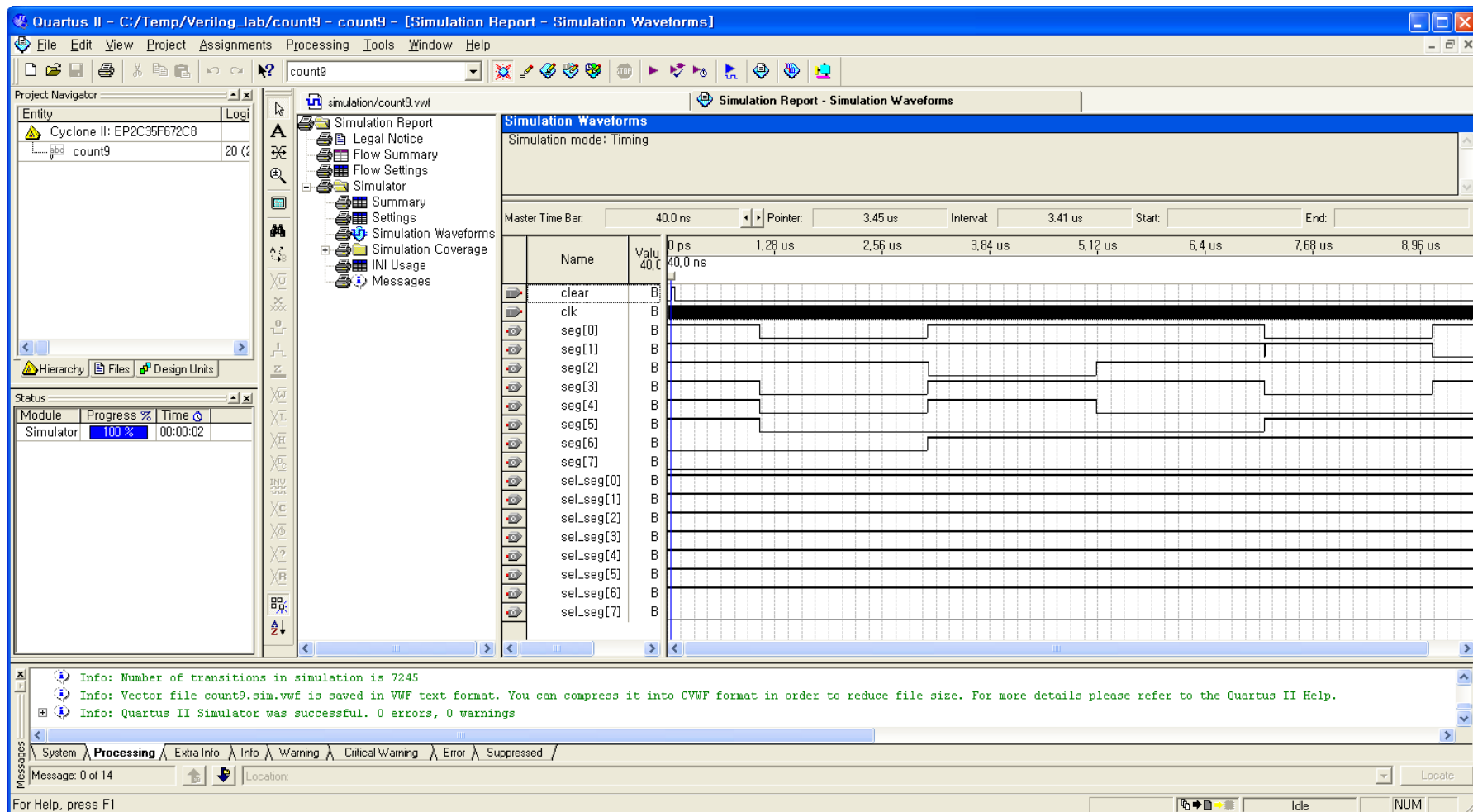
◆ Processing -> Start Simulation





시뮬레이션

◆ 시뮬레이션 결과

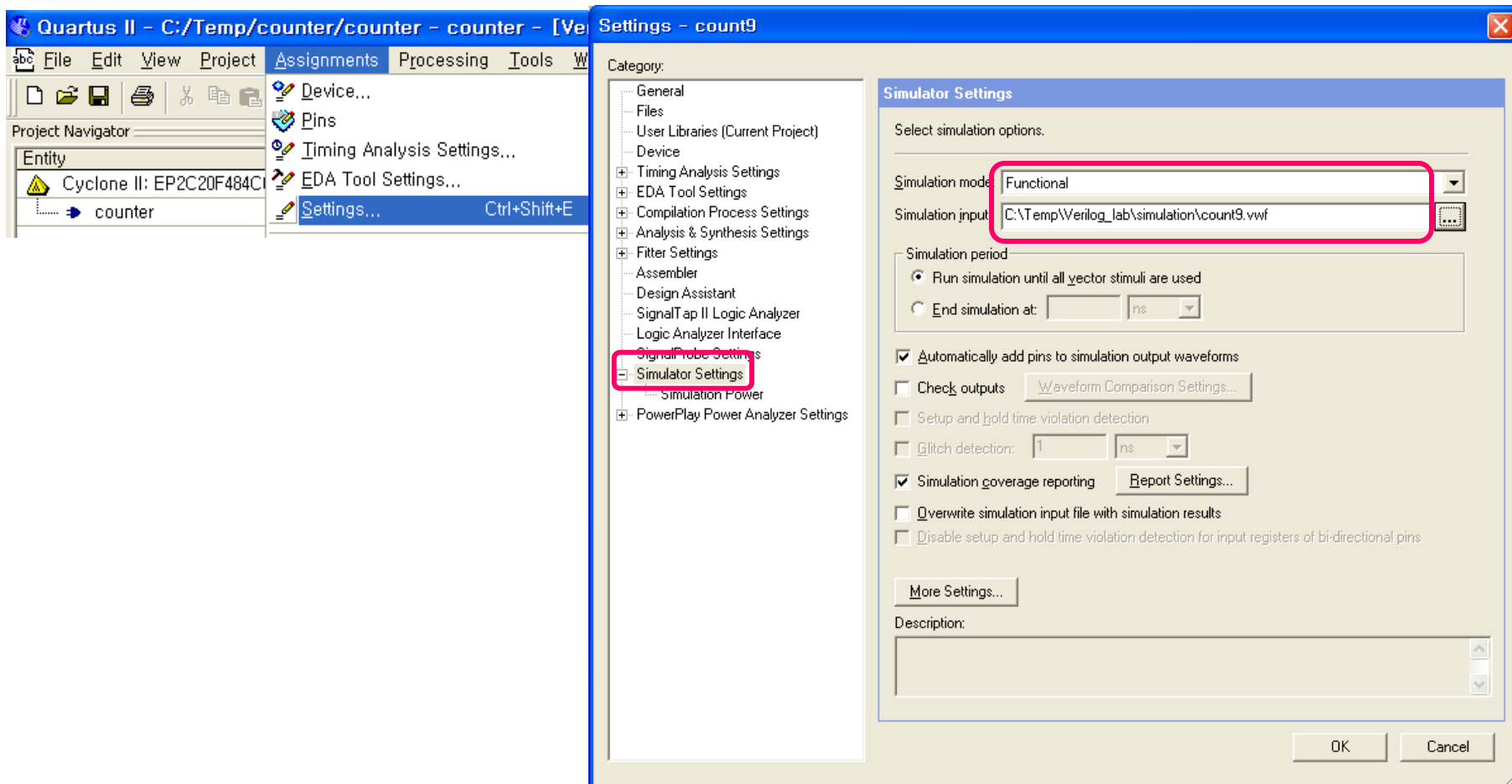




시뮬레이션

□ 기능 시뮬레이션 설정

◆ Assignments -> Settings

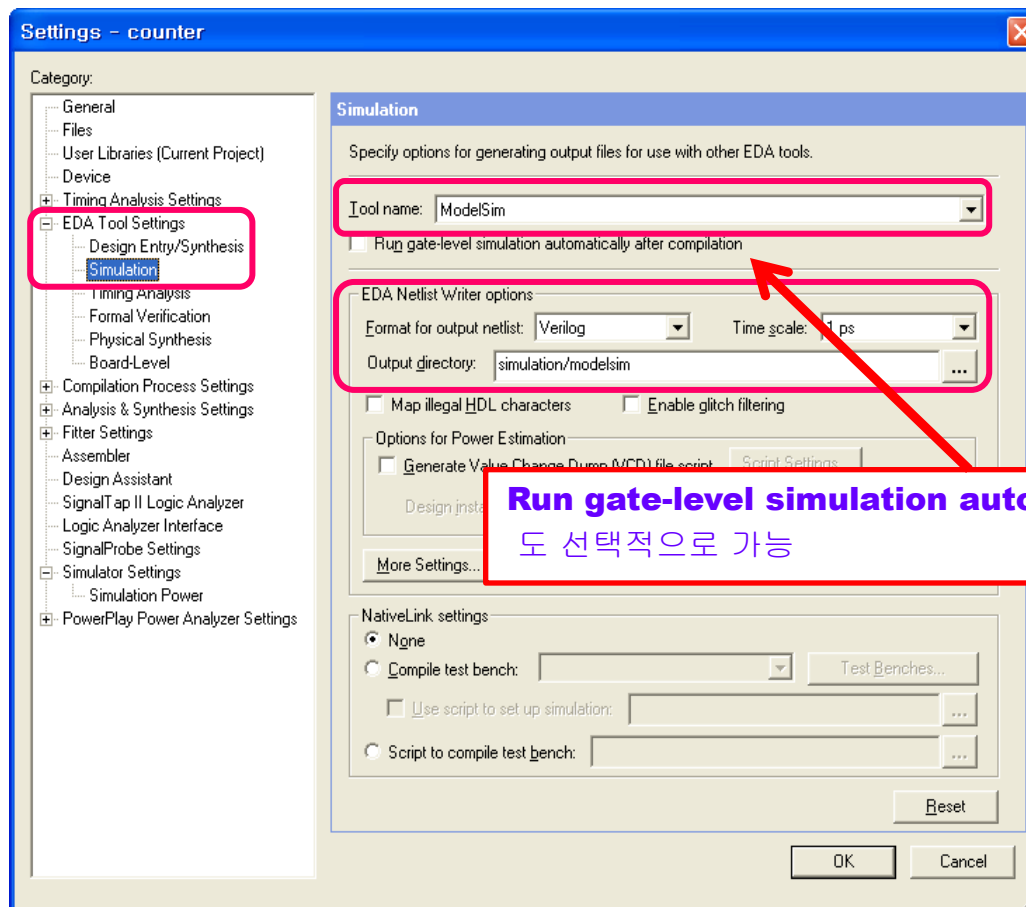




ModelSim을 이용한 시뮬레이션

□ 시뮬레이터 설정

- ◆ Assignments -> Settings
- ◆ EDA Tool Settings -> Simulation



Run gate-level simulation automatically after compile
도 선택적으로 가능

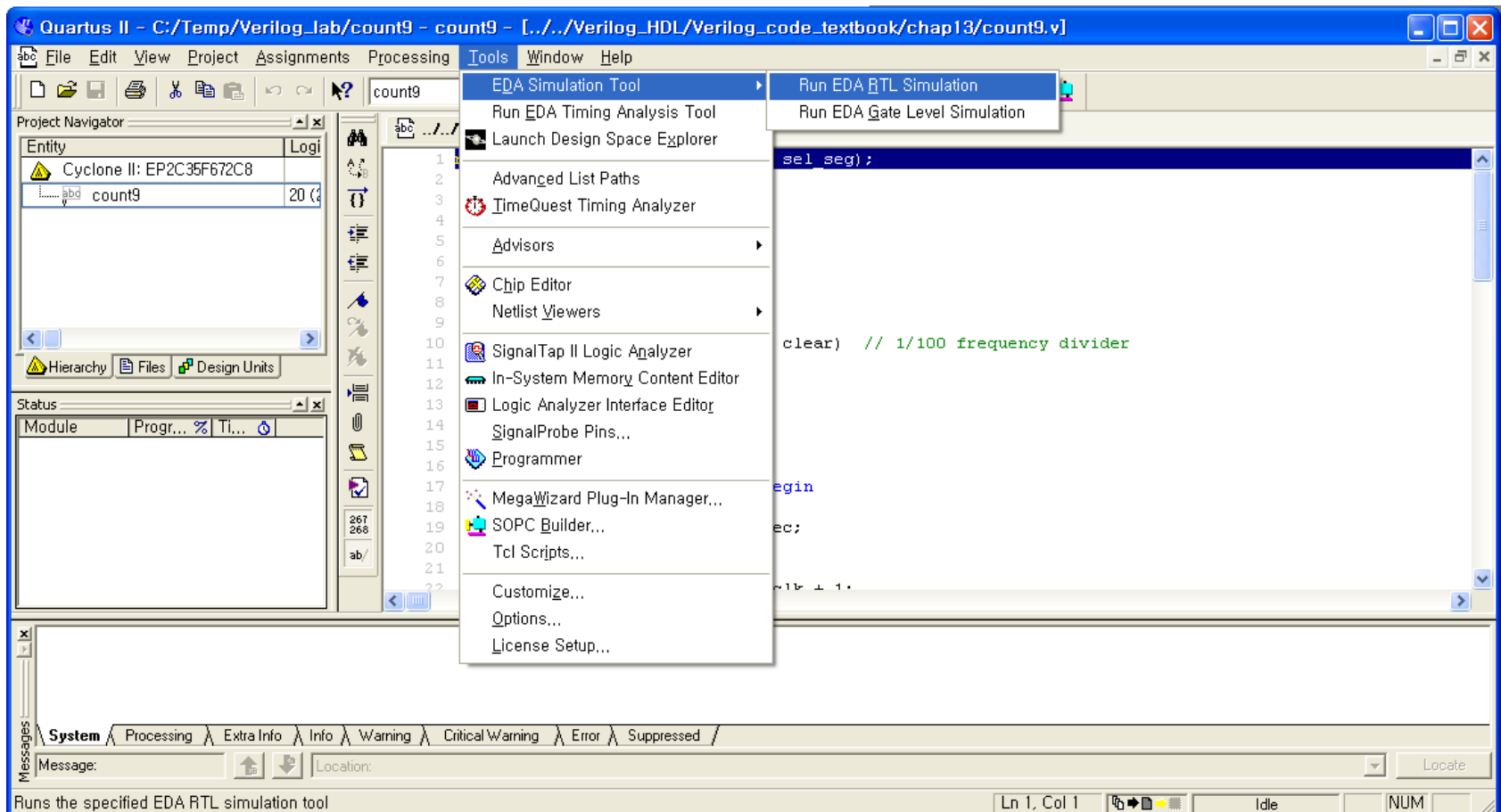




ModelSim을 이용한 시뮬레이션

□ 시뮬레이터 실행

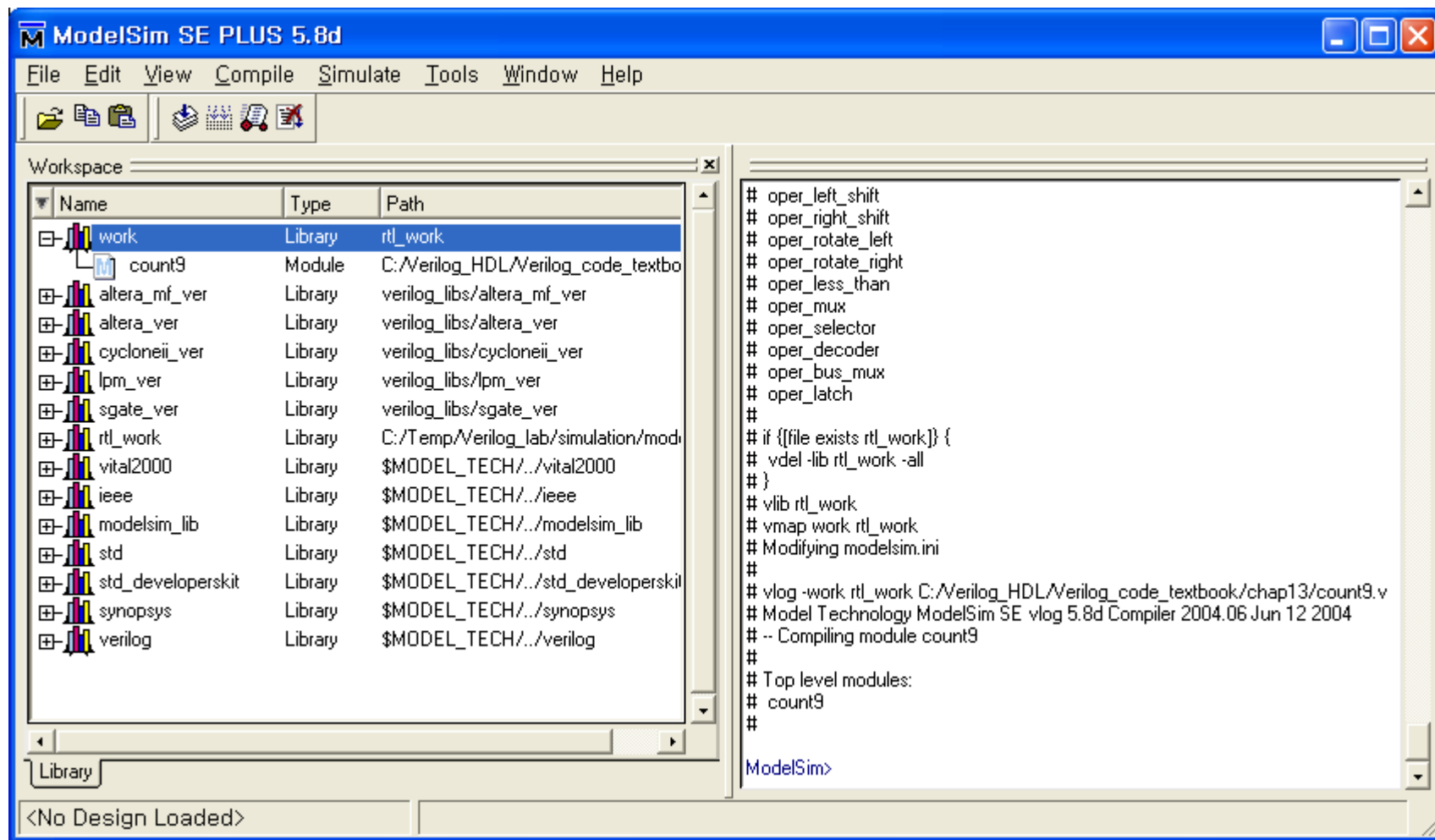
- ◆ Tools -> EDA Simulation Tool -> Run EDA RTL Simulation
- > Run EDA Gate Level Simulation





ModelSim을 이용한 시뮬레이션

◆ ModelSim이 실행된 상태





ModelSim을 이용한 시뮬레이션

- ◆ 기존에 없던 테스트벤치 파일이 컴파일 되어 추가된 상태

The screenshot shows the ModelSim SE PLUS 5.8d interface. The Workspace window on the left displays a list of files and libraries. The 'tb_count9' file is highlighted with a red box. The Command window on the right shows the compilation process, including the command 'vlog -work work C:/Verilog_HDL/Verilog_code_textbook/chap13/tb_count9.v' and the output 'ModelSim>'. A red arrow points from the Command window to a text box at the bottom right.

Name	Type	Path
work	Library	rtl_work
count9	Module	C:/Verilog_HDL/Verilog_code_textbook/chap13/count9.v
tb_count9	Module	C:/Verilog_HDL/Verilog_code_textbook/chap13/tb_count9.v
altera_mf_ver	Library	verilog_libs/altera_mf_ver
altera_ver	Library	verilog_libs/altera_ver
cycloneii_ver	Library	verilog_libs/cycloneii_ver
lpm_ver	Library	verilog_libs/lpm_ver
sgate_ver	Library	verilog_libs/sgate_ver
rtl_work	Library	C:/Temp/Verilog_lab/simulation/mod
vital2000	Library	\$MODEL_TECH/./vital2000
ieee	Library	\$MODEL_TECH/./ieee
modelsim_lib	Library	\$MODEL_TECH/./modelsim_lib
std	Library	\$MODEL_TECH/./std
std_developerskit	Library	\$MODEL_TECH/./std_developerskit
synopsys	Library	\$MODEL_TECH/./synopsys
verilog	Library	\$MODEL_TECH/./verilog

```
# oper_decoder
# oper_bus_mux
# oper_latch
#
# if {[file exists rtl_work]} {
#   vdel -lib rtl_work -all
# }
# vlib rtl_work
# vmap work rtl_work
# Modifying modelsim.ini
#
# vlog -work rtl_work C:/Verilog_HDL/Verilog_code_textbook/chap13/count9.v
# Model Technology ModelSim SE vlog 5.8d Compiler 2004.06 Jun 12 2004
# -- Compiling module count9
#
# Top level modules:
# count9
#
vlog -reportprogress 300 -work work C:/Verilog_HDL/Verilog_code_textbook/chap13/tb_count9.v
# Model Technology ModelSim SE vlog 5.8d Compiler 2004.06 Jun 12 2004
# -- Compiling module tb_count9
#
# Top level modules:
# tb_count9

ModelSim>
```

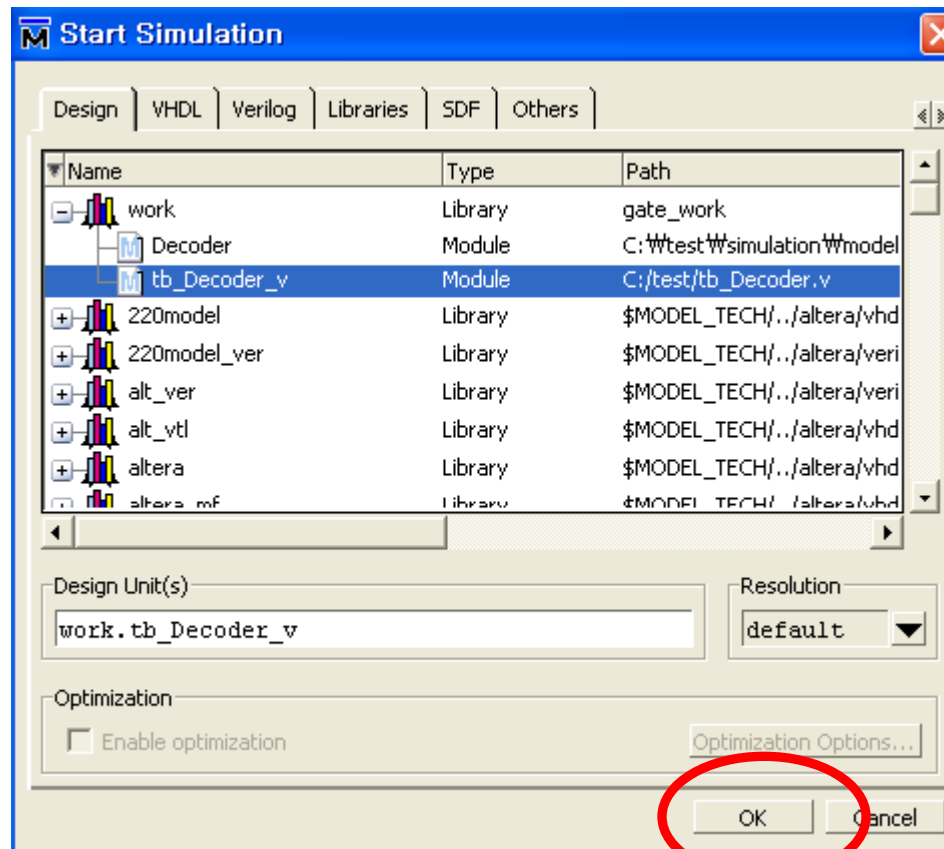
터미널에 입력 :
vlog -work work C:.....v





Gate Level 시뮬레이션 시 문제 해결

라이브러리 찾지 못하는 에러 발생

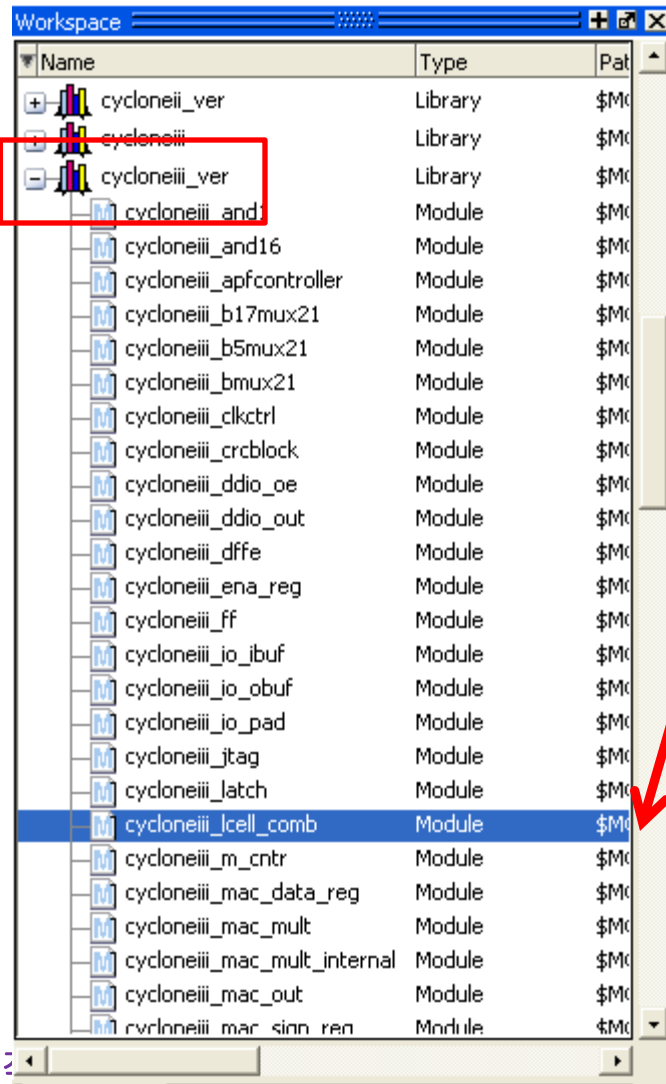


```
# ** Error: (vsim-3033) Decoder_8_1200mv_85c_slow.vo(385): Instantiation of 'cycloneiii_lcell_comb' failed. The design unit was not found.  
# Region: /tb_Decoder_v/uut  
# Searched libraries:  
# C:\test\simulation\modelsim\gate_work  
# Error loading design
```

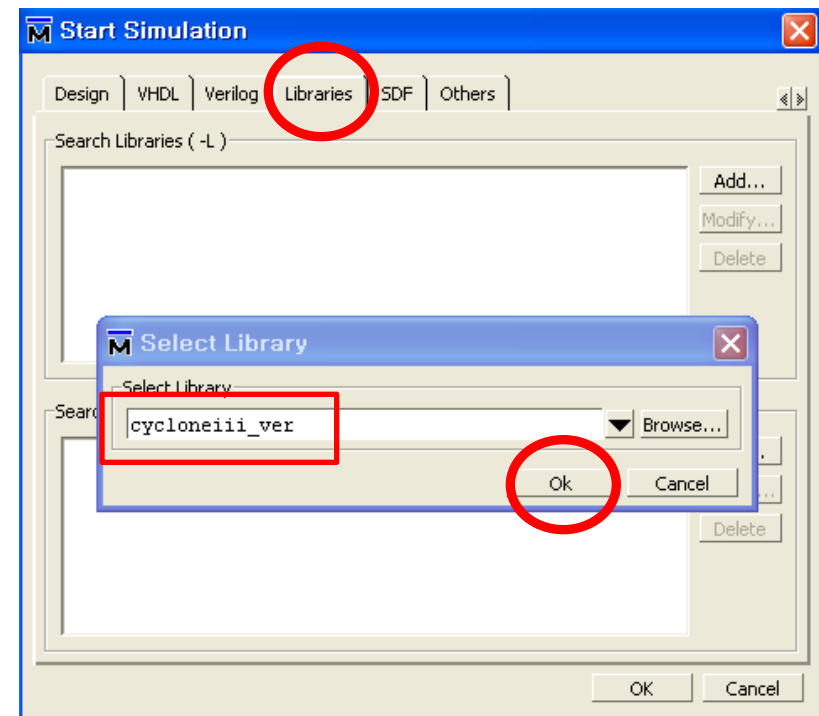


Gate Level 시뮬레이션 시 문제 해결

라이브러리 찾지 못하는 에러 발생



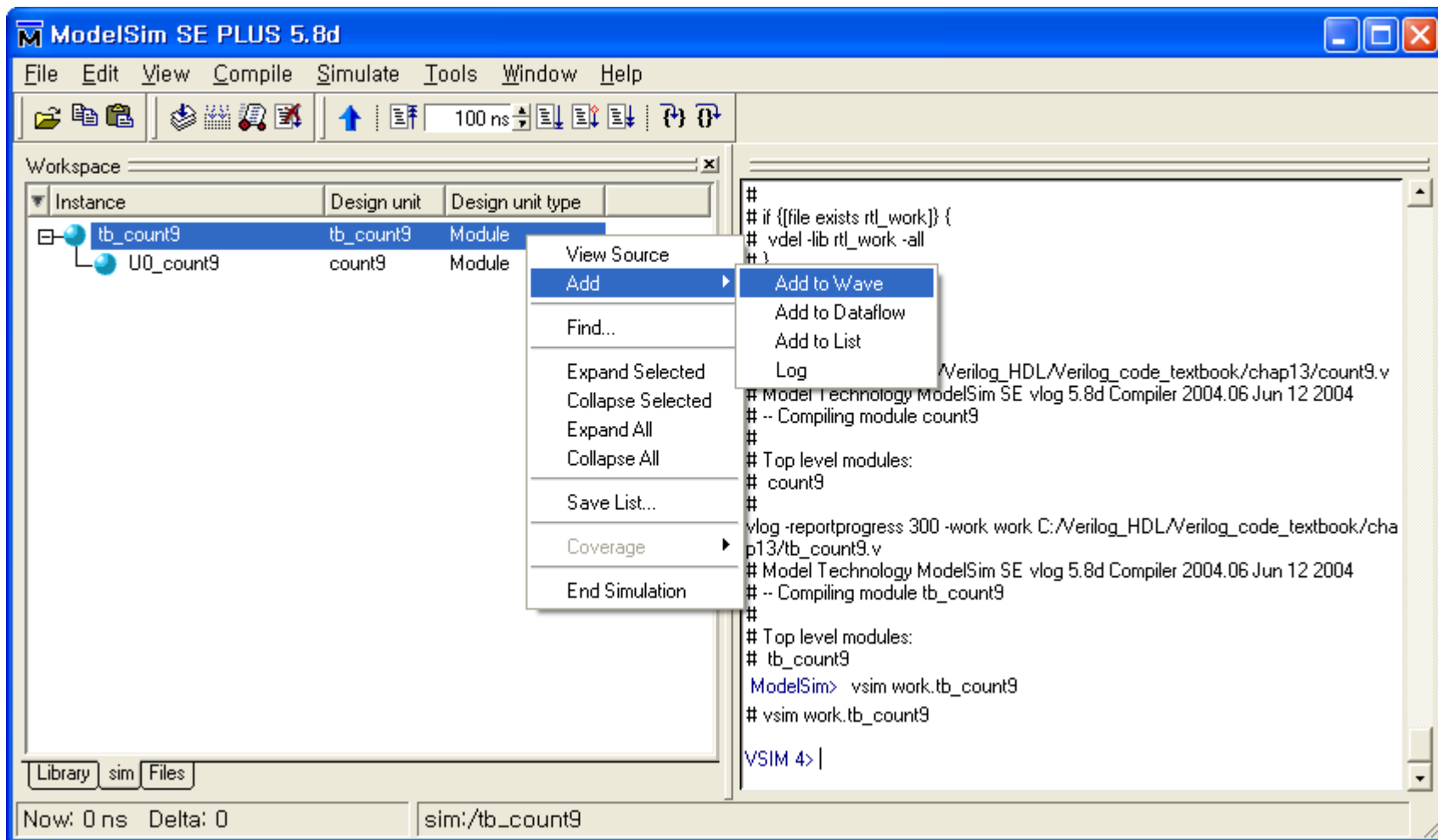
그럼 처럼 **work space**에서
해당 라이브러리 존재함을 확인





ModelSim을 이용한 시뮬레이션

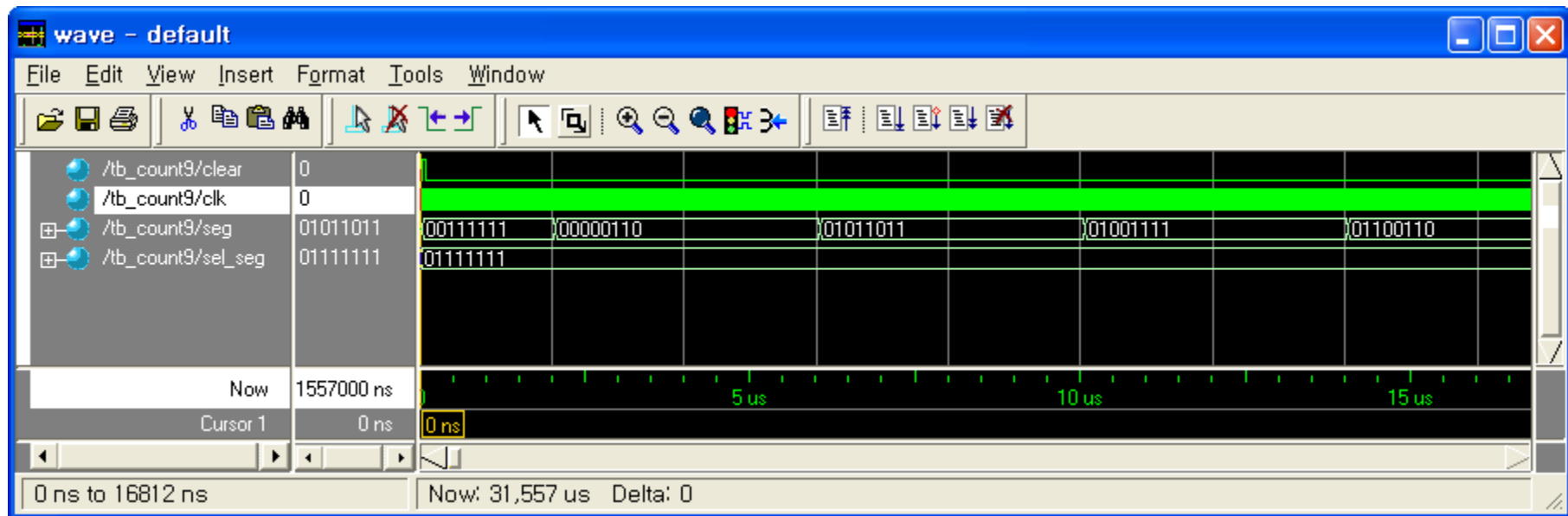
◆ Waveform 창에 신호 추가하기





ModelSim을 이용한 시뮬레이션

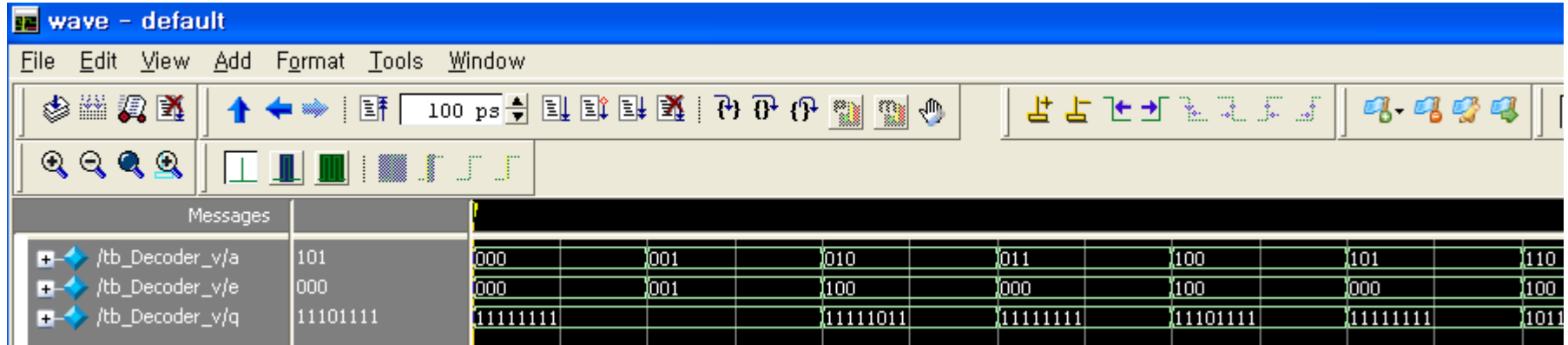
◆ ModelSim 시뮬레이션 결과



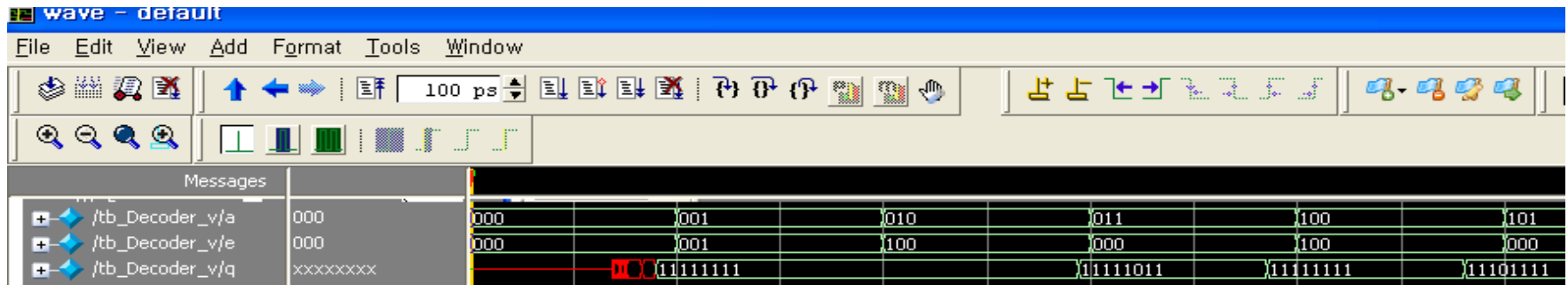


ModelSim을 이용한 시뮬레이션

Functional 한 RTL 시뮬레이션 결과



Gate-level 시뮬레이션 결과 : 실제 Gate 의 계산 결과 시간을 확인 가능

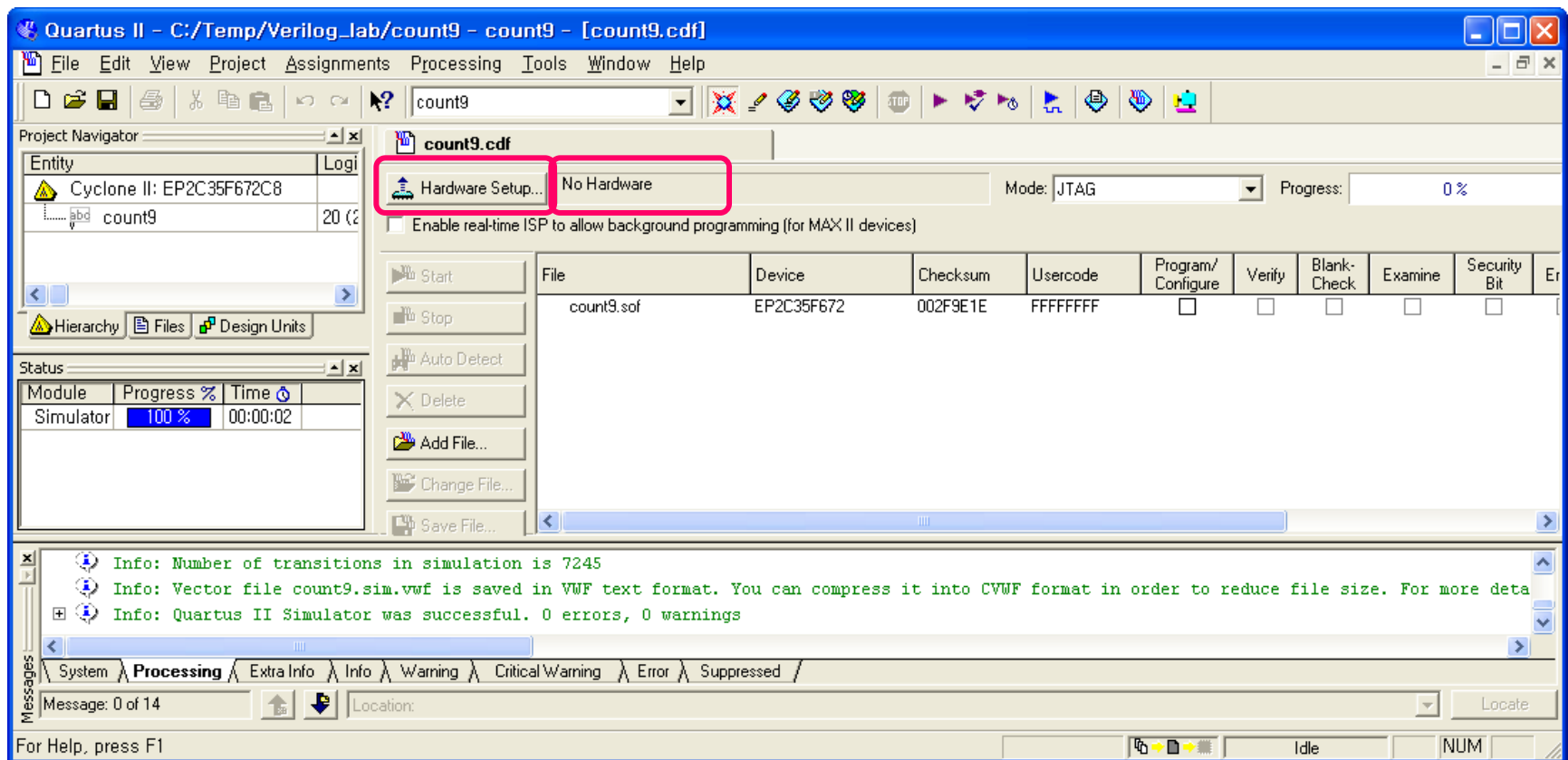




디바이스 프로그래밍

□ 프로그래밍 하드웨어 설정

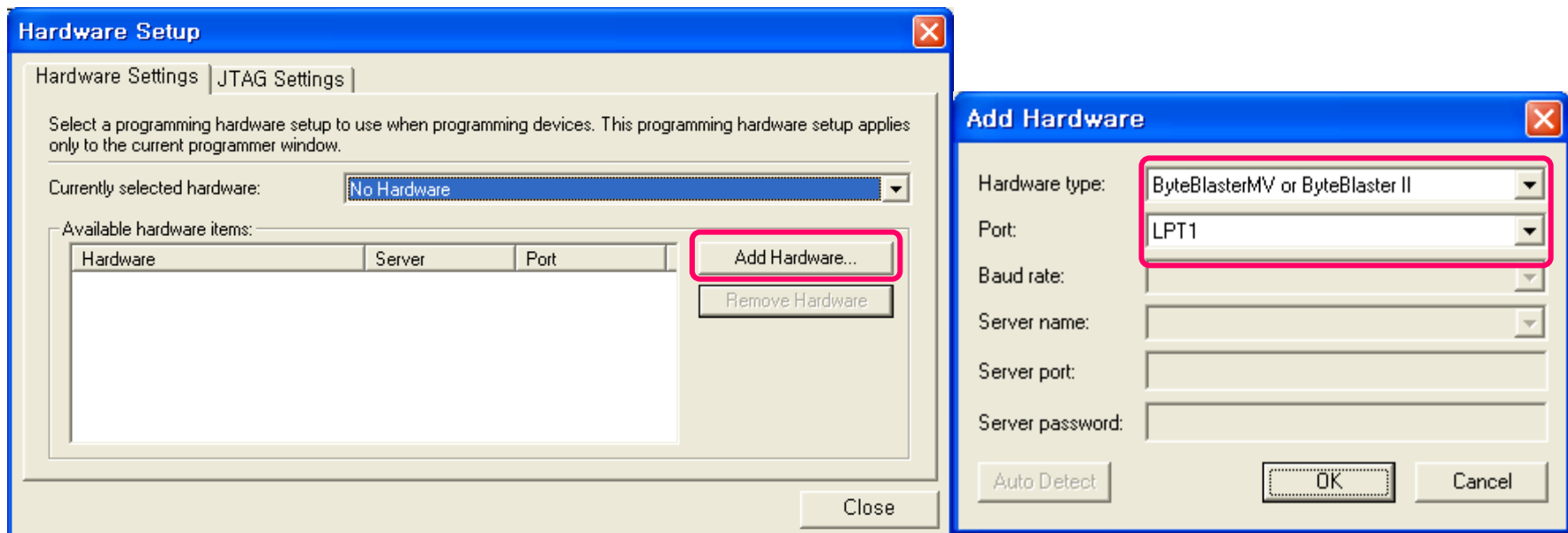
◆ Tools -> Programmer -> Hardware Setup





디바이스 프로그래밍

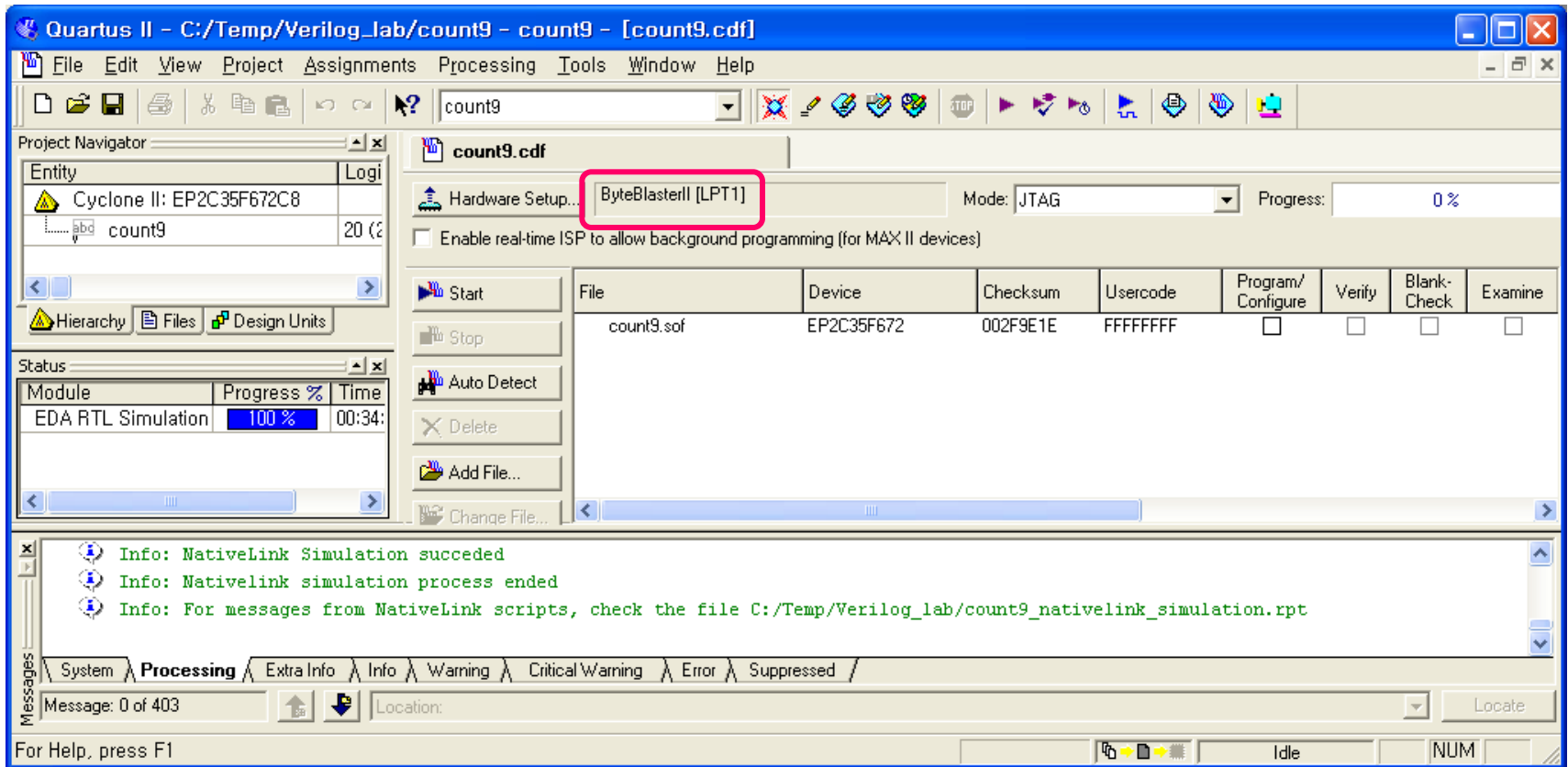
□ 프로그래밍 하드웨어 설정





디바이스 프로그래밍

□ 프로그래밍 하드웨어 설정이 완료된 상태





디바이스 프로그래밍

□ 디바이스 프로그래밍

Quartus II - C:/Temp/Verilog_lab/count9 - count9 - [count9.cdf*]

File Edit View Project Assignments Processing Tools Window Help

count9

Project Navigator

Entity	Logi
Cyclone II: EP2C35F672C8	
count9	20 (2)

Hardware Setup... ByteBlasterII [LPT1] Mode: JTAG Progress: 100 %

☐ Enable real-time ISP to allow background programming (for MAX II devices)

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine
count9.sof	EP2C35F672	002F9E1E	FFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Start Stop Auto Detect Delete Add File... Change File...

Status

Module	Progress %	Time
EDA RTL Simulation	100 %	00:34

Messages

- Info: Device 1 contains JTAG ID code 0x020B40DD
- Info: Configuration succeeded -- 1 device(s) configured
- Info: Successfully performed operation(s)
- Info: Ended Programmer operation at Sat Oct 27 22:17:25 2007

System Processing Extra Info Info Warning Critical Warning Error Suppressed

Message: 0 of 10 Location: Locate

For Help, press F1

Idle NUM

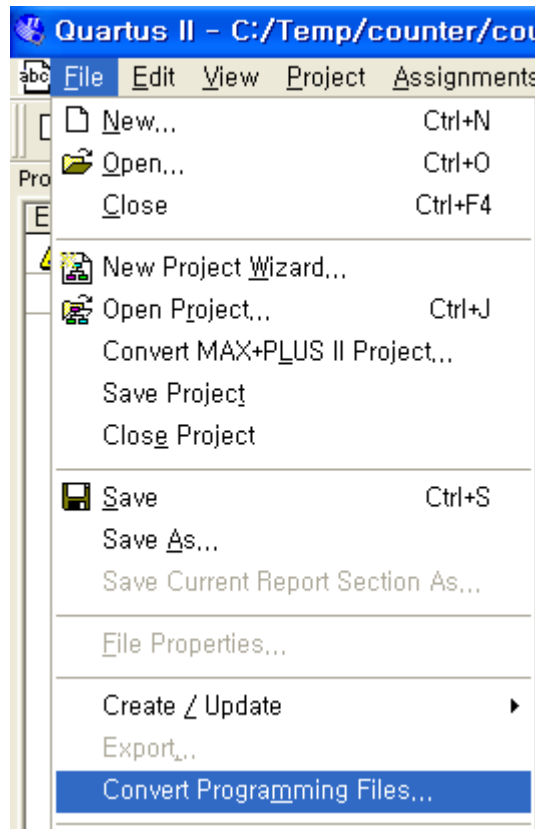




디바이스 프로그래밍

□ PROM 프로그래밍

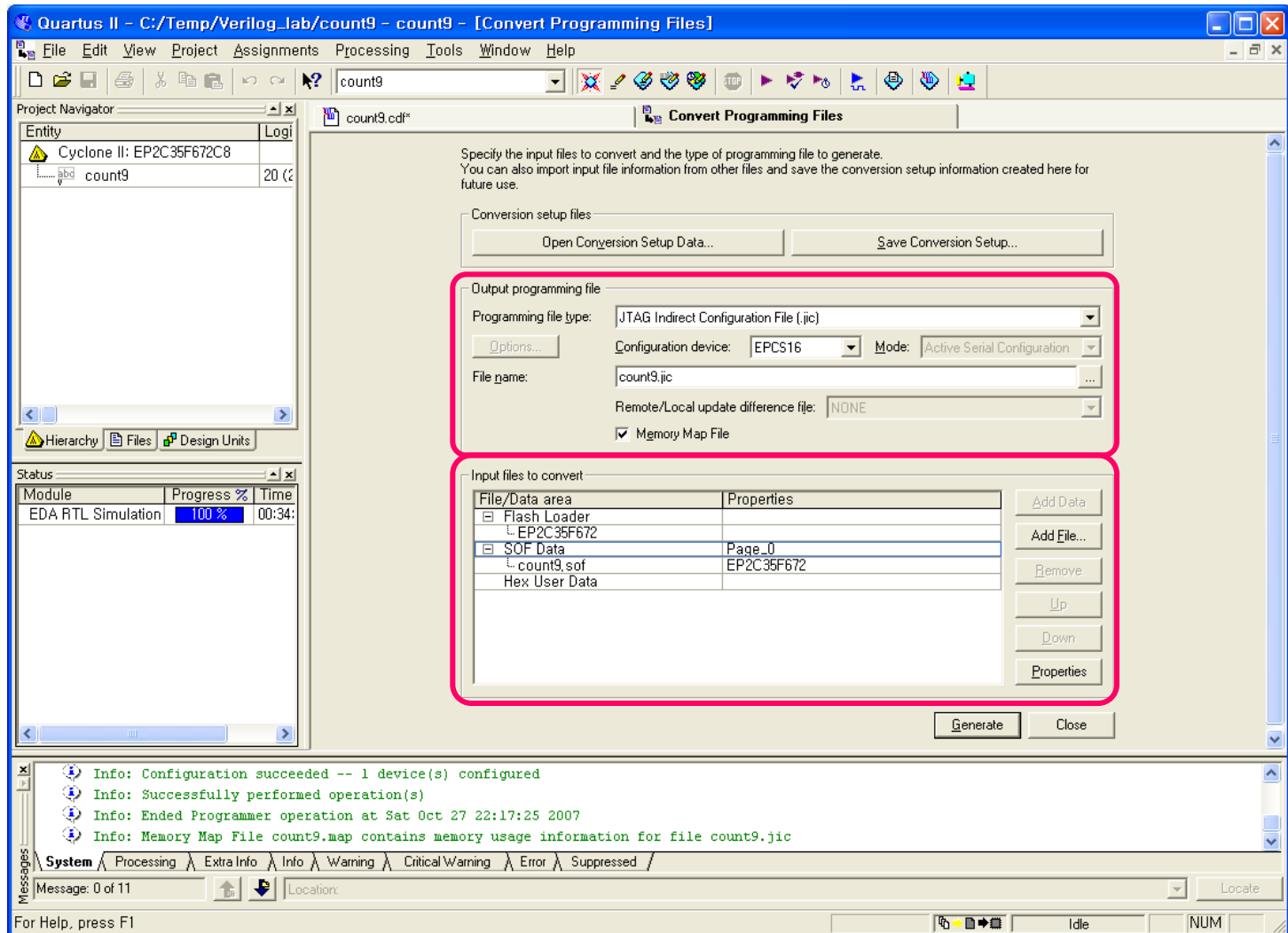
◆ File -> Convert Programming Files





디바이스 프로그래밍

◆ .sof 파일을 .jic 파일로 변환





디바이스 프로그래밍

◆ PROM 프로그래밍

Quartus II - C:/Temp/Verilog_lab/count9 - count9 - [count9.cdf*]

File Edit View Project Assignments Processing Tools Window Help

count9

Project Navigator

Entity	Logi
Cyclone II: EP2C35F672C8	
count9	20 (2

Hierarchy Files Design Units

Status

Module	Progress %	Time
EDA RTL Simulation	100 %	00:34:

Hardware Setup... ByteBlasterII (LPT1) Mode: JTAG Progress: 100 %

Enable real-time ISP to allow background programming (for MAX II devices)

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Er
count9.jic	EP2C35	00301460	FFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
EPCS16				<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

Start Stop Auto Detect Delete Add File...

Info: Configuration succeeded -- 1 device(s) configured
Info: Successfully performed operation(s)
Info: Ended Programmer operation at Sat Oct 27 22:17:25 2007
Info: Memory Map File count9.map contains memory usage information for file count9.jic

System Processing Extra Info Info Warning Critical Warning Error Suppressed

Message: 0 of 11 Location: Locate

For Help, press F1

Idle NUM

