TB_SC_CC_STIM_V00

SCHEMATICs

00. HISTORY
01.CURRENT MIRROR
02.STEP_UP
03.STIM
04.PEAK DETECTION

REVISION HISTORY

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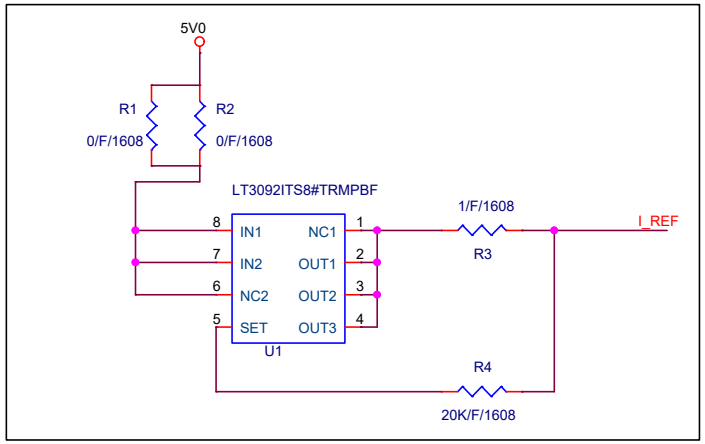
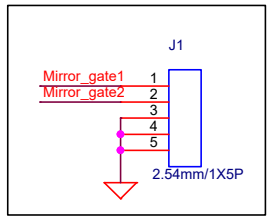
CURRENT MIRROR

CURRENT SOURCE

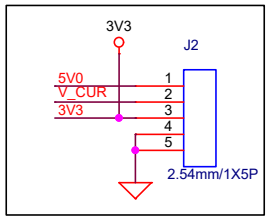


VDDH = 1~40V
I_REF = 0.5mA~200mA
I_CURRENT = 35uA ~ 1.3mA

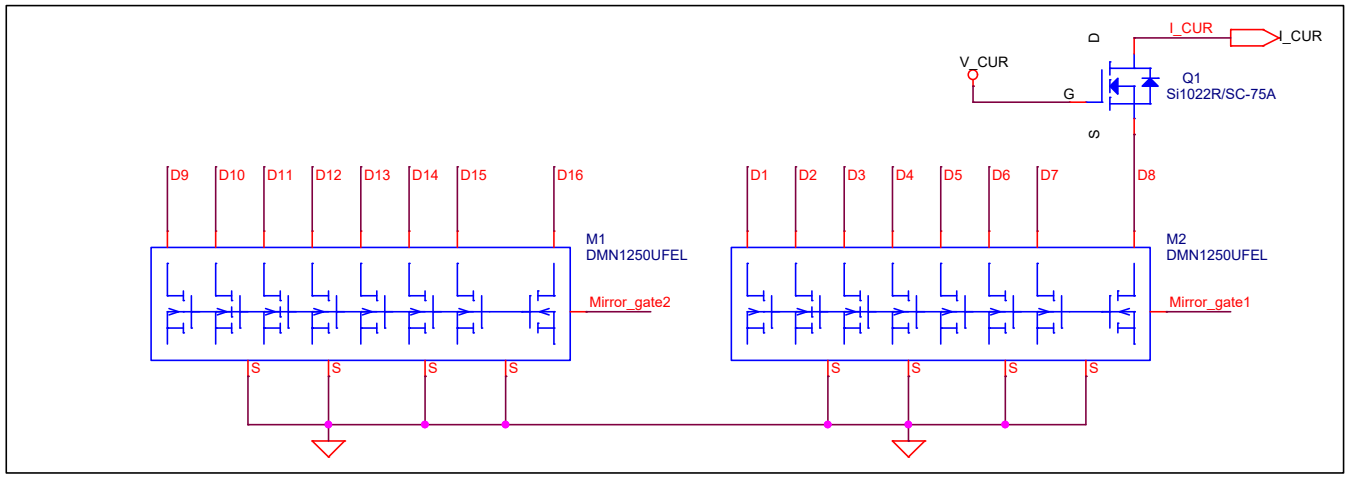
CURRENT SOURCE INPUT_1



CURRENT SOURCE INPUT_2

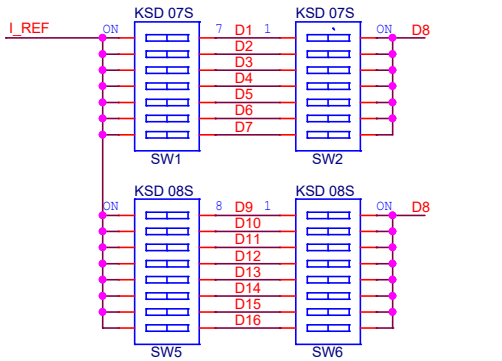


Current mirror control

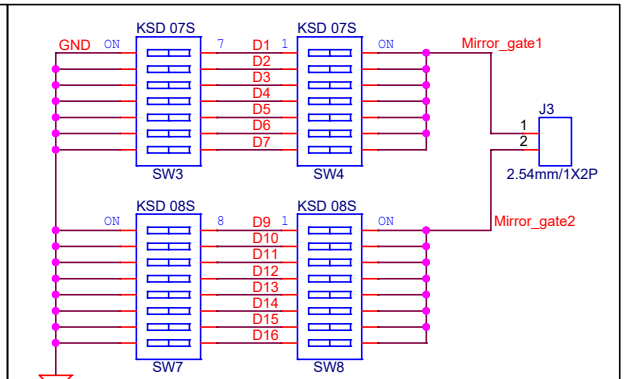


1. Vgs(th) = 0.4~1V (최소 채널 형성 전압)
2.Rds(on)=280~450mΩ,Vgs=4.5V,ID= 0.2A
3.Id (TA = +25°C,Id=2.0A)->Id=1A
4.P=id^2*Rds = 1.0*1.0*0.45=0.45W[MAX = 1.25W)
5 IDSS=1μA, VDS=12V,VGS=0V
6.junction 25 +(2.0^2*0.3*100) = 145 < 150도(최대Tj)

CURRENT SOURCE TO DRAIN



GATE TO DRAIN



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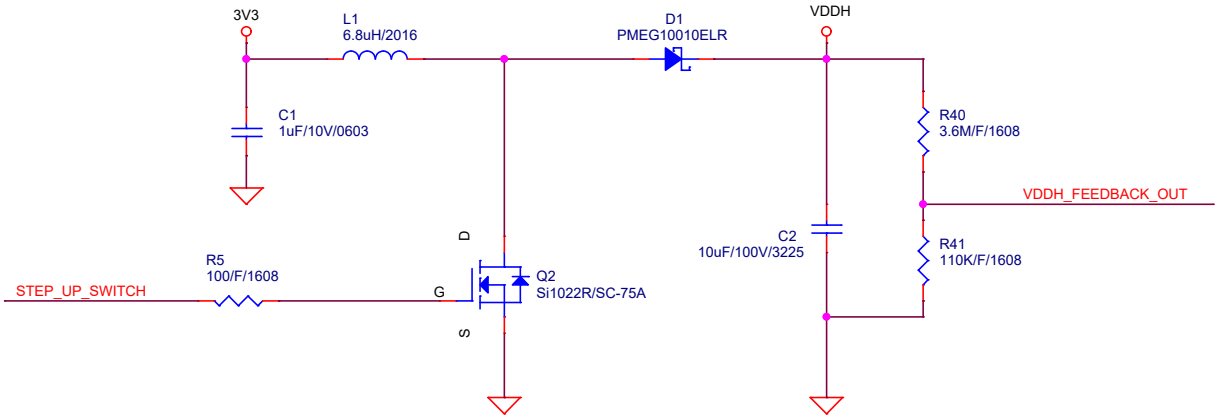
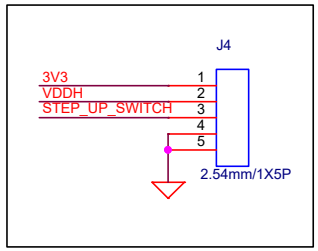
STEP UP



STEP UP_INPUT_1



Range

- VDC : 15Vdc ~ 50Vdc
- Function generator (STEP_UP_SWITCH)
- FPGA (STIM_CH_ON / STIM_REF_ON)

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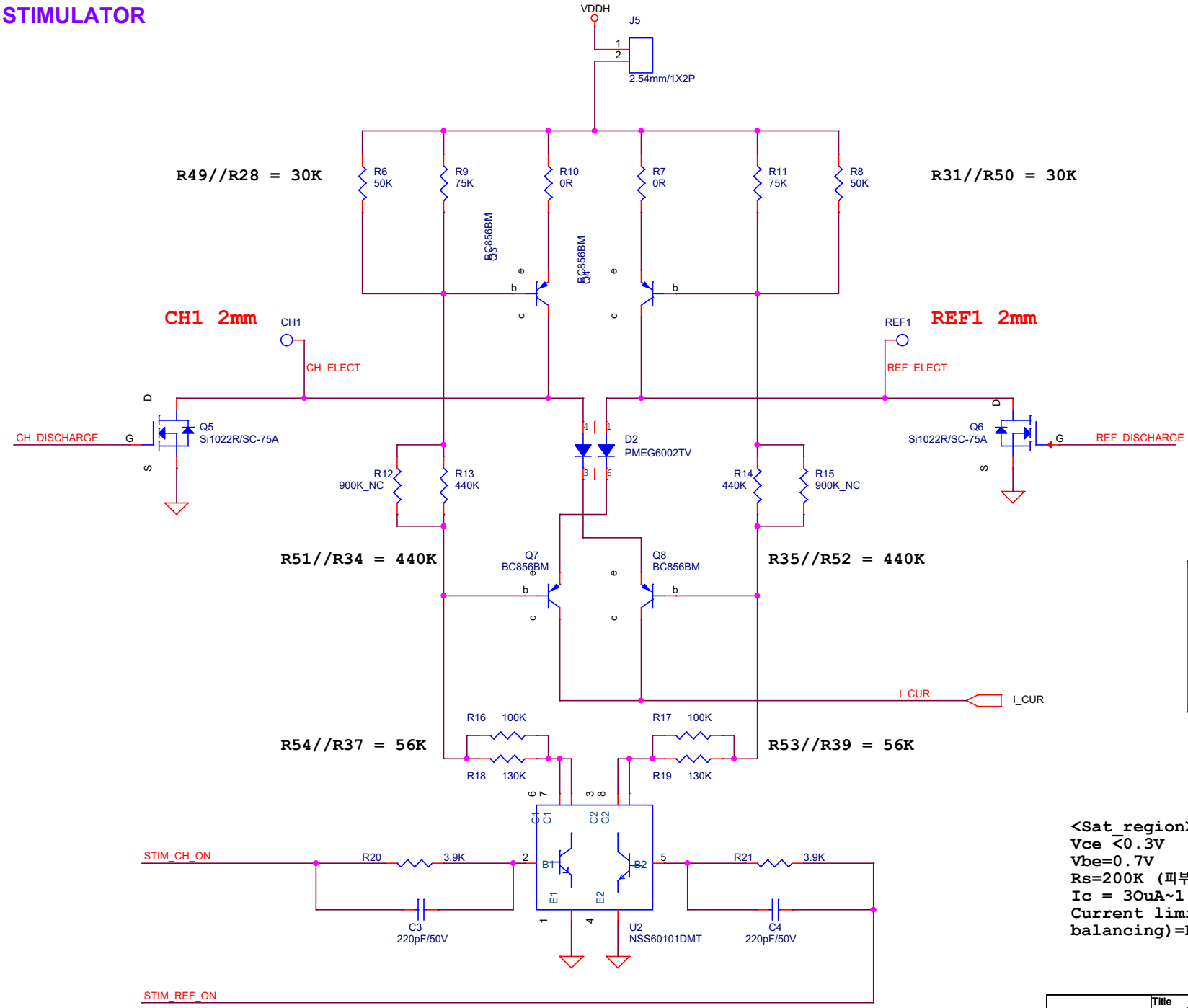
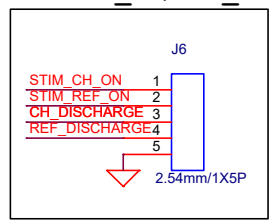
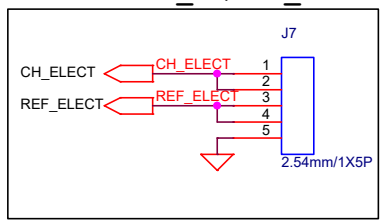
STIMULATOR



STIMULATOR_CH/REF_IN



STIMULATOR_CH/REF_OUT



<Sat_region>
Vce <0.3V
Vbe=0.7V
Rs=200K (피부)
Ic = 3OuA~1.3mA (LT3092 0.5mA~200mA)
Current limit(charge balancing)=REF/CH_DISCHARGE

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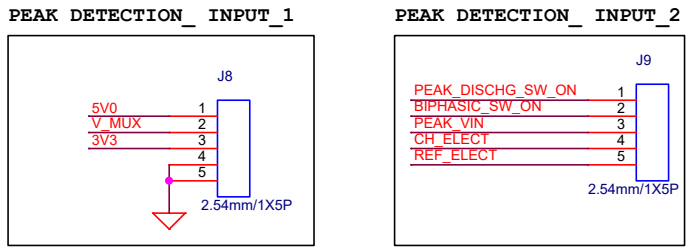
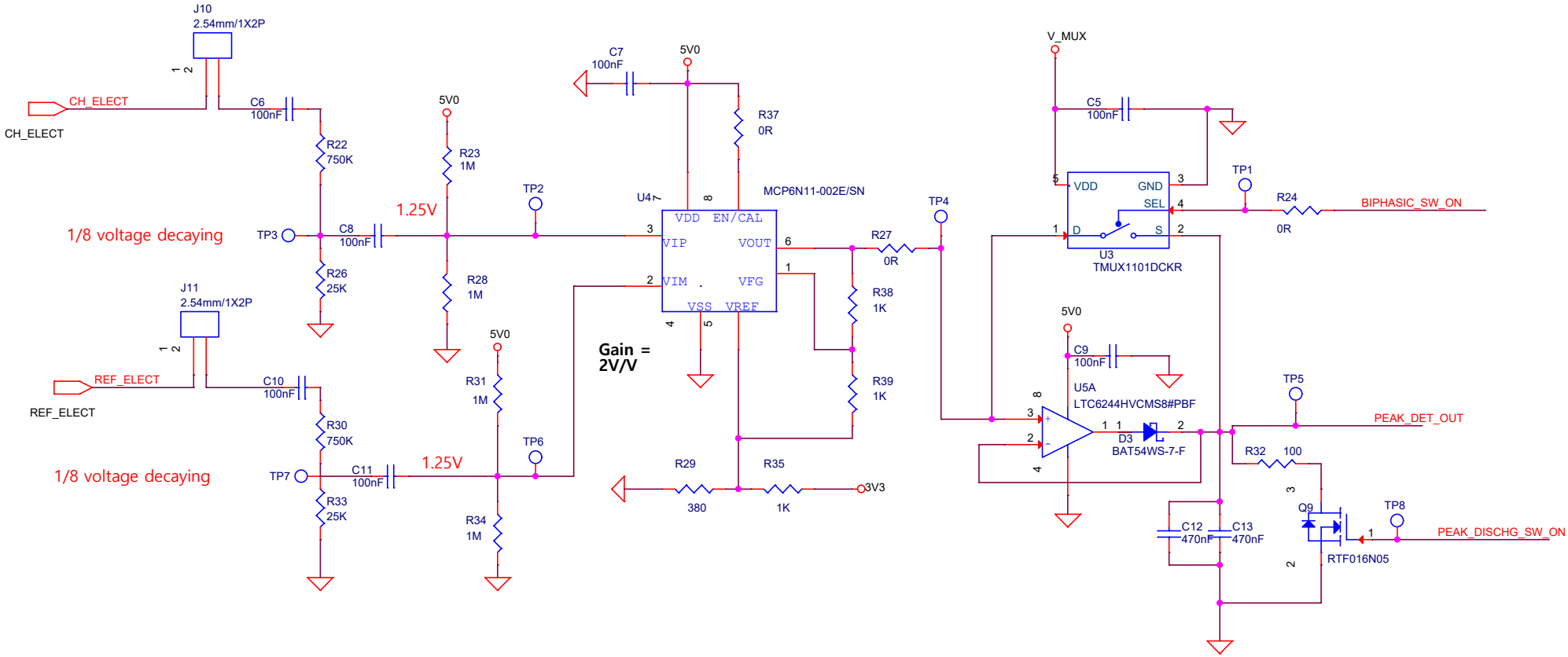
PEAK DETECTION





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