

EPS FPGA

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5.5.1.406 PIN_U21	101
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5.8 PWM_submodule.vhd File Reference	108
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Chapter 1

Hierarchical Index

1.1 Design Unit Hierarchy

Here is a hierarchical list of all entities:

DE0_CV_golden_top	17
MPPT	25
adc	7
adder	10
PWM_submodule	33
sixteenBitComparator	35
eightBitComparator	20
fourBitComparator	23

Chapter 2

Design Unit Index

2.1 Design Unit List

Here is a list of all design unit members with links to the Entities they belong to:

entity adc	7
entity adder	10
architecture arch	12
architecture arch	14
architecture arch	15
architecture arch	16
entity DE0_CV_golden_top	17
entity eightBitComparator	20
entity fourBitComparator	23
entity MPPT	25
architecture MPPT	28
architecture PWM	32
entity PWM_submodule	33
entity sixteenBitComparator	35
architecture struct	38
architecture top	38

Chapter 3

File Index

3.1 File List

Here is a list of all files with brief descriptions:

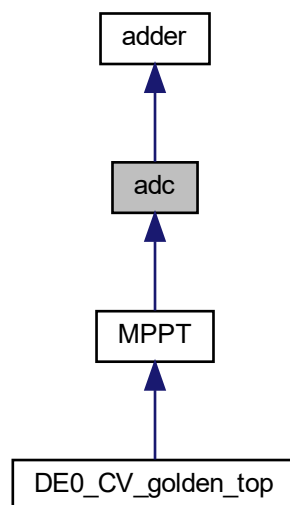
ADC.vhd	41
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DE0_CV_golden_top.vhd	41
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sixteenBitComparator.vhd	108

Chapter 4

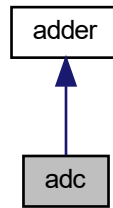
Design Unit Documentation

4.1 adc Entity Reference

Inheritance diagram for adc:



Collaboration diagram for adc:



Entities

- [arch](#) architecture

Libraries

- [ieee](#)

Use Clauses

- [std_logic_1164](#)
- [numeric_std](#)

Ports

- [clk](#) **in** [std_logic](#)
- [gpio1](#) **out** [std_logic_vector](#)([35](#) **downto** [0](#))
- [result_sig_out](#) **out** [std_logic_vector](#)([7](#) **downto** [0](#))
- [add_sub_sig](#) **in** [std_logic](#)

4.1.1 Member Data Documentation

4.1.1.1 add_sub_sig

[add_sub_sig](#) **in** [std_logic](#) [Port]

4.1.1.2 clk

```
clk in std_logic [Port]
```

4.1.1.3 gpio1

```
gpio1 out std_logic_vector( 35 downto 0 ) [Port]
```

4.1.1.4 ieee

```
ieee [Library]
```

4.1.1.5 numeric_std

```
numeric_std [use clause]
```

4.1.1.6 result_sig_out

```
result_sig_out out std_logic_vector( 7 downto 0 ) [Port]
```

4.1.1.7 std_logic_1164

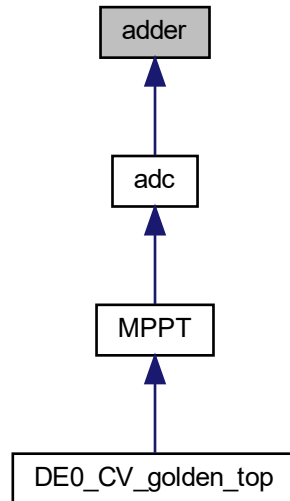
```
std_logic_1164 [use clause]
```

The documentation for this design unit was generated from the following file:

- [ADC.vhd](#)

4.2 adder Entity Reference

Inheritance diagram for adder:



Entities

- [arch](#) architecture

Libraries

- [ieee](#)

Use Clauses

- [std_logic_1164](#)
- [numeric_std](#)

Ports

- [clock](#) **in** [std_logic](#)
- [add_sub](#) **in** [std_logic](#)
- [dataa](#) **in** [std_logic_vector](#)([7](#) **downto** [0](#))
- [datab](#) **in** [std_logic_vector](#)([7](#) **downto** [0](#))
- [result](#) **out** [std_logic_vector](#)([7](#) **downto** [0](#))

4.2.1 Member Data Documentation

4.2.1.1 add_sub

```
add_sub in std_logic [Port]
```

4.2.1.2 clock

```
clock in std_logic [Port]
```

4.2.1.3 dataa

```
dataa in std_logic_vector( 7 downto 0 ) [Port]
```

4.2.1.4 datab

```
datab in std_logic_vector( 7 downto 0 ) [Port]
```

4.2.1.5 ieee

```
ieee [Library]
```

4.2.1.6 numeric_std

```
numeric_std [use clause]
```

4.2.1.7 result

```
result out std_logic_vector( 7 downto 0 ) [Port]
```

4.2.1.8 std_logic_1164

`std_logic_1164` [use clause]

The documentation for this design unit was generated from the following file:

- [adder.vhd](#)

4.3 arch Architecture Reference

Architecture >> [arch](#)

Processes

- [rotator](#)([clk](#))

Components

- [adder](#)

Types

- [byte_arr](#) ([7 downto 0](#)) [std_logic_vector](#)([7 downto 0](#))

Signals

- [dataa_arr](#) [byte_arr](#)
- [rotate](#) [std_logic_vector](#)([7 downto 0](#)) := "10000000 "
- [sel_sig](#) [std_logic_vector](#)([2 downto 0](#))
- [result_sig](#) [std_logic_vector](#)([7 downto 0](#))

Instantiations

- [adder_inst](#) [adder](#)

4.3.1 Member Function Documentation

4.3.1.1 rotator()

```
rotator(
    clk    ) [Process]
```

4.3.2 Member Data Documentation

4.3.2.1 adder

`adder` [Component]

4.3.2.2 adder_inst

`adder_inst` `adder` [Instantiation]

4.3.2.3 byte_arr

`byte_arr` (`7` `downto` `0`) `std_logic_vector`(`7` `downto` `0`) [Type]

4.3.2.4 dataa_arr

`dataa_arr` `byte_arr` [Signal]

4.3.2.5 result_sig

`result_sig` `std_logic_vector`(`7` `downto` `0`) [Signal]

4.3.2.6 rotate

`rotate` `std_logic_vector`(`7` `downto` `0`) := " 10000000 " [Signal]

4.3.2.7 sel_sig

`sel_sig` `std_logic_vector`(`2` `downto` `0`) [Signal]

The documentation for this design unit was generated from the following file:

- [ADC.vhd](#)

4.4 arch Architecture Reference

Architecture >> [arch](#)

Processes

- [artih](#)([all](#))

Signals

- [u_dataa](#) unsigned([7 downto 0](#)):=unsigned([dataa](#))
- [u_datab](#) unsigned([7 downto 0](#)):=unsigned([datab](#))
- [u_result](#) unsigned([7 downto 0](#))

4.4.1 Member Function Documentation

4.4.1.1 artih()

```
artih(  
    all ) [Process]
```

4.4.2 Member Data Documentation

4.4.2.1 u_dataa

```
u\_dataa unsigned( 7 downto 0 ):=unsigned(dataa ) [Signal]
```

4.4.2.2 u_datab

```
u\_datab unsigned( 7 downto 0 ):=unsigned(datab ) [Signal]
```


4.4.2.3 u_result

`u_result` unsigned(7 downto 0) [Signal]

The documentation for this design unit was generated from the following file:

- [adder.vhd](#)

4.5 arch Architecture Reference

Architecture >> [arch](#)

Components

- [fourBitComparator](#)

Signals

- [carryOver](#) std_logic_vector(2 downto 0)

Instantiations

- [comp1](#) fourBitComparator
- [comp2](#) fourBitComparator

4.5.1 Member Data Documentation

4.5.1.1 carryOver

`carryOver` std_logic_vector(2 downto 0) [Signal]

4.5.1.2 comp1

`comp1` fourBitComparator [Instantiation]

4.5.1.3 comp2

`comp2 fourBitComparator` [Instantiation]

4.5.1.4 fourBitComparator

`fourBitComparator` [Component]

The documentation for this design unit was generated from the following file:

- [eightBitComparator.vhd](#)

4.6 arch Architecture Reference

Architecture >> [arch](#)

Components

- [eightBitComparator](#)

Signals

- `carryOver` `std_logic_vector(2 downto 0)`

Instantiations

- `comp1` `eightBitComparator`
- `comp2` `eightBitComparator`

4.6.1 Member Data Documentation

4.6.1.1 carryOver

`carryOver` `std_logic_vector(2 downto 0)` [Signal]

4.6.1.2 comp1

`comp1` `eightBitComparator` [Instantiation]

4.6.1.3 comp2

`comp2` `eightBitComparator` [Instantiation]

4.6.1.4 eightBitComparator

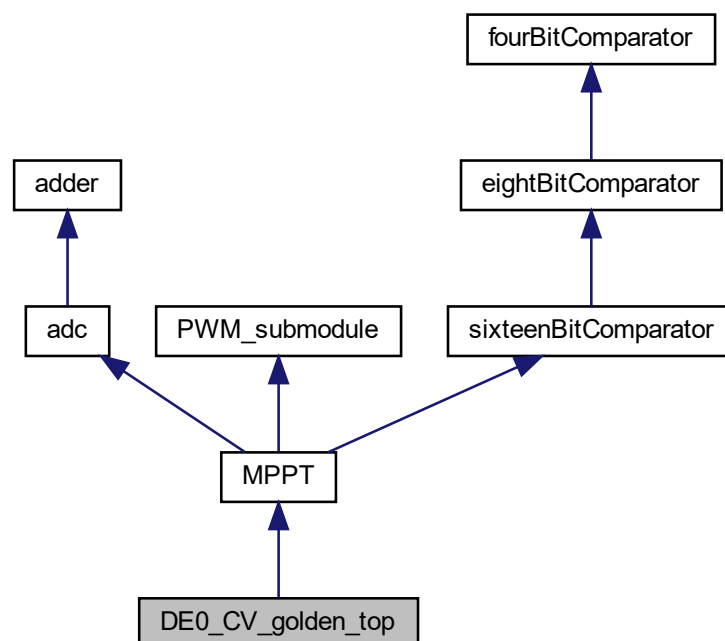
`eightBitComparator` [Component]

The documentation for this design unit was generated from the following file:

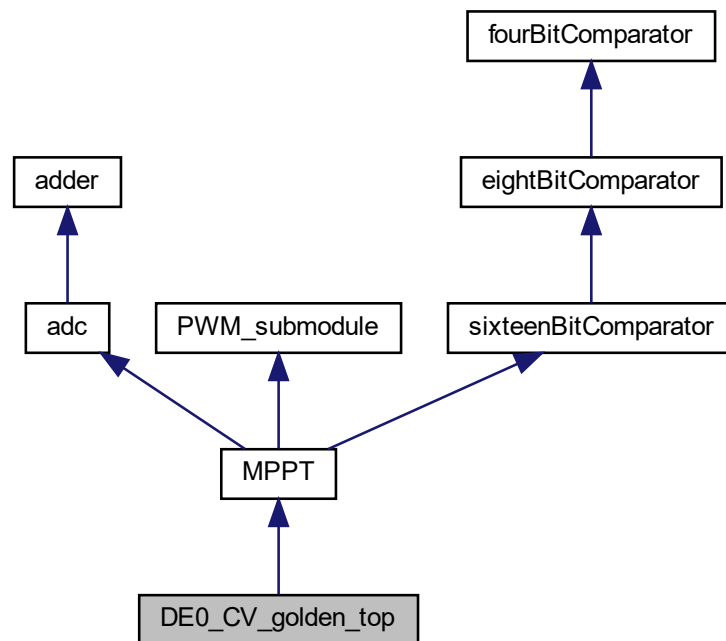
- [sixteenBitComparator.vhd](#)

4.7 DE0_CV_golden_top Entity Reference

Inheritance diagram for DE0_CV_golden_top:



Collaboration diagram for DE0_CV_golden_top:



Entities

- [top](#) architecture

Libraries

- [ieee](#)

Use Clauses

- [std_logic_1164](#)
- [numeric_std](#)
- [std_logic_unsigned](#)

Ports

- `CLOCK2_50` in `std_logic`
- `GPIO_0` in `std_logic_vector(35 downto 0)`
- `GPIO_1` out `std_logic_vector(35 downto 0)`
- `KEY` in `std_logic_vector(3 downto 0)`
- `LEDR` out `std_logic_vector(9 downto 0)`
- `SW` in `std_logic_vector(9 downto 0)`

4.7.1 Member Data Documentation

4.7.1.1 CLOCK2_50

`CLOCK2_50` `in` `std_logic` [Port]

4.7.1.2 GPIO_0

`GPIO_0` `in` `std_logic_vector`(`35` `downto` `0`) [Port]

4.7.1.3 GPIO_1

`GPIO_1` `out` `std_logic_vector`(`35` `downto` `0`) [Port]

4.7.1.4 ieee

`ieee` [Library]

4.7.1.5 KEY

`KEY` `in` `std_logic_vector`(`3` `downto` `0`) [Port]

4.7.1.6 LEDR

`LEDR` `out` `std_logic_vector`(`9` `downto` `0`) [Port]

4.7.1.7 numeric_std

`numeric_std` [use clause]

4.7.1.8 std_logic_1164

`std_logic_1164` [use clause]

4.7.1.9 std_logic_unsigned

`std_logic_unsigned` [use clause]

4.7.1.10 SW

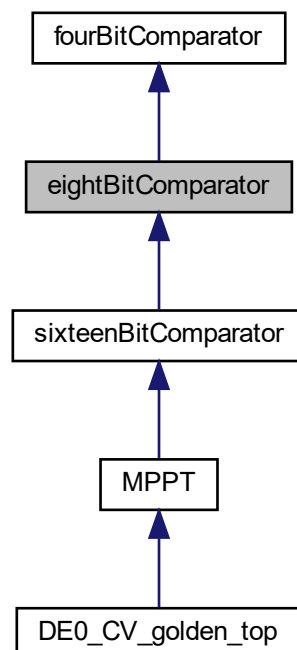
`SW in std_logic_vector(9 downto 0)` [Port]

The documentation for this design unit was generated from the following file:

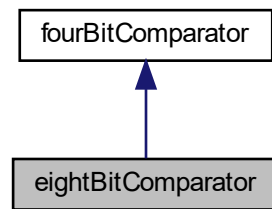
- [DE0_CV_golden_top.vhd](#)

4.8 eightBitComparator Entity Reference

Inheritance diagram for eightBitComparator:



Collaboration diagram for eightBitComparator:



Entities

- [arch](#) architecture

Libraries

- [ieee](#)
- [altera](#)

Use Clauses

- [std_logic_1164](#)
- [altera_syn_attributes](#)

Ports

- `saveA` **in** `std_logic_vector(7 downto 0)`
- `saveB` **in** `std_logic_vector(7 downto 0)`
- `exIn` **in** `std_logic_vector(2 downto 0)`
- `exOut` **out** `std_logic_vector(2 downto 0)`

4.8.1 Member Data Documentation

4.8.1.1 altera

`altera` [Library]

4.8.1.2 altera_syn_attributes

`altera_syn_attributes` [use clause]

4.8.1.3 exIn

`exIn` `in` `std_logic_vector`(`2` `downto` `0`) [Port]

4.8.1.4 exOut

`exOut` `out` `std_logic_vector`(`2` `downto` `0`) [Port]

4.8.1.5 ieee

`ieee` [Library]

4.8.1.6 saveA

`saveA` `in` `std_logic_vector`(`7` `downto` `0`) [Port]

4.8.1.7 saveB

`saveB` `in` `std_logic_vector`(`7` `downto` `0`) [Port]

4.8.1.8 std_logic_1164

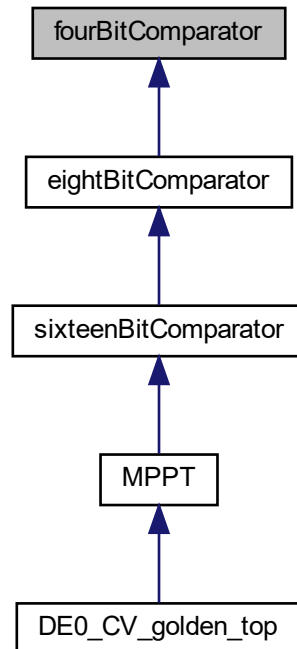
`std_logic_1164` [use clause]

The documentation for this design unit was generated from the following file:

- `eightBitComparator.vhd`

4.9 fourBitComparator Entity Reference

Inheritance diagram for fourBitComparator:



Entities

- [struct](#) architecture

Libraries

- [ieee](#)
- [altera](#)

Use Clauses

- [std_logic_1164](#)
- [altera_syn_attributes](#)

Ports

- **A** in std_logic_vector(**3** downto **0**)
- **B** in std_logic_vector(**3** downto **0**)
- **ind** in std_logic_vector(**2** downto **0**)
- **ud** out std_logic_vector(**2** downto **0**)

4.9.1 Member Data Documentation

4.9.1.1 A

`A` in `std_logic_vector(3 downto 0)` [Port]

4.9.1.2 altera

`altera` [Library]

4.9.1.3 altera_syn_attributes

`altera_syn_attributes` [use clause]

4.9.1.4 B

`B` in `std_logic_vector(3 downto 0)` [Port]

4.9.1.5 ieee

`ieee` [Library]

4.9.1.6 ind

`ind` in `std_logic_vector(2 downto 0)` [Port]

4.9.1.7 std_logic_1164

`std_logic_1164` [use clause]

4.9.1.8 ud

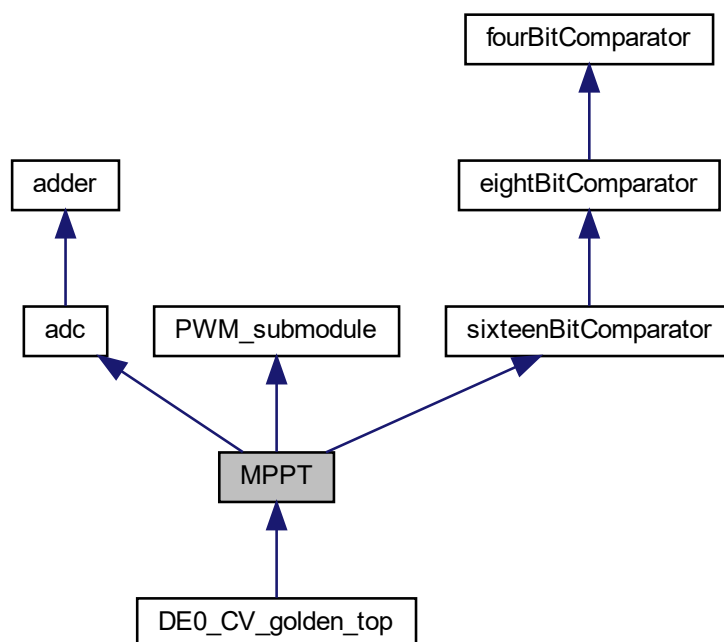
```
ud out std_logic_vector( 2 downto 0 ) [Port]
```

The documentation for this design unit was generated from the following file:

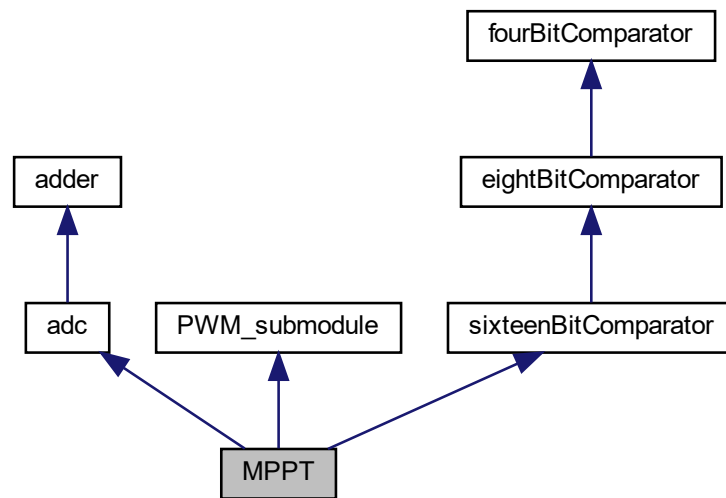
- [fourBitComparator.vhd](#)

4.10 MPPT Entity Reference

Inheritance diagram for MPPT:



Collaboration diagram for MPPT:



Entities

- [MPPT](#) architecture

Libraries

- [ieee](#)

Use Clauses

- [std_logic_1164](#)
- [numeric_std](#)

Ports

- [ADC_Volt_out](#) **out** [std_logic_vector\(7 downto 0 \)](#)
- [ADC_Curr_out](#) **out** [std_logic_vector\(7 downto 0 \)](#)
- [add_sub_sig](#) **in** [std_logic_vector\(1 downto 0 \)](#)
- [main_clk](#) **in** [std_logic](#)
- [PWM_out](#) **out** [std_logic](#)
- [res_sig](#) **out** [std_logic_vector\(7 downto 0 \)](#)

4.10.1 Member Data Documentation

4.10.1.1 ADC_Curr_out

```
ADC_Curr_out out std_logic_vector( 7 downto 0 ) [Port]
```

4.10.1.2 ADC_Volt_out

```
ADC_Volt_out out std_logic_vector( 7 downto 0 ) [Port]
```

4.10.1.3 add_sub_sig

```
add_sub_sig in std_logic_vector( 1 downto 0 ) [Port]
```

4.10.1.4 ieee

```
ieee [Library]
```

4.10.1.5 main_clk

```
main_clk in std_logic [Port]
```

4.10.1.6 numeric_std

```
numeric_std [use clause]
```

4.10.1.7 PWM_out

```
PWM_out out std_logic [Port]
```

4.10.1.8 res_sig

```
res_sig out std_logic_vector( 7 downto 0 ) [Port]
```

4.10.1.9 std_logic_1164

`std_logic_1164` [use clause]

The documentation for this design unit was generated from the following file:

- [MPPT.vhd](#)

4.11 MPPT Architecture Reference

Architecture >> [MPPT](#)

Processes

- [clockscaler](#)([all](#))
Clockscaler: downscale fra main-clk til ADC, for at comparator modulet kan følge med.
- [PWM_clockscaler](#)([all](#))
- [MPPT_algoritme](#)([all](#))
Ganger resultaterne fra de to adc sammen til en repræsentation af effekten.

Components

- [ADC](#)
Herefter opstilles alle submodulerne.
- [sixteenBitComparator](#)
- [PWM_submodule](#)

Signals

- [adc_clk](#) **unsigned**([15 downto 0](#))
Signal til at downscale main clock.
- [result_sig_volt](#) **std_logic_vector**([7 downto 0](#))
Vector til at gemme resultatet fra ADC.
- [result_sig_curr](#) **std_logic_vector**([7 downto 0](#))
Vector til at gemme resultatet fra ADC.
- [result_sig](#) **std_logic_vector**([15 downto 0](#))
Vector til at gemme resultatet fra ADC.
- [vej_h](#) **std_logic**
Værdi, som holder styr på hvilken vej algorithmen lige har gået.
- [result_sig_old](#) **std_logic_vector**([15 downto 0](#)):=**(others=>'0')**
Den forrige værdi for effekten.
- [duty_cycle](#) **unsigned**([6 downto 0](#)):=**(others=>'0')**
Duty cycle som går ned i PWM sub modulet.
- [comp_out](#) **std_logic_vector**([2 downto 0](#))
Outputs fra sixteenbit comparatoren.
- [MPPT_clk](#) **unsigned**([2 downto 0](#)):=**"100"**
Clock for PWM signal.

Instantiations

- `adc_volt adc`
Her kaldes alle instances af submodulerne.
- `adc_curr adc`
ADC til måling af volt over shuntmodstand, hvilket er afhængig af strømmen igennem modstanden.
- `pwm_comp PWM_submodule`
PWM generator til buck/boost converteren.
- `comp1 sixteenBitComparator`
Sixteenbitcomparator til at compare effekten fra solcellerne.

4.11.1 Member Function Documentation

4.11.1.1 clockscaler()

```
clockscaler (
    all )
```

Clockscaler: downscale fra main-clk til ADC, for at comparator modulet kan følge med.

4.11.1.2 MPPT_algoritme()

```
MPPT_algoritme(
    all ) [Process]
```

Ganger resultaterne fra de to adc sammen til en repræsentation af effekten.

4.11.1.3 PWM_clockscaler()

```
PWM_clockscaler(
    all ) [Process]
```

4.11.2 Member Data Documentation

4.11.2.1 ADC

```
ADC [Component]
```

Herefter opstilles alle submodulerne.

4.11.2.2 adc_clk

```
adc_clk unsigned( 15 downto 0 ) [Signal]
```

Signal til at downscale main clock.

4.11.2.3 adc_curr

```
adc_curr adc [Instantiation]
```

ADC til måling af volt over shuntmodstand, hvilket er afhængig af strømmen igennem modstanden.

4.11.2.4 adc_volt

```
adc_volt adc [Instantiation]
```

Her kaldes alle instances af submodulerne.

ADC til måling af volt over solcellerne.

4.11.2.5 comp1

```
comp1 sixteenBitComparator [Instantiation]
```

Sixteenbitcomparator til at compare effekten fra solcellerne.

4.11.2.6 comp_out

```
comp_out std_logic_vector( 2 downto 0 ) [Signal]
```

Outputs fra sixteenbit comparatoren.

4.11.2.7 duty_cycle

```
duty_cycle unsigned( 6 downto 0 ) := (others=>' 0 ') [Signal]
```

Duty cycle som går ned i PWM sub modulet.

4.11.2.8 MPPT_clk

```
MPPT_clk unsigned( 2 downto 0 ) := " 100 " [Signal]
```

Clock for PWM signal.

4.11.2.9 pwm_comp

```
pwm_comp PWM_submodule [Instantiation]
```

PWM generator til buck/boost converteren.

4.11.2.10 PWM_submodule

```
PWM_submodule [Component]
```

4.11.2.11 result_sig

```
result_sig std_logic_vector( 15 downto 0 ) [Signal]
```

Vector til at gemme resultatet fra ADC.

4.11.2.12 result_sig_curr

```
result_sig_curr std_logic_vector( 7 downto 0 ) [Signal]
```

Vector til at gemme resultatet fra ADC.

4.11.2.13 result_sig_old

```
result_sig_old std_logic_vector( 15 downto 0 ) := (others=>' 0 ') [Signal]
```

Den forrige værdi for effekten.

4.11.2.14 result_sig_volt

`result_sig_volt` `std_logic_vector(7 downto 0)` [Signal]

Vector til at gemme resultatet fra ADC.

4.11.2.15 sixteenBitComparator

`sixteenBitComparator` [Component]

4.11.2.16 vej_h

`vej_h` `std_logic` [Signal]

Værdi, som holder styr på hvilken vej algorithmen lige har gået.

The documentation for this design unit was generated from the following file:

- [MPPT.vhd](#)

4.12 PWM Architecture Reference

Architecture >> [PWM](#)

Processes

- [PWM_clockscaler_pro](#)(`clk`)
- [PWM_signal](#)([PWM_clockscaler](#) (`2`))

Signals

- `cnt` `unsigned(6 downto 0)`
- [PWM_clockscaler](#) `unsigned(2 downto 0)`

4.12.1 Member Function Documentation

4.12.1.1 PWM_clockscaler_pro()

```
PWM_clockscaler_pro(  
    clk ) [Process]
```

4.12.1.2 PWM_signal()

```
PWM_signal(  
    PWM_clockscaler ( 2 ) ) [Process]
```

4.12.2 Member Data Documentation

4.12.2.1 cnt

```
cnt unsigned( 6 downto 0 ) [Signal]
```

4.12.2.2 PWM_clockscaler

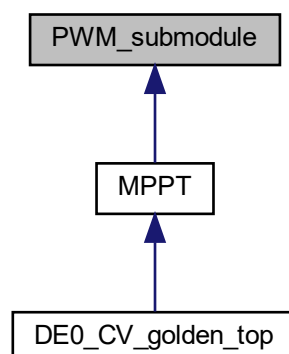
```
PWM_clockscaler unsigned( 2 downto 0 ) [Signal]
```

The documentation for this design unit was generated from the following file:

- [PWM_submodule.vhd](#)

4.13 PWM_submodule Entity Reference

Inheritance diagram for PWM_submodule:



Entities

- [PWM](#) architecture

Libraries

- [ieee](#)

Use Clauses

- [std_logic_1164](#)
- [numeric_std](#)

Ports

- [pwm_out](#) **out** [std_logic](#)
- [duty_cycle](#) **in** [std_logic_vector](#)([6](#) **downto** [0](#))
- [clk](#) **in** [std_logic](#)

4.13.1 Member Data Documentation

4.13.1.1 clk

[clk](#) **in** [std_logic](#) [Port]

4.13.1.2 duty_cycle

[duty_cycle](#) **in** [std_logic_vector](#)([6](#) **downto** [0](#)) [Port]

4.13.1.3 ieee

[ieee](#) [Library]

4.13.1.4 numeric_std

[numeric_std](#) [use clause]

4.13.1.5 pwm_out

`pwm_out` `out` `std_logic` [Port]

4.13.1.6 std_logic_1164

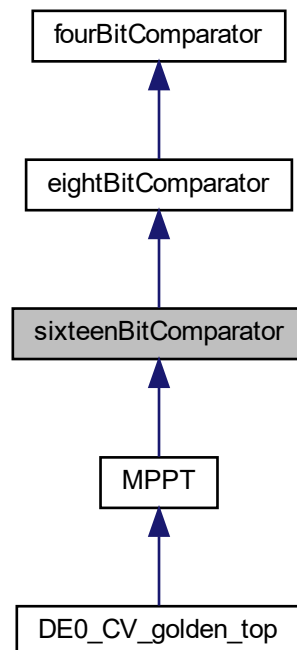
`std_logic_1164` [use clause]

The documentation for this design unit was generated from the following file:

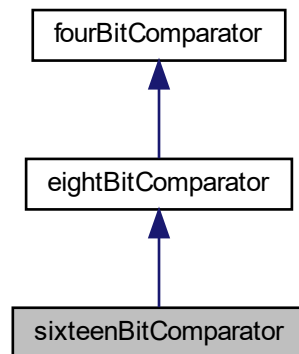
- [PWM_submodule.vhd](#)

4.14 sixteenBitComparator Entity Reference

Inheritance diagram for sixteenBitComparator:



Collaboration diagram for sixteenBitComparator:



Entities

- [arch](#) architecture

Libraries

- [ieee](#)
- [altera](#)

Use Clauses

- [std_logic_1164](#)
- [altera_syn_attributes](#)

Ports

- [saveA16](#) **in** [std_logic_vector](#)(**15** **downto** **0**)
- [saveB16](#) **in** [std_logic_vector](#)(**15** **downto** **0**)
- [exIn16](#) **in** [std_logic_vector](#)(**2** **downto** **0**)
- [exOut16](#) **out** [std_logic_vector](#)(**2** **downto** **0**)

4.14.1 Member Data Documentation

4.14.1.1 altera

[altera](#) [Library]

4.14.1.2 altera_syn_attributes

`altera_syn_attributes` [use clause]

4.14.1.3 exIn16

`exIn16` **in** `std_logic_vector(2 downto 0)` [Port]

4.14.1.4 exOut16

`exOut16` **out** `std_logic_vector(2 downto 0)` [Port]

4.14.1.5 ieee

`ieee` [Library]

4.14.1.6 saveA16

`saveA16` **in** `std_logic_vector(15 downto 0)` [Port]

4.14.1.7 saveB16

`saveB16` **in** `std_logic_vector(15 downto 0)` [Port]

4.14.1.8 std_logic_1164

`std_logic_1164` [use clause]

The documentation for this design unit was generated from the following file:

- [sixteenBitComparator.vhd](#)

4.15 struct Architecture Reference

Architecture >> [struct](#)

Signals

- [tmp](#) `std_logic_vector(0 to 27)`

4.15.1 Member Data Documentation

4.15.1.1 tmp

`tmp std_logic_vector(0 to 27)` [Signal]

The documentation for this design unit was generated from the following file:

- [fourBitComparator.vhd](#)

4.16 top Architecture Reference

Architecture >> [top](#)

Components

- [MPPT](#)

Signals

- [PWM_mes](#) `std_logic`

Instantiations

- [eps_mppt1](#) MPPT

4.16.1 Member Data Documentation

4.16.1.1 eps_mppt1

`eps_mppt1` **MPPT** [Instantiation]

4.16.1.2 MPPT

MPPT [Component]

4.16.1.3 PWM_mes

`PWM_mes` **std_logic** [Signal]

The documentation for this design unit was generated from the following file:

- [DE0_CV_golden_top.vhd](#)

Chapter 5

File Documentation

5.1 ADC.vhd File Reference

Entities

- [adc](#) entity
- [arch](#) architecture

5.2 adder.vhd File Reference

Entities

- [adder](#) entity
- [arch](#) architecture

5.3 DE0_CV_golden_top.vhd File Reference

Entities

- [DE0_CV_golden_top](#) entity
- [top](#) architecture

5.4 eightBitComparator.vhd File Reference

Entities

- [eightBitComparator](#) entity
- [arch](#) architecture

5.5 EPS-ADC.qsf File Reference

Constraints

- FAMILY "CycloneV"
- DEVICE 5CEBA4F23C7
- TOP_LEVEL_ENTITY DE0_CV_golden_top
- ORIGINAL_QUARTUS_VERSION 13
- PROJECT_CREATION_TIME_DATE "MONMAY 5 11 : 54 : 18 2014 "
- LAST_QUARTUS_VERSION " 21 . 1 . 0 LiteEdition"
- PROJECT_OUTPUT_DIRECTORY output_files
- IO_STANDARD " 3 . 3 -VLVTTL"-toCLOCK2_50
- IO_STANDARD " 3 . 3 -VLVTTL"-toCLOCK3_50
- IO_STANDARD " 3 . 3 -VLVTTL"-toCLOCK4_50
- IO_STANDARD " 3 . 3 -VLVTTL"-toCLOCK_50
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[0]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[1]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[2]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[3]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[4]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[5]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[6]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[7]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[8]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[9]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[10]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[11]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_ADDR[12]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_BA[0]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_BA[1]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_CAS_N
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_CKE
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_CLK
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_CS_N
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[0]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[1]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[2]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[3]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[4]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[5]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[6]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[7]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[8]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[9]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[10]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[11]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[12]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[13]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[14]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_DQ[15]
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_LDQM
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_RAS_N
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_UDQM
- IO_STANDARD " 3 . 3 -VLVTTL"-toDRAM_WE_N

- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[0]
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- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[2]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[3]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[4]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[5]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[6]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[7]
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- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[11]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[12]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[13]
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- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[16]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[17]
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- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[27]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[28]
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- IO_STANDARD "3.3-VLVTTL"-toGPIO_0[32]
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- IO_STANDARD "3.3-VLVTTL"-toGPIO_1[16]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_1[17]
- IO_STANDARD "3.3-VLVTTL"-toGPIO_1[18]

- IO_STANDARD "3.3-VLVTTTL"-toGPIO_1[19]
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- IO_STANDARD "3.3-VLVTTTL"-toHEX0[3]
- IO_STANDARD "3.3-VLVTTTL"-toHEX0[4]
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- IO_STANDARD "3.3-VLVTTTL"-toHEX1[2]
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- IO_STANDARD "3.3-VLVTTTL"-toHEX4[3]
- IO_STANDARD "3.3-VLVTTTL"-toHEX4[4]
- IO_STANDARD "3.3-VLVTTTL"-toHEX4[5]
- IO_STANDARD "3.3-VLVTTTL"-toHEX4[6]
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- IO_STANDARD "3.3-VLVTTTL"-toHEX5[1]
- IO_STANDARD "3.3-VLVTTTL"-toHEX5[2]

- IO_STANDARD "3.3-VLVTTTL"-toHEX5[3]
- IO_STANDARD "3.3-VLVTTTL"-toHEX5[4]
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- IO_STANDARD "3.3-VLVTTTL"-toKEY[1]
- IO_STANDARD "3.3-VLVTTTL"-toKEY[2]
- IO_STANDARD "3.3-VLVTTTL"-toKEY[3]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[0]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[1]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[2]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[3]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[4]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[5]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[6]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[7]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[8]
- IO_STANDARD "3.3-VLVTTTL"-toLEDR[9]
- IO_STANDARD "3.3-VLVTTTL"-toPS2_CLK
- IO_STANDARD "3.3-VLVTTTL"-toPS2_CLK2
- IO_STANDARD "3.3-VLVTTTL"-toPS2_DAT
- IO_STANDARD "3.3-VLVTTTL"-toPS2_DAT2
- IO_STANDARD "3.3-VLVTTTL"-toRESET_N
- IO_STANDARD "3.3-VLVTTTL"-toSD_CLK
- IO_STANDARD "3.3-VLVTTTL"-toSD_CMD
- IO_STANDARD "3.3-VLVTTTL"-toSD_DATA[0]
- IO_STANDARD "3.3-VLVTTTL"-toSD_DATA[1]
- IO_STANDARD "3.3-VLVTTTL"-toSD_DATA[2]
- IO_STANDARD "3.3-VLVTTTL"-toSD_DATA[3]
- IO_STANDARD "3.3-VLVTTTL"-toSW[0]
- IO_STANDARD "3.3-VLVTTTL"-toSW[1]
- IO_STANDARD "3.3-VLVTTTL"-toSW[2]
- IO_STANDARD "3.3-VLVTTTL"-toSW[3]
- IO_STANDARD "3.3-VLVTTTL"-toSW[4]
- IO_STANDARD "3.3-VLVTTTL"-toSW[5]
- IO_STANDARD "3.3-VLVTTTL"-toSW[6]
- IO_STANDARD "3.3-VLVTTTL"-toSW[7]
- IO_STANDARD "3.3-VLVTTTL"-toSW[8]
- IO_STANDARD "3.3-VLVTTTL"-toSW[9]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_B[0]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_B[1]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_B[2]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_B[3]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_G[0]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_G[1]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_G[2]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_G[3]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_HS
- IO_STANDARD "3.3-VLVTTTL"-toVGA_R[0]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_R[1]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_R[2]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_R[3]
- IO_STANDARD "3.3-VLVTTTL"-toVGA_VS
- CYCLONEII_RESERVE_NCEO_AFTER_CONFIGURATION "USEASREGULARIO"
- PIN_H13 -toCLOCK2_50

- PIN_E10 -toCLOCK3_50
- PIN_V15 -toCLOCK4_50
- PIN_M9 -toCLOCK_50
- PIN_W8 -toDRAM_ADDR[0]
- PIN_T8 -toDRAM_ADDR[1]
- PIN_U11 -toDRAM_ADDR[2]
- PIN_Y10 -toDRAM_ADDR[3]
- PIN_N6 -toDRAM_ADDR[4]
- PIN_AB10 -toDRAM_ADDR[5]
- PIN_P12 -toDRAM_ADDR[6]
- PIN_P7 -toDRAM_ADDR[7]
- PIN_P8 -toDRAM_ADDR[8]
- PIN_R5 -toDRAM_ADDR[9]
- PIN_U8 -toDRAM_ADDR[10]
- PIN_P6 -toDRAM_ADDR[11]
- PIN_R7 -toDRAM_ADDR[12]
- PIN_T7 -toDRAM_BA[0]
- PIN_AB7 -toDRAM_BA[1]
- PIN_V6 -toDRAM_CAS_N
- PIN_R6 -toDRAM_CKE
- PIN_AB11 -toDRAM_CLK
- PIN_U6 -toDRAM_CS_N
- PIN_Y9 -toDRAM_DQ[0]
- PIN_T10 -toDRAM_DQ[1]
- PIN_R9 -toDRAM_DQ[2]
- PIN_Y11 -toDRAM_DQ[3]
- PIN_R10 -toDRAM_DQ[4]
- PIN_R11 -toDRAM_DQ[5]
- PIN_R12 -toDRAM_DQ[6]
- PIN_AA12 -toDRAM_DQ[7]
- PIN_AA9 -toDRAM_DQ[8]
- PIN_AB8 -toDRAM_DQ[9]
- PIN_AA8 -toDRAM_DQ[10]
- PIN_AA7 -toDRAM_DQ[11]
- PIN_V10 -toDRAM_DQ[12]
- PIN_V9 -toDRAM_DQ[13]
- PIN_U10 -toDRAM_DQ[14]
- PIN_T9 -toDRAM_DQ[15]
- PIN_U12 -toDRAM_LDQM
- PIN_AB6 -toDRAM_RAS_N
- PIN_N8 -toDRAM_UDQM
- PIN_AB5 -toDRAM_WE_N
- PIN_N16 -toGPIO_0[0]
- PIN_B16 -toGPIO_0[1]
- PIN_M16 -toGPIO_0[2]
- PIN_C16 -toGPIO_0[3]
- PIN_D17 -toGPIO_0[4]
- PIN_K20 -toGPIO_0[5]
- PIN_K21 -toGPIO_0[6]
- PIN_K22 -toGPIO_0[7]
- PIN_M20 -toGPIO_0[8]
- PIN_M21 -toGPIO_0[9]
- PIN_N21 -toGPIO_0[10]
- PIN_R22 -toGPIO_0[11]
- PIN_R21 -toGPIO_0[12]

- PIN_T22 -toGPIO_0[13]
- PIN_N20 -toGPIO_0[14]
- PIN_N19 -toGPIO_0[15]
- PIN_M22 -toGPIO_0[16]
- PIN_P19 -toGPIO_0[17]
- PIN_L22 -toGPIO_0[18]
- PIN_P17 -toGPIO_0[19]
- PIN_P16 -toGPIO_0[20]
- PIN_M18 -toGPIO_0[21]
- PIN_L18 -toGPIO_0[22]
- PIN_L17 -toGPIO_0[23]
- PIN_L19 -toGPIO_0[24]
- PIN_K17 -toGPIO_0[25]
- PIN_K19 -toGPIO_0[26]
- PIN_P18 -toGPIO_0[27]
- PIN_R15 -toGPIO_0[28]
- PIN_R17 -toGPIO_0[29]
- PIN_R16 -toGPIO_0[30]
- PIN_T20 -toGPIO_0[31]
- PIN_T19 -toGPIO_0[32]
- PIN_T18 -toGPIO_0[33]
- PIN_T17 -toGPIO_0[34]
- PIN_T15 -toGPIO_0[35]
- PIN_H16 -toGPIO_1[0]
- PIN_A12 -toGPIO_1[1]
- PIN_H15 -toGPIO_1[2]
- PIN_B12 -toGPIO_1[3]
- PIN_A13 -toGPIO_1[4]
- PIN_B13 -toGPIO_1[5]
- PIN_C13 -toGPIO_1[6]
- PIN_D13 -toGPIO_1[7]
- PIN_G18 -toGPIO_1[8]
- PIN_G17 -toGPIO_1[9]
- PIN_H18 -toGPIO_1[10]
- PIN_J18 -toGPIO_1[11]
- PIN_J19 -toGPIO_1[12]
- PIN_G11 -toGPIO_1[13]
- PIN_H10 -toGPIO_1[14]
- PIN_J11 -toGPIO_1[15]
- PIN_H14 -toGPIO_1[16]
- PIN_A15 -toGPIO_1[17]
- PIN_J13 -toGPIO_1[18]
- PIN_L8 -toGPIO_1[19]
- PIN_A14 -toGPIO_1[20]
- PIN_B15 -toGPIO_1[21]
- PIN_C15 -toGPIO_1[22]
- PIN_E14 -toGPIO_1[23]
- PIN_E15 -toGPIO_1[24]
- PIN_E16 -toGPIO_1[25]
- PIN_F14 -toGPIO_1[26]
- PIN_F15 -toGPIO_1[27]
- PIN_F13 -toGPIO_1[28]
- PIN_F12 -toGPIO_1[29]
- PIN_G16 -toGPIO_1[30]
- PIN_G15 -toGPIO_1[31]

- PIN_G13 -toGPIO_1[32]
- PIN_G12 -toGPIO_1[33]
- PIN_J17 -toGPIO_1[34]
- PIN_K16 -toGPIO_1[35]
- PIN_U21 -toHEX0[0]
- PIN_V21 -toHEX0[1]
- PIN_W22 -toHEX0[2]
- PIN_W21 -toHEX0[3]
- PIN_Y22 -toHEX0[4]
- PIN_Y21 -toHEX0[5]
- PIN_AA22 -toHEX0[6]
- PIN_AA20 -toHEX1[0]
- PIN_AB20 -toHEX1[1]
- PIN_AA19 -toHEX1[2]
- PIN_AA18 -toHEX1[3]
- PIN_AB18 -toHEX1[4]
- PIN_AA17 -toHEX1[5]
- PIN_U22 -toHEX1[6]
- PIN_Y19 -toHEX2[0]
- PIN_AB17 -toHEX2[1]
- PIN_AA10 -toHEX2[2]
- PIN_Y14 -toHEX2[3]
- PIN_V14 -toHEX2[4]
- PIN_AB22 -toHEX2[5]
- PIN_AB21 -toHEX2[6]
- PIN_Y16 -toHEX3[0]
- PIN_W16 -toHEX3[1]
- PIN_Y17 -toHEX3[2]
- PIN_V16 -toHEX3[3]
- PIN_U17 -toHEX3[4]
- PIN_V18 -toHEX3[5]
- PIN_V19 -toHEX3[6]
- PIN_U20 -toHEX4[0]
- PIN_Y20 -toHEX4[1]
- PIN_V20 -toHEX4[2]
- PIN_U16 -toHEX4[3]
- PIN_U15 -toHEX4[4]
- PIN_Y15 -toHEX4[5]
- PIN_P9 -toHEX4[6]
- PIN_N9 -toHEX5[0]
- PIN_M8 -toHEX5[1]
- PIN_T14 -toHEX5[2]
- PIN_P14 -toHEX5[3]
- PIN_C1 -toHEX5[4]
- PIN_C2 -toHEX5[5]
- PIN_W19 -toHEX5[6]
- PIN_U7 -toKEY[0]
- PIN_W9 -toKEY[1]
- PIN_M7 -toKEY[2]
- PIN_M6 -toKEY[3]
- PIN_AA2 -toLEDR[0]
- PIN_AA1 -toLEDR[1]
- PIN_W2 -toLEDR[2]
- PIN_Y3 -toLEDR[3]
- PIN_N2 -toLEDR[4]

- PIN_N1 -toLEDR[5]
- PIN_U2 -toLEDR[6]
- PIN_U1 -toLEDR[7]
- PIN_L2 -toLEDR[8]
- PIN_L1 -toLEDR[9]
- PIN_D3 -toPS2_CLK
- PIN_E2 -toPS2_CLK2
- PIN_G2 -toPS2_DAT
- PIN_G1 -toPS2_DAT2
- PIN_P22 -toRESET_N
- PIN_H11 -toSD_CLK
- PIN_B11 -toSD_CMD
- PIN_K9 -toSD_DATA[0]
- PIN_D12 -toSD_DATA[1]
- PIN_E12 -toSD_DATA[2]
- PIN_C11 -toSD_DATA[3]
- PIN_U13 -toSW[0]
- PIN_V13 -toSW[1]
- PIN_T13 -toSW[2]
- PIN_T12 -toSW[3]
- PIN_AA15 -toSW[4]
- PIN_AB15 -toSW[5]
- PIN_AA14 -toSW[6]
- PIN_AA13 -toSW[7]
- PIN_AB13 -toSW[8]
- PIN_AB12 -toSW[9]
- PIN_B6 -toVGA_B[0]
- PIN_B7 -toVGA_B[1]
- PIN_A8 -toVGA_B[2]
- PIN_A7 -toVGA_B[3]
- PIN_L7 -toVGA_G[0]
- PIN_K7 -toVGA_G[1]
- PIN_J7 -toVGA_G[2]
- PIN_J8 -toVGA_G[3]
- PIN_H8 -toVGA_HS
- PIN_A9 -toVGA_R[0]
- PIN_B10 -toVGA_R[1]
- PIN_C9 -toVGA_R[2]
- PIN_A5 -toVGA_R[3]
- PIN_G8 -toVGA_VS
- PARTITION_NETLIST_TYPE SOURCE-section_idTop
- PARTITION_FITTER_PRESERVATION_LEVEL PLACEMENT_AND_ROUTING-section_idTop
- PARTITION_COLOR 16764057 -section_idTop
- STRATIX_DEVICE_IO_STANDARD " 2.5 V"
- OPTIMIZATION_TECHNIQUE SPEED
- SYNTH_TIMING_DRIVEN_SYNTHESIS ON
- OPTIMIZE_HOLD_TIMING "ALLPATHS"
- OPTIMIZE_MULTI_CORNER_TIMING ON
- FITTER_EFFORT "STANDARDFIT"
- STRATIXV_CONFIGURATION_SCHEME "ACTIVESERIALX1"
- USE_CONFIGURATION_DEVICE ON
- STRATIXII_CONFIGURATION_DEVICE EPCS64
- CRC_ERROR_OPEN_DRAIN ON
- OUTPUT_IO_TIMING_NEAR_END_VMEAS "HALFVCCIO"-rise
- OUTPUT_IO_TIMING_NEAR_END_VMEAS "HALFVCCIO"-fall

- OUTPUT_IO_TIMING_FAR_END_VMEAS "HALFSIGNALSWING"-rise
- OUTPUT_IO_TIMING_FAR_END_VMEAS "HALFSIGNALSWING"-fall
- ACTIVE_SERIAL_CLOCK FREQ_100MHZ
- BOARD "DE0-CVDevelopmentBoard"
- EDA_SIMULATION_TOOL "QuestaIntelFPGA(VHDL)"
- EDA_TIME_SCALE "1 ps"-section_ideda_simulation
- EDA_OUTPUT_DATA_FORMAT VHDL-section_ideda_simulation
- EDA_GENERATE_FUNCTIONAL_NETLIST F-section_ideda_board_design_timing
- EDA_GENERATE_FUNCTIONAL_NETLIST F-section_ideda_board_design_symbol
- EDA_GENERATE_FUNCTIONAL_NETLIST F-section_ideda_board_design_signal_integrity
- EDA_GENERATE_FUNCTIONAL_NETLIST F-section_ideda_board_design_boundary_scan
- MIN_CORE_JUNCTION_TEMP 0
- MAX_CORE_JUNCTION_TEMP 85
- POWER_PRESET_COOLING_SOLUTION "23 MMHEATSINKWITH 200 LFPMAIRFLOW"
- POWER_BOARD_THERMAL_MODEL "NONE(CONSERVATIVE)"
- VHDL_INPUT_VERSION VHDL_2008
- VHDL_SHOW_LMF_MAPPING_MESSAGES F
- VHDL_FILE MPPT.vhd
- VHDL_FILE sixteenBitComparator.vhd
- VHDL_FILE PWM_submodule.vhd
- VHDL_FILE fourBitComparator.vhd
- VHDL_FILE eightBitComparator.vhd
- VHDL_FILE adder.vhd
- VHDL_FILE ADC.vhd
- VHDL_FILE DE0_CV_golden_top.vhd
- QIP_FILE multiplexer.qip
- PARTITION_HIERARCHY root_partition-to|-section_idTop

5.5.1 Variable Documentation

5.5.1.1 ACTIVE_SERIAL_CLOCK

[Constraints]

5.5.1.2 BOARD

[Constraints]

5.5.1.3 CRC_ERROR_OPEN_DRAIN

[Constraints]

5.5.1.4 CYCLONEII_RESERVE_NCEO_AFTER_CONFIGURATION

[Constraints]

5.5.1.5 DEVICE

[Constraints]

5.5.1.6 EDA_GENERATE_FUNCTIONAL_NETLIST [1/4]

[Constraints]

5.5.1.7 EDA_GENERATE_FUNCTIONAL_NETLIST [2/4]

[Constraints]

5.5.1.8 EDA_GENERATE_FUNCTIONAL_NETLIST [3/4]

[Constraints]

5.5.1.9 EDA_GENERATE_FUNCTIONAL_NETLIST [4/4]

[Constraints]

5.5.1.10 EDA_OUTPUT_DATA_FORMAT

[Constraints]

5.5.1.11 EDA_SIMULATION_TOOL

[Constraints]

5.5.1.12 EDA_TIME_SCALE

[Constraints]

5.5.1.13 FAMILY

[Constraints]

5.5.1.14 FITTER_EFFORT

[Constraints]

5.5.1.15 IO_STANDARD [1/206]

[Constraints]

5.5.1.16 IO_STANDARD [2/206]

[Constraints]

5.5.1.17 IO_STANDARD [3/206]

[Constraints]

5.5.1.18 IO_STANDARD [4/206]

[Constraints]

5.5.1.19 IO_STANDARD [5/206]

[Constraints]

5.5.1.20 IO_STANDARD [6/206]

[Constraints]

5.5.1.21 IO_STANDARD [7/206]

[Constraints]

5.5.1.22 IO_STANDARD [8/206]

[Constraints]

5.5.1.23 IO_STANDARD [9/206]

[Constraints]

5.5.1.24 IO_STANDARD [10/206]

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5.5.1.25 IO_STANDARD [11/206]

[Constraints]

5.5.1.26 IO_STANDARD [12/206]

[Constraints]

5.5.1.27 IO_STANDARD [13/206]

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5.5.1.28 IO_STANDARD [14/206]

[Constraints]

5.5.1.29 IO_STANDARD [15/206]

[Constraints]

5.5.1.30 IO_STANDARD [16/206]

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5.5.1.31 IO_STANDARD [17/206]

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5.5.1.32 IO_STANDARD [18/206]

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5.5.1.33 IO_STANDARD [19/206]

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5.5.1.34 IO_STANDARD [20/206]

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5.5.1.35 IO_STANDARD [21/206]

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5.5.1.36 IO_STANDARD [22/206]

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5.5.1.37 IO_STANDARD [23/206]

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5.5.1.38 IO_STANDARD [24/206]

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5.5.1.39 IO_STANDARD [25/206]

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5.5.1.40 IO_STANDARD [26/206]

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5.5.1.41 IO_STANDARD [27/206]

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5.5.1.42 IO_STANDARD [28/206]

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5.5.1.43 IO_STANDARD [29/206]

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5.5.1.44 IO_STANDARD [30/206]

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5.5.1.45 IO_STANDARD [31/206]

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5.5.1.46 IO_STANDARD [32/206]

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5.5.1.47 IO_STANDARD [33/206]

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5.5.1.48 IO_STANDARD [34/206]

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5.5.1.49 IO_STANDARD [35/206]

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5.5.1.50 IO_STANDARD [36/206]

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5.5.1.51 IO_STANDARD [37/206]

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5.5.1.52 IO_STANDARD [38/206]

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5.5.1.53 IO_STANDARD [39/206]

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5.5.1.54 IO_STANDARD [40/206]

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5.5.1.55 IO_STANDARD [41/206]

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5.5.1.56 IO_STANDARD [42/206]

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5.5.1.57 IO_STANDARD [43/206]

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5.5.1.58 IO_STANDARD [44/206]

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5.5.1.59 IO_STANDARD [45/206]

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5.5.1.60 IO_STANDARD [46/206]

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5.5.1.61 IO_STANDARD [47/206]

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5.5.1.62 IO_STANDARD [48/206]

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5.5.1.63 IO_STANDARD [49/206]

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5.5.1.64 IO_STANDARD [50/206]

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5.5.1.65 IO_STANDARD [51/206]

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5.5.1.66 IO_STANDARD [52/206]

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5.5.1.67 IO_STANDARD [53/206]

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5.5.1.68 IO_STANDARD [54/206]

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5.5.1.69 IO_STANDARD [55/206]

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5.5.1.70 IO_STANDARD [56/206]

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5.5.1.71 IO_STANDARD [57/206]

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5.5.1.72 IO_STANDARD [58/206]

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5.5.1.73 IO_STANDARD [59/206]

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5.5.1.74 IO_STANDARD [60/206]

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5.5.1.75 IO_STANDARD [61/206]

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5.5.1.76 IO_STANDARD [62/206]

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5.5.1.77 IO_STANDARD [63/206]

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5.5.1.78 IO_STANDARD [64/206]

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5.5.1.79 IO_STANDARD [65/206]

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5.5.1.80 IO_STANDARD [66/206]

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5.5.1.81 IO_STANDARD [67/206]

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5.5.1.82 IO_STANDARD [68/206]

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5.5.1.83 IO_STANDARD [69/206]

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5.5.1.84 IO_STANDARD [70/206]

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5.5.1.85 IO_STANDARD [71/206]

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5.5.1.86 IO_STANDARD [72/206]

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5.5.1.87 IO_STANDARD [73/206]

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5.5.1.88 IO_STANDARD [74/206]

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5.5.1.89 IO_STANDARD [75/206]

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5.5.1.90 IO_STANDARD [76/206]

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5.5.1.91 IO_STANDARD [77/206]

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5.5.1.92 IO_STANDARD [78/206]

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5.5.1.93 IO_STANDARD [79/206]

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5.5.1.94 IO_STANDARD [80/206]

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5.5.1.95 IO_STANDARD [81/206]

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5.5.1.96 IO_STANDARD [82/206]

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5.5.1.97 IO_STANDARD [83/206]

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5.5.1.98 IO_STANDARD [84/206]

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5.5.1.99 IO_STANDARD [85/206]

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5.5.1.100 IO_STANDARD [86/206]

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5.5.1.101 IO_STANDARD [87/206]

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5.5.1.102 IO_STANDARD [88/206]

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5.5.1.103 IO_STANDARD [89/206]

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5.5.1.104 IO_STANDARD [90/206]

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5.5.1.105 IO_STANDARD [91/206]

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5.5.1.106 IO_STANDARD [92/206]

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5.5.1.107 IO_STANDARD [93/206]

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5.5.1.108 IO_STANDARD [94/206]

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5.5.1.109 IO_STANDARD [95/206]

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5.5.1.110 IO_STANDARD [96/206]

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5.5.1.111 IO_STANDARD [97/206]

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5.5.1.112 IO_STANDARD [98/206]

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5.5.1.113 IO_STANDARD [99/206]

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5.5.1.114 IO_STANDARD [100/206]

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5.5.1.115 IO_STANDARD [101/206]

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5.5.1.116 IO_STANDARD [102/206]

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5.5.1.117 IO_STANDARD [103/206]

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5.5.1.118 IO_STANDARD [104/206]

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5.5.1.119 IO_STANDARD [105/206]

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5.5.1.120 IO_STANDARD [106/206]

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5.5.1.121 IO_STANDARD [107/206]

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5.5.1.122 IO_STANDARD [108/206]

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5.5.1.123 IO_STANDARD [109/206]

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5.5.1.124 IO_STANDARD [110/206]

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5.5.1.125 IO_STANDARD [111/206]

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5.5.1.126 IO_STANDARD [112/206]

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5.5.1.127 IO_STANDARD [113/206]

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5.5.1.128 IO_STANDARD [114/206]

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5.5.1.129 IO_STANDARD [115/206]

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5.5.1.130 IO_STANDARD [116/206]

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5.5.1.131 IO_STANDARD [117/206]

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5.5.1.132 IO_STANDARD [118/206]

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5.5.1.133 IO_STANDARD [119/206]

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5.5.1.134 IO_STANDARD [120/206]

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5.5.1.135 IO_STANDARD [121/206]

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5.5.1.136 IO_STANDARD [122/206]

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5.5.1.137 IO_STANDARD [123/206]

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5.5.1.138 IO_STANDARD [124/206]

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5.5.1.139 IO_STANDARD [125/206]

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5.5.1.140 IO_STANDARD [126/206]

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5.5.1.141 IO_STANDARD [127/206]

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5.5.1.142 IO_STANDARD [128/206]

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5.5.1.143 IO_STANDARD [129/206]

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5.5.1.144 IO_STANDARD [130/206]

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5.5.1.145 IO_STANDARD [131/206]

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5.5.1.146 IO_STANDARD [132/206]

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5.5.1.147 IO_STANDARD [133/206]

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5.5.1.148 IO_STANDARD [134/206]

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5.5.1.149 IO_STANDARD [135/206]

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5.5.1.150 IO_STANDARD [136/206]

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5.5.1.151 IO_STANDARD [137/206]

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5.5.1.152 IO_STANDARD [138/206]

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5.5.1.153 IO_STANDARD [139/206]

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5.5.1.154 IO_STANDARD [140/206]

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5.5.1.155 IO_STANDARD [141/206]

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5.5.1.156 IO_STANDARD [142/206]

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5.5.1.157 IO_STANDARD [143/206]

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5.5.1.158 IO_STANDARD [144/206]

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5.5.1.159 IO_STANDARD [145/206]

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5.5.1.160 IO_STANDARD [146/206]

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5.5.1.161 IO_STANDARD [147/206]

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5.5.1.162 IO_STANDARD [148/206]

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5.5.1.163 IO_STANDARD [149/206]

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5.5.1.164 IO_STANDARD [150/206]

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5.5.1.165 IO_STANDARD [151/206]

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5.5.1.166 IO_STANDARD [152/206]

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5.5.1.167 IO_STANDARD [153/206]

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5.5.1.168 IO_STANDARD [154/206]

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5.5.1.169 IO_STANDARD [155/206]

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5.5.1.170 IO_STANDARD [156/206]

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5.5.1.171 IO_STANDARD [157/206]

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5.5.1.172 IO_STANDARD [158/206]

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