PID Controlled Thermal Management in Photonic Network-on-Chip

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***Abstract*—The communication bandwidth and power consumption of network-on-chip (NoC) are going to meet their limits soon because of traditional metallic interconnects. Photonic NoC (PNoC) is emerging as a promising alternative to address these bottlenecks. However, PNoCs are highly susceptible to thermal fluctuations which is highly common in a manycore chip. This paper first introduces a low power, low cost mesh-based PNoC architecture and provides a quantitative analysis of it's power consumption over varying on-chip temperature. The paper then proposes a proportional-integral-derivative (PID) heater mechanism that minimizes the effect of thermal variation on PNoC's performance and power. Experimental results for a 8×8 PNoC shows that the proposed technique offers the maximum network-bandwidth considering the thermal effects. Compared to the recently reported results, the proposed design consumes 40% less power and has a temperature variation as low as 1 $^\circ$C.**

I. Introduction

Increasing density trend of chip-multiprocessors(CMP) requires higher bandwidth to support extensive communication among all cores. Semiconductor NoCs would not provide such a large bandwidth while maintaining an acceptable level of power consumption[1]. Recently, silicon-photonic links are being adopted as reliable and attractive alternative to traditional metallic interconnects[2]. They hold promise to higher rate data transfer with minimal power dissipation[3]. Also, *low loss in optical waveguides* [2] and *bit rate transparency*[3] are added advantages of photonic on-chip communication. However, silicon-photonic interconnects suffer from susceptibility to thermal fluctuations. Hence a widespread adoption of PNoC has not been demonstrated.

Microring resonator (MRR) and silicon-photonic waveguides are the building blocks of a PNoC. MRR is used as modulator at the transmitter side and as filter at the reciever side. It is also used for switching of optical carrier singal. MRR switches an optical signal by filtering the desired wavelength. However, these MRRs are highly vulnerable to thermal fluctuations. For reliable data transmission in PNoC, MRRs need to be at the same temperature [6]. However, temperature variations and thermal gradient are highly common in CMPs. Hotspot [12] simulation indicates a $15 - 20\,^\circ$C thermal gradient in a 64-core CMP with random traffic as shown in Fig.1. This may result in a mismatch of resonant wavelengths of MRRs, which leads to unreliable data transmisison and PNoC performance degradation. In this paper, our goal is to adaptically minimize thermal fluctuations in the PNoC.

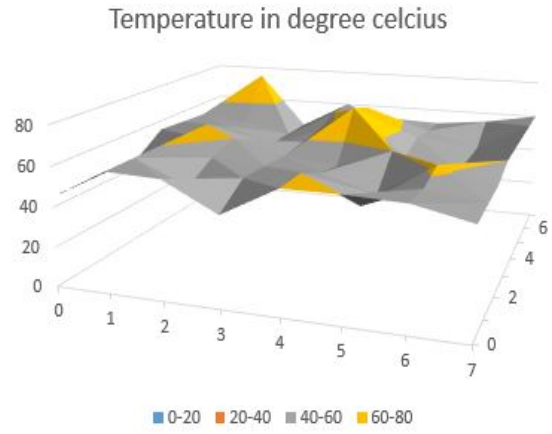


Fig. 1: Thermal Gradient Across a 64-core Chip

Numerous techniques such as workload scheduling[4], DVFS, and liquid cooling[5] have been proposed for the thermal management of manycore architectures. However, a very little has been explored on thermal management in PNoC except[6]. In[6], authors have proposed a job allocation technique to reduce the thermal gradient in PNoC. But it comes with a compromise on overall performance. We propose an adaptive heater based MRR design that minimizes the thermal fluctuations in PNoC without any compromise in overall peformance.

This paper has following contributions:
1) We model the thermal behavior of photonic interconnects based manycore sysetms for various workloads using Hotspot 5.0. We analytically determine PNoC power consumption w.r.t thermal fluctuations over varying network bandwidth.
2) We propose a temperature-aware heater design inside each MRR which adaptically reduces the thermal gradients in PNoC without producing any performance or area overhead. To the best of our knowledge, this approach is the first of its kind in thermal management of PNoC.
3) We evaluated our design using circuit level simulator and reported: (a) $4\times$ improvement in network bandwidth compared

to recently reported result[6]; (b) 2× improvement in area overhead compared to the best reported result[7]; (c) The design also shows 40% improvement in power consumption compared to the most recently reported design[6].

The paper is organized as follows. In section II PNoC is introduced and switching mechanism of PNoC is described. Effects of temperature variations on and thermal model of PNoC is presented in section III. Section IV depicts the microarchitecture and working of proposed adaptive heater based design and it's design space has been explored. Experiments, results, and comparative analysis are depicted in section V followed by conclusion.

II. Photonic Network-on-Chip

Photonic interconnect is an emerging technology for manycore NoCs for its low power consumption and higher bandwidth compared to electrical NoCs. Several topologies have been explored for high performance PNoC architecture design such as mesh[2], crossbar[3], torus[8], and clos[9]. Our focus is on MRR and waveguides based two-dimensional mesh PNoC. In this research, we are considering a 64-core mesh connected 2D PNoC. A 16-core version of the actual PNoC is shown in Fig.2.

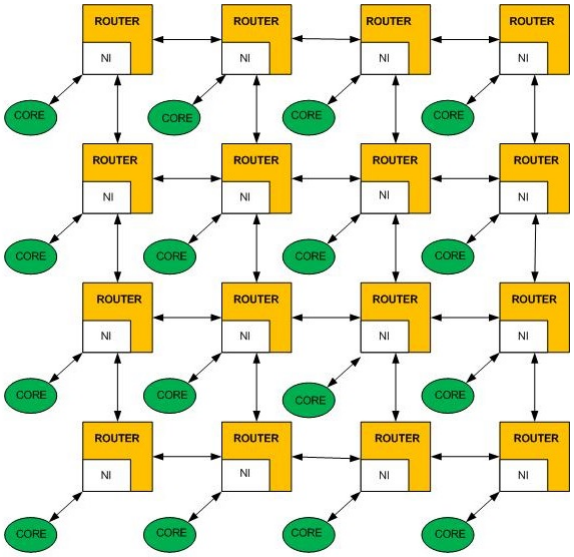


Fig. 2: 2D PNoC architecture

Each router in PNoC is a non-blocking 5×5 photonic router as shown in Fig.3. One of the router ports is connected to a core, while other four ports are connected to neighbouring routers. The circular structures in the router layout are MRRs. An MRR is a circularly coiled waveguide that filters optical signals. It is used as basic switching element in the photonic router.

The switching mechanism of an MRR is depicted in Fig.4. As shown in Fig.4a and Fig.4c MRR in OFF state allows the optical signal to be transmitted from the input port in a

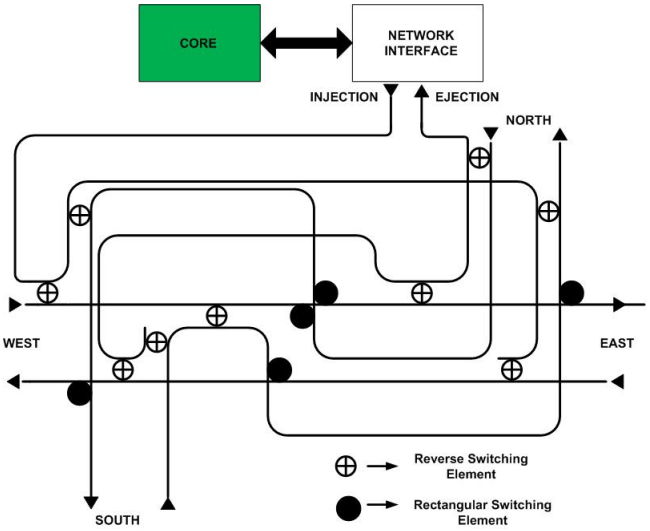
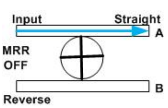
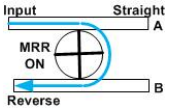


Fig. 3: Logical layout of router

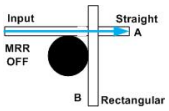
straight line without deflection. When in ON state (Fig.4b and Fig.4d), MRR couples the optical signal of specific wavelength from waveguide A to waveguide B. For reverse-switching, we use two parallel waveguides as shown in Fig.4b. Two waveguides are placed with an angle of 90 degree to each other for rectangular-switching as shown in Fig.4d.



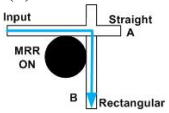
(a) Reverse Switch(OFF State)



(b) Reverse Switch(ON State)



(c) Rectangular Switch(OFF State)



(d) Rectangular Switch(ON State)

Fig. 4: MRR Switching

III. Thermal Modeling of PNoC

We use HOTSPOT 5.0 [12] for thermal simulations of PNoC. The ambient temperature is set at 35 °C. Default configurations of HOTSPOT is set for the entire simulation. We virtually fabricate the proposed PNoC using IPKISS [17] which is explained in later section. The floorplan and design configuration obtained from IPKISS are used for system configurations in HOTSPOT. The proposed thermal model of PNoC constitutes of three parts: a) thermal resistivity of PNoC, b) on-chip temperature variation, and c) thermo-optic effects.

A. Thermal resistivity of PNoC

As shown in Fig.5, PNoC floorplan is divided into several rectangular blocks (grey box) which contain either waveguides, or MRR (black circle inside each box) and waveguides. The thermal resistivity of any block in PNoC

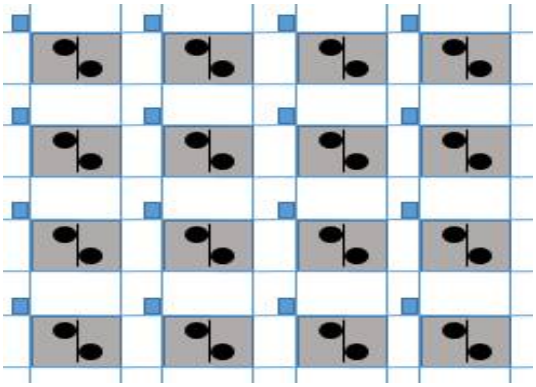


Fig. 5: Floorplan of PNoC Architecture

can be obtained by

$$R_{block} = \frac{V_{total}}{\sum \frac{V_j}{R_j}} \tag{1}$$

The thermal resistivity of block having waveguide is 0.001003 m-K/W and that of block with MRRs and waveguides is 0.001005 m-K/W. These are approximately equal to the thermal resistivity of silicon. Hence, we use a single thermal resistivity of 0.001 m-K/W across the die.

B. On-chip temperature variation

We derive the dynamic core power values with uniform traffic using the power dissipation data of Intel SCC [10]. When all the cores are idle, the PNoC temperature remains at 70 °C. At 70 °C we're assuming the leakage power to be 35% of the dynamic power [6]. The core temperature T in the chip is related to the leakage power as follows:

$$P_{Leak} = 0.0014T - 0.0722 \tag{2}$$

Here T is in °K.

C. Thermo-optic effects

Temperature fluctuations in many-core chip is a major concern because rise in temperature causes performance degradation of PNoC components like MRR, laser, and photonic transceiver. This will degrade the overall performance of PNoC. The resonant wavelength of MRR shifts approximately linearly with increasing temperatures [11]. For a MRR working at temperature T, the shifted resonance wavelength λ is given by Eqn.(3).

$$\lambda = \lambda_B + \rho \times (T - T_B) \tag{3}$$

Here, λ_R is the resonance wavelength of MRR at base temperature T_B, and ρ is temperature-dependent wavelength shift coefficient of MRR. Temperature fluctuation in PNoC also results in optical (signal) power loss. It can be governed by the following equations, where P_T represents energy of the transimitted signal, L_M represents losses in MRRs, and S_R stands for receiver sensitivity.

$$P_T - L_M \geq S_R \tag{4}$$

Wavelength mismatch in MRR and signal power loss affect the overall performance of PNoC.

$$P_T = 10 \times \log((I - \alpha - \beta \times (T_{Laser} - T_B)^2) \times (\epsilon - \gamma \times T_{Laser}) \tag{5}$$

$$L_M = \sum_{i=1}^{N} 10\log\left(\left(\frac{2K^2 + K_p^2}{2k^2}\right)^2 \times \left(1 + \frac{(\lambda_B + \rho_{Laser}(T_{Laser} - T_B) - \rho_M(T_i - T_B) - \lambda_R)^2}{d^2}\right)\right) \tag{6}$$

In Equation.[5] and [6], α, β, ϵ, γ, K and K_p are design parameters obtained from [15], T_{Laser} is the laser temperature, T_i represents temperature around i_{th} MRR, ρ_{Laser} and ρ_M are wavelength shift coefficients of laser and MRR respectively, and d is wavelength-shift in MRR.

IV. Thermal Management in PNoC

A. Adaptive Heater based MRR

As the MRRs are vulnerable to thermal fluctuations in the surroundings, our aim is to maintain a fixed temperature around each MRR. Integrated heaters are resistive elements constructed from nichrome, titanium, Ni-silicide, or impurity-doped silicon materials. Applying current through these resistive materials generates heat that can be utilized to tune the surrounding temperature of MRR. Each of the MRRs in the proposed PNoC is integrated with a tunable heating material as shown in Fig 6.

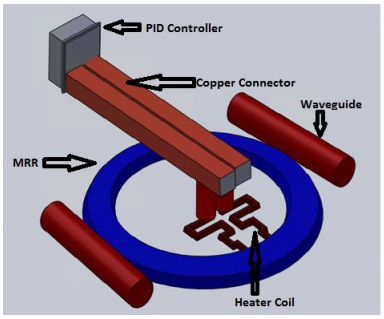


Fig. 6: Heater based MRR design

A proportional-integral-derivative (PID) controller associated with each heater maintains the thermal tuning. It collects the temperature data from thermal sensor integrated with the corresponding core and converts that to an equivalent current which is applied to the heater. It uses an algorithm as depicted in Algorithm 1.

In the algorithm, T represents the temperature as detected by the thermal sensor, T_{Max} is the maximum temperature in PNoC, P_{Heat} is the heater power, i_{Heat} represents heater current, and H_{eff} stands for transfer function of heater. As per the algorithm, current is fed to heaters with an interval of

Algorithm 1 PID Control Algorithm for thermal Management of Micro-ring Resonator

procedure PID WANTS TO CONVERT SURROUNDING TEMPERATURE TO EQUIVALENT MRR-HEATER POWER

[1] T=Temperature around the core as detected by Thermal sensor

[2] PID Controller converts T to equivalent heater current as follows:

if (T $\leq T_{Max}$) **then**

dT = T_{Max} - T

$P_{Heat} = \frac{dT}{\rho} \times H_{eff}$

$i_{Heat} = i_{Max} - \sqrt{\frac{P_{Heat}}{R_{Heat}}}$

if (T $> T_{Max}$) **then**

dT = T - T_{Max}

$P_{Heat} = \frac{dT}{\rho} \times H_{eff}$

$i_{Heat} = i_{Max} + \sqrt{\frac{P_{Heat}}{R_{Heat}}}$

[3] Delay of 1 milisecond

[4] Go to step [1]

1 milisecond. Our experiments using HOTSPOT shows that 1 milisecond is the least duration of time in which any point of PNoC can encounter a significant temperature change to alter the characteristics of MRR. PID converts the difference between T and T_{Max} to i_{Heat} which is fed to heater coil.
Fig 7 shows the PID tuning result over a period of 2000 mili-second as obtained from MATLAB. Simulation of PID controller for each MRR is carried out in MATLAB. The result shows that the heater power decreses as the core temperature of PNoC increases due to workload. This makes the the resulting temperature across each MRR constant.

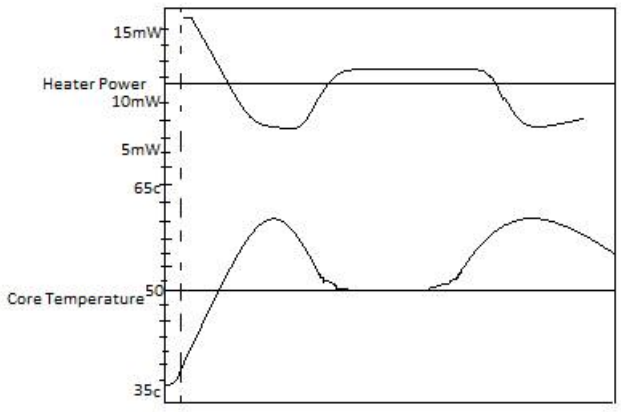


Fig. 7: Heater tuning w.r.t workload variation

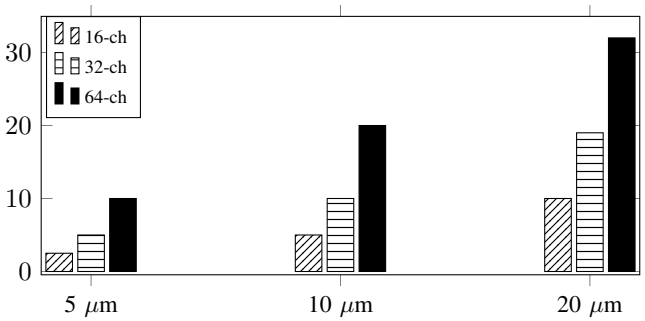


Fig. 8: Area Overhead per MRR diameter

B. Design Space Exploration

To understand the design space of PNoC, we consider an integrated heater design, PNoC architecture design, and PNoC performance. Table I depicts performance comparison of several types of heaters. Here, the metric for transfer-number is mW/nm and that of heating or cooling time constant (τ) is μs. Transfer-number of heater can be defined as the amount of power needed to shift resonant wavelength of MRR by 1 nm. From the table, it is evident that doped-silicon has the lowest transfer-number and has reasonable heating time constant. Hence, we adopt doped-Si for integrated heater design.

Fabricating photonic components are expensive compared to electrical components. Hence we limit the area of photonic components to be at most 10% of the total chip area. This area constraint puts a higher limit on the size of MRR. We have considered three diameters for MRRs: 5 μm, 10 μm, and 20 μm. The area overhead of photonic devices w.r.t MRR size are shown in Fig. 8. In the figure, 16-ch stands for 16-optical channel per waveguide. It is clear that the area overhead increases with increase in MRR diameter. But the optical insertion loss is larger for smaller MRR. Hence we're adopting MRRs of 10 μm diameter in our studies.

TABLE I: Heater Performance Comparison

Heater type	Transfer-Number	Heating τ	Cooling τ
Doped-Si	3.138	21.3	66.0
Silicide	3.462	19.1	75.8
Tungsten	3.6	38.2	45.11
Doped Waveguide	3.369	43.4	39.8

V. Experiments, Results, and Analysis

IPKISS[17] platform has been used for design and simulation of the heater integrated PNoC. This tool allows photonic component layout design, virtual fabrication of components in different technologies, physical simulation of components, and optical circuit design and simulation. We custom-designed photonic components like MRR, waveguide, mode-locked laser, tapered waveguide, and photodiode required for the proposed architecture.

A. PNoC Component Simulations on IPKISS

The design parameters adopted to carry out various experiments are depicted in TABLE II. MRR of diameter 10μm was adopted to keep the area of the PNoC foot-print small without letting the waveguides interfere much. The multimode waveguide supports four optical modes TE_0, TE_1, TE_2 and TE_3 with a refractive index of 2.46. The waveguide also supports multiple wavelengths. The mode-locked laser used has a frequency of 10-GHz. It produces optical signal with a pulse width of 10ps. Each of the pulses contains multiple wavelengths ranging from 1547.5nm to 1550nm. The laser also produces hundreds of modes. But we're considering modes TE_0, TE_1, TE_2 and TE_3 as the proposed MDM scheme supports 4 modes. Using all these fundamental components, we built the heater integrated PNoC in IPKISS and performed the physical simulation.

TABLE II: Design Parameters for Experimental Setup

Design Parameters	Value
MRR diameter	10μm
Waveguide(MRR) width	450nm
Waveguide(Signal Transmission) height	250nm
Waveguide(Signal Transmission) width	450nm
Refractive index Of waveguides	2.46
Pulse-width of Optical Signal	10ps
Frequency(mode-locked laser)	10GHz
Wavelength	1547.5nm and 1550nm

MRRs with heaters and waveguides were integrated to virtually fabricate the router. Routers, lasers, and waveguides were connected and virtually fabricated. After virtual fabrication, to cater design issues we carried out simulation using CAMFR [13]. CAMFR provides refractive index profile and optical transmission profile of the fabricated design. Uniform refractive index across the PNoC is necessary for ripple free photonic transmission. After testing the uniformity of refractive index across the router, we simulated the PNoC in CAPHE [14]. CAPHE is an optical circuit simulator for time-domain and frequency-domain analysis. It is also used to evaluate component level power consumption and insertion loss in an optical circuit.

B. Evaluation and Comparison of Power Consumption of PNoC

The power consumption of PNoC can be divided into two parts: electrical power and optical power. Electrical power consumption accounts for the power consumed in electrical components like router controller, laser driver etc. Similarly, optical power is the sum of power consumption in MRRs, lasers, optical transmitters and receivers, and waveguides. As we are addressing the thermal vulnerability of photonic devices, our focus is entirely on the optical power consumption of PNoC. Optical power of PNoC is given by Equation.7, where P_{Laser} is power consumed by lasers, P_{Switch} is power consumed by photonic switches

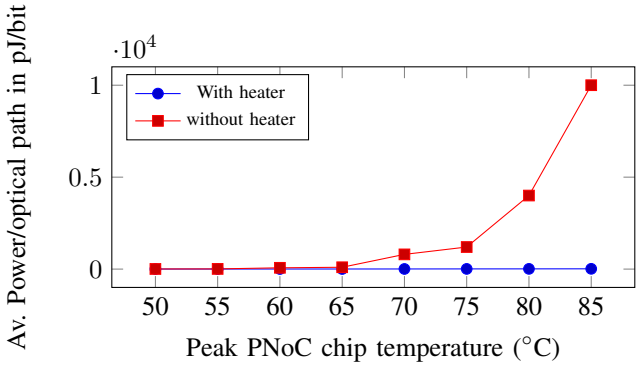


Fig. 9: Average Power/Path in pJ/bit with rising PNoC temperature

or MRRs, and P_{Det} is power consumed by photonic detectors.

$$P_{optical} = P_{Laser} + P_{Switch} + P_{Det} \tag{7}$$

MRRs are the most vulnerable towards temperature fluctuations. Hence we assume P_{Laser} and P_{Det} to be invariant with temperature changes. The total power consumed across MRRs in PNoC can be given by Equation. 8.

$$L_{sw} = \sum_{i=1}^{N} 10\log\left(\left(\frac{2K^2 + K_p^2}{2k^2}\right)^2 \times \left(1 + \frac{(\lambda_B + \rho_{Laser}(T_{Laser} - T_B) - \rho_M(T_i - T_B) - \lambda_R)^2}{d^2}\right)\right) \tag{8}$$

Definition of each symbol in Equation. 8 has already been mentioned in thermal-modeling section.

Using Equation. 8 we evaluate the power consumption of proposed PNoC with and without integrated heaters when chip temperature varies from 50°C to 85°C. The results are depicted in Fig.9 which clearly shows that PNoC with integrated heaters has a steady average power consumption/path of approximately 10 pJ/bit. On the contrary, without integrated heaters, power consumption rises upto 10000 pJ/bit when chip temperature reaches 85°C.

Power consumption increases with swicthing of MRRs. It increases more as temperature across MRR fluctuates which is evident from Equation. 8. The router as depicted in Fig. 3 ensures not more than 3 switching stages to be switched on for any optical path in PNoC. Authors in [8] and [6]have crossbar router whereas λ router has been adopted in [16], and Corona architecture is adopted in [15]. All these architectures require more number switching stages (> 3) to be turned on for packet transmission. Fig.10 shows average power consumption/path in each architecture integrated with heater, when chip temperature rises from 50°C to 85°C. We have considered 64-core for all the architecture. From the graph, it is clear that the proposed

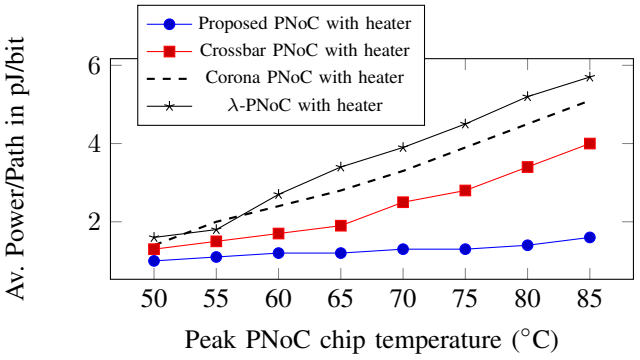


Fig. 10: Average Power/path for different architecture with varying temperature

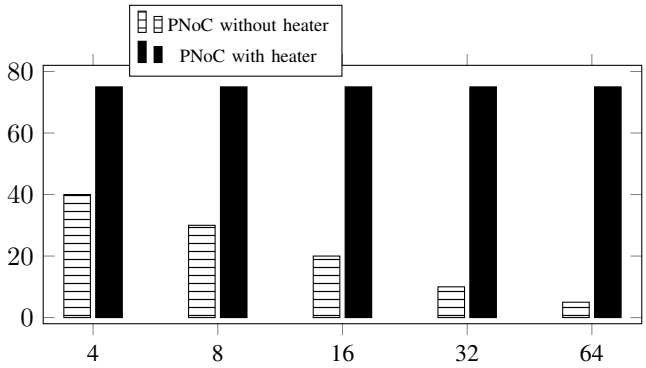


Fig. 11: Tolerable temperature gradient in °C w.r.t. λ per waveguide

architecture with heater has a fixed power consumption across varying temperature environment. The proposed heater based PNoC shows 40% improvement in power consumption over the crossbar architecture adopted by [6].

C. Evaluation and Comparison of PNoC bandwidth

As the PID based heater nullifies the temperature fluctuations in PNoC, the proposed design offers full NoC bandwidth. The overall PNoC bandwidth is evaluated by Equation. 9. Here BW per λ represents data rate of each carrier wavelength, λ per waveguide stands for number of wavelength channel in each waveguide, and modes per λ represents number of optical modes in each carrier. We consider a BW per λ of 10 Gbps and 4 wavelengths for WDM. We also consider 4 optical modes per each optical carrier. Hence the proposed PNoC offers an overall bandwidth of 160 Gbps. It is $4\times$ improvement over the recently reported result [6].

$$BW = (BW - per - \lambda)\times (\lambda - per - waveguide) \times (Modes - per - \lambda) \quad (9)$$

MRR radius defines its free spectral range (FSR). FSR is the wavelength range that can be tuned by any MRR. We have adopted MRRs of 5 μm radii and they have a thermal sensitivity of 78 pm/K. Using Equation.10 we evaluate the thermal sensitivity in terms of frequency. Here λ is the resonating wavelength of MRR which is 1550 nm. $f_0 = \frac{c}{\lambda_0}$ = 194 THz; where 'c' is the velocity of light. Applying these values, we get a thermal sensivity of 10 GHz/K for each MRR. Thermal sensitivity determines frequency spacing between each channel of light in the waveguide. In manycore architecture, temperature gradient across chip is a common phenomenon as discussed earlier. This temperature gradient affects the overall bandwidth of PNoC. We can say that, PNoC with higher bandwidth is more vulnerable to temperature gradient and hence has a less tolerable temperature gradient.That's because temperature gradient results in variable λ-shift among MRRs. Fig.11 depicts a comparative study of the tolerable temperature gradient of heater based PNoC and that of PNoC without heater when λ-per-waveguide is varied. From Equation. 9, it is clear that PNoC bandwidth is directly proportional to λ-per-waveguide. From Fig. 11, we can see that the tolerable temperature gradient is decreasing with increase in λ-per-waveguide as the bandwidth increases. But PNoC with heater has a fixed tolerable limit of 70 °C.

$$\frac{\Delta\lambda}{\lambda_0} = \frac{\Delta f}{f_0} \quad (10)$$

D. Peak Temperature Variation in PNoC

As discussed earlier, peak temperature variation is a major concern in PNoC. Fig.12 depicts a comparative analysis of peak temperature variation in various architecture. It is quite clear from the figure that heater based proposed PNoC has less variation in peak temperature compared to other architectures. Heater based design enables a variation as low as 1 °C as opposed to $3 - 7^{\circ}C$ variation in the most recent work [6] which follows crossbar architecture.

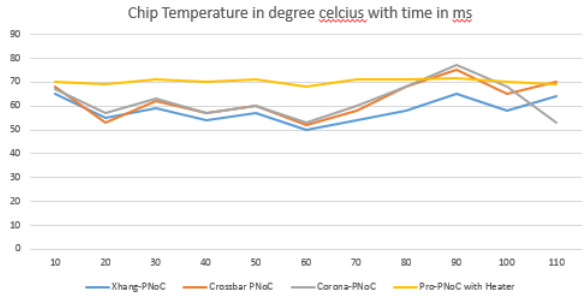


Fig. 12: Peak temperature variations in PNoC

VI. Conclusion

In this paper we model the thermal behavior of photonic interconnects based manycore sysetms. We also analytically evaluated PNoC power consumption w.r.t to thermal fluctuations over various network bandwidths. We propose a temperature-aware heater design inside each MRR which

adaptically reduces the thermal gradients in PNoC without producing any performance or area overhead. To the best of our knowledge, this is first of its kind for thermal manegement of silicon-PNoC. We evaluated our design using circuit level simulator and reported: (a) $4\times$ improvement in network bandwidth compared to recently reported result [6], (b) $2\times$ improvement in area overhead compared to the best reported result [7], and (c) The design also shows 40% improvement in power consumption compared to the most recently reported design [6]. As for the future work, we are working on a system-level simulator to evaluate our design with realtime applications and benchmarks. Relaibility of PNoC is also affected by temperature fluctuations. Reliability-aware thermal management will be addressed in the future.

VII. Acknowledgements

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