Machine Learning Based Fault Detection and Protection Method for Three-Phase Inverter

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I. Abstract

This work presents a real-time machine learning (ML) - based fault detection and protection scheme for a three-phase inverter using residual current analysis. Residual currents are computed by comparing measured and predicted phase currents, and discriminative features of the time and frequency domains are extracted over a fixed observation window. A classification tree model is used to identify inverter operating conditions, including healthy and faulty states. To ensure reliable protection, a fault persistence logic is implemented to confirm faults before initiating a Pulse Width Modulation (PWM) shutdown. The results of the numerical simulation demonstrate accurate fault classification and effective protection of the inverter through timely PWM tripping.

Keywords: Three-phase inverter, Fault detection, Residual current, Machine learning, PWM protection, Classification tree

II. Background

Three-phase inverters used in motor drives, renewable systems, EV powertrains, and industrial converters are prone to open-phase and short-circuit faults that can cause severe damage [2], [3]. Conventional threshold-based protection often fails under noise and varying conditions. This project proposes a residual current-based real-time machine learning framework, with feature extraction and PWM tripping logic, to ensure robust and reliable inverter protection.

Method	Principle	Limitations
Threshold-based	Fixed current and voltage waveform obtained. It limits the inverter tripping operation. Simple, cheap and reliable	Noise sensitive, False trips occur frequently [2]
Model-based	Compare actual signals vs. accurate reference model. Detects subtle faults effectively	Needs accurate model parameters to detect faults [3]
Signal processing	Harmonic and Transient analysis of inverter signals are used. Good for short circuit detection	Needs fast and accurate sampling hardware [4]
AI/ML	Learns fault patterns using training data. Adaptive, robust, scalable	Needs data, complex implementation [5]

Table I: Comparative methods for fault detection in three-phase inverters

Table I summarises existing approaches. The proposed residual current-based real-time ML framework improves robustness over threshold methods and reduces dependence on exact models. Residual features simplify classification and enable real-time integration. However, disadvantages include reliance on labelled training data, classifier tuning, higher computational effort, and validation requirements compared to simpler threshold or signal-processing approaches.

III. Architecture of 3-Phase Inverter System [3]

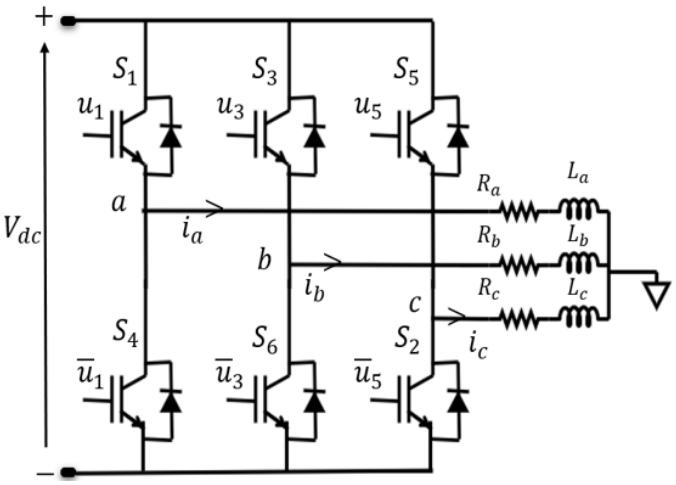

Figure 1: Three-Phase Voltage Source Inverter (VSI)

- **Inverter Topology - Universal Bridge**
  The system utilises a 2-level, three-phase inverter with six IGBT switches arranged in three legs, as shown in Figure 1. Each leg corresponds to one phase (A, B, C) and operates as a half-bridge. The switching sequence is controlled by PWM signals, which convert DC input to an AC waveform, ensuring balanced output, reduced harmonics, and efficient power delivery to connected loads.
- **DC Source and Load**
  - **Power Stage**: The inverter operates from a stable DC source V_{dc}, ensuring reliable performance under varying loads and maintaining consistent voltage regulation across operating conditions.

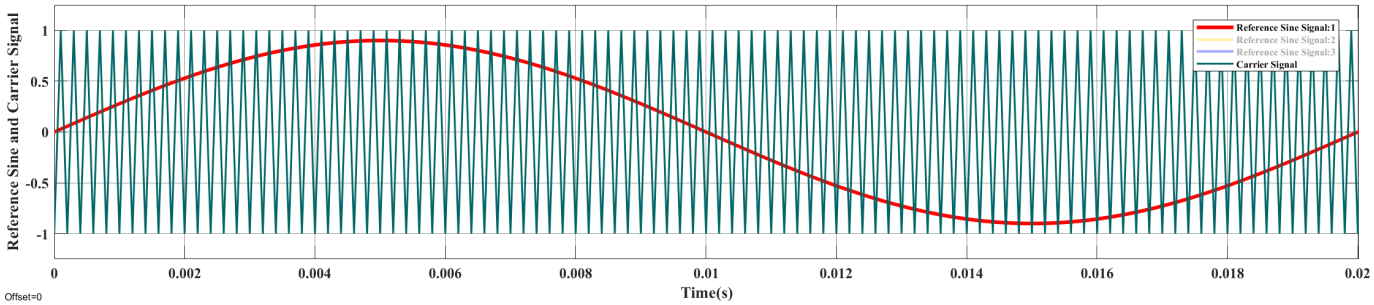

Figure 2: SPWM compares 50 Hz sinusoidal reference with 5 kHz triangular carrier, generating pulses controlling switching.

Parameter	Value
DC Link Voltage (V_{dc})	300 V
Load Resistance ($R_a = R_b = R_c$)	1 Ω
Load Inductance ($L_a = L_b = L_c$)	10 mH
Short-Circuit Resistance (R_{sc})	0.1 Ω
Modulation Index (m_a)	0.9
Carrier Signal Frequency (f_c)	5 kHz
Reference Sinusoidal Signal Frequency (f_{ref})	50 Hz
Windowing Time (T_w)	20 ms
Discretisation of ZOH Block Time (T_s)	10 ms

Table II: Parameters of Power Stage and Control Stage of Voltage Source Inverter.

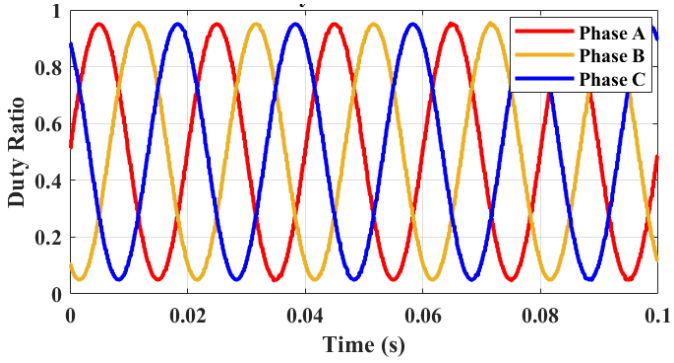

Figure 3: Sinusoidally varying PWM signals

- **Control Stage**: The inverter output is connected to a balanced three-phase linear RL load, closely resembling the characteristics of a motor load. This setup ensures realistic current and voltage waveforms, effectively replicating practical operating conditions found in real electrical systems and industrial applications. Figures 5, 6, and 7 illustrate the obtained waveforms for phase current and phase voltage for the respective phases.

- **PWM Generation and Its Importance in Control**
  - **Definition:** The modulation index is defined as the ratio of the amplitude of the sinusoidal reference signal (V_m) to the amplitude of the triangular carrier signal (V_c):

$$m = \frac{V_m}{V_c}$$

In sinusoidal PWM (SPWM), this parameter determines how strongly the reference signal modulates the carrier, thereby controlling the width of the generated pulses, as shown in Figure 2. A higher modulation index increases the fundamental output voltage, while a lower index reduces it, influencing harmonic distortion and inverter efficiency. Additionally, the modulation index directly impacts voltage utilisation, dynamic response, and overall inverter performance under varying load conditions.

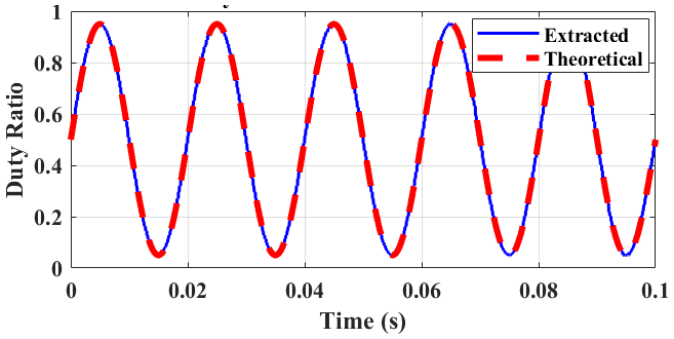

Figure 4: Phase A – Duty ratio comparison

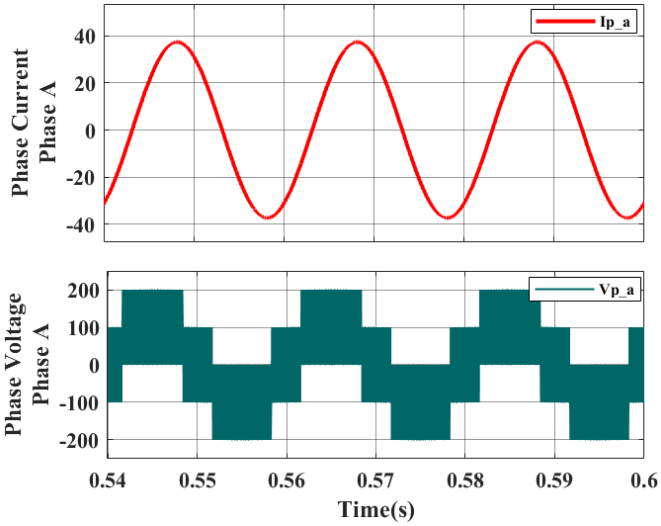

Figure 5: Phase A – Phase voltage and current

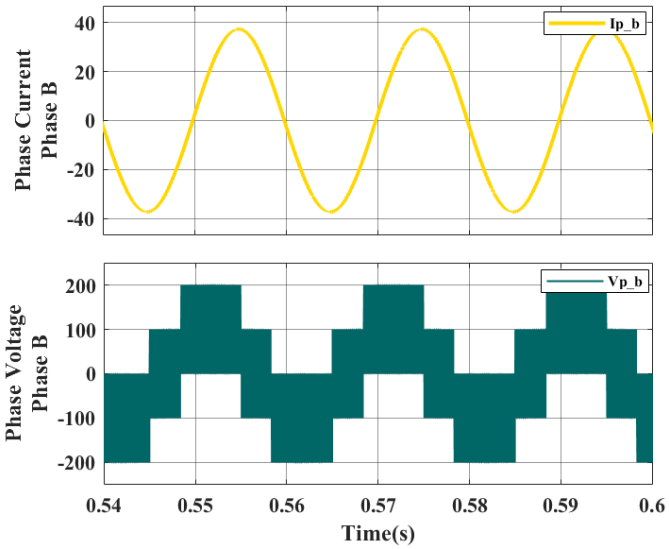

Figure 6: Phase B – Phase voltage and current

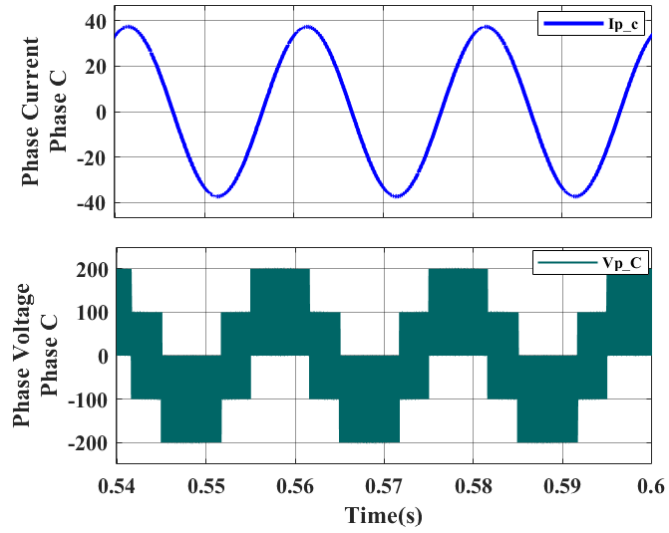

Figure 7: Phase C – Phase voltage and current

- **Phase Voltage and Current Waveform Characteristics** The following observations are derived from the phase voltage and current waveforms shown in Figures 5 - 7.
  - **Balanced Operation:** Phase currents in Phases A, B, and C are sinusoidal with equal magnitudes and a 120° phase displacement.
  - **Voltage–Current Characteristics:** Phase voltages exhibit PWM-modulated quasi-square waveforms due to high-frequency PWM switching, while the RL load filters these components to produce smooth sinusoidal current waveforms, confirming proper SPWM operation.
  - **Relevance to Machine Learning:** Stable voltage and current waveforms yield consistent residuals, enabling reliable feature extraction and robust ML-based fault classification.

IV. Residual Current Computation [3], [5]

The Figure 8 shows the methodology for the fault detection.

- **Why residual current is used:** Residual current serves as a fault detection signal. By comparing actual & predicted currents, deviations indicate abnormalities such as inverter malfunctions, faults in the line, and load changes.
- **Predictor blocks for each phase:** In a three-phase system, predictor blocks estimate each phase current using the discrete RL model based on applied voltages and system parameters.

$$i(k+1) = \left(1 - \frac{RT_s}{L}\right) i(k) + \frac{T_s}{L} v(k)$$

- **Residual Generator:** The residual generator computes the difference between the measured current waveform (obtained after discretisation with a Zero-Order Hold block) and the predicted current from the RL model.
- **Absolute residual computation:** The residual is expressed as the absolute value of the difference between actual and predicted currents:

$$r(k) = |i_{\text{actual}}(k) - i_{\text{predicted}}(k)|$$

This ensures that both positive and negative deviations are treated uniformly.

V. Feature Extraction Methodology [3]

A. Windowing and Buffering Concepts

- **Window size:** Each analysis window spans 20 ms of signal duration, capturing segments of data for accurate feature extraction. If the sampling frequency is f_s, then the number of samples per window is:

$$N = f_s \cdot 0.020$$

- **Overlap:** Successive windows overlap by 50%, i.e. half the samples are reused. This reduces information loss. The step size (hop length) is:

$$\text{Step} = \frac{N}{2}$$

- **Sliding window approach:** First window: samples $[1, N]$, Second window: samples $[N/2+1, 3N/2]$, Third window: samples $[N+1, 2N]$ and so on. This ensures continuity.
- **One ML decision per window:** For each 20 ms window, one feature vector is extracted and passed to the machine learning model, yielding one decision output, making it simpler to analyse.
- **Advantage of overlapping windows:** Overlap provides smoother tracking of signal changes, reduces abrupt transitions between decisions, and increases robustness of the machine learning model.

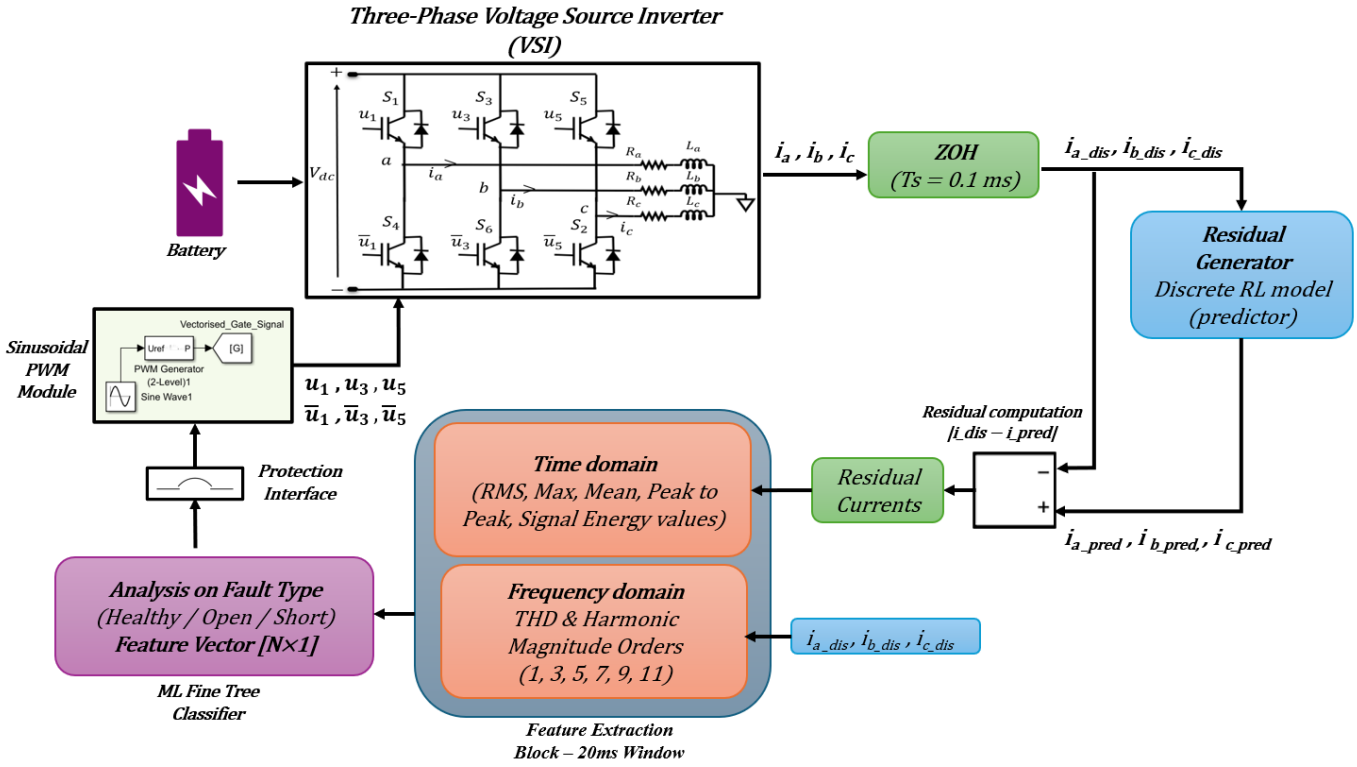

Figure 8: Fault detection in a three-phase Voltage Source Inverter (VSI). The battery, Sinusoidal PWM module, and inverter form the physical system generating phase currents and voltages. These currents are sampled and compared with the Residual Generator (RL-model). Features from residuals feed a Fine Tree classifier to detect healthy, open-phase, and short-circuit faults; integrated PWM logic enables fault isolation. [3]

B.Time-Domain Features

- **Root Mean Square (RMS):**

$$\text{RMS} = \sqrt{\frac{1}{N}\sum_{n=1}^{N} x(n)^2}$$

- **Mean:**

$$\mu = \frac{1}{N}\sum_{n=1}^{N} x(n)$$

- **Peak:**

$$\text{Peak} = \max_{1\le n\le N} |x(n)|$$

- **Peak-to-Peak (P2P):**

$$\text{P2P} = \max(x(n)) - \min(x(n))$$

- **Standard Deviation:**

$$\sigma = \sqrt{\frac{1}{N}\sum_{n=1}^{N} \left(x(n) - \mu\right)^2}$$

  where μ is the mean of the signal and N is the total number of samples.
- **Energy:**

$$E = \sum_{n=1}^{N} x(n)^2$$

C. Frequency-Domain Features

- **Harmonic orders:** Magnitudes are taken at harmonic orders $1, 3, 5, 7, 9, 11$, providing insight into distortion levels and inverter performance characteristics.
- **Total Harmonic Distortion (THD):**

$$\text{THD} = \frac{\sqrt{\sum_{h=2}^{H} |X(h)|^2}}{|X(1)|}$$

  where H is the highest harmonic considered, indicating waveform quality and overall system efficiency under load.

D. Feature Vector Size

- **Total features extracted:** A total of 39 features are computed, containing both time- and frequency-domain characteristics. The feature vector is crucial as it enables effective discrimination between different operating states.
  - **Healthy condition:** Features remain within normal ranges, with stable RMS values, low THD.
  - **Short-circuit fault:** Sudden increase in energy, P2P, and RMS values; waveform distortion leads to higher THD and Abnormal harmonic content in the faulty phase line.

– **Open-circuit fault:** Reduction in RMS & energy, less harmonic components and irregular P2P values in the faulty phase line.

Feature	Explanation and Importance
Root Mean Square (RMS)	Square root of mean of squared values; shows effective signal magnitude. Important for estimating real power delivered to the load.
Mean	Arithmetic average of all signal values. Helps detect DC offset, which can affect system balance.
Peak	Maximum absolute value of the signal. Useful for checking device voltage/current limits.
Peak-to-Peak (P2P)	Difference between the highest and lowest values. Indicates full signal swing.
Standard Deviation	Square root of variance; shows how much the signal varies from the average, measuring waveform ripple.
Energy	Sum of squared values of the signal. Represents total signal power
Harmonic Magnitudes (orders 1,3,5,7,9,11)	Amplitudes of frequency components. Analysing the distortion caused by switching and load nonlinearity.
Total Harmonic Distortion (THD)	Ratio of harmonic content to fundamental amplitude. Key measure of waveform quality and inverter efficiency.
Time-Domain	Total - 6 features for each of 3 phases = 18.
Frequency-Domain	Total - Harmonics (18) + THD (3) = 21.
Total Features	39 features.

Table III: Extracted Features

VI. Feature Normalization

The extracted features exhibit different numerical values because of the combination of quantities in the time and frequency domains. Without normalisation, the accuracy of the model decreases.

- **Mean–variance normalization:** To ensure uniform feature scaling, mean–variance normalisation is applied to each feature. This process shifts it so the average is zero (centring), and resizes it so differences are measured on the same scale (unit variance).
- **Normalization parameters from training data:** The normalisation parameters, namely the mean (μ) and standard deviation (σ), are computed offline using the training dataset.
- **Normalization equation:** Each feature is normalised using the following expression:

$$x_{\text{norm}} = \frac{x - \mu}{\sigma}$$

  where x represents the raw feature value, and x_{norm} denotes the normalized feature.
- **Consistency during real-time operation:** During testing and real-time simulation, the same μ and σ values obtained from the training phase are reused. This guarantees consistency between the training and deployment stages of the machine learning model.
- **Implementation outside the ML block:** Feature normalisation is applied before the classification tree to adjust the input data for better predictions.

VII. Machine Learning Classification Tree Model

After feature extraction and normalisation, the classifier processes input feature vectors to identify inverter health conditions, distinguishing between healthy operation, open-phase failures, and short-circuit events in real-time.

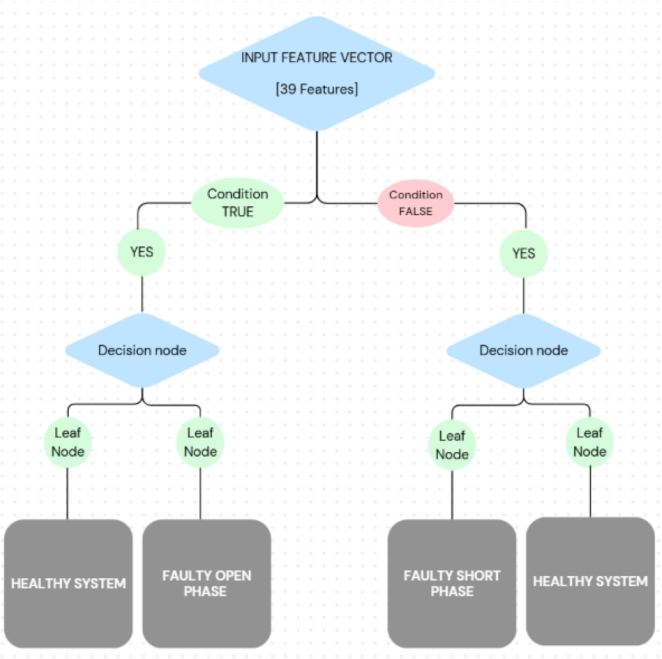

Figure 9: Machine Learning Workflow - Fine Tree Model

- **Why use a classification tree:** A classification tree is simple, fast, and interpretable, offering clear, rule-based decisions that enable reliable, real-time inverter fault protection.
- **Training the model:** The tree is trained offline with labelled inverter simulation data, where each feature vector (time window) is tagged as:

$$\textbf{Class} \in \{\textbf{Healthy}, \textbf{Open-phase}, \textbf{Short-circuit}\}$$

- **Input to the classifier:** The classifier receives a statistically normalised feature vector derived from residual current analysis, which ensures consistent feature scaling, reduces sensitivity to magnitude variations, and enables stable, reliable performance during both offline training and real-time fault classification under varying operating conditions.
- **How the tree makes decisions:** The tree splits the data step by step using learned thresholds, with each branch ending in a leaf node that represents a fault type or a healthy condition, as shown in Figure 9. **Holdout validation was performed with 25% of the data**.
- **Integration into Simulink:** The trained tree is exported & added into Simulink using the *Classification Tree Predict* block. This allows real-time fault detection in simulations without retraining.

- **Classifier output:** Model accuracy is the proportion of correctly classified cases relative to the total number of observations. For example, 90% accuracy means that 9 out of 10 inverter conditions are correctly identified, while 1 is misclassified. In this work, the classification tree achieves a high accuracy, indicating that nearly all operating states are detected with minimal error. Such high accuracy demonstrates the robustness of the proposed diagnostic framework, ensuring reliable fault detection, improved system stability under varying operating scenarios and noise conditions.

$$\text{Accuracy} = \frac{TP + TN}{TP + TN + FP + FN}$$

where TP and TN represent true positives and true negatives, and FP and FN represent false positives and false negatives. This formulation provides a quantitative measure of classifier performance, balancing correct identifications against possible misclassifications in practical applications.

Model Accuracy is around 98% – 99%

VIII. Fault Decision and PWM Protection Logic [3]

Safety logic, latching, and PWM blocking guarantee correct fault detection and secure inverter shutdown in real time. When a fault is identified, the control system blocks PWM signals to isolate the faulty phase. This fast response prevents damage to the inverter and load, ensuring reliable protection under varying conditions [3], [5].

- **Making a fault signal:** The classifier output (*Healthy*, *Open-phase*, *Short-circuit*) is converted into a `uint8` fault flag: 1 for fault, 0 for healthy, providing a simple binary interface for reliable protection logic in inverters.
- **Persistence counter:** Transient disturbances cause misclassifications. To avoid this, a persistence counter is introduced. The counter increments whenever the fault flag remains active across consecutive steps. If the system returns healthy, the counter resets until manually reset by the operator.
- **Confirming a fault:** A fault is confirmed only when the persistence counter reaches a predefined threshold N. In this work, a fault occurs at $t = 0.5\,s$ with $N = 35$, and is confirmed at approximately $t = 0.53\,s$.
- **Trip latching:** Once a fault is confirmed, the trip signal is latched. Latching ensures that the inverter remains in protection mode until a manual reset is performed.
- **PWM protection:** The latched trip signal directly blocks the PWM gate pulses. All switching signals are forced to zero, immediately shutting down the inverter. This action isolates the fault, prevents further damage to the power devices, and protects the connected load. PWM blocking is a widely adopted method in industrial drives for rapid fault isolation.
- **Note on ML after tripping:** After PWM shutdown, inverter currents drop to zero, leaving the ML classifier without valid inputs. Thus, ML evaluation applies only before tripping; afterwards, safety is ensured by latched protection until reset.

IX. Simulation Results

This section presents simulation results validating the ML-based fault detection and PWM protection scheme for a three-phase VSI. The results for healthy and faulty conditions are analysed, highlighting detection accuracy, dynamic response, robustness under disturbances, and overall effectiveness in ensuring reliable inverter operation across diverse scenarios.

A. Phase Currents

The simulation waveforms illustrate the behaviour of phase currents under different operating conditions:

- **Healthy System (Figure 10):** All three-phase currents remain balanced, equal in magnitude and sinusoidal in shape, thus clearly confirming that the inverter operates under stable, healthy conditions without distortion.
- **Open-Circuit Fault with PWM Trip (Figure 11):** When an open-phase fault occurs at $t = 0.5\,\text{s}$, the Phase-A current immediately drops to zero. This sudden loss creates an imbalance among the three phases. The persistence counter monitors this condition and confirms the fault. Once confirmed, the protection logic triggers PWM blocking, forcing all gate signals to zero.

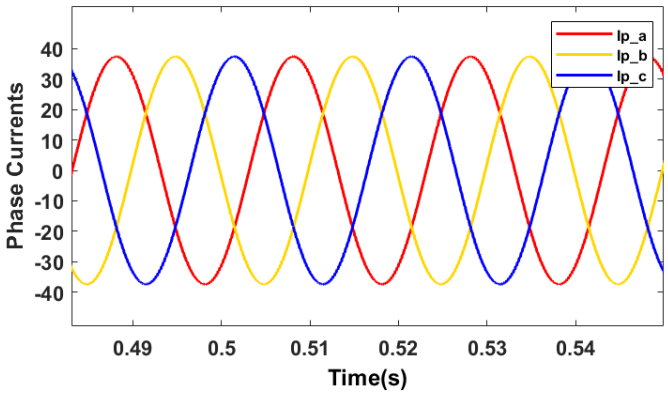

Figure 10: Phase Currents in Healthy System

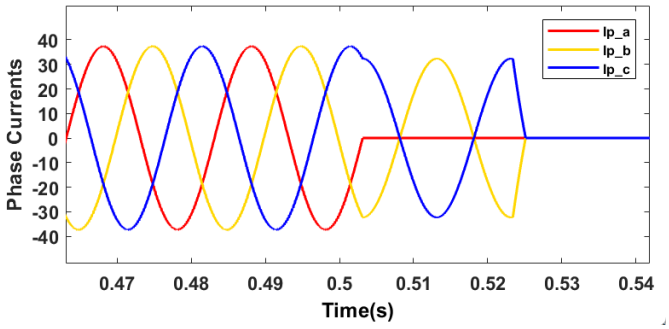

Figure 11: Phase Currents in Open-Circuit Fault with PWM Trip ($t = 0.5\,\text{s}$)

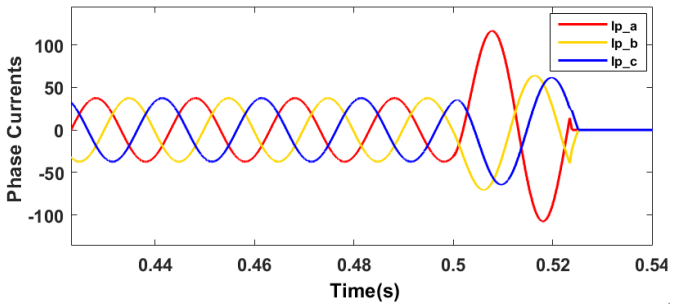

Figure 12: Phase Currents in Short-Circuit Fault with PWM Trip ($t = 0.5\,\text{s}$)

- **Short-Circuit Fault with PWM Trip (Figure 12):** When a short-circuit fault occurs at $t = 0.5\,\text{s}$, the Phase-A current rises sharply, producing a severe distortion and imbalance among the three phases. The persistence counter monitors this abnormal surge and confirms the fault after consecutive detections. Once confirmed, the protection logic triggers PWM blocking, forcing all gate signals to zero and safely shutting down the inverter.

B. PWM gate signals

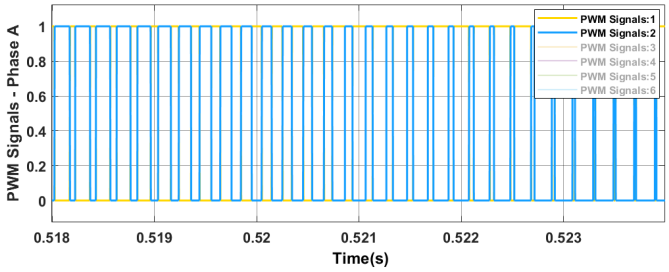

Figure 13: Phase A PWM Signal in Healthy Condition

The simulation waveforms illustrate the behaviour of Phase-A PWM signals before and after the fault.

- **Healthy Operation (Figure 13)** - PWM signals maintain proper inverter switching, producing balanced sinusoidal three-phase currents and confirming stable, disturbance-free operation.
- **Fault Response (Figure 14)** - At $t = 0.53\,\text{s}$, the persistence counter confirms a fault following the ML decision. The protection logic then blocks the PWM signals, shutting down the inverter, switching to safely isolate the system and protect the connected load from damage.

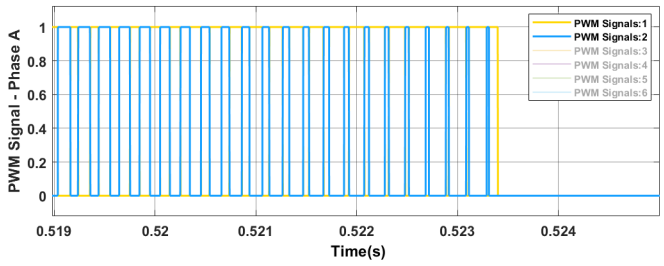

Figure 14: PWM signals after fault at $t = 0.5\,\text{s}$

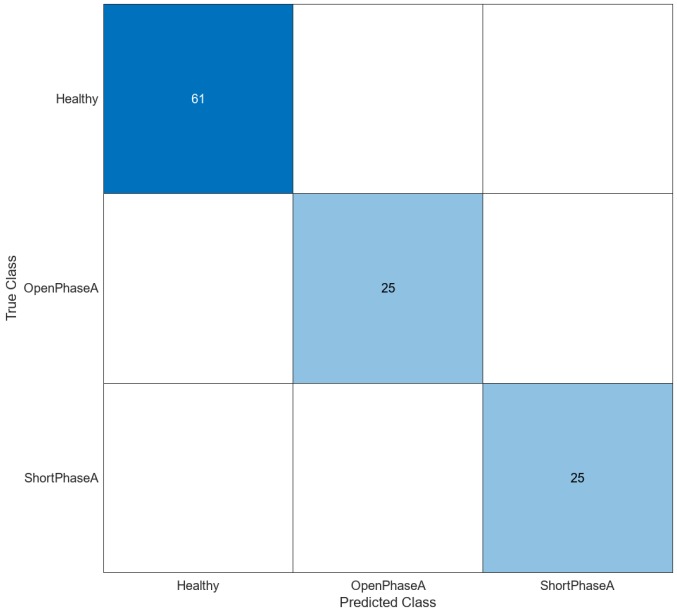

Figure 15: Fine Tree Model - Validation Confusion Matrix

C. ML Classification Output

Figure 15 shows the Fine Tree classifier's confusion matrix. Diagonal entries mark correct classifications, off-diagonal entries mark misclassifications. The model achieves high accuracy in distinguishing healthy, open-circuit, and short-circuit states, confirming reliable real-time inverter fault detection, thereby ensuring robust performance, improved reliability, enhanced monitoring, and consistent fault diagnosis across diverse operating conditions. Moreover, the confusion matrix highlights the classifier's robustness in minimising false alarms, which is critical for maintaining operational stability and confidence in automated protection systems.

X. Conclusion

This study presents an ML-based system for detecting faults in a three-phase Voltage source inverter. Using predictive analysis of voltage and current signals, the framework combines residual current computation, feature extraction, and classification tree models. The approach achieved 99% accuracy in identifying faults and provided PWM protection within just 3 ms post-fault. These results are important for electric vehicle (EV) powertrains, where inverter reliability is linked to safety and performance, ensuring fast, robust protection across operating scenarios, while supporting scalability, adaptability, and efficient deployment in diverse industrial and automotive applications. Ultimately, this work bridges advanced machine learning with power electronics, setting a benchmark for intelligent, fault-tolerant inverter systems of the future.

XI. Future Scope

Based on recent advances in inverter and EV fault diagnosis, future extensions of this research may include:

- **Extension to EV subsystems:** Apply residual current–based fault detection to motor drives, battery converters, and other EV subsystems, supporting holistic powertrain reliability [6].
- **Advanced ML and hybrid models:** Explore deep learning, ensemble methods, and hybrid AI approaches to improve classification accuracy, adaptability, and resilience under varying load and noise conditions [5].
- **FPGA and embedded implementation:** Deploy the framework on FPGA hardware for real-time execution, ultra-low latency, and scalability in embedded EV applications [6].
- **Digital twin integration:** Combine the detection scheme with digital twin models for predictive monitoring, lifecycle health management, and proactive maintenance in EV powertrains [6].

References

[1] H. Liu, "Fault Diagnosis of Electronic Circuits Based on Matlab," *International Journal of Research in Engineering and Science (IJRES)*, vol. 4, no. 11, pp. 06–13, Nov. 2016.

[2] M. Tete, N. K. Ahirwar, G. R. Ratnakar, V. Chandra, M. M. Bhaduri, and A. K. Jain, "Fault Analysis of 3 Phase System in MATLAB," *International Research Journal of Engineering and Technology (IRJET)*, vol. 11, no. 11, pp. 595–597, Nov. 2024.

[3] M. Talha, F. Asghar, and S. H. Kim, "A Novel Three-Phase Inverter Fault Diagnosis System Using Three-dimensional Feature Extraction and Neural Network," *Arabian Journal for Science and Engineering*, vol. 43, no. 2, pp. 707–720, Feb. 2018, doi: 10.1007/s13369-018-3156-8.

[4] Y. Ajra, G. Hoblos, H. Al Sheikh, and N. Moubayed, "A Literature Review of Fault Detection and Diagnostic Methods in Three-Phase Voltage-Source Inverters," *Machines*, vol. 12, no. 9, p. 631, Sep. 2024, doi: 10.3390/machines12090631.

[5] Z. Pengbo, C. Renxiang, X. Xiangyang, Y. Lixia, and R. Mengyu, "Recent progress and prospective evaluation of fault diagnosis strategies for electrified drive powertrains: A comprehensive review," *Measurement*, vol. 222, p. 113711, Oct. 2023, doi: 10.1016/j.measurement.2023.113711.

[6] M. P. Kumar, S. Velpula, C. Saiprakash, and B. Sahoo, "Advancements in fault detection and diagnosis methods for electric vehicles: a review," *Discover Applied Sciences*, vol. 7, p. 1235, 2025, doi: 10.1007/s42452-025-07758-9.

[7] M. Talha, F. Asghar, and S. H. Kim, "A Matlab and Simulink-Based Three-Phase Inverter Fault Diagnosis Method Using Three-Dimensional Features," *International Journal of Fuzzy Logic and Intelligent Systems*, vol. 16, no. 3, pp. 173–180, Sep. 2016, doi: 10.5391/IJFIS.2016.16.3.173.

[8] J. Francisti, K. Fodor, Z. Balogh, and M. Magdin, "Predictive modelling and anomaly detection in solar PV inverters using machine learning," *Results in Engineering*, vol. 28, p. 108348, Nov. 2025, doi: 10.1016/j.rineng.2025.108348.

[9] C. Wu, R. Sehab, A. Akrad, and C. Morel, "Fault Diagnosis Methods and Fault Tolerant Control Strategies for the Electric Vehicle Powertrains," *Energies*, vol. 15, no. 13, p. 4840, Jul. 2022, doi: 10.3390/en15134840.