TSMC 65nm CMOS Process – Basic Design Rules Summary

This summary provides approximate design-rule values for the TSMC 65nm Low-Power (LP) process for educational and reference purposes. Exact values depend on foundry variant and PDK release.

Layer / Feature	Rule	Typical Value (µm)	Notes
Poly (Gate)	Minimum width	0.07	Smallest gate length (Lmin)
Poly (Gate)	Minimum spacing	0.10	Between poly lines
Poly over Active	Extension	0.05	Poly overlap over diffusion edge
Active (Diffusion)	Minimum width	0.10	Smallest diffusion region
Active (Diffusion)	Minimum spacing	0.10	Between active regions
Contact (CA)	Contact size	0.08 × 0.08	Via/contact hole
Contact (CA)	Contact spacing	0.08	Edge-to-edge spacing
Metal 1	Minimum width	0.09	Local interconnect routing
Metal 1	Minimum spacing	0.09	Adjacent M1 spacing
Metal 2–6	Minimum width/spacing	0.10–0.14	Intermediate routing layers
Metal 7–9	Minimum width/spacing	0.28–0.50	Top-level and power routing
Via (V1–V8)	Size	0.08 × 0.08	Between metal layers
Via (V1–V8)	Spacing	0.08	Edge-to-edge spacing
N-Well / P-Well	Width / Spacing	0.40 / 0.40	For device isolation
Guard Ring	Width	≥ 0.50	Used for substrate isolation
Metal Density	Min / Max	20–80%	CMP planarity requirement
Antenna Ratio	Max	≈ 300–500	Gate protection rule
Current Density	Max	1–5 mA/µm	Electromigration limit (depends on layer)

■■ **Note:** Exact values and rule names (e.g. M1.W.1, POLY.S.2) are defined in the official TSMC Design Rule Manual (DRM) and are accessible only under NDA. These figures are educational approximations.