

1. Description

1.1. Project

Project Name	ADC_ContinuousConversion
Board Name	STM32F411E-DISCO
Generated with:	STM32CubeMX 6.15.0
Date	07/19/2025

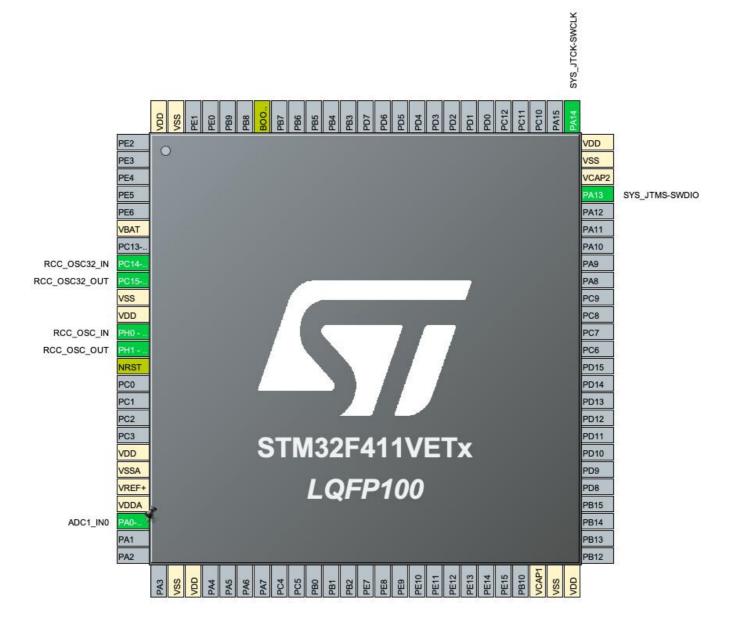
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411VETx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

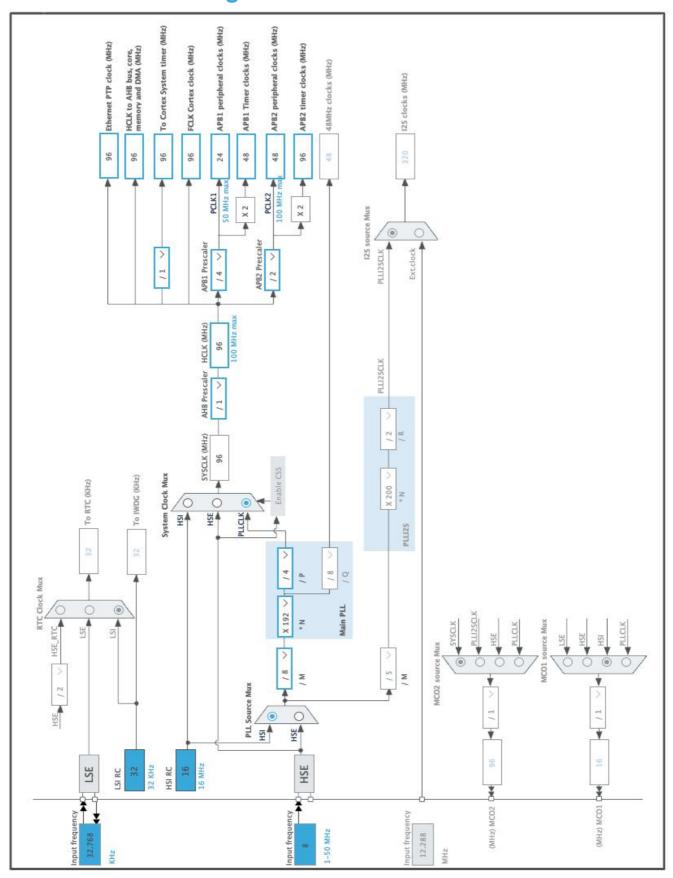
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0 - OSC_IN	I/O	RCC_OSC_IN	
13	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0	
27	VSS	Power		
28	VDD	Power		
48	VCAP1	Power		
49	VSS	Power		
50	VDD	Power		
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
94	воото	Boot		
99	VSS	Power		
100	VDD	Power		

4. Clock Tree Configuration



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1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
мси	STM32F411VETx
Datasheet	DS10314_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	1.7

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

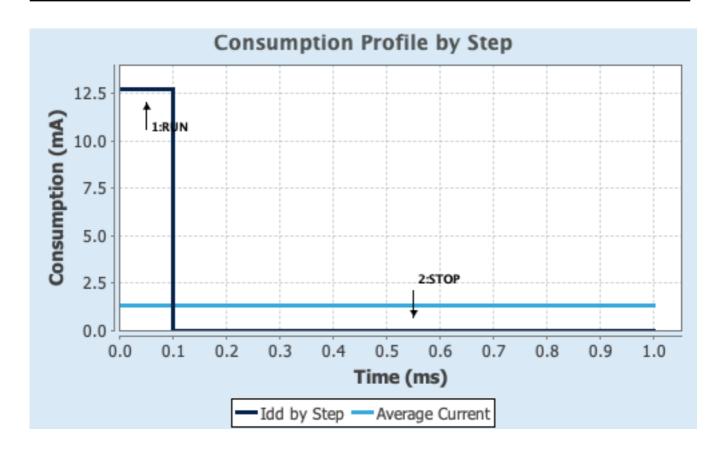
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-
		PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 μA
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	104.07	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19	Average DMIPS	125.0 DMIPS
	days, 6 hours	-	

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value	
Project Name	ADC_ContinuousConversion	
Project Folder	/Users/abdelilahelkarmoudi/Desktop/sect4/ADC_ContinuousConversion	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.2	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1 SystemClock_Config		RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1

3. Peripherals and Middlewares Configuration

3.1. ADC1 mode: IN0

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment
Scan Conversion Mode Disabled

Continuous Conversion Mode Enabled *

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Channel 0

Sampling Time 480 Cycles *

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

3.2. RCC

High Speed Clock (HSE): BYPASS Clock Source Low Speed Clock (LSE): Crystal/Ceramic Resonator

3.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled

Data Cache Enabled

Flash Latency(WS) 3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

3.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

^{*} User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1 global interrupt	unused			
FPU global interrupt	unused			

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
	sequence ordering	Handlei	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f411_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f411_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f4-svd.zip

Description

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